calculated: $R = 1/G$. For example, a resistance of 10 MΩ is measured as 0.100 μS.

Inductance and capacitance measurements may be made directly over a range of 200 μH to 200 H, and 200 pF to 2000 μF, respectively. The dissipation factor D is measured by pressing and holding in the D button while the L or C button is still selected. The directly measured inductance is the series equivalent circuit quantity L_s. The Q factor of the inductor is calculated as the reciprocal of D:

$$Q = \frac{\omega L_s}{R_s} = \frac{1}{D} \text{ (see Section 7-4).}$$

Direct capacitance measurements give the parallel equivalent circuit quantity C_p. In this case D (for the parallel equivalent CR circuit) is:

$$D = \frac{1}{\omega C_p R_p} \text{ (see Section 7-4).}$$

When measuring low values of resistance or inductance, the connecting clips should first be shorted together and the residual R or L values noted (as indicated digitally). These values should then be subtracted from the measured value of the component. When measuring low capacitances, the connecting clips should first be placed as close together as the terminals of the component to be measured (i.e., without connecting the component). The indicated residual capacitance is noted and then subtracted from the measured component capacitance.

Return to Figure 10-13(a) and assume that a capacitor is connected in place of the inductor. The measured quantity is displayed as an inductance prefixed by a negative sign on the LCR meter in Figure 10-14. The capacitive impedance is equivalent to the impedance of the indicated inductance:

$$\omega L_s = \frac{1}{\omega C_s},$$

or

$$C_s = \frac{1}{\omega^2 L_s}.$$

For an indicated inductance of 100 mH, and a measuring frequency of 1 kHz,

$$C_s = \frac{1}{(2\pi \times 1 \text{ kHz})^2 \times 100 \text{ mH}} = 0.25 \ \mu\text{F}.$$

Similarly, inductance can be measured as capacitance when it is convenient to do so.

REVIEW QUESTIONS AND PROBLEMS

10-1. Sketch the block diagram of a time base system for a digital frequency meter. Starting with a 1-MHz crystal controlled oscillator, show the time periods of the output waveforms at various points in the system. Briefly explain.

10-2. If the time base system in Question 10-1 has the 1-MHz oscillator replaced with a 3.3-MHz oscillator, calculate the new time periods at each output terminal.

10-3. A square wave is applied to a digital frequency meter that uses a time base consisting of a 1-MHz clock generator which has its output divided by decade counters. Determine the meter indication when: (a) the square wave frequency is 5 kHz and the time base uses six decade counters, (b) the square wave frequency is 2.9 kHz and the time base uses five decade counters.

10-4. Explain the function of a latch and a display-enable control as used with a frequency counter.

10-5. Sketch the block diagram of a digital frequency meter. Also sketch the waveforms at various points in the system, and carefully explain the system operation.

10-6. A frequency meter with a stated accuracy of ±1 count ±(1×10^{-5}) is used to measure frequencies of 30 Hz, 30 MHz, and 300 MHz. Calculate the percentage measurement error in each case.

10-7. Sketch a block diagram of the input stages of a digital frequency meter arranged for reciprocal counting. Explain the system operation.

10-8. The frequency meter in Question 10-6 is rearranged for reciprocal counting. Calculate the percentage error that occurs when a 30-Hz frequency is measured on this system.

10-9. Explain how time period and frequency ratio can be measured on a digital frequency meter. Use illustrations in your explanation.

10-10. Using illustrations, discuss the need for an input amplifier/attenuator stage with a digital frequency meter. Explain the situation where (a) amplification and (b) attenuation is required to avoid errors.

10-11. Sketch the circuit of an IC op-amp Miller integrator. Briefly explain the circuit operation, and sketch input and output waveforms.

10-12. Sketch the circuit of a dual-slope integrator. Sketch the waveforms that occur at the various points throughout the circuit. Identify each part of the circuit, and carefully explain the circuit operation.

10-13. A dual-slope integrator, as shown in Figure 10-9, has a square wave input with each half-cycle equivalent to 1563 clock pulses. The clock output frequency is 1 MHz. During time t_2 (in Figure 10-10), 1000 pulses are to represent $V_i = 1$ V. Calculate the required level of reference current.

10-14. Show that small drifts in clock frequency have little effect on the accuracy of a dual-slope integrator system for use with a digital voltmeter.

8-43. Sketch the circuit of an ac electronic voltmeter using a voltage-to-current converter with full-wave rectification. Explain the operation of the circuit.

8-44. Sketch a half-bridge full-wave rectifier circuit with dc blocking capacitors, as used with an electronic voltmeter. Explain the circuit operation.

8-45. Sketch a peak detector circuit for use with a peak response electronic voltmeter. Show the voltage waveforms at the points throughout the circuit, and explain its operation. Discuss the need for the peak detector probe.

8-46. Sketch the circuit of a true rms electronic voltmeter using thermocouples. Explain the operation of the circuit.

8-47. Sketch the circuit of a true rms meter using a diode-resistor nonlinear circuit. Explain the operation of the circuit.

8-48. Two waveforms displayed on an oscilloscope have their rms values measured on three different ac voltmeters. The waveforms are: (a) a sine wave with amplitude of 20 V peak-to-peak, and (b) a pulse wave with peak voltage of 20 V, pulse width of 2 ms, and time period of 5 ms. Determine the indicated voltage for each waveform when measured on: (1) a peak response instrument, (2) a full-wave rectifier instrument, (3) a true rms voltmeter.

8-49. Sketch a circuit to show how currents can be measured on an analog electronic voltmeter. Briefly explain.

8-50. Sketch the circuit of a chopper-stabilized electronic voltmeter. Show the voltage waveforms at various points in the circuit, and explain the circuit operation.

8-51. Discuss procedures and precautions for using electronic voltmeters for measurement of: (a) voltage, (b) resistance, and (c) dB.

9

BASICS OF DIGITAL INSTRUMENTS

INTRODUCTION

Before the operation, performance, and applications of digital instruments can be studied, a basic understanding of digital counting circuits must be achieved. These involve the use of the transistor as a switch, in which it is either *on* (conducting) or *off* (not conducting). Transistors and diodes are connected to form *logic gates* and *flip flops*. The flip flop is basically a two-transistor circuit that has two states: Q_1 *on* and Q_2 *off*, or Q_1 *off* and Q_2 *on*. One flip flop may be used to count up to 2, and a cascade of four flip flops can count to 16. Four flip flops may also be connected as a decade counter or scale-of-ten. Three decade counters and one additional flip flop may be cascaded to count to 2000. As well as counting, digital circuits must be able to display the count. Seven-segment light-emitting-diode (LED) displays and liquid-crystal (LCD) displays are available for this purpose.

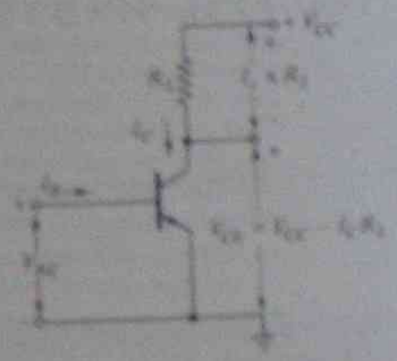
9-1 TRANSISTOR SWITCHING

The transistors in the circuits discussed in Chapter 8 all function as *linear* devices. Each transistor is biased *on*, and in every case the collector current and voltage increase and decrease linearly in relation to the base current. A transistor can also be switched *off* by providing a reverse voltage at its base-emitter junction, or simply by making the base potential equal to the emitter voltage. Similarly, a transistor can be switched *on* into a *saturated*

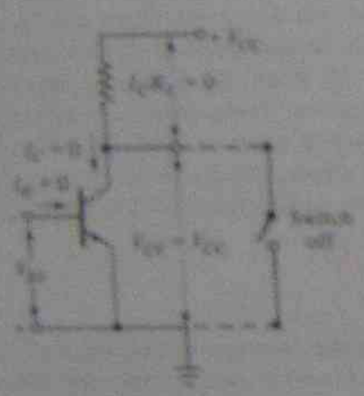
condition, where its collector-emitter voltage is held constant at a level of approximately 0.2 V. In digital circuits, transistors are usually either *on* (saturated) or *off*.

Figure 9-1(a) shows a transistor arranged to function as a switch. A load resistor R_L is connected from supply voltage V_{CC} to the transistor collector. The emitter terminal is grounded. The base-emitter voltage controls the transistor. When $V_{BE} = 0.7$ V (for a silicon transistor) the device is *on*. When $V_{BE} = 0$, or when V_{BE} is negative, the transistor is *off*. The transistor collector-emitter voltage is

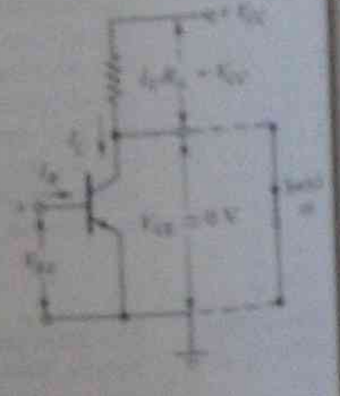
$$V_{CE} = V_{CC} - I_C R_L \tag{9-1}$$



(a) Transistor currents and voltages



(b) Transistor in *off* condition



(c) Transistor in *on* condition

FIGURE 9-1 Transistor switching.

When V_{BE} is zero (or negative) no base current flows [Figure 9-1(b)]. Since $I_C = h_{FE} I_B$ (see Section 8-1), I_C is also zero when $I_B = 0$. The transistor is *off*, there is no voltage drop across R_L, and the transistor collector-emitter voltage equals supply voltage V_{CC}. From Equation 9-1,

$$V_{CE} = V_{CC} - (0 \times R_L) = V_{CC}.$$

The transistor is switched *on* when its base-emitter junction is forward biased [Figure 9-1(c)]. Sufficient base current flows to make I_C large enough that $I_C R_L = V_{CC}$. Then Equation 9-1 gives

$$V_{CE} = V_{CC} - V_{CC} = 0 \text{ V}.$$

A practical transistor cannot have $V_{CE} = 0$ when it is biased *on*. There is always a small saturation *voltage* ($V_{CE(sat)}$):

$$V_{CE(sat)} = 0.2 \text{ V}.$$

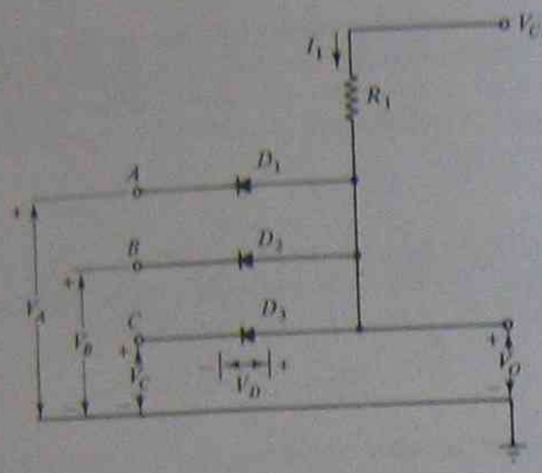
In digital applications transistors are normally either *off* or *on*, and their collector voltages are referred to as either *high* or *low*. Depending upon the supply voltage and the particular circuit, a high voltage level might be between 3 V and 6 V, while a low level might be 1 V or less. To conveniently indicate the *on-off* state of several transistors in a circuit, the high level is usually designated 1, and the low level is designated 0.

There are many important aspects of transistor switching circuits, such as switching speed, power dissipation, and maximum load current. However, an understanding of how digital instrument circuits operate can be achieved without studying these details.

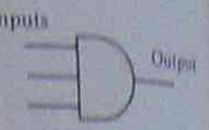
9-2 BASIC LOGIC GATES

The circuit of a diode *AND* gate with three input terminals is shown in Figure 9-2(a). If one or more of the input terminals (i.e., diode cathodes) is grounded, then the diodes are forward biased. Consequently, current I_L flows from V_{CC}, and the output voltage V_o is equal to the diode forward voltage drop V_F. Suppose the supply is $V_{CC} = 5$ V, and an input of 5 V is applied to terminal *A*, while terminals *B* and *C* are grounded. Diode D_1 is reverse biased while D_2 and D_3 remain forward biased, and V_o remains equal to V_F. If levels of 5 V are applied to all three inputs, no current flows through R_L, and $V_o = V_{CC} = 5$ V. Thus, a *high* output voltage is obtained from the *AND* gate only when high input voltages are present at input *A*, *AND* at input *B*, *AND* at input *C*. Hence the name *AND* gate.

An *AND* gate may have as few as two, or a great many input terminals. In all cases an output is obtained only when the correct input voltage level is provided simultaneously at every input terminal.



(a) Circuit diagram of AND gate

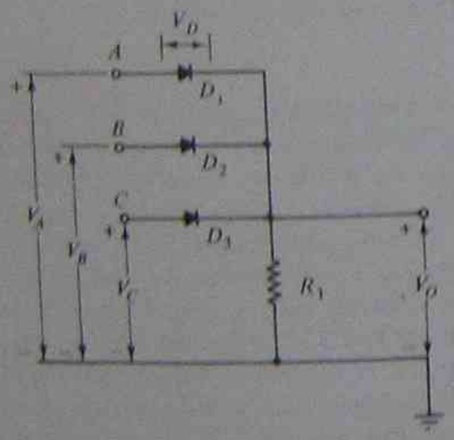


(b) Logic symbol for AND gate

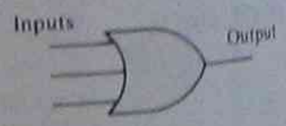
FIGURE 9-2. Circuit of a three-input diode AND gate and logic symbol for the AND gate.

Figure 9-2(b) shows the graphic symbol employed to represent an AND gate in logic system diagrams.

A three-input diode *OR* gate and its logic symbol are shown in Figure 9-3. It is obvious from the gate circuit that the output is zero when all three inputs are at ground level. If a 5-V input is applied to terminal A, diode D_1 is forward biased, and V_o becomes (5 V − V_D). If terminals B and C are



(a) Circuit diagram for OR gate



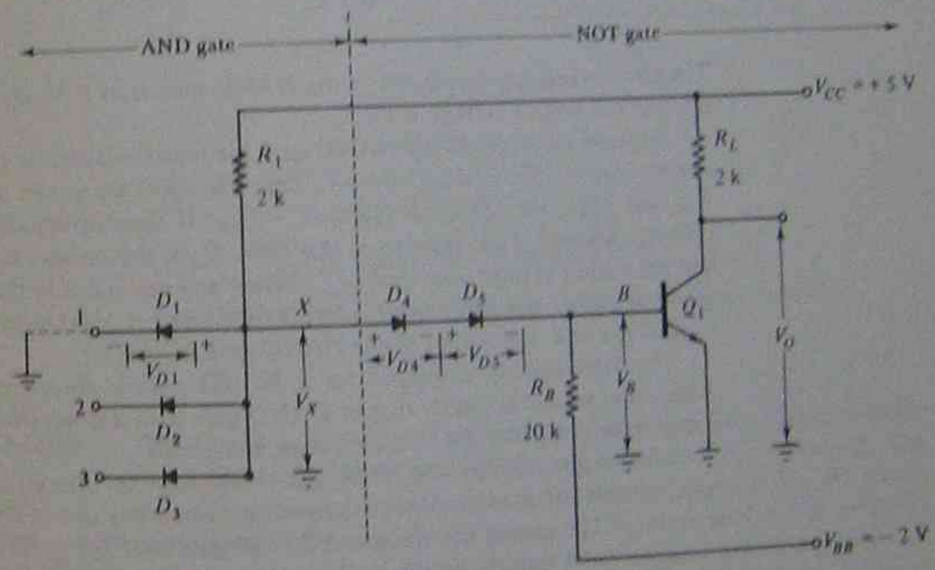
(b) Logic symbol for OR gate

FIGURE 9-3. Circuit of a three-input diode OR gate and logic symbol for the OR gate.

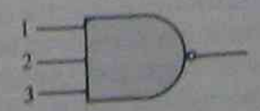
grounded at this time, diodes D_2 and D_3 are reverse biased. Instead of terminal A, the positive input might be applied to terminal B or C to obtain a positive output voltage. A *high* output voltage is obtained from an OR gate, when a high input is applied to terminal A, OR to terminal B, OR to terminal C; hence the name *OR* gate. As in the case of the AND gate, an OR gate may have only two or a great many input terminals.

As already explained, a diode AND gate has a low voltage output when one or more of its inputs are low, and a high output when all inputs are high. If a transistor is connected to invert the output of the AND gate [Figure 9-4(a)], the transistor output is *high* when one or more of the AND gate inputs are low, and *low* when all AND gate inputs are high. Used in this fashion, the inverting stage is termed a *NOT* gate. The combination of the NOT gate and the AND gate is then referred to as a *NOT-AND* gate, or *NAND* gate.

Figure 9-4(a) shows an integrated circuit *diode transistor logic* (*DTL*) NAND gate composed of a diode AND gate and a transistor *inverter*. R_1,



(a) DTL NAND gate



(b) Logic symbol for NAND gate

FIGURE 9-4. Diode transistor NAND gate and logic symbol.

D_1, D_2, and D_3 constitute the AND gate. The inverter is formed by transistor Q_1 with load resistor R_L and bias resistor R_B. When all input terminals are at ground level, the voltage at point X is the voltage drop across the input diodes (i.e., $V_x = V_D$). If diodes D_4 and D_5 were not present, V_x would be sufficient to forward bias the base-emitter junction of Q_1. The negative supply $(-V_{BB})$ keeps diodes D_4 and D_5 forward biased, so that when the inputs are at 0 V the transistor base voltage is

$$\begin{aligned} V_B &= V_x - (V_{D4} + V_{D5}) \\ &= V_{D1} - V_{D4} - V_{D5}. \end{aligned}$$

For silicon devices,

$$\begin{aligned} V_B &\simeq 0.7\text{ V} - 0.7\text{ V} - 0.7\text{ V} \\ &= -0.7\text{ V}. \end{aligned}$$

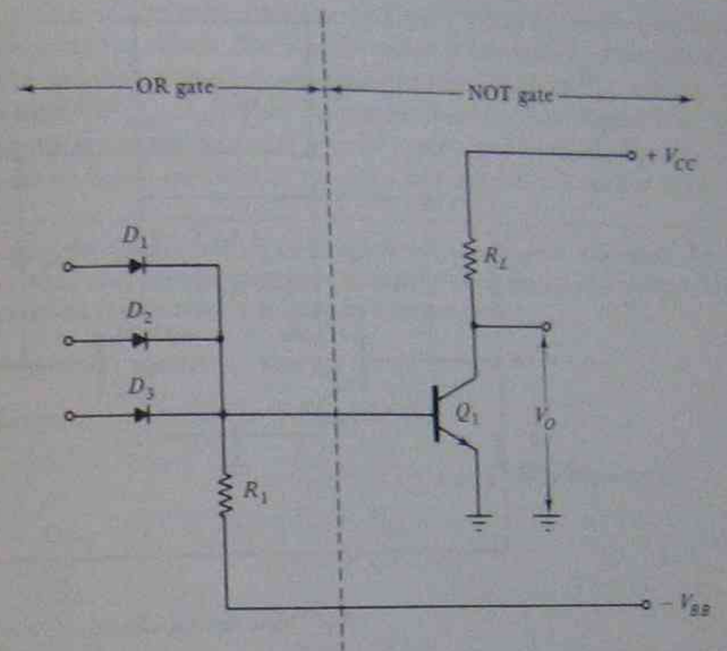
Therefore, when any one input to the NAND gate is at 0 V, Q_1 is biased off, and the output voltage is V_{CC}.

Suppose all inputs to the NAND gate are made sufficiently positive to reverse-bias D_1, D_2, and D_3. Now V_B depends upon the values of R_1 and R_B, and upon the levels of V_{CC} and $-V_{BB}$. If these quantities are all correctly selected, V_B is positive at this time, Q_1 is driven into saturation, and the output voltage goes to $V_{CE(sat)}$. When any one input to the NAND gate is at logic 0, the gate output is at 1. When input A AND input B AND input C are at 1, the output of the NAND gate is level 0.

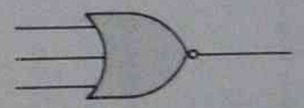
The logic symbol employed for a NAND gate is shown in Figure 9-4(b). The symbol is simply that of a AND gate with a small circle at the output to indicate that the output voltage is inverted.

A transistor inverter (or NOT gate) connected at the output of a positive logic OR gate produces a zero output when any one of the inputs is positive. The circuit is termed a *NOT-OR* gate or *NOR* gate. A diode transistor NOR gate is shown in Figure 9-5(a), with its logic symbol in Figure 9-5(b). As in the case of the NAND gate, a small circle is employed to denote the polarity inversion at the output.

The above brief introduction to logic gates refers only to *diode circuits* and DTL circuits. There are several other families of logic gates, for example, *transistor transistor logic (TTL)*, *emitter coupled logic (ECL)*, and *complementary MOSFET logic (CMOS)*. Each type has its own particular advantages and disadvantages. To study the operation of digital instruments, only an understanding of basic logic gates is required.



(a) DTL NOR gate



(b) Logic symbol for NOR gate

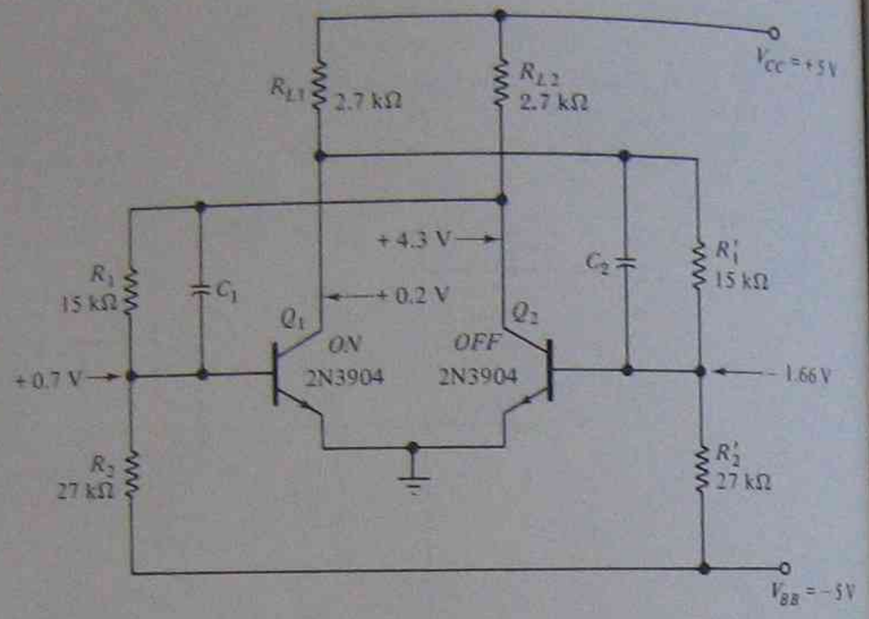
FIGURE 9-5. Diode transistor NOR gate and logic symbol.

9-3 THE FLIP-FLOP

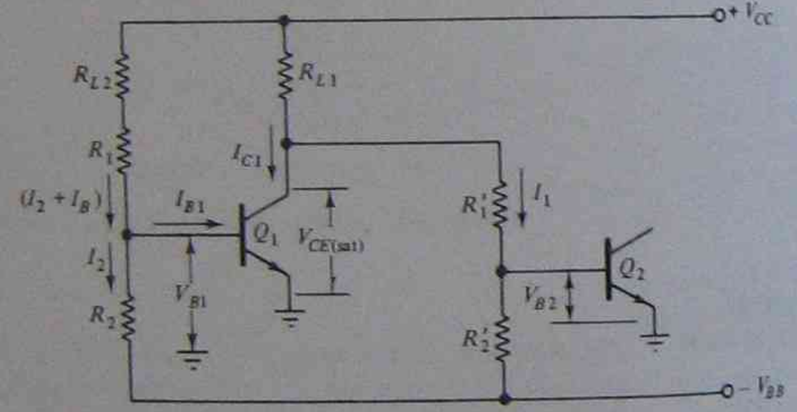
9-3-1 Circuit Operation

The *flip-flop* or *bistable multivibrator* circuit in Figure 9-6(a) has two stable states. Either Q_1 is *on* and Q_2 is *off*; or Q_2 is *on* and Q_1 is biased *off*. The circuit is completely symmetrical. Load resistors R_{L1} and R_{L2} are equal, and potential dividers (R_1, R_2) and (R_1', R_2') form similar bias networks at the transistor bases. Each transistor base is biased from the collector of the other device. When either transistor is *on*, the other transistor is biased *off*.

Consider the condition of the circuit when Q_1 is *on* and Q_2 is *off*. With Q_2 *off*, there is no collector current flowing through R_{L2}. Therefore, as shown in Figure 9-6(b), R_{L2}, R_1, and R_2 can be treated as a potential divider biasing Q_1 base from supply voltages V_{CC} and $-V_{BB}$. With Q_1 *on* in saturation, its collector voltage is $V_{CE(sat)}$, and R_1' and R_2' bias V_{B2} below ground level. Since the emitters of the transistors are grounded, Q_2 is *off*.



(a) Basic flip-flop circuit



(b) Q_1 on, Q_2 off

FIGURE 9-6. Basic circuit of flip-flop or bistable multivibrator and circuit condition when Q_1 is *on* and Q_2 is *off*.

The circuit can remain in this condition (Q_1 *on*, Q_2 *off*) indefinitely. When Q_1 is triggered *off*, Q_2 switches *on*, and remains *on* with its base biased via R_{L1}, R_1', and R_2'. At this time, the base of Q_1 is biased negatively from Q_2 collector. Thus Q_1 remains *off* and Q_2 remains *on* indefinitely. The output voltage at each collector is *high* (logic 1) when the transistor is *off*, and *low* (logic 0) when *on*.

The voltage levels indicated in Figure 9-6(a) are easily determined by analyzing the circuit. The level of collector current (I_{C1}) necessary for Q_1 to be *on* in saturation can be calculated from V_{CC} and R_{L1}. For this current to flow, $\left[h_{FE(\min)} I_{B1}\right]$ must be greater than I_{C1}, [see Figure 9-6(b)]. Also, the voltage at the base of Q_2 can be determined from R_1', R_2', and V_{BB}. V_{B2} must be below the level of the transistor emitter voltage for Q_2 to be *off*.

EXAMPLE 9-1 Using the resistor values and supply voltages shown, calculate the transistor base and collector voltages in the flip-flop circuit in Figure 9-6(a). The transistors each have a minimum current gain $h_{FE(\min)} = 70$.

SOLUTION

Assume Q_1 is on and refer to Figure 9-6(b):

$$V_{B1} = V_{BE} = 0.7 \text{ V} \text{ (for a silicon transistor)},$$

$$V_{R2} = V_{B1} - V_{BB}$$
$$= 0.7 \text{ V} - (-5 \text{ V})$$
$$= 5.7 \text{ V},$$

$$I_2 = \frac{V_{R2}}{R_2} = \frac{5.7 \text{ V}}{27 \text{ k}\Omega}$$
$$= 211 \ \mu\text{A},$$

$$V_{RL2} + V_{R1} = V_{CC} - V_{B1}$$
$$= 5 \text{ V} - 0.7 \text{ V}$$
$$= 4.3 \text{ V},$$

$$(I_2 + I_B) = \frac{V_{RL2} + V_{R1}}{R_{L2} + R_1} = \frac{4.3 \text{ V}}{2.7 \text{ k}\Omega + 15 \text{ k}\Omega}$$
$$= 243 \ \mu\text{A},$$

$$I_B = (I_2 + I_B) - I_2$$
$$= 243 \ \mu\text{A} - 211 \ \mu\text{A}$$
$$= 32 \ \mu\text{A},$$

$$I_C = h_{FE} I_B$$
$$= 70 \times 32 \ \mu\text{A}$$
$$= 2.24 \text{ mA},$$

for saturation,

$$I_{C(\min)} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_{L1}}$$
$$= \frac{5 \text{ V} - 0.2 \text{ V}}{2.7 \text{ k}\Omega}$$
$$= 1.78 \text{ mA},$$

$h_{FE}I_B > I_C(\text{min})$, *therefore* Q_1 *is saturated.*

With Q_1 *saturated,*

$$V_{C1} = V_{CE(\text{sat})} = 0.2\ \text{V}\ (\textit{as illustrated}),$$

$$V_{R'1} + V_{R'2} = V_{C1} - V_{BB}$$
$$= 0.2\ \text{V} - (-5\ \text{V})$$
$$= 5.2\ \text{V},$$

$$I_1 = \frac{V_{R'1} + V_{R'2}}{R_1' + R_2'} = \frac{5.2\ \text{V}}{15\ \text{k}\Omega + 27\ \text{k}\Omega}$$
$$= 124\ \mu\text{A},$$

$$V_{R'1} = I_1 R_1' = 124\ \mu\text{A} \times 15\ \text{k}\Omega$$
$$= 1.86\ \text{V},$$

$$V_{B2} = V_{C1} - V_{R1}$$
$$= 0.2\ \text{V} - 1.86\ \text{V}$$
$$= -1.66\ \text{V}\ (\textit{as illustrated}),$$

$$V_{BE2} = V_{B2} - V_E$$
$$= -1.66\ \text{V} - 0$$
$$= -1.66\ \text{V},\ Q_2\ \textit{is biased off.}$$

With Q_2 *off,*

$$I_{C2} = 0$$

and

$$I_{RL2} = (I_2 + I_b)$$
$$= 243\ \mu\text{A}$$

$$V_{C2} = V_{CC} - I_{RL2}R_{L2}$$
$$= 5\ \text{V} - (243\ \mu\text{A} \times 2.7\ \text{k}\Omega)$$
$$= 4.3\ \text{V}\ (\textit{as illustrated}).$$

Example 9-1 shows that the collector voltage of the *on* transistor is 0.2 V and that of the *off* transistor is 4.3 V. Also, the base voltage of the *on* transistor is 0.7 V, while that at the base of the *off* transistor is −1.66 V. Although Q_1 is shown as *on* and Q_2 as *off* in Figure 9-6, Q_2 could be *on* and Q_1 *off*.

Capacitors C_1 and C_2 in Figure 9-6(a) are equal in value and are known as *commutating capacitors* or *memory capacitors*. The voltages across C_1 and C_2 are easily determined from the collector and base voltages calcu-

lated in Example 9-1:

$$E_{C1} = V_{C2} - V_{B1}$$
$$= 4.3\ \text{V} - 0.7\ \text{V}$$
$$= 3.6\ \text{V}$$

$$E_{C2} = V_{C1} - V_{B2}$$
$$= 0.2\ \text{V} - (-1.66\ \text{V})$$
$$= 1.86\ \text{V}.$$

It can be stated that the voltage on the capacitor connected to the base of the *on* transistor is 3.6 V, and that on the capacitor connected to the base of the *off* transistor is 1.86 V. These capacitor voltage levels are important when the flip-flop is to be triggered from one state to another.

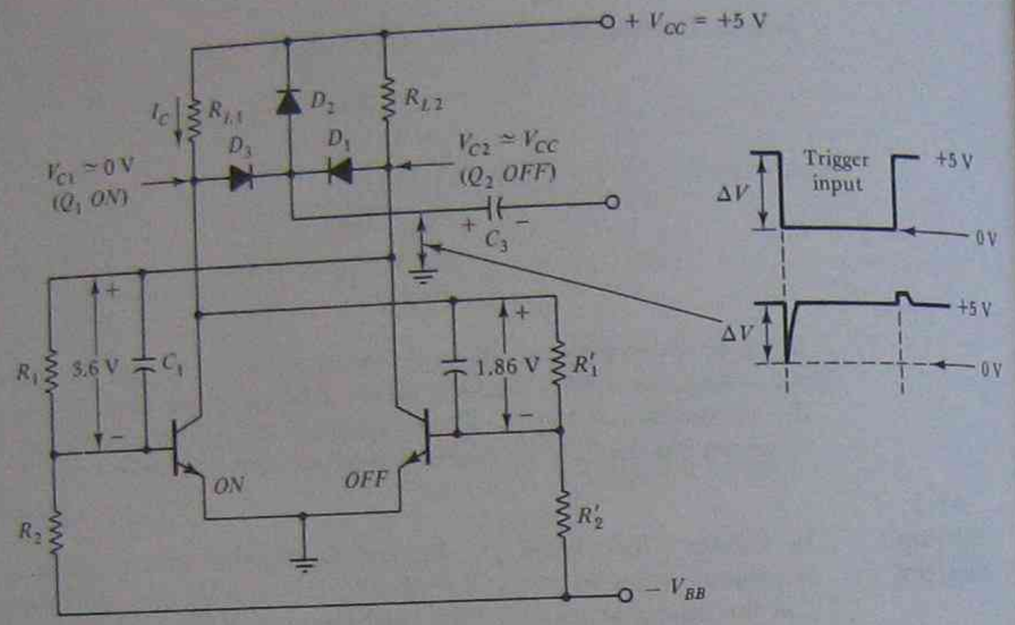
9-3-2 Flip-Flop Triggering

In Figure 9-7(a) diodes D_1, D_2, and D_3 together with capacitor C_3 constitute a *triggering circuit*. Note that Q_1 is *on* and Q_2 is *off*. This means that the voltage across C_1 is 3.6 V, and that on C_2 is 1.8 V, as determined above. Also note that the collector voltage of Q_1 is approximately zero, and that of Q_2 is approximately $V_{CC} = 5$ V. When the trigger input voltage is +5 V, D_3 is reverse biased, and D_1 and D_2 are neither forward nor reverse biased. At this time there is no charge on C_3.

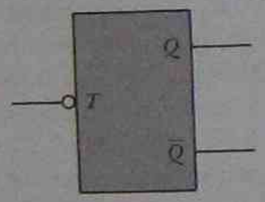
Now consider what happens when the trigger input voltage suddenly goes from +5 V to 0. The junction of the three diodes is rapidly pulled down by $\Delta V = 5$ V, as illustrated. C_3 charges quickly, so that a negative-going voltage spike actually occurs at the cathodes of D_3 and D_1 and the anode of D_2. At the peak of this spike, the cathodes of D_3 and D_1 are at 0 V. Since the anode of D_3 is at $V_{C1} = 0$ V, D_3 is *not* forward biased at this time. However, D_1 *is* forward biased when its cathode is pulled to 0 V, and it pulls the collector of Q_2 down to approximately 0.7 V above ground level. Because C_1 is connected to Q_2 collector, the base of Q_1 is pushed down to

$$V_{B1} = V_{C2} - E_{C1}$$
$$= 0.7\ \text{V} - 3.6\ \text{V}$$
$$= -2.9\ \text{V}.$$

At this instant, both Q_1 and Q_2 are biased *off*. As the spike voltage at the cathodes of D_1 and D_3 rises towards +5 V, the collector and base voltages of both transistors also rise. Because $E_{C2} = 1.86$ V and $E_{C1} = 3.6$ V, Q_2 base rises above ground before Q_1 base gets there. Thus, (the formerly *off*) Q_2 switches *on* before Q_1. As soon as Q_2 switches *on*, its collector voltage drops to approximately zero. This causes Q_1 base to be biased below ground level via R_1 and R_2.



(a) Flip-flop with a triggering circuit



(b) Logic symbol for toggled flip-flop

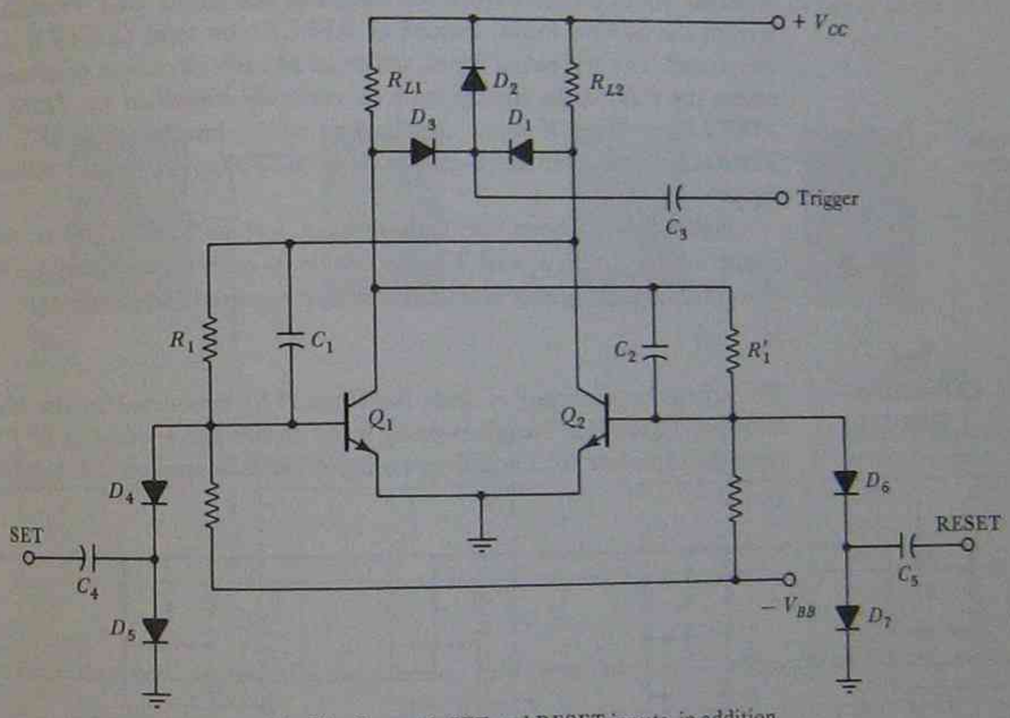
FIGURE 9-7. Triggered (or toggled) flip-flop circuit and logic symbol.

It is seen that the action of the negative-going spike causes Q_2 to switch from *off* to *on* and Q_1 to switch from *on* to *off*. When switch-over occurs, E_{C1} becomes 1.86 V and E_{C2} becomes 3.6 V. Now, another negative-going spike would switch Q_1 *on* and Q_2 *off* again. Before another negative spike can be generated C_3 must be discharged. This is done via diode D_2 as the trigger input returns to +5 V. At this instant the charge on C_3 (+ on the left, − on the right) forward biases D_2, and a *clipped* positive spike is generated, as illustrated in Figure 9-7(a).

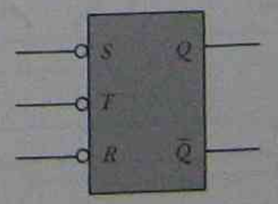
Note that the trigger input voltage levels in Figure 9-7(a) (0 V and +5 V) are the same as the flip-flop (output) collector voltages. So the triggering input can be derived as an output from a similar flip-flop circuit.

Figure 9-7(b) shows the logic symbol for a *triggered* (or *toggled*) flip-flop. The terminals identified as Q and $\bar{Q}$ are the outputs from the transistor collectors. The toggle input (T) has a small circle to indicate that negative-going inputs are required for triggering. Other flip-flops which trigger on positive-going inputs would not have a circle at the T input.

In Figure 9-8(a) two additional diodes and a capacitor are shown connected to each transistor base in the flip-flop circuit. A negative input spike applied via C_4 pulls the cathode of D_4 down and causes the base of Q_1 to be pulled below ground. Thus, Q_1 is set to its *off* condition, and



(a) Flip-flop with SET and RESET inputs, in addition to the trigger (or toggle) input



(b) Logic symbol for RST flip-flop

FIGURE 9-8. Circuit and logic symbol of *RESET-SET-TOGGLE* flip-flop.

consequently Q_2 is *on*. If Q_1 was already *off*, the input via C_4 has no effect. Similarly, a negative spike to Q_2 base via C_5 and D_6 causes Q_2 to switch *off* and Q_1 to go *on*. Once again, if the transistors were already in this condition, the input to C_5 has no effect. Diodes D_5 and D_7 (like diode D_4) discharge the capacitors when the negative inputs return to the normal levels.

When Q_1 is *off*, its collector voltage output is (*high*) logic 1, and Q_2 is *on* with its output (*low*) logic 0. If this condition is identified as a desired initial condition for the flip-flop, it is referred to as a *SET* condition. So the input terminal at C_4 is identified as the *SET* input. The other input terminal (to C_5) which resets the flip-flop out of its SET condition is termed the *RESET* input. Instead of RESET, the term *CLEAR* is sometimes used. The triggering input, which as already discussed, continuously causes the flip-flop to change state, is variously identified as: *TRIGGER*, *TOGGLE*, or *CLOCK* input. A flip-flop which has RESET, SET, and TOGGLE input terminals is known as an *RST flip-flop*, or as a *clocked SC flip-flop*.

Figure 9-8(b) shows the logic symbol for an RST flip-flop. As in Figure 9-7(b), the *R*, *S*, and *T* input terminals each have a small circle to show that negative-going input voltages are required for triggering.

9-4 COUNTING CIRCUITS

The schematic diagram of four flip-flops (FF) connected in cascade is shown in Figure 9-9. Negative-going input pulses are applied to FF 1 via coupling capacitor C_1. Each time an input pulse is applied, FF 1 changes

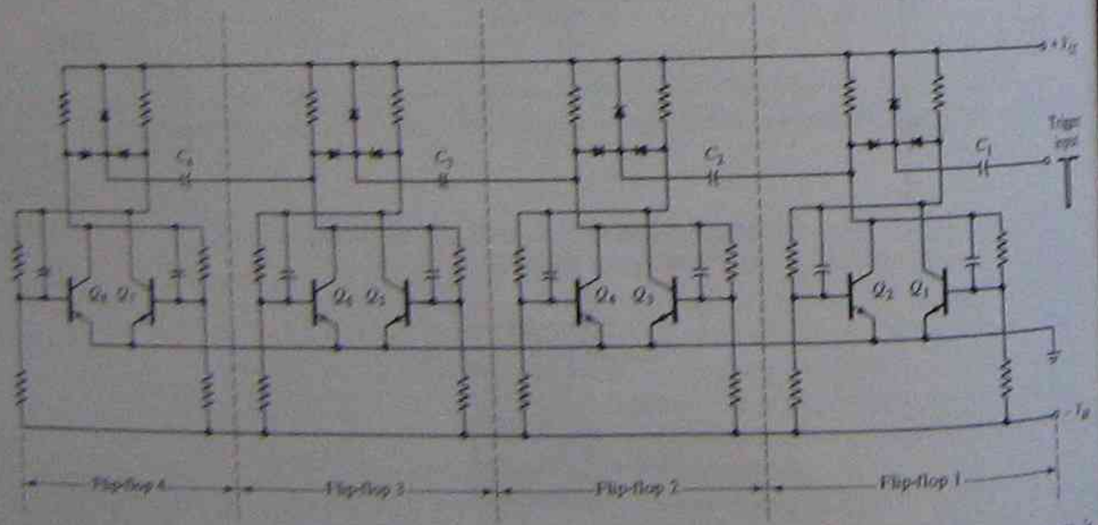


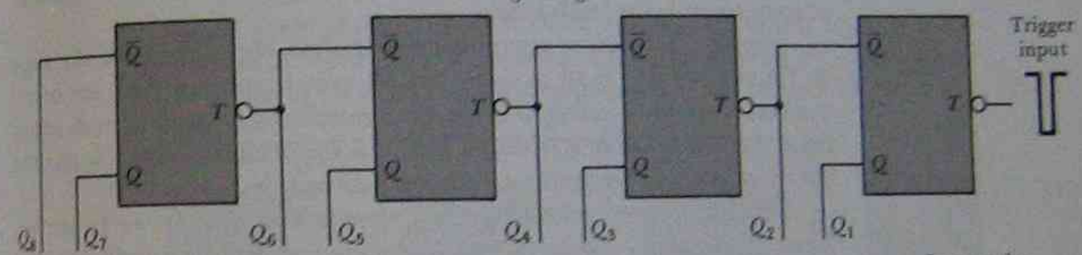
FIGURE 9-9. Four flip-flops connected in cascade. Flip-flop #2 (FF2) is triggered by the output of FF1. FF3 is triggered by FF2, and FF4 is triggered by FF3.

9-4-1 Scale-of-Sixteen Counter

state. The triggering circuit for FF 2 is coupled via capacitor C_2 to transistor Q_2 in FF 1. When Q_2 switches *off*, its collector voltage rises, applying a positive voltage step to C_2. Since a negative-going voltage is required to trigger these flip-flops (see Section 9-3), FF 2 is not affected by the positive-going voltage. When Q_2 switches *on*, its collector voltage drops, thus applying a negative voltage step to FF 2 via C_2. This negative voltage change triggers FF 2. In a similar way, FF 3 is triggered from FF 2, and FF 4 is triggered from FF 3. It is seen that each flip-flop is triggered from each preceding stage.

The four-stage cascade in Figure 9-9 is represented by the logic diagram in Figure 9-10. The various combinations of flip-flop states that

Logic Diagram



Truth Table

Q_{8C}	Q_{4C}	Q_{2C}	Q_{1C}	Input pulse count: Binary count	Input pulse count: Decimal count
0	0	0	0	0000	0
0	0	0	1	0001	1
0	0	1	0	0010	2
0	0	1	1	0011	3
0	1	0	0	0100	4
0	1	0	1	0101	5
0	1	1	0	0110	6
0	1	1	1	0111	7
1	0	0	0	1000	8
1	0	0	1	1001	9
1	0	1	0	1010	10
1	0	1	1	1011	11
1	1	0	0	1100	12
1	1	0	1	1101	13
1	1	1	0	1110	14
1	1	1	1	1111	15
1	1	1	0	0000	16

FIGURE 9-10. Logic diagram and truth table for four flip-flops in cascade or scale-of-sixteen counter.

can exist in the four-stage circuit are indicated in the *truth table* in Figure 9-10.

The state of each of the four flip-flops is best indicated by using the *binary* number system, where 0 represents a voltage at or near ground level and 1 represents a positive voltage level. When a transistor is *on*, its collector voltage is low and is represented by 0. An *off* transistor has a high collector voltage and is designated 1. In the decimal system, counting goes from 0 to 9, then the next count is indicated by 0 in the first column and 1 in the next leftward column. In the binary system, the count in all columns can go only from 0 to 1. Thus the count for 1 in both binary and decimal systems is 1. In the binary system, the count for decimal 2 is indicated by 0 in the first column and 1 in the next leftward column. So binary 10 is equivalent to *decimal 2*. The next count in a binary system is 11 and is followed by 100. The table of 0's and 1's showing the state of the flip-flops at each count is the truth table.

Suppose that, before any pulses are applied, the state of the flip-flops in Figures 9-9 and 9-10 is such that all even-numbered (i.e., left-hand) transistors are *on*. Reading only the even-numbered transistors from left to right, the binary count is 0000. At this time the decimal count is 0 and the binary count is 0. See the first horizontal column in Figure 9-10.

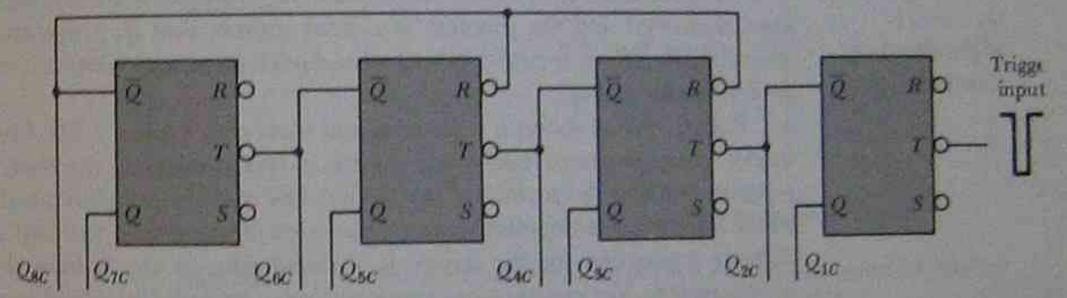
The first trigger pulse causes Q_1 to switch *on* and Q_2 to switch *off*. Thus, Q_2 reads as 1 (positive), and the binary count and decimal count are both 1 (second horizontal column in Figure 9-10). The second input trigger pulse causes FF 1 to change state again, so that Q_1 goes *off* and Q_2 switches *on*. When Q_2 switches *on*, its collector voltage goes low, applying a negative step to FF 2 which triggers Q_3 *on* and Q_4 *off*. Now the binary count is 10, and the decimal count is 2. The third input pulse triggers Q_1 *on* and Q_2 *off* once again. This produces a positive output from FF 1, which does not affect FF 2. At this time, the binary count is 11, for a decimal count of 3. The fourth trigger pulse applied to the input switches Q_1 *off* and Q_2 *on*. Q_2 coming *on* produces a negative step which causes Q_3 to go *off* and Q_4 to switch *on*. Q_4 switch-*on*, in turn, produces a negative voltage step which switches Q_5 *on* and Q_6 *off*. Now the binary count is read from the flip-flops as 100, and the decimal count is 4.

The counting process is continued with each new pulse until the maximum binary count of 1111 is reached. This occurs when 15 input pulses have been applied. The 16th input switches Q_2 *on* once more, producing a negative pulse which triggers Q_4 *on*. Q_4 output is a negative pulse which triggers Q_6 *on*, and Q_6 output triggers Q_8 *on*. Thus, the four flip-flops have returned to their original states, and the binary count has returned to 0000. It is seen that the four flip-flops in cascade have 16 different states, including the zero condition. Therefore, the circuit is termed a *scale-of-sixteen counter* or *modulus sixteen* counter.

9-4-2 Decade Counter

A *scale-of-ten counter*, or *decade counter* is produced by modifying the scale-of-sixteen circuit. Six states of the sixteen must be eliminated to leave only ten possible states. In the method shown in Figure 9-11, the first six states are eliminated leaving the last ten as the only possible circuit conditions. Note that RST flip-flops are employed, so that *reset* and *set* inputs are available. A connection is made from Q_8 (FF 4 output) to the reset terminals in FF 2 and FF 3.

The initial condition of the flip-flops in the decade counter in Figure 9-11 is binary 0110, or decimal 6 (see Figure 9-10). To obtain this condition, transistors Q_4 and Q_6 must be in the *off* state. The first input pulse changes the state of FF 1, causing Q_2 to switch *off*. Thus the collector of Q_2 becomes 1 (i.e., high positive), and the condition of the counter is 0111 (see the truth table in Figure 9-11). The second input pulse (decimal 2) again changes the state of FF 1, this time causing Q_2 to switch *on*. The output from Q_2 is a negative step which triggers FF 2, switching Q_4 *on*. This, in turn, produces a negative step which triggers FF 3 from Q_6 *off* to



Truth Table

Q_{8C}	Q_{6C}	Q_{4C}	Q_{2C}	Decimal count
0	1	1	0	0
0	1	1	1	1
1	0	0	0	2
1	0	0	1	3
1	0	1	0	4
1	0	1	1	5
1	1	0	0	6
1	1	0	1	7
1	1	1	0	8
1	1	1	1	9
Reset 0	0	0	0	10 Reset
0	1	1	0	0

FIGURE 9-11. Logic diagram and truth table for decade counter.

Q_6 *on*. The output from FF 3 triggers FF 4. Counting continues in this way, exactly as explained for the scale-of-sixteen counter, until the tenth pulse. The ninth pulse sets the counter at 1111, and the tenth pulse changes it to 0000. However, as Q_8 switches *on*, it provides the negative output step which resets FF 2 and FF 3 to put Q_4 and Q_6 *off*. The flip-flops have now returned to their initial conditions of 0110, and it is seen that the circuit has only ten different states.

Although the states of the outputs from the decade counter are represented by binary numbers, the numbers no longer correspond with the decimal count, as in the scale-of-sixteen counter. Thus, the numbers representing the outputs from the decade counter are termed *binary coded decimal* (BCD) numbers.

9-5 DIGITAL DISPLAYS OR READOUTS

9-5-1 Light-Emitting Diode Display

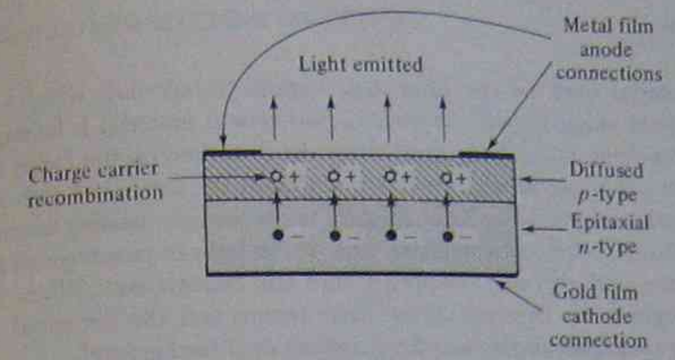
Charge carrier recombination occurs at a forward-biased *pn*-junction as electrons cross from the *n*-side and recombine with *holes* on the *p*-side. When recombination takes place, the charge carriers give up energy in the form of heat and light. If the semiconductor material is translucent, the light is emitted and the junction is a light source, that is, a *light-emitting diode* (LED). When forward biased, the device is *on* and glowing. When reverse biased it is *off*.

Figure 9-12(a) shows a cross-sectional view of a typical LED. Charge carrier recombinations take place in the *p*-type material; therefore, the *p*-region becomes the surface of the device. For maximum light emission, a metal film anode is deposited around the edge of the *p*-type material. The cathode connection for the device is a metal film at the bottom of the *n*-type region. Various types of semiconductor material are used to give red, yellow, or green light emission.

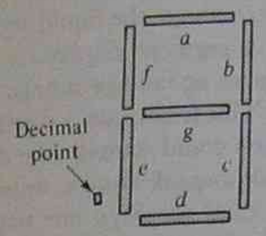
Figure 9-12(b) illustrates the arrangement of a *seven-segment* LED numerical display. Passing a current through the appropriate segments allows any numeral from 0 to 9 to be displayed. The LEDs in a seven-segment display either have all of the anodes connected together, *common anode* [see Figure 9-12(c)], or all of the cathodes connected, *common cathode*. The typical voltage drop across a forward-biased LED is 1.2 V, and typical forward current for reasonable brightness is about 20 mA. This relatively large current requirement is a major disadvantage of LED displays. Some advantages of LEDs over other types of displays are: the ability to operate from a low voltage dc supply, ruggedness, rapid switching ability, and small physical size.

9-5-2 Liquid Crystal Displays

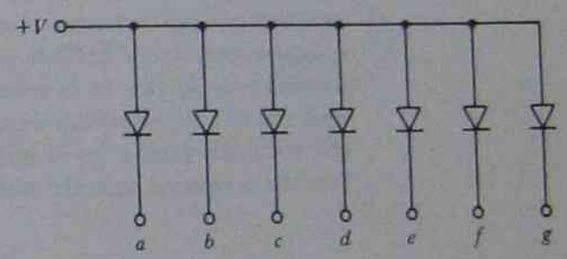
Liquid crystal cell displays (LCD) are usually arranged in the same seven-segment numerical format as the LED display. The cross-section of a *field effect* type liquid crystal cell is illustrated in Figure 9-13(a). The liquid crystal



(a) LED cross-section

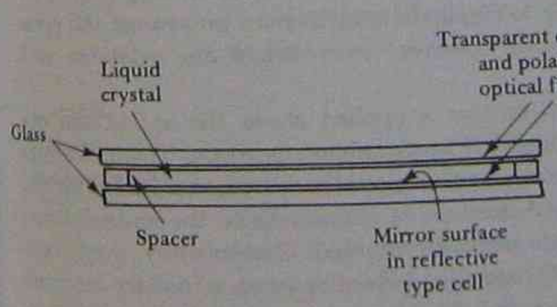


(b) LED numerical display

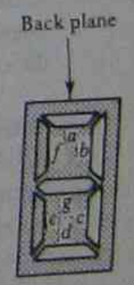


(c) Common anode circuit

FIGURE 9-12. Light-emitting diode cross-section, seven-segment numerical display, and common anode circuit of seven-segment display.



(a) Construction of liquid crystal cell



(b) Liquid crystal cell seven-segment display

FIGURE 9-13. Liquid-crystal cell construction and seven-segment display.

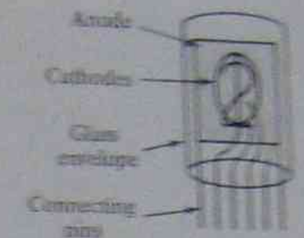
material may be one of several organic compounds which exhibit the optical properties of a crystal. Liquid crystal material is layered between glass sheets with transparent electrodes deposited on the inside faces. Two thin polarizing optical filters are placed at the surface of each glass sheet. The liquid crystal material actually twists the light passing through the cell when the cell is not energized. This allows light to pass through the optical filters, and the cell disappears into the background. When the cell is energized, no twisting of the light occurs and the energized cells in a seven-segment display stand out against their background.

Since liquid crystal cells are light reflectors or transmitters rather than light generators, they consume very small amounts of energy. The only energy required by the cell is that needed to activate the liquid crystal. The total current flow through four small seven-segment displays is typically about 300 μA. However, the LCD requires an ac voltage supply, either in the form of a sine wave or a square wave. This is because a direct current produces plating of the cell electrodes which could damage the device. A typical supply for a LCD is an 8-V peak-to-peak square wave with a frequency of 60 Hz. As in seven-segment LED displays, one terminal of each cell in a liquid crystal display is commoned. In the LCD display the cell terminals cannot be identified as anodes or cathodes; the common terminal is referred to as the *back plane* [see Figure 9-13(*b*)].

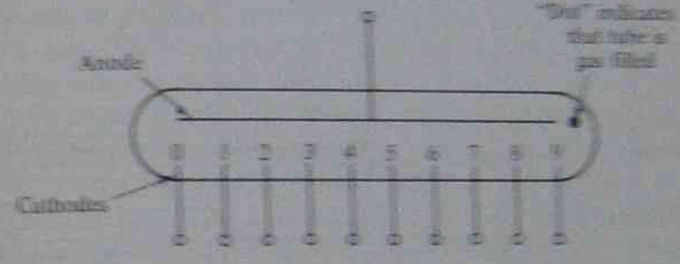
9-5-3 Digital Indicator Tube

The basic construction of a *digital indicator tube* is shown in Figure 9-14(*a*), and its schematic symbol is illustrated in Figure 9-14(*b*). A flat metal plate with a positive voltage supply functions as an anode, and there are ten separate wire cathodes, each in the shape of a numeral from 0 to 9. The electrodes are enclosed in a gas-filled glass tube with connecting pins at the bottom. Neon gas usually is employed and it gives an orange red glow when the tube is activated; however, other colors are available with different gases.

When a high enough voltage is applied across the anode and a cathode, electrons are accelerated from cathode to anode. These electrons collide with gas atoms and cause other electrons to be emitted from the gas atoms. The effect is termed *ionization by collision*. Since the ionized atoms have lost electrons, they are positively charged. Consequently, they accelerate toward the (negative) cathode, where they cause secondary electrons to be emitted when they strike. The secondary emitted electrons cause ionization and electron-atom recombination in the region close to the cathode. This results in energy being released in the form of light and produces a visible glow around the cathode. Since the cathodes are in the shape of numerals, a glowing numeral appears depending upon which cathode is energized.



(*a*) Construction



(*b*) Schematic symbol

FIGURE 9-14 Digital indicator tube, construction, and schematic symbol.

High supply voltages (140 to 200 V) are required for these tubes, and in general they are much bulkier than comparable seven-segment devices. Gas discharge displays are also available in seven-segment format comparable in size to LED displays.

9-6 DISPLAY DRIVERS

As already explained, the state of a decade counter is read in binary form by identifying each collector voltage as either 1 (high) or 0 (low). For display purposes it is necessary to convert the binary output to decimal form. In Figure 9-15 the various states of the decade counter are reproduced from Figure 9-11. In Figure 9-11, only the states of the even-numbered transistors are shown. In Figure 9-15 the states of the odd-numbered transistors are also shown alongside the even-numbered transistor states. The corresponding decimal count of input pulses to the decade counter is also shown.

The lower portion of Figure 9-15 shows ten NAND gates (see Section 9-2) each of which has its output connected to one cathode of a digital

Voltage levels at collectors									Decimal count
0	1	1	0	1	0	0	1		0
0	1	1	0	1	0	1	0		1
0	1	1	0	1	0	1	0		2
1	0	0	1	0	1	1	0		3
1	0	0	1	0	1	1	0		4
1	0	0	1	1	0	0	1		5
1	0	0	1	1	0	1	0		6
1	0	1	0	0	1	0	1		7
1	0	1	0	0	1	1	0		8
1	0	1	0	1	0	0	1		9
1	0	1	0	1	0	1	0		

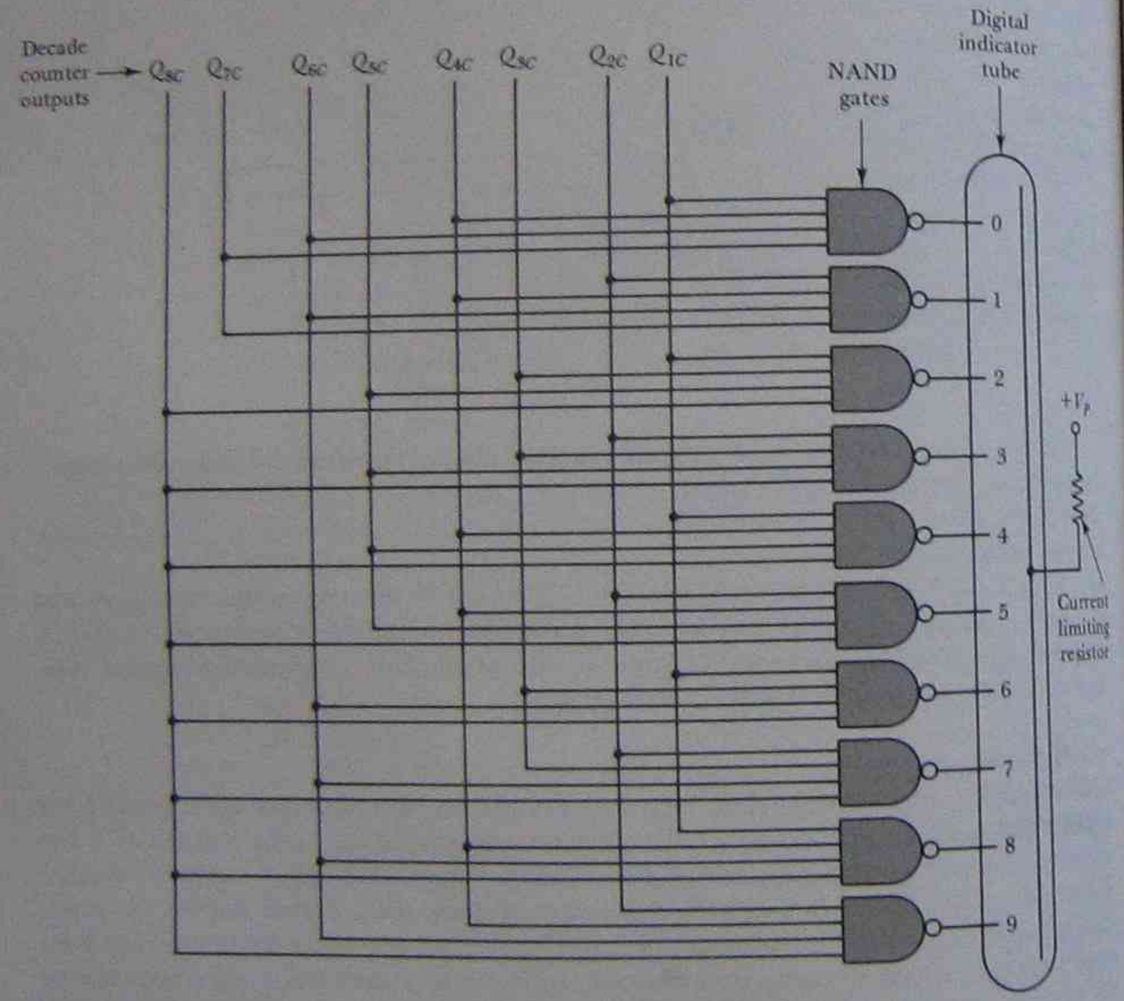


FIGURE 9-15. Logic diagram of display decoder/driver to control digital indicator tube from outputs of decade counter; binary-coded-decimal to decimal conversion.

indicator tube. The four inputs of each NAND gate are connected to the outputs of the decade counter. The input terminal connection arrangement is different for each NAND gate. A positive supply voltage is connected to the anode of the digital indicating tube. When the output of a NAND gate is low (near ground level), current flows through the tube and the grounded cathode glows. As will be seen, only one NAND gate has a low output at any time.

Consider the collector voltage levels in Figure 9-15 for a decimal count of zero. *All* the transistor collector levels, Q_8 to Q_1, are read as: 01 10 10 01. Now look at the inputs to the NAND gate connected to cathode 0 in the digital indicator tube. The inputs of gate 0 are connected to Q_{7C}, Q_{6C}, Q_{4C}, and Q_{1C}. All of these collectors are at high (logic 1) levels. Thus all four inputs to gate 0 are *high*, and consequently the output of this NAND gate is *low*. The 0 cathode in the digital indicator tube is glowing, indicating that the decimal count is zero.

For a correct 0 indication, all other gates (1 through 9) must have high output levels, so that only cathode 0 is energized. To check that this is the case, it is only necessary to identify one low input to each of gates 1 through 9. Gates 1, 3, 5, 7, and 9 each have one input connected to Q_{2C}. Since Q_{2C} is low, all of these gates have a high output. Gates 2 and 6 each have low input from Q_{3C}, gate 4 has a low input from Q_{5C}, and gate 8 has a low input from Q_{8C}. Therefore, only gate 0 has a low output, and only cathode 0 glows.

A careful examination of the gate input conditions for any particular decimal count shows that only the correct cathode is energized. For example, at a decimal count of 5, only gate 5 produces a low output to energize cathode 5. All other gates have *high* outputs at this time.

The NAND gate system illustrated in Figure 9-15 converts the BCD outputs from the decade counter to a decimal output. Thus it can be termed *BCD to decimal* conversion. Conversion of the decade counter outputs to drive a seven-segment display is termed *BCD to seven-segment* conversion, and it is a little more complex than BCD to decimal conversion.

9-7 SCALE-OF-2000 COUNTER

One decade counter together with a digital display and the necessary conversion circuitry can be employed to count from 0 to 9. Each time the tenth input pulse is applied, the display goes from 9 to 0 again. When this occurs, the output of the final transistor in the decade counter goes from 1 to 0 (see Figure 9-11). This is the only time that the final transistor produces a negative-going output, and this output can be used to trigger another decade counter.

Consider the block diagram of the *scale-of-2000* counter shown in Figure 9-16. The system consists of three complete decade counters and

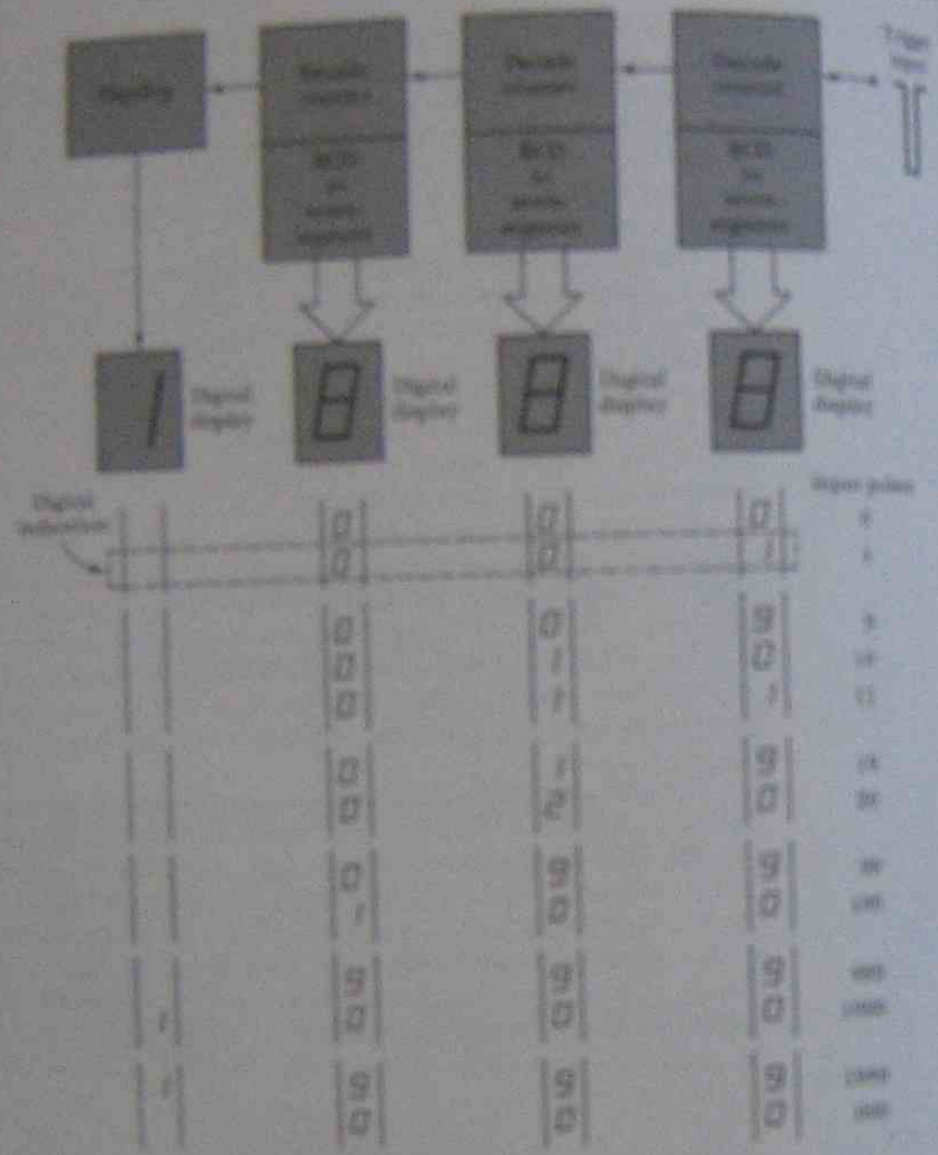


FIGURE 9-16. Scale-of-2000 counter.

displays, and one flip-flop controlling a display which indicates as numeral 1 when on. Starting from 0, all three counters are at the normal starting conditions, and the numeral 1 indicator is off. This gives an indication of 000. The first 9 input pulses register only on the 1s (right-hand side) display. On the tenth input pulse, the first display goes to 0, and a negative-going pulse output from the first decade counter triggers the second decade counter. The display of the second counter now registers 1, so that the complete display reads 010. The counter has counted to 10, and has also registered 10 on the display system.

The next nine input pulses cause the first counter to go from 0 to 9 again so that the display reads 019 on the 19th pulse. The 20th pulse causes the first display to go 0 again. At this time, the final transistor in the first decade counter puts out another negative pulse, which again triggers the second decade counter. The total display now reads 020, which indicates the fact that 20 pulses have been applied to the input of the first decade counter. It is seen that the second decade counter and display is counting ten's of input pulses.

Counting continues as described until the display indicates 099 after the 99th input pulse. The 100th input pulse causes the first two displays (from the right) to go to 0. The second decade counter emits a negative pulse at this time, which triggers the third decade counter. Therefore, the count reads 100. On the 1000th pulse, the first three decade counters go from 999 to 000, and the negative pulse emitted from the third decade counter triggers the flip-flop and turns on the 1 display. The display now reads 1000. It is seen that the system shown in Figure 9-16 can count to a maximum of 1999. One more pulse causes the display to return to its initial 000 condition. The three components of the display which indicate up to 999 are referred to as a *three-digit display*. With the additional 1 component included, the complete numerical display is termed a *3½ digit display*.

REVIEW QUESTIONS AND PROBLEMS

9-1. Sketch a circuit to show an npn transistor employed as a switch. Identify the *on* and *off* voltage polarities and typical voltage levels at the base-emitter and at the collector-emitter terminals. Briefly explain.

9-2. A transistor connected as in Figure 9-1(a) has $V_{CC} = 9$ V, $R_L = 3.3$ kΩ, $h_{FE} = 50$. Calculate the level of V_{CE}: (a) when $I_B = 0$, (b) when $I_B = 25$ μA, and (c) when $I_B = 54.5$ μA.

9-3. Sketch the circuit and logic symbol of a four-input diode AND gate. Explain the operation of the circuit.

9-4. Sketch the circuit and logic symbol of a two-input diode OR gate. Explain the circuit operation.

9-5. Sketch the circuit and logic symbol of a three-input DTL NAND gate. Explain the operation of the circuit.

9-6. Sketch the circuit and logic symbol of a three-input DTL NOR gate. Explain the operation of the circuit.

9-7. Sketch the circuit of a flip-flop using two npn transistors. Carefully explain the conditions that keep one transistor *on* and the other one *off*.

9-8. A transistor flip-flop, as shown in Figure 9-6, has the following components and supply voltage: $R_{1A} = R_{1B} = 4.7$ kΩ, $R_1 = R_C =$

27 kΩ, $R_2 = R_2' = 40$ kΩ, $h_{FE(min)} = 110$, $V_{CC} = \pm 9$ V. Calculate the transistor base and collector voltages.

9-9. For the circuit described in Question 9-8, calculate the voltage across each of the commutating capacitors. Explain the function of these capacitors.

9-10. Sketch a circuit to show how a flip-flop may be triggered (or toggeled) continuously by input pulses. Explain the triggering circuit operation.

9-11. Sketch a circuit to show how a flip-flop may be set and reset by different inputs. Explain the operation of the circuit.

9-12. Sketch the logic symbols for a toggeled flip-flop and for an RST flip-flop.

9-13. Sketch the logic diagram and truth table for a scale-of-16 counter. Explain the operation of the system.

9-14. Sketch a logic diagram and truth table for a decade counter. Explain the operation of the system. Define *binary-coded decimal*.

9-15. Sketch the cross-section of a light-emitting diode. Explain its operation. Sketch a LED seven-segment display. Explain common-cathode and common-anode type LED displays.

9-16. Sketch the cross-section of a liquid crystal cell, and briefly explain its operation. Sketch a seven-segment liquid crystal display. Discuss the supply requirements for liquid crystal displays, and compare LCD and LED displays.

9-17. Sketch the construction of a digital indicator tube. Explain its operation, and discuss its supply voltage requirements.

9-18. Sketch the logic diagram of a display decoder/driver for controlling a digital indicator tube from a decade counter. Explain the operation of the system.

9-19. Sketch a block diagram for a scale-of-2000 counter. Explain the operation of the system. Show how the system should be modified to count up to: (a) 20 000, (b) 9999. Define $3\frac{1}{2}$ digit display.

10

DIGITAL INSTRUMENTS

INTRODUCTION If a pulse waveform is fed to the input of a digital counter for a time period of exactly one second, the counter indicates the frequency of the waveform. Suppose the counter registers 1000 at the end of a second; then the frequency of the input is 1000 pulses per second. Essentially, a *digital frequency meter* is a digital counter combined with an accurate timing system.

A dc voltage can be converted to a time period which is directly proportional to the voltage. This time period can be measured digitally and the output read as a voltage. Direct current, resistance, and alternating quantities can all be converted into dc voltages for digital measurement. Inductance and capacitance can also be measured digitally.

10-1 TIME BASE

A block diagram and voltage waveforms of a typical time base circuit for a digital frequency meter are shown in Figure 10-1. The source of time interval over which input pulses are counted is a very accurate crystal-controlled oscillator usually referred to as a *clock source*. The crystal is often enclosed in a constant temperature *oven* to maintain a stable oscillation frequency.

The output frequency from the final flip-flop of a decade counter is exactly one-tenth of the input triggering frequency. This means that the time period of the output waveform is exactly ten times the time period of

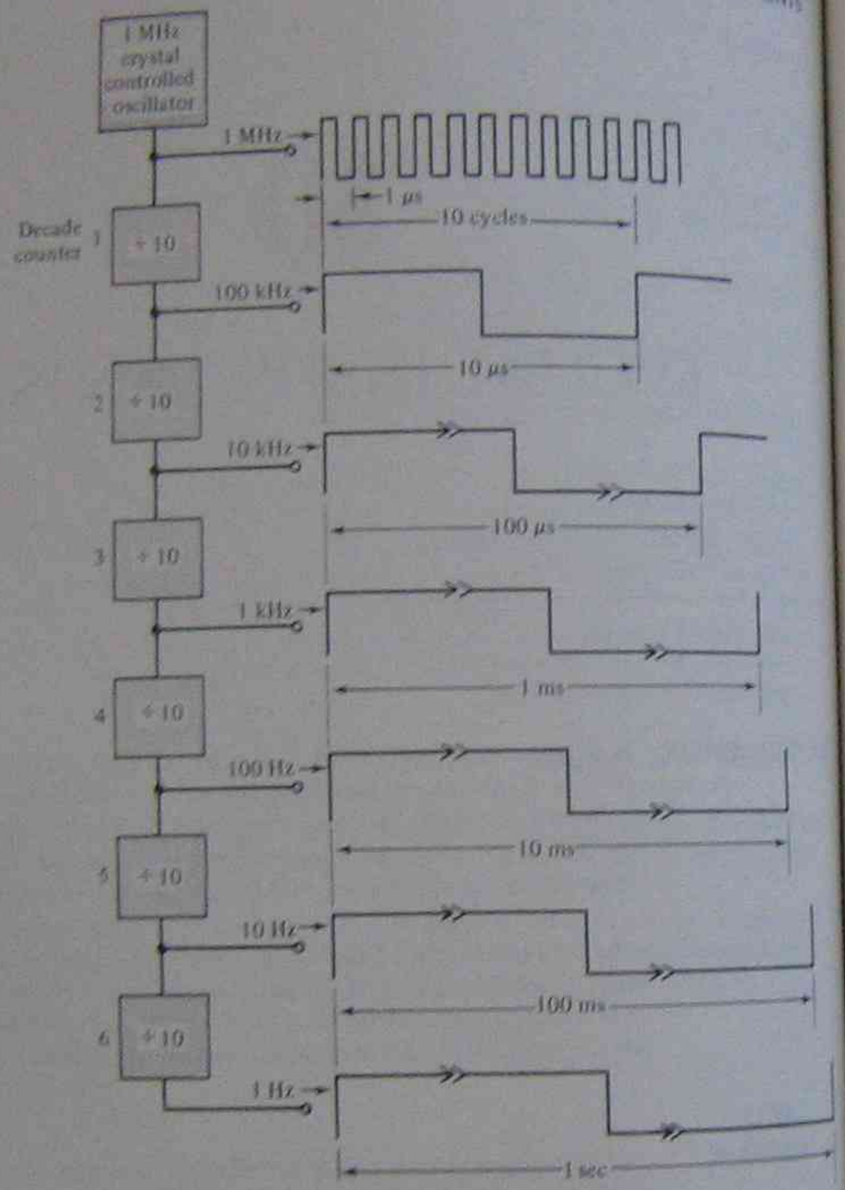


FIGURE 10-1. Time base generation for digital frequency meter.

the input waveform. The 1-MHz output from the crystal oscillator in Figure 10-1 has a time period of 1 μs, and the output waveform from the first decade counter (triggered by the 1-MHz oscillator) has a time period of 10 μs. The time period of the output from the second decade counter (triggered by the output of the first decade counter) is 100 μs, and that from the third decade counter is 1 ms, etc. With all six decade counters, the

available time periods are 1 μs, 10 μs, 100 μs, 1 ms, 10 ms, 100 ms, and 1 sec.

When the counting circuits in a digital frequency meter are triggered for a period of exactly 1 sec, the display registers the input frequency directly. A count of 1000 cycles over the 1-sec period represents a frequency of 1000 Hz or 1 kHz; a 5000 display indicates 5000 Hz, etc. These figures are more easily read when a decimal point is placed after the first numeral and the output is identified in kilohertz. Thus a display of 1.000 is 1 kHz, 5.000 is 5 kHz, and 5.473 is 5.473 kHz. In an LED display, the decimal point is created by use of a single suitably placed light-emitting diode. Also, a *kHz* indication usually is displayed.

Now consider the effect of using the 100-ms time period to control the counting circuits. A display of 1000 now means 1000 cycles per 100 ms. This is 10 000 cycles per sec or 10 kHz. When the time period is switched from 1 sec to 100 ms, the decimal point is also switched from the first numeral to a position after the second numeral. The 10.00 display is now read as 10.00 kHz; 50.00 is read as 50.00 kHz, etc.

When the time period is switched to 10 ms, the decimal point is moved to a new position after the third numeral on the display. A 100.0 display now becomes 100.0 kHz. Since this is the result of 1000 cycles of input counted over a period of 10 ms, the actual input frequency is 1000/10 ms, that is, 100 kHz. With a 1-ms time period, a display of 1000 indicates 1000 cycles during 1 ms, or 1 MHz. The decimal point is now moved back to its original position after the first numeral, and a *MHz* indication is displayed. Therefore, the display of 1.000 with a 1-ms time base is read as 1.000 MHz. If the 100-μs and 10-μs time periods are used, the decimal point is again moved so that the 1000 indication becomes 10.00 MHz and 100.0 MHz, respectively.

EXAMPLE 10-1 A 3.5-kHz sine wave is applied to a digital frequency meter. The time base is derived from a 1-MHz clock generator frequency divided by decade counters. Determine the meter indication when the time base uses (a) six counters. Determine the meter indication when the time base uses (b) four decade counters.

SOLUTION

a. When six decade counters are used:

$$\textit{time base frequency} = f_1 = \frac{1 \text{ MHz}}{10^6} = 1 \text{ Hz},$$

$$\textit{time base} = t_1 = \frac{1}{f_1} = \frac{1}{1 \text{ Hz}} = 1 \text{ sec}$$

$$\left.\begin{matrix}\textit{cycles of input} \\ \textit{counted during } t_1\end{matrix}\right\} = (\textit{input frequency}) \times t_1$$

$$= 3.5 \text{ kHz} \times 1 \text{ sec}$$

$$= 3500.$$

b. When four decade counters are used:

$$\text{time base frequency} = f_2 = \frac{1\text{ MHz}}{10^4} = 100\text{ Hz},$$

$$\text{time base} = t_2 = \frac{1}{f_2} = \frac{1}{100\text{ Hz}} = 10\text{ ms},$$

$$\left.\begin{matrix}\text{cycles of input} \\ \text{counted during } t_2\end{matrix}\right\} = \text{input frequency} \times t_2$$

$$= 3.5\text{ kHz} \times 10\text{ ms}$$

$$= 35.$$

10-2 LATCH AND DISPLAY ENABLE

If the numerical display devices in a digital frequency meter are controlled directly from the counting circuits, the display changes rapidly as the count progresses from zero. Suppose the input pulses are counted over a period of 1 sec, and then the count is held constant for 1 sec. The display alternates between changing continuously for one second and being constant for the next second. Therefore, the display is quite difficult to read, and the difficulty is increased when shorter time periods are employed for counting. To overcome this problem, *latch circuits* are employed.

A *latch* isolates the display devices from the counting circuits while counting is in progress. At the end of the counting time, a signal to the latch causes the display to change to the decimal equivalent of the final condition of the counting circuits. Latch circuits are essentially additional (special kind) flip-flops connected between the outputs of a decade counter and the display decoder/driver circuitry (e.g., between the transistor collectors and the NAND gate inputs in Figure 9-15). While counting is in progress, the latch flip-flop outputs are held in a constant state. At the end of the counting time, the flip-flops are released to set the displays according to the final states of the decade counter outputs.

A *display enable* control which open-circuits the supply voltage to the display devices is sometimes used instead of a latch. The display is simply switched *off* during the counting time and *on* during the noncounting time. The (normally constant) displayed numerals are thus switched *on* and *off* continuously, with no display occurring during the counting time. When the display time and counting time are brief enough, the *on*/*off* frequency of the display is so high that the human eye sees only a constant display.

10-3 BASIC DIGITAL FREQUENCY METER SYSTEM

The block diagram of a digital frequency meter with a four-digit display is shown in Figure 10-2, and the voltage waveforms for the system are illustrated in Figure 10-3. The input signal which is to have its frequency measured is first amplified or attenuated, as necessary, and then fed to a

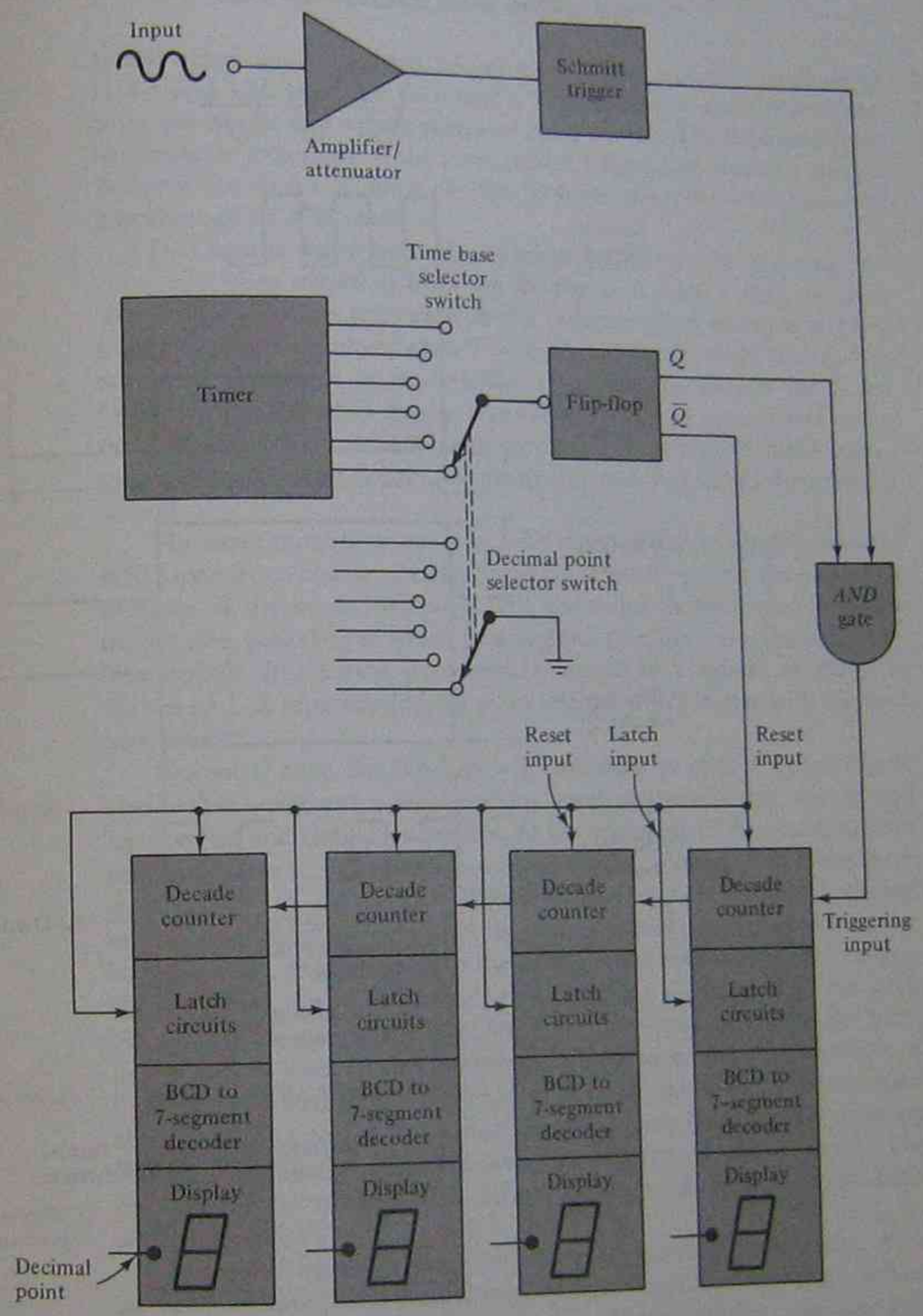


FIGURE 10-2. Block diagram of a digital frequency meter.

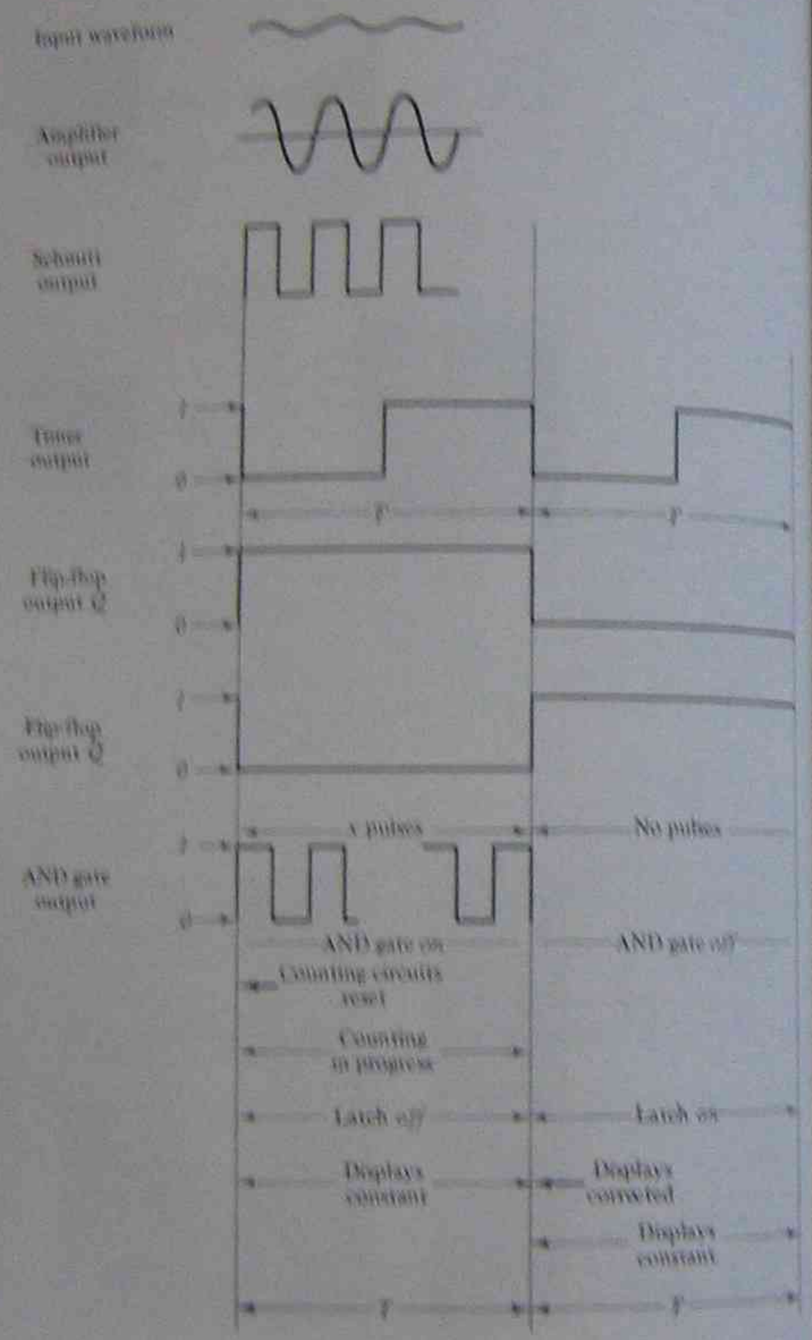


FIGURE 10-3 Waveforms for a digital frequency meter.

Schmitt trigger circuit. (Schmitt trigger circuits are explained in Sections 11-4-1 and 15-2. For now note that a Schmitt circuit converts sine and other waveforms into square waves or pulse waves). The Schmitt output has the same frequency as the input, and it triggers the counting circuits. Before it gets to the counting circuits, however, the pulse waveform must pass through an AND gate.

The square wave from the Schmitt passes to the counting circuits only when output Q from the *flip-flop* is at logic 1 (i.e., positive). The flip-flop changes state each time a negative-going output is received from the timer. Therefore, when $T = 1$ sec (see Figure 10-3), the flip-flop output is alternately at level 1 for 1 sec and at level 0 for 1 sec. Consequently, the AND gate is alternately *on* for one second and *off* for one second. That is, the AND gate alternately passes the Schmitt output pulses to the counting circuits for one second, and then blocks them for one second.

The exact number of input pulses is counted during the time that the AND gate is *on*, and as already discussed, when $T = 1$ sec the count is a measure of the input frequency. The timer has six (or more) available output time periods over which counting can take place (see Section 10-1). The desired time period is selected by means of a switch, as shown in Figure 10-2. A separate decimal point selector switch moves with the time base selector.

Output $\bar{Q}$ from the flip-flop is in antiphase to output Q (see Figure 10-3). This waveform is employed for resetting the counting circuits and for opening and closing the latches. At the beginning of the counting time, output $\bar{Q}$ from the flip-flop is a negative-going voltage. This triggers the reset circuitry in the decade counters to correctly set the initial starting conditions of each counter. Since flip-flop output $\bar{Q}$ is at logic 0 during the counting time, its application to the latch circuits ensures that each latch is *off*. Therefore, during the counting time nothing passes through the latch circuits. At the end of the counting time, the waveform fed to the latch inputs goes to logic 1. This triggers each latch *on* so that the conditions of the displays are corrected, if necessary, to reflect the states of the counting circuits. During the latch *on* time, the AND gate is *off* and no counting occurs. Therefore, once corrected, the displays remain constant. The displays remain constant also during the counting time, since the latch circuits are *off*.

Instead of manually switching to the appropriate timer range, some instruments have an automatic range selection system (*auto ranging*). This usually consists of a circuit which generates a voltage approximately proportional to the input frequency. Depending upon the actual voltage level, one of several transistor switches is turned *on* to select the correct time base and decimal point position.

10-4 FREQUENCY MEASUREMENTS, ERRORS, AND RECIPROCAL COUNTING

In the system described in Section 10-3, the time base could switch the AND gate *on* or *off* while an input pulse (from the Schmitt) is being applied. The partial pulses that get through the AND gate may or may not succeed in triggering the counting circuits. So there is always a possible error of ±1 cycle in the count of input cycles during the timing period. Thus, the accuracy of a digital frequency meter is usually stated as

$$\pm 1 \text{ count} \pm \text{time base error}.$$

Errors in the time base generated by the crystal oscillator (Figure 10-1) are normally the result of variations in temperature, supply voltage changes, and aging of crystals. With reasonable precautions, the total time base error might typically be $< 1 \times 10^{-6}$, or *less than one part in* 10^6 *parts*. (Higher quality time bases have smaller errors.) The total measurement error depends upon the actual frequency being measured. This is demonstrated by Example 10-2.

EXAMPLE 10-2 A frequency counter with an accuracy of ±1 count $\pm(1 \times 10^{-6})$ is employed to measure frequencies of 100 Hz, 1 MHz, and 100 MHz. Calculate the percentage measurement error in each case.

SOLUTION

At $f = 100$ Hz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 100 \text{ Hz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 1 \times 10^{-4} \text{ counts}) \\ &\simeq \pm 1 \text{ count}, \\ \% \text{ error} &= \pm \left(\frac{1}{100 \text{ Hz}} \times 100\% \right) \\ &= \pm 1\%. \end{aligned}$$

At $f = 1$ MHz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 1 \text{ MHz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 1 \text{ count}) \\ &\simeq \pm 2 \text{ counts}, \\ \% \text{ error} &= \frac{2}{1 \text{ MHz}} \times 100\% \\ &= 2 \times 10^{-4}\%. \end{aligned}$$

At $f = 100$ MHz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 100 \text{ MHz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 100 \text{ counts}) \\ &= \pm 101 \text{ counts}, \\ \% \text{ error} &= \pm \left(\frac{101}{100 \text{ MHz}} \times 100\% \right) \\ &= \pm 1.01 \times 10^{-4}\%. \end{aligned}$$

Example 10-2 demonstrates that at a frequency of 100 Hz the error due to ±1 count is ±1%, while that due to the time base is insignificant. At 1 MHz, the error due to one count is equal to that due to the time base. At 100 MHz, the time base is responsible for an error of ±100 counts, although the total error is still a very small percentage of the measured frequency. Therefore, at high frequencies the time base error is larger than the ±1 count error, while at low frequencies the ±1 count error is the larger of the two.

Obviously, the greatest measurement error occurs at low frequencies. At frequencies lower than 100 Hz, the percentage error due to ±1 count is greater than 1%. The low frequency error can be greatly reduced by the *reciprocal counting technique*.

Suppose the time base is disconnected from the system shown in Figure 10-2. Also, assume that the 1-MHz frequency from the crystal-controlled oscillator in the time base (Figure 10-1) is connected directly to the AND gate input in place of the Schmitt. The Schmitt output is now applied as an input to the flip-flop, so that the frequency to be measured is going to the flip-flop instead of to the AND gate input. The new arrangement is shown in Figure 10-4. The result is that the AND gate is switched *on* for the period of the frequency to be measured (see Figure 10-4) and that pulses from the 1-MHz crystal source trigger the counting circuits during this time.

When the frequency to be measured is 100 Hz, the AND gate is *on* for a period of 1/100 Hz = 10 ms. Each cycle from the 1-MHz crystal has a time period of 1 μs. Therefore, the number of pulses counted during 10 ms is

$$\frac{10 \text{ ms}}{1 \mu s} = 10\,000.$$

This is indicated on the display as *100.00 Hz*. (In fact, the four-digit display in Figure 10-2 would not be suitable in this case. A $4\frac{1}{2}$-digit display, or a 5-digit display is required.) The accuracy of measurement of the 100-Hz

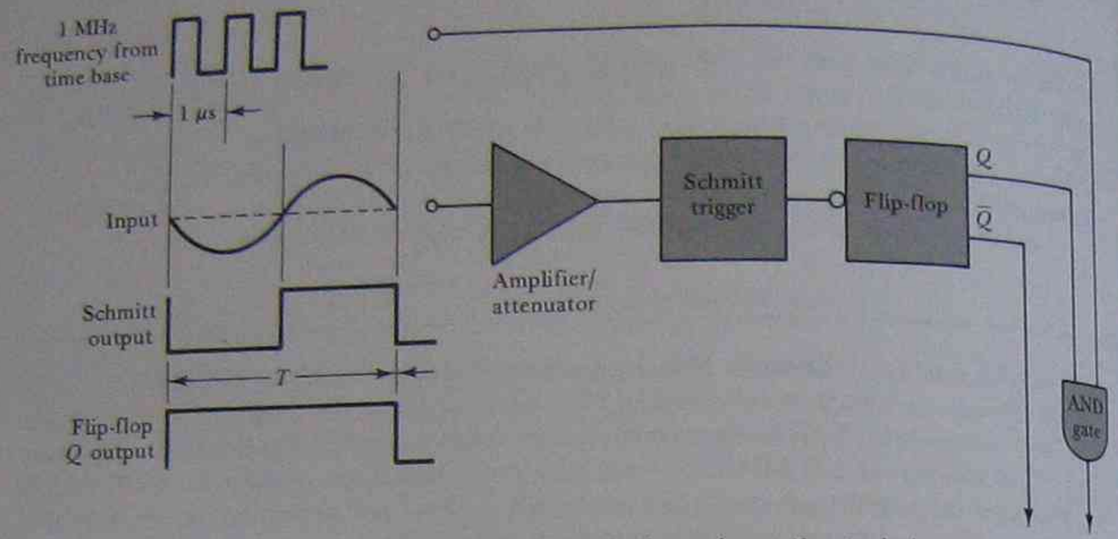


FIGURE 10-4. Reciprocal counting technique.

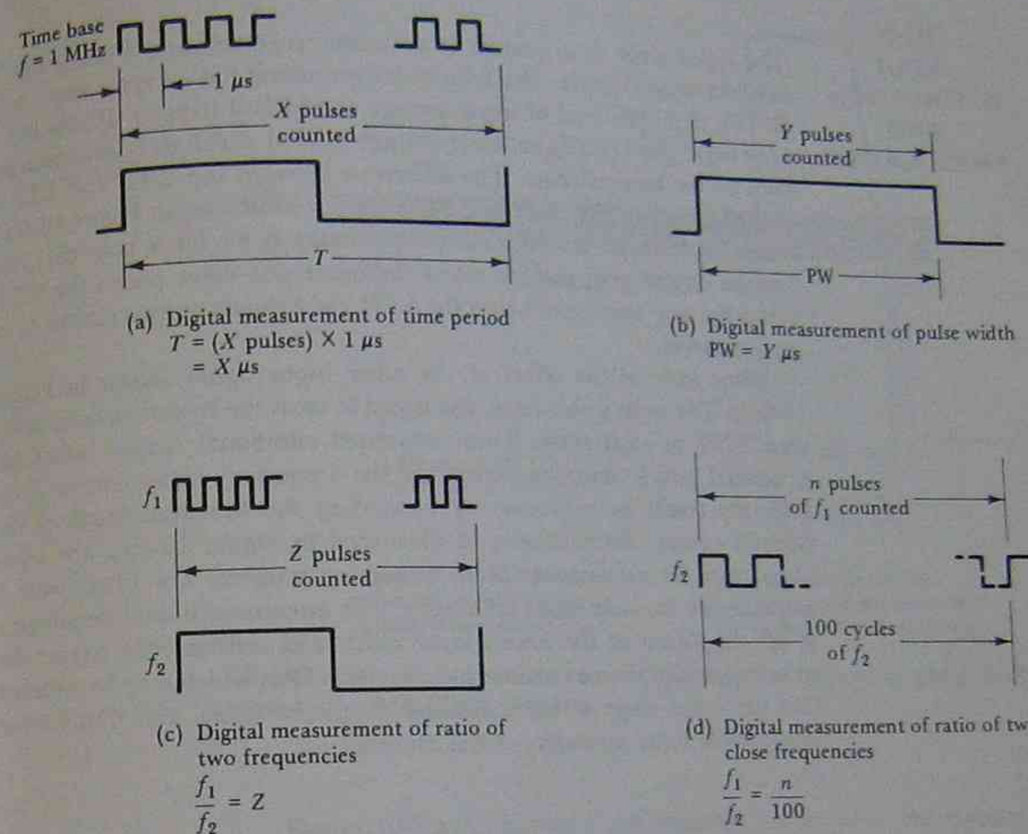
frequency is now ±1 count in 10 000, or 100 Hz/10 000 = 0.01 Hz. As a percentage of the measured frequency the error is

$$\% \text{ error} = \frac{0.01 \text{ Hz}}{100 \text{ Hz}} \times 100\% = \pm 0.01\%.$$

A 0.01% error is a big improvement over the 1% error that occurs with the straight counting technique. At frequencies lower than 100 Hz, the accuracy of measurement is even better (with the reciprocal counting technique). At high frequencies, the straight counting method gives the most accurate results.

10-5 TIME AND RATIO MEASUREMENT

The reciprocal count technique described in Section 10-4 is, in fact, a time measurement method, although the display is expressed as a frequency. The display could be properly expressed as a time period; for example, the 100.00-Hz measurement is made as 10 000 × 1 μs, which is 10.000 ms. The time period of any input waveform can be measured in this way [see Figure 10-5(a)]. If the flip-flop in Figure 10-4 is made to trigger on positive-going inputs as well as on negative-going signals, the width or duration of an input pulse can be measured [Figure 10-5(b)]. Most digital counters have a *start input* and a *stop input*, so that the *time between events* can be measured.



(a) Digital measurement of time period
$T = (X \text{ pulses}) \times 1\ \mu s = X\ \mu s$

(b) Digital measurement of pulse width
$PW = Y\ \mu s$

(c) Digital measurement of ratio of two frequencies
$\frac{f_1}{f_2} = Z$

(d) Digital measurement of ratio of two close frequencies
$\frac{f_1}{f_2} = \frac{n}{100}$

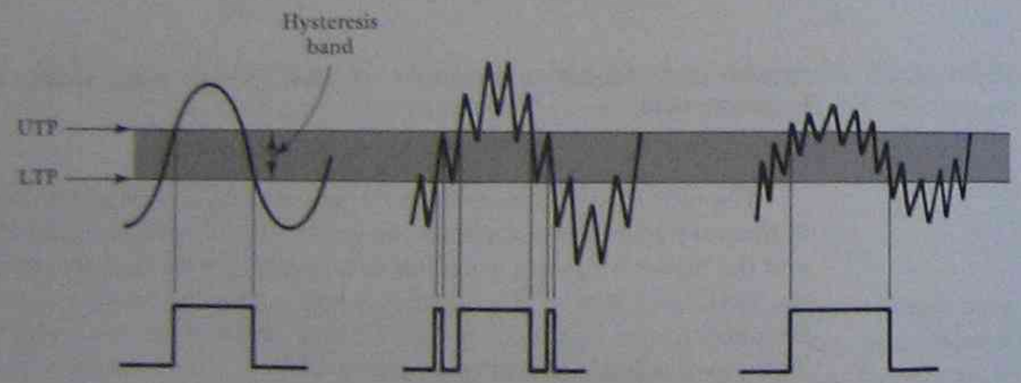
FIGURE 10-5. Digital measurement of time period, pulse width, and frequency ratio.

The ratio of two frequencies can be measured by a counter. The lowest of the two frequencies is applied as an input to the flip-flop in Figure 10-4, and the higher frequency is applied (via appropriate shaping circuitry) to the AND gate input. The instrument now counts the number of high-frequency cycles that occur during the time period of the low frequency. The waveforms are illustrated in Figure 10-5(c). If the high frequency is 100 times the low input frequency, 100 cycles of high frequency are counted. Thus, the displayed number is the ratio of the two input frequencies. The waveform illustrated in Figure 10-5(c) are for the case when one frequency is very much greater than the other. When this is *not* the case (e.g., when $f_1/f_2 = 1.11$), the cycles of f_1 are counted over perhaps 100 cycles of f_2 [Figure 10-5(d)]. With the decimal point selected correctly, the displayed ratio is 1.110.

10-6 INPUT ATTENUATION AND AMPLIFICATION

The input stage to a counter is an amplifier/attenuator feeding into a Schmitt trigger circuit. The Schmitt trigger circuit has an *upper trigger point* (UTP), or upper level of input voltage at which it triggers. It also has a *lower trigger point* (LTP), or lower voltage level at which its output switches back to the original state. The difference between the UTP and LTP is termed *hysteresis*. The effect of the hysteresis is illustrated in Figure 10-6(a). Assuming that the amplifier/attenuator stage is set for a gain of 1, the Schmitt output goes positive when the input sine wave passes the UTP. When the sine wave goes below the LTP, the Schmitt output returns to its previous level.

Now look at the effect of the noisy input signal shown in Figure 10-6(b). The noise spikes cause the signal to cross the hysteresis band more than twice in each cycle. Thus, unwanted additional output pulses are generated which introduce errors in the frequency measurement. This difficulty could be overcome by expanding the hysteresis band of the Schmitt circuit. Alternatively, as illustrated in Figure 10-6(c), the input signal can be attenuated. Most frequency counters are fitted with a continuously variable input attenuator. The attenuator should be adjusted to set the signal at the lowest level which will satisfactorily trigger the counting circuits. Some counters have *low-pass filters* which may be switched into the input stage to attenuate high-frequency noise, and thus further improve the noise immunity of the counter.

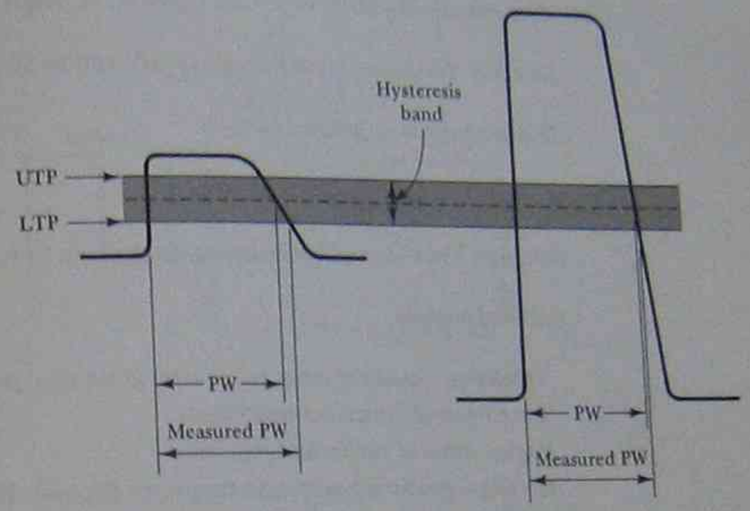


(a) 'Clean' sine wave crosses the hysteresis band twice during each cycle — triggers counting circuits once per cycle

(b) Noisy sine wave crosses hysteresis band more than twice during each cycle — produces counting errors

(c) Attenuated noisy waveform crosses hysteresis band twice in each cycle

FIGURE 10-6. Noisy input signals must be attenuated to avoid frequency counting errors.



(a) A low amplitude input pulse can produce errors in pulse width measurement

(b) Amplification of the input pulse minimizes the pulse width measurement

FIGURE 10-7. Pulses should be amplified to avoid errors in pulse width measurement by digital counter.

Figure 10-7(a) illustrates a problem that occurs when the counter is used as a timer to measure pulse width (PW). The average width of the pulse is the PW illustrated in Figure 10-7(a). However, because of the hysteresis of the Schmitt trigger circuit there is an error in the measured pulse width (see illustration). This error can be minimized either by reducing the hysteresis, or by amplifying the pulse as shown in Figure 10-7(b).

10-7 SPECIFICATIONS FOR DIGITAL COUNTER/TIMERS

The following specification statements are typical of the range of digital counter/timer instruments available today:

Frequency measurement	
Low range	10 Hz to 80 MHz
Wide range, direct measurement	dc to 1.5 GHz
Wide range with added high-frequency converter	dc to 40 GHz

Time measurement: 10 ns to 10^9 sec (approx. 31 years)

Sensitivity: Minimum input voltage 10 mV rms to 50 mV rms

Display: 7 digits to 9 digits

Accuracy: ± 1 digit ± time base error

Gate time: Time over which counting occurs 1 μs to 1 sec

Additional functions

Totalizing—count of input pulses over given time period.
Time interval—time between events.
Ratio—ratio of two input frequencies.
Scaling—producing an output frequency digitally divided from input.

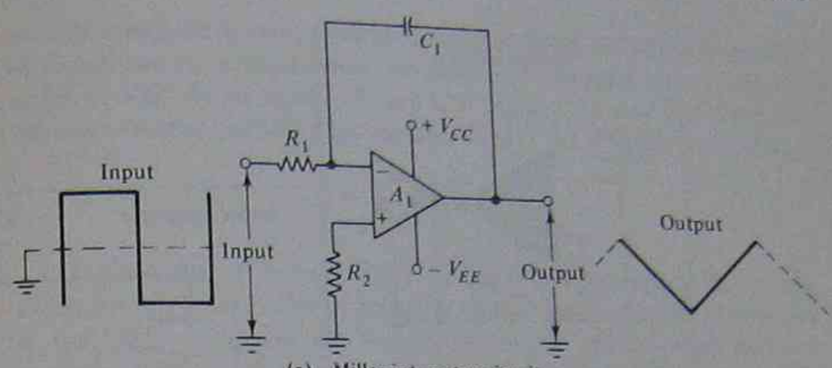
10-8 DIGITAL VOLTMETER SYSTEM

In a *digital voltmeter* (DVM), the voltage to be measured is converted into a time period. This time period is then fed to a digital counter, and the display is read as a voltage. For example, suppose an input of 1 V is converted into a time of exactly 1 sec. If the time base frequency is 1 kHz, then 1000 pulses are counted during the 1-sec time period. This is read as 1.000 V. Now, if the input goes to 1.295 V, it produces a time period of 1.295 sec, during which 1295 pulses are counted. The display is now 1.295 V. One system which accurately converts voltage into time period uses a circuit known as a *Miller integrator*.

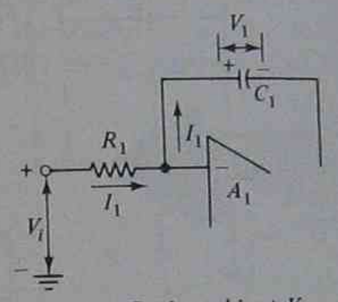
The Miller integrator circuit in Figure 10-8(a) consists of resistor R_1, capacitor C_1, and operational amplifier A_1. With no input voltage and C_1 initially uncharged, the operational amplifier behaves as a voltage follower (see Section 8-6-2) with its noninverting terminal grounded. Thus, the inverting input and the output terminal are also at ground level.

When a positive input voltage V_i is applied [Figure 10-8(b)], the op-amp inverting terminal remains at ground level, and the input current is $I_1 = V_i/R_1$. This is a *constant* current which is very much greater than the op-amp input bias current. Effectively all of I_1 flows to capacitor C_1 to charge it: + on the left-hand side and − on the right. Because the op-amp inverting terminal remains at ground level, the output decreases as C_1 charges. Also, because I_1 is constant, C_1 charges linearly producing a negative-going linear ramp output [see Figure 10-8(d)].

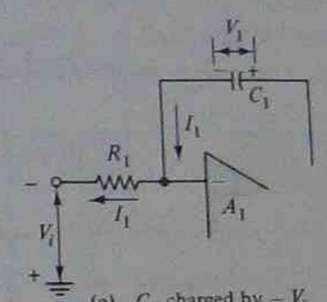
When the input voltage goes negative [Figure 10-8(c)], $I_1 = -V_i/R_1$. Once again, this a constant current which flows through C_1. Again C_1 charges at a constant rate, but now, because of the reversed current



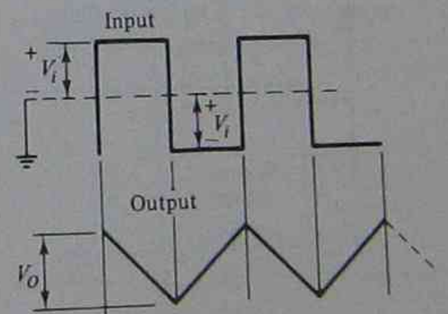
(a) Miller integrator circuit



(b) C_1 charged by $+V_i$



(c) C_1 charged by $-V_i$



(d) Input and output waveforms

FIGURE 10-8. Miller integrator circuit, C_1 charging action, and waveforms.

direction, its polarity is going + on the right and − on the left. At this time the op-amp output voltage is a linear positive-going ramp [Figure 10-8(d)].

A Miller integrator circuit is incorporated in the *dual-slope integrator* illustrated in Figure 10-9. The voltage to be measured (V_i) is applied via a voltage follower which offers a high input impedance. The voltage follower output is switched via FET Q_1 to the input of the Miller integrator. An

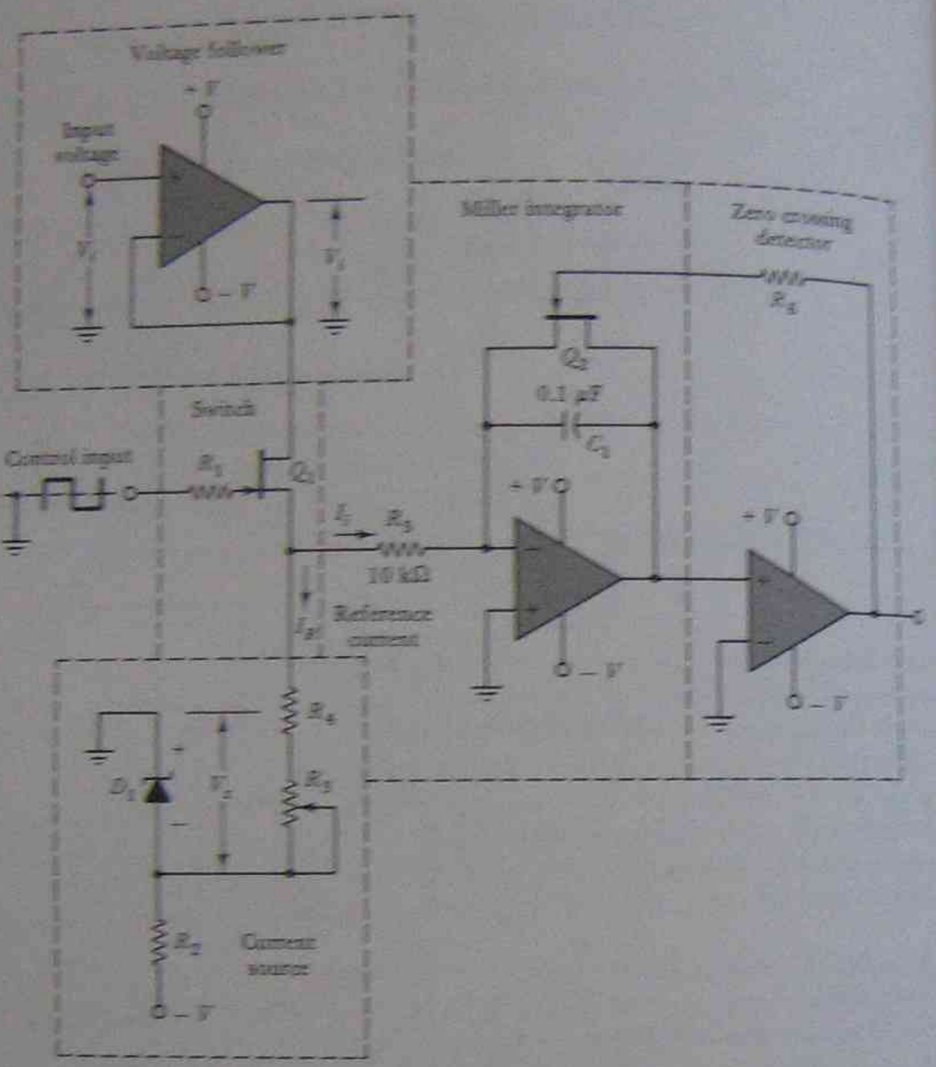


FIGURE 10-9. Dual-slope integrator.

accurate current source is also connected to the Miller integrator input, and the integrator output level is monitored by a *zero-crossing detector*. The zero-crossing detector is basically a high-gain operational amplifier. A large positive output is produced when its input is slightly above ground, and a large negative output occurs when the input is below ground level. The zero-crossing detector controls FET Q_2. When the output of the zero-crossing detector is high, Q_2 is *on* and C_1 is short-circuited. When the zero-crossing detector has a low output, Q_2 is *off* and C_1 can be charged.

The square wave input to Q_1 controls the time interval during which I_i flows into R_3, and the time during which I_R flows out of R_3. This square

wave is generated by using decade counters to divide the output frequency of a clock source, as explained in Section 10-1. When the control input is negative, FET Q_1 is biased *off* and V_i is isolated. During this time, the reference current flows through R_3. The level of the reference current is

$$I_R = \frac{-V_z}{R_3 + R_4 + R_5}.$$

The direction of the current is such that it flows through C_1 from right to left, and C_1 tends to charge positively on the right-hand side. The output of the Miller integrator now eventually rises to ground level, and the zero-crossing detector generates a large positive output. This biases FET Q_2 on, and Q_2 short-circuits C_1. Therefore, at the end of the negative half of the square wave input to Q_1, capacitor C_1 is short-circuited and the Miller circuit output is held close to ground level.

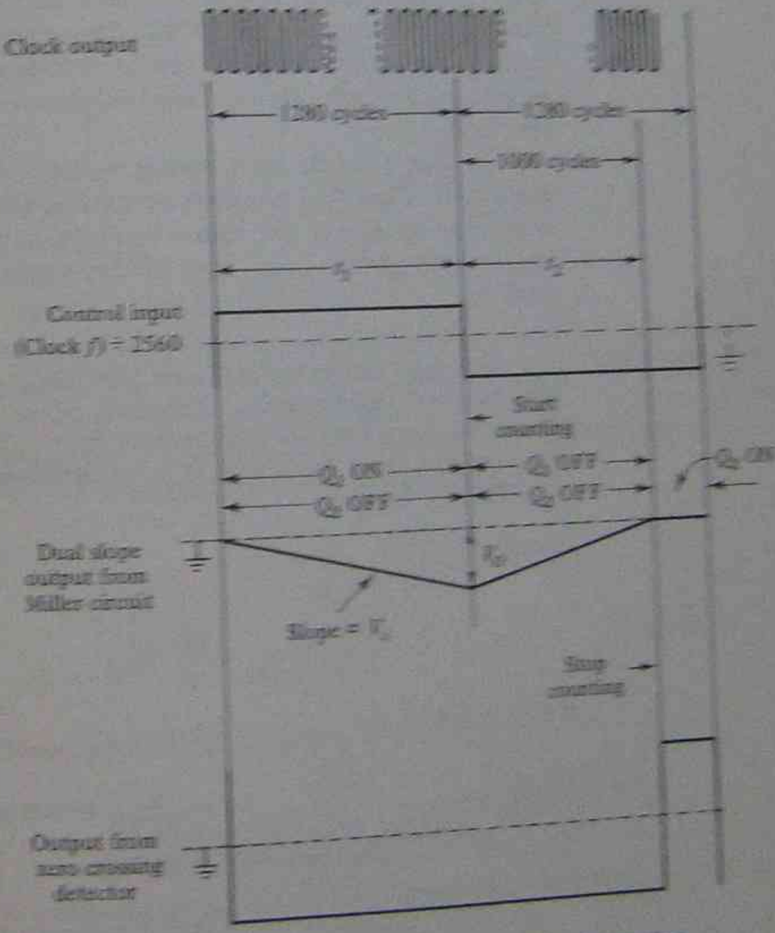


FIGURE 10-10. Waveforms for a dual-slope integrator.

Transistor Q_1 switches *on* when the square wave input becomes positive. This action connects voltage V_i to resistance R_5, and provides the input current $I_i = V_i/R_5$ to the Miller circuit. Capacitor C_1 now charges with negative polarity on the right-hand side and this produces a negative-going output from the Miller circuit (see waveforms in Figure 10-10). Consequently, the zero-crossing detector has a large negative output, which biases transistor Q_2 *off*, thus permitting C_1 to charge. The output from the Miller circuit is a linear negative ramp voltage (Figure 10-10) which continues during the positive portion of the square wave input to Q_1. Since I_i is directly proportional to V_i, the slope of the ramp is also proportional to V_i. Also, the time duration t_1 of the positive input voltage is a constant (Figure 10-10). This means that the ramp amplitude V_o is directly proportional to V_i.

When the square wave input again becomes negative, Q_1 switches *off* and the reference current I_R commences to flow through R_5 and C_1 once more. I_R discharges C_1 so that the Miller circuit output now becomes a positive-going ramp (Figure 10-10). The positive-going ramp continues until it arrives at ground level. Then the zero-crossing detector provides an output which switches Q_2 *on*, discharges C_1, and holds C_1 in short-circuit once again.

The time t_2 for the ramp voltage to climb to zero is directly proportional to V_i. Time t_2 is measured by starting the counting circuits at the negative-going edge of the square wave input to Q_1, and stopping the count at the positive-going edge of the output from the zero-crossing detector.

EXAMPLE 10-3 The dual slope integrator in Figure 10-9 has a square wave input with each half cycle equivalent to 1280 clock pulses (see Figure 10-10). The output frequency from the clock is 200 kHz. If 1000 pulses during time t_2 are to represent an input of $V_i = 1$ V, determine the required level of reference current.

SOLUTION

$$I_i = \frac{V_i}{R_5}.$$

For $V_i = 1$ V,

$$I_i = \frac{1\text{ V}}{10\text{ k}\Omega} = 100\ \mu\text{A},$$

$$\text{Clock frequency} = 200\text{ kHz},$$

$$T = \frac{1}{f} = \frac{1}{200\text{ kHz}} = 5\ \mu\text{s}.$$

If t_1 is the time duration of 1280 clock pulses;

$$t_1 = 5\ \mu\text{s} \times 1280 = 6.4\text{ ms}.$$

I_i is applied to the integrator input for a time period t_1. Since

$$C = \frac{It}{V},$$

ramp voltage

$$V_o = \frac{I_i t_1}{C_1} = \frac{100\ \mu\text{A} \times 6.4\text{ ms}}{0.1\ \mu\text{F}} = 6.4\text{ V}.$$

If t_2 is the time duration of 1000 clock pulses,

$$t_2 = 5\ \mu\text{s} \times 1000 = 5\text{ ms},$$

and I_R must discharge C_1 in time period t_2,

$$I_R = \frac{C_1 V_o}{t_2}$$

$$= \frac{0.1\ \mu\text{F} \times 6.4\text{ V}}{5\text{ ms}}$$

$$= 128\ \mu\text{A}.$$

One of the most important advantages of the dual-slope integration method is that small drifts in the clock frequency have little or no effect on the accuracy of measurements. Consider the following example: Let clock frequency = f; then time period of one cycle of clock frequency = $T = 1/f$. The time duration of 1280 clock pulses (t_1) is $1280 \times T$.

$$V_o = \frac{I_1 t_1}{C_1} = \frac{100\ \mu\text{A} \times 1280T}{C_1}$$

$$t_2 = \frac{C_1 V_o}{I_R} = \left(\frac{C_1}{128\ \mu\text{A}}\right)\left(\frac{100\ \mu\text{A} \times 1280T}{C_1}\right) = 1000T.$$

The number of clock pulses during t_2 is given by

$$\frac{t_2}{\text{Time period of clock pulses}} = \frac{1000T}{T} = 1000.$$

It is seen that when the clock frequency drifts, the digital measurement of voltage is unaffected.

Figure 10-11 shows a block diagram of a DVM system employing dual slope integration. In this particular system, the clock generator has a frequency of 200 kHz. The 200 kHz is divided by a decade counter and two divide-by-sixteen counters as shown, giving a frequency of approximately 78 Hz. As already explained, this (78 Hz) is the square wave which controls the integrator. The 200-kHz clock signal, the 78-Hz square wave, and the integrator output are all fed to input terminals of a NAND gate.

The 200-kHz clock output acts as a triggering signal to the counting circuitry when the other two inputs to the NAND gate are high. This occurs during time t_2, as illustrated in Figure 10-10. The integrator output

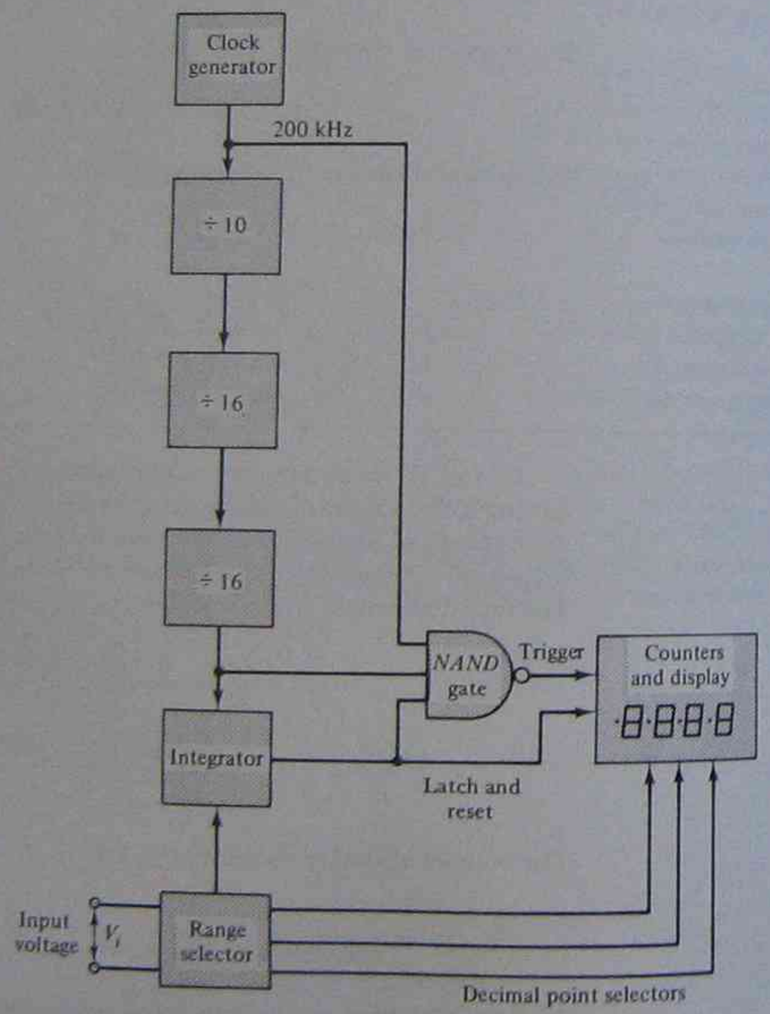


FIGURE 10-11. Digital voltmeter system.

(i.e., zero-crossing detector output) is also used to reset the counting circuits and to control the latch. The counting circuits are reset at the beginning of time period t_1. Counting commences at the start of t_2. The latch is switched *on* at the end of t_2 in order to set the displays according to the counting circuits.

The range selector is adjusted to suit the input voltage. An input of less than 1 V is applied directly to the integrator, and a decimal point is selected so that the display can indicate a maximum of .9999 V. An input voltage between 1 V and 10 .V is first potentially divided by 10 and applied to the integrator again as a voltage less than 1 V. In this case the decimal point is selected so that the display can indicate a maximum of 9.999 V. An input voltage between 10 V and 100 V is reduced by a factor of 100 before passing to the integrator. Decimal point selection now allows the meter to indicate a maximum of 99.99 V.

Some DVMs employ *automatic ranging circuits*. These determine the approximate level of the input voltage, and trigger transistor switches to select the appropriate time base and decimal point position.

10-9 DIGITAL MEASUREMENT OF CURRENT RESISTANCE AND AC QUANTITIES

The method used in digital instruments to convert current and resistance into measurable voltage levels are similar to those employed in analog electronic instruments. As explained in Section 8-10 for analog instruments, shunts are used for digital current measurements. The digital display is identified as mA, μA, etc. For very low current ranges, relatively high shunt resistances are used, and this must be taken into account when connecting the meter into a circuit.

In digital instruments, resistance must be converted into direct voltage by a linear method such as that described in Section 8-8-3. The voltage is then measured digitally and displayed as kΩ or MΩ.

Alternating voltage and current must be converted into dc quantities either by rectification or by a true rms method, as discussed in Section 8-9. Once again as in the case of analog instruments, where rectification is used the digital meter readings are true only for pure sine waves. When true rms conversion techniques are used, the instrument indicates the true rms measurement no matter what the waveform.

10-10 DIGITAL MULTIMETER

Perhaps the most important feature of a *digital multimeter* (DMM) compared to an analog instrument is the direct digital indication of the measurement. With analog instruments the pointer position must be carefully read to avoid parallax, and the range must be noted to avoid misreading. Neither of these are necessary with a digital instrument.

Furthermore, with a deflection instrument the exact pointer position cannot be determined more accurately than to about ±0.3% of full scale. Digital instruments, on the other hand, can give readings with three or more decimal places. Thus, a digital instrument has better *resolution* than an analog instrument.

Many DMMs have automatic ranging circuits which select the most appropriate range. When the range is selected manually, greatest accuracy is achieved by using a range that gives the largest possible numerical display. This is the same as adjusting the range of analog instruments for the greatest on-scale pointer deflection. For example, a display of 1.933 V is obviously more accurate than a display of 001.9 V. When the selected range is too low, the display usually *blanks*, or flashes on and off continuously.

Another very important advantage of digital instruments over analog is that digital instruments are by far the most accurate. Good quality analog voltmeters have ±1% accuracy, while even the least expensive DVMs have a typical accuracy of ±0.5%. Good quality digital instruments have ±0.1% or better accuracy.

Digital instrument accuracy is usually stated as ±(0.1% rdg + 1 d). This means ±(0.1% of reading +1 digit). The 1 digit refers to the right-hand numeral of the display. The maximum error in a 1.500-V reading on a $3\frac{1}{2}$-digit display would be

$$\begin{aligned} \text{error} &= \pm\,[(0.1\%\text{ of }1.5\text{ V}) + 0.001\text{ V}] \\ &= \pm\,(0.0015\text{ V} + 0.001\text{ V}) \\ &= \pm 0.0025\text{ V} \\ &\simeq \pm\,(0.17\%\text{ of }1.5\text{ V}). \end{aligned}$$

The following specification statements are typical of currently available digital multimeters:

Display

$3\frac{1}{2}$ and $4\frac{1}{2}$ digit

dc voltage

range 0.1 V to 1000 V
accuracy ±(0.1% rdg + 1 d)
input resistance 10 MΩ

ac Voltage

range 0.1 V to 1000 V rms
accuracy ±(0.6% rdg + 10 d)
frequency range 10 Hz to 10 kHz
input resistance 10 MΩ

dc Current

range 100 mA to 10 A
accuracy ±(1% rdg +10 d)
shunt resistance 0.1 Ω to 1 kΩ

ac Current

range 100 mA to 10A
accuracy ±(2% rdg + 15 d)
shunt resistance 0.1 Ω to 1 kΩ

Resistance

range 1 kΩ to 11 MΩ
accuracy ±(0.6% rdg + 10 d)
open-circuit terminal voltage 5 V

Various probes are available for extending the ranges of digital multimeters. Some of these are:

- *50 A shunt* extends current measurements to 50 A
- *High voltage probe* extends voltage range to 40 kV
- *RF probe* extends frequency range to 100 MHz
- *Clamp-on ac current probe* extends ac current range to 200 A rms.

The controls and terminals of a representative laboratory type DMM are shown in Figure 10-12. The function and range selections are performed by push-button controls. Starting from the left-hand side, the first button is a power *on / off* switch. The next five buttons are for function selection: AC/DC, *LO / HI* (resistance range), Ω, V, and A. The five right-hand buttons are for range selection. To use the instrument, switch *on* the power, select the appropriate function and range, connect the source to be measured, and read the display.

FIGURE 10-12. Front panel of digital multimeter (Courtesy of Keithley Instruments Inc.).

The input terminals are identified as LO (*low*) and HI (*high*). Some DMMs have more than two terminals (for example, there may be an additional resistance or current terminal). On these instruments the *low* terminal is identified as COM (*common*) terminal. In all cases the *low* or *common* terminal should be connected to any ground point in a circuit where measurements are being made. Also, when more than one electronic instrument is connected in a circuit the *low* or *common* terminals should all be connected to one point in the circuit. As explained in Section 8-3-3, this is because the *low* or *common* terminal is usually grounded via a capacitor within the instrument.

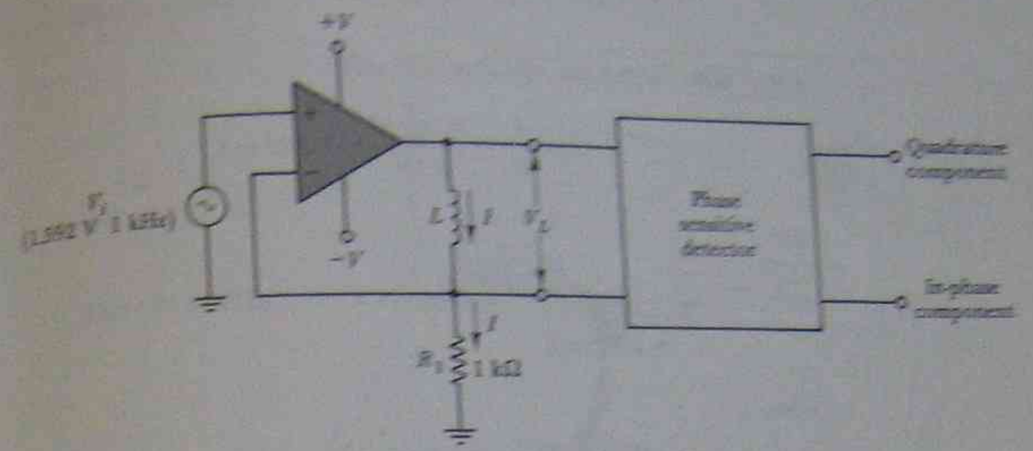
When measuring quantities which have a negative polarity with respect to the *low* terminal, a negative sign is displayed beside the digital indication. For the instrument in Figure 10-12, the absence of a polarity sign indicates a positive polarity. If the selected range is too low for the applied voltage or current, the display flashes 0000.

Analog instruments must be *zeroed* before use, and the same is true of many digital instruments. For the instrument illustrated in Figure 10-12 the zeroing procedure is: select the resistance function, short the terminals together, adjust the slot-headed *zero* control until the display indicates zero.

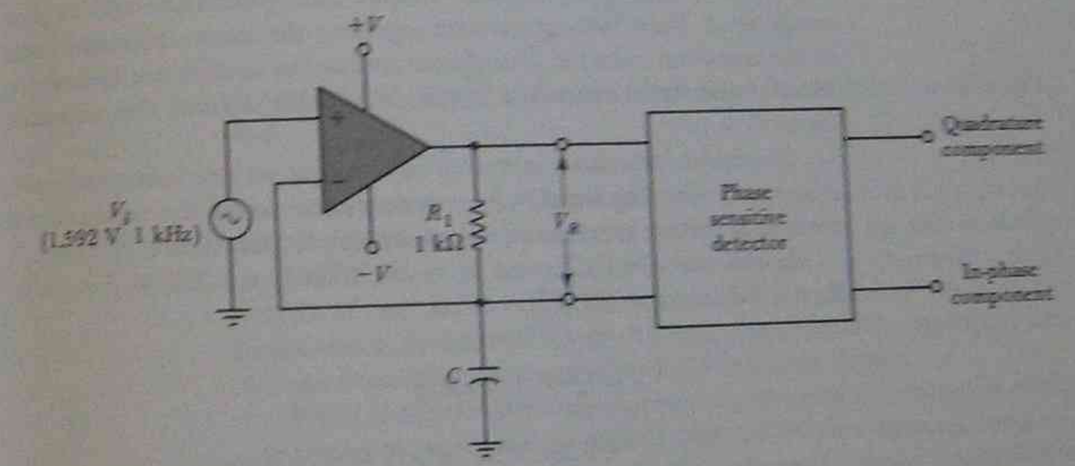
10-11 DIGITAL LCR MEASUREMENTS

As in the case of the resistance measuring techniques described in Section 8-8-3, inductive and capacitive impedances are first converted into voltages before measurement. Figure 10-13 illustrates the basic method.

In Figure 10-13(a) an ac voltage is applied to the noninverting input terminal of the operational amplifier. The input voltage is developed across resistor R_1 to give a current: $I = V_i/R_1$. This current also flows through the inductor giving a voltage drop: $V_L = IX_L$. If $V_i = 1.592$ V,



(a) Linear conversion of inductive impedance into voltage



(b) Linear conversion of capacitive impedance into voltage

FIGURE 10-13. Basic circuits for converting inductive and capacitive impedances into voltage components for digital measurement.

$f = 1$ kHz, $R_1 = 1$ kΩ, and $L = 100$ mH:

$$I = \frac{V_1}{R_1} = \frac{1.592\text{ V}}{1\text{ k}\Omega} = 1.592\text{ mA},$$

and

$$V_2 = I(2\pi fL) = 1.592\text{ mA} \times 2\pi \times 1\text{ kHz} \times 100\text{ mH}$$
$$= 1\text{ V(rms)},$$

when

$$L = 200\text{ mH}, V_2 = 2\text{ V}; \text{ when } L = 300\text{ mH}, V_2 = 3\text{ V}; \text{ etc.}$$

It is seen that the voltage developed across L is directly proportional to the inductive impedance. A *phase sensitive detector* [Figure 10-13(a)] is employed to resolve the inductor voltage into quadrature and in-phase components. These two components represent the series equivalent circuit of the measured inductor. The digital measuring circuits are arranged to measure the series equivalent circuit inductance L_s and the dissipation factor $D = 1/Q$.

Capacitive impedance is treated in a similar way to inductive impedance, except that the input voltage is developed across the capacitor and the output voltage is measured across the resistor [see Figure 10-13(b)].

In this case $I = V_1/X_c$, and $V_R = IR$. With $V_1 = 1.592$ V, $f = 1$ kHz, $R_1 = 1$ kΩ, and $C = 0.1$ μF:

$$I = \frac{V_1}{X_c} = V_1(2\pi fC)$$
$$= 1.592\text{ V} \times 2\pi \times 1\text{ kHz} \times 0.1\ \mu\text{F}$$
$$= 1\text{ mA},$$

and

$$V_R = IR = 1\text{ mA} \times 1\text{ k}\Omega$$
$$= 1\text{ V (rms)},$$

when $C = 0.2$ μF, $V_R = 2$ V; when $C = 0.3$ μF, $V_R = 3$ V, etc.

The voltage developed across R is directly proportional to the capacitive impedance. The phase sensitive detector [Figure 10-13(b)] resolves the resistor voltage into quadrature and in-phase components, which in this case are proportional to the capacitor current. The displayed capacitance measurement is that of the parallel equivalent circuit (C_p). The dissipation factor (D) of the capacitor is also displayed.

The digital LCR meter shown in Figure 10-14 can measure *inductance*, *capacitance*, *resistance*, *conductance*, and *dissipation factor*. The desired function is

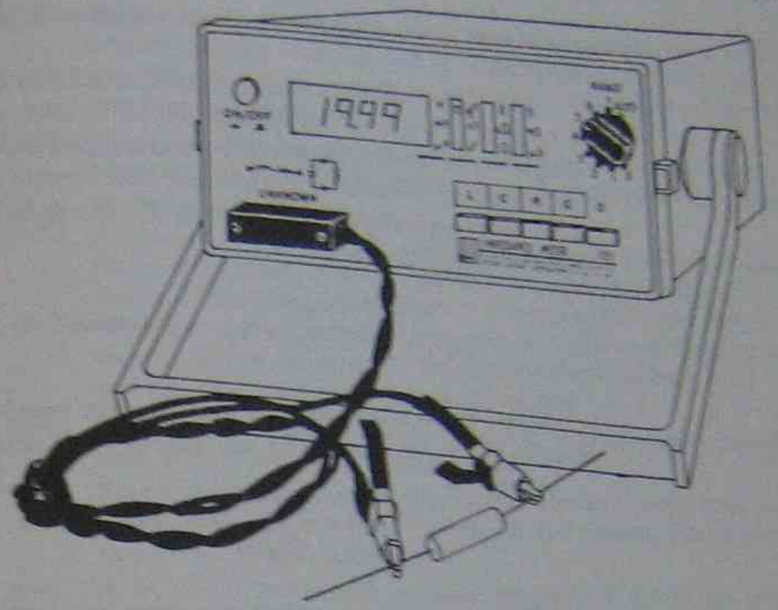


FIGURE 10-14. Digital LCR meter (Courtesy of Electro Scientific Industries, Inc.).

selected by push button. The range switch is normally set to the automatic (AUTO) position for convenience. However, when a number of similar measurements are to be made, it is faster to use the appropriate range instead of the automatic range selection. The numerical value of the measurement is indicated on the 3½-digit display, and the multiplier and measured quantity are identified by LED indicating lamps.

Four (*current* and *potential*) terminals are provided for connection of the component to be measured. (See Section 6-4 for four-terminal measurements.) For general use each pair of current and voltage terminals are joined together at two spring clips which facilitate quick connection of components. A ground terminal for guard-ring type measurements (see Section 6-5) is provided at the rear of the instrument. The ground terminal together with the other four terminals is said to give the instrument *five-terminal measurement* capability. *Bias terminals* are also available at the rear of the instrument, so that a bias current can be passed through an inductor or a bias voltage applied to a capacitor during measurement.

For R, L, C, and G, typical measurement accuracies are $\pm$[0.25% + (1 + 0.002 R, L, C, or G) digits]; for D the measurement accuracy is $\pm$(2% + 0.010).

Resistance measurements may be made directly on the digital LCR instrument in Figure 10-14, over a range of 2 Ω to 2 MΩ. Conductance is measured directly over a range of 2 μS to 20 S. Resistances between 2 MΩ and 1000 MΩ can be measured as conductances, and the resistance