Section 1.7

1.22 A temperature sensor has a transfer function of 0.15 mV/°C and a time constant of 3.3 s. If a step change of 22°C to 50°C is applied at $t = 0$, find the output voltages at 0.5 s, 2.0 s, 3.3 s, and 9 s. What is the *indicated* temperature at these times?

1.23 A pressure sensor measures 44 psi just before a sudden change to 70 psi. The sensor measures 52 psi at a time 4.5 seconds after the change. What is the sensor time constant?

1.24 A photocell with a 35-ms time constant is used to measure light flashes. How long after a sudden dark to light flash before the cell output is 80% of the final value?

1.25 An alarm light goes ON when a pressure sensor voltage rises above 4.00 volts. The pressure sensor outputs 20 mV/kPa and has a time constant of 4.9 seconds. How long after the pressure rises suddenly from 100 kPa to 400 kPa does the light go ON?

Section 1.8

1.26 A circuit design calls for a 1.5-kΩ resistor to have 4.7 volts across its terminals. What would be the expected current? The circuit is built and the resistance is measured to be 1500 Ω and the voltage 4.7 V. What is the current through the resistor?

1.27 Flow rate was monitored for a week, and the following values were recorded as gal/min: 10.1, 12.2, 9.7, 8.8, 11.4, 12.9, 10.2, 10.5, 9.8, 11.5, 10.3, 9.3, 7.7, 10.2, 10.0, 11.3. Find the mean and the standard deviation for these data.

1.28 A manufacturer specification sheet lists the transfer function of a pressure sensor as 45 ± 5% mV/kPa with a time constant of 4 ± 10% seconds. A highly accurate test system applies a step change of pressure from 20 kPa to 100 kPa.

a. What is the range of sensor voltage outputs initially and finally?

b. What range of voltages would be expected to be measured 2 seconds after the step change is applied?

CHAPTER 2

ANALOG SIGNAL CONDITIONING

INSTRUCTIONAL OBJECTIVES

The purpose of this chapter is to just familiarize the reader with the basic techniques of signal conditioning in process control, not to produce experts in the subject. In view of this goal, attention has been given to only the most common techniques. After you have read this chapter, you should be able to

1. **Define the common types of analog signal conditioning.**
2. **Design a Wheatstone bridge for resistance measurement.**
3. **Draw a diagram of a current balance bridge and describe its operation.**
4. **Design *RC* low-pass and high-pass filters for specific applications.**
5. **Define the operation of a silicon-controlled rectifier.**
6. **Design a high-input impedance op amp dc amplifier for specific gain.**
7. **Analyze a simple op amp circuit for its transfer characteristics.**
8. **Explain the purpose of compensation leads in a bridge circuit.**
9. **Design a voltage-to-current converter for specified voltage input and current output.**
10. **Define the basic linearization procedure.**

2.1 INTRODUCTION

The wide variety of sensors needed to transform the wide variety of process variables in process-control systems into electrical analogs produces an equally wide variety of signal characteristics. *Signal conditioning* refers to operations

performed on such signals to convert them to a form suitable for *interface* with other elements in the process-control loop. In this chapter, we are concerned only with *analog* conversions, where the conditioned output is still an analog representation of the variable. Even in applications involving digital processing, some type of analog conditioning usually is required before analog-to-digital conversion is made. Specifics of digital signal conditioning are considered in Chapter 3.

2.2 PRINCIPLES OF ANALOG SIGNAL CONDITIONING

A sensor measures a variable by converting information about that variable into a dependent signal of either electrical or pneumatic nature. To develop such transducers, we take advantage of fortuitous circumstances in nature where a dynamic variable influences some characteristic of a material. Consequently, there is little choice of the type or extent of such proportionality. For example, once we have researched nature and found that cadmium sulfide resistance varies inversely and nonlinearly with light intensity, we must then learn to employ this device for light measurement within the confines of that dependence. Analog signal conditioning provides the operations necessary to transform a sensor output into a form necessary to interface with other elements of the process-control loop. We will confine our attention to electrical transformations.

We often describe the effect of the signal conditioning by the term *transfer function*. By this term we mean the effect of the signal conditioning on the input signal. Thus, a simple voltage amplifier has a transfer function of some constant that, when multiplied by the input voltage, gives the output voltage.

It is possible to categorize signal conditioning into several general types.

2.2.1 Signal-Level Changes

The simplest method of signal conditioning is to change the level of a signal. The most common example is the necessity to either amplify or attenuate a voltage level. Generally, process-control applications result in slowly varying low-frequency signals where dc or low-frequency response amplifiers can be employed. An important factor in the selection of an amplifier is the input impedance that the amplifier offers to the sensor (or any other element that serves as an input). In process control, the signals are always representative of a process variable, and any loading effects obscure the correspondence between the measured signal and the variable value. In some cases, such as accelerometers and optical detectors, the frequency response of the amplifier is very important.

2.2.2 Linearization

As pointed out earlier, the process-control designer has little choice of the characteristics of a sensor output versus process variable. Often the dependence that

exists between input and output is nonlinear. Even those devices that are approximately linear may present problems when precise measurements of the variable are required. One of the functions of analog signal conditioning is to linearize a transducer's response.

Linearization may be provided by an amplifier whose gain is a function of input voltage level to linearize the overall variation of input voltage to output voltage. An example of this linearization occurs quite frequently for a sensor where the output is exponential with respect to the dynamic variable. In Figure 2.1 we see such a case (contrived) where the voltage of a transducer is assumed to be exponential with respect to light intensity I. We may write this variation as

$$V_I = V_0\, e^{-\alpha I} \tag{2.1}$$

where

V_I = output voltage at intensity I
V_0 = zero intensity voltage
α = exponential constant
I = light intensity

To linearize this signal, we employ an amplifier whose output varies at the natural logarithm or inverse of the input

$$V_A = K \log_e (V_{IN}) \tag{2.2}$$

where

V_A = amplifier output voltage
K = calibration constant
V_{IN} = amplifier input voltage = V_I [in Equation (2.1)]

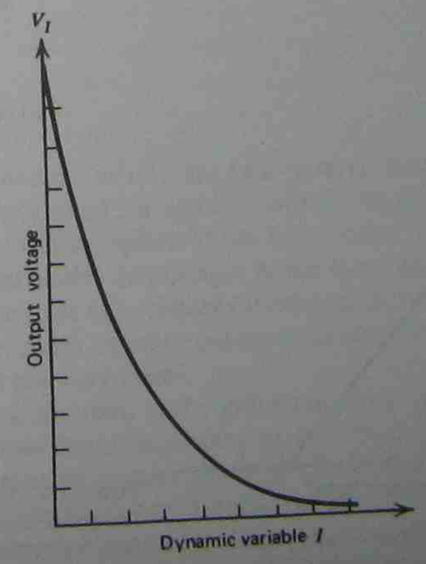


Figure 2.1 An example of a nonlinear sensor output. Here, light intensity is assumed to produce an output voltage.

By substituting Equation (2.1) into Equation (2.2) where $V_{IN} = V_I$, we find

$$V_A = K \log_e(V_0) - \alpha KI \tag{2.3}$$

where all terms have been defined.

The amplifier output *does* vary linearly with intensity but with an offset $K \log_e(V_0)$ and a scale factor of αK as shown in Figure 2.2. Further signal conditioning may be employed, if required, to eliminate the offset and provide any desired calibration of voltage versus intensity.

Other types of linearization are possible, including eliminating small variations (in response) away from linearity.

2.2.3 Conversions

Often, signal conditioning is used to convert one type of electrical variation into another. Thus, a large class of sensors provides changes of resistance with changes in a dynamic variable. In these cases, it is necessary to provide a circuit to convert this resistance change either to a voltage or current signal. This is generally accomplished by bridges when the fractional resistance change is small and/or by amplifiers whose gain varies with resistance.

Signal transmission

An important type of conversion is associated with the process-control standard of transmitting signals as 4–20 mA current levels in wire. This gives rise to the need for converting resistance and voltage levels to an appropriate current level at the transmitting end and for converting the current back to voltage at the receiving end. Of course, current transmission is used because such a signal is independent of load variations other than accidental shunt conditions that may

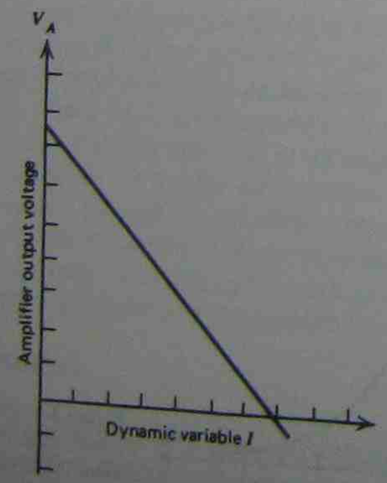


Figure 2.2 Proper signal conditioning has produced an output voltage which now varies linearly with light intensity.

draw off some current. Thus, voltage-to-current and current-to-voltage converters are often required.

Digital interface

The use of computers in process control requires conversion of analog data into a digital format by integrated circuit devices called analog-to-digital converters (ADCs). Analog signal conversion is usually required to adjust the analog measurement signal to match the input requirements of the ADC. For example, the ADC may need a voltage that varies between 0 and 5 volts, but the sensor provides a signal that varies from 30 to 80 mV. Signal conversion circuits can be developed to interface the output to the required ADC input.

2.2.4 Filtering and Impedance Matching

Two other common signal conditioning requirements are filtering and matching impedance.

Often, spurious signals of considerable strength are present in the industrial environment, such as the 60-Hz line frequency signals. Motor start transients also may cause pulses and other unwanted signals in the process-control loop. In many cases, it is necessary to use high-pass, low-pass, or notch *filters* to eliminate unwanted signals from the loop. Such filtering can be accomplished by *passive* filters using only resistors, capacitors, inductors, or *active* filters, using gain and feedback.

Impedance matching is an important element of signal conditioning when transducer internal impedance or line impedance can cause errors in measurement of a dynamic variable. Both active and passive networks are employed to provide such matching.

2.3 PASSIVE CIRCUITS

Bridge and divider circuits are two passive measurement techniques that have been extensively used for signal conditioning for many years. Although modern active circuits often replace these techniques, there are still many applications where their particular advantages make them useful.

Bridge circuits are primarily used as an accurate means of measuring changes in impedance. Such circuits are particularly useful when the fractional *changes* in impedance are *very small*.

It is quite common in the industrial environment to find signals that possess high- and/or low-frequency noise as well as the desired measurement data. For example, a transducer may convert temperature information into a dc voltage, proportional to temperature. Because of the ever-present ac power lines, however, there may be a 60-Hz noise voltage impressed on the output that makes deter-

mination of the temperature difficult. A passive circuit consisting of a resistor and capacitor often can be used to eliminate both high- and low-frequency noise without changing the desired signal information.

2.3.1 Divider Circuit

The elementary voltage divider shown in Figure 2.3 often can be used to provide conversion of resistance variation into a voltage variation. The voltage of such a divider is given by the well-known relationship

$$V_D = \frac{R_2 V_s}{R_1 + R_2} \tag{2.4}$$

where

V_s = supply voltage
R_1, R_2 = divider resistors

Either R_1 or R_2 can be the transducer whose resistance varies with some measured variable.

It is important to consider the following issues when using a divider for conversion of resistance to voltage variation:

1. The variation of V_D with either R_1 or R_2 is nonlinear; that is, even if the resistance varies linearly with the measured variable, the divider voltage will not vary linearly.
2. The effective output impedance of the divider is the parallel combination of R_1 and R_2. This may not necessarily be high, so loading effects must be considered.
3. In a divider circuit, current flows through both resistors; that is, power will be dissipated by both, including the transducer. The power rating of both the resistor and transducer must be considered.

Example 2.1

The divider of Figure 2.3 has $R_1 = 10.0$ kΩ and $V_s = 5.00$ V. Suppose R_2 is a transducer whose resistance varies from 4.00 to 12.0 kΩ as some dynamic variable

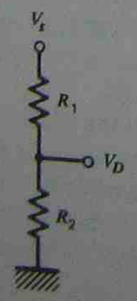


Figure 2.3 The simple voltage divider can often be used to convert resistance variation into voltage variation.

varies over a range. Then find (a) the minimum and maximum of V_D, (b) the range of output impedance, and (c) the range of power dissipated by R_2 (the transducer).

Solution The solution to part (a) is given by Equation (2.4). For $R_2 = 4$ kΩ, we have

$$V_D = \frac{(5\text{ V})(4\text{ k}\Omega)}{10\text{ k}\Omega + 4\text{ k}\Omega} = 1.43\text{ V}$$

For $R_2 = 12$ kΩ, the voltage is

$$V_D = \frac{(5\text{ V})(12\text{ k}\Omega)}{10\text{ k}\Omega + 12\text{ k}\Omega} = 2.73\text{ V}$$

Thus, the voltage varies from 1.43 to 2.73 volts.

For part (b), the range of output impedance is found from the parallel combination of R_1 and R_2 for the minimum and maximum of R_2. Simple parallel resistance computation shows that this will be from 2.86 to 5.45 kΩ.

For part (c), the power dissipated by the transducer can be determined most easily from V^2/R, as the voltage across R_2 has been calculated. The power dissipated varies from 0.51 to 0.62 mW.

2.3.2 Bridge Circuits

Bridge circuits are passive networks often used to measure impedances by the technique of potential matching. In this case, a set of accurately known impedances is adjusted in value in relation to an unknown until a condition exists where the potential difference between two points in the network is zero, that is, *null*. This condition defines an equation used to find the unknown impedance in terms of the known values. A distinct advantage of such measurement techniques is that they are based on reaching the null condition, that is, zero voltage or current, as opposed to an absolute measurement. It is usually much easier to refine and improve techniques for detection of a null than for measurement of some other specific value. This leaves the accuracy of the measurement predominantly dependent on the accuracy with which the known impedances have been determined.

Wheatstone bridge

The simplest and most common bridge circuit is the dc Wheatstone bridge, as shown in Figure 2.4. This network is used in signal conditioning applications where a sensor changes resistance with process variable changes. Many modifications of this basic bridge are employed for other specific applications. In Figure 2.4 the object labeled D is a *null detector* used to compare the potentials of points a and b of the network. In most modern applications the null detector is a very high-input impedance differential amplifier. In some cases, a highly sensitive galvanometer with a relatively low impedance may be used, especially for calibration purposes and single measurement instruments.

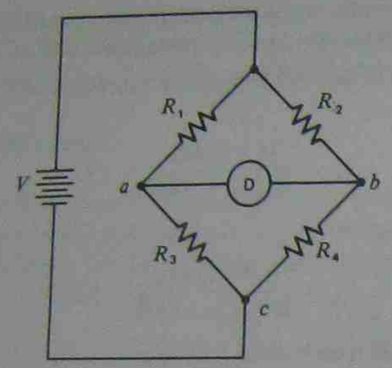


Figure 2.4 The basic dc Wheatstone bridge.

For our initial analysis, assume the null detector impedance is infinite, that is, an open circuit.

In this case the potential difference, ΔV between points a and b, is simply

$$\Delta V = V_a - V_b \tag{2.5}$$

where

V_a = potential of point a with respect to c
V_b = potential of point b with respect to c

The values of V_a and V_b now can be found by noting that V_a is just the supply voltage V divided between R_1 and R_3.

$$V_a = \frac{VR_3}{R_1 + R_3} \tag{2.6}$$

In a similar fashion, V_b is a divided voltage given by

$$V_b = \frac{VR_4}{R_2 + R_4} \tag{2.7}$$

where

V = bridge supply voltage
R_1, R_2, R_3, R_4 = bridge resistors as given in Figure 2.4

If we now combine Equations (2.5), (2.6), and (2.7), the voltage difference or voltage offset can be written

$$\Delta V = \frac{VR_3}{R_1 + R_3} - \frac{VR_4}{R_2 + R_4} \tag{2.8}$$

After some algebra, the reader can show that this equation reduces to

$$\Delta V = V \frac{R_3R_2 - R_1R_4}{(R_1 + R_3) \cdot (R_2 + R_4)} \tag{2.9}$$

Equation (2.9) shows how the difference in potential across the detector is a function of the supply voltage and the values of the resistors. Because a difference appears in the *numerator* of Equation (2.9), it is clear that a particular combination of resistors can be found that will result in zero difference and zero voltage across the detector, that is, a null. Obviously, this combination, from examination of Equation (2.9), is

$$R_3R_2 = R_1R_4 \tag{2.10}$$

Equation (2.10) indicates that whenever a Wheatstone bridge is assembled and resistors are adjusted for a detector null, the resistor values must satisfy the indicated equality. It does *not* matter if the supply voltage drifts or changes; the null is maintained. Equations (2.9) and (2.10) underlie the application of Wheatstone bridges to process-control applications using high-input impedance detectors.

Example 2.2

If a Wheatstone bridge, as shown in Figure 2.4, nulls with $R_1 = 1000\ \Omega$, $R_2 = 842\ \Omega$, and $R_3 = 500\ \Omega$, find the value R_4.

Solution Because the bridge is nulled, find R_4 using

$$R_1R_4 = R_3R_2$$

$$R_4 = \frac{R_3R_2}{R_1} = \frac{(500\ \Omega)(842\ \Omega)}{1000\ \Omega} \tag{2.10}$$

$$R_4 = \mathbf{421\ \Omega}$$

Example 2.3

The resistors in a bridge are given by $R_1 = R_2 = R_3 = 120\ \Omega$ and $R_4 = 121\ \Omega$. If the supply is 10.0 volts, find the voltage offset.

Solution Assuming the detector impedance to be very high, we find the offset from

$$\Delta V = V \frac{R_3R_2 - R_1R_4}{(R_1 + R_3) \cdot (R_2 + R_4)}$$

$$\Delta V = 10V \frac{(120\ \Omega)(120\ \Omega) - (120\ \Omega)(121\ \Omega)}{(120\ \Omega + 120\ \Omega) \cdot (120\ \Omega + 121\ \Omega)} \tag{2.9}$$

$$\Delta V = \mathbf{-20.8\ mV}$$

Galvanometer detector

The use of a galvanometer as a null detector in the bridge circuit introduces some differences in our calculations because the detector resistance may be low and because we must determine the bridge offset as current offset. When the bridge is nulled, Equation (2.10) still defines the relationship between the resistors in the

bridge arms. Equation (2.9) must be modified to allow determination of current drawn by the galvanometer when a null condition is *not* present. Perhaps the easiest way to determine this offset current is first to find the Thévenin equivalent circuit between points a and b of the bridge (as drawn in Figure 2.4 with the detector removed). The Thévenin voltage is simply the open circuit voltage difference between points a and b of the circuit. But wait! Equation (2.9) *is* the open circuit voltage, so

$$V_{Th} = V\frac{R_3R_2 - R_1R_4}{(R_1 + R_3)(R_2 + R_4)} \tag{2.11}$$

The Thévenin resistance is found by replacing the supply voltage by its internal resistance and calculating the resistance between terminals a and b of the network. We may assume that the internal resistance of the supply is negligible compared to the bridge arm resistances. It is left as an exercise for the reader to show that the Thévenin resistance seen at points a and b of the bridge is

$$R_{Th} = \frac{R_1R_3}{R_1 + R_3} + \frac{R_2R_4}{R_2 + R_4} \tag{2.12}$$

The Thévenin equivalent circuit for the bridge enables us easily to determine the current through any galvanometer with internal resistance R_G, as shown in Figure 2.5. In particular, the offset current is

$$I_G = \frac{V_{Th}}{R_{Th} + R_G} \tag{2.13}$$

Using this equation in conjunction with Equation (2.10) defines the Wheatstone bridge response whenever a galvanometer null detector is used.

Example 2.4

A bridge circuit has resistances of $R_1 = R_2 = R_3 = 2.00\ \text{k}\Omega$ and $R_4 = 2.05\ \text{k}\Omega$, and a 5.00-V supply. If a galvanometer with a 50.0 Ω internal resistance is used for a null detector, find the offset current.

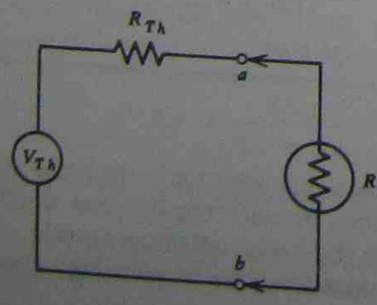


Figure 2.5 When a galvanometer is used for a null detector, it is convenient to use the Thévenin equivalent circuit of the Wheatstone bridge.

Solution From Equation (2.11), the offset voltage is V_{Th}.

$$V_{Th} = 5V\frac{(2\ \text{k}\Omega)(2\ \text{k}\Omega) - (2\ \text{k}\Omega)(2.05\ \text{k}\Omega)}{(2\ \text{k}\Omega + 2\ \text{k}\Omega)(2\ \text{k}\Omega + 2.05\ \text{k}\Omega)}$$

$$V_{Th} = \mathbf{-30.9\ mV} \tag{2.11}$$

We next find the bridge Thévenin resistance.

$$R_{Th} = \frac{(2\ \text{k}\Omega)(2\ \text{k}\Omega)}{(2\ \text{k}\Omega + 2\ \text{k}\Omega)} + \frac{(2\ \text{k}\Omega)(2.05\ \text{k}\Omega)}{(2\ \text{k}\Omega + 2.05\ \text{k}\Omega)}$$

$$R_{Th} = \mathbf{2.01\ k\Omega} \tag{2.12}$$

Finally, the current is

$$I_G = \frac{-30.9\ \text{mV}}{2.01\ \text{k}\Omega + 0.05\ \text{k}\Omega}$$

$$I_G = \mathbf{-15.0\ \mu A} \tag{2.13}$$

Bridge resolution

The resolution of the bridge circuit is a function of the resolution of the null detector used to determine the bridge offset. Thus, referring primarily to the case where a voltage offset occurs, we define the resolution in resistance as that resistance change in one arm of the bridge that causes an offset voltage that is equal to the resolution of the null detector. If a null detector can measure a null to 100 μV, this sets a limit on the minimum measurable resistance change in a bridge using this detector. In general, once given the detector resolution, we may use Equation (2.9) to find the change in resistances from null that causes this offset.

Example 2.5

A bridge circuit has $R_1 = R_2 = R_3 = R_4 = 120.0\ \Omega$ resistances and a 10.0-volt supply. Clearly, the bridge is nulled, as Equation (2.10) shows. If a detector of 10.0-mV resolution is employed to detect the null, find the resolution in resistance change in R_4.

Solution We can simply use Equation (2.8) with R_4 unspecified and find the change in R_4 that will produce a 10.0-mV offset voltage as

$$10\ \text{mV} = \frac{(120\ \Omega)(10\ \text{V})}{120\ \Omega + 120\ \Omega} - \frac{R_4(10V)}{120\ \Omega + R_4}$$

Solving for R_4, we get

$$R_4 = 119.52\ \Omega$$

so the bridge resolution is

$$\Delta R = 0.48\ \Omega$$

In this example, we see that a minimum resistance change of 0.48 Ω must occur before the detector indicates a change in offset voltage.

One may also view this as an overall *accuracy* of the instrument, because it can also be said that ΔR represents the uncertainty in any determination of resistance using the given bridge and detector.

The same arguments can be applied to a galvanometer measurement where the resolution is limited by the minimum measurable current.

Lead compensation

In many process-control applications, a bridge circuit may be located at considerable distance from the sensor whose resistance changes are to be measured. In such cases, the remaining fixed bridge resistors can be chosen to account for the resistance of leads required to connect the bridge to the sensor in providing a null. Furthermore, any measurement of resistance can be adjusted for lead resistance to determine the actual resistance. Another problem exists that is not so easily handled, however. There are many effects that can change the resistance of the long lead wires on a transient basis, such as frequency, temperature, stress, and chemical vapors. Such changes normally are picked up by the bridge response and interpreted as changes in the sensor output. This problem is reduced using *lead compensation*, where any changes in lead resistance are introduced equally into *two* (both) arms of the bridge circuit, thus causing no effective change in bridge offset. Lead compensation is shown in Figure 2.6. Here we see that R_4, which is assumed to be the sensor, has been removed to a remote location with lead wires (1), (2), and (3). Wire (3) is the power lead and has no influence on the bridge balance condition. If wire (2) changes in resistance because of spurious influences, it introduces this change into the R_4 leg of the bridge. Wire (1) is exposed to the same environment and changes by the same amount but is in the

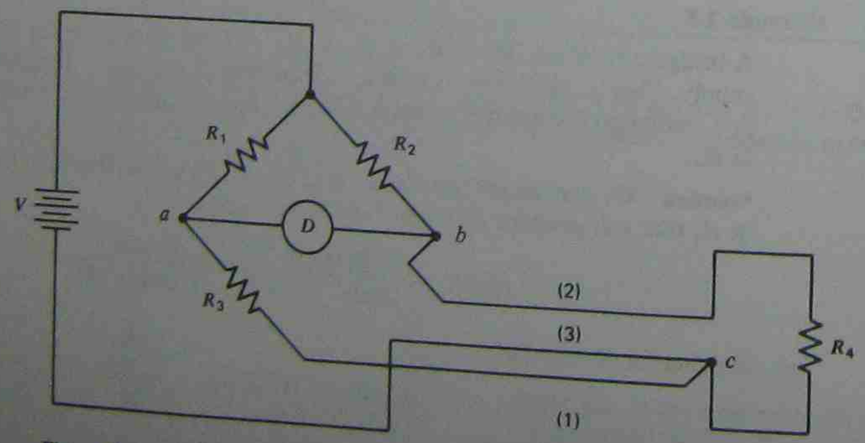


Figure 2.6 For remote sensor applications, a compensation system is used to avoid errors for lead resistance.

R_3 leg of the bridge. Effectively, both R_3 and R_4 are identically changed, and thus Equation (2.10) shows that no change in the bridge null occurs. This type of compensation is often employed where bridge circuits must be used with long leads to the active element of the bridge.

Current balance bridge

One disadvantage of the simple Wheatstone bridge is the need to obtain a null by variation of resistors in bridge arms. In the past, many process-control applications used a feedback system in which the bridge offset voltage was amplified and used to drive a motor whose shaft altered a variable resistor to renull the bridge. Such a system does not suit the modern technology of electronic processing because it is not very fast, is subject to wear, and generates electronic noise. A technique that provides for an electronic nulling of the bridge and that uses only fixed resistors (except as may be required for calibration) can be used with the bridge. This method uses a *current* to null the bridge. A closed-loop system can even be constructed that provides the bridge with a *self-nulling* ability.

The basic principle of the current balance bridge is shown in Figure 2.7. The standard Wheatstone bridge is modified by splitting one arm resistor into two, R_4 and R_5. A current I is fed into the bridge through the junction of R_4 and R_5 as shown. We now stipulate that the size of the bridge resistors is such that the current flows predominantly through R_5. This can be provided for by any of several requirements. The least restrictive is to require

$$R_4 \gg R_5 \tag{2.14}$$

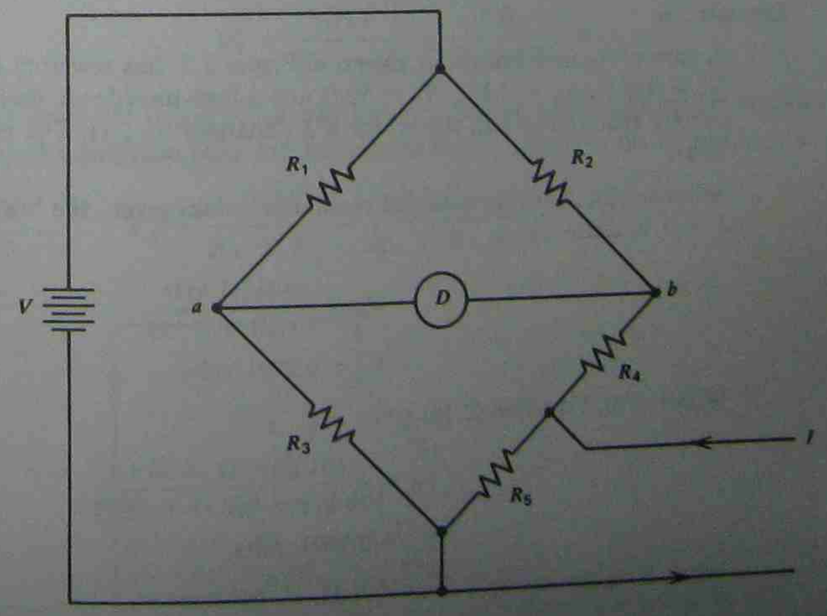


Figure 2.7 The current balance bridge.

Often, if a high-impedance null detector is used, then the restriction of Equation (2.14) becomes

$$(R_2 + R_4) \gg R_5 \tag{2.15}$$

Assuming that either conditions of Equations (2.14) or (2.15) are satisfied, the voltage at point b is the sum of the divided supply voltage plus the voltage dropped across R_5 from the current I.

$$V_b = \frac{V(R_4 + R_5)}{R_2 + R_4 + R_5} + IR_5 \tag{2.16}$$

The voltage of point a is still given by Equation (2.6). Thus, the bridge offset voltage is given by $\Delta V = V_a - V_b$, or

$$\Delta V = \frac{VR_3}{R_1 + R_3} - \frac{V(R_4 + R_5)}{R_2 + R_4 + R_5} - IR_5 \tag{2.17}$$

This equation shows that a null is reached by adjusting the magnitude and polarity of the current I until IR_5 equals the voltage difference of the first two terms. If one of the bridge resistors changes, the bridge can be renulled by changing current I. In this manner, the bridge is electronically nulled from any convenient current source. In most applications the bridge is nulled at some nominal set of resistances with zero current. Changes of a bridge resistor are detected as a bridge offset signal that is used to provide the renulling current. The action is explained in Example 2.6.

Example 2.6

A current balance bridge, as shown in Figure 2.7, has resistors $R_1 = R_2 = 10\ \text{k}\Omega$, $R_4 = 950\ \Omega$, $R_3 = 1\ \text{k}\Omega$, $R_5 = 50\ \Omega$ and a high-impedance null detector. Find the current required to null the bridge if R_3 changes by 1 Ω. The supply voltage is 10 volts.

Solution First, for the nominal resistance values given, the bridge is at a null with $I = 0$, because

$$V_a = \frac{(10V)(1\ \text{k}\Omega)}{10\ \text{k}\Omega + 1\ \text{k}\Omega}$$

$$V_a = 0.9091 \text{ volts} \tag{2.6}$$

With $I = 0$, Equation (2.16) gives

$$V_b = \frac{(10V)(950\ \Omega + 50\ \Omega)}{10\ \text{k}\Omega + 950\ \Omega + 50\ \Omega}$$

$$V_b = 0.9091 \text{ volts} \tag{2.16}$$

When R_3 increases by 1 Ω to 1001 Ω, V_a becomes

$$V_a = \frac{(10V)(1001)}{10\ \text{k}\Omega + 1001}$$

$$V_a = 0.9099 \text{ volts}$$

which shows that the voltage at b must increase by 0.0008 volts or 0.8 mV to renull the bridge. This can be provided by a current, from Equation (2.17) with $\Delta V = 0$, of $50I = 0.8$ mV.

$$\mathbf{I = 16.0\ \mu A}$$

Potential measurements using bridges

A bridge circuit is also useful to measure small potentials at a very high impedance, using either a conventional Wheatstone bridge or a current balance bridge. This type of measurement is performed by placing the potential to be measured in series with the null detector, as shown in Figure 2.8. The null detector responds to the potential between points c and b. In this case, V_b is given by Equation (2.7) and V_c by

$$V_c = V_x + V_a \tag{2.18}$$

where V_a is given by Equation (2.6), and V_x is the potential to be measured. The voltage appearing across the null detector is

$$\Delta V = V_c - V_b = V_x + V_a - V_b$$

A null condition is established when $\Delta V = 0$; furthermore, no current flows through the unknown potential when such a null is found. Thus, V_x can be measured by varying bridge resistors to provide a null with V_x in the circuit and solving for V_x using the null condition

$$V_x + \frac{R_3 V}{R_1 + R_3} - \frac{VR_4}{R_2 + R_4} = 0 \tag{2.19}$$

A similar analysis using a current balance bridge and fixed bridge resistors provides a null condition that can be solved for V_x in terms of the nulling current I.

$$V_x + \frac{R_3 V}{R_1 + R_3} - \frac{V(R_4 + R_5)}{R_2 + R_4 + R_5} - IR_5 = 0 \tag{2.20}$$

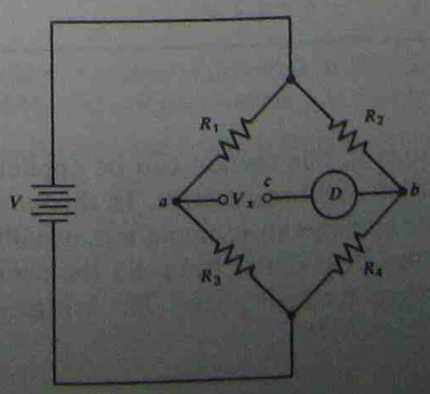


Figure 2.8 Using the basic Wheatstone bridge for potential measurement.

If the fixed resistors are chosen to null the bridge with $I = 0$ when $V_x = 0$, then the two middle terms in Equation (2.20) cancel leaving a very simple relationship between V_x and the nulling current

$$V_x - IR_5 = 0 \tag{2.21}$$

Example 2.7

A bridge circuit for potential measurement nulls when $R_1 = R_2 = 1\ \text{k}\Omega$, $R_3 = 605\ \Omega$, and $R_4 = 500\ \Omega$ with a 10-volt supply. Find the unknown potential.

Solution Here we simply use Equation (2.19) to solve for V_x.

$$V_x + \frac{(605)(10)}{605 + 1000} - \frac{(10)(500)}{1000 + 500} = 0$$

$$V_x + 3.769 - 3.333 = 0 \tag{2.19}$$

$$V_x = \mathbf{-0.436\ volts}$$

Example 2.8

A current balance bridge is used for potential measurement. The fixed resistors are $R_1 = R_2 = 5\ \text{k}\Omega$, $R_3 = 1\ \text{k}\Omega$, $R_4 = 990\ \Omega$, and $R_5 = 10\ \Omega$ with a 10-volt supply. Find the current necessary to null the bridge if the potential is 12 mV.

Solution First, an examination of the resistances shows that the bridge is nulled when $I = 0$ and $V_x = 0$ because, from Equation (2.20),

$$\frac{VR_3}{R_1 + R_3} = \frac{10(1\ \text{k})}{1\ \text{k} + 5\ \text{k}} = 1.667\ \text{volts}$$

and

$$\frac{V(R_4 + R_5)}{R_2 + R_4 + R_5} = \frac{10(990 + 10)}{5\ \text{k} + 990 + 10} = 1.667\ \text{volts}$$

Thus, we can use Equation (2.21)

$$12\ \text{mV} - 10I = 0$$

$$I = \mathbf{1.2\ mA}$$

Ac bridges

The bridge concept described in this section can be applied to the matching of impedances in general as well as to resistances. In this case, the bridge is represented as in Figure 2.9 and employs an ac excitation, usually a sine wave voltage signal. The analysis of bridge behavior is basically the same as in the previous treatment, but impedances replace resistances. The bridge offset voltage then is represented as

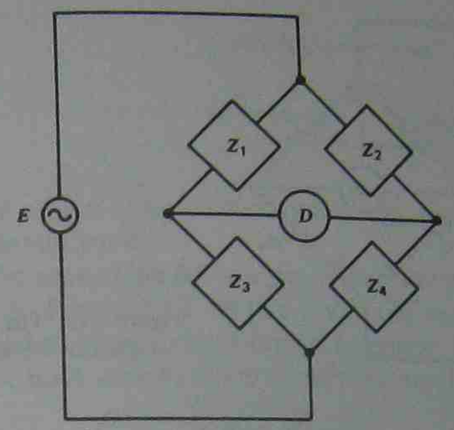


Figure 2.9 A general ac bridge circuit.

$$\Delta E = E\frac{Z_3Z_2 - Z_1Z_4}{(Z_1 + Z_3)(Z_2 + Z_4)} \tag{2.22}$$

ΔE = ac offset voltage

where

E = sine wave excitation voltage

Z_1, Z_2, Z_3, Z_4 = bridge impedances

A null condition is defined as before by a zero offset voltage $\Delta E = 0$. From Equation (2.22), this condition is met if the impedances satisfy the relation

$$Z_3Z_2 = Z_1Z_4 \tag{2.23}$$

This condition is analogous to Equation (2.10) for resistive bridges.

A special note is necessary concerning the achievement of a null in ac bridges. In some cases, the null detection system is phase sensitive with respect to the bridge excitation signal. In these instances, it is necessary to provide a null of both the in-phase and quadrature (90° out-of-phase) signals before Equation (2.23) applies.

Example 2.9

An ac bridge employs impedances as shown in Figure 2.10. Find the value of R_x and C_x when the bridge is nulled.

Solution Because the bridge is at null, we have

$$Z_2Z_3 = Z_1Z_x \tag{2.23}$$

or

$$R_2\left(R_3 - \frac{j}{\omega C}\right) = R_1\left(R_x - \frac{j}{\omega C_x}\right)$$

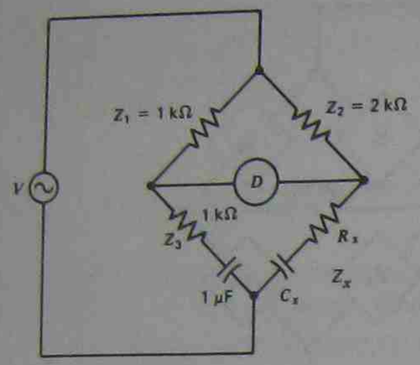


Figure 2.10 The ac bridge circuit and components for Example 2.9.

$$R_2R_3 - j\frac{R_2}{\omega C} = R_1R_x - \frac{jR_1}{\omega C_x}$$

The real and imaginary parts must be independently satisfied so that

$$R_x - \frac{R_2R_3}{R_1} = 0$$

$$R_x = \frac{(2\ \text{k}\Omega)(1\ \text{k}\Omega)}{1\ \text{k}\Omega}$$

$$R_x = \mathbf{2\ k\Omega}$$

and

$$C_x = C\frac{R_1}{R_2}$$

$$C_x = (1\ \mu\text{F})\frac{1\ \text{k}\Omega}{2\ \text{k}\Omega}$$

$$C_x = \mathbf{0.5\ \mu F}$$

2.3.3 *RC* Filters

To eliminate unwanted noise signals from measurements, it is often necessary to use circuits that block certain frequencies or bands of frequencies. These circuits are called *filters*. In many cases a simple filter can be constructed from a single resistor and a single capacitor to accomplish the desired rejection.

Low-pass *RC* filter

The simple circuit shown in Figure 2.11 is called a *low-pass RC* filter. It is called low-pass because it blocks high frequencies and passes low frequencies. It would be most desirable if a low-pass filter had a characteristic such that all signals with

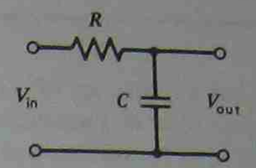


Figure 2.11 Circuit for the low-pass *RC* filter.

frequency above some critical value are simply rejected. Unfortunately, such circuits do not exist.

In the case of the *RC* low-pass filter, the variation of rejection with frequency is shown in Figure 2.12. In this graph the vertical is the ratio of output voltage to the input voltage without regard to phase. When this ratio is one, the signal is passed without effect; when it is very small or zero, the signal is effectively blocked.

The horizontal is actually the logarithm of the ratio of the input voltage signal frequency to a *critical frequency*. This critical frequency is that frequency for which the ratio of the output to the input voltage is 0.707. In terms of the resistor and capacitor, the critical frequency is given by

$$f_c = 1/(2\pi RC) \tag{2.24}$$

The voltage ratio for any signal frequency can be determined graphically from Figure 2.12 or can be computed by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{[1 + (f/f_c)^2]^{1/2}} \tag{2.25}$$

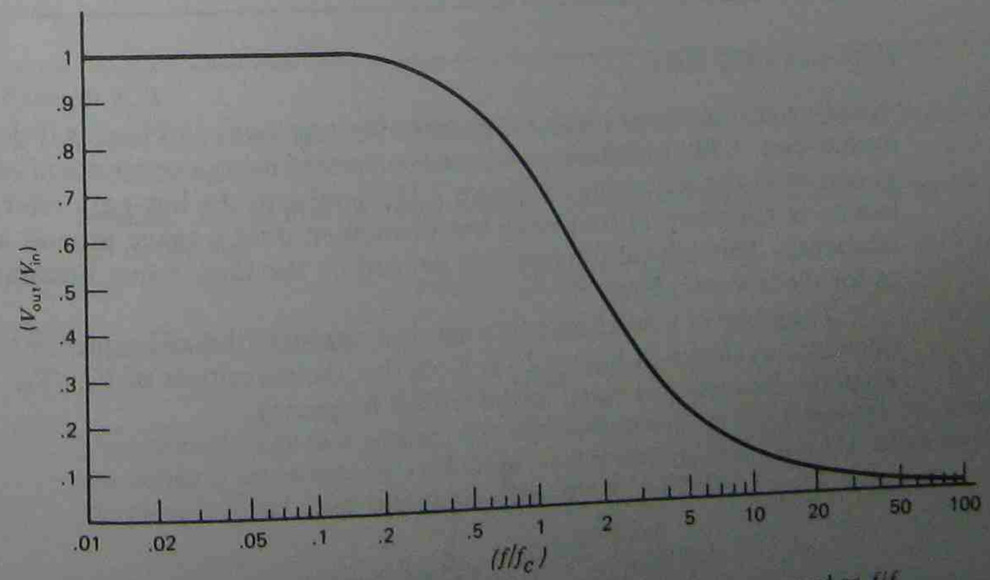


Figure 2.12 Variation of V_{out}/V_{in} as a function of frequency expressed as f/f_c and plotted on a semilog graph.

Example 2.10

A measurement signal has a frequency of <1 kHz, but there is unwanted noise at 1 MHz. Design a low-pass filter that attenuates the noise to 1%. What is the effect on the measurement signal at its maximum of 1 kHz?

Solution Use Equation (2.25) to determine what critical frequency will give $(V_{out}/V_{in}) = 0.01$ at 1 MHz. To do this we have the relationship

$$0.01 = \frac{1}{[1 + (1\text{ MHz}/f_c)^2]^{1/2}}$$

which gives us

$$(1\text{ MHz}/f_c)^2 = 9999$$

or

$$f_c = 10\text{ kHz}$$

Any resistor and capacitor combination that gives this critical frequency will be a correct solution. Let us pick a capacitor of some practical value, say, 0.01 μF; then, from Equation (2.24), the resistor is

$$R = 1/[2\pi(0.01\ \mu\text{F})(10\text{ kHz})] = 1.59\text{ k}\Omega$$

To determine the effect on a signal of 1 kHz, we use the graph of Figure 2.12 or Equation (2.25) with the (now) known critical frequency of 10 kHz. The graph is used first to find $(f/f_c) = (1\text{ kHz}/10\text{ kHz}) = 0.1$; from the graph you can see that the rejection is very small. Equation (2.25) can be used to find the rejection more accurately, that is, $(V_{out}/V_{in}) = 0.995$. Thus, the measurement signal at maximum frequency is attenuated by only 0.5%.

High-pass *RC* filter

A high-pass filter passes high frequencies (no rejection) and blocks (rejects) low frequencies. A filter of this type can be constructed using a resistor and capacitor, as shown in the schematic of Figure 2.13. Similar to the low-pass filter, the rejection is not sharp in frequency but distributed over a range around a critical frequency. This critical frequency is defined by the *same* value Equation (2.24) as for the low-pass filter.

The graph of voltage output to input versus logarithm of frequency to critical frequency is shown in Figure 2.14. Note that the magnitude of $V_{out}/V_{in} = 0.707$ when the frequency is equal to the critical frequency.

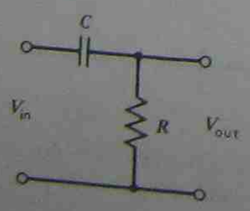


Figure 2.13 Circuit for the high-pass *RC* filter.

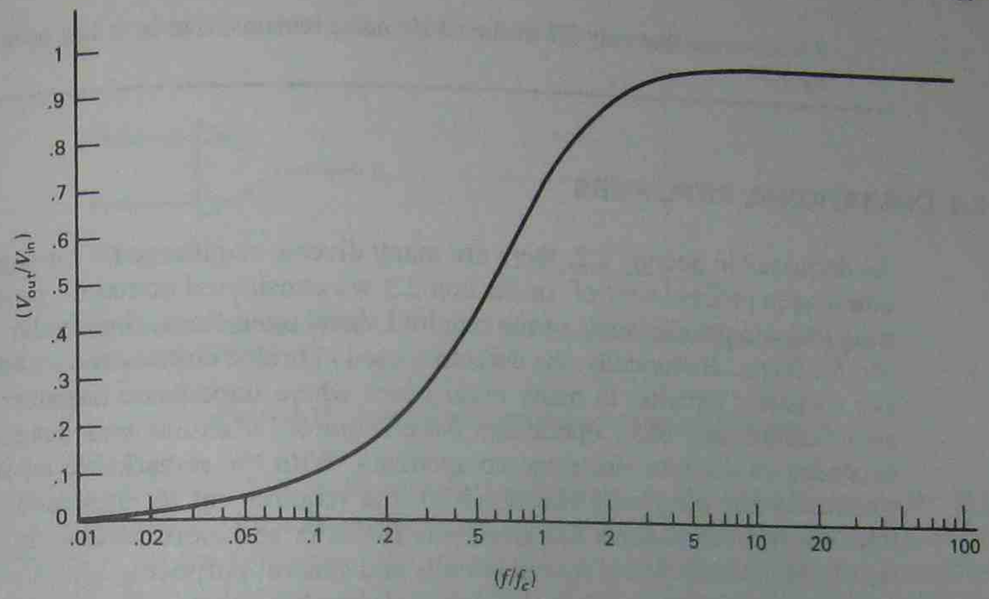


Figure 2.14 Variation of V_{out}/V_{in} as a function of frequency expressed as f/f_c and plotted on a semilog graph.

An equation for the ratio of output voltage to input voltage as a function of the frequency for the high-pass filter is found to be

$$V_{out}/V_{in} = \frac{(f/f_c)}{[1 + (f/f_c)^2]^{1/2}} \tag{2.26}$$

Example 2.11

Pulses for a stepping motor are being transmitted at 2000 Hz. Design a filter to reduce 60-Hz noise, but reduce the pulses by no more than 3 dB.

Solution Let us first find what voltage ratio corresponds to a 3-dB reduction. We remember that

$$P(\text{dB}) = 20\log(V_{out}/V_{in})$$

so *down* by 3 dB means that $P = -3$. Therefore

$$(V_{out}/V_{in}) = 10^{-3/20} = 0.707$$

You probably saw that coming. The critical frequency is that frequency for which the output is attenuated by 3 dB. Thus, in this case, $f_c = 2$ kHz. The effect on 60-Hz noise is found using Equation (2.26), with $f = 60$ Hz.

$$V_{out}/V_{in} = \frac{(60/2000)}{[1 + (60/2000)^2]^{1/2}}$$

$$V_{out}/V_{in} = 0.03$$

Thus, we see that only 3% of the 60-Hz noise remains; that is, it has been reduced by 97%.

2.4 OPERATIONAL AMPLIFIERS

As discussed in Section 2.2, there are many diverse requirements for signal conditioning in process control. In Section 2.3 we considered common, passive circuits that can provide some of the required signal operations, the divider, bridge, and *RC* filters. Historically, the detectors used in bridge circuits consisted of tube and transistor circuits. In many other cases where impedance transformations, amplification, and other operations were required, a circuit was designed that depended on discrete electronic components. With the remarkable advances in electronics and integrated circuits (ICs), the requirement to implement designs from discrete components has given way to easier and more reliable methods of signal conditioning. Many special circuits and general-purpose amplifiers are now contained in integrated circuit (IC) packages producing a quick solution to signal conditioning problems together with small size, low power consumption, and low cost.

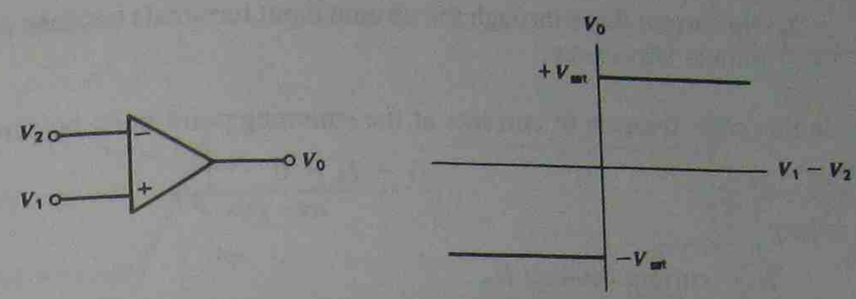
In general, the application of ICs requires familiarity with an available line of such devices, their specifications and limitations, before they can be applied to a specific problem. Apart from these specialized ICs, there also is a type of amplifier that finds wide application as the building block of signal conditioning applications. This device, called an operational amplifier (op amp), has been in existence for many years. It was first constructed from tubes, then from discrete transistors, and now as integrated circuits. Although many lines of op amps with diverse specifications exist from many manufacturers, they all have common characteristics of operation that can be employed in basic designs relating to any general op amp.

2.4.1 Op Amp Characteristics

Taken alone, an op amp is an exceedingly simple and apparently useless electronic amplifier. In Figure 2.15a we see the standard symbol of an op amp with the designations (+) input, (−) input, and the output. The (+) input is also called the *noninverting* input and the (−) the *inverting* input. The relation of op amp input to output is very simple indeed, as will be seen by considering an idealization of its description.

Ideal op amp

To describe the response of an ideal op amp, we label V_1 the voltage on the (+) input, V_2 the voltage on the (−) input terminal, and V_0 the output voltage. Ideally, if $V_1 - V_2$ is positive ($V_1 > V_2$), then V_0 saturates positively. If $V_1 - V_2$ is



a) Operational amplifier (op amp) symbol

b) Relation between input and output

Figure 2.15 Symbol and ideal characteristics of an op amp.

negative ($V_2 > V_1$), then V_0 saturates negatively, as shown in Figure 2.15b. The (−) input is called the inverting input. If the voltage on this input is more positive than that on the (+) input, the output saturates negatively. This ideal amplifier has infinite gain because an infinitesimal difference between V_1 and V_2 results in a saturated output.

Other characteristics of ideal op amps are (1) an infinite impedance between inputs and (2) a zero output impedance. Basically, the op amp is a device that has only two output states: $+V_{sat}$ and $-V_{sat}$. In practice, the device is always used with feedback of output to input. Such feedback permits implementation of many special relationships between input and output voltage.

Ideal inverting amplifier

To see how the op amp is used, let us consider the circuit of Figure 2.16. Resistor R_2 is used to feed back the output to the inverting input of the op amp, and R_1 connects the input voltage V_{in} to this same point. The common connection is called the summing point. We can see that with no feedback and the (+) grounded, $V_{in} > 0$ saturates the output negative and $V_{in} < 0$ saturates the output positive. With feedback, the output adjusts to a voltage such that

1. The summing point voltage is equal to the (+) op amp input level, zero in this case.

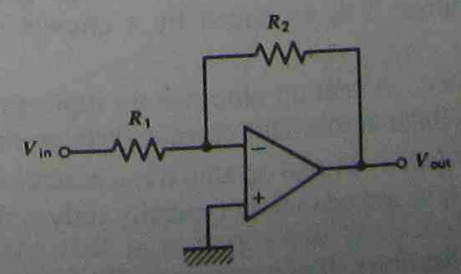


Figure 2.16 Inverting amplifier using an op amp.

2. No current flows through the op amp input terminals because of the assumed infinite impedance.

In this case, the sum of currents at the summing point must be zero.

$$I_1 + I_2 = 0 \tag{2.27}$$

where

I_1 = current through R_1
I_2 = current through R_2

Because the summing point potential is assumed to be zero, we have

$$\frac{V_{in}}{R_1} + \frac{V_{out}}{R_2} = 0 \tag{2.28}$$

From Equation (2.27), we can write the circuit response as

$$V_{out} = -\frac{R_2}{R_1} V_{in} \tag{2.29}$$

Thus, the circuit of Figure 2.16 is an inverting *amplifier* with gain R_2/R_1 that is shifted 180° in phase (inverted) from the input. This device is also an *attenuator* by making $R_2 < R_1$.

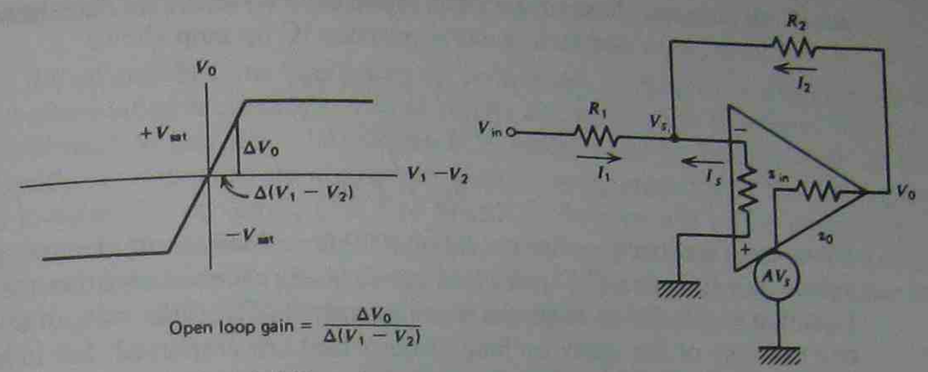
A similar approach may be applied to the ideal analysis of many other op amp circuits where steps (1) and (2) lead to equations such as Equations (2.27) and (2.28). We must note, however, that the inverting amplifier of Figure 2.16 has an input impedance of R_1 that, in general, may not be high. Thus, although blessed with the virtue of variable gain or attenuation, the circuit does not have inherently high-input impedance.

Nonideal effects

Analysis of op amp circuits with nonideal response is performed by considering the following parameters:

1. *Finite open loop gain* A real op amp has finite voltage gain, as shown by the amplifier response in Figure 2.17a. The voltage gain is defined as the change in output voltage ΔV_0 produced by a change in differential input voltage $\Delta[V_1 - V_2]$.
2. *Finite input impedance* A real op amp has an input impedance and, consequently, a finite voltage across and current through input terminals.
3. *Nonzero output impedance* A real op amp has a nonzero output impedance, although this low output impedance is typically only a few ohms.

In most modern applications, these nonideal effects can be ignored in de-



a) Nonideal characteristics of an op amp

b) Nonideal effects

Figure 2.17 Types of nonideal effects in op amp and circuit analysis.

signing op amp circuits. For example, consider the circuit of Figure 2.17b, where the finite impedances and gain of the op amp have been included. We can employ standard circuit analysis to find the relationship between input and output voltage for this circuit. Summing the currents at the summing point gives

$$I_1 + I_2 + I_s = 0$$

Then, each current can be identified in terms of the circuit parameters to give

$$\frac{V_{in} - V_s}{R_1} + \frac{V_0 - V_s}{R_2} - \frac{V_s}{z_{in}} = 0$$

Finally, V_0 can be related to the op amp gain as

$$V_0 = AV_s - \left(\frac{V_0 - V_s}{R_2}\right) z_0$$

Now, combining the equations, we find

$$V_0 = -\frac{R_2}{R_1}\left(\frac{1}{1 - \mu}\right) V_{in} \tag{2.30}$$

where

$$\mu = \frac{\left(1 + \frac{z_0}{R_2}\right)\left(1 + \frac{R_2}{R_1} + \frac{R_2}{z_{in}}\right)}{\left(A + \frac{z_0}{R_2}\right)} \tag{2.31}$$

If we assume that μ is very small compared with unity, then Equation (2.30) reduces to the ideal case given by Equation (2.29). Indeed, if typical values for

an IC op amp are chosen for a case where $R_2/R_1 = 100$, we can show that $\mu \ll 1$. For example, a common, general-purpose IC op amp shows

$$A = 200{,}000$$

$$z_o = 75\ \Omega$$

$$z_{in} = 2\ \text{M}\Omega$$

If we use a feedback resistance R_2 of 100 kΩ and substitute the aforementioned values into Equation (2.31), we find $\mu \approx 0.0005$, which shows that the gain from Equation (2.30) differs from the ideal by only 0.05%. This was, of course, only one example of the many op amp circuits that are employed, but in most cases a similar analysis shows that the ideal characteristics may be assumed.

2.4.2 Op Amp Specifications

There are characteristics of op amps other than those given in the previous section that enter into design applications. These characteristics are given in the specifications for particular op amps together with the open loop gain and input and output impedance previously defined. Several of these characteristics are as follows:

- *Input offset voltage* In many cases, the op amp output voltage may not be zero when the voltage across the input is zero. The voltage that must be applied across the input terminals to drive the output to zero is the *input offset voltage*.
- *Input offset current* Just as a voltage offset may be required across the input to zero the output voltage, so a net current may be required between the inputs to zero the output voltage. Such a current is referred to as an *input offset current*. This is taken as the difference of the two input currents.
- *Input bias current* This is the average of the two input currents required to drive the output voltage to zero.
- *Slew rate* If a voltage is suddenly applied to the input of an op amp, the output will saturate to the maximum. For a step input the *slew rate* is the rate at which the output changes to the saturation value. This typically is expressed as volts per microsecond (V/μs).
- *Unity gain frequency bandwidth* The frequency response of an op amp is typically defined by a Bode plot of open loop voltage gain versus frequency. Such a plot is very important for the design of circuits that deal with ac signals. It is beyond the scope of this text to consider the details of designs employing Bode plots. Instead, the gross frequency behavior can be seen by determination of the frequency at which the open loop gain of the op amp has become unity, thus defining the *unity gain frequency bandwidth*.

2.5 OP AMP CIRCUITS IN INSTRUMENTATION

As the op amp became familiar to the individuals working in process control and instrumentation technology, a large variety of circuits were developed with direct application to this field. In general, it is much easier to develop a circuit for a specific service using op amps than discrete components; with the development of low-cost IC op amps, it is also practical. Perhaps one of the greatest disadvantages is the requirement of a bipolar power supply for the op amp. This section presents a number of typical circuits and their basic characteristics together with a derivation of the circuit response assuming an ideal op amp.

2.5.1 Voltage Follower

Figure 2.18 shows an op amp circuit with unity gain and very high input impedance. The input impedance is essentially the input impedance of the op amp itself, which can be greater than 100 MΩ. The voltage output tracks the input over a range defined by the plus and minus saturation voltage outputs. Current output is limited to the short circuit current of the op amp, and output impedance is typically much less than 100 Ω. In many cases a manufacturer will market an op amp voltage follower whose feedback is provided internally. Such a unit is usually specifically designed for very high input impedance. The unity gain voltage follower is essentially an impedance transformer in the sense of converting a voltage at high impedance to the same voltage at low impedance.

2.5.2 Inverting Amplifier

The inverting amplifier has already been discussed in connection with our treatment of op amp characteristics. Equation (2.29) shows that this circuit inverts the input signal and may have either attenuation or gain depending on the ratio of input resistance R_1 and feedback resistance R_2. The circuit for this amplifier is shown in Figure 2.16. It is important to note that input impedance of this circuit is essentially equal to R_1, the input resistance. In general, this resistance is not large, and hence the input impedance is not large.

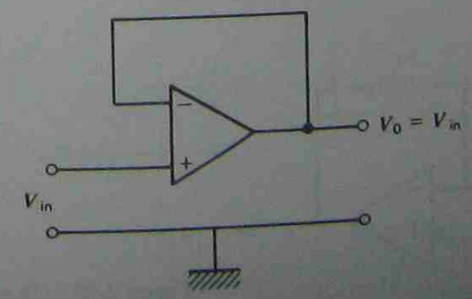


Figure 2.18 An op amp voltage follower. This circuit has a very high impedance; depending on the op amp, it may be 10^6 to 10^{11} Ω. This circuit serves as an impedance transformer.

Summing amplifier

A common modification of the inverting amplifier is an amplifier that sums or adds two or more applied voltages. This circuit is shown in Figure 2.19 for the case of summing two input voltages. The transfer function of this amplifier is given by

$$V_{out} = -\left[\frac{R_2}{R_1} V_1 + \frac{R_2}{R_3} V_2\right] \tag{2.32}$$

The sum can be scaled by proper selection of resistors. For example, if we make $R_1 = R_2 = R_3$, then the output is simply the (inverted) sum of V_1 and V_2. The average can be found by making $R_1 = R_3$ and $R_2 = R_1/2$.

Example 2.12

Develop an op amp circuit that can provide an output voltage that is related to the input voltage by

$$V_{out} = 3.4V_{in} + 5$$

Solution There are many ways to do this. One way is to use a summing amplifier with V_{in} on one input and 5 volts on the other. The gains will be selected to be 3.4 and 1.0, respectively. The summing amplifier of Figure 2.19 is also an inverter, however, so the sign will be wrong. Thus, a second amplifier will be used with a gain of -1 to make the sign correct. The result is shown in Figure 2.20. Selection

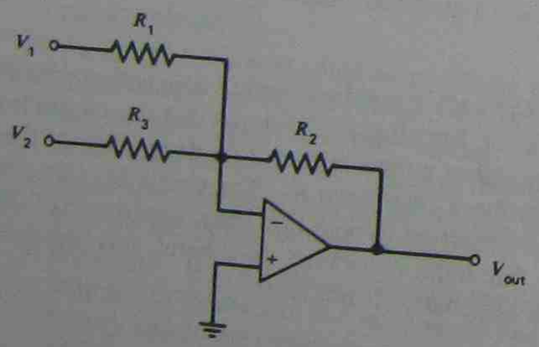


Figure 2.19 Summing amplifier.

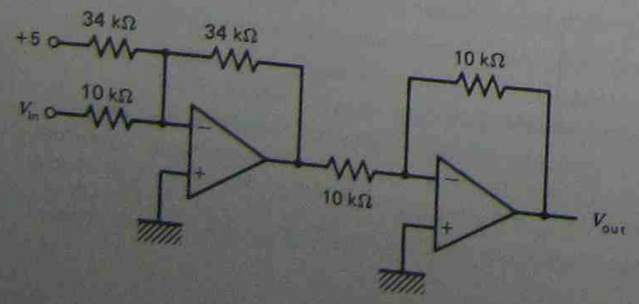


Figure 2.20 Op amp solution to Example 2.12.

of the values of the resistors is based on the general notion of keeping the currents in milliamperes.

2.5.3 Noninverting Amplifier

A noninverting amplifier may be constructed from an op amp, as shown in Figure 2.21. The gain of this circuit is found by summing the currents at the summing point S, and using the fact that the summing point voltage is V_{in} so that no voltage difference appears across the input terminals.

$$I_1 + I_2 = 0$$

where

I_1 = current through R_1
I_2 = current through R_2

But these currents can be found from Ohm's law such that this equation becomes

$$\frac{V_{in}}{R_1} + \frac{V_{in} - V_{out}}{R_2} = 0$$

Solving this equation for V_{out}, we find

$$V_{out} = \left[1 + \frac{R_2}{R_1}\right] V_{in} \tag{2.33}$$

Equation (2.33) shows that the noninverting amplifier has a gain that depends on the ratio of feedback resistor R_2 and the ground resistor R_1, but this gain can never be used for voltage attenuation. Because the input is taken directly into the noninverting input of the op amp, the input impedance is very high since it is effectively equal to the op amp input impedance.

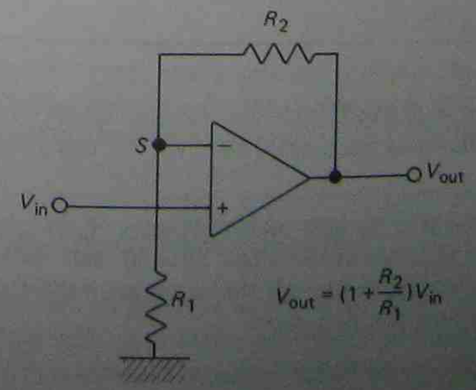


Figure 2.21 Noninverting amplifier.

Example 2.13

Design a high-impedance amplifier with a voltage gain of 42.

Solution We use the noninverting circuit of Figure 2.21 with resistors selected from

$$V_{out} = \left[1 + \frac{R_2}{R_1}\right] V_{in}$$

$$42 = 1 + \frac{R_2}{R_1} \tag{2.33}$$

$$R_2 = 41R_1$$

so we could choose $R_1 = \mathbf{1\ k\Omega}$, which requires $R_2 = \mathbf{41\ k\Omega}$.

2.5.4 Differential Amplifier

Frequently, in the instrumentation associated with process control, differential voltage amplification is required (for example, for a bridge circuit). A differential amplifier is constructed using an op amp, as shown in Figure 2.22a. Analysis of this circuit shows that the output voltage is given by

$$V_{out} = \frac{R_2}{R_1}(V_2 - V_1) \tag{2.34}$$

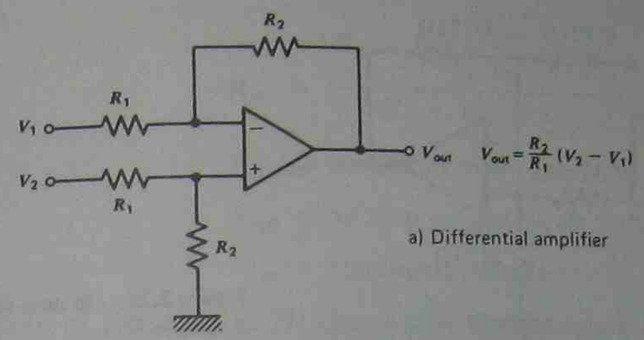
This circuit has a variable gain or attenuation given by the ratio of R_2 and R_1 and responds to the difference in voltage inputs as required. It is very important that the resistors in Figure 2.22a that have the same indicated value be carefully matched to assure rejection of voltage common to both inputs. A significant disadvantage of this circuit is that the input impedance at each input terminal is not large, that is, $R_1 + R_2$ at the V_2 input and R_1 at the V_1 input. To employ this circuit when a high input impedance differential amplification is desired, voltage followers may be employed before each input, as shown in Figure 2.22b. This circuit makes a very versatile high-gain, high-input impedance differential amplifier for use in instrumentation systems.

Example 2.14

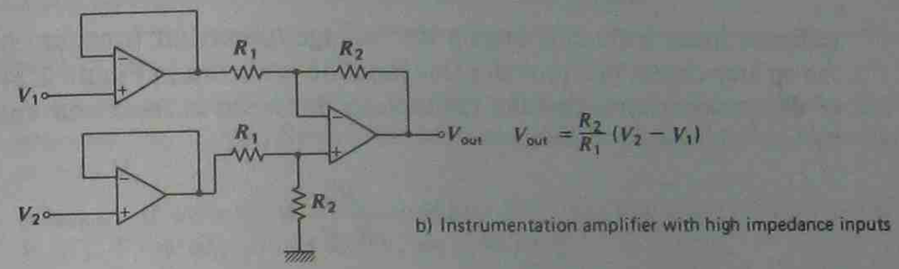
A sensor outputs a range of 20.0 to 250 mV as a variable varies over its range. Develop signal conditioning so that this becomes 0 to 5 V. The circuit must have very high input impedance.

Solution A very logical way to approach problems of this sort is to develop an equation for the output in terms of the input, such as that shown in Example 2.12. A circuit can then be developed to provide the variation of the equation. The equation is that of a straight line; we can then write

$$V_{out} = mV_{in} + V_0$$



a) Differential amplifier



b) Instrumentation amplifier with high impedance inputs

Figure 2.22 Differential amplifiers. (a) Differential amplifier. (b) Instrumentation amplifier with high-impedance inputs.

where m is the slope of the line and represents the gain ($m > 1$) or attenuation ($m < 1$) required and V_0 is the intercept; that is, the value V_{out} would be if $V_{in} = 0$.

For the two conditions we have in this problem, form two equations to solve for m and V_0.

$$0 = m(0.02) + V_0$$

$$5 = m(0.25) + V_0$$

We get $m = 21.7$ and $V_0 = -0.434$ V using standard algebra. The equation is

$$V_{out} = 21.7V_{in} - 0.434$$

This also can be written in the form

$$V_{out} = 21.7(V_{in} - 0.02)$$

There are many, many circuits that provide this answer. Figure 2.23 shows one. Notice the voltage follower on the input that provides high input impedance and a differential amplifier with a gain of 21.7. The 0.02 volts could be provided by a divider from a well-regulated source.

2.5.5 Voltage-to-Current Converter

Because signals in process control are most often transmitted as a current, specifically 4–20 mA, it is often necessary to employ a linear voltage-to-current converter. Such a circuit must be capable of sinking a current into a number of

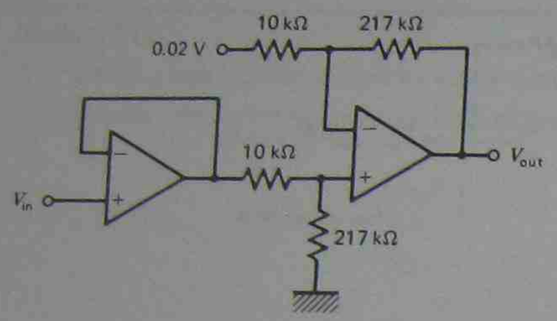


Figure 2.23 Op amp solution to Example 2.14.

different loads without changing the voltage-to-current transfer characteristics. An op amp circuit that provides this function is shown in Figure 2.24. An analysis of this circuit shows that the relationship between current and voltage is given by

$$I = -\frac{R_2}{R_1 R_3} V_{in} \tag{2.35}$$

provided that the resistances are selected so that

$$R_1(R_3 + R_5) = R_2 R_4 \tag{2.36}$$

The circuit can deliver current in either direction, as required by a particular application.

The maximum load resistance and maximum current are related and determined by the condition that the amplifier output saturates in voltage. Analysis of the circuit shows that when the op amp output voltage saturates, the maximum load resistance and maximum current are related by

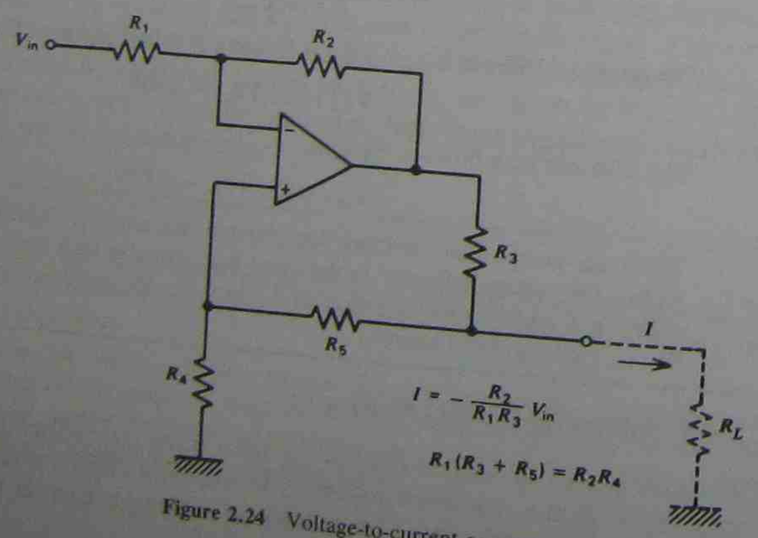


Figure 2.24 Voltage-to-current converter.

$$R_{ml} = \frac{(R_4 + R_5)\left[\frac{V_{sat}}{I_m} - R_3\right]}{R_3 + R_4 + R_5} \tag{2.37}$$

R_{ml} = maximum load resistance

V_{sat} = op amp saturation on voltage

I_m = maximum current

A study of Equation (2.37) shows that the *maximum* load resistance is always less than V_{sat}/I_m. The *minimum* load resistance is zero.

Example 2.15

A sensor outputs 0 to 1 volts. Develop a voltage-to-current convertor so that this becomes 0 to 10 mA. Specify the maximum load resistance if the op amp saturates at ±10 V.

Solution If we make $R_1 = R_2$ in Figure 2.24, then Equation (2.35) reduces to $I = V_{in}/R_3$. To satisfy 10 mA at 1 V, we must have

$$R_3 = 1 \text{ V}/10 \text{ mA} = 100\ \Omega$$

Let us take $R_5 = 0$ (which is allowed) so that Equation (2.36) also specifies

$$R_3 = R_4 = 100\ \Omega$$

This completes the voltage-to-current converter. The maximum load resistance is found from Equation (2.37).

$$R_{ml} = 100[10 \text{ V}/10 \text{ mA} - 100]/200$$

$$R_{ml} = 450\ \Omega$$

2.5.6 Current-to-Voltage Converter

At the receiving end of the process-control signal transmission system, we often need to convert the current back into a voltage. This can be done most easily with the circuit shown in Figure 2.25. This circuit provides an output voltage

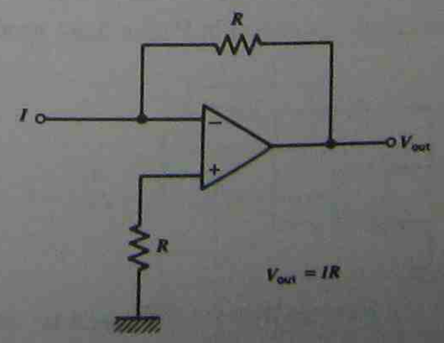


Figure 2.25 Current-to-voltage converter.

given by

$$V_{out} = IR \tag{2.38}$$

provided the op amp saturation voltage has not been reached. The resistor R in the noninverting terminal is employed to provide temperature stability to the configuration.

2.5.7 Integrator

The last regular op amp circuit to be considered is the *integrator*. This configuration, shown in Figure 2.26, consists of an input resistor and feedback capacitor. Using the ideal analysis, we can sum the currents at the summing point as

$$\frac{V_{in}}{R} + C\frac{dV_{out}}{dt} = 0 \tag{2.39}$$

which can be solved by integrating both terms so that the circuit response is

$$V_{out} = -\frac{1}{RC}\int V_{in}\,dt \tag{2.40}$$

This result shows that the output voltage varies as an integral of the input voltage with a scale factor of $-1/RC$. This circuit is employed in many cases where an integration of a transducer output is desired.

Other functions also can be implemented, such as a highly linear ramp voltage. If the input voltage is constant, $V_{in} = K$, and Equation (2.40) reduces to

$$V_{out} = -\frac{K}{RC}t \tag{2.41}$$

which is a linear ramp, a negative slope of K/RC. Some mechanism of reset through discharge of the capacitor must be provided because otherwise V_{out} will rise to the output saturation value and remain fixed there in time.

Example 2.16

Use an integrator to produce a linear ramp voltage rising at 10 volts per ms.

Solution An integrator circuit, as shown in Figure 2.26, produces a ramp of

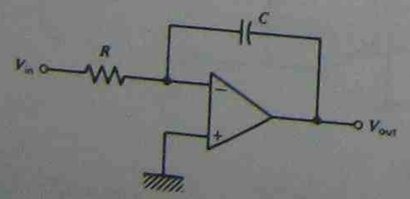


Figure 2.26 Integrator circuit.

$$V_{out} = -\frac{V_{in}}{RC}t \tag{2.41}$$

when the input voltage is constant. If we make $RC = 1$ ms and $V_{in} = -10$ V, then we have

$$V_{out} = (10 \cdot 10^{+3})t$$

which is a ramp rising at 10 volts/ms. A choice of $R = 1$ kΩ and $C = 1$ μF will provide the required RC product.

2.5.8 Linearization

The op amp represents a very effective device to implement linearization. Generally, this is achieved by placing a *nonlinear* element in the feedback loop of the op amp, as shown in Figure 2.27. The summation of currents provides

$$\frac{V_{in}}{R} + F(V_{out}) = 0 \tag{2.42}$$

where

V_{in} = input voltage
R = input resistance
$F(V_{out})$ = nonlinear variation of current with voltage

If Equation (2.42) is solved (in principle) for V_{out}, we get

$$V_{out} = G\left(\frac{V_{in}}{R}\right) \tag{2.43}$$

where

V_{out} = output voltage
$G\left(\frac{V_{in}}{R}\right)$ = a nonlinear function of the input voltage [actually the inverse function of $F(V_{out})$].

Thus, as an example, if a diode is placed in the feedback as shown in Figure 2.28,

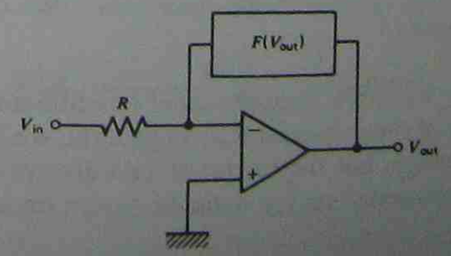


Figure 2.27 A nonlinear amplifier is constructed by placing any nonlinear element in the feedback of the op amp.

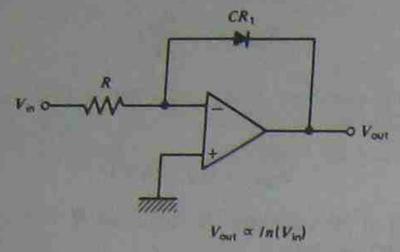


Figure 2.28 When a diode is placed in the feedback leg of an op amp, a nonlinear amplifier is formed whose output is proportional to the natural logarithm of the input.

the function $F(V_{out})$ is an exponential

$$F(V_{out}) = F_0 \exp(\alpha V_{out}) \tag{2.44}$$

where

F_0 = amplitude constant
α = exponential constant

The inverse of this is a logarithm, and thus Equation (2.43) becomes

$$V_{out} = \frac{1}{\alpha} \log_e(V_{in}) - \frac{1}{\alpha} \log_e(F_0 R) \tag{2.45}$$

which thus constitutes a (linear) logarithmic amplifier.

Different feedback devices can produce amplifiers that only smooth out nonlinear variations or provide specified operations such as the logarithmic amplifier.

2.5.9 Special Integrated Circuits (ICs)

A vast line of special integrated circuits (ICs) is available from many manufacturers and is useful to the process-control instrumentation designer. Such special-purpose devices include

1. High-gain differential instrumentation amplifiers
2. Current-to-voltage converters
3. Modulator/demodulators
4. Bridge and null detectors
5. Phase-sensitive detectors

In the following chapters, we often require signal conditioning that can be implemented through the use of these special ICs. In general, we indicate the details of a signal conditioning design, but the reader should always be aware that use of special-purpose ICs may render such a detailed design unnecessary.

2.6 INDUSTRIAL ELECTRONICS

The signal conditioning discussed thus far in this chapter has referred mainly to measurement signal modification. It is often necessary to perform a type of signal conditioning on the controller output to activate the final control element. For example, the 4–20 mA controller output may be required to adjust heat input to a large, heavy-duty oven for baking crackers. Such heat may be provided by a 2-kW electrical heater. Clearly, some sort of conditioning is required to allow such a high-power system to be controlled by a low-energy current signal. In this section we present two devices that are commonly used in process control to provide a mechanism where such energy conversion can occur. The intent here is not to give you all the information needed to construct practical circuits to use these devices, but to familiarize you with them and their specifications.

2.6.1 Silicon-Controlled Rectifier (SCR)

The SCR has become a very important part of high-power electrical signal conditioning and control. In some regards, it is a solid-state replacement for the relay, although there are some problems if that analogy is taken too far. The standard diode is, in the ideal sense, a device that will conduct current in only one direction. The SCR, again in the ideal sense, is like a diode that will not conduct in either direction until it is turned on or "fired." Figure 2.29 shows the schematic symbol of an SCR. Note the similarity to a diode but with the added terminal, called the *gate*. If the SCR is forward biased (that is, positive voltage on the anode with respect to the cathode), it will *not* be conducting. Now suppose a voltage is placed on the gate with respect to the cathode. There will be some positive value of this voltage—the trigger voltage—at which the SCR will start conducting and behave then like a normal diode. Even if the gate voltage is taken away, it will continue to conduct like a diode; that is, once turned on it will stay on, regardless of the gate. The only way to turn the SCR back "off" is to have the forward bias condition taken away. This means the voltage must drop below the forward voltage drop of the SCR so that the current drops below a minimum value, called the holding current, or the polarity from anode to cathode must actually reverse. The fact that the SCR cannot be turned off easily limits its use in dc applications to those cases when some method of reducing the forward current to below the holding values can be provided. In ac circuits, the SCR will automatically turn off in every half cycle when the ac voltage applied to the SCR reverses polarity.

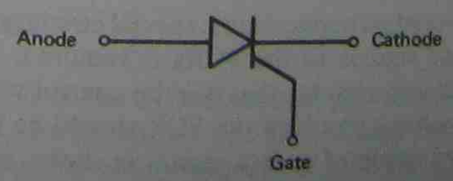


Figure 2.29 Symbol for an SCR.

Characteristics and specifications of SCRs are as follows:

1. *Maximum forward current* There is a maximum current that the SCR can carry in the forward direction without damage. This value varies from a few hundred milliamps to more than a thousand amps for large industrial types.
2. *Peak reverse voltage* Like a diode, there is a peak reverse bias voltage that can be applied to the SCR without damage. The value varies from a few volts to several thousand volts.
3. *Trigger voltage* The minimum gate voltage to drive the SCR into conduction varies between types and sizes from a few volts to 40 volts.
4. *Trigger current* There is a minimum current that the source of trigger voltage must be able to provide before the SCR can be fired. This varies from a few milliamps to several hundred milliamps.
5. *Holding current* This refers to the minimum anode to cathode current necessary to keep the SCR conducting in the forward conducting state. The value varies from 20 to 100 mA.

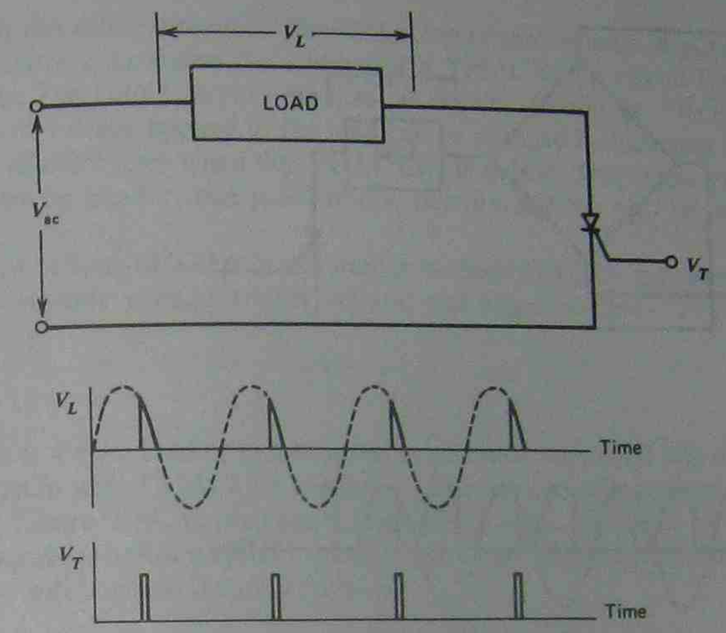
Ac operation

Figure 2.30 illustrates the operation of an SCR in varying the rms dc voltage in half-wave operation. The trigger voltage is developed by some circuit that produces a pulse at a certain selected phase of the applied ac signal. Thus, the SCR turns on in a repetitive fashion as shown. The SCR is turned back off, of course, in each half cycle when the ac polarity reverses. By changing the part of the positive half cycle when the trigger is applied, the effective (rms) value of dc voltage applied to the load can be increased. Of course, with this circuit the maximum possible rms dc voltage is that which would be developed by a half-wave rectifier. If more power is required, the SCR can be used with a full-wave bridge circuit. Figure 2.31 shows this type of circuit and the voltages versus time that result. The trigger voltage must now be generated in each half cycle and applied to the SCR trigger (gate) terminal. In a process-control application, the controller output signal would be used to drive a circuit that changed the time at which the pulses were applied to the gates and thus changed the power applied to the load. The voltage applied to the load is pulsating dc. This configuration could not be used with a load that required ac voltage for operation.

Trigger control

To use the SCR in process-control applications, special circuitry to convert control signals into suitable trigger signals to the SCRs is required. These circuits are usually composed of electronic systems that use the control voltage to determine the phase of the ac load voltage at which the SCR should be turned on.

A very elementary example of such a circuit is shown in Figure 2.32. The control signal voltage is used to provide base drive to a transistor via an LED



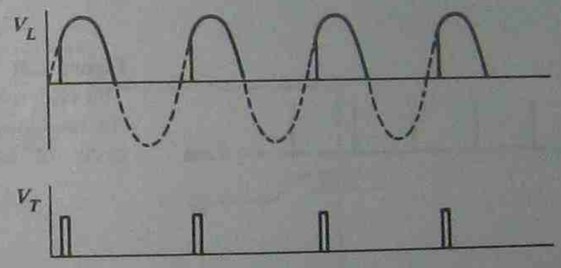


Figure 2.30 Half-wave SCR operation. Changing the time of V_T application changes the dc rms voltage applied to the load V_L.

that assures isolation of the control circuit from the power circuit. At low-base drive the capacitor is charged slowly and will not reach the SCR trigger voltage until late in the cycle (hence low load power).

A large control signal will provide high base drive, and the capacitor will charge much more quickly. Then the SCR will turn on much earlier in the cycle and more power will be delivered to the load.

2.6.2 TRIAC

An extension of the SCR discussed previously is a device that can be triggered to conduct in either direction. The TRIAC can be thought of as two SCRs connected in parallel and reversed, but with the gates connected. A positive trigger will cause it to conduct in one direction, and a negative trigger will cause it to

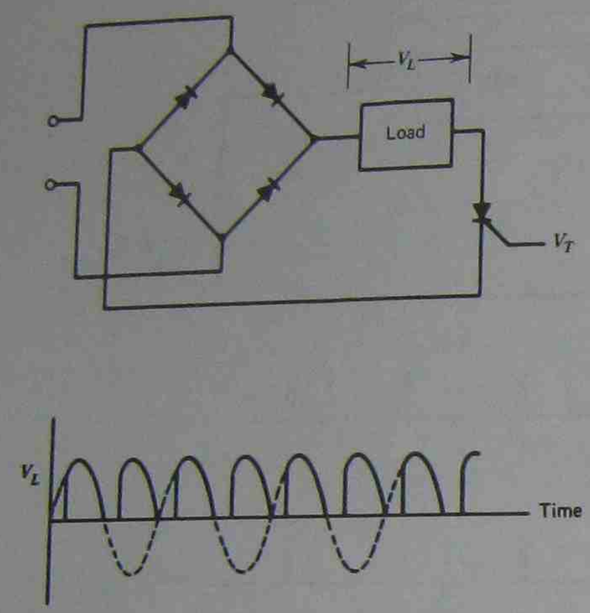


Figure 2.31 Full-wave SCR circuit. The effective rms dc voltage applied to the load is increased because both cycles of the ac are used.

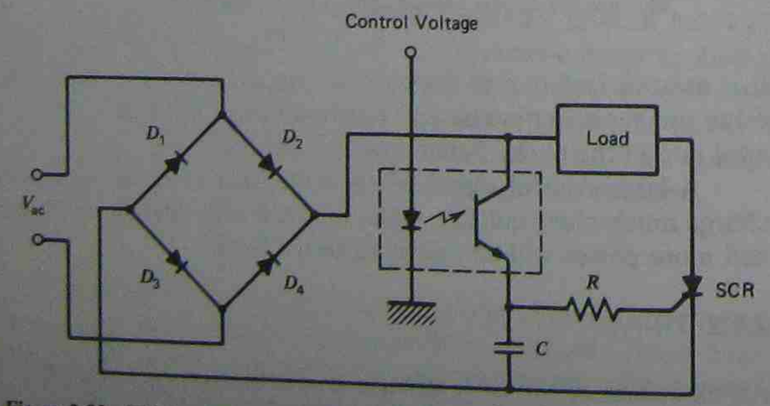


Figure 2.32 This is one example of how an SCR can be triggered from an isolated dc signal voltage.

conduct in the other direction. The TRIAC thus can be used in pure ac applications. Figure 2.33 shows the symbol of a TRIAC and a circuit for a typical application. The voltage across the load, as shown, remains ac. The effective ac rms value of voltage applied to the load can be changed by changing the time in the phase of the cycles when the TRIAC gate is pulsed. The trigger voltage generated must be bipolar, one pulse in one polarity and the next of the opposite polarity.

Specifications of TRIACs are similar to those of SCRs: maximum rms current, peak reverse voltage, trigger voltage, and trigger current.

DIAC

A DIAC is a special kind of two-terminal semiconductor switch that is often used in conjunction with TRIACs for triggering. This device, with a schematic symbol shown in Figure 2.34, is nonconducting (off) in either direction as long as the applied voltage is below a certain value. If that value is exceeded in either polarity, the device will begin to conduct (turn on).

Figure 2.33 The TRIAC can conduct in both directions so that the load voltage remains ac, but the rms value is determined by the time at which the trigger voltages are applied.

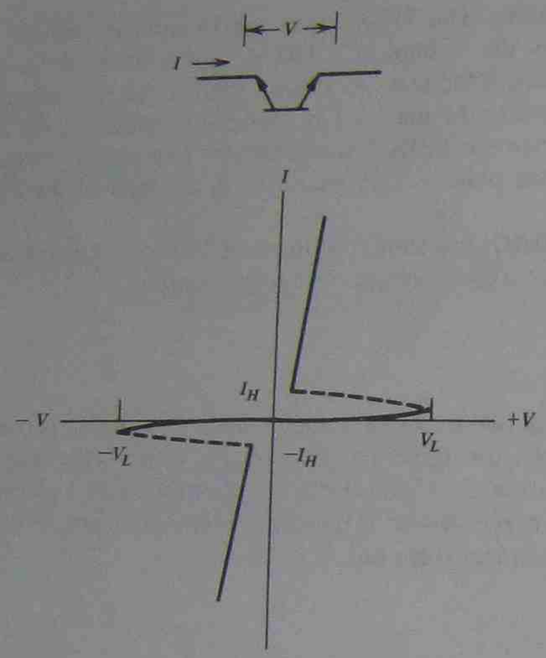


Figure 2.34 The DIAC goes from a nonconducting to conducting state if the voltage exceeds V_T in either polarity. It reverts to nonconducting if the current falls below I_H.

Trigger control

Similar to the SCR, for the TRIAC to be useful in control applications, it is necessary to link the control signal to the application of trigger signals. This involves adjusting the time (or phase) in a cycle of ac voltage when the TRIAC is triggered.

An elementary method of doing this is shown in Figure 2.35. Note the use of a DIAC between the capacitor and the TRIAC trigger terminal. The principle of operation is the same as the SCR system discussed previously, but the load is impressed with an ac voltage and the bridge rectifier is not needed. The capacitor

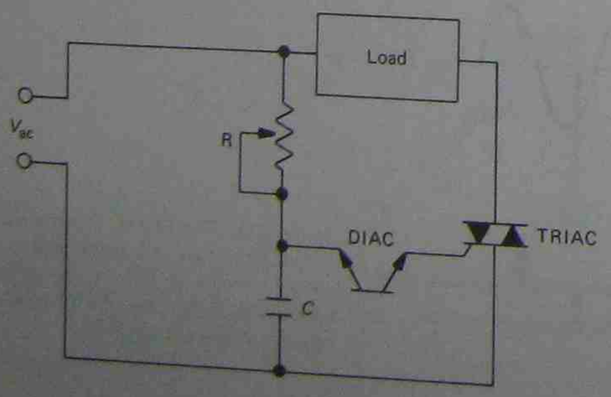


Figure 2.35 The TRIAC can be triggerd from the ac line voltage using the DIAC.

charges in either polarity until the DIAC turns on, which, in turn, triggers the TRIAC.

2.7 DESIGN GUIDELINES

This section discusses typical issues which should be considered when designing an analog signal conditioning system. The examples show how the guidelines can be used to develop a design. The guidelines assure that the problem is clearly understood and that the important issues are included.

Not every guideline will be important in every design, so some will be not applicable. In many cases, not enough information will be available to address an issue properly; then the designer must exercise good technical judgment in accounting for that part of the design.

Figure 2.36 shows the measurement and signal conditioning model. In some cases, the entire system is to be developed, from selecting the sensor to designing the signal conditioning. In other cases, only the signal conditioning will be developed. The guidelines are generalized. Since the sensor is selected from what is available, the actual design is really for the signal conditioning.

GUIDELINES FOR ANALOG SIGNAL CONDITIONING DESIGN

1. *Define the measurement objective.*
   - **a.** *Parameter:* What is the nature of the measured variable: pressure, temperature, flow, level, voltage, current, resistance, etc.?
   - **b.** *Range:* What is the range of the measurement: 100 to 200°C, 45 to 85 psi, 2 to 4 V, etc.?
   - **c.** *Accuracy:* What is the required accuracy: 5% FS, 3% of reading, etc.?
   - **d.** *Linearity:* Must the measurement output be linear?
   - **e.** *Noise:* What is the noise level and frequency spectrum of the measurement environment?

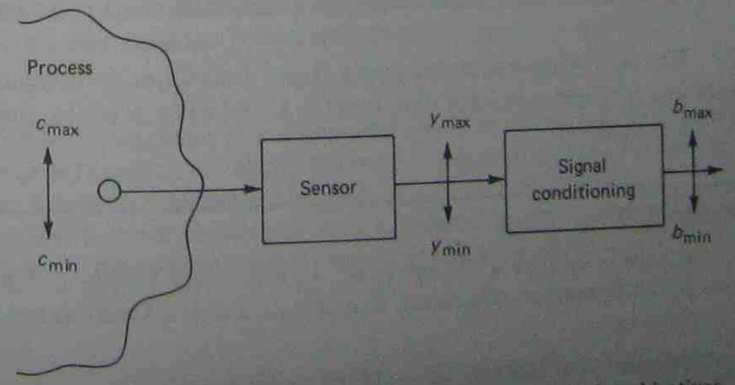


Figure 2.36 Model for measurement and signal conditioning objectives.

2. *Select a sensor (if applicable).*
   a. *Parameter:* What is the nature of the sensor output: resistance, voltage, etc.?
   b. *Transfer function:* What is the relationship between the sensor output and the measured variable: linear, graphical, equation, accuracy, etc.?
   c. *Time response:* What is the time response of the sensor: first-order time constant, second-order damping, and frequency?
   d. *Range:* What is the range of sensor parameter output for the given measurement range?
   e. *Power:* What is the power specification of the sensor: resistive dissipation maximum, current draw, etc.?
3. *Design the analog signal conditioning (S/C).*
   a. *Parameter:* What is the nature of the desired output? The most common is voltage, but current and frequency are sometimes specified. In the latter cases, conversion to voltage is still often a first step.
   b. *Range:* What is the desired range of the output parameter (e.g., 0 to 5 V, 4 to 20 mA, 5 to 10 kHz)?
   c. *Input impedance:* What input impedance should the S/C present to the input signal source? This is very important in preventing loading of a voltage signal input.
   d. *Output impedance:* What output impedance should the S/C offer to the output load circuit?
4. *Notes on analog signal conditioning design.*
   a. If the input is a resistance change and a bridge or divider must be used, be sure to consider the effect of output voltage nonlinearity with resistance *and* the effect of current through the resistive sensor.
   b. For the op amp portion of the design, the easiest design approach is to develop an equation for output versus input. From this equation, it will be clear what types of circuits may be used. This equation represents the static transfer function of the signal conditioning.
   c. Always consider any possible loading of voltage sources by the signal conditioning. Such loading is a direct error in the measurement system.

The following examples apply these guidelines to measurement signal conditioning problems. In later chapters (4, 5, and 6) on sensors, many other examples will be presented.

Example 2.17

A sensor outputs a voltage from −2.4 to −1.1 V. For interface to an analog-to-digital converter, this needs to be 0 to 2.5 volts. Develop the required signal conditioning.

Solution For this type of problem, no information is provided about the measured variable, the measurement environment, or the sensor. We are simply asked to provide a voltage-to-voltage conversion. Since the source impedance is not known, it is good design practice to assume it is high and design a high-input-impedance system to avoid loading. Most ADCs have input impedances of at least tens of kilohms, and the output impedance of op amp circuits is quite low, so there is no real concern for the output impedance of the S/C system.

For this type of problem, it is easiest to develop an equation for the output in terms of the input. From this, circuits can be envisioned.

$$V_{out} = mV_{in} + V_0$$

Using the specified information, we form two equations for the unknown slope (gain) m, and offset (bias) V_0.

$$-2.4 = 0m + V_0$$

$$-1.1 = 5m + V_0$$

Clearly, from the first equation we have $V_0 = -2.4$ V, and when this is substituted into the second equation, we get

$$-1.1 = 5m - 2.4$$

Then, solving for m,

$$m = (2.4 - 1.1)/5 = 0.26$$

The transfer function equation is thus

$$V_{out} = 0.26V_{in} - 2.4$$

There are many ways to satisfy this equation. A summing amplifier could be used, but it does not have high input impedance, so a voltage follower would be needed at the input. Also, the summing amplifier inverts, so an inverter would be required to get the correct sign. This circuit is shown in Figure 2.37. Note that the bias has been provided by a divider. A 15-volt supply has been assumed for the divider resistance calculations. The 100-Ω resistor was selected to keep loading by the op amp circuit small. A trimmer (variable) resistor has been used so both loading of the divider by the op amp circuit and variation of the supply from exactly 15 volts can be compensated for by adjusting until the bias is exactly 2.4 volts.

The design could also be accomplished by a differential amplifier. If the 0.26 in the transfer equation is factored, we get

$$V_{out} = 0.26(V_{in} - 9.23)$$

So this is the equation of a differential amplifier with a gain of 0.26 and one input fixed at 9.23 volts. A voltage follower would still be required on the input. (The reader should complete this design.)

Why is it not possible to use a noninverting amplifier? Since it has high input impedance, the voltage follower would not be necessary.

Example 2.18

Temperature is to be measured in the range of 250°C to 450°C with an accuracy of ±2°C. The sensor is a resistance which varies linearly from 280 Ω to 1060 Ω for this

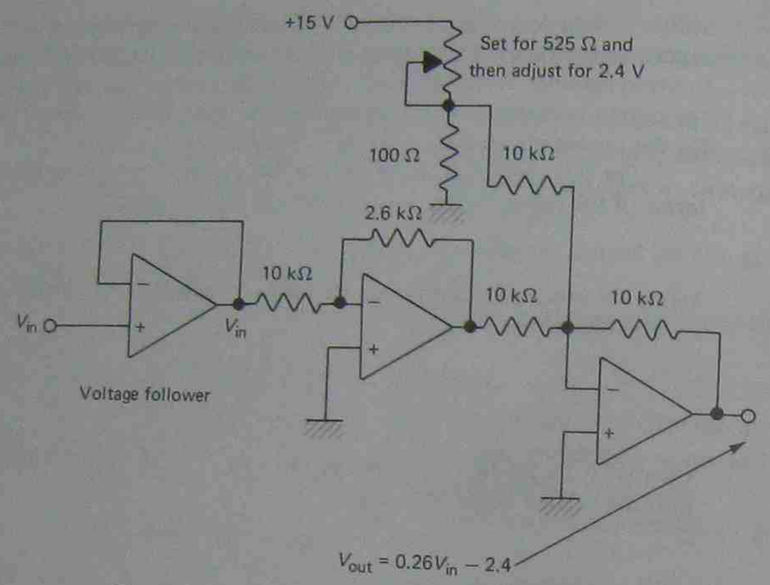


Figure 2.37 One possible solution to Example 2.17.

temperature range. Power dissipated in the sensor must be kept below 5 mW. Develop analog signal conditioning which provides a voltage varying linearly from −5 to +5 volts for this temperature range. The load is a high-impedance recorder.

Solution Following the guidelines, let us first identify all the elements of the problem.

MEASURED VARIABLE PARAMETER: TEMPERATURE
Range: 250 to 450°C
Accuracy: ±2°C
Noise: unspecified

SENSOR SIGNAL
Parameter: resistance
Transfer function: linear
Time response: unspecified
Range: 280 Ω to 1060 Ω, linear
Power: maximum 5 mW dissipated in sensor

SIGNAL CONDITIONING
Parameter: voltage, linear
Range: −5 to +5 volts
Input impedance: keep power in sensor below 5 mW
Output impedance: no problem, high-impedance recorder

The accuracy is ±0.8% at the low end and ±0.44% at the high end. Therefore, we will keep three significant figures to provide 0.1% on values selected.

The 5-mW maximum sensor dissipation means the current must be limited. To find the maximum current, we note that

$$P = I^2R$$
$$0.005 = I^2R$$
$$I = 0.005/R$$

The minimum current will thus occur at the maximum resistance,

$$I_{max} = 0.005/1060 = 2.17 \text{ mA}$$

Thus, the design must always keep the sensor current below 2 mA.

Since the system must be linear, we should set up a linear equation between the sensor resistance and the output voltage. Then it is a matter of determining what circuits will implement the equation.

$$V_{out} = mR_s + V_0$$

We solve for m and V_0 by using the given information.

$$-5 = 280m + V_0$$
$$+5 = 1060m + V_0$$

Subtracting the first equation from the second gives

$$10 = 780m \quad \text{or} \quad m = 0.0128$$

Then, using this in the first equation,

$$-5 = 280(0.0128) + V_0$$
$$V_0 = -8.58$$

So the transfer function equation is

$$V_{out} = 0.0128R_s - 8.58$$

This can be provided by an inverting amplifier with the sensor resistor in the feedback, followed by an inverting summer to get the signs correct. Figure 2.38 shows one possible solution. The fixed input voltage and input resistor of the first op amp have been selected to satisfy the 5-mW maximum power dissipation. This has been done by noting that the current through the sensor is just equal to the current through the input circuit. Thus, by using 1.00 kΩ and 1.00 volt, the current will always be 1 mA and thus less than 2 mA, as required.

As in Example 2.17, trimmers are used in dividers so the fixed voltages can be adjusted to 1.00 and 8.58 volts and thus account for supply voltage differences.

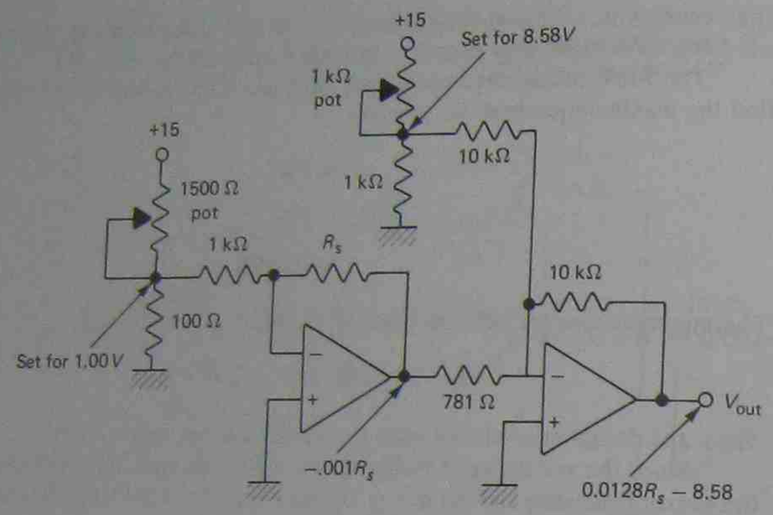


Figure 2.38 One possible solution to Example 2.18.

SUMMARY

The signal conditioning discussed in this chapter relates to the standard techniques employed for providing signal compatibility and measurement in analog systems. The reader was introduced to the basic concepts that form the foundation of such analog conditioning.

To present a complete picture of analog signal conditioning, the following points were considered:

1. The need for analog signal conditioning was reviewed and resolved into the requirements of signal-level changes, linearization, signal conversions, and filtering and impedance matching.
2. Bridge circuits are a common example of a conversion process where a changing resistance is measured either by a current or by a voltage signal. Many modifications of the bridge are used, including *electronic balancing* and techniques of *lead compensation*.
3. The high- and low-pass *RC* filters are passive circuits used to block undesired frequencies from data signals.
4. Operational amplifiers (op amps) are a very special signal conditioning building block around which many special function circuits can be developed. The device was demonstrated in applications involving amplifiers, converters, linearization circuits, integrators, and several other functions.
5. Silicon-controlled rectifiers (SCRs) and TRIACs are semiconductor devices, similar to diodes, that can control large-energy ac or dc signals using low-level imputs.

PROBLEMS

Section 2.3

2.1 A sensor resistance varies from 520 to 2500 Ω. This is used for R_1 in the divider of Figure 2.3, along with $R_2 = 500\ \Omega$ and $V_s = 10.0$ V. Find (a) the range of the divider voltage V_D and (b) the range of power dissipation by the sensor.

2.2 Prepare graphs of the divider voltage versus transducer resistance for Example 2.1 and Problem 2.1. Does the voltage vary linearly with resistance? Does the voltage increase or decrease with resistance?

2.3 A Wheatstone bridge, as shown in Figure 2.4, nulls with $R_1 = 227\ \Omega$, $R_2 = 448\ \Omega$, and $R_3 = 1414\ \Omega$. Find R_4.

2.4 A sensor with a nominal resistance of 50 Ω is used in a bridge with $R_1 = R_2 = 100\ \Omega$, $V = 10.0$ V, and $R_3 = 100\ \Omega$ potentiometer. It is necessary to resolve 0.1 Ω changes of the sensor resistance. (a) At what value of R_3 will the bridge null? (b) What voltage resolution must the null detector possess?

2.5 A bridge circuit is used with a sensor located 100 m away. The bridge is not lead compensated, and the cable to the sensor has a resistance of 0.45 Ω/ft. The bridge nulls with $R_1 = 3400\ \Omega$, $R_2 = 3445\ \Omega$, and $R_3 = 1560\ \Omega$. What is the sensor resistance?

2.6 The bridge of Figure 2.4 has $R_1 = 250\ \Omega$, $R_3 = 500\ \Omega$, $R_4 = 340\ \Omega$, and $V = 1.5$ V. The detector is a galvanometer with $R_G = 150\ \Omega$. (a) Find the value of R_2 that will null the bridge. (b) Find the offset current that will result if $R_2 = 190\ \Omega$.

2.7 A current balance bridge, shown in Figure 2.7, has resistances of $R_1 = R_2 = 1$ kΩ, $R_4 = 590\ \Omega$, $R_5 = 10\ \Omega$, and $V = 10.0$ V. (a) Find the value of R_3 that nulls the bridge with no current. (b) Find the value of R_3 that balances the bridge with a current of 0.25 mA.

2.8 A potential measurement bridge, such as in Figure 2.8, has $V = 10.0$ V, $R_1 = R_2 = R_3 = 10$ kΩ. Find the unknown potential if the bridge nulls with $R_4 = 9.73$ kΩ.

2.9 An ac Wheatstone bridge with all arms as capacitors nulls when $C_1 = 0.4\ \mu$F, $C_2 = 0.31\ \mu$F, and $C_3 = 0.27\ \mu$F. Find C_4.

2.10 The ac bridge of Figure 2.39 nulls with $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, $R_3 = 100\ \Omega$, and

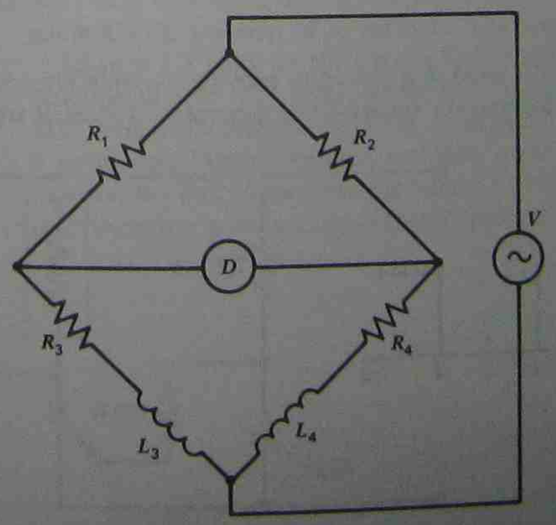


Figure 2.39 Bridge for Problem 2.10.

CHAPTER 3

DIGITAL SIGNAL CONDITIONING

INSTRUCTIONAL OBJECTIVES

In this chapter, the basic principles of digital signal processing will be considered with particular emphasis on digital-to-analog (D/A) and analog-to-digital (A/D) conversion techniques and data acquisition systems. After you have read this chapter, you should be able to

1. **Develop a Boolean equation for a simple process-control alarm problem.**
2. **Implement a process-control design of an alarm by digital circuits and comparators.**
3. **Define the representation of fractional binary and decimal numbers.**
4. **Diagram a basic DAC and describe its operation.**
5. **Diagram a successive approximation ADC and describe its operation.**
6. **Define the conversion resolution of ADCs and DACs.**
7. **Design a data acquisition system.**

3.1 INTRODUCTION

Perhaps the best way to start this chapter is to consider briefly why we are interested in *digital* signal conditioning. An overall survey of electronics applications in industry shows that conversions to digital techniques are occurring rapidly. There are many reasons for this conversion, but two in particular are important. One is the reduction in *uncertainty* when dealing with digitally encoded information compared to analog information. We did not say *accuracy*, we said

uncertainty. If a system presents analog information, great care must be taken to account for electrical noise influence, drift of amplifier gains, loading effects, and a host of other problems familiar to the analog electronics designer. In a digitally encoded signal, however, a wire carries either a high or low level and is not particularly susceptible to the problems associated with analog processing. Thus, there is an inherent certainty in representing information by digital encoding because of the *isolation* of digital representation from spurious influences. The *accuracy* of this signal in representing the information is discussed later in this chapter (Section 3.3).

A second reason for conversion to digital electronics is the growing desire to use digital computers in the industrial process. The digital computer by nature requires information encoded in digital format before it can be used. The question of the need for digital signal conditioning becomes a question of why computers are so widely used in industry. As discussed in Chapter 11, a few reasons are (1) the ease with which a computer controls a multivariable process-control system, (2) through computer programming, nonlinearities in a sensor output can be linearized, (3) complicated control equations can be solved to determine required control functions, and (4) the ability to microminiaturize rather complex digital processing circuits as integrated circuits (ICs). Finally, the development of microprocessors has brought about quite a transformation of process control to digitally based control systems. With microprocessor-based computers, implementation of computer-based control systems has become practical, and with it, the need for knowledge of digital signal conditioning. This technology not only reduces physical size but both power consumption and failure rate.

With the growing use of computers in process-control technology, it is now clear that any individual trained to work in this field also must be versed in the technology of digital electronics. The basic question is how far such preparation should extend into this related complex field of study. The answer is that a process-control technologist must understand the elements and characteristics of process-control loops. In this context, digital electronics is used as a tool to implement necessary features of process control and therefore should be understood to the extent of knowing how such devices affect the characteristics of the loop. Consider that one does not need to know detailed physics of stretched wires to understand the application of strain gages and to use these devices successfully in process control. Similarly, one does not need to know the internal design of logic gates and microcomputers to use such devices in process control. In this light, the objectives of this chapter have been carefully chosen to provide the reader with sufficient background in digital technology to understand its application to process control.

3.2 REVIEW OF DIGITAL FUNDAMENTALS

A working understanding of the application of digital techniques to process control requires a foundation of basic digital electronics. The design and implementation of control logic systems and microcomputer control systems require a depth of

understanding that can only be obtained after several courses devoted to the subject. In this text, we assume a sufficient background so the reader can appreciate the essential features of digital electronic design and its application to process control. A summary of basic digital electronics concepts is presented in Appendix 2.

3.2.1 Digital Information

The use of digital techniques in process control requires that process variable measurements and control information be encoded into a digital form. Digital signals themselves are simply two-state (binary) levels of voltage on a wire, as discussed in Section 1.5.2. We speak, then, of the digital information as a high state (H or **1**) or a low state (L or **0**) on a wire that carries the digital signal.

Digital word

Given the simple binary information that is carried by a digital signal, it is clear that a more complicated arrangement must be used to describe analog information. Generally, this is done by using an assemblage of digital levels to construct a *word*. The individual digital levels are referred to as *bits* of the word. Thus, for example, a 6-bit word consists of six independent digital levels as **101011**, which can be thought of as a six-digit base 2 number. An important consideration, then, is how the process-control information is encoded into this digital word.

Decimal whole numbers

One of the most common schemes for encoding analog data into a digital word is to use the straight counting of decimal (or base 10) and binary representations. The principles of this are reviewed in Appendix 2, together with octal and hexadecimal representations.

Example 3.1

Find the base 10 equivalent of the binary whole number **00100111**.

Solution As in the base 10 system, zeros preceding the first significant digit do not contribute. Thus, the binary number is actually **100111** and so $n = 5$. To find the decimal equivalent, we use Appendix 2 and

$$N_{10} = a_5 2^5 + a_4 2^4 + \cdots a_1 2^1 + a_0 2^0$$

$$N_{10} = (1)2^5 + (0)2^4 + (0)2^3 + (1)2^2 + (1)2^1 + (1)2^0 \qquad \text{(A.2.1)}$$

$$N_{10} = 32 + 4 + 2 + 1$$

$$N_{10} = 39$$

Example 3.2

Find the binary equivalent of the base 10 number 47.

Solution Starting the successive division, we get

$$\frac{47}{2} = 23 \text{ with a remainder of } \frac{1}{2} \text{ so that } a_0 = 1$$

then

$$\frac{23}{2} = 11 \text{ with a remainder of } \frac{1}{2} \text{ so that } a_1 = 1$$

then

$$\frac{11}{2} = 5 + \frac{1}{2} \therefore a_2 = 1$$

$$\frac{5}{2} = 2 + \frac{1}{2} \therefore a_3 = 1$$

$$\frac{2}{2} = 1 + 0 \therefore a_4 = 0$$

$$\frac{1}{2} = 0 + \frac{1}{2} \therefore a_5 = 1$$

We find that base 10 number 47 becomes a binary number $\mathbf{101111}_2$.

The representation of negative numbers in binary format takes on several forms, as discussed in Appendix 2.

Octal and hex numbers

It is quite cumbersome for humans to work with digital words expressed as numbers in the binary representation. For this reason, it has become common to use either the octal (base 8) or hexadecimal (base 16, called hex) representations, which are reviewed in Appendix 2. Octal numbers are conveniently formed from groupings of three binary digits; that is, $\mathbf{000}_2$ is 0_8 and $\mathbf{111}_2$ is 7_8. Thus, a binary number like $\mathbf{101011}_2$ is equivalent to 53_8. Hex numbers are formed easily from groupings of four binary digits; that is, $\mathbf{0000}_2$ is 0H and $\mathbf{1111}_2$ is FH. The capital H is used to designate a hex number instead of a subscript of 16. Also recall that the hex counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F to cover the possible states. Because microcomputers must frequently use either 4-bit, 8-bit, or 16-bit words, the hex notation is very commonly used with these machines. In hex, a binary number like $\mathbf{10110110}_2$ would be written B6H.

3.2.2 Fractional Binary Numbers

Although not as commonly used, it is possible to define a fractional binary number in the same manner as whole numbers using only the **1** and **0** of this counting system. Such numbers, just as in the decimal framework, represent divisions of the counting system to values less than unity. A correlation can be made to decimal

numbers in a similar fashion to Equation (A.2.1), as

$$N_{10} = b_1 2^{-1} + b_2 2^{-2} + \cdots b_m 2^{-m} \tag{3.1}$$

where

N_{10} = base 10 number less than one
$b_1 b_2 \cdots b_{m-1} b_m$ = base 2 number less than one
m = number of digits in base 2 number

Example 3.3

Find the base 10 equivalent of the binary number $\mathbf{0.11010_2}$.

Solution This can be found most easily by using

$$N_{10} = b_1 2^{-1} + b_2 2^{-2} + \cdots b_m 2^{-m} \tag{3.1}$$

with

$$m = 5$$

$$N_{10} = (1)2^{-1} + (1)2^{-2} + (0)2^{-3} + (1)2^{-4} + (0)2^{-5}$$

$$N_{10} = \frac{1}{2} + \frac{1}{4} + \frac{1}{16}$$

$$N_{10} = 0.8125_{10}$$

Conversion of a base 10 number that is less than 1 to a binary equivalent employs a procedure where repeated multiplication by 2 is performed. The result of each multiplication will be a fractional part and either a 0 or 1 whole number part, which determines whether that digit is a **0** or **1**. The first multiplication gives the most significant bit b_1, and the last gives either a 0 or 1 for the least significant bit b_m.

Example 3.4

Find the binary, octal, and hex equivalent of 0.3125_{10}.

Solution Using successive multiplication, we find

$$2(0.3125) = 0.6250 \quad \text{so} \quad b_1 = 0$$
$$2(0.625) = 1.250 \quad \text{so} \quad b_2 = 1$$
$$2(0.25) = 0.5 \quad \text{so} \quad b_3 = 0$$
$$2(0.5) = 1.0 \quad \text{so} \quad b_4 = 1$$

Thus, we find that 0.3125_{10} is equivalent to $\mathbf{0.0101_2}$. It can be represented as $\mathbf{0.010100_2}$ because trailing zeros are not significant in a number less than one and thus as 0.24 octal, because $\mathbf{010_2} = 2_8$ and $\mathbf{100_2} = 4_8$. Similarly, this is 0.50H.

3.2.3 Boolean Algebra

In process control, as well as in many other technical disciplines, action is taken on the basis of an evaluation of observations made in the environment. In driving an automobile, for example, we are constantly observing such external factors as traffic, lights, speed limits, pedestrians, street conditions, low-flying aircraft, and such internal factors as how fast we wish to go, where we are going, and many others. We evaluate these factors and take actions predicated on the evaluations. We may see that the light is green, streets good, speed low, no pedestrians or aircraft, we are late, and thus conclude that an action of pressing on the accelerator is required. Then we may observe a parked police radar unit with all other factors the same, negate the aforementioned conclusion, and apply the brake. Many of these parameters can be represented by a *true* or *not true* observation and, in fact, with enough definition, all the observations could be reduced to simple *true* or *false* conditions. When we learn to drive, we are actually setting up internal response to a set of such true/false observations in the environment. In the industrial world, an analogous condition exists relative to the external and internal influences on a manufacturing process, and when we control a process we are in effect teaching a control system response to a set of true/false observations. This teaching may consist of designing electronic circuits that can *logically* evaluate the set of true/false conditions and initiate some appropriate action. To design such an electronic system, we must first be able to mathematically express the inputs, the logical evaluation, and the corresponding outputs. *Boolean algebra* is a mathematical procedure that allows the combinations of true/false conditions in various logical operations so that conclusions can be drawn. For purposes of this text, we do not require expertise in Boolean technique, but an operational familiarity with it that can be applied to a process-control environment.

Before a particular problem in industry can be implemented using digital electronics, it must be analyzed in terms that are amenable to the binary nature of digital techniques. Generally, this is accomplished by stating the problem in the form of a set of true/false-type conditions that must be applied to derive some desired result. These sets of conditions then are stated in the form of one or more Boolean equations. We will see in the next section that a Boolean equation is in a form that is readily implemented with existing digital circuits. The mathematical approach of Boolean algebra allows us to write an analytical expression to represent these stipulations. The fundamentals of Boolean algebra are summarized in Appendix 2.

Let us consider a simple example of how a Boolean equation may result from a practical problem. Consider a mixing tank for which there are three variables of interest: liquid level, pressure, and temperature. The problem is that we must signal an alarm when certain combinations of conditions occur between these variables. Referring to Figure 3.1, we denote level by A, pressure by B, and temperature by C, and assume that setpoint values have been assigned for each variable so that the Boolean variables are either **1** or **0** as the physical quantities are above or below the setpoint values. The alarm will be triggered when the

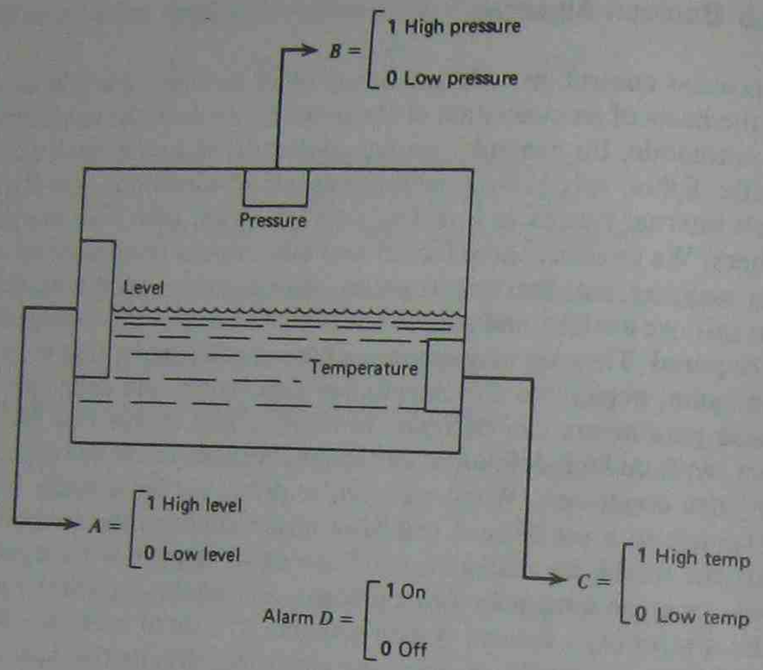


Figure 3.1 System for the application example of Section 3.2.3.

Boolean variable D goes to the logic true state. The alarm conditions are

1. Low level with high pressure
2. High level with high temperature
3. High level with low temperature and high pressure

We now define a Boolean expression with AND operations that will give a $D = 1$ for each condition

1. $D = \overline{A} \cdot B$ will give $D = 1$ for condition (1).
2. $D = A \cdot C$ will give $D = 1$ for condition (2).
3. $D = A \cdot \overline{C} \cdot B$ will give $D = 1$ for condition (3).

The final logic equation results by combining all three conditions so that if any are true, the alarm will sound ($D = 1$). This is accomplished with the OR operation

$$D = \overline{A} \cdot B + A \cdot C + A \cdot \overline{C} \cdot B \tag{3.2}$$

This equation would now form the starting point for a design of electronic digital circuitry that would perform the indicated operations.

3.2.4 Digital Electronics

The electronic building blocks of digital electronics are designed to operate on the binary levels present on digital signal lines. These building blocks are based on families of types of electronic circuits, as discussed in Appendix 2, that have their specific stipulations of power supplies and voltage levels of the **1** and **0** states. The basic structure involves the use of AND/OR logic and NAND/NOR logic to implement Boolean equations.

Example 3.5

Develop a digital circuit using AND/OR gates that implements the equation developed in Section 3.2.3.

Solution The problem posed in Section 3.2.3 (with Figure 3.1) has a Boolean equation solution of

$$D = \overline{A} \cdot B + A \cdot C + A \cdot \overline{C} \cdot B \tag{3.2}$$

The implementation of this equation using AND/OR gates is shown in Figure 3.2. The AND, OR, and inverter are used in a straightforward implementation of the equation.

Example 3.6

Repeat Example 3.5 using NAND/NOR gates.

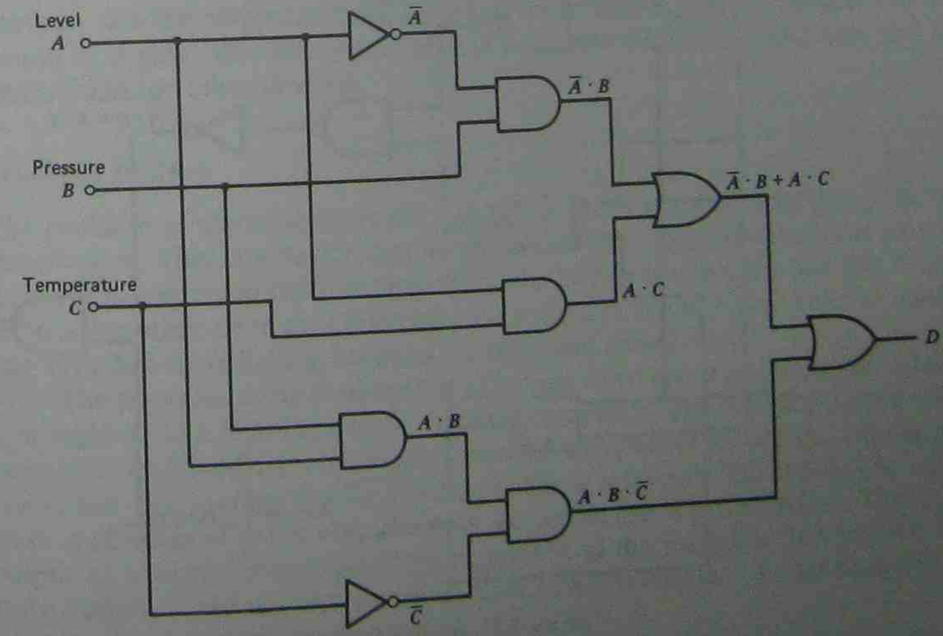


Figure 3.2 Solution for Example 3.5.

Solution One way to implement the equation in NAND/NOR would be to provide inverters after every gate to, in effect, convert the devices back to AND/OR gates. In this case, the circuit developed would look like Figure 3.2 but with an inverter after every gate. A second approach is to use the Boolean theorems to *reformulate* the equation for better implementation using NAND/NOR logic. For example, if we are to get the desired equation for D as output from a NAND gate, then the inputs must have been

$$\overline{\overline{A} \cdot B + A \cdot C}$$

and

$$\overline{A \cdot B \cdot \overline{C}}$$

because NAND between these produces

$$\overline{\overline{(\overline{A} \cdot B + A \cdot C)} \cdot \overline{(A \cdot B \cdot \overline{C})}}$$

that, by DeMorgan's theorem, becomes

$$\overline{A} \cdot B + A \cdot C + A \cdot B \cdot \overline{C}$$

that is, the desired output. Working backward from this result allows the circuit to be realized, as shown in Figure 3.3. Many other correct configurations are possible.

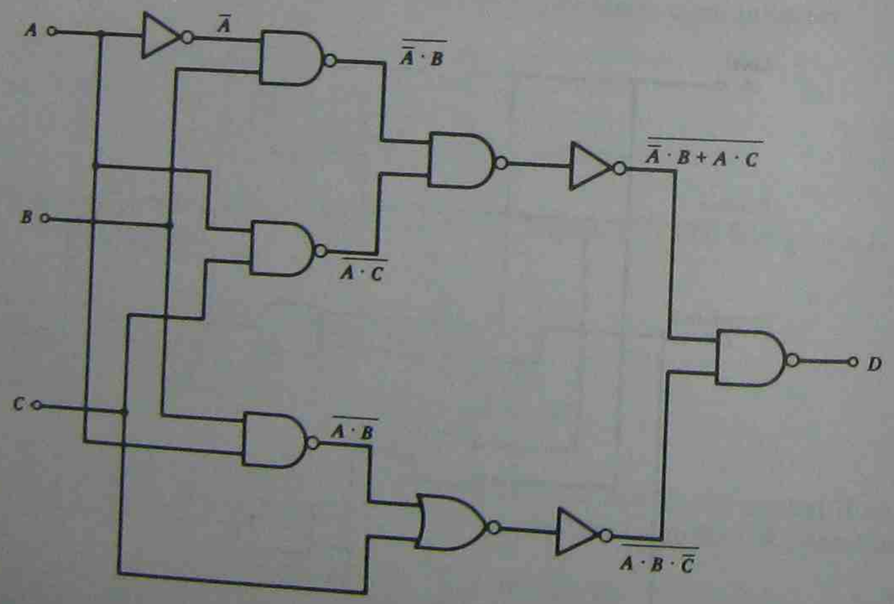


Figure 3.3 Solution for Example 3.6.

3.2.5 Programmable Logic Controllers

The move toward digital logic techniques and computers in industrial control paralleled the development of special controllers called *programmable logic controllers* (PLCs) or simply *programmable controllers* (PCs). These devices are particularly suited to the solution of control problems associated with Boolean equations and binary logic problems in general. They are a computer-based outgrowth of relay sequence controllers. Detailed treatment of this type of control system is given in Chapter 8.

3.2.6 Busses and Tri-State Buffers

Two concepts that deserve special comment are important features of microprocessor-based computers in control applications. These concepts are the use of common busses for data input and output, and the use of tri-state buffers for connections to these busses.

Bus

A data bus is a parallel arrangement of lines connected to a computer, where each line is dedicated to one bit of the data word. Thus, an 8-bit computer may have a data bus with eight lines in parallel. All data input and output to the computer are carried over these lines. Clearly, an important issue is that the data bus lines be free for use by many different devices, including memory, input devices, output devices, and the computer itself. If one of these lines is simply connected to the output of a gate, that line would always represent the state of that gate and be unavailable for other devices.

Tri-state buffers

The problem of allowing many devices to use the bus is solved by using the tri-state buffer. This is a device that acts like a switch. When the switch is closed, its input is placed on the bus line. When the switch is open, the bus line is free for use by other devices. Of course, the switch is actually electronic in nature and very fast in switching between the open and closed state.

The tri-state buffer is described as having three states *on its output*: a logic 1, a logic 0, or a high-impedance state (open circuit). The high-impedance state lasts until an ENABLE command is issued from some other source, usually the computer. The symbol for the tri-state buffer is shown in Figure 3.4. The input state is *not* passed to the output unless the enable line is driven active. Thus, the output of several devices could be connected to the same bus line through tri-state buffers. Only the one whose tri-state buffer is enabled (if any) would have its state impressed on the bus line.

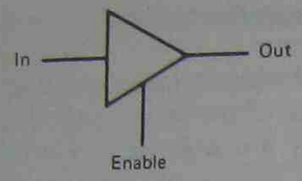


Figure 3.4 Diagram symbol for the tri-state buffer with an active HIGH enable. Active LOW would have the invert symbol on the enable line.

3.3 CONVERTERS

The most important digital tool for the process-control technologist is one that translates digital information to analog and vice versa. Most measurements of process variables are performed by devices that translate information about the variable to an analog electrical signal. To interface this signal with a computer or digital logic circuit, it is necessary first to perform an analog-to-digital (A/D) conversion. The specifics of this conversion must be well known so that a unique, known relationship exists between the analog and digital signals. Often, the reverse situation occurs where a digital signal is required to drive an analog device. In this case, a digital-to-analog (D/A) converter is required.

3.3.1 Comparators

The most elementary form of communication between the analog and digital is a device (usually an IC) called a *comparator*. This device, which is shown schematically in Figure 3.5, simply compares two analog voltages on its input terminals. Depending on which voltage is larger, the output will be a **1** (high) or **0** (low) digital signal. The comparator is extensively used for alarm signals to computers or digital processing systems. This element also is an integral part of the analog-to-digital and digital-to-analog converter, to be discussed in Section 3.3.2.

A comparator can be constructed from an op amp provided the output is properly clamped to provide the required levels for the logic states (as +5 and 0 for transistor–transistor logic [TTL] **1** and **0**). Commercial comparators are designed to have the necessary logic levels on the output.

One of the voltages on the comparator inputs, V_a or V_b in Figure 3.5, will be the variable input and the other a fixed value called a trip, trigger, or reference voltage. The reference value is computed from the specifications of the problem and then applied to the appropriate comparator input terminal, as illustrated in Example 3.7. The reference voltage is provided from a divider from available power supplies.

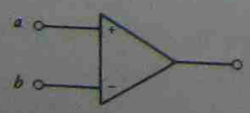


Figure 3.5 A comparator changes output logic state as a function of the analog input voltages.

Example 3.7

A process-control system specifies that temperature should never exceed 160°C if the pressure also exceeds 10 Pa. Design an alarm system to detect this condition, using temperature and pressure transducers with transfer functions of 2.2 mV/°C and 0.2 V/Pa, respectively.

Solution The alarm conditions will be a temperature signal of (2.2 mV/°C)(160°C) = 0.352 V coincident with a pressure signal of (0.2 V/Pa)(10 Pa) = 2 volts. The circuit of Figure 3.6 shows how this alarm can be implemented with comparators and one AND gate. The reference voltages could be provided from dividers.

Hysteresis comparator

When using comparators, there is often a problem if the signal voltage has noise or approaches the reference value very slowly. The comparator output may "jiggle" back and forth between high and low as the reference level is reached. This effect is shown in Figure 3.7. Such fluctuation of output may cause problems with the equipment designed to interpret the comparator output signal.

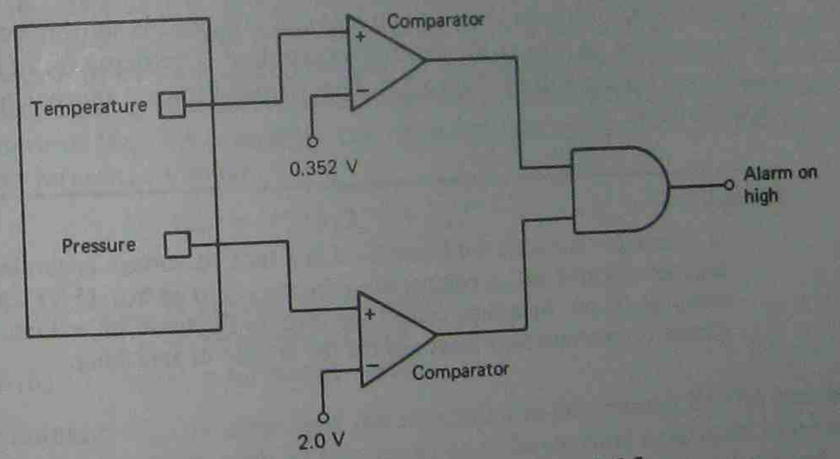


Figure 3.6 Diagram of circuit for Example 3.7.

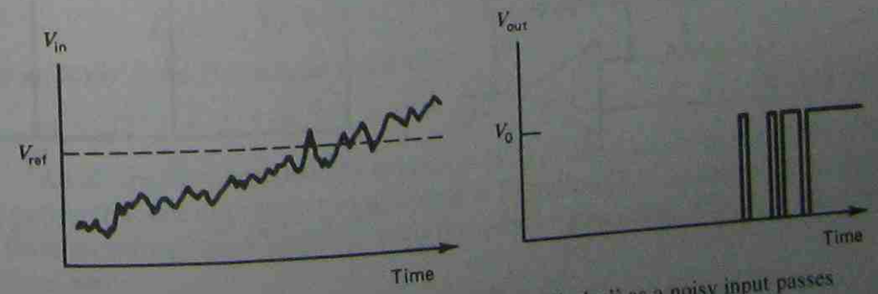


Figure 3.7 Notice how the comparator output "jiggles" as a noisy input passes through the reference voltage value.

This problem often can be solved by providing a *deadband* or *hysteresis* to the reference level about which output changes occur. Once the comparator has been triggered high, the reference level is automatically reduced so that the signal must fall to some value below the old reference before the comparator goes to the low state.

There are many ways this hysteresis can be provided, but Figure 3.8 shows one very common technique. Feedback resistor R_f is provided between the output and one of the inputs of the comparator, and that input is separated from the signal by another resistor R. Under the *condition* that $R_f \gg R$, the response of the comparator is shown in Figure 3.8.

The condition for which the output will go high (V_0) is defined by the condition

$$V_{in} \geq V_{ref} \tag{3.3}$$

Once having been driven high, the condition for the output to drop back to the low ($0V$) state is given by the relation

$$V_{in} \leq V_{ref} - (R/R_f)V_0 \tag{3.4}$$

The deadband or hysteresis is given by $(R/R_f)V_0$ and is thus selectable by choice of the resistors, as long as this relation is satisfied. The response of this comparator is shown by the graph of Figure 3.8. The arrows indicate increasing or decreasing input voltage.

Example 3.8

A transducer converts the liquid level in a tank to voltage according to the transfer function (20 mV/cm). A comparator is supposed to go high (5 V) whenever the level becomes 50 cm. Splashing causes the level to fluctuate by ±3 cm. Develop a hysteresis comparator to protect against the effects of splashing.

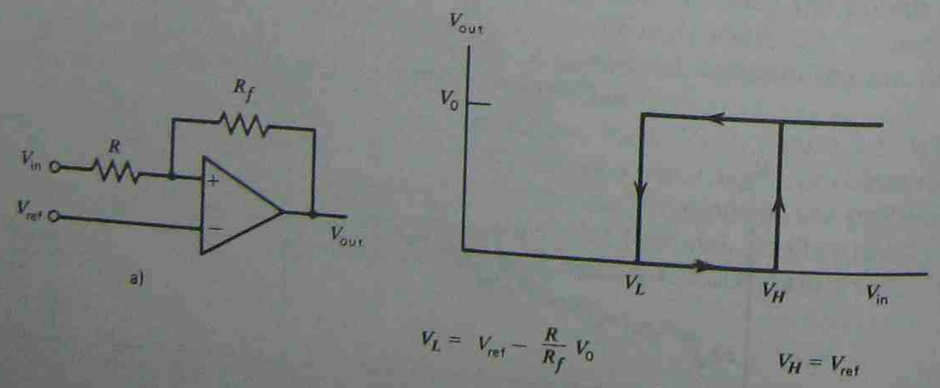


Figure 3.8 The hysteresis comparator has a window within which output changes do not occur.

Solution The nominal reference for the comparator occurs at 50 cm, which is V_{ref} = (20 mV/cm)(50 cm) = 1 volt. The splashing, however, causes a "noise" of (20 mV/cm)(±3 cm) = ±60 mV. This is a total range of 120 mV. We need a deadband of at least 120 mV, but let us make it 150 mV for security. Thus, we have

$$(R/R_f)(5\text{ V}) = 150\text{ mV}$$

$$(R/R_f) = 0.03$$

If we make $R_f = 100\text{ k}\Omega$, then $R = 3\text{ k}\Omega$. Thus, use of these resistors, as shown in Figure 3.8, with a reference of 1 volt will meet the requirement.

3.3.2 Digital-to-Analog Converters (DACs)

A DAC accepts digital information and transforms it into an analog voltage. The digital information is in the form of a binary number with some fixed number of digits. Especially when used in connection with a computer, this binary number is called a binary *word* or *computer* word. The *digits* are called *bits* of the word. Thus, an 8-bit word would be a binary number having eight digits, such as $\mathbf{10110110_2}$. The D/A converter converts a digital word into an analog voltage by scaling the analog output to be zero when all bits are zero and some maximum value when all bits are one. This can be mathematically represented by treating the binary number that the word represents as a *fractional* number. In this context, the output of the D/A converter can be defined using Equation (3.1) as a *scaling* of some reference voltage.

$$V_{out} = V_R[b_1 2^{-1} + b_2 2^{-2} + \cdots b_n 2^{-n}] \tag{3.5}$$

where

V_{out} = analog voltage output
V_R = reference voltage
$b_1 b_2 \cdots b_n$ = n-bit binary word

The minimum V_{out} is zero, and the maximum is determined by the size of the binary word because, with all bits set to one, the decimal equivalent *approaches* V_R as the number of bits increases. Thus, a 4-bit word has a maximum of

$$V_{max} = V_R[2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}] = 0.9375V_R$$

and an 8-bit word has a maximum of

$$V_{max} = V_R[2^{-1} + 2^{-2} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-6} + 2^{-7} + 2^{-8}] = 0.9961V_R$$

An alternative equation to Equation (3.5) is often easier to use. This is based on noting that the expression in brackets in Equation (3.5) is really just the fraction of total counting states possible with the n-bits being used. With this recognition, we can write

$$V_{out} = \frac{N}{2^n} V_R \tag{3.6}$$

where

N = base 10 equivalent of DAC input

Suppose an 8-bit converter with a 5.0-volt reference has an input of $\mathbf{10100111_2}$, or A7H. If this input is converted to base 10, we get $N = 167_{10}$ and $2^8 = 256$. From Equation (3.6), the output of the ADC will be

$$V_{out} = \frac{167}{256} 5.0 = 3.2617 \text{ volts}$$

Example 3.9

What is the output voltage of a 10-bit ADC with a 10.0-volt reference if the input is (a) $\mathbf{0010110101_2}$ = 0B5H, (b) 20FH? What input is needed to get a 6.5-volt output?

Solution Let's use Equation (3.5) for the part (a) and Equation (3.6) for the part (b). Thus, for the 0B5H input we have

$$V_{out} = 10.0[2^{-3} + 2^{-5} + 2^{-6} + 2^{-8} + 2^{-10}]$$

$$= 10.0[0.1767578]$$

$$= 1.767578 \text{ volts}$$

For the (b) case we have 20FH = 527_{10} and $2^{10} = 1024$, so

$$V_{out} = (527/1024)\ 10.0$$

$$= (.514648)\ 10.0$$

$$= 5.14648 \text{ volts}$$

We can use Equation (3.6) to determine what input is needed to get a 6.5-volt output by solving for N,

$$N = 2^n(V_{out}/V_R)$$

$$N = 1024(6.5/10)$$

$$N = 665.6$$

The fact that there is a fractional remainder tells us that we cannot get *exactly* 6.5 volts from the converter. The best we can do is get an output for $N = 665 = 299$H or 666 = 29AH. The outputs for these two inputs are 6.494 V and 6.504 V, respectively. The only way to get exactly 6.5 volts of output would be to change the value of the reference slightly.

Conversion resolution

The conversion resolution is also a function of the *number* of bits in the word. The *more* bits, the smaller change in analog output for a 1-bit change in binary

word and hence the *greater* the resolution. The smallest possible change is simply given by

$$\Delta V_{out} = V_R 2^{-n} \tag{3.7}$$

where

ΔV_{out} = smallest output change
V_R = reference voltage
n = number of bits in the word

Thus, a 5-bit word D/A converter with a 10-volt reference will provide changes of $\Delta V_{out} = (10)(2^{-5}) = 0.3125$ volts per bit.

Example 3.10

Determine how many bits a D/A converter must have to provide output increments of 0.04 volts or less. The reference is 10 volts.

Solution One way to find the solution is to continually try word sizes until the resolution falls below 0.04 volts per bit. A more analytical procedure is to use Equation (3.7).

$$\Delta V = 0.04 = (10)(2^{-y})$$

Any n larger than the integer part of the exponent of two in this equation will satisfy the requirement. Taking logarithms

$$\log(0.04) = \log[(10)(2^{-y})]$$

$$\log(0.04) = \log(10) - y \log 2$$

$$y = \frac{\log(10) - \log(0.04)}{\log 2}$$

$$y = 7.966$$

Thus, an $n = 8$ will be satisfactory. This can be proved by Equation (3.7).

$$\Delta V_{out} = (10)(2^{-8})$$

$$\Delta V_{out} = \mathbf{0.0390625} \text{ volts}$$

DAC characteristics

For modern applications, most DACs are integrated circuit (IC) assemblies, viewed as a black box having certain input and output characteristics. In Figure 3.9, we see the essential elements of the DAC in terms of required input and output. The associated characteristics can be summarized by reference to this figure.

1. *Digital input* Typically, a parallel binary word of a number of bits spec-

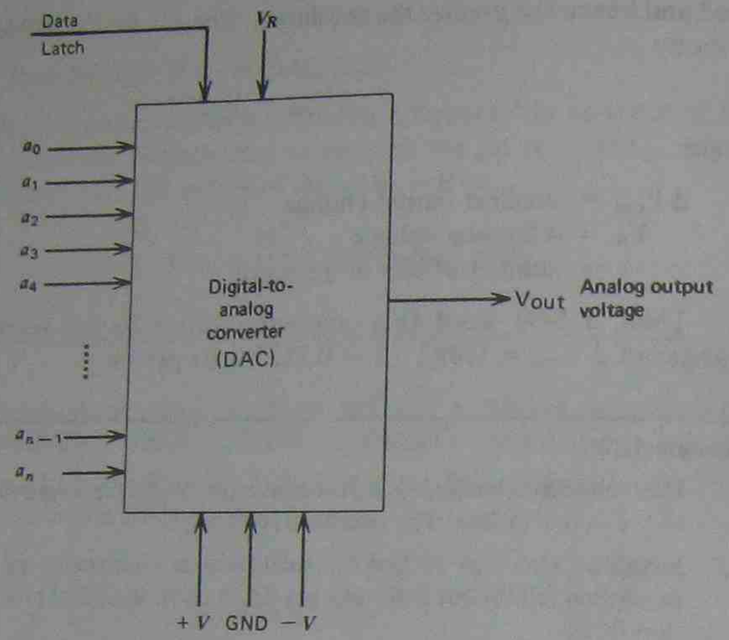


Figure 3.9 Diagram showing typical inputs and outputs for an n-bit digital-to-analog converter (DAC).

ified by the device specification sheet. Typically, TTL logic levels are required unless otherwise noted.

2. *Power supply* This is bipolar at a level of ±12 to ±18 V as required for internal amplifiers. Some DACs operate from a single supply.

3. *Reference supply* Required to establish the range of output voltages and resolution of the converter. This must be a stable, low-ripple source. In some units, an internal reference is provided.

4. *Output* A voltage representing the digital input. This voltage changes in steps as the digital input changes by bits with the step determined by Equation (3.7). The actual output may be bipolar if the converter is designed to interpret negative digital inputs.

5. *Offset* Because the DAC is usually implemented with op amps, there may be the typical output offset voltage with a zero input (see Section 2.4.2). Typically, connections will be provided to facilitate a zeroing of the DAC output with a zero word input.

6. *Data latch* Many DACs have a data latch built into their inputs. When a logic command is given to latch data, whatever data are on the input bus will be latched into the DAC and the analog output will be updated for that input data. The output will stay at that value until new digital data are latched into the input. In this way the input of the DAC can be connected directly onto the data bus of a computer, but it will only be updated when a latch command is given by the computer.

DAC structure

Generally speaking, a DAC is used as a black box, and no knowledge of the internal workings is required. There is some value, however, to briefly show how such conversion can be implemented. The simplest conversion uses a series of op amps for input for which the gains have been selected to provide an output as given by Equation (3.5). The most common variety, however, uses a *resistive ladder network* to provide the transfer function. This is shown in Figure 3.10 for the case of a 4-bit converter. With the R-$2R$ choice of resistors, it can be shown through network analysis that the output voltage is given by Equations (3.5) or (3.6). The switches are analog electronic switches.

Example 3.11

A control valve has a linear variation of opening as the input voltage varies from 0–10 volts. A microcomputer outputs an 8-bit word to control valve opening using an 8-bit DAC to generate the valve voltage. (a) Find the reference voltage required to

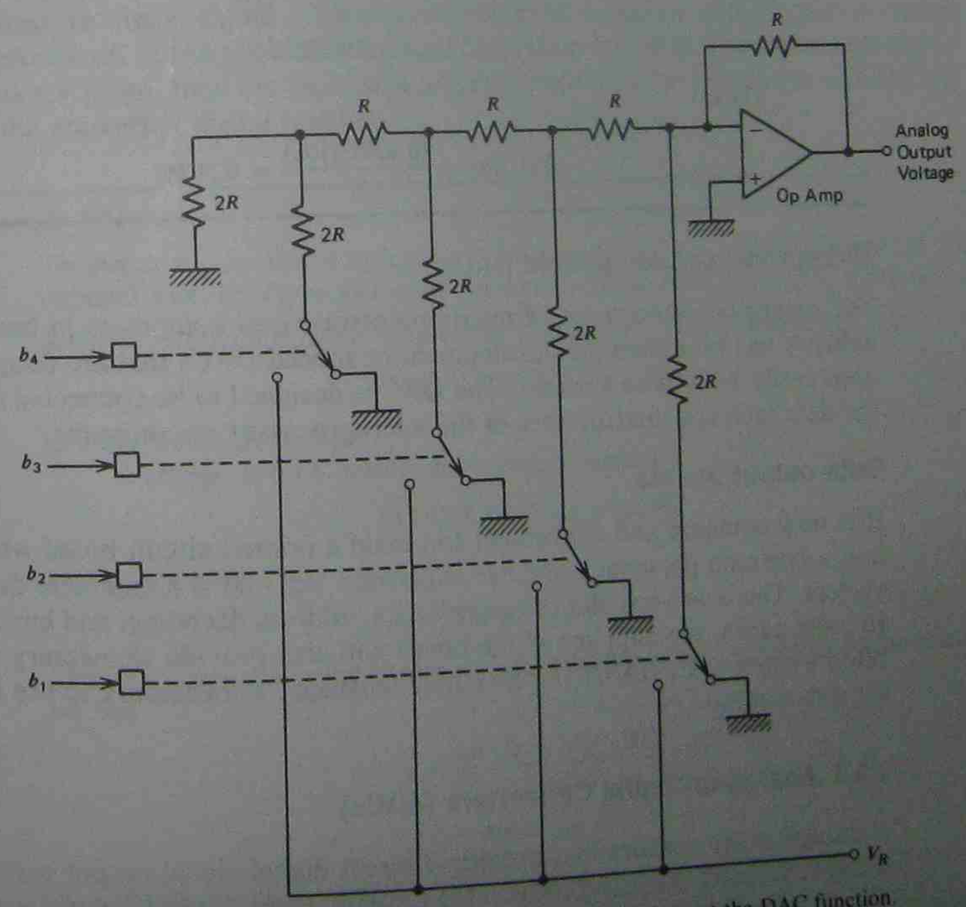


Figure 3.10 The ladder network is often used to implement the DAC function.

obtain a full open valve (10 volts): (b) find the percentage of valve opening for a 1-bit change in the input word.

Solution

(a) The full open valve condition occurs with a 10-volt input. If a 10-volt reference is used, a full digital word **11111111** will not quite give 10 volts, so we use a larger reference. Thus, we have

$$V_{out} = V_R(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_8 2^{-8})$$

$$10 = V_R\left(\frac{1}{2} + \frac{1}{4} + \cdots + \frac{1}{256}\right) \tag{3.5}$$

$$V_R = \frac{10}{0.9961} = 10.039 \text{ V}$$

(b) The percentage of valve change per step is found first from

$$\Delta V_{out} = V_R 2^{-8}$$

$$\Delta V_{out} = (10.039)\frac{1}{256} \tag{3.7}$$

$$\Delta V_{out} = 0.0392 \text{ V}$$

Thus,

$$\text{Percent} = \frac{(0.0392)(100)}{10} = \mathbf{0.392\%}$$

Microprocessor compatible DACs

The extensive deployment of microprocessor-based computers in business and industry has prompted the development of special DACs that are designed to be used easily with these systems. The DAC is designed to be connected directly to the data bus, and control lines of the microprocessor or computer.

Data output boards

It is now common and convenient to obtain a printed circuit board which plugs into a common personal computer expansion slot and is a complete data output system. The board has all necessary DACs, address decoding, and bus interface. In most cases, the supplier of the board will also provide elementary software, often written in C, BASIC, or assembly language, as necessary to use the board for data output.

3.3.3 Analog-to-Digital Converters (ADCs)

Although many sensors that provide a direct digital signal output exist and are being developed, most still convert the measured variable into an analog electrical signal. With the growing use of digital logic and computers in process control, it

is necessary to employ an ADC to provide a digitally encoded signal for the computer. The transfer function of the ADC can be expressed in the same manner as Equation (3.5) in that some analog voltage is provided as input, and the converter finds a binary number that, when substituted into Equation (3.5), gives the analog input. Thus,

$$V_{in} \simeq V_R[b_1 2^{-1} + b_2 2^{-2} + \cdots + b_n 2^{-n}] \tag{3.8}$$

where

V_{in} = analog voltage input
V_R = reference voltage
$b_1 b_2 \cdots b_n$ = n-bit digital outputs

We use an *approximate equality* in this equation because the voltage on the right can change by only a finite step size given by Equation (3.7),

$$\Delta V = V_R 2^{-n} \tag{3.7}$$

Therefore there is an inherent uncertainty of ΔV in any conversion of analog voltage to digital signal. This uncertainty must be taken into account in design applications. If the problem under consideration specifies a certain resolution in analog voltage, then the word size and reference must be selected to provide this in the converted digital number.

Example 3.12

Temperature is measured by a sensor with an output of 0.02 volts/°C. Determine the required ADC reference and word size to measure 0–100°C with 0.1°C resolution.

Solution At the maximum temperature of 100°C, the voltage output is

$$(0.02 \text{ V/°C})(100°\text{C}) = 2 \text{ V}$$

so a 2-V reference is used.

A change of 0.1°C results in a voltage change of

$$(0.1°\text{C})(0.02 \text{ V/°C}) = 2 \text{ mV}$$

so we need a word size where

$$0.002 \text{ V} = (2)(2^{-y})$$

Choose a size n that is the integer part of y plus one. Thus, solving with logarithms, we find

$$y = \frac{\log(2) - \log(0.002)}{\log 2}$$

$$y = 9.996 \simeq 10$$

so a **10**-bit word is required for this resolution. A 10-bit word has a resolution of

$$V = (2)(2^{-10})$$

$$V = 0.00195 \text{ volts}$$

which is better than the minimum required resolution of 2 mV.

Example 3.13

Find the digital word that results from a 3.127-volt input to a 5-bit ADC with a 5-volt reference.

Solution The relationship between input and output is

$$V_{in} \simeq V_R[a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + a_4 2^{-4} + a_5 2^{-5}] \tag{3.8}$$

Thus, we are to encode a fractional number of V_{in}/V_R or

$$a_1 2^{-1} + a_2 2^{-2} \cdots + a_5 2^{-5} = \frac{3.127}{5} = 0.6254$$

Using the method of successive multiplication defined in Section 3.2.2, we find

$$0.6254\ (2) = 1.2508 \therefore a_1 = 1$$

$$0.2508\ (2) = 0.5016 \therefore a_4 = 0$$

$$0.5016\ (2) = 1.0032 \therefore a_3 = 1$$

$$0.0032\ (2) = 0.0064 \therefore a_4 = 0$$

$$0.0064\ (2) = 0.0128 \therefore a_5 = 0$$

so that the output is $\mathbf{10100_2}$.

It is possible to write Equation (3.8) in a simpler fashion by using the fraction of counting states, as was done for the DAC. In this case, we can write an expression for the actual output N expressed as a base-10 integer.

$$\text{INT}(N) = \frac{V_{in}}{V_R} 2^n \tag{3.9}$$

where

$\text{INT}(N)$ = the integer part of N

The integer part of N is then converted to hex and/or binary to determine the actual output of the ADC. In the previous example, we would have

$$\text{INT}(N) = (3.127/5.0)2^5$$

$$= \text{INT}(20.0128) = 20_{10}$$

or an output of $14\text{H} = \mathbf{10100_2}$ as already found.

Example 3.14

The input to a 10-bit ADC with a 2.500-volt reference is 1.45 volts. What is the hex output? Suppose the output was found to be 1B4H. What is the voltage input?

Solution We will use Equation (3.9) to find the solution to these questions. For the first part, we can form the expression

$$\text{INT}(N) = (1.45/2.5)2^{10}$$

$$= 593.92$$

$$= 593$$

$$= 251\text{H}$$

So the output of the ADC is 251H for a 1.45-volt input. To get the voltage input for a 1B4H output, we solve Equation (3.9) for the voltage

$$V_{in} = (\text{INT}(N)/2^n)V_R$$

A conversion yields $1\text{B4H} = 436_{10}$,

$$V_{in} = (436/1024)2.50$$

$$= 1.06445 \text{ volts}$$

However, it is important to realize that any voltage from this to $1.06445 + 2.5/1024 = 1.06689$ will give an output of 1B4H. So the correct answer to the question is that the input voltage lies in the range 1.06445 to 1.06689 volts.

Bipolar operation

A bipolar ADC is one which accepts bipolar input voltage for conversion into an appropriate digital output. The most common bipolar ADCs provide an output which is called *offset binary*. This simply means that the normal output is shifted by half the scale so that all zeros corresponds to the negative maximum input voltage instead of 0. In equation form, the relation would be written from Equation (3.9) as

$$\text{INT}(N) = \frac{1}{V_R}[V_{in} + V_R/2]2^n \tag{3.10}$$

From this equation, you can see that if $V_{in} = -V_R/2$, then the output is zero, $\text{INT}(N) = 0$. If $V_{in} = 0$, then the output would be half of 2^n. The output will be the maximum count when the input is $V_R/2 - V_R 2^n$. For example, for 8 bits with a 10.0-volt reference, the step size is $\Delta V_{in} = (10)2^8 \approx 0.039$ volts. Looking at the possible states, we would have

$$V_{in} = -5.000 \quad N = \mathbf{00000000_2}$$

$$V_{in} = -4.961 \quad N = \mathbf{00000001_2}$$

etc.

$$V_{in} = -0.039 \quad N = \mathbf{01111111_2}$$

$$V_{in} = 0.000 \quad N = \mathbf{10000000_2}$$

$$V_{in} = +0.039 \qquad N = \mathbf{10000001_2}$$

etc.

$$V_{in} = +4.961 \qquad N = \mathbf{11111111_2}$$

There is an asymmetry to the result so that the converter cannot represent the full range from minus to plus $V_R/2$.

Example 3.15

What is the hex and binary output of a bipolar 12-bit ADC with a 5.00-volt reference for inputs of -0.85 volts and $+1.5$ volts? What input voltage would cause an output of 72H?

Solution Using Equation (3.10), we get

$$\begin{aligned} \text{INT}(N) &= (1/5.00)[-0.85 + 2.50]2^8 \\ &= (1.65/5)256 = 84.48 \\ &= 84_{10} \\ &= 54\text{H} = \mathbf{01010100_2} \end{aligned}$$

and

$$\begin{aligned} \text{INT}(N) &= (1/5.00)[1.5 + 2.50]256 \\ &= (4/5)256 = 204.8 \\ &= 204_{10} \\ &= \text{CCH} = \mathbf{11001100_2} \end{aligned}$$

To get an output of 72H, we solve Equation (3.10) for V_{in}

$$\begin{aligned} V_{in} &= (\text{INT}(N)/2^n)V_R - V_R/2 \\ &= (114/256)5.00 - 2.50 \\ &= -0.2734 \text{ V} \end{aligned}$$

But of course the actual answer is any voltage between -0.2734 volts and $(-0.2734 + 5/256) = -0.2539$ volts.

A/D structure

Most ADCs are available in the form of integrated circuit (IC) assemblies that can be used as a black box in applications. To fully appreciate the characteristics of these devices, however, it is valuable to examine the standard techniques employed to perform the conversions. There are two methods in use that represent very different approaches to the conversion problem.

Parallel-feedback ADC

The parallel-feedback A/D converter employs a feedback system to perform the conversion, as shown in Figure 3.11. Essentially, a *comparator* is used to compare the input voltage V_x to a feedback voltage V_F that comes from a DAC as shown. The comparator output signal drives a logic network that steps the digital output (and hence DAC input) until the comparator indicates the two signals are the *same* within the resolution of the converter. The most popular parallel-feedback converter is the *successive approximation* device. The logic circuitry is such that it successively sets and tests each bit, starting with the most significant bit of the word. We start with all bits zero. Thus, the first operation will be to set $b_1 = \mathbf{1}$ and test $V_F = V_R 2^{-1}$ against V_x through the comparator.

If V_x is greater, then b_1 will be **1**; b_2 is set to **1** and a test is made of V_x versus $V_V = V_R(2^{-1} + 2^{-2})$, and so on.

If V_x is less than $V_R 2^{-1}$, then b_1 is reset to zero; b_2 is set to **1**, and a test is made for V_x versus $V_R 2^{-2}$. This process is repeated to the least significant bit of the word. The operation can be illustrated best through an example.

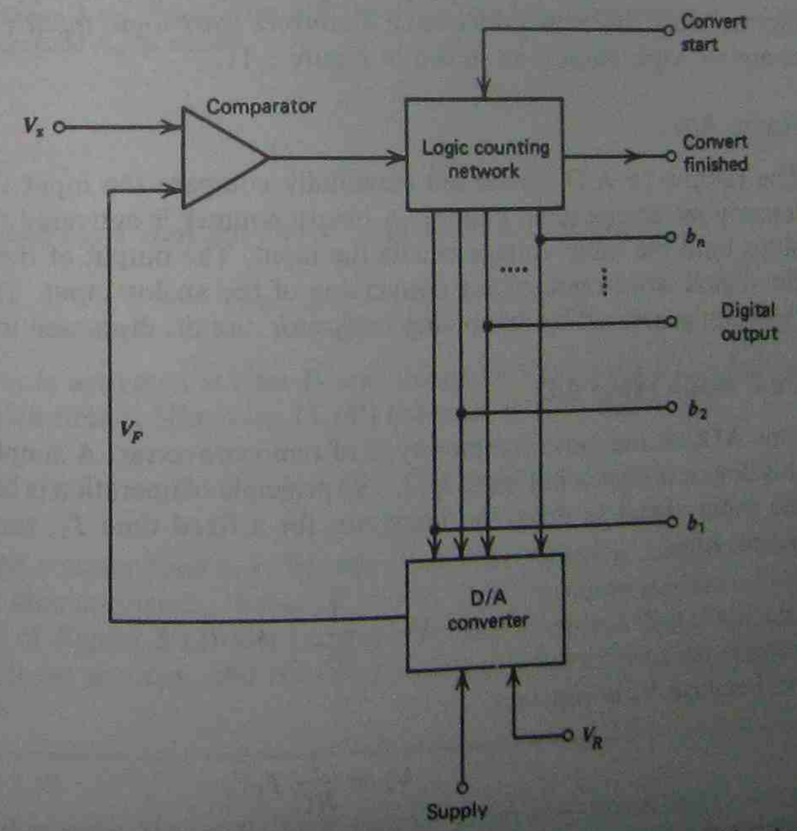


Figure 3.11 The successive approximation ADC is very common and involves the use of an internal DAC.

Example 3.16

Find the successive approximation ADC output for a 4-bit converter to a 3.217-volt input if the reference is 5 volts.

Solution Following the procedure outlined, we have the following operations: Let $V_x = 3.217$, then

(1) Set $b_1 = 1$	$V_F = 5(2^{-1}) = 2.5$ volts
$V_x > 2.5$	leave $b_1 = 1$
(2) Set $b_2 = 1$	$V_F = 2.5 + 5(2^{-2}) = 3.75$
$V_x < 3.75$	reset $b_2 = 0$
(3) Set $b_3 = 1$	$V_F = 2.5 + 5(2^{-3}) = 3.125$
$V_x > 3.125$	leave $b_3 = 1$
(4) Set $b_4 = 1$	$V_F = 3.125 + 5(2^{-4})$
$V_x < 3.4375$	reset $b_4 = 0$

By this procedure, we find the output is a binary word of $\mathbf{1010}_2$.

In addition to the analog input, digital output, power supply, and reference inputs, most A/D converters have a *convert start logic input* and a *conversion complete logic output*, as shown in Figure 3.11.

Ramp A/D

The ramp-type A/D converters essentially compare the input voltage against a linearly increasing ramp voltage. A binary counter is activated that counts ramp steps until the ramp voltage equals the input. The output of the counter is then the digital word representing conversion of the analog input. The ramp itself is typically generated by an op amp integrator circuit, discussed in Section 2.5.8.

Dual slope ramp A/D

This ADC is the most common type of ramp converter. A simplified diagram of this device is shown in Figure 3.12. The principle of operation is based on allowing the input signal to drive the integrator for a fixed time T_1, thus generating an output of

$$V_1 = \frac{1}{RC}\int V_x\,dt \tag{3.11}$$

or, because V_x is constant,

$$V_1 = \frac{1}{RC}T_1V_x \tag{3.12}$$

After time T_1, the input of the integrator is electronically switched to the reference supply. The comparator then sees an input voltage that decreases from V_1 as

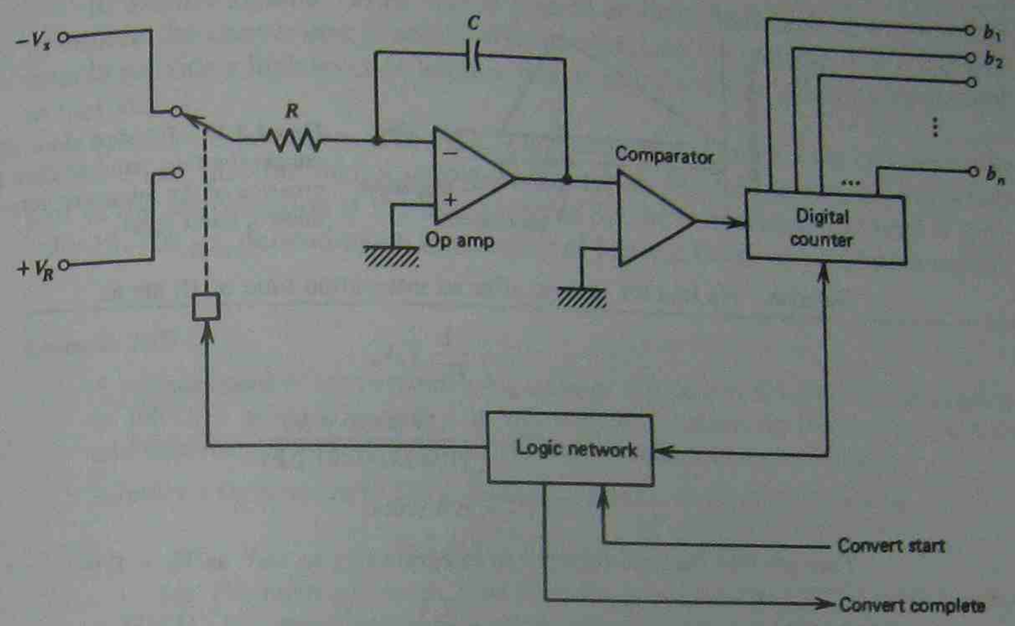


Figure 3.12 A dual slope ADC uses an op amp integrator, comparator, and associated digital circuits.

$$V_2 = V_1 - \frac{1}{RC}\int V_R\,dt \tag{3.13}$$

or, because V_R is constant and V_1 is given from Equation (3.12),

$$V_2 = \frac{1}{RC}T_1V_x - \frac{1}{RC}tV_R \tag{3.14}$$

A counter is activated at time T_1 and counts until the comparator indicates $V_2 = 0$, at which time t_x [Equation (3.14)] indicates that V_x will be

$$V_x = \frac{t_x}{T_1}V_R \tag{3.15}$$

Thus, the counter time t_x is linearly related to V_x and is independent of the integrator characteristics, that is, R and C. This procedure is shown in the timing diagram of Figure 3.13. Conversion *start* and *complete* digital signals are also used in these devices, and (in many cases) internal or external references may be used.

Example 3.17

A dual slope ADC as shown in Figure 3.12 has $R = 100$ kΩ and $C = 0.01$ μF. The reference is 10 volts, and the fixed integration time is 10 ms. Find the conversion time for a 6.8-volt input.

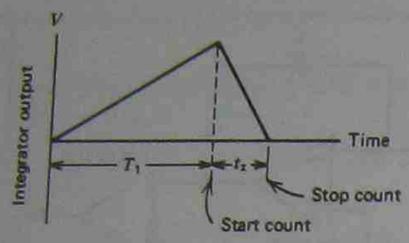


Figure 3.13 The dual slope ADC counts the time required for a zero crossing of the integrator output from a known, fixed input.

Solution We find the voltage after an integration time of 10 ms as

$$V_1 = \frac{1}{RC} T_1 V_x$$

$$V_1 = \frac{(10 \text{ ms})(6.8 \text{ V})}{(100 \text{ k}\Omega)(0.01 \ \mu\text{F})} \tag{3.12}$$

$$V_1 = 6.8 \text{ volts}$$

Then we find the time required to integrate this to zero as $V_2 = 0$ in

$$V_2 = \frac{T_1 V_x}{RC} - \frac{t_x}{RC} V_R \tag{3.14}$$

thus,

$$t_x = \frac{T_1 V_x}{V_R}$$

$$t_x = \frac{(10 \text{ ms})(6.8 \text{ V})}{10 \text{ V}}$$

$$t_x = 6.8 \text{ ms}$$

The total conversion time is then 10 ms + 6.8 ms = **16.8 ms.**

General characteristics

Numerous general features may be indicated for successive approximation A/D converters, important in applications:

1. *Input* Generally an analog voltage level. The most common levels are 0–10 and 0–5 volts or −10 to +10 if bipolar conversion is possible. In some cases, the level is determined by an externally supplied reference.

2. *Output* A parallel or serial binary word that is an encoding of the analog input.

3. *Reference* A stable, low ripple source against which the conversion is performed.

4. *Power supplies* Generally, a bipolar ±12- to ±18-V supply is required for the analog amplifiers and comparators and a +5-V supply for the digital circuitry.

5. *Digital signals* Most ADCs require an input logic high on a given line to initiate the conversion process. When conversion is complete, the ADC will usually provide a high level on another line as an indicator to following equipment of that status.

6. *Conversion time* The ADC must sequence through a set of operations before it can find the digital output as described. For this reason, an important part of the specification is the time required for the conversion. The time is typically 10–100 μs, depending on the number of bits and the design of the converter.

Example 3.18

A measurement of temperature using a sensor that outputs 6.5 mV/°C must measure to 100°C. A 6-bit ADC with a 10-volt reference is used. (a) Develop a circuit to interface the sensor and the ADC; (b) find the temperature resolution.

Solution To measure to 100°C means the sensor output at 100°C will be

$$(6.5 \text{ mV/°C})(100°\text{C}) = 0.65 \text{ volts}$$

(a) The interface circuit must provide a gain so that at 100°C the ADC output is **111111**. The input voltage that will provide this output is found from

$$V_x = V_R(a_1 2^{-1} + a_2 2^{-2} + \cdots + a_6 2^{-6})$$

$$V_x = 10\left(\frac{1}{2} + \frac{1}{4} + \cdots + \frac{1}{64}\right)$$

$$V_x = \mathbf{9.84375 \text{ V}}$$

Thus, the required gain must provide this voltage when the temperature is 100°C.

$$\text{Gain} = \frac{9.84375}{0.65}$$

$$= \mathbf{15.14}$$

The op amp circuit of Figure 3.14 will provide this gain.

(b) The temperature resolution can be found by working backward from the least significant bit (LSB) voltage change of the ADC.

$$\Delta V = V_R 2^{-n} \tag{3.7}$$

$$\Delta V = (10)(2^{-6}) = 0.15625 \text{ V}$$

Working back through the amplifier, this corresponds to a sensor change of

$$\Delta V_T = \frac{0.15625}{15.14} = 0.01032 \text{ V}$$

or a temperature of

$$\Delta T = \frac{0.01032 \text{ V}}{0.0065 \text{ V/°C}} = \mathbf{1.59°C}$$

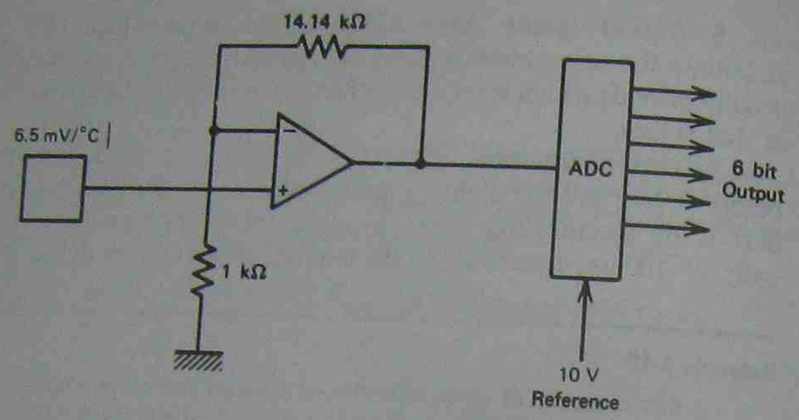


Figure 3.14 Circuit for Example 3.18.

Microprocessor compatible ADCs

Just as with DACs, a whole line of ADCs have been developed that interface easily with microprocessor-based computers. The ADCs have built-in tri-state outputs so that they can be connected directly to the data bus of the computer. Data from the ADC is only placed on the data bus lines when the computer issues an appropriate enable command (often called a READ). Figure 3.15 shows how the ADC appears when connected to the environment of the microprocessor-based computer. The ADC appears much the same as memory. In some cases an ADC input is actually taken by the computer using a memory-read instruction.

The decoding circuitry is necessary to provide the start-convert command, to input the convert-complete response from the ADC, and to issue the tri-state enable back to the ADC.

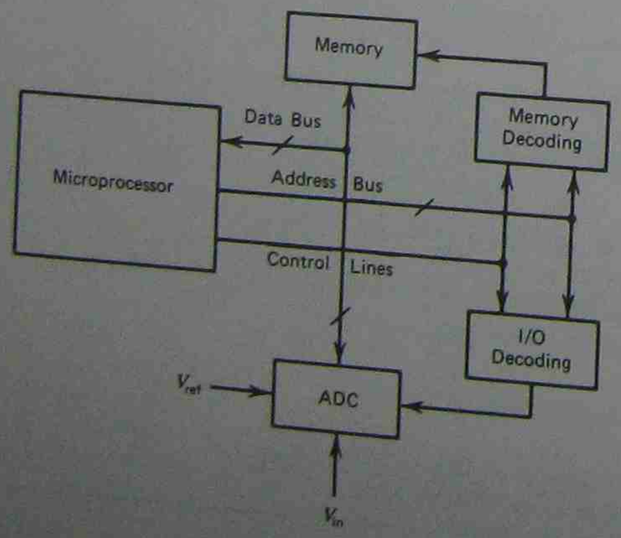


Figure 3.15 A typical microprocessor-based computer with ADC interface.

Data input boards

Just as in the case of DACs, there are now many types of data input boards for personal computers. These boards, which plug into expansion slots, contain the ADC(s), addressing and decoding, bus interface, and the reference for the converter. Often, many channels of input can be taken from a single board. In most cases, the manufacturer will provide user manuals and software in a common language for use in data acquisition systems.

Sample and hold

The ADC requires a certain length of time to determine the appropriate digital output from an analog input. For different ADCs, this time varies from a few microseconds to several milliseconds. It is clear that the input voltage should not change during the conversion.

For slowly varying signals and converters performing the conversion in a few microseconds, this is not a problem. In some cases, however, the signal change rate and conversion rate are of the same order. In these cases it is necessary to "freeze" the input signal during conversion. This can be done using a special op amp circuit called a *sample and hold*.

The circuit in Figure 3.16 shows the essential elements of a sample and hold. The field effect transistor (FET) on the input operates as a simple switch. When it is in the "closed" state, the voltage on the capacitor follows the input voltage. The capacitor voltage is coupled to the output through the very high input impedance voltage follower.

When the FET is driven to the "open" state, the voltage on the capacitor will hold the last value before the open state of the FET occurred. It is possible now to measure this value using the voltage follower, because its high input impedance will not appreciably discharge the capacitor.

This circuit is placed between the signal source and the ADC. It is normally in the closed or sample state. When a conversion is to be made, the FET is first driven to the open or hold state. Then the converter is started and conversion proceeds. When the data acquisition is complete, the FET is driven back to the sample state.

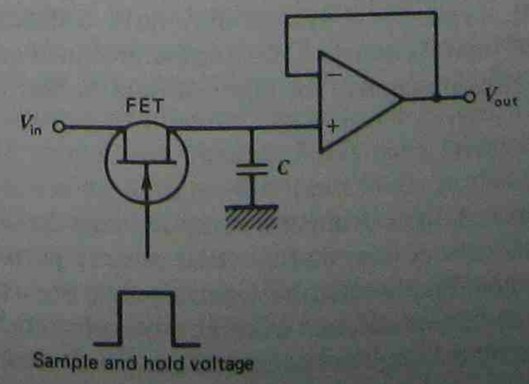


Figure 3.16 The principal elements of a sample and hold circuit.

3.4 DATA ACQUISITION SYSTEMS

A digital computer can make a tremendous number of calculations in a second, because the typical time required to execute one instruction may be only a few microseconds. For example, a typical microprocessor can add two 8-bit binary numbers in 2 μs. By contrast, most process-control installations involve process variable variations with a time scale on the order of minutes. For this reason and others discussed in Chapter 11, the efficient use of computers in process control means that a single computer may control many variables. To do this, the computer periodically *samples* the value of a variable, evaluates it according to programmed control operations, and outputs an appropriate controlling signal to the final control element. Under the program control, the computer then selects another of the controlled variables, samples, evaluates, and outputs, and so on for all the loops under its control. Getting a sample of a real-world number into the computer is not easy. It requires a combination of hardware and software (programs) to enable the computer to read in a number that may represent some process variable, such as temperature, pressure, and so on. The overall process of doing this, and its reverse of output, is called by the general term *interface*. One can take an ADC and any necessary amplifiers and write the programs required to put together an interface to some computer for a process application. If the computer is to control many loops, we would need such a system for each variable to be inputted. Instead, for input we can use a data acquisition system (DAS) that allows sampled variables from many sources to be inputted to the computer with appropriate programming.

3.4.1 Data Acquisition System (DAS)

There are many different types of data acquisition systems, but it is possible to generalize the essential elements as shown in Figure 3.17. The following paragraphs present general descriptions of each block of the DAS. Most data acquisition systems are available as small modules containing the circuits shown in Figure 3.17. In general, the module accepts a number of analog inputs, called *channels*, as either differential voltage signals (two-wire) or single-ended voltage signals (referred to ground). Typically, a system may have 8 differential input channels or 16 single-ended input channels. The computer can then select any one of the channels under program control for input of data in that channel.

Address decoder

This part of the DAS accepts an input from the computer via the address lines (16 bits for a typical 8-bit microprocessor) that serve to select a particular analog channel to be sampled. The module is often designed so that the association of a particular channel and a computer address word can be selected by the user. In some cases, this is done by making the module channel addresses appear to

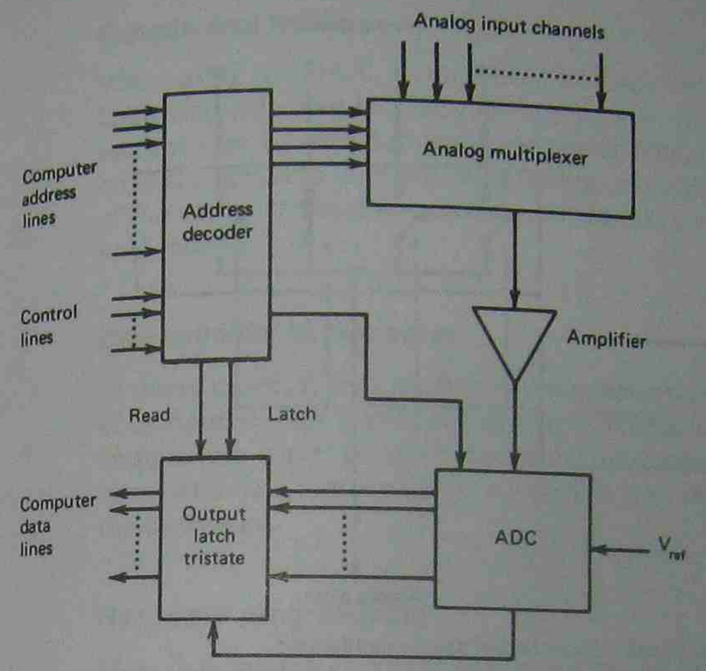


Figure 3.17 Data acquisition system.

the computer as addresses of memory locations. Thus, if the computer executes a command to fetch the contents of some memory location, it may actually be selecting some analog input channel. In other words, the selecting of an input channel is equivalent to reading the contents of a memory location. In other systems, a binary code is sent from the computer through special input/output devices to select an analog channel and input the data on that channel. In such cases, the selection of a channel is done by what may be called a *device select* code.

Analog multiplexer

This element of the DAS is essentially a solid-state switch that takes the decoded address signal and selects the data for the selected channel by closing a switch connected to that analog input line.

As shown in Figure 3.18 for a single-ended system, the multiplexer accepts an input from the address decoder and uses this to close the appropriate switch to allow that channel signal to be passed to the next stage of the DAS. Figure 3.18 shows that channel 2 has been selected, which would probably have been selected by a **10** on the input lines. In this sense, **00** then would select channel 0, **01** channel 1, **10** channel 2, and **11** channel 3. Thus, the address decoder must convert the computer address line to one of these four possibilities when the DAS has been addressed by the computer. The actual switch elements are usually field effect transistors (FETs) that have an "on" resistance of a few hundred ohms and an "off" resistance of hundreds to thousands of megohms.

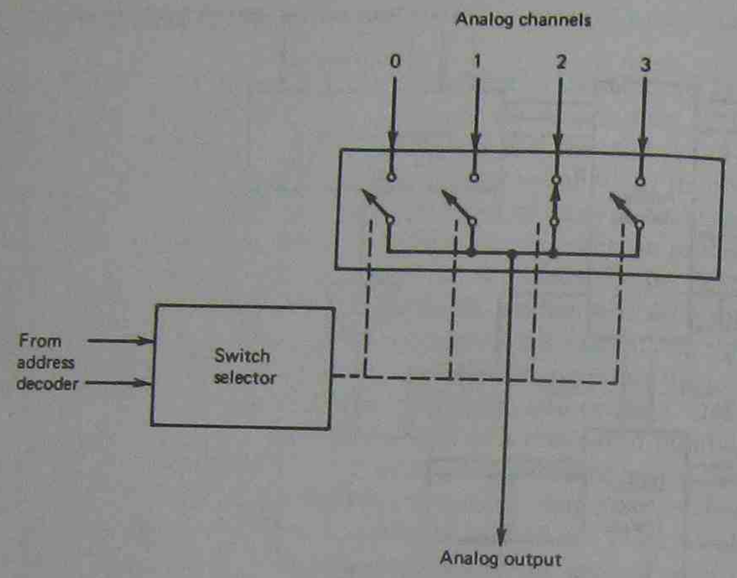


Figure 3.18 Four-channel analog multiplexer.

Amplifier

Most data acquisition systems include a variable gain amplifier that allows the user to compensate for the input level of the signals. The integral ADC usually is designed to work from a definite unipolar or bipolar input range so that input levels must be adjusted to fall within this range. Thus, if the ADC signal input must be in the range of 0 to 5 volts, the amplifier is given a gain to assure that the inputs will be within this range. If there is a great difference between the various input signal levels, some signal conditioning may be required prior to application of the signal to the DAS.

ADC

Of course, an important part of the DAS is an analog-to-digital converter. The converter will accept voltages that span a specific range as provided by the preceding signal conditioning. The converter usually can be configured to accept either unipolar or bipolar inputs. Features such as offset adjustment and full-scale adjustment are common.

3.4.2 Application Notes

There are numerous factors that must be considered when a DAS is to be used. The following paragraphs discuss several of these factors.

Sample and hold

When using the DAS, account must be made for the fact that the signals on the input channels may be changing very rapidly. If the changes are fast enough so that the signal varies during the conversion time, a sample and hold must be used on that channel to hold the value during conversion. This adds to the complexity of the software because account must be taken of commands to the sample and hold module.

Compatibility to computer

In many cases, a data module is designed to work with only one model or type of computer. This is particularly true of microprocessor-based computers where architecture varies greatly between microprocessor models. Thus, it is necessary to select a data module that is compatible with the input/output characteristics of the computer.

Hardware programming

Most data modules give the user many options for use in input/output operations. These options include unipolar/bipolar operation, address selection, amplifier gain, differential/single-ended operation, and others. They are typically selected by wired jumpers between pins of the module or by the attachment of resistors as specified in the specification sheet of the module.

Software programming

Another important aspect of input/output interfacing is the software routines that will use the data modules. These routines must be compatible with the hardware programming and the other characteristics of the module. The programs may include delays waiting for the ADC to complete conversion, for example. This aspect is discussed further in Chapter 11.

Overall response time

A data acquisition system does not provide the digital conversion of data on a selected channel the instant the selection occurs. Rather, there is a delay while the multiplexer acquires the system channel, while the amplifier settles to the value on the channel, and while the ADC performs the conversion operations. This time will be important for a determination of the maximum sampling rate from the DAS. The time may run from tens of microseconds to hundreds of microseconds, depending on the number of bits converted, gains of the amplifiers, and signal-switching speed.

SUMMARY

This chapter provides a digital electronics background to make the reader conversant with the elements of digital signal processing and able to perform simple analysis and design as associated with process control.

1. The use of digital words enables the encoding of analog information into a digital format.

2. It is possible to encode fractional decimal numbers as binary and vice versa using

$$N_{10} = b_1 2^{-1} + b_2 2^{-2} + \cdots + b_m 2^{-m} \tag{3.1}$$

3. Boolean algebra techniques can be applied to the development of process alarms and elementary control functions.

4. Digital electronic gates and comparators allow the implementation of process Boolean equations.

5. DACs are used to convert digital words into analog numbers using a fractional number representative. The resolution is

$$\Delta V = V_R 2^{-n} \tag{3.7}$$

6. An ADC of the successive approximations type determines an output digital word for an input analog voltage in as many steps as bits to the word.

7. The dual slope ADC converts analog-to-digital information by a combination of integration and time counting.

8. The data acquisition system (DAS) is a modular device that interfaces many analog signals to a computer. Signal address decoding, multiplexing, and ADC operations are included in the device.

PROBLEMS

Section 3.2

3.1 Convert the following binary numbers into decimal, octal, and hex: (a) $\mathbf{1010_2}$, (b) $\mathbf{111011_2}$, (c) $\mathbf{010110_2}$.

3.2 Convert the following binary numbers into decimal, octal, and hex: (a) $\mathbf{1011010_2}$, (b) $\mathbf{0.1101_2}$, (c) $\mathbf{1011.0110_2}$.

3.3 Convert the following decimal numbers into binary, octal, and hex: (a) 21_{10}, (b) 630_{10}, (c) 427_{10}.

3.4 Convert 27.156_{10} into a binary number with the fractional binary part expressed in 6-bits. What actual decimal does this binary equal?

3.5 Find the 2s complement of (a) $\mathbf{1011_2}$, (b) $\mathbf{10101100_2}$.

3.6 Prove by a table of values that $\overline{A \cdot B} = \overline{A} + \overline{B}$ (DeMorgan's theorem).

3.7 Show that the Boolean equation $A \cdot B + A \cdot \overline{A \cdot B)}$ reduces to A.

3.8 A process control's moving speed, load weight, and rate of loading in a conveyor system. The variables are provided as high (**1**) and low (**0**) levels for digital control. An alarm should be initiated whenever any of the following occur:
- **a.** Speed is low; both weight and loading rate are high.
- **b.** Speed is high; loading rate is low.

Find a Boolean equation describing the required alarm output. Let the variables be S for speed, W for weight, and R for loading rate.

3.9 Implement Problem 3.8 with (a) AND/OR logic and (b) NAND/NOR logic.

Section 3.3

3.10 A sensor provides temperature data as 360 μV/°C. Develop a comparator circuit that goes high when the temperature reaches 530°C.

3.11 A light level is to trigger a comparator high (5 V) when the intensity reaches 30 W/m^2. Intensity is converted to voltage according to a transfer function of 0.04 V/(W/m^2). Noise is found to contribute ±1.6 W/m^2 of intensity fluctuations. Develop a hysteresis comparator to provide the required output and immunity for noise.

3.12 A 6-bit DAC has an input of $\mathbf{100101_2}$ and uses a 10.0-volt reference. (a) Find the output voltage produced. (b) Specify the conversion resolution.

3.13 A 4-bit DAC must have an 8.00-volt output when all inputs are high. Find the required reference.

3.14 An 8-bit DAC with a 5.00-volt reference connects to a light source with an intensity given by $I_L = 45V^{(3/2)}$ W/m^2.
- **a.** What is the range of intensity which can be produced?
- **b.** What intensities are produced by digital inputs of 1BH, 7AH, 9FH, and E5H?
- **c.** Plot the intensity versus hex input, and comment on linearity.

3.15 An 8-bit ADC with a 10.0-volt reference has an input of 3.797 volts. Find the digital output word. What range of input voltages would produce this same output? Suppose the output of the ADC is $\mathbf{10110111_2}$. What is the input voltage?

3.16 An ADC that will encode pressure data is required. The input signal is 666.6 mV/psi.
- **a.** If a resolution of 0.5 psi is required, find the number of bits necessary for the ADC. The reference is 10.0 volts.
- **b.** Find the maximum measurable pressure.

3.17 A bipolar ADC has 10 bits and a 10.00-volt reference. What output is produced by inputs of −4.3 V, −0.66 volts, +2.4 volts, and +4.8 volts? What is the input voltage if the output is 30BH?

3.18 A sample and hold circuit like the one shown in Figure 3.16 has $C = 0.47$ μF, and the ON resistance of the FET is 75 Ω. For what signal frequency is the sampling capacitor voltage down 3 dB from the signal voltage? How does this limit the application of the sample hold?

Section 3.4

3.19 A DAS has an ADC of 8 bits with a 0- to 2.5-volt range of input for 00H to FFH output (i.e., FEH to FFH occurs at 2.50 volts). Inputs are temperature from 20 to 100°C scaled at 40 mV/°C, pressure from 1 to 100 psi scaled at 100 mV/psi, and flow

CHAPTER 7

FINAL CONTROL

INSTRUCTIONAL OBJECTIVES

In this chapter, the general techniques used to implement the final control element function are presented. After you have read this chapter, you should be able to

1. **Define the three parts of final control operation.**
2. **Give two examples of electrical signal conversion.**
3. **Make a diagram and describe the operating principles of the flapper/nozzle pneumatic system.**
4. **Describe the operating principle of ac, dc, and stepping motors.**
5. **Explain how a pneumatic positioning actuator functions in both the direct and reverse modes.**
6. **Contrast quick-opening, linear, and equal percentage control valves in terms of the flow versus stem position.**
7. **Explain how control valve sizing techniques allow selection of the proper size of control valve.**

7.1 INTRODUCTION

In a typical process-control application, the measurement and evaluation of some process variable are carried out by a low-energy analog or digital representation of the variable. The control signal that carries feedback information back to the

process for necessary corrective action is expressed by the same low level o representation. In general, the controlled process itself may involve a high-energ condition, such as the flow of thousands of cubic meters of liquid or severa hundred thousand newton hydraulic forces, as in a steel rolling mill. The functio of the final control element is to translate low-energy control signals into a leve of action commensurate with the process under control. This can be considere an amplification of the control signal, although in many cases the signal is als converted into an entirely *different* form.

In this chapter, the general concepts to implement the final control elemer function are presented together with specific examples in several areas of proces control.

A sensor used to measure some variable in a process-control applicatio should have negligible effect on the process itself. It follows that sensor selectio is based mainly on required measurement specifications and necessary protection (of the sensor) from harmful effects of the process environment. In sensor selec tion, the process-control technologist need not have intimate knowledge of th mechanisms of the process itself.

These arguments do not apply, however, when considering the *final contro element*. By necessity, the final control element has a profound effect on th process and therefore must be selected after detailed considerations of the proces operational mechanisms. Such a selection, therefore, cannot be the responsibilit of the process-control technologist alone. In this view, the process-control tech nologist should have sufficient background on the final control element and it associated signal conditioning to know how such devices interface with precedin process controllers and transducers. The technologist should be able to com municate and work closely with process engineers on these subjects. The objec tives of this chapter were selected to fulfill such responsibility.

7.2 FINAL CONTROL OPERATION

Final control element operations involve the steps necessary to convert the contro signal (generated by a process controller) into proportional action on the proces itself. Thus, to use a typical 4–20 mA control signal to vary a large flow rate from say, 10.0 m^3/min to 50.0 m^3/min certainly requires some intermediate operations The specific intermediate operations vary considerably depending on the process control design, but certain generalizations can be made regarding the steps leadin from the control signal to the final control element. For a typical process-contro application the conversion of a process-controller signal to a control function can be represented by the steps shown in Figure 7.1. The input control signal may take many forms, including an electric current, digital signal, or pneumatic pres sure.