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- Understanding is reinforced with frequent worked examples
- Uses manufacturers' data sheets and real engineering problems
- Contains up-to-date treatment of current trends and chip technology

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ELECTRONIC

instrumentation and measurements

David A. Bell

ELECTRONIC INSTRUMENTATION AND MEASUREMENTS

David A. Bell

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CONTENTS

PREFACE ix

1 BASIC DEFLECTION INSTRUMENTS 1

Introduction 1
1-1 Fundamentals of Deflection Instruments 2
1-2 Permanent-Magnet Moving-Coil Instrument 7
1-3 The Electrodynamic Instrument 11
1-4 Moving-Iron Instruments 14
1-5 The Galvanometer 16
1-6 Errors in Deflection Instruments 19
Review Questions and Problems 22

2 DEFLECTION TYPE AMMETERS, VOLTMETERS, AND WATTMETERS 25

Introduction 25
2-1 DC Ammeter 26
2-2 DC Voltmeter 34
2-3 Rectifier Voltmeters 41
2-4 Rectifier Ammeters 48
2-5 Electrodynamic Voltmeter and Ammeter 50
2-6 Electrodynamic Wattmeter 53
2-7 Thermocouple Instruments 59
Review Questions and Problems 64

3 THE OHMMETER AND THE VOLT-OHM-MILLIAMMETER 67

Introduction 67
3-1 Series Ohmmeter 67
3-2 Multirange Shunt Ohmmeter 74
3-3 Ohmmeter Accuracy 78
3-4 The Volt-Ohm-Milliammeter or Multimeter 80
3-5 Using the VOM as an Ammeter 82
3-6 Using the VOM as a Voltmeter 84
3-7 Decibel Measurement by VOM 85
3-8 VOM Adapters and Probes 89
Review Questions and Problems 89

4 ERRORS IN MEASUREMENTS 91

Introduction 91
4-1 Absolute and Relative Errors 91
4-2 Observer Errors 93
4-3 Accuracy, Precision, and Resolution 93
4-4 Systematic Errors 95
4-5 Random Errors 99
Review Questions and Problems 100

5 THE DC POTENTIOMETER AND INSTRUMENT CALIBRATION 103

Introduction 103
5-1 Standard Cell 103
5-2 Basic DC Potentiometer 105
5-3 Potentiometer with Switched Resistors 107
5-4 Multirange Potentiometer 110
5-5 DC Ammeter Calibration by Potentiometer 114
5-6 DC Voltmeter Calibration by Potentiometer 117
5-7 Wattmeter Calibration by Potentiometer 119
5-8 Calibration of AC Instruments 120
5-9 Instrument Calibration Procedures and Accuracy 121
5-10 Self-balancing Potentiometer 123
Review Questions and Problems 124

6 PRECISE RESISTANCE MEASUREMENTS 127

Introduction 127
6-1 Voltmeter and Ammeter Methods 127
6-2 Resistance Measurement by Potentiometer 131
6-3 The Wheatstone Bridge 132
6-4 Low Resistance Measurement 139
6-5 High Resistance Measurement 142
6-6 The Megohmmeter 145
Review Questions and Problems 146

7 ALTERNATING CURRENT BRIDGES 149

Introduction 149
7-1 General AC Bridge Theory 149
7-2 Detectors for AC Bridges 152
7-3 Simple Capacitance Bridge 154
7-4 CR and LR Equivalent Circuits Q Factor and D Factor 157
7-5 Series-Resistance Capacitance Bridge 162
7-6 Parallel-Resistance Capacitance Bridge 165
7-7 The Inductance Comparison Bridge 170
7-8 The Maxwell Inductance Bridge 172
7-9 The Hay Inductance Bridge 175
7-10 Multifunction Impedance Bridge 179
7-11 Owen, Schering, and Wien Bridges 186
7-12 AC Bridge Sensitivity, Accuracy, and Residuals 188
Review Questions and Problems 190

8 ANALOG ELECTRONIC INSTRUMENTS 193

Introduction 193
8-1 Transistor Operation 193
8-2 Field Effect Transistors 196
8-3 Transistor Emitter Follower Voltmeter 196
8-4 FET Input Voltmeter 208
8-5 Transistor Amplifier Voltmeters 211
8-6 Integrated Circuit Operational Amplifiers in Voltmeters 219
8-7 Vacuum Tube Voltmeters 226
8-8 The Ohmmeter Function in Electronic Multimeters 231
8-9 AC Electronic Voltmeters 237

8-10 Current Measurement with Analog Electronic Instruments 249
8-11 Electronic Galvanometers 250
8-12 Multirange Analog Electronic Voltmeter 252
Review Questions and Problems 254

9 BASICS OF DIGITAL INSTRUMENTS 259

Introduction 259
9-1 Transistor Switching 259
9-2 Basic Logic Gates 261
9-3 The Flip-Flop 265
9-4 Counting Circuits 272
9-5 Digital Displays or Readouts 276
9-6 Display Drivers 279
9-7 Scale-of-2000 Counter 281
Review Questions and Problems 283

10 DIGITAL INSTRUMENTS 285

Introduction 285
10-1 Time Base 285
10-2 Latch and Display Enable 288
10-3 Basic Digital Frequency Meter System 288
10-4 Frequency Measurements, Errors, and Reciprocal Counting 292
10-5 Time and Ratio Measurement 294
10-6 Input Attenuation and Amplification 296
10-7 Specifications for Digital Counter/Timers 297
10-8 Digital Voltmeter System 298
10-9 Digital Measurement of Current Resistance and AC Quantities 305
10-10 Digital Multimeter 305
10-11 Digital LCR Measurements 308
Review Questions and Problems 313

11 CATHODE-RAY OSCILLOSCOPES 315

Introduction 315
11-1 The Cathode-Ray Tube 315
11-2 Deflection Amplifiers 320

11-3 Waveform Display 322
11-4 Oscilloscope Time Base 326
11-5 Dual-Trace Oscilloscopes 336
11-6 Oscilloscope Controls 341
11-7 Measurement of Voltage, Frequency, and Phase 343
11-8 Pulse Measurements 347
11-9 Oscilloscope Probes 353
11-10 Display of Device Characteristics 360
11-11 Lissajou Figures 363
Review Questions and Problems 368

12 SPECIAL OSCILLOSCOPES 373

Introduction 373
12-1 Delayed Time Base Oscilloscope 374
12-2 Analog Storage Oscilloscope 384
12-3 Sampling Oscilloscopes 388
12-4 Digital Storage Oscilloscope 395
Review Questions and Problems 407

13 GRAPHIC RECORDING INSTRUMENTS 411

Introduction 411
13-1 Galvanometric Strip Chart Recorder 411
13-2 Potentiometric Strip Chart Recorder 414
13-3 Solid State Electrode Strip Chart Recorder 417
13-4 XY Recorder 419
13-5 Plotting Device Characteristics on an XY Recorder 425
13-6 Memory Recorder 426
Review Questions and Problems 427

14 DC POWER SUPPLIES 429

Introduction 429
14-1 Unregulated DC Power Supplies 429
14-2 Basic DC Voltage Regulators 436
14-3 Operational Amplifier Regulators and IC Voltage Regulators 443
14-4 DC Power Supply Performance and Use 451
14-5 Power Supply Testing 453
14-6 Switching Regulators 456
Review Questions and Problems 458

15 SIGNAL GENERATORS 461

Introduction 461
15-1 Low Frequency Sine Wave Generators 462
15-2 Function Generators 469
15-3 Pulse Generators 478
15-4 RF Signal Generators 487
15-5 Sweep Frequency Generators 494
15-6 The Frequency Synthesizer 498
Review Questions and Problems 501

16 MISCELLANEOUS INSTRUMENTS 505

Introduction 505
16-1 Distortion Analyzer 505
16-2 The Q Meter 511
16-3 Spectrum Analyzer 518
Review Questions and Problems 524

INDEX 526

PREFACE

In this book, I discuss the measuring instruments and techniques normally encountered in an electronics technology laboratory. An understanding of basic electric circuitry is assumed, and prior knowledge of transistor circuits is preferable, although brief explanations of bipolar transistors, FETs, and IC operational amplifiers are included in the text.

The first half of the book treats the operation, calibration, and use of deflection instruments, as well as dc and ac bridges and techniques for measuring voltage, current, power, resistance, inductance, and capacitance. Coverage includes: the volt-ohm-milliameter, the dc potentiometer, precise resistance measurements, and ac bridge applications.

The final nine chapters of the book (the second half) are devoted to electronics (rather than electrical) instruments, beginning with analog electronic voltmeters. Basic digital circuits are introduced prior to the study of digital instruments. Included in these chapters are: digital measurements of f, V, I, R, L, and C; oscilloscopes; delayed time base scopes and digital scopes; XY recorders; sine wave and pulse generators; and the spectrum analyzer.

Efforts have been made throughout the text to explain each instrument as thoroughly as possible and to describe performance characteristics and appropriate applications. However, complete books have been written about individual instruments, so there are limitations to the depth and range of treatment possible. I would very much like to receive comments

from users of the book—suggestions for improvements and/or inclusions in the second edition and notifications of errors.

I am hopeful that this book will prove useful as a text for college and university measurement courses and as a handbook for technicians, technologists, and engineers.

David Bell

1

BASIC DEFLECTION INSTRUMENTS

INTRODUCTION

All deflection instruments require three forces for correct functioning: a deflecting force, a controlling force, and a damping force. Usually, the deflecting force is generated by a magnetic field produced by a current flowing through a coil. This field interacts with another magnetic field which may be from a permanent magnet or from other current-carrying coils. The coil is pivoted so that it can rotate and deflect a pointer over a scale. The controlling force is almost always provided by spirally wound springs which oppose the rotation of the coil. Most instruments use eddy current damping which is produced by nonmagnetic conductors in motion through a magnetic field.

The most common deflection instrument in use today is the permanent-magnet moving-coil (PMMC) instrument. The PMMC instrument is essentially a dc meter, although it can be used on ac when rectifiers are employed. It has an easy-to-read linear scale and can be manufactured to be sensitive to extremely low current levels.

The electrodynamic instrument differs from the PMMC instrument by the use of stationary coils instead of a permanent magnet. The most important advantage of an electrodynamic instrument is that it can be used directly for ac or dc measurements.

In the moving-iron instrument, two iron vanes are magnetized with the same polarity by a current flowing in a coil. The resultant repulsion force between the vanes produces pointer deflection.

1-1 FUNDAMENTALS OF DEFLECTION INSTRUMENTS

The outside appearance of a simple deflection ammeter shows two terminals identified as + and −, and a pointer which moves over a calibrated scale. The electromechanical mechanism (or *movement*) inside the instrument must cause the pointer to accurately indicate the current flowing through the instrument. For this to occur, three forces are involved: a *deflecting force*, a *controlling force*, and a *damping force*.

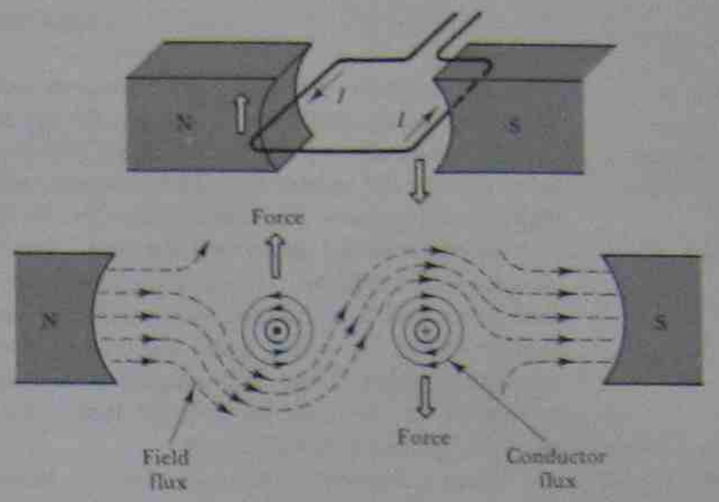
The *deflecting force* causes the pointer to move from its zero position when a current flows. In the *permanent-magnet moving-coil* (PMMC) instrument the deflecting force is magnetic. When a current flows in a lightweight moving coil pivoted between the poles of a permanent magnet [Figure 1-1(a)], the current sets up a magnetic field which interacts with the field of the permanent magnet. A force is exerted upon a current-carrying conductor situated in a magnetic field. Consequently, a force is exerted upon the coil turns, as illustrated, causing the coil to rotate on its pivots. The pointer is fixed to the coil, so it moves over the scale as the coil rotates.

The *controlling force* is the force which returns the coil and pointer to their initial zero position when current ceases to flow in the coil. The controlling force also balances the deflecting force so that, for a constant current in the coil, the pointer remains stationary at the appropriate position on the scale. If there were no (or too little) controlling force, the pointer would be damaged by excessive deflection when a small current flows.

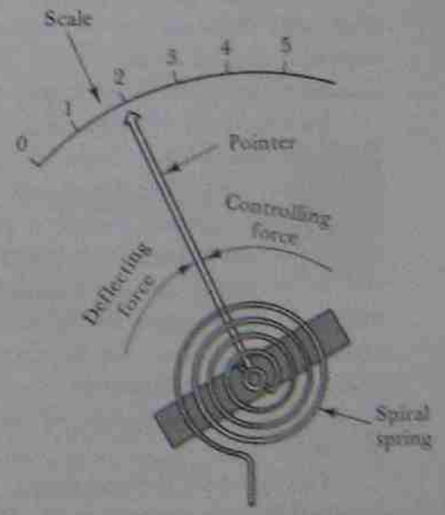
In the PMMC instrument the controlling force is provided by spiral springs [see Figure 1-1(b)]. The springs retain the coil and pointer at their zero position when no current is flowing. When current flows, the springs "wind up" as the coil rotates, and the force they exert on the coil increases. The coil and pointer stop rotating when the controlling force becomes equal to the deflecting force.

The spiral springs have a large number of turns so that they are not severely distorted when wound up by the motion of the coil. The spring material must be nonmagnetic to avoid any magnetic field influence on the controlling force. Since the springs are also used to make electrical connection to the coil, they must have a low resistance. Phosphor bronze is the material usually employed.

Suppose only the deflecting force and controlling force are present. An applied deflecting force rotates the coil and pointer and winds up the springs. Instead of stopping at the point where the controlling force equals the deflecting force, the inertia of the moving system causes the coil and pointer to continue past this position. Then, as the springs wind up tighter, the controlling force exerted by the springs becomes greater than the deflecting force. The coil and pointer are now pushed back towards the position at which the two forces are equal. However, once again the inertia of the moving parts causes the coil and pointer to swing past this position.



(a) The deflecting force in a PMMC instrument is provided by a current-carrying coil pivoted in a magnetic field.



(b) The controlling force from the springs balances the deflecting force.

FIGURE 1-1. Deflecting force and controlling force for a PMMC instrument.

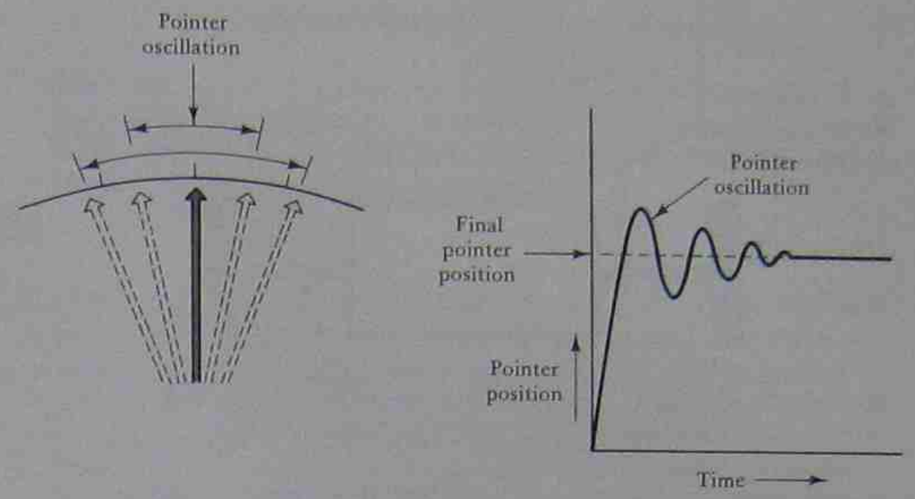
Now the magnetic deflecting force becomes greater than the controlling force once more, and the coil and pointer are again rotated towards the position where the two forces are equal. The process is repeated over and over, causing the pointer to oscillate for some time before it finally settles down at one position. The effect is illustrated in Figure 1-2(a).

To minimize (or damp out) the oscillations of the pointer and coil, a *damping force* is required. The damping force must be present only when the instrument coil is in motion. Any additional force when the coil is stationary would, of course, upset the balance between the deflecting and controlling forces. Thus, the damping force should be generated by the movement of the coil. In PMMC instruments the damping force is normally provided by *eddy currents*.

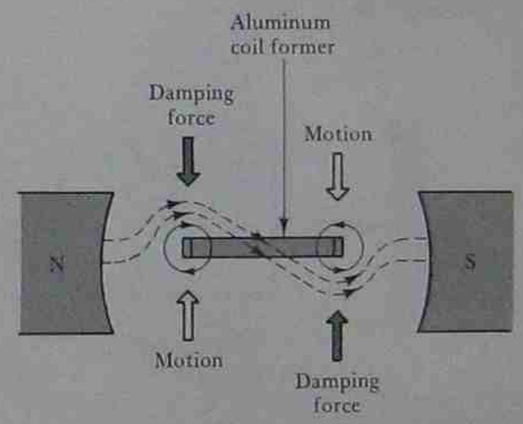
When a short-circuited conductor is in motion in a magnetic field, a current is induced in the conductor. The direction of this current is such that it sets up its own magnetic field which opposes the motion of the conductor. In a PMMC instrument the *former* (or frame) on which the coil is wound is usually constructed of aluminum, a nonmagnetic conductor. As the coil rotates within the magnetic field, a current is induced in the aluminum coil former [Figure 1-2(b)], and this sets up a flux which effectively *damps out* the oscillations of the coil and pointer. This induced current is termed an *eddy current*. When coil motion ceases, no eddy current is induced and there is no longer any damping force.

Two methods of supporting the moving system of a deflection instrument are illustrated in Figure 1-3. In the *jewelled-bearing* suspension shown in Figure 1-3(a), the pointed ends of shafts or *pivots* fastened to the coil are inserted into circular v-cuts in jewel (sapphire or glass) bearings. This allows the coil to freely rotate with the least possible friction. Although the coil is normally very lightweight, the pointed ends of the pivots have extremely small areas, so the surface load per unit area can be considerable. In some cases the bearings may be broken by the shock of an instrument being slammed down heavily upon a bench. Some jewel bearings are spring supported (as illustrated) to more easily absorb such shocks.

The *taut-band* method shown in Figure 1-3(b) is much tougher than jewelled-bearing suspension. As illustrated, two flat metal ribbons (phosphor bronze or platinum alloy) are held under tension by springs to support the coil. Because of the springs, the metal ribbons behave like rubber under tension. The ribbons also exert a controlling force as they twist, and they can be used as electrical connections to the moving coil. Because there is less friction, taut-band instruments can be much more sensitive than the jewelled-bearing type. A full-scale deflection (FSD) of 25 μA is a typical minimum for a jewelled-bearing instrument. With taut-band suspension, an FSD (or *sensitivity*) of 2 μA is possible. The fact that the spring-mounted ribbon behaves as a rubber band makes the instrument

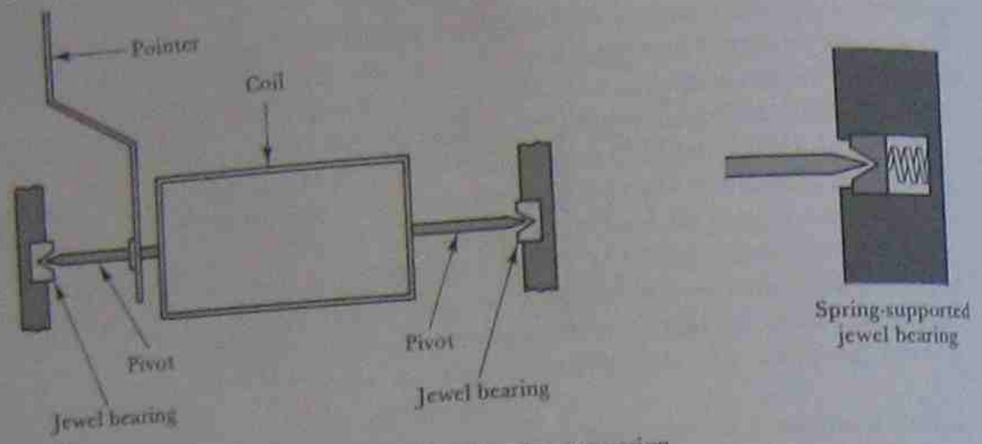


(a) Lack of damping causes the pointer to oscillate.

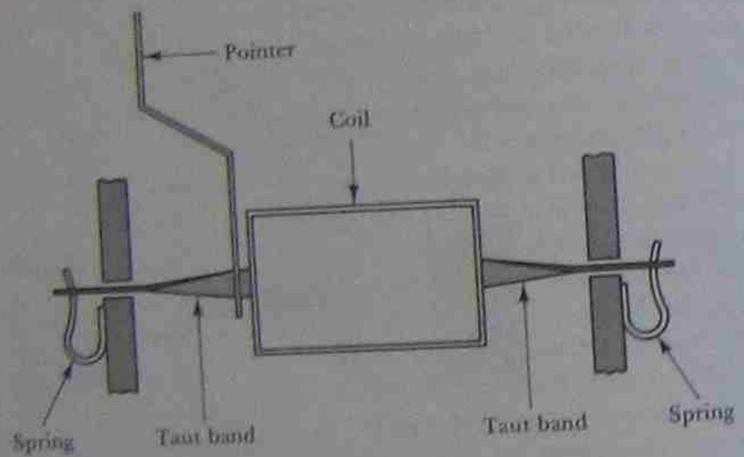


(b) The damping force in a PMMC instrument is provided by eddy currents induced in the aluminum coil former as it moves through the magnetic field.

FIGURE 1-2. Damping force in a PMMC instrument.



(a) Pivot and jewel-bearing suspension



(b) Taut-band suspension

FIGURE 1-3. Jewel-bearing and taut-band methods of supporting the coil in a PMMC instrument.

extremely rugged compared to a jewelled-bearing instrument. If a jewelled-bearing instrument is dropped to a concrete floor from bench height, the bearings will almost certainly be shattered. A taut-band instrument is unlikely to be affected by a similar fall.

1-2 PERMANENT-MAGNET MOVING-COIL INSTRUMENT

1-2-1 Construction

Details of the construction of a PMMC instrument or *D'Arsonval instrument* are illustrated in Figure 1-4. The main feature is a permanent magnet with two soft iron *pole shoes*. A cylindrical soft iron *core* is positioned between the shoes so that only very narrow air gaps exist between the core and the faces of the pole shoes. The lightweight moving coil is pivoted to move within these narrow air gaps. The air gaps are made as narrow as possible in order to have the strongest possible level of magnetic flux crossing the gaps.

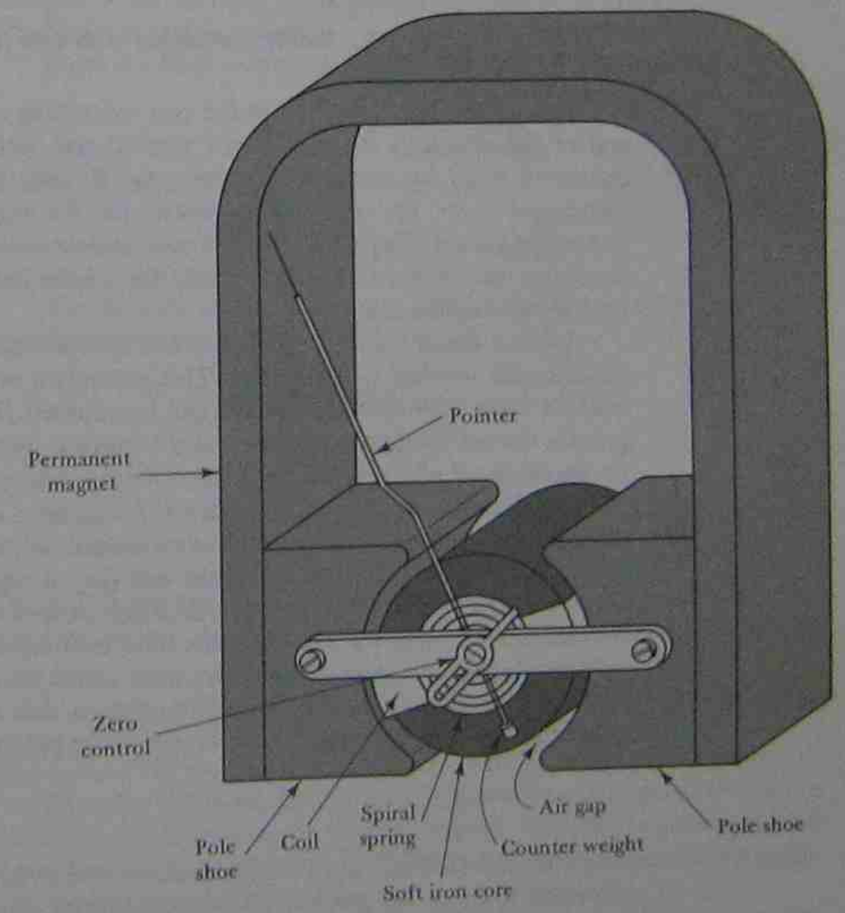


FIGURE 1-4. Electromechanical system of a PMCC instrument.

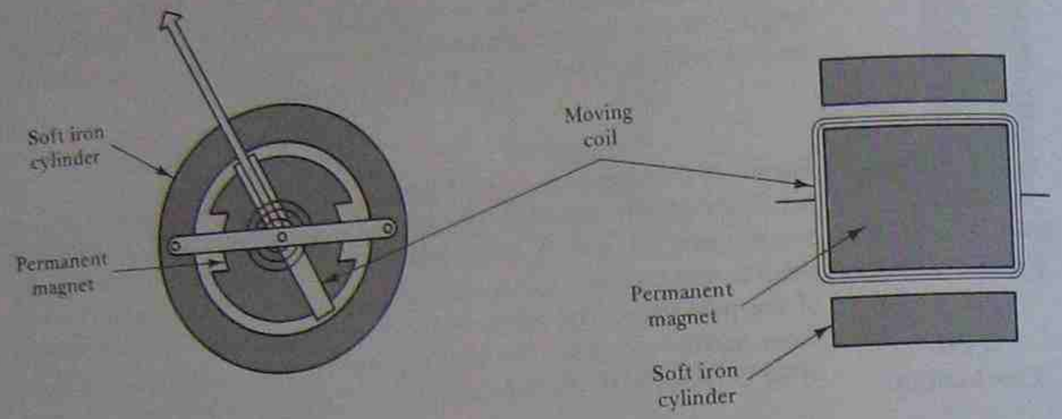


FIGURE 1-5. PMMC instrument with core magnet.

Figure 1-4 also shows one of the two controlling spiral springs. One end of this spring is fastened to the pivoted coil, and the other end is connected to an adjustable *zero-position-control*. By means of a screw on the instrument cover, the zero-position-control can be adjusted to move the end of the spring. This allows the coil and pointer position to be adjusted (when no coil current is flowing) so that the pointer indicates exactly zero on the instrument scale.

Another detail shown in Figure 1-4 is one of (usually) two or three *counterweights* attached to the pointer. This is simply a machine screw along which a small screw-threaded weight can be adjusted. The counterweights provide correct mechanical balance of the moving system so that there is no gravitational effect on the accuracy of the instrument.

The PMMC instrument in Figure 1-5 illustrates a different type of construction. Instead of using a horseshoe-shaped permanent magnet, the permanent magnet is placed inside the coil (i.e., it replaces the soft iron core shown in Figure 1-4). A thick cylindrical piece of soft iron surrounds the coil and the magnet. The magnetic flux flows across the air gaps and through the soft iron, and the coil sides move within the narrow air gaps. A major advantage of this type of construction is that the moving coil is shielded from external magnetic fields due to the presence of the soft iron cylinder.

1-2-2 Operation

The current in the coil of a PMMC instrument must flow in one particular direction to cause the pointer to move (positively) from the zero position over the scale. When the current is reversed, the interaction of the magnetic flux from the coil with that of the permanent magnet causes the

coil to rotate in the opposite direction, and the pointer is deflected to the left of zero, i.e., off-scale. The terminals of a PMMC instrument are identified as + and − to indicate the correct polarity for connection, and the instrument is said to be *polarized*.

Because it is polarized, the PMMC instrument cannot be used directly to measure alternating current. Without rectifiers, it is purely a dc instrument.

1-2-3 Torque Equation and Scale

When a current I flows through a one-turn coil situated in a magnetic field, a force F is exerted on each side of the coil:

$$F = BIl \text{ Newtons}$$

where B is the field flux in Teslas, I is the current in Amperes, and l is the length of the coil in meters.

Since the force acts on each side of the coil, the total force is

$$F = 2BIl \text{ Newtons},$$

and for a coil of N turns,

$$F = 2BIlN \text{ Newtons}.$$

The force on each side acts at a radius r [see Figure 1-6(a)], producing a deflecting torque:

$$\begin{aligned} T_D &= 2BIlNr \text{ Newton meters (Nm)} \\ &= BIlN(2r) \end{aligned}$$

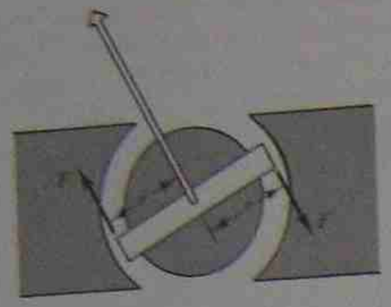
$$\boxed{T_D = BIlND \text{ Nm}} \qquad (1\text{-}1)$$

where D is the coil diameter. Since $l \times D$ is the area (A) enclosed by the coil [see Figure 1-6(b)], the torque equation can be rewritten as

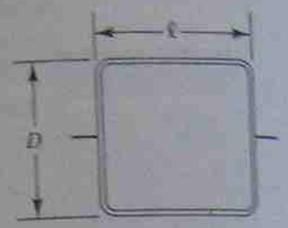
$$\boxed{T_D = BINA \text{ Nm}} \qquad (1\text{-}2)$$

Equation 1-2 shows that the torque is directly proportional to: the flux produced by the permanent magnet, the coil current, the number of coil turns, and the size of the coil. For a given instrument all quantities except the current are constant.

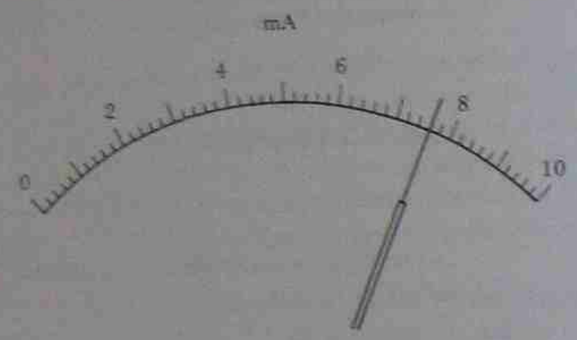
The controlling torque exerted by the spiral springs is directly proportional to the deformation or "wind-up" of the springs. Thus, the control-



(a) Force F acts on each side of the coil



(b) Area enclosed by coil is $D \times \ell$



(c) Linear scale on a PMMC instrument

FIGURE 1-6. Moving coil and scale of a PMMC instrument.

ling torque is proportional to the actual angle of deflection of the pointer.

$$T_C = K\theta^\circ$$

where K is a constant.

For a given deflection, the controlling and deflecting torques are equal:

$$T_C = T_D$$

or

$$K\theta^\circ = BINA.$$

Since all quantities except θ and I are constant for any given instrument, the deflection angle is

$$\boxed{\theta^\circ = CI} \tag{1-3}$$

where C is a constant.

Equation 1-3 shows that the pointer deflection is always proportional to the coil current. Consequently, the scale of the instrument is *linear*, or uniformly divided, i.e., if 1 mA produces a 1-cm movement of the pointer from zero, 2 mA produces a 2-cm movement, and so on [see Figure 1-6(c)].

EXAMPLE 1-1 A PMMC instrument with a 100-turn coil has a magnetic flux density in its air gaps of $B = 0.2T$. The coil dimensions are $D = 1$ cm and $l = 1.5$ cm. Calculate the torque on the coil for a current of 1 mA.

SOLUTION

Equation 1-1,

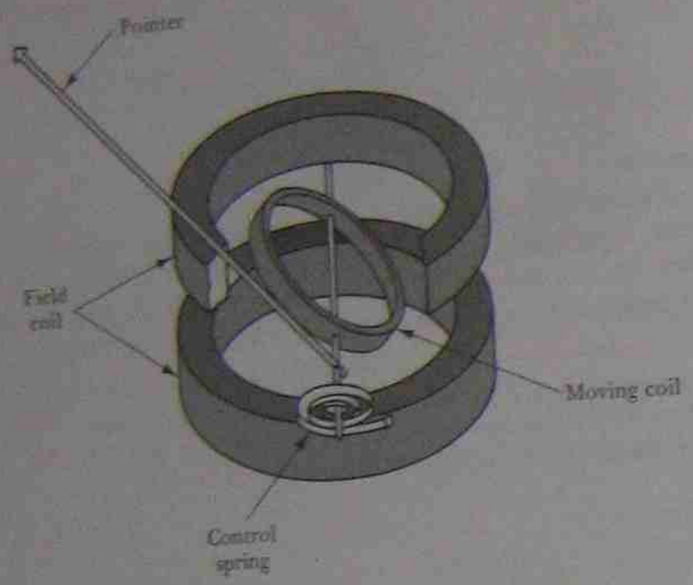
$$\begin{aligned} T_D &= BlIND \text{ Nm} \\ &= 0.2T \times 1.5 \times 10^{-2} \times 1 \text{ mA} \times 100 \times 1 \times 10^{-2} \\ &= 3 \times 10^{-6} \text{ Nm}. \end{aligned}$$

As will be seen in later chapters, the PMMC instrument can be used as a dc voltmeter, a dc ammeter, and an ohmmeter. When connected with rectifiers and transformers, it can also be employed to measure alternating voltage and current.

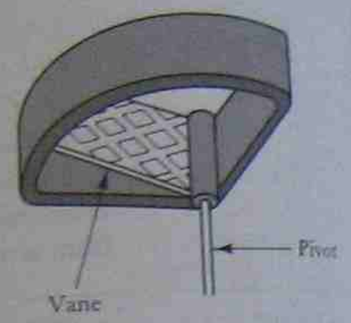
1-3 THE ELECTRODYNAMIC INSTRUMENT

The basic construction of an *electrodynamic* or *dynamometer* instrument is illustrated in Figure 1-7(a). When this is compared to the PMMC instrument in Figure 1-4, it is seen that the major difference is that two magnetic *field coils* are substituted in place of the permanent magnet. The magnetic field in which the moving coil is pivoted is generated by passing a current through the stationary field coils. When a current flows through the pivoted coil, the two fluxes interact (as in the PMMC instrument), causing the coil and pointer to be deflected. Spiral springs provide controlling force and connecting leads to the pivoted coil. Zero adjustment and moving system balance are also as in the PMMC instrument.

Another major difference from the PMMC instrument is that the electrodynamic instrument usually has air damping. A lightweight vane



(a) Coil arrangement



(b) Air damping system

FIGURE 1-7. Basic construction of an electrodynamic instrument.

pushes air around in an enclosure when the pivoted coil is in motion [see Figure 1-7(b)]. This damps out all rapid movements and oscillations of the moving system. As will be explained, electrodynamic instruments can be used on ac. The alternating current would induce unwanted eddy currents in a metallic coil former. Therefore, the damping method employed in a PMMC instrument would not be suitable for an electrodynamic instrument.

Normally, there is no iron core in an electrodynamic instrument, so the flux path is entirely an air path. Consequently, the field flux is much smaller than in a PMMC instrument. To produce a strong enough deflecting torque, the moving-coil current must be much larger than the small currents required in a PMMC instrument. Thus, the PMMC instrument is sensitive to lower current levels than the electrodynamic instrument.

Depending upon the application of the instrument, the field coil and moving-coil currents may be the same current or different currents. For example, the coils may be connected in series so that the same current flows through all three. Alternatively, they may be parallel connected. In this case, the moving-coil current is likely to be very much smaller than the current levels in each field coil. As in the case of the PMMC instrument, the deflecting torque of an electrodynamic instrument is dependent upon field flux, coil current, coil dimensions, and number of coil turns. However,

the field flux is directly proportional to the current through the field coils, and the moving-coil flux is directly proportional to the current through the moving coil. Consequently, the deflecting torque is proportional to the product of the two currents:

$$T_D \propto I_{\text{field coil}} I_{\text{moving coil}}.$$

When the same current flows through field coils and pivoted coil, the deflecting torque is proportional to the square of the current:

$$T_D \propto I^2.$$

This gives the deflection angle as

$$\boxed{\theta = CI^2} \tag{1-4}$$

where C is a constant.

The scale of the instrument is nonlinear because the deflection is proportional to I^2. Suppose the deflection is $\theta = 5^0$ for a current of 10 mA:

$$5^0 = C(10\text{ mA})^2$$

or

$$C = 5^0/(10\text{ mA})^2$$
$$= 5 \times 10^4.$$

When $I = 20$ mA:

$$\theta = C(20\text{ mA})^2$$
$$= 5 \times 10^4\,(20\text{ mA})^2$$
$$= 20^0.$$

It is seen that when the current is doubled, the deflection angle is increased by a factor of 4. This gives a scale which is cramped at the low (left-hand) end and spaced out at the high end.

The major disadvantages of an electrodynamic instrument compared to a PMMC instrument are the lower sensitivity and the nonlinear scale. A major advantage of the electrodynamic instrument is that it is not polarized; i.e., a positive deflection is obtained regardless of the direction of current in the coils. Thus the instrument can be used to measure ac or dc. This is further discussed in Section 2-5.

1-4 MOVING-IRON INSTRUMENTS

Moving-iron instruments are based on the principle that when two adjacent pieces of soft iron are magnetized by the current passing through a coil, *repulsion* occurs.

Figure 1-8(a) illustrates the *radial-vane* type of moving-iron instrument. Current passed through the surrounding coil magnetizes the two soft iron vanes. One vane is fixed and the other is pivoted. Both vanes are magnetized with the same polarity so that the two N poles are adjacent and the two S poles are adjacent. The resulting repulsion force causes the pivoted vane to rotate away from the fixed vane. The pointer attached to the spindle is deflected over the instrument scale when the pivoted vane rotates.

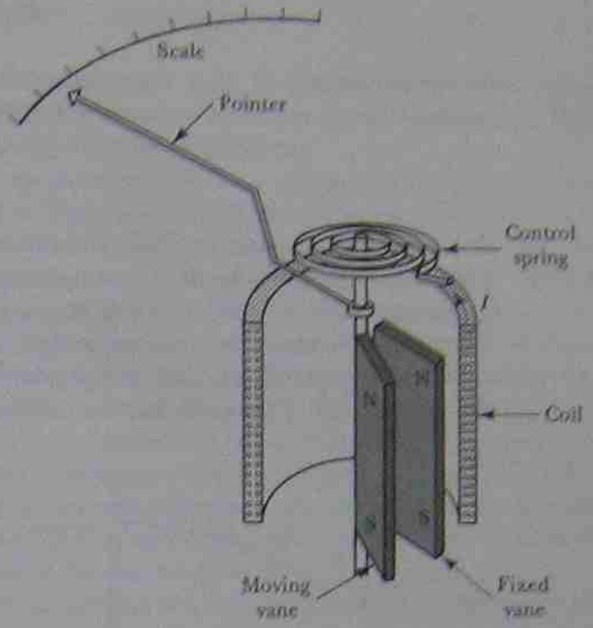
Coiled springs are used to produce the controlling force for this instrument, exactly as in the PMMC instrument. Eddy current damping is not possible in the moving-iron instrument. So the damping force is generated by a lightweight aluminum vane moving in an enclosed box, as is done in the electrodynamic instrument.

The deflecting torque in the moving-iron instrument is directly proportional to the magnetic flux in both of the two iron vanes. The flux in *each* vane is proportional to the current I that flows in the surrounding coil. Consequently, the deflecting torque is proportional to I^2.

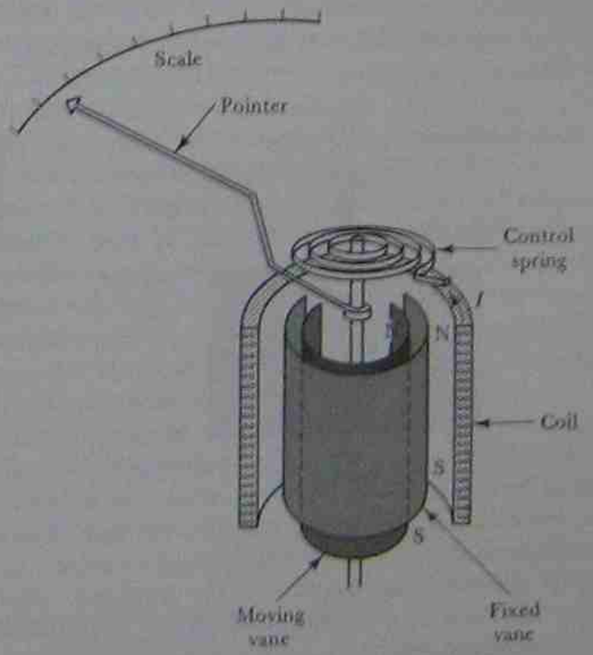
The fact that $T_D \propto I^2$ results in a scale which is cramped at the low end and spaced out at the upper end. Once again, this is similar to the scale of an electrodynamic instrument in which the same current flows in field coils and moving coil. Also, like the electrodynamic instrument, the moving-iron instrument can be used to indicate either dc or rms ac.

The illustration in Figure 1-8(b) is known as a *concentric-vane* type moving-iron instrument. The vanes are partially cylindrical, and the pivoted moving vane is situated within the fixed vane. When no coil current flows, the moving vane is at rest in its zero position where it is closest to the fixed vane. With coil current flowing in the direction shown, both vanes are magnetized so that N poles occur at the top and S poles at the bottom of each. Thus, there is a force of repulsion which causes the moving vane to rotate to a position where it is farther away from the fixed vane. As the coil current is increased, the repulsion force increases and greater rotation (and pointer movement) results. Both vanes may be rectangular (i.e., when flat). Alternatively, the fixed vane may be tapered to make the instrument scale more linear.

The deflection system of a moving-iron instrument absorbs more power than a similar PMMC instrument (i.e., it is not as sensitive). Also because of residual magnetism in the iron vanes, the moving-iron instrument is the least accurate of the two. *Hysteresis* is a further source of error when the instrument is used on ac. Some advantages are that moving-iron instruments are quite rugged and fairly inexpensive to manufacture



(a) Radial vane type



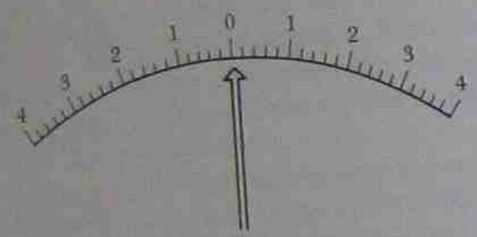
(b) Concentric vane type

FIGURE 1-8. Moving-iron instruments.

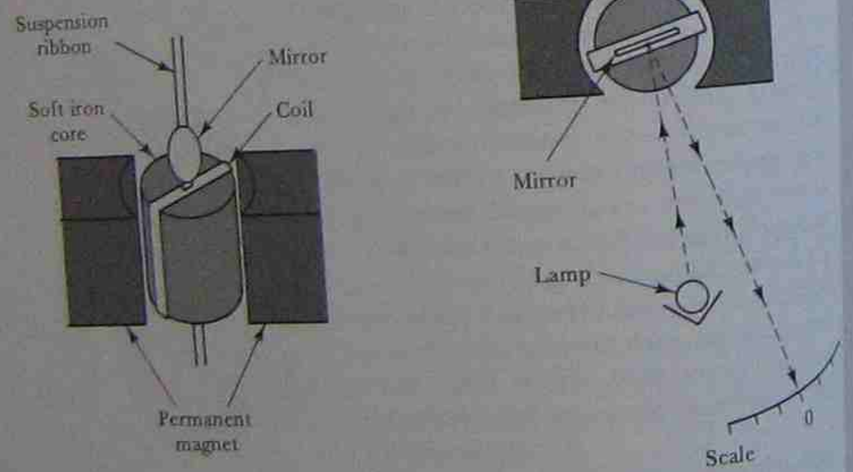
However, because of their lower sensitivity and accuracy, moving-iron instruments are not as widely used as PMMC instruments.

1-5 THE GALVANOMETER

A *galvanometer* is essentially a PMMC instrument designed to be sensitive to extremely low current levels. The simplest galvanometer is a very sensitive instrument with the type of center-zero scale illustrated in Figure 1-9(a). The deflection system is arranged so that the pointer can be deflected to either right or left of zero, depending upon the direction of current through the moving coil. The scale may be calibrated in microamps, or it may



(a) Center-zero scale



(b) Basic deflection system of a galvanometer using a light beam

FIGURE 1-9. Galvanometer center-zero scale and basic deflection system for a light-beam type galvanometer.

simply be a millimeter scale. In the latter case, the instrument *current sensitivity* (usually stated in μA/mm) is used to determine the current level that produces a measured deflection.

The torque equation for a galvanometer is exactly as discussed in Section 1-2. The torque is proportional to the number of coil turns, the coil dimensions, and the current flowing in the coil. The most sensitive moving-coil galvanometers use taut-band suspension, and the controlling torque is generated by the twist in the suspension ribbon. (Older, extremely sensitive laboratory type galvanometers have very lightweight coils delicately suspended on long phosphor bronze ribbons for minimum control torque.) Eddy current damping may be provided, as in other PMMC instruments, by winding the coil on a nonmagnetic conducting coil former. Sometimes a nonconducting coil former is employed, and the damping currents are generated solely by the moving coil. In this case, the coil is shunted by a *damping resistor* which controls the level of eddy currents generated by the coil movements.

With the moving-coil weight reduced to the lowest possible minimum for greatest sensitivity, the weight of the pointer can create a problem. This is solved in many instruments by mounting a small mirror on the moving coil instead of a pointer. The mirror reflects a beam of light on to a scale, as illustrated in Figure 1-9(b). The light beam behaves as a very long weightless pointer which can be substantially deflected by a very small coil current. This gives light-beam type galvanometers a much lower current sensitivity than pointer type instruments.

All galvanometers have a mechanical zero control which should be set with the instrument terminals short-circuited.

Because of their lightweight coils and delicate coil suspension, PMMC galvanometers must be carefully handled. Electronic galvanometers are also available (see Section 8-11). These use amplifiers which give the instrument a very high input impedance and a very low current sensitivity. The amplifier output is indicated by a simple center-zero PMMC deflection meter. An electronic galvanometer is much more rugged than any other type of galvanometer.

As already discussed, the *current sensitivity* defines the amount of current (in μA) flowing through the instrument for a given deflection (in mm). The *damping resistance* referred to earlier is usually connected in series with the galvanometer and the current source being measured. In this case the source resistance should normally be very much smaller than that of the damping resistance. Frequently, a *critical damping resistance* value is stated, which gives just sufficient damping to allow the pointer to settle down quickly with only a very small short-lived oscillation. The galvanometer *voltage sensitivity* is often expressed for a given value of critical damping resistance. This is usually stated in microvolts/millimeter. A *megohm sensitivity* is sometimes specified for galvanometers, and this is the value of

resistance that must be connected in series with the instrument to restrict the deflection to one scale division when a potential difference of 1 V is applied across its terminals.

Typical pointer type galvanometers have current sensitivities ranging from 0.1 to 1 μA/mm. For light-beam instruments typical current sensitivities are 0.01 to 0.1 μA per scale division. For electronic galvanometers, sensitivities of 10 $\mu\mu$A/division or 10 pA/division are possible.

EXAMPLE 1-2 A galvanometer has a current sensitivity of 1 μA/mm and a critical damping resistance of 1 kΩ. Calculate (a) the voltage sensitivity and (b) the megohm sensitivity.

SOLUTION

$$\text{Voltage sensitivity} = 1\ \text{k}\Omega \times 1\ \mu\text{A/mm}$$
$$= 1\ \text{mV/mm}.$$

For a voltage sensitivity of 1 V/mm,

$$\text{megohm sensitivity} = \frac{1\ \text{V/mm}}{1\ \mu\text{A/mm}} = 1\ \text{M}\Omega.$$

Galvanometers are usually used to detect zero current or voltage in a circuit, rather than to measure the actual level of current or voltage. In this situation, the instrument is referred to as a *null meter* or *null detector*. A galvanometer used as a null meter must be protected from the excessive current flow that might occur when the voltage across the instrument terminals is not close to zero. Protection is provided by an adjustable resistance connected in shunt with the instrument (see Figure 1-10). When the shunt resistance is zero, all of the circuit current flows through the shunt. As the shunt resistance is increased above zero, an increasing amount of current flows through the galvanometer. The necessary circuit adjustments are made, e.g., balancing of a Wheatstone bridge (see Section

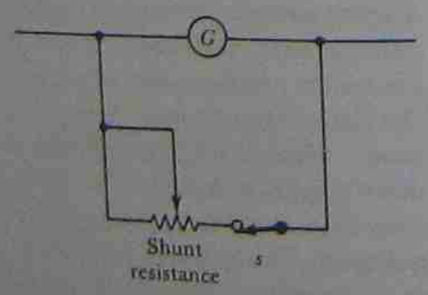


FIGURE 1-10. Galvanometer with adjustable shunt resistance for protection

6-3), to reduce the current towards zero as indicated by the galvanometer. The shunt resistance is further increased to allow more of the (unbalance) circuit current to flow through the galvanometer, and circuit adjustments are again made to reduce the current to zero. This process is repeated until the galvanometer indicates zero with the shunting resistance at infinity, i.e., switch S open.

1-6 ERRORS IN DEFLECTION INSTRUMENTS

Some sources of error in measurements made by deflection instruments are: bearing friction, improperly adjusted zero, and incorrect reading of the pointer indication. There are, of course, other error sources involving balance of the moving system, temperature effects on control springs, ageing of permanent magnets, inaccurately marked scale, etc., all of which involve the design and manufacture of the instrument.

1-6-1 Error Sources

Zero and friction errors can be minimized by carefully adjusting the mechanical zero of an instrument before use and by gently tapping the meter to relieve friction when zeroing and reading. Care in deciding the exact position of the pointer on the scale will reduce reading errors.

1-6-2 Parallax Error

Inexpensive instruments usually have printed scales which do not allow for any differences from one instrument to another. Good quality instruments have scales which are hand marked under test conditions. Even with an accurately marked scale and a sharp pointer, two observers may disagree about the exact scale reading. This occurs because of *parallax error*, the uncertainty about the eye of the observer being directly in line with the end of the pointer [see Figure 1-11(a)]. Parallax error is eliminated in good instruments by the use of a knife-edge pointer and a mirror alongside the scale [see Figure 1-11(b)]. When an observer lines up the pointer and the mirror image of the pointer, the observer's eye is exactly in line with the pointer, and the scale can be read accurately.

1-6-3 Frequency Effects

All deflection instruments use coils which have inductance. With increasing frequency, the impedance of the coil increases and thus reduces the current that would otherwise pass through the coil. As well as inductance, coils have capacitance between adjacent turns. The inductance and (distributed) capacitance can resonate at a particular frequency and introduce large errors in the measured quantity.

Of the three types of instruments discussed in preceding sections—PMMC, electrodynamic, and moving iron—the PMMC instrument has by far the best frequency response. A PMMC instrument cannot be used directly on ac but must be employed together with rectifiers. (This is explained in Section 2-3.) When correctly used, a typical PMMC instrument can operate satisfactorily up to frequencies of about 100 kHz.

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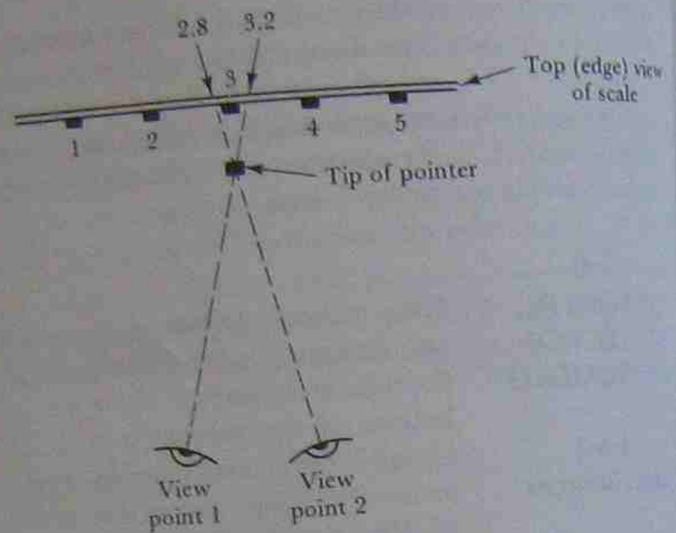
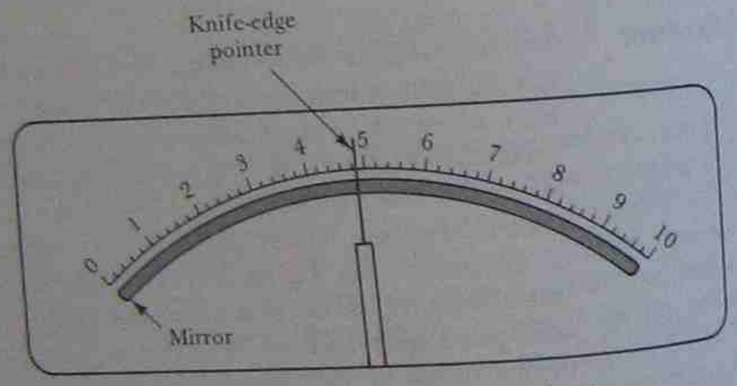


(a) Parallax error



(b) Use of a mirror and knife-edge pointer

FIGURE 1-11. Parallax error and its elimination.

Its low frequency limit is, of course, dc. But when used on very low frequency ac, its pointer follows the instantaneous value of the (rectified) waveform, and in this circumstance no measurement is obtainable. A low frequency limit for a PMMC instrument used on rectified ac is approximately 20 Hz.

The electrodynamic instrument has field coils which do not exist in a PMMC instrument. Thus, an electrodynamic instrument has much larger inductance and distributed winding capacitance than a PMMC instrument. The upper frequency limit for accurate measurements with an electrodynamic instrument is typically 500 Hz. Although this type of instrument is unpolarized and can be used directly to measure either ac

dc, at very low frequencies its pointer follows the changing instantaneous value of the alternating quantity. Its low frequency limit is typically around 20 Hz.

Moving-iron instruments have large coils which, like those of electrodynamic instruments, possess relatively large inductance values. Frequency-dependent iron losses (hysteresis and eddy current) also occur in moving-iron instruments. Most moving-iron instruments are designed for use at power frequencies, and their typical range of operation is from 20 to 125 Hz. With careful construction, some moving-iron instruments can be made to operate satisfactorily up to 2 kHz.

1-6-4 Specified Accuracy

High quality instruments with hand-calibrated scales usually have their accuracy specified as a percentage of the actual scale reading, or measured quantity. However, for a great many instruments, manufacturers specify the accuracy as a percentage of FSD. This means, for example, that an instrument which gives FSD for a coil current of 100 μA, and which is specified as accurate to $\pm 1\%$, has a ± 1-μA accuracy at *all points* on its scale. Thus, as demonstrated in Example 1-3, the measurement error becomes progressively greater for low scale readings.

EXAMPLE 1-3 An instrument which indicates 100 μA at FSD has a specified accuracy of $\pm 1\%$. Calculate the upper and lower limits of measured current and the percentage error in the measurement for (a) FSD, (b) 0.5 FSD, and (c) 0.1 FSD.

SOLUTION

a. At FSD:

$$\begin{aligned} \textit{indicated current} &= 100\ \mu\text{A} \\ \textit{error} &= \pm 1\% \text{ of } 100\ \mu\text{A} \\ &= \pm 1\ \mu\text{A}, \\ \textit{actual measured current} &= 100 \pm 1\ \mu\text{A} \\ &= 99 \text{ to } 101\ \mu\text{A}, \\ \textit{error} &= \pm 1\% \textit{ of measured current.} \end{aligned}$$

b. At 0.5 FSD:

$$\begin{aligned} \textit{indicated current} &= 0.5 \times 100\ \mu\text{A} \\ &= 50\ \mu\text{A}, \\ \textit{error} &= \pm 1\% \textit{ of FSD} \\ &= \pm 1\ \mu\text{A}, \\ \textit{actual measured current} &= 50\ \mu\text{A} \pm 1\ \mu\text{A} \\ &= 49\ \mu\text{A to } 51\ \mu\text{A}, \\ \textit{error} &= \frac{\pm 1\ \mu\text{A}}{50\ \mu\text{A}} \times 100\% \\ &= \pm 2\% \textit{ of measured current.} \end{aligned}$$

c. At 0.1 FSD:

$$\begin{aligned} \textit{indicated current} &= 0.1 \times 100\ \mu\text{A} \\ &= 10\ \mu\text{A}, \\ \textit{error} &= \pm\ 1\%\ \text{of FSD} \\ &= \pm\ 1\ \mu\text{A}, \\ \textit{actual measured current} &= 10\ \mu\text{A} \pm 1\ \mu\text{A} \\ &= 9\ \mu\text{A to } 11\ \mu\text{A} \\ \textit{error} &= \frac{\pm 1\ \mu\text{A}}{10\ \mu\text{A}} \times 100\% \\ &= \pm\ 10\%\ \text{of } \textit{measured current}. \end{aligned}$$

REVIEW QUESTIONS AND PROBLEMS

1-1. List the three forces involved in the moving system of a deflection instrument. Explain the function of each force, and give examples of how each force is produced. Illustrate your explanations with suitable sketches.

1-2. Describe jewelled-bearing suspension and taut-band suspension, as used in deflection instruments. Discuss the merits of each.

1-3. Draw a sketch to show the basic construction of a typical PMMC instrument. Identify each part in the sketch, and explain the operation of the instrument.

1-4. Sketch the construction of a core-magnet type of PMMC instrument. Briefly explain.

1-5. Develop the torque equation for a PMMC instrument, and show that its scale is linear.

1-6. List the performance characteristics of PMMC instruments.

1-7. A PMMC instrument with a 300-turn coil has a magnetic flux density of $B = 0.15\ T$ in its air gaps. The coil dimensions are: $D = 1.25$ cm and $l = 2$ cm. Calculate the torque when the coil current is 500 μA.

1-8. A PMMC instrument has a flux density of 0.12 T in its air gaps. The coil has $D = 1.5$ cm and $l = 2.25$ cm. Determine the number of coil turns required if the torque is to be 4.5×10^{-6} Nm when the coil is 100 μA.

1-9. Sketch the construction of an electrodynamic instrument. Identify each part of the sketch, and explain the operation of the instrument.

1-10. Discuss the torque equation and scale for an electrodynamic instrument. List the advantages and disadvantages of this type of instrument compared to a PMMC instrument.

1-11. Draw sketches to show the construction of two types of moving-iron instrument. Identify the various parts, and briefly explain how each instrument operates. State advantages and disadvantages of moving-iron instruments.

1-12. Sketch the basic construction of a light-beam type galvanometer. Briefly explain its operation.

1-13. Discuss one application of the galvanometer, and define: current sensitivity, critical damping resistance, voltage sensitivity, and megohm sensitivity.

1-14. A galvanometer has a current sensitivity of 500 nA/mm, and a critical damping resistance of 3 kΩ. Calculate its voltage sensitivity and its megohm sensitivity.

1-15. A galvanometer has a voltage sensitivity of 300 μV/mm and a megohm sensitivity of 1.5 MΩ. Determine the value of its critical damping resistance.

1-16. Determine the current sensitivity and the megohm sensitivity of a galvanometer that deflects by 5 cm when a current of 20 μA is passed through its coil.

1-17. Explain parallax error as it applies to a deflection instrument, and show how it can be eliminated. List other sources of error in deflection instrument measurements.

1-18. Explain the purpose and use of the mechanical zero control on a deflection instrument.

1-19. List the characteristics of polarized and nonpolarized instruments. Name one instrument of each type.

1-20. Define linear and nonlinear scales. At what point on a scale is the most accurate current measurement made?

1-21. Which of the major types of deflection instruments can operate satisfactorily on ac and dc without additional components? Which will normally operate only on dc? State the upper and lower limits of operating frequency for: PMMC, electrodynamic, and moving-iron instruments.

1-22. A PMMC instrument that indicates 250 μA at full-scale deflection has a specified accuracy of $\pm 2\%$. Calculate the measurement accuracy at currents of 200 μA and 100 μA.

1-23. A deflection instrument with FSD = 100 μA has a specified accuracy of $\pm 3\%$. Calculate the possible error when the instrument is indicating: (a) 50 μA, (b) 10 μA.

1-24. A current of 25 μA is measured on an instrument with FSD of 37.5 μA. If the 25 μA measurement is to be accurate to within $\pm 5\%$, calculate the required instrument accuracy.

2

DEFLECTION TYPE AMMETERS, VOLTMETERS, AND WATTMETERS

INTRODUCTION All deflection type instruments are essentially current meters. In the case of the ammeter, the current to be measured (or a portion of it) passes through the instrument and produces pointer deflection. A voltmeter is simply a very low current ammeter with a high resistance. The current that flows in a voltmeter is directly proportional to the applied voltage, and the instrument scale is calibrated to indicate voltage.

A PMMC instrument can be employed directly as a dc voltmeter or ammeter. When connected with rectifiers, it can be used as an ac voltmeter. Together with a current transformer and rectifiers, the PMMC instrument functions as an ac ammeter.

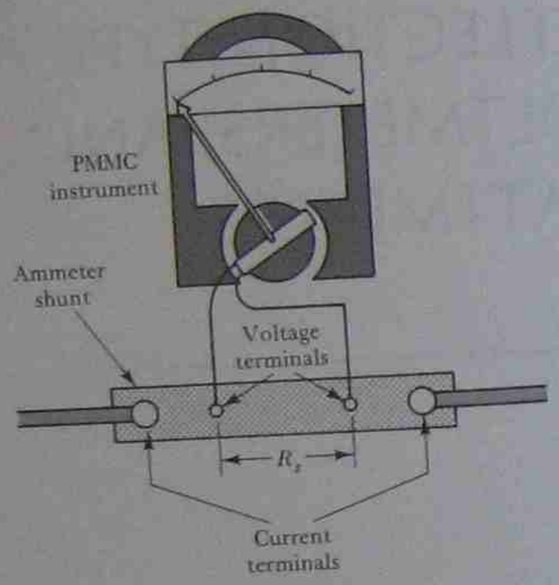
An electrodynamic instrument can be used on ac or dc, as an ammeter, a voltmeter, or a wattmeter. Its most important application is as a wattmeter. In this situation, the field coils pass the load current, and the moving coil carries a current proportional to the supply voltage.

In thermocouple instruments, thermocouples are used to generate a voltage proportional to the heating effect of a current. Thermocouple voltmeters, ammeters, and wattmeters can be constructed. They function on dc or ac and can operate satisfactorily to very high frequencies.

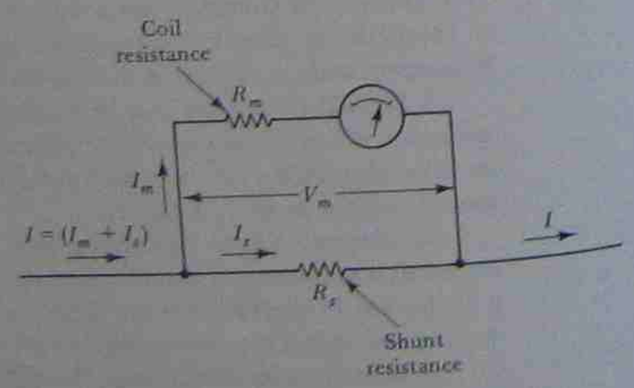
2-1 DC AMMETER

2-1-1 Operation

The PMMC instrument is an ammeter. Pointer deflection is directly proportional to the current flowing in the coil. However, maximum pointer deflection is produced by a very small current, and the coil is usually wound of thin wire that would be quickly destroyed by large currents. For larger currents, the instrument must be modified so that most of the



(a) Construction of dc ammeter



(b) Ammeter circuit

FIGURE 2-1. dc ammeter construction and circuit diagram.

current to be measured is shunted around the coil of the meter. Only a small portion of the current passes through the moving coil. Figure 2-1 illustrates how this is arranged.

A *shunt*, or very low resistance, is connected in parallel with the instrument coil [Figure 2-1(a)]. The shunt has two sets of terminals identified as *voltage terminals* and *current terminals*. This is to ensure that the resistance in parallel with the coil (R_s) is accurately defined and the contact resistance of the current terminals is removed from R_s. Contact resistance can vary with change in current level and thus introduce errors.

In the circuit diagram in Figure 2-1(b), r_m is the meter resistance (or coil circuit resistance) and R_s is the resistance of the shunt. Suppose the meter resistance is exactly 99 Ω and the shunt resistance is 1 Ω. The shunt current (I_s) will be ninety-nine times the meter current (I_m). In this situation, if the meter gives FSD for a coil current of 0.1 mA, the scale should be calibrated to read 100 × 0.1 mA or 10 mA at full scale. The relationship between shunt current and coil current is further investigated in Examples 2-1 and 2-2.

EXAMPLE 2-1 An ammeter (as in Figure 2-1) has a PMMC instrument with a coil resistance of $R_m = 99\ \Omega$ and FSD current of 0.1 mA. Shunt resistance $R_s = 1\ \Omega$. Determine the total current passing through the ammeter at (a) FSD, (b) 0.5 FSD, and (c) 0.25 FSD.

SOLUTION

a. At FSD:

$$\text{meter voltage } V_m = I_m R_m \qquad \text{[see Figure 2-1(b)]}$$
$$= 0.1\ \text{mA} \times 99\ \Omega$$
$$= 9.9\ \text{mV},$$

shunt voltage = meter voltage,

$$I_s R_s = V_m$$
$$I_s = \frac{V_m}{R_s} = \frac{9.9\ \text{mV}}{1\ \Omega} = 9.9\ \text{mA},$$

$$\text{total current } I = I_s + I_m$$
$$= 9.9\ \text{mA} + 0.1\ \text{mA} = 10\ \text{mA}.$$

b. *At 0.5 FSD:*

$$I_m = 0.5 \times 0.1 \text{ mA} = 0.05 \text{ mA},$$
$$V_m = I_m R_m = 0.05 \text{ mA} \times 99\ \Omega = 4.95 \text{ mV},$$
$$I_s = \frac{V_m}{R_s} = \frac{4.95 \text{ mV}}{1\ \Omega} = 4.95 \text{ mA},$$

total current $I = I_s + I_m$
$= 4.95 \text{ mA} + 0.05 \text{ mA} = 5 \text{ mA}.$

c. *At 0.25 FSD:*

$$I_m = 0.25 \times 0.1 \text{ mA} = 0.025 \text{ mA},$$
$$V_m = I_m R_m = 0.025 \text{ mA} \times 99\ \Omega$$
$$= 2.475 \text{ mV},$$
$$I_s = \frac{V_m}{R_s} = \frac{2.475 \text{ mV}}{1\ \Omega} = 2.475 \text{ mA},$$

total current $I = I_s + I_m$
$= 2.475 \text{ mA} + 0.025 \text{ mA} = 2.5 \text{ mA}.$

2-1-2 Scale

In Example 2-1 the total ammeter current is 10 mA when the moving-coil instrument indicates FSD. Therefore, the meter scale can be calibrated so

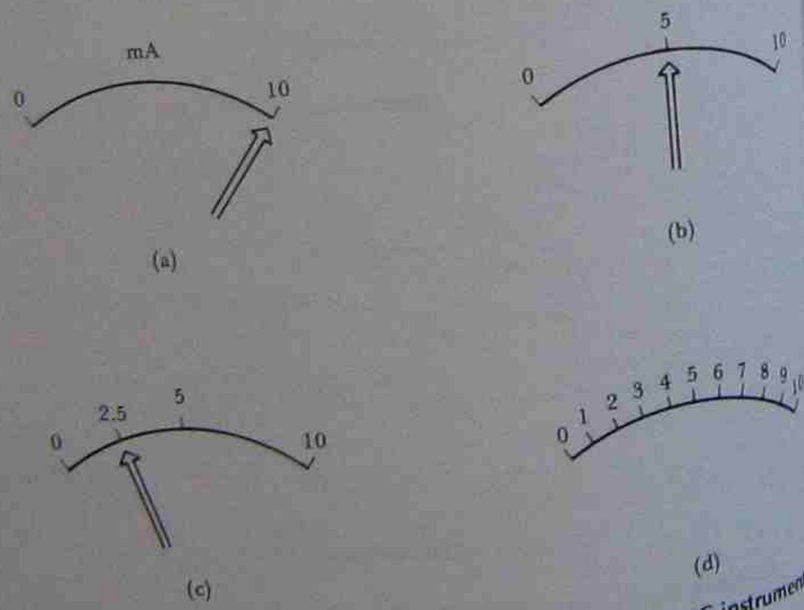


FIGURE 2-2. Linear scale of a dc ammeter using a PMMC instrument

that FSD represents 10 mA [see Figure 2-2(a)]. When the pointer indicates 0.5 FSD and 0.25 FSD, the total current levels are 5 mA and 2.5 mA, respectively [Figures 2-2(b) and (c)].

It is seen that the ammeter scale can be calibrated linearly to represent all current levels from 0 to 10 mA [Figure 2-2(d)].

2-1-3 Shunt Resistance

Refer again to Example 2-1. If a shunt having a smaller resistance is used, the shunt current and the total meter current will be larger than the levels calculated. In fact, shunt resistance values can be determined to convert a PMMC instrument into an ammeter for measuring virtually any desired level of current. Example 2-2 demonstrates how shunt resistances are calculated.

EXAMPLE 2-2 A PMMC instrument has a FSD of 100 μA and a coil resistance of 1 kΩ. Calculate the required shunt resistance value to convert the instrument into an ammeter: (a) with FSD = 100 mA and (b) with FSD = 1 A.

SOLUTION

a. *FSD = 100 mA:*

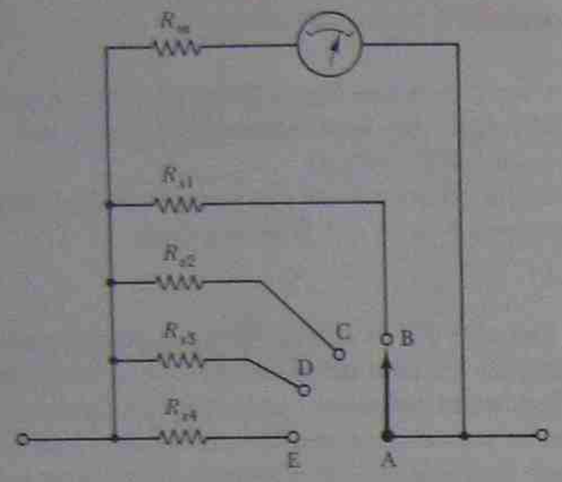
$$V_m = I_m R_m = 100\ \mu A \times 1\ \text{k}\Omega = 100 \text{ mV},$$
$$I = I_s + I_m,$$
$$I_s = I - I_m = 100 \text{ mA} - 100\ \mu\text{A} = 99.9 \text{ mA},$$
$$R_s = \frac{V_m}{I_s} = \frac{100 \text{ mV}}{99.9 \text{ mA}} = 1.001\ \Omega.$$

b. *FSD = 1 A:*

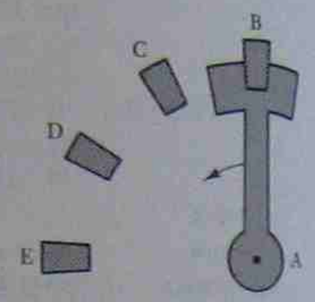
$$V_m = I_m R_m = 100 \text{ mV},$$
$$I_s = I - I_m = 1 \text{ A} - 100\ \mu\text{A} = 999.9 \text{ mA},$$
$$R_s = \frac{V_m}{I_s} = \frac{100 \text{ mV}}{999.9 \text{ mA}} = 0.10001\ \Omega.$$

2-1-4 Multirange Ammeters

The circuit of a multirange ammeter is shown in Figure 2-3(a). As illustrated, a rotary switch is employed to select any one of several shunts having different resistance values. A *make-before-break switch* [Figure 2-3(b)] must be used so that the instrument is not left without a shunt in parallel with it even for a brief instant. If this occurred, the high resistance of the instrument would affect the current flowing in the circuit. More im-

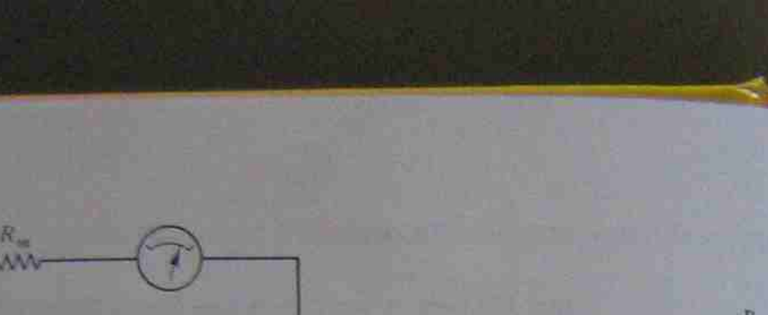


(a) Multirange ammeter using switched shunts

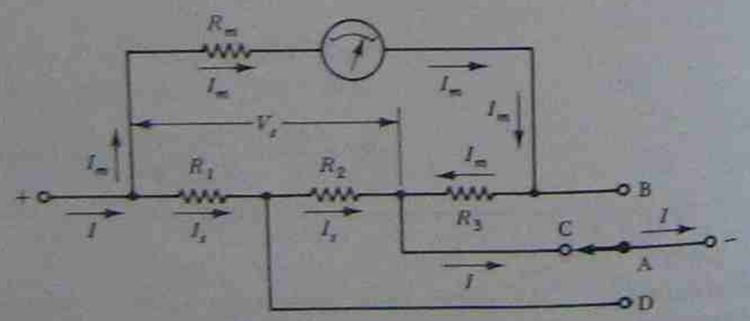


(b) Make-before-break switch

FIGURE 2-3. Multirange ammeter and range-changing switch.



(a) $(R_1 + R_2 + R_3)$ in parallel with R_m



(b) $(R_1 + R_2)$ in parallel with $(R_m + R_3)$

FIGURE 2-4. Multirange ammeter using an Ayrton shunt.

portantly, a current large enough to destroy the instrument might flow through its moving coil. When switching between shunts, the wide-ended moving contact of the make-before-break switch makes contact with the next terminal before it breaks contact with the previous terminal. Thus, during switching there are actually two shunts in parallel with the instrument.

Figure 2-4 shows another method of protecting the deflection instrument of an ammeter from excessive current flow when switching between shunts. Resistors R_1, R_2, and R_3 constitute an *Ayrton shunt*. In Figure 2-4(a) the switch is at contact B, and the total resistance in parallel with the instrument is $R_1 + R_2 + R_3$. The meter resistance remains R_m. When the switch is at contact C [Figure 2-4(b)], the resistance R_3 is in series with the meter, and $R_1 + R_2$ is in parallel with $R_m + R_3$. Similarly, with the switch at contact D, R_1 is in parallel with $R_m + R_2 + R_3$. Because the shunts are permanently connected, and the switch makes contact with the shunt junctions, the deflection instrument is never left without a parallel-connected shunt (or shunts). In Example 2-3 ammeter current ranges are calculated for each switch position on an Ayrton shunt.

EXAMPLE 2-3 A PMMC instrument has a three-resistor Ayrton shunt connected across it to make an ammeter, as in Figure 2-4. The resistance values are $R_1 = 0.05\ \Omega$, $R_2 = 0.45\ \Omega$, and $R_3 = 4.5\ \Omega$. The meter has $R_m = 1\ \text{k}\Omega$ and FSD = 50 μA. Calculate the three ranges of the ammeter.

SOLUTION

Refer to Figure 2-4

Switch at contact B:

$$V_s = I_m R_m = 50\ \mu\text{A} \times 1\ \text{k}\Omega = 50\ \text{mV},$$

$$I_s = \frac{V_s}{R_1 + R_2 + R_3}$$

$$= \frac{50\ \text{mV}}{0.05\ \Omega + 0.45\ \Omega + 4.5\ \Omega} = 10\ \text{mA},$$

$$I = I_m + I_s = 50\ \mu\text{A} + 10\ \text{mA}$$

$$= 10.05\ \text{mA}.$$

Ammeter range = 10 mA.

Switch at contact C:

$$V_s = I_m(R_m + R_3)$$
$$= 50\ \mu\text{A}(1\ \text{k}\Omega + 4.5\ \Omega)$$
$$= 50\ \text{mV},$$
$$I_s = \frac{V_s}{(R_1 + R_2)}$$
$$= \frac{50\ \text{mV}}{(0.05\ \Omega + 0.45\ \Omega)}$$
$$= 100\ \text{mA},$$
$$I = 50\ \mu\text{A} + 100\ \text{mA}$$
$$= 100.05\ \text{mA}.$$

Ammeter range = 100 mA.

Switch at contact D:

$$V_s = I_m(R_m + R_3 + R_2)$$
$$= 50\ \mu\text{A}(1\ \text{k}\Omega + 4.5\ \Omega + 0.45\ \Omega)$$
$$= 50\ \text{mV},$$
$$I_s = \frac{V_s}{R_1} = \frac{50\ \text{mV}}{0.05\ \Omega}$$
$$= 1\ \text{A},$$
$$I = 50\ \mu\text{A} + 1\ \text{A}$$
$$= 1.00005\ \text{A}.$$

Ammeter range = 1 A.

2-1-5 Temperature Error

The moving coil in a PMMC instrument is wound with thin copper wire, and its resistance can change significantly when its temperature changes. The heating effect of the coil current may be enough to produce a resistance change. Any such change in coil resistance will introduce an error in ammeter current measurements. To minimize the effect of coil resistance variation, a *swamping resistance* made of *manganin* or *constantan* is connected in series with the coil, as illustrated in Figure 2-5. Manganin and constantan have resistance temperature coefficients very close to zero. If

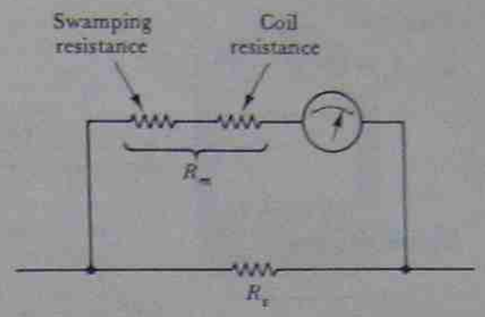


FIGURE 2-5. Use of a swamping resistance to minimize temperature errors in an ammeter.

the swamping resistance is nine times the coil resistance, then a 1% change in coil resistance would result in a total (swamping plus coil) resistance change of 0.1%.

The ammeter shunt must also be made of manganin or constantan to avoid shunt resistance variations with temperature. As noted in Figure 2-5, the swamping resistance must be considered part of the meter resistance r_m when calculating shunt resistance values.

2-1-6 Ammeter Resistance

An ammeter is always connected in series with a circuit in which current is to be measured. To avoid affecting the current level in the circuit, the ammeter must have a resistance much lower than the circuit resistance. Therefore, ammeter resistance is an important quantity. In Examples 2-2 and 2-3 the ammeter resistances are essentially the same as the total shunt resistance in parallel with the deflection instrument.

EXAMPLE 2-4 An ammeter is connected to measure the current in a 10-Ω load supplied from a 10-V source (see Figure 2-6). Calculate the circuit current if the ammeter resistance (R_a) is (a) 0.1 Ω or (b) 1 Ω. Also, in each case, calculate the effect of the ammeter on the current level.

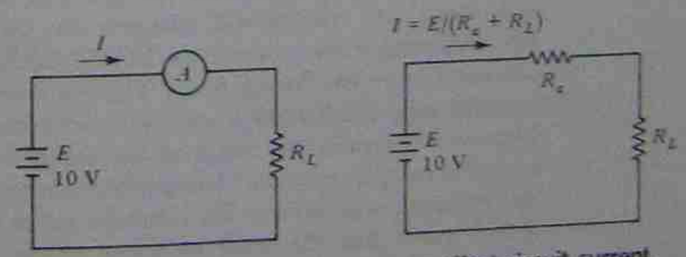


FIGURE 2-6. Ammeter resistance can affect circuit current.

SOLUTION

a. $R_a = 0.1\ \Omega$

$$I = \frac{E}{R_L + R_a} = \frac{10\text{ V}}{10\ \Omega + 0.1\ \Omega} \approx 0.99\text{ A}$$

Without the ammeter,

$$I = \frac{E}{R_L} = \frac{10\text{ V}}{10}$$

$$= 1\text{ A},$$

$$\textit{effect of ammeter} = \frac{(1\text{ A} - 0.99\text{ A})}{1\text{ A}}(100\%) = 1\%.$$

b. $R_a = 1\ \Omega$

$$I = \frac{E}{R_L + R_a} = \frac{10\text{ V}}{10\ \Omega + 1\ \Omega} \approx 0.909\text{ A},$$

$$\textit{effect of ammeter} = \frac{1\text{ A} - 0.909\text{ A}}{1\text{ A}}(100\%) = 9.1\%.$$

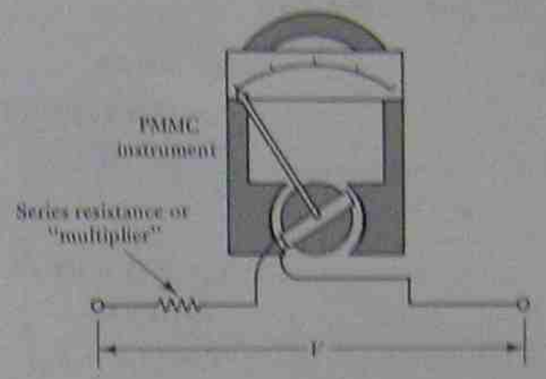
2-1-7 Using Ammeters

The procedure for using a multirange ammeter is exactly as listed in Section 3-5 for a multifunction instrument.

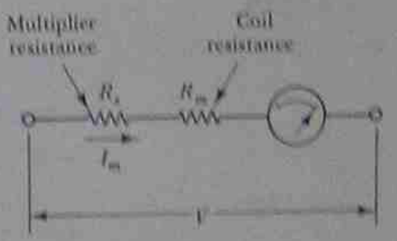
2-2 DC VOLTMETER

2-2-1 Operation

The deflection of a PMMC instrument is proportional to the current flowing through the moving coil. The coil current is directly proportional to the voltage across the coil. Therefore, the scale of the PMMC meter could be calibrated to indicate voltage. The coil resistance is normally quite small, and thus the coil voltage is also usually very small. Without any additional series resistance the PMMC instrument would only be able to measure very low voltage levels. The voltmeter range is easily increased by connecting a resistance in series with the instrument [see Figure 2-7(a)]. Because it increases the range of the voltmeter, the series resistance is termed a *multiplier resistance*. A multiplier resistance which is nine times the coil resistance will increase the voltmeter range by a factor of 10. Figure 2-7(b) shows that the total resistance of the voltmeter is (multiplier resistance) + (coil resistance).



(a) Construction of dc voltmeter



(b) Voltmeter circuit

FIGURE 2-7. dc voltmeter construction and circuit diagram.

EXAMPLE 2-5 A PMMC instrument with a FSD of 100 μA and a coil resistance of 1 kΩ is to be converted into a voltmeter. Determine the required multiplier resistance if the voltmeter is to measure 100 V at full scale. Also calculate the applied voltage when the instrument indicates 0.75, 0.5, and 0.25 of FSD.

SOLUTION

$$V = I_m(R_s + R_m) \qquad \text{[see Figure 2-7(b)]},$$

$$R_s + R_m = \frac{V}{I_m},$$

and

$$R_s = \frac{V}{I_m} - R_m$$

for V = 100 V FSD,

$$I_m = 100\ \mu A,$$
$$R_s = (100\ V/100\ \mu A) - 1\ k\Omega$$
$$= 999\ k\Omega.$$

At 0.75 FSD:

$$I_m = 0.75 \times 100\ \mu A$$
$$= 75\ \mu A,$$
$$V = I_m(R_s + R_m)$$
$$= 75\ \mu A(999\ k\Omega + 1\ k\Omega)$$
$$= 75\ V.$$

at 0.5 FSD:

$$I_m = 50\ \mu A,$$
$$V = 50\ \mu A(999\ k\Omega + 1\ k\Omega)$$
$$= 50\ V.$$

at 0.25 FSD:

$$I_m = 25\ \mu A,$$
$$V = 25\ \mu A(999\ k\Omega + 1\ k\Omega)$$
$$= 25\ V.$$

Example 2-5 demonstrates that the PMMC voltmeter has the linear scale shown in Figure 2-8.

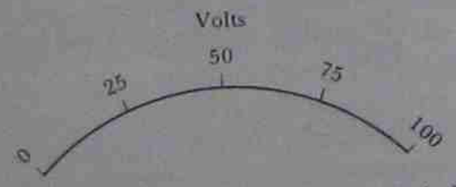
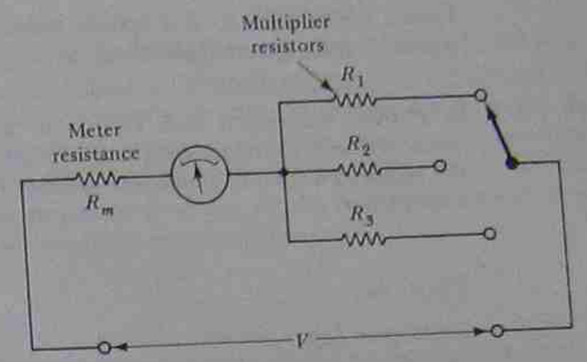


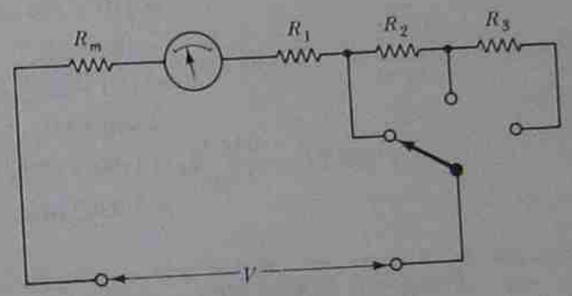
FIGURE 2-8. Voltmeter scale for Example 2-5.

2-2-2 Multirange Voltmeters

A multirange voltmeter consists of a deflection instrument, several multiplier resistors, and a rotary switch. Two possible circuits are illustrated in Figure 2-9. In Figure 2-9(a) only one of the three multiplier resistors is



(a) Multirange voltmeter using switched multiplier resistors



(b) Multirange voltmeter using series-connected multiplier resistors

FIGURE 2-9. Multirange voltmeter circuits.

connected in series with the meter at any time. The range of this voltmeter is

$$V = I_m(R_m + R)$$

where R can be R_1, R_2, or R_3.

In Figure 2-9(b) the multiplier resistors are connected in series, and each junction is connected to one of the switch terminals. The range of this voltmeter can also be calculated from the equation $V = I_m(R_m + R)$, where R can now be R_1, $R_1 + R_2$, or $R_1 + R_2 + R_3$.

Of the two circuits, the one in Figure 2-9(b) is the least expensive to construct. This is because (as shown in Example 2-6) all of the multiplier resistors in Figure 2-9(a) must be special (nonstandard) values, while in

Figure 2-9(b) only R_1 is a special resistor and all other multipliers are standard value (precise) resistors.

EXAMPLE 2-6 A PMMC instrument with FSD = 50 μA and R_m = 1700 Ω is to be employed as a voltmeter with ranges of 10 V, 50 V, and 100 V. Calculate the required values of multiplier resistors for the circuits of Figure 2-9(a) and (b).

SOLUTION

Circuit as in Figure 2-9(a):

$$R_m + R_1 = V/I_m,$$
$$R_1 = (V/I_m) - R_m$$
$$= (10\text{ V}/50\ \mu\text{A}) - 1700\ \Omega$$
$$= 198.3\ \text{k}\Omega,$$
$$R_2 = (50\text{ V}/50\ \mu\text{A}) - 1700\ \Omega$$
$$= 998.3\ \text{k}\Omega,$$
$$R_3 = (100\text{ V}/50\ \mu\text{A}) - 1700\ \Omega$$
$$= 1.9983\ \text{M}\Omega.$$

Circuit as in Figure 2-9(b):

$$R_m + R_1 = V_1/I_m,$$
$$R_1 = (V_1/I_m) - R_m$$
$$= (10\text{ V}/50\ \mu\text{A}) - 1700\ \Omega$$
$$= 198.3\ \text{k}\Omega,$$
$$R_m + R_1 + R_2 = V_2/I_m,$$
$$R_2 = (V_2/I_m) - R_1 - R_m$$
$$= \frac{50\text{ V}}{50\ \mu\text{A}} - 198.3\ \text{k}\Omega - 1700\ \Omega$$
$$= 800\ \text{k}\Omega,$$
$$R_m + R_1 + R_2 + R_3 = V_3/I_m$$
$$R_3 = (V_3/I_m) - R_2 - R_1 - R_m$$
$$= \frac{100\text{ V}}{50\ \mu\text{A}} - 800\ \text{k}\Omega - 198.3\ \text{k}\Omega - 1700\ \Omega$$
$$= 1\ \text{M}\Omega.$$

2-2-3 Temperature Error

As in the case of the PMMC ammeter, the change in coil resistance with temperature change can introduce an error into a voltmeter. The solution to the problem is exactly the same as that for the ammeter. A swamping resistance made of manganin or constantan must be connected in series with the coil. However, in the voltmeter the multiplier performs the swamping resistance function, so the multiplier resistor is simply constructed of manganin or constantan.

2-2-4 Voltmeter Sensitivity

The voltmeter designed in Example 2-5 has a total resistance of:

$$R_v = R_s + R_m = 1\ \text{M}\Omega.$$

Since the instrument measures 100 V at full scale, its *resistance per volt* is:

$$\frac{1\ \text{M}\Omega}{100\text{ V}} = 10\ \text{k}\Omega/\text{V}.$$

This quantity is also termed the *sensitivity* of the voltmeter. The sensitivity of a voltmeter is always specified by the manufacturer, and it is frequently printed on the scale of the instrument. If the sensitivity is known, the total voltmeter resistance is easily calculated. If the full-scale meter current is known, the sensitivity can be determined as the reciprocal of full-scale current. In Example 2-6, the PMMC meter gives FSD for 50 μA:

$$\text{sensitivity} = \frac{1}{50\ \mu\text{A}} = 20\ \text{k}\Omega/\text{V}.$$

Ideally, a voltmeter should have an extremely high resistance. A voltmeter is always connected across, or in parallel with, the points in a circuit at which the voltage is to be measured. If its resistance is too low, it can alter the circuit voltage. This is known as *voltmeter loading effect*.

EXAMPLE 2-7 A voltmeter on a 5-V range is connected to measure the voltage across R_2 in the circuit shown in Figure 2-10. Calculate V_{R2} (a) without the voltmeter connected, (b) with a voltmeter having a sensitivity of 20 kΩ/V, and (c) with a voltmeter having a sensitivity of 200 kΩ/V.

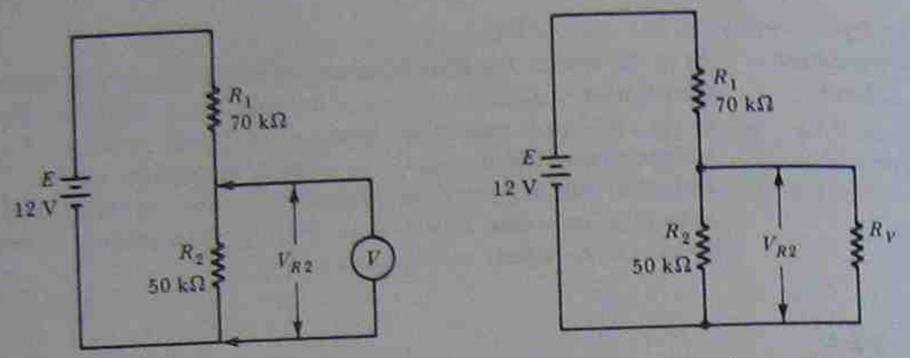


FIGURE 2-10. Voltmeter loading effect can alter the voltage within a circuit.

SOLUTION

a. Without the voltmeter:

$$V_{R2} = E\frac{R_2}{R_1 + R_2}$$

$$= 12\text{ V} \times \frac{50\text{ k}\Omega}{70\text{ k}\Omega + 50\text{ k}\Omega}$$

$$= 5\text{ V}.$$

b. With 20 kΩ/V voltmeter:

$$\text{voltmeter resistance } R_v = 5\text{ V} \times 20\text{ k}\Omega/\text{V}$$

$$= 100\text{ k}\Omega,$$

$$R_v \| R_2 = 100\text{ k}\Omega \| 50\text{ k}\Omega$$

$$= 33.3\text{ k}\Omega,$$

$$V_{R2} = E\frac{R_v \| R_2}{R_1 + R_v \| R_2}$$

$$= 12\text{ V} \times \frac{33.3\text{ k}\Omega}{70\text{ k}\Omega + 33.3\text{ k}\Omega}$$

$$= 3.87\text{ V}.$$

c. With a 200 kΩ/V voltmeter:

$$R_v = 5\text{ V} \times 200\text{ k}\Omega/\text{V}$$

$$= 1\text{ M}\Omega,$$

$$R_v \| R_2 = 1\text{ M}\Omega \| 50\text{ k}\Omega$$

$$= 47.62\text{ k}\Omega,$$

$$V_{R2} = 12\text{ V} \times \frac{47.62\text{ k}\Omega}{70\text{ k}\Omega + 47.62\text{ k}\Omega}$$

$$= 4.86\text{ V}.$$

2-2-5 Using Voltmeters

The procedure for using a multirange voltmeter is exactly as listed in Section 3-6 for a multifunction instrument.

2-3 RECTIFIER VOLTMETERS

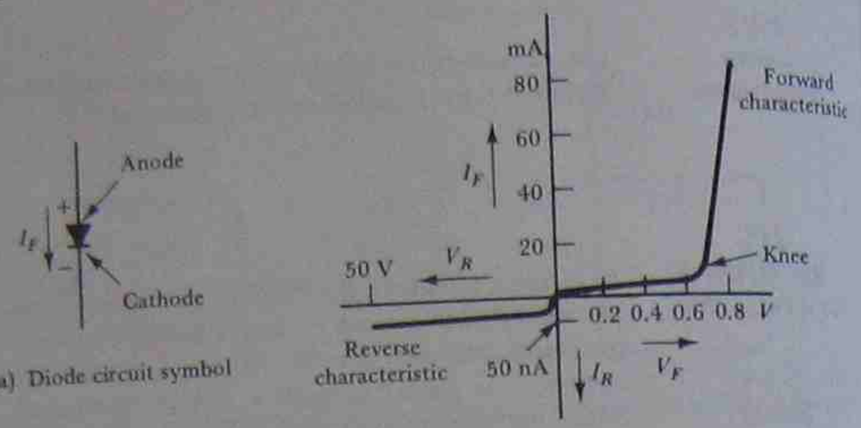
2-3-1 PMMC Instrument on ac

As already discussed, the PMMC instrument is *polarized*, i.e., its terminals are identified as + and −, and it must be correctly connected for positive (on-scale) deflection to occur. When an alternating current with a very low frequency is passed through a PMMC instrument, the pointer tends to follow the instantaneous level of the ac. As the current grows positively, the pointer deflection increases to a maximum at the peak of the ac. Then as the instantaneous current level falls, the pointer deflection decreases towards zero. When the ac goes negative, the pointer is deflected (off-scale) to the left of zero. This kind of pointer movement can occur only with ac having a frequency of perhaps 0.1 Hz or lower. With the normal 60-Hz supply frequencies, or higher frequencies, the damping mechanism of the instrument and the inertia of the meter movement prevents the pointer from following the changing instantaneous levels. Instead, the instrument pointer settles at the average value of the current flowing through the moving coil. The average value of purely sinusoidal ac is zero. Therefore, a PMMC instrument directly connected to measure 60-Hz ac indicates zero.

It is important to note that, although a PMMC instrument connected to an ac supply may be indicating zero, there can actually be a very large rms current flowing in its coils. In fact, sufficient current to destroy the instrument might easily flow while its pointer indicates zero.

2-3-2 Rectification

Rectifier instruments use silicon or germanium diodes to convert alternating current to a series of unidirectional current pulses, which produce positive deflection when passed through a PMMC instrument. Figure 2-11(a) shows the diode circuit symbol as an arrowhead and a bar. The arrowhead points in the direction of (conventional) current flow when the device is forward biased, i.e., from + to −. When correctly forward biased, a silicon diode typically has a forward volt drop (V_F) of 0.7 V, while a germanium diode has approximately 0.3 V. As illustrated in Figure 2-11(b), V_F increases slightly with increase in I_F, and if I_F falls to a very low level (below the knee of the characteristic) there can be a substantial drop in V_F. Usually, the device is assumed to have a constant forward volt drop when conducting. When reverse biased, the *reverse leakage current* that flows through the device is usually extremely small compared to the diode forward current.

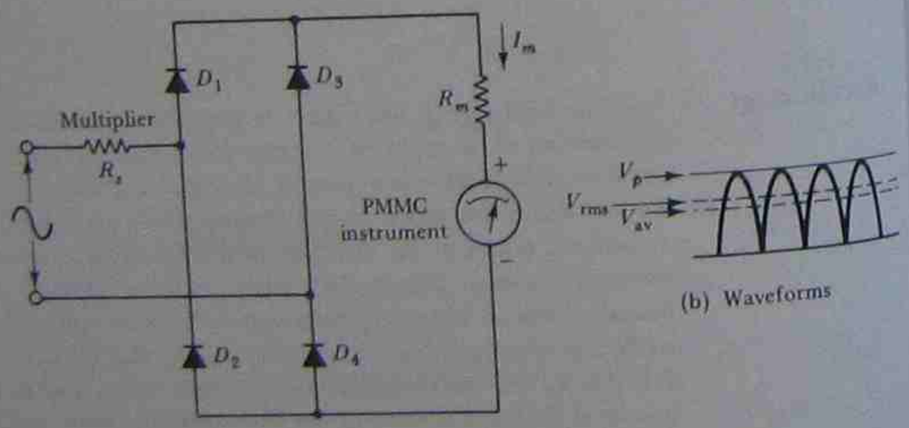


(a) Diode circuit symbol

(b) Characteristics of typical low current silicon diode

FIGURE 2-11. Diode circuit symbol and characteristics.

The full-wave bridge rectifier circuit in Figure 2-12(a) passes the positive half cycles of the sinusoidal input waveform and inverts the negative half cycles. When the input is positive, diodes D_1 and D_4 conduct, causing current to flow through the meter from top to bottom, as shown. When the input goes negative, D_2 and D_3 conduct, and current again flows through the meter from the positive terminal to the negative terminal. The resulting output is a series of positive half-cycles without any intervening spaces [see Figure 2-12(b)].



(a) Circuit

(b) Waveforms

FIGURE 2-12. ac voltmeter using a bridge rectifier and a PMMC instrument.

2-3-3 Full-wave Rectifier Voltmeter

As in the case of a dc voltmeter, the rectifier voltmeter circuit in Figure 2-12(a) uses a series-connected multiplier resistor to limit the current flow through the PMMC instrument. The actual current that flows in the instrument has the waveform illustrated in Figure 2-12(b). The meter deflection is proportional to the average current, which is 0.637 × peak current. But the actual current (or voltage) to be indicated in ac measurements is normally the rms quantity, which is 0.707 of the peak value, or 1.11 times the average value. Since there are direct relationships between rms, peak, and average values, the meter scale can be calibrated to indicate rms volts.

It must be noted that the above relationships between average, peak, and rms values apply only to pure sinusoidal waveforms. For nonsinusoidal waves, there are different factors relating the quantities.

EXAMPLE 2-8 A PMMC instrument with FSD = 100 μA and $R_m = 1$ kΩ is to be employed as an ac voltmeter with FSD = 100 V (rms). Silicon diodes are used in the bridge rectifier circuit of Figure 2-12. Calculate the multiplier resistance value required.

SOLUTION

At FSD, the average current flowing through the PMMC instrument is

$$I_{av} = 100\ \mu\text{A},$$

$$\textit{peak current } I_m = \frac{I_{av}}{0.637} = \frac{100\ \mu\text{A}}{0.637} \simeq 157\ \mu\text{A},$$

$$I_m = \frac{\text{(applied peak voltage)} - \text{(rectifier volt drop)}}{\text{total circuit resistance}},$$

$$\textit{rectifier volt drops} = 2V_F \text{ (for } D_1 \text{ and } D_4 \text{ or } D_2 \text{ and } D_3),$$

$$\textit{applied peak voltage} = 1.414V_{rms},$$

$$\textit{total circuit resistance} = R_s + R_m,$$

$$I_m = \frac{1.414V_{rms} - 2V_F}{R_s + R_m},$$

or

$$R_s = \frac{1.414V_{rms} - 2V_F}{I_m} - R_m$$

$$= \frac{(1.414 \times 100\ \text{V}) - (2 \times 0.7\ \text{V})}{157\ \mu\text{A}} - 1\ \text{k}\Omega$$

$$= 890.7\ \text{k}\Omega.$$

EXAMPLE 2-9 Calculate the pointer indications for the voltmeter in Example 2-8, when the rms input voltage is (a) 75 V and (b) 50 V.

SOLUTION

a. 75 V

$$I_{av} = 0.637I_m = 0.637\left(\frac{1.414V_{rms} - 2V_F}{R_s + R_m}\right)$$

$$= 0.637\left[\frac{(1.414 \times 75\ \text{V}) - (2 \times 0.7\ \text{V})}{890.7\ \text{k}\Omega + 1\ \text{k}\Omega}\right]$$

$$= 75\ \mu\text{A} = \tfrac{3}{4}\ \text{FSD},$$

b. 50 V

$$I_{av} = 0.637\left[\frac{(1.414 \times 50\ \text{V}) - (2 \times 0.7\ \text{V})}{890.7\ \text{k}\Omega + 1\ \text{k}\Omega}\right]$$

$$= 50\ \mu\text{A} = \tfrac{1}{2}\ \text{FSD}.$$

EXAMPLE 2-10 Calculate the sensitivity of the voltmeter in Example 2-8.

SOLUTION

$$I_m = 157\ \mu\text{A},$$

$$I_{rms} = 0.707I_m = 0.707 \times 157\ \mu\text{A}$$

$$\simeq 111\ \mu\text{A (at FSD)},$$

$$V_{rms} = 100\ \text{V (at FSD)},$$

$$\text{total } R = \frac{100\ \text{V}}{111\ \mu\text{A}} = 900.9\ \text{k}\Omega,$$

$$\text{sensitivity} = \frac{900.9\ \text{k}\Omega}{100\ \text{V}}\ \Omega/\text{V}$$

$$= 9.009\ \text{k}\Omega/\text{V}$$

$$\simeq 9\ \text{k}\Omega/\text{V}.$$

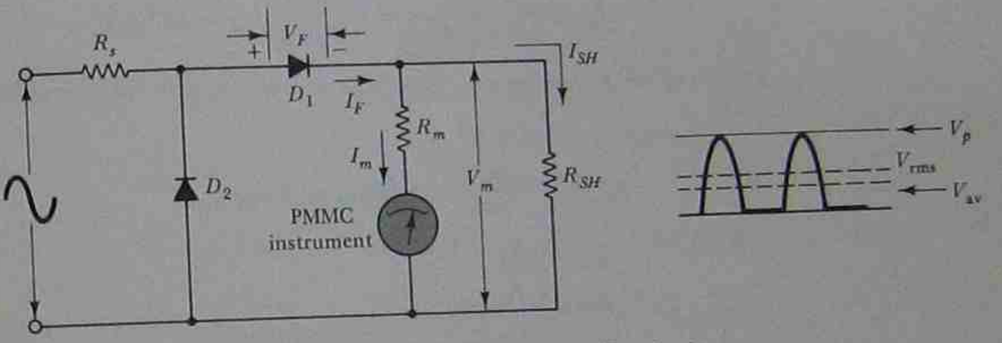
Examples 2-8 and 2-9 demonstrate that the rectifier instrument designed to indicate 100 V rms at full scale, also indicates $\frac{3}{4}$ FSD when 75 V rms is applied, and $\frac{1}{2}$ FSD when 50 V rms is applied. The instrument has a linear scale. At low levels of input voltage, the forward voltage drop across the rectifiers can introduce errors.

A rectifier voltmeter as designed above is for use only on pure sine wave voltages. When other than pure sine waves are applied, the voltmeter will *not* indicate the rms voltage.

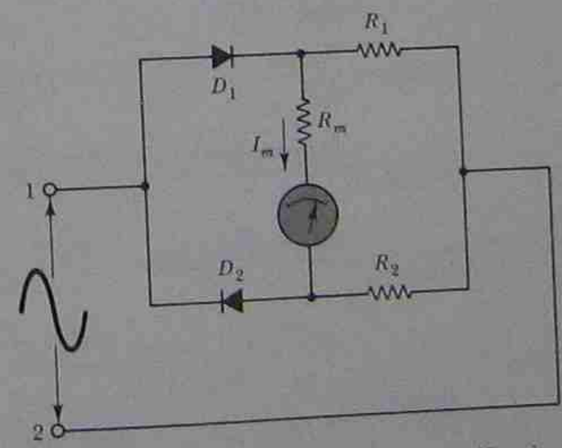
2-3-4 Half-wave Rectifier Voltmeter

Half-wave rectification is employed in the ac voltmeter circuit shown in Figure 2-13(a). R_{SH} shunting the meter is included to cause a relatively large current to flow through diode D_1 (larger than the meter current) when the diode is forward biased. This is to ensure that the diode is biased beyond the knee and well into the linear range of its characteristics [see Figure 2-11(b)]. Diode D_2 conducts during the negative half cycles of the input. When conducting, D_2 causes a very small voltage drop (V_F) across D_1 and the meter, thus preventing the flow of any significant reverse leakage current through the meter via D_1.

The waveform of voltage developed across the meter and R_{SH} is a series of positive half cycles with intervening spaces [Figure 2-13(a)]. In



(a) Voltmeter using half-wave rectifier circuit



(b) Voltmeter using half-bridge full-wave rectifier circuit

FIGURE 2-13. ac voltmeter circuits using half-wave rectification and half-bridge, full-wave rectification.

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half-wave rectification, $I_{av} = \frac{1}{2}(0.637\ I_m)$. This must be taken into account in the circuit design calculations.

EXAMPLE 2-11 A PMMC instrument with FSD = 50 μA and R_m = 1200 Ω is used in the half-wave rectifier voltmeter circuit illustrated in Figure 2-13(a). The silicon diode (D_1) must have a minimum forward current of 100 μA when the measured voltage is 20% of FSD. The voltmeter is to indicate 50 V rms at full scale. Calculate the values of R_s and R_{SH}.

SOLUTION

At FSD, $I_{av} = 50\ \mu A$.

Meter peak current,

$$I_m = \frac{I_{av}}{0.5 \times 0.637} = \frac{50\ \mu A}{0.5 \times 0.637} = 157\ \mu A.$$

At 20% of FSD, *diode current* I_F *must be at least 100* μA; *therefore at 100% of* FSD,

$$I_{F(peak)} = \frac{100\%}{20\%} \times 100\ \mu A = 500\ \mu A,$$

$$I_{F(peak)} = I_m + I_{SH},$$

$$I_{SH(peak)} = I_{F(peak)} - I_m$$

$$= 500\ \mu A - 157\ \mu A = 343\ \mu A,$$

$$V_{m(peak)} = I_m R_m = 157\ \mu A \times 1200\ \Omega$$

$$= 266.9\ mV,$$

$$R_{SH} = \frac{V_{m(peak)}}{I_{SH(peak)}} = \frac{266.9\ mV}{343\ \mu A} = 778\ \Omega,$$

$$I_{F(peak)} = \frac{\text{(applied peak voltage)} - V_{m(peak)} - V_F}{R_s},$$

$$I_{F(peak)} = \frac{1.414 V_{rms} - V_{m(peak)} - V_F}{R_s},$$

$$R_s = \frac{1.414 V_{rms} - V_{m(peak)} - V_F}{I_{F(peak)}}$$

$$= \frac{(1.414 \times 50\ V) - 266.9\ mV - 0.7\ V}{500\ \mu A}$$

$$= 139.5\ k\Omega.$$

EXAMPLE 2-12 Calculate the sensitivity of the voltmeter in Example 2-11 (a) when D_2 is included in the circuit [see Figure 2-13(a)] and (b) when D_2 is omitted from the circuit.

SOLUTION

a. *D_2 in circuit*

Peak input current during positive half cycle:

$$I_{F(peak)} = 500\ \mu A.$$

Peak input current during negative half cycle:

$$I_{(peak)} = \frac{1.14 V_{rms}}{R_s} = \frac{1.414 \times 50\ V}{139.5\ k\Omega}$$

$$= 500\ \mu A,$$

$$I_{rms} = 0.707 \times 500\ \mu A$$

$$= 353.5\ \mu A,$$

$$\text{total } R = \frac{50\ V}{353.5\ \mu A} = 141.4\ k\Omega,$$

$$\text{sensitivity} = \frac{141.4\ k\Omega}{50\ V} = 2.8\ k\Omega/V.$$

b. *without D_2*

Peak input current during positive half cycle:

$$I_{F(peak)} = 500\ \mu A.$$

During negative half cycle:

$$I = 0,$$

$$I_{rms} = 0.5\ I_{F(peak)} \quad \text{(for half-wave rectified)}$$

$$= 0.5 \times 500\ \mu A$$

$$= 250\ \mu A,$$

$$\text{total } R = \frac{50\ V}{250\ \mu A} = 200\ k\Omega,$$

$$\text{sensitivity} = \frac{200\ k\Omega}{50\ V} = 4\ k\Omega/V.$$

2-3-5 Half-bridge Full-wave Rectifier Voltmeter

The circuit in Figure 2-13(b) is that of an ac voltmeter employing a *half-bridge full-wave rectifier* circuit. The *half-bridge* name is applied because two diodes and two resistors are employed, instead of the four diodes used in a full-wave bridge rectifier. This circuit passes full-wave rectified current through the meter, but as in the circuit of Figure 2-13(a), some of the current bypasses the meter.

During the positive half cycle of the input, diode D_1 is forward biased and D_2 is reverse biased. Current flows from terminal 1 through D_1 and the meter (positive to negative), and then through R_2 to terminal 2. But R_1 is in parallel with the meter and R_2, which are connected in series. Therefore, much of the current flowing in D_1 passes through R_1, while only part of it flows through the meter and R_2. During the negative half cycle of the input, D_2 is forward biased and D_1 is reverse biased. Current now flows from terminal 2 through R_1 and the meter, and through D_2 to terminal 1. Now, R_2 is in parallel with the series-connected meter and R_1. Once again, much of the diode current bypasses the meter by flowing through R_2. This arrangement forces the diodes to operate beyond the knee of their characteristics and helps to compensate for differences that might occur in the characteristics of D_1 and D_2.

2-4 RECTIFIER AMMETERS

Like a dc ammeter, an ac ammeter must have a very low resistance because it is always connected in series with the circuit in which current is to be measured. This low resistance requirement means that the voltage drop across the ammeter must be very small, typically not greater than 100 mV. However, the voltage drop across a diode is 0.3 to 0.7 V depending upon whether the diode is made from germanium or silicon. When a bridge rectifier circuit is employed the total diode volt drop is 0.6 to 1.4 V. Clearly, a rectifier instrument is not suitable for direct application as an ac ammeter.

The use of a *current transformer* (Figure 2-14) gives the ammeter a low terminal resistance and low voltage drop. The transformer also steps up the input voltage (more secondary turns than primary turns) to provide sufficient voltage to operate the rectifiers, and at the same time it steps down the primary current to a level suitable for measurement by a PMMC meter. Since the transformer is used in an ammeter circuit, the current transformation ratio $I_p/I_s = N_s/N_p$ is very important.

A precise load resistor (R_L in Figure 2-14) is connected across the secondary winding of the transformer. This is selected to take the portion of secondary current not required by the meter. For example, suppose the PMMC instrument requires 100 μA (average) for FSD, and the current transformer has $N_s = 2000$ and $N_p = 5$. If the rms primary current is 100

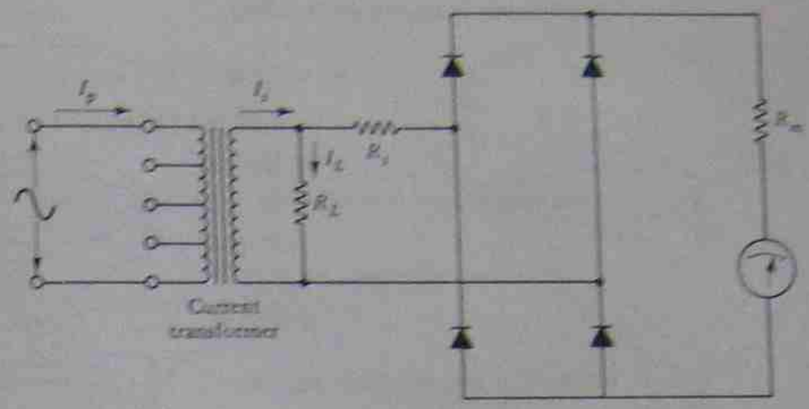


FIGURE 2-14. Rectifier ammeter circuit.

mA, then the secondary rms current is:

$$I_s = \frac{5}{2000} \times 100 \text{ mA} = 250 \text{ μA}$$

or an average of

$$I_{s(av)} = \frac{1}{1.11} \times 250 \text{ μA} = 225.2 \text{ μA}.$$

Since the meter requires 100 μA for FSD, the value of R_L is calculated to pass the remaining 125.2 μA.

The range of the instrument can be changed by switching-in different values of load resistance. Another method of range changing involves the use of additional terminals (or taps) on the primary winding to alter the number of primary turns. Additional transformer primary terminals are shown in Figure 2-14.

EXAMPLE 2-13 A rectifier ammeter with the circuit shown in Figure 2-14 is to give FSD for a primary current of 250 mA. The PMMC meter has FSD = 1 mA and $R_m = 1700$ Ω. The current transformer has $N_s = 500$ and $N_p = 4$. The diodes each have $V_F = 0.7$ V, and the series resistance is $R_s = 20$ kΩ. Calculate the required value of R_L.

SOLUTION

$$\textit{peak meter current } I_m = \frac{I_{av}}{0.637} = \frac{1 \text{ mA}}{0.637}$$
$$= 1.57 \text{ mA},$$

[illegible] peak voltage,

$$E_m = I_m(R_i + R_m) + IR_p$$
$$= 1.37\ \text{mA}\ (20\ \text{k}\Omega + 1700\ \Omega) + 1.8\ \text{V}$$
$$= 35.5\ \text{V},$$

or [illegible] voltage $E_s = (0.707 \times 35.5\ \text{V})\ \text{rms}$

$$= 25.1\ \text{V},$$

and [illegible] current $= 1.11 I_m$

$$= 1.11\ \text{mA}.$$

[illegible] the secondary current,

$$I_s = I_p \frac{E_p}{E_s}$$

$$= 200\ \text{mA} \times \frac{1}{100} = 2\ \text{mA},$$

and I_s = meter current + load current,

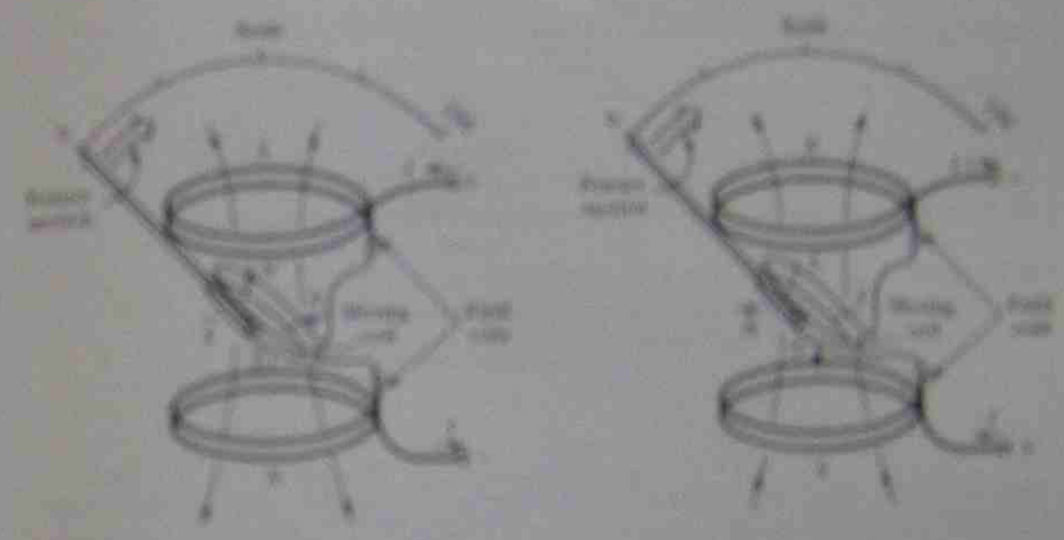
$$2\ \text{mA} = 1.11\ \text{mA} + I_L,$$
$$I_L = 2\ \text{mA} - 1.11\ \text{mA} = 0.89\ \text{mA},$$
$$R_L = \frac{E_s}{I_L} = \frac{25.1\ \text{V}}{0.89\ \text{mA}}$$
$$= 28.2\ \text{k}\Omega$$

2-5 ELECTRODYNAMIC VOLTMETER AND AMMETER

2-5-1 Electrodynamic instrument on ac

Consider Figure 2-15 in which the fixed and moving coils of an electrodynamic instrument are shown connected in series. In Figure 2-15(a) the current direction is such that the flux of the field coils are up 2 poles at the top, and N poles at the bottom of each coil. The moving-coil flux produces an N pole at the right-hand side of the coil, and an S pole at the left-hand side. The N pole of the moving coil is adjacent to the N pole of the upper field coil, and the S pole of the moving coil is adjacent to the S pole of the lower field coil. Since like poles repel, the moving coil rotates to a clockwise direction, causing the pointer to turn to the right from its zero position on the scale.

Now consider what occurs when the current through all three coils is reversed. Figure 2-15(b) shows that the reversed current causes the field coils to set up N poles at the top and S poles at the bottom of each coil.



(a) Current flowing from top to bottom produces pointer

(b) Current flowing from bottom to top also produces pointer deflection

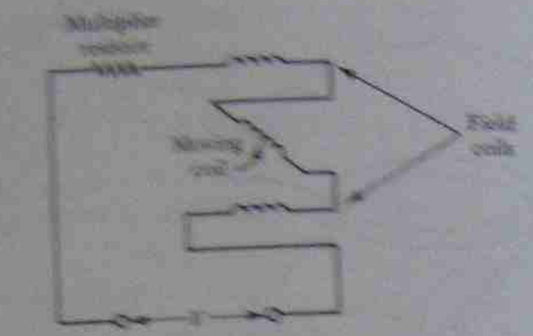
FIGURE 2-15. An electrodynamic instrument has a positive deflection for current flowing in either direction.

The moving-coil flux is also reversed so that it has an S pole at the right-hand side and an N pole at the left. Once again similar poles are adjacent, and repulsion produces clockwise rotation of the coil and pointer.

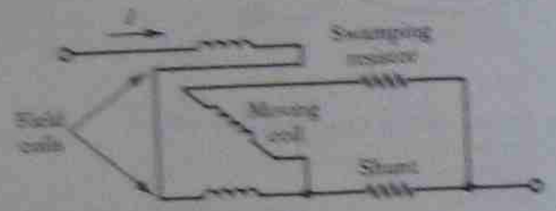
It is seen that the electrodynamic instrument has a positive deflection, no matter what the direction of current through the meter. Consequently, the terminals are not marked + and −, i.e., the instrument is not polarized.

As explained in Section 2-6, the electrodynamic instrument deflection is proportional to I^2 (i.e., when the same current flows in the moving coil and field coils). When used on ac, the deflection arises due to a position proportional to the average value of I^2. Thus, the deflection is proportional to the mean-squared value of the current. Since the scale of the meter is calibrated to indicate I, rather than I^2, the meter indicates (mean-squared current)$^{1/2}$, or the rms value. The rms value has the same effect as a numerically equivalent dc value. Therefore, the scale of the instrument can be read as either dc or rms ac. This is the characteristic of a simple instrument, which can be calibrated on dc and then used to measure ac.

Because the resistance of the coils increases rapidly with increasing frequency, electrodynamic instruments are useful only at low frequencies. Electrodynamic instruments, in particular, perform very satisfactorily at domestic and industrial power frequencies.



(a) Electrodynamic voltmeter



(b) Electrodynamic ammeter

FIGURE 2-16. Electrodynamic voltmeter and ammeter circuits.

2-5-2 Electrodynamic Voltmeter

Figure 2-16(a) shows the usual circuit arrangement for an electrodynami voltmeter. Since a voltmeter must have a high resistance, all three coils ar connected in series, and a multiplier resistor (made of manganin o constantan) is included. When the total resistance of the coils, and th required current for FSD are known, the multiplier resistance is calculate exactly as for dc voltmeters. The instrument scale can be read either as d voltage or rms ac voltage. Since it is more convenient to calibrate a instrument on dc than on ac, the electrodynamic voltmeter can be calibrate on dc, and then used either on dc or ac.

Because electrodynamic instruments usually require at least 100 mA for FSD, an electrodynamic voltmeter has a much lower sensitivity than a PMMC voltmeter. At 100-mA FSD, the sensitivity is 1/100 mA = 1 Ω/V. For a 100-V instrument, this sensitivity gives a total resistance of only 1 kΩ. Therefore, an electrodynamic voltmeter is not suitable fo measuring voltages in electronic circuits because of the loading effect.

2-5-3 Electrodynamic Ammeter

In an electrodynamic ammeter, the moving coil and its series-connecte swamping resistance are connected in parallel with the ammeter shun This is illustrated in Figure 2-16(b). The two field coils should be co

nected in series with the parallel arrangement of shunt and moving coil, as shown.

Because the field coils are always passing the actual current to be measured, resistance changes in the coils with temperature variations have no effect on the instrument performance. However, as in PMMC ammeters, the moving coil must have a manganin or constantan swamping resistance connected in series. Also, the shunt resistor must be made of manganin.

The scale of the electrodynamic ammeter can be read either as dc levels or rms ac values. Like the electrodynamic voltmeter, this instrument can be calibrated on dc and then used to measure either dc or ac.

2-6 ELECTRO-DYNAMIC WATTMETER

For both dc and ac applications, the most important use of the electrodynamic instrument is as a wattmeter. The coil connections for power measurement are illustrated in Figure 2-17(a). The field coils are connected in series with the load in which power is to be measured so that the load current flows through them. The moving coil and a multiplier resistor are connected in parallel with the load. Thus, the field coils carry the load current, and the moving-coil current is proportional to the load voltage. Since the instrument deflection is proportional to the product of the two currents, deflection = $C \times (EI)$, where C is a constant, or meter indication = EI watts.

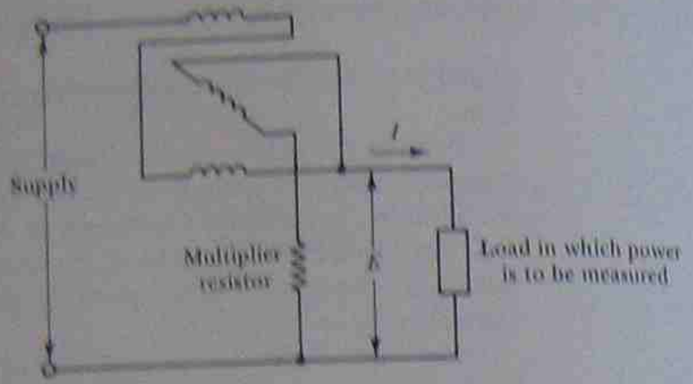
2-6-1 Wattmeter operation

In Figure 2-17(b) the electrodynamic wattmeter is shown in a slightly less complicated form than in Figure 2-17(a). A single-coil symbol is used to represent the two series-connected field coils.

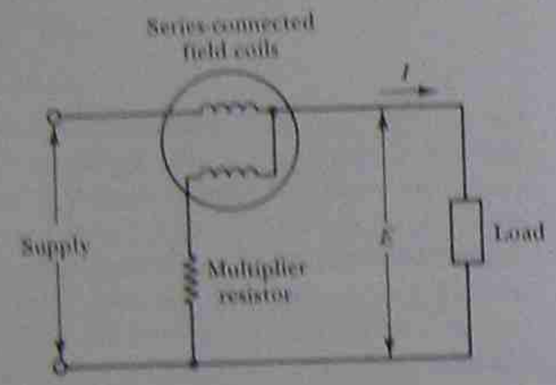
Suppose the instrument is correctly connected and giving a positive deflection. If the supply voltage polarity were reversed, the fluxes would reverse in both the field coils and the moving coil. As already explained in Section 2-5, the instrument would still have a positive deflection. In ac circuits where the supply polarity is reversing continuously, the electrodynamic wattmeter gives a positive indication proportional to $E_{rms}I_{rms}$. Like electrodynamic ammeters and voltmeters, the wattmeter can be calibrated on dc and then used to measure power in either dc or ac circuits.

In ac circuits the load current may lead or lag the load voltage by a phase angle ϕ. The wattmeter deflection is proportional to the in-phase components of the current and voltage. As shown in Figure 2-17(c), the instrument deflection is proportional to $EI\cos\phi$. Since the true power dissipated in a load with an ac supply is $EI\cos\phi$, the electrodynamic wattmeter measures true power.

To avoid errors due to changes in the resistance of the moving coil with temperature variations, the multiplier resistor employed in the voltage circuit of a wattmeter must be made of manganin, as in the case of a



(a) Electrodynamic wattmeter circuit



(b) Another way to show the wattmeter circuit



(c) Wattmeter measures $EI \cos \phi$

FIGURE 2-17. Electrodynamic wattmeter circuits and phasor diagram.

voltmeter. Resistance changes in the field coils normally have no effect on the instrument, unless shunts are used in parallel with the coils. When no shunts are used, all of the load current flows through the field coils regardless of the coil resistances.

2-6-2 Compensated Wattmeter

An important source of error in the wattmeter is illustrated in Figure 2-18(a) and (b). Figure 2-18(a) shows that if the moving coil (or voltage coil) circuit is connected in parallel with the load, the field coils pass a current ($I + I_v$), the sum of the load current and the moving-coil current. This results in the wattmeter indicating the load power (EI), plus a small additional quantity (EI_v). Where the load current is very much larger than I_v, this error may be negligible. In low load current situations, the error may be quite significant.

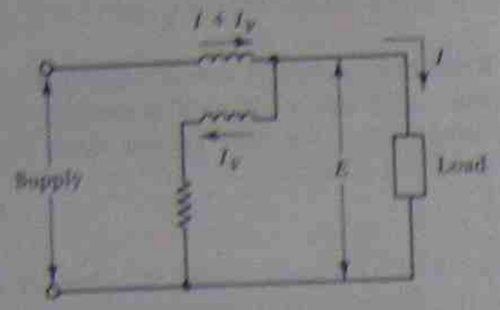
In Figure 2-18(b) the voltage coil is connected to the supply side of the field coils so that only the load current flows through the field coils. However, the voltage applied to the series-connected moving coil and multiplier is $E + E_F$ (the load voltage plus the voltage drop across the field coils). Now the wattmeter indicates load power (EI) plus an additional quantity ($E_F I$). In high voltage circuits, where the load voltage is very much larger than the voltage drop across the field coils, the error may be insignificant. In low voltage conditions, this error may be serious.

The *compensated wattmeter* illustrated in Figure 2-18(c) eliminates the errors described above. Since the field coils carry the load current, they must be wound of thick copper wire. In the compensated wattmeter, an additional thin conductor is wound right alongside every turn on the field coils. This additional coil, shown broken in Figure 2-17(c), becomes part of the voltage coil circuit. The voltage coil circuit is seen to be connected directly across the load, so that the moving-coil current is always proportional to load voltage. The current through the field coils in $I + I_v$, so that a field coil flux is set up proportional to $I + I_v$. But the additional winding on the field coils carries the moving-coil current I_v, and this sets up a flux in opposition to the main flux of the field coils. The resulting flux in the field coils is $\propto [(I + I_v) - I_v] \propto I$.

Thus the additional winding cancels the field flux due to I_v, and the wattmeter deflection is now directly proportional to EI.

2-6-3 Multirange Wattmeter

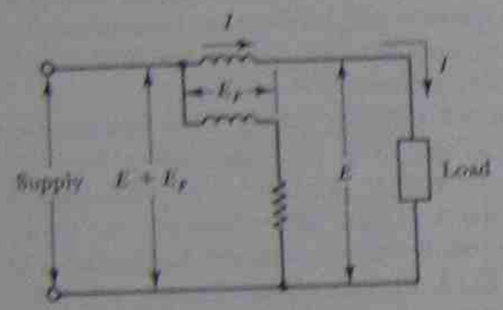
The range of voltages which may be applied to the moving-coil circuit of a wattmeter can be changed by switching different values of multiplier resistors into or out of the circuit, exactly as in the case of a voltmeter. Current range changes can be most easily effected by switching the two field coils from series connection to parallel connection. Figure 2-19 illustrates the circuitry, controls, and scale for a typical multirange wattmeter.



Deflection $\alpha\ E(I + I_V)$

$\alpha\ EI + \underbrace{EI_V}_{\text{Error}}$

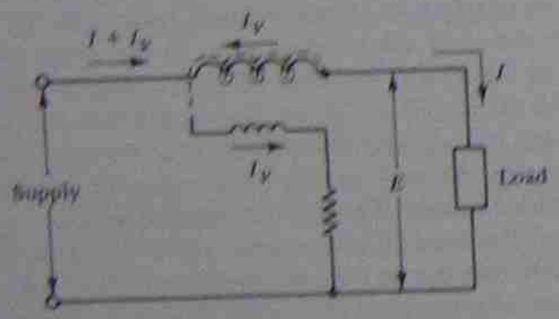
(a) Error due to moving-coil current



Deflection $\alpha\ (E + E_F)I$

$\alpha\ EI + \underbrace{E_F I}_{\text{Error}}$

(b) Error due to field coils voltage drop

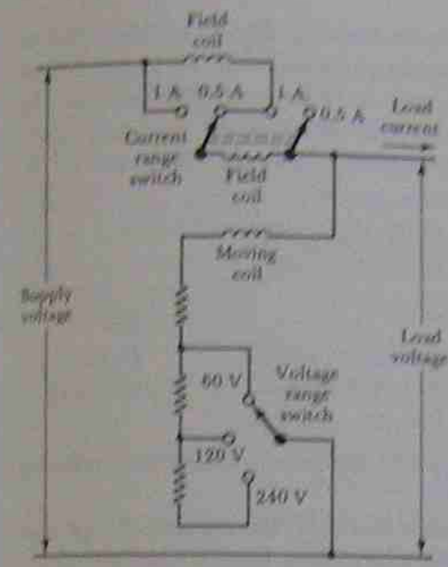


Deflection $\alpha\ E(I + I_V - I_V)$

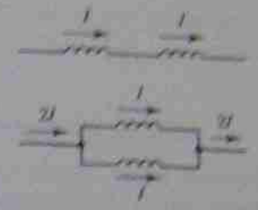
$\alpha\ EI$

(c) Compensated wattmeter using an additional coil wound alongside the field coils

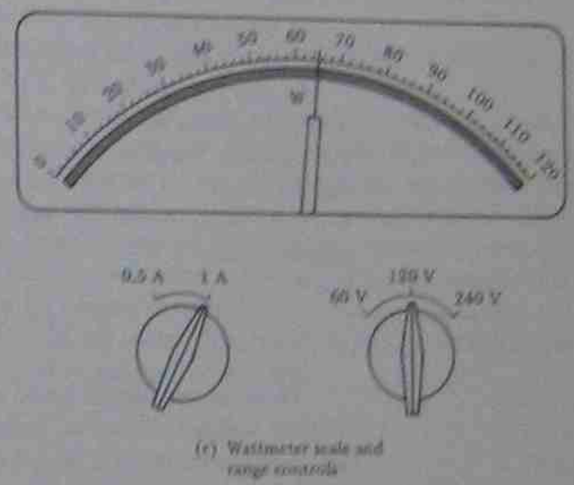
FIGURE 2-18. Wattmeter error sources and the compensated wattmeter.



(a) Circuit of multirange wattmeter



(b) Series-connected and parallel-connected field coils



(c) Wattmeter scale and range controls

FIGURE 2-19. Multirange wattmeter.

In the circuit shown in Figure 2-19(a), the series-connected multiplier resistors give three possible voltage range selections: 60 V, 120 V, and 240 V. The current range switch connects the field coils in series when set to the right, and in parallel when switched left. Figure 2-19(b) shows that if the coils can pass a maximum load current of 0.5 A when connected in series, then when parallel connected the load current can be 1 A. Note that this current (1 A) gives the same deflection as a current of 0.5 A when the field coils were series connected (assuming a constant voltage applied to the moving-coil circuit). However, if the load current is doubled and the load voltage remains constant, then the load power is doubled and the instrument scale reading must be multiplied by a factor of 2.

The wattmeter scale and controls illustrated in Figure 2-19(c) relate to the circuitry in Figure 2-19(a). With the range switches set at 0.5 A and 240 V, the instrument scale reads directly in watts, and FSD indicates 120 W. Similarly, with the 1-A and 120-V ranges selected, the scale may again be read directly in watts. When the range selections are 120 V and 0.5 A,

$$\text{FSD} = 120\ \text{V} \times 0.5\ \text{A} = 60\ \text{W},$$

Also, for a range selection of 1 A and 60 V,

$$\text{FSD} = 60\ \text{V} \times 1\ \text{A} = 60\ \text{W},$$

and for the switch at 0.5 A and 60 V, maximum deflection indicates $0.5\ \text{A} \times 60\ \text{V} = 30\ \text{W}$.

It is seen that to read the wattmeter correctly, the selected voltage and current ranges must be multiplied together to find the FSD power.

In using a wattmeter it is possible to obtain a reasonable on-scale deflection, while actually overloading either the current or voltage coils. For example, suppose the wattmeter voltage range is set to 60 V and the current range to 1 A. The instrument will have FSD = 60 V × 1 A = 60 W. Now suppose that the actual load current is 0.5 A, and the actual supply voltage is 120 V. The indicated power is

$$P = 120\ \text{V} \times 0.5\ \text{A} = 60\ \text{W}.$$

Thus the instrument would indicate 60 W at full scale, and there is no obvious problem. However, because the voltage circuit has 120 V applied to it, while set at a 60-V range, the moving coil is actually passing twice as much current as it is designed to take. This could cause overheating which may destroy the insulation on the moving coil.

A similar situation could occur with the current coils being overloaded although the wattmeter pointer is indicating on-scale. To avoid such overloads, it is important to know the approximate levels of load voltage and current and to set the instrument ranges accordingly.

The wattmeter scale illustrated in Figure 2-19(c) is linear, although as already explained, electrodynamic voltmeter and ammeter scales are nonlinear. In the case of the voltmeter, the same current I flows through both the moving coil and field coils so that the instrument deflection is proportional to I^2. With the ammeter, I flows through the field coils, and a portion of I flows in the moving coil. Thus the instrument deflection is again proportional to I^2, and the scale is nonlinear.

With the electrodynamic wattmeter, the moving coil and field coils are supplied independently. Usually, a load in which power is to be measured

has a constant level of supply voltage. When the load current changes, the supply voltage does not change. In this situation, the moving coil carries a constant current proportional to the supply voltage. The instrument deflection is now directly proportional to the load current, and the scale can be calibrated linearly.

Electrodynamic wattmeters are useful for measurement on supply frequencies up to a maximum of 500 Hz. Thus, they are not suitable for high-frequency power measurements.

2-6-4 Using Wattmeters

Before connecting a wattmeter into a circuit, check the mechanical zero of the instrument and adjust it if necessary. While zeroing, tap the instrument gently to relieve bearing friction.

The current circuit of a wattmeter must be connected in series with the load in which power is to be measured. The voltage circuit must be connected in parallel with the load.

If the pointer deflects to the left of zero, either the current terminals or voltage terminals must be reversed.

Before connecting a multirange wattmeter into a circuit, select a voltage range equal to or higher than the supply voltage. Select the highest current range. Then, switch down to the current range which gives the greatest on-scale deflection. Do not adjust the voltage range below the level of the supply voltage. This step ensures that the (low current) voltage coil does not have an excessive current flow. However, it is still possible that excessive current may be passing through the current coils, although the meter is indicating less than full scale. This should also be avoided, but it is less damaging than excessive voltage coil current.

2-7 THERMOCOUPLE INSTRUMENTS

A junction of two dissimilar metals develops an electromotive force (emf) when heated. By using a current to heat the junction, an emf is produced which is proportional to the heating effect of the current. Since the heating effect of a current is directly proportional to the rms value of the current (no matter what its waveform), the generated emf can be used as a measure of the rms level of the current.

2-7-1 Thermocouples

Figure 2-20 illustrates the principle of the *thermocouple instrument*. The thermocouple consists of the junction of two dissimilar metal wires welded to a heating wire. The current to be measured passes through the heater and thus heats the junction. A millivoltmeter measures the voltage developed across the junction. The scale of the meter is calibrated to indicate the actual rms current in the heater.

Two types of thermocouples are illustrated in Figure 2-21. Figure 2-21(a) shows a thermocouple enclosed in a vacuum tube to protect the

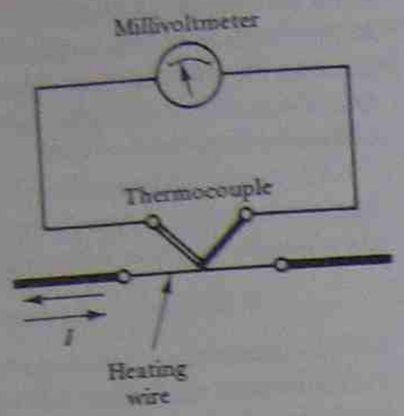
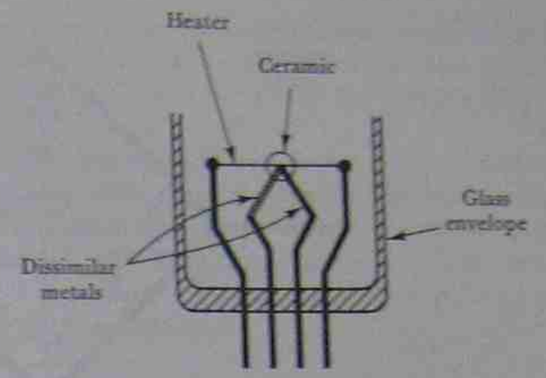


FIGURE 2-20. Basic thermocouple instrument.

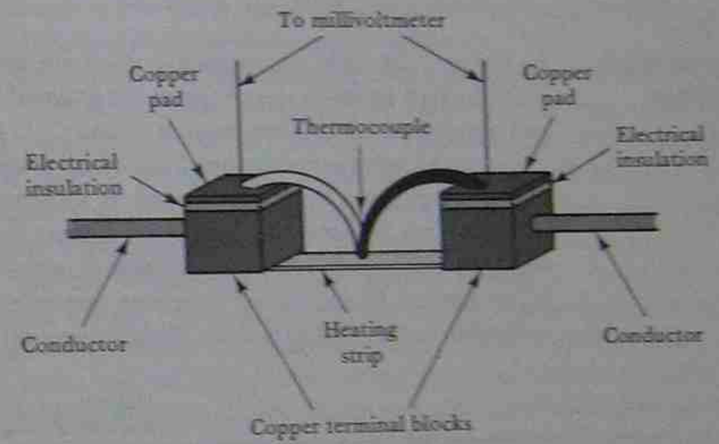
junction from loss of heat. The junction may be directly welded to the heater, or it may be thermally (but not electrically) connected to the heater by a bead of ceramic material.

In Figure 2-21(b) a thermocouple with a flat heating conductor is shown. The ends of the thermocouple wires are connected to copper pads which are electrically insulated from the heater. Although electrically insulated, the copper pads are in thermal contact with the large copper terminal blocks of the heater. This has the effect of keeping the ends of the thermocouple wires at the same ambient temperature as the terminal blocks. Thus, the thermocouple junction is heated, but the ends of the wires are at the normal (relatively cold) temperature of the terminals. When no current flows, both ends of each thermocouple wire are maintained at ambient temperature, and no voltage is generated. When the current flows, the junction of the dissimilar metal wires is heated, while the opposite ends remain at the ambient temperature. These opposite ends are electrically connected together through the millivoltmeter, so they can be termed a *cold junction*. This condition, of a hot junction and a cold junction in the thermocouple circuit, is the requirement for maximum emf generation. Since the thermocouple wires are maintained at the same ambient temperature when no current is flowing, the emf generated at the heated junction results only from the heating effect of the current. The device just described [Figure 2-21(b)] is termed a *compensated thermocouple*, meaning that it is compensated against the effects of any change in ambient temperature.

Some of the most common materials used as thermocouple pairs are Iron-Constantan, Copper-Constantan, Chromel-Alumel, and Platinum-platinum/Rhodium. Thermocouple junctions can survive very high temperatures and are used as temperature transducers. However, when used in a measuring instrument, the typical maximum heater temperature is about 300°C. The typical maximum thermocouple output at this temperature is around 12 mV. Heating element currents range from 2 mA to 50 mA.



(a) Thermocouple in a vacuum tube



(b) Compensated thermocouple

FIGURE 2-21. Two types of thermocouples.

2-7-2 Thermocouple Ammeters and Voltmeters

A thermocouple instrument can be used directly as an ammeter, and shunts can be employed to expand its range of current measurement. By connecting multiplier resistors in series with the heater, a voltmeter can be constructed. The sensitivity of thermocouple voltmeters is considerably lower than that of a PMMC voltmeter. However, thermocouple instruments indicate true rms value, no matter what the waveform of the applied voltage or current. They can also be used as transfer instruments; calibrated on dc and then employed to measure either ac or dc. Furthermore, thermocouple instruments can be used from dc to very high frequencies, 50 MHz and higher. The frequency limit, in fact, is due not to the thermocouple but to the capacitance and inductance of connecting leads and series resistors.

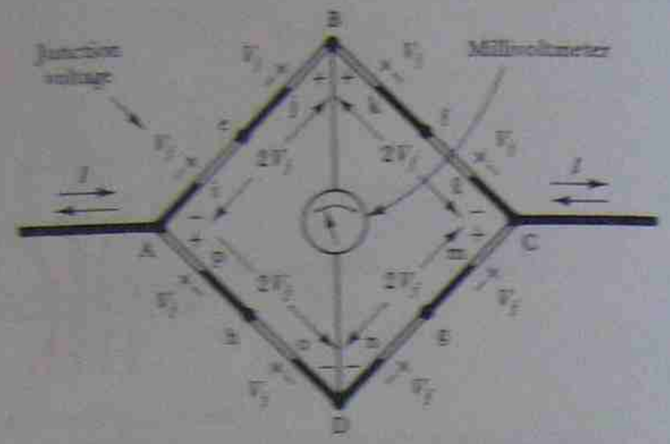


FIGURE 2-22. Thermocouple bridge instrument.

2-7-3 Thermocouple Bridge

In Figure 2-22 eight thermocouple pairs are arranged in a bridge configuration. Two series-connected pairs are situated between A and B. Another two are connected between each of B and C, C and D, D and A. Junctions e, f, g, and h are secured to terminals which project from an insulated base. These are *cold* junctions, maintained at ambient temperature. Junctions i through p are *hot* junctions, heated by current flowing from A to C (or the reverse) through each of the two chains of series-connected thermocouples. When current flows, the hot junctions generate voltages with the polarity indicated on the diagram. Thus, if each junction produces an emf of 6 mV,

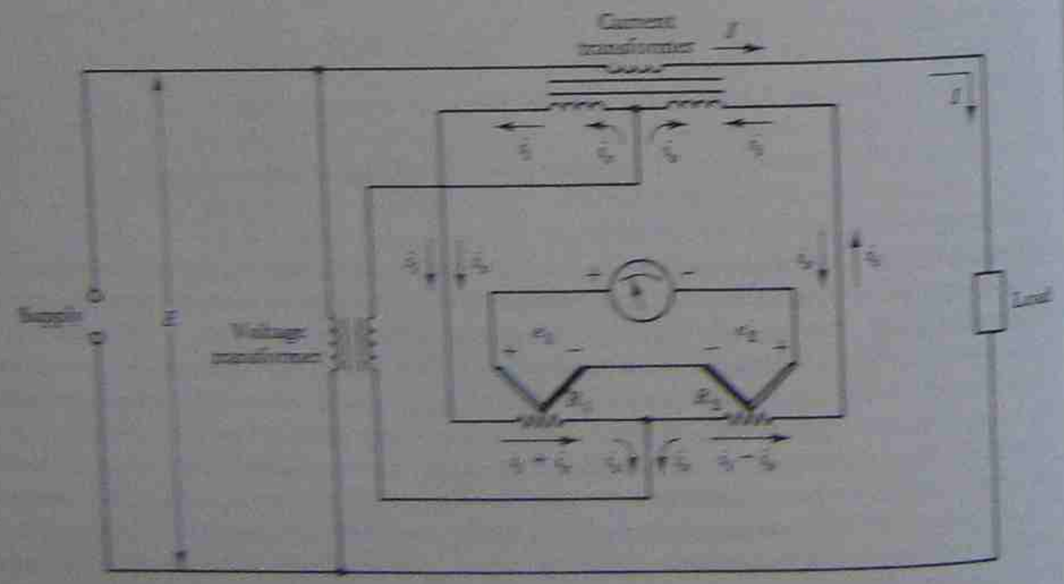


FIGURE 2-23. Basic circuit of a thermocouple wattmeter.

the total emf developed across the millivoltmeter connected to B and D is 4×6 mV $= 24$ mV. Note that no portion of the main circuit current I flows through the millivoltmeter because of the bridge configuration (see Section 6-3).

It is seen that a thermocouple bridge can generate more emf than a single junction acting alone. Also, the weakest part of the *separately heated* thermocouple is the heater itself, which tends to be rapidly destroyed when only 50% overloaded. The bridge type instrument (with directly heated thermocouples) is quite rugged because the current to be measured flows directly through the thermocouples.

2-7-4 Thermocouple Wattmeter

Since thermocouple instruments can be operated to very high frequencies, a thermocouple wattmeter is useful for power measurements at frequencies far beyond the range of electrodynamic wattmeters.

The basic circuit of a thermocouple wattmeter is shown in Figure 2-23. A *current transformer* is employed to produce a secondary current i_s, which is directly proportional to the load current I. The *voltage transformer* secondary voltage is directly proportional to the supply voltage E. Suppose, at a given instant, that the instantaneous current i_s is flowing from left to right through the thermocouple heaters, as illustrated. At the same instant, the current directly proportional to the supply voltage E flows into the center-tap of the secondary winding of the current transformer, then splits into equal current levels i_v. These currents (i_v) flow from the center-tap through each half of the current transformer secondary winding, as illustrated, then through R_1 and R_2 in opposite directions. The currents again combine at the junction of R_1 and R_2 where they flow back to the transformer secondary winding.

The current $i_v + i_s$ in R_1 heats its adjacent thermocouple and produces an output e_1 with polarity: + on the left, − on the right. Current $i_v - i_s$ flowing in R_2 heats its thermocouple and produces an output e_2 with polarity opposite to that of e_1: − on the left, + on the right. The millivoltmeter indicates $e_1 - e_2$. Since e_1 and e_2 are proportional to the square of the current in each heater:

$$e_1 \propto (i_v + i_s)^2,$$

$$i_v \propto I, \text{ and } i_s \propto E,$$

so $$e_1 \propto (I + E)^2,$$

or $$e_1 \propto I^2 + 2EI + E^2,$$

also $$e_2 \propto (i_v - i_s)^2 \propto (I - E)^2,$$

or $$e_2 \propto I^2 - 2EI + E^2,$$

millivoltmeter reading $= e_1 - e_2$

$$\propto (I^2 + 2EI + E^2) - (I^2 - 2EI + E^2)$$

$$\propto 4EI.$$

Therefore the millivoltmeter indicates a voltage proportional to EI, which is the power delivered to the load. When there is a phase difference between E and I, the power dissipated in each of the thermocouple heaters is proportional to $(I + E\cos\phi)^2$ and $(I - E\cos\phi)^2$. This gives a millivoltmeter indication proportional to $EI\cos\phi$, i.e., proportional to true power.

In practice, the thermocouple wattmeter circuit is usually a little more complicated than that shown in Figure 2-23. Instead of two thermocouples, a thermocouple bridge may be employed with the heating currents flowing directly through the thermocouple junctions.

REVIEW QUESTIONS AND PROBLEMS

2-1. Sketch a circuit diagram to show how a PMMC instrument can be converted into an ammeter. Explain the operation of the circuit.

2-2. Explain the following terms: *four terminal resistor*, *make-before-break switch*, *Ayrton shunt*.

2-3. Sketch the circuit diagram of a *multirange ammeter*: (a) using a number of individual shunts and (b) using an Ayrton shunt. Explain the circuit operation in each case.

2-4. A PMMC instrument has a coil resistance of 750 Ω and FSD of 500 μA. Determine the required shunt resistance value to convert the instrument into an ammeter with: (a) FSD = 50 mA and (b) FSD = 30 mA.

2-5. An ammeter is constructed of a 133.3-Ω resistance in parallel with a PMMC instrument. The instrument has FSD = 30 μA and its coil resistance is 1.2 kΩ. Calculate the measured current at FSD, $\frac{1}{2}$ FSD, and $\frac{1}{3}$ FSD.

2-6. An ammeter consists of a PMMC instrument in parallel with an Ayrton shunt. The PMMC instrument has a coil resistance of 1.2 kΩ and FSD = 100 μA. The Ayrton shunt consists of four 0.1-Ω series-connected resistances. Sketch the circuit diagram, and calculate the ammeter range at each setting of the shunt.

2-7. Discuss temperature error in ammeters and explain how it is minimized.

2-8. A 12-V source supplies 25 A to a load. Calculate the load current that would be measured when using an ammeter with: (a) a resistance of 0.12 Ω, (b) a resistance of 0.52 Ω, and (c) a resistance of 0.002 Ω.

2-9. Sketch the circuit diagram to show how a PMMC instrument can be converted into a voltmeter. Explain the operation of the circuit.

2-10. Sketch the circuit diagram of a *multirange voltmeter* using: (a) individual multiplier resistors and (b) series-connected multipliers. Explain the circuit operation in each case.

2-11. A PMMC instrument with a FSD of 75 μA and coil resistance of 900 Ω is to be used as a voltmeter. Calculate the values of the individual multiplier resistance required to give FSD of (a) 100 V, (b) 30 V, and (c) 5 V. Also determine the voltmeter sensitivity.

2-12. Calculate the values of the multiplier resistances required for the voltmeter described in Question 2-11 when series-connected multipliers are employed.

2-13. Discuss temperature error in voltmeters and explain how it is minimized.

2-14. A multirange voltmeter employs a PMMC instrument with $R_m = 1.3$ kΩ and FSD = 500 μA. The series-connected multiplier resistors [as in Figure 2-9(b)] are $R_1 = 38.7$ kΩ, $R_2 = 40$ kΩ, and $R_3 = 40$ kΩ. Calculate the three voltage ranges for the voltmeter and determine its sensitivity.

2-15. Two resistors R_1 and R_2 are connected in series across a 15-V supply. A voltmeter on a 10-V range is connected to measure the voltage across R_2. $R_1 = 47$ kΩ, $R_2 = 82$ kΩ, and the voltmeter sensitivity is 10 kΩ/V. Calculate V_{R2}: (a) when the voltmeter is connected and (b) without the voltmeter in the circuit.

2-16. A 100-kΩ potentiometer and a 33-kΩ resistor are connected in series across a 9-V supply. Calculate the maximum output voltage that can be measured across the potentiometer using: (a) a voltmeter with a sensitivity of 20 kΩ/V on a 15-V range and (b) a voltmeter with a sensitivity of 100 kΩ/V on a 10-V range.

2-17. Sketch the symbol and characteristics of a semiconductor rectifier. Briefly explain.

2-18. Discuss the response of a PMMC instrument when an alternating current passes through it when: (a) no rectification is involved and (b) a rectifier is connected in series with the instrument.

2-19. Sketch the circuit of an ac voltmeter using a PMMC instrument and a bridge rectifier. Sketch the rectified voltage waveform, and briefly explain the operation of the circuit.

2-20. Sketch the circuit and waveforms for an ac voltmeter using a PMMC instrument and half-wave rectification. Explain the circuit operation.

2-21. An ac voltmeter uses a bridge rectifier with silicon diodes and a PMMC instrument with FSD = 75 μA. The meter coil resistance is 900 Ω, and the voltmeter multiplier resistor is 708 kΩ. Calculate the applied rms voltage when the meter indicates FSD.

2-22. For the voltmeter described in Question 2-21, determine the new value of multiplier resistance to change the range to 300 V at FSD.

2-23. Calculate the pointer position on the instrument in Question 2-22 when the rms input voltage is: (a) 30 V and (b) 10 V.

2-24. A PMMC instrument with a FSD of 75 μA and coil resistance of 900 Ω is to be used with a half-wave rectifier circuit as an ac voltmeter. Silicon diodes are used, and the minimum diode forward current is to be 80 μA when the instrument indicates $\frac{1}{4}$ of FSD. Calculate the values of the meter shunt resistance and the multiplier resistance required to give a FSD of 200 V.

2-25. Calculate the sensitivity of the ac voltmeter in Question 2-21.

2-26. Calculate the sensitivity of the ac voltmeter in Question 2-24.

2-27. Sketch the circuit of an ac voltmeter using half-bridge full-wave rectification. Briefly explain.

2-28. Sketch the circuit of a rectifier ammeter and explain its operation.

2-29. A rectifier ammeter is to indicate full scale for a current of 1 A. The PMMC meter used has FSD = 500 μA and $R_m = 1200\ \Omega$. The current transformer turns are $N_s = 7000$ and $N_p = 10$. Silicon diodes are used and the meter series resistance is $R_s = 150\ \text{k}\Omega$. Determine the required value of the secondary shunt resistance.

2-30. A rectifier ammeter has the following components: PMMC instrument, FSD = 200 μA, $R_m = 900\ \Omega$. Current transformer, $N_s = 600$, $N_p = 5$. Germanium diodes, $V_F = 0.3$ V. Meter series resistance, $R_s = 270\ \text{k}\Omega$. Transformer secondary shunt resistance, $R_L = 99.06\ \text{k}\Omega$. Calculate the level of transformer primary current which will give FSD on the instrument.

2-31. Sketch the arrangement of coils in an electrodynamic instrument and briefly explain how the instrument behaves when passing ac.

2-32. Sketch the circuits of an electrodynamic instrument employed as: (a) a voltmeter and (b) an ammeter. Briefly explain each circuit.

2-33. Sketch the circuit of an electrodynamic instrument employed as a wattmeter. Explain why the instrument measures true power on ac and on dc.

2-34. Sketch the circuit of a compensated wattmeter and explain how it eliminates measurement errors.

2-35. Sketch the circuit of a multirange electrodynamic wattmeter. Explain its operation and state all precautions that should be observed in using the instrument.

2-36. Draw sketches of two basic types of thermocouples. Explain the operation of each. Discuss the use of thermocouples in dc and ac ammeters and voltmeters.

2-37. Sketch the circuit of a thermocouple bridge. Explain its operation and advantages over a single thermocouple.

2-38. Sketch the basic circuit of a thermocouple wattmeter. Explain the operation of the circuit and show that the instrument deflection is proportional to voltage × current.

3

THE OHMMETER AND THE VOLT-OHM-MILLIAMMETER

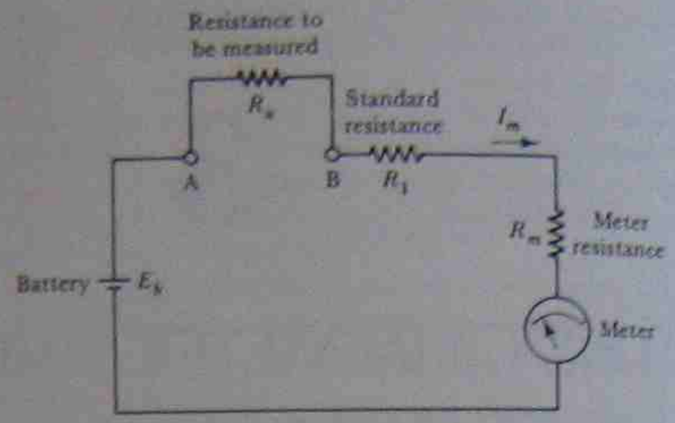
INTRODUCTION An *ohmmeter* is a PMMC instrument with an internal battery and standard resistors. The resistance to be measured is connected so that current flows through it via a standard resistor and the meter. The meter current is inversely proportional to the unknown resistance, and the scale is calibrated to indicate resistance. A means of adjusting the meter current is included to take care of battery voltage variations. Range changing is effected by switching standard resistance values.

The *volt-ohm-milliammeter* (VOM) is a multifunction instrument capable of operating as an ac or dc voltmeter, an ohmmeter, or an ac or dc ammeter. A function switch is provided to permit selection of any function, and a range switch facilitates range changing. Additional functions are available with the use of adapters or probes.

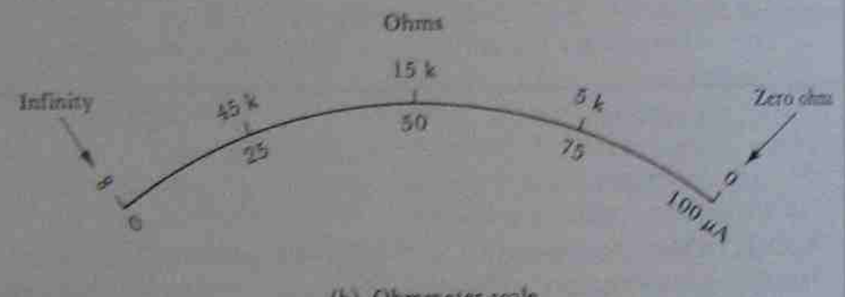
3-1 SERIES OHMMETER

3-1-1 Basic Circuit and Scale

An *ohmmeter* (ohm-meter) is normally part of a *volt-ohm-milliammeter* (VOM), or *multifunction* meter. Ohmmeters do not usually exist as individual instruments. The simplest ohmmeter circuit consists of a voltage source connected in series with a pair of terminals, a standard resistance, and a low current PMMC instrument. Such a circuit is shown in Figure 3-1(a). The resistance to be measured (R_x) is connected across terminals A and B.



(a) Basic circuit of series ohmmeter



(b) Ohmmeter scale

FIGURE 3-1. Circuit and scale of a basic series ohmmeter.

The meter current indicated by the instrument in Figure 3-1(a) is (battery voltage)/(total series resistance):

$$I_m = \frac{E_b}{R_x + R_1 + R_m}. \tag{3-1}$$

When the external resistance is zero (i.e., terminals A and B short-circuited), Equation (3-1) becomes

$$I_m = \frac{E_b}{R_1 + R_m}.$$

If R_1 and R_m are selected (or if R_1 is adjusted) to give FSD when A and B are short-circuited, then FSD is marked as *zero ohms*. Thus, for $R_x = 0$, the pointer indicates 0 Ω [see Figure 3-1(b)]. When terminals A

and B are open-circuited, the effective value of resistance R_x is infinity. No meter current flows, and the pointer indicates zero current. This point (zero current) is marked as *infinity* (∞) on the resistance scale [Figure 3-1(b)].

If a resistance R_x with a value between zero and infinity is connected across terminals A and B, the meter current is greater than zero but less than FSD. The pointer position on the scale now depends upon the relationship between R_x and $R_1 + R_m$. This is demonstrated by Example 3-1.

EXAMPLE 3-1 The series ohmmeter in Figure 3-1(a) is made up of a 1.5-V battery, a 100-μA meter, and a resistance R_1 which makes $(R_1 + R_m) = 15$ kΩ. (a) Determine the instrument indication when $R_x = 0$. (b) Determine how the resistance scale should be marked at $\frac{1}{2}$ FSD, $\frac{1}{4}$ FSD, and $\frac{3}{4}$ FSD.

SOLUTION

a. Equation 3-1

$$I = \frac{E_b}{R_x + R_1 + R_m}$$
$$= \frac{1.5\text{ V}}{0 + 15\text{ k}\Omega}$$
$$= 100\ \mu\text{A (FSD)}.$$

b. *At* $\frac{1}{2}$ FSD:

$$I = \frac{100\ \mu\text{A}}{2} = 50\ \mu\text{A};$$

From Equation 3-1,

$$R_x + R_1 + R_m = \frac{E_b}{I},$$
$$R_x = \frac{E_b}{I} - (R_1 + R_m)$$
$$= \frac{1.5\text{ V}}{50\ \mu\text{A}} - 15\text{ k}\Omega$$
$$= 15\text{ k}\Omega.$$

At $\frac{1}{4}$ FSD:

$$I = \frac{100\ \mu\text{A}}{4} = 25\ \mu\text{A},$$
$$R_x = \frac{1.5\text{ V}}{25\ \mu\text{A}} - 15\text{ k}\Omega$$
$$= 45\text{ k}\Omega.$$

At $\frac{1}{2}$ FSD:

$$I = 0.75 \times 100\ \mu\text{A} = 75\ \mu\text{A},$$

$$R_x = \frac{1.5\ \text{V}}{75\ \mu\text{A}} - 15\ \text{k}\Omega$$

$$= 5\ \text{k}\Omega.$$

The ohmmeter scale is now marked as shown in Figure 3-1(*b*).

From Example 3-1 note that the measured resistance at center-scale is equal to the internal resistance of the ohmmeter, i.e., $R_x = R_1 + R_m$. The trouble arose because at FSD the total resistance is $R_1 + R_m$, and when its resistance is doubled, $R_x + R_1 + R_m = 2(R_1 + R_m)$, the circuit current is halved.

3-3-2 Calibration Control

The simple ohmmeter described above will operate satisfactorily as long as the battery voltage remains exactly at 1.5 V. When the battery voltage changes, the instrument scale is no longer correct. Even if R_1 were adjusted to give full-scale when terminals *A* and *B* are short-circuited, the scale would still be in error because now mid-scale would represent a resistance equal to the sum value of $R_1 + R_m$. Failing battery voltage can be taken care of by an adjustable resistor connected in parallel with the meter (R_2 in Figure 3-2).

In Figure 3-2 the battery current I_b splits up into meter current I_m and resistor current I_2. With terminals *A* and *B* short-circuited, R_2 is adjusted to give FSD on the meter. At this time the total circuit resistance is $R_1 + R_2 \| R_m$. Since R_1 is always very much larger than $R_2 \| R_m$, the total circuit resistance can be assumed to equal R_1. When a resistance R_x equal to $R_1 +$

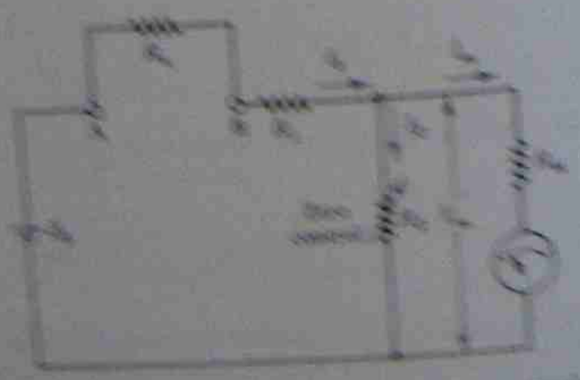


FIGURE 3-2 Series ohmmeter with zero control.

connected across terminals *A* and *B*, the circuit resistance is doubled and the circuit current is halved. This causes both I_2 and I_m to be reduced to half of their previous levels (i.e., when *A* and *B* were short-circuited). Thus, the mid-scale measured resistance is again equal to the ohmmeter internal resistance R_1.

The equation for the battery current in Figure 3-2 is

$$I_b = \frac{E_b}{R_1 + R_2 \| R_m}.$$

If $(R_2 \| R_m) \ll R_1$,

$$\boxed{I_b = \frac{E_b}{R_1 + R_x}} \tag{3-2}$$

Also, the meter voltage is:

$$E_m = I_b(R_2 \| R_m)$$

which gives meter current as:

$$\boxed{I_m = \frac{I_b(R_2 \| R_m)}{R_m}} \tag{3-3}$$

Each time the ohmmeter is used, terminals *A* and *B* are first short-circuited, and R_2 is adjusted for zero-ohm indication on the scale (i.e., for FSD). If this procedure is followed, then even when the battery voltage falls below its initial level, the scale remains correct. Examples 3-2 and 3-3 demonstrate that this is so.

EXAMPLE 3-2 The ohmmeter circuit in Figure 3-2 has $E_b = 1.5$ V, $R_1 = 15$ kΩ, $R_m = 50$ Ω, $R_2 = 50$ Ω, and meter FSD = 50 μA. Determine the ohmmeter scale readings at FSD, $\frac{1}{2}$ FSD, and $\frac{1}{5}$ FSD.

At FSD:

$$I_m = 50\ \mu\text{A}$$

$$E_m = I_m R_m = 50\ \mu\text{A} \times 50\ \Omega$$

$$= 2.5\ \text{mV},$$

$$I_2 = \frac{E_m}{R_2} = \frac{2.5\ \text{mV}}{50\ \Omega}$$

$$= 50\ \mu\text{A}.$$

$$\text{Battery current } I_b = I_2 + I_m$$

$$= 50\ \mu\text{A} + 50\ \mu\text{A}$$

$$= 100\ \mu\text{A}.$$

From Equation 3-2,

$$R_x + R_1 \simeq \frac{E_b}{I_b} = \frac{1.5\text{ V}}{100\ \mu\text{A}}$$
$$= 15\ \text{k}\Omega,$$
$$R_x = (R_x + R_1) - R_1$$
$$= 15\ \text{k}\Omega - 15\ \text{k}\Omega$$
$$= 0\ \Omega.$$

At $\frac{1}{2}$ FSD:

$$I_m = 25\ \mu\text{A},$$
$$V_m = 25\ \mu\text{A} \times 50\ \Omega$$
$$= 1.25\ \text{mV},$$
$$I_2 = \frac{1.25\text{ mV}}{50\ \Omega} = 25\ \mu\text{A},$$
$$I_b = 25\ \mu\text{A} + 25\ \mu\text{A} = 50\ \mu\text{A},$$
$$R_x + R_1 = \frac{1.5\text{ V}}{50\ \mu\text{A}} = 30\ \text{k}\Omega,$$
$$R_x = 30\ \text{k}\Omega - 15\ \text{k}\Omega$$
$$= 15\ \text{k}\Omega.$$

At $\frac{3}{4}$ FSD:

$$I_m = 0.75 \times 50\ \mu\text{A} = 37.5\ \mu\text{A},$$
$$V_m = 37.5\ \mu\text{A} \times 50\ \Omega$$
$$= 1.875\ \text{mV},$$
$$I_2 = \frac{1.875\text{ mV}}{50\ \Omega} = 37.5\ \mu\text{A},$$
$$I_b = 37.5\ \mu\text{A} + 37.5\ \mu\text{A} = 75\ \mu\text{A},$$
$$R_x + R_1 = \frac{1.5\text{ V}}{75\ \mu\text{A}} = 20\ \text{k}\Omega,$$
$$R_x = 20\ \text{k}\Omega - 15\ \text{k}\Omega$$
$$= 5\ \text{k}\Omega.$$

EXAMPLE 3-3 For the ohmmeter circuit in Figure 3-2, determine the new resistance value to which R_2 must be adjusted when E_b falls to 1.3 V. Also, once more determine the resistance scale readings at $\frac{1}{2}$ FSD and $\frac{3}{4}$ FSD when R_2 is adjusted.

SOLUTION

When $R_x = 0$:

Equation 3-2,

$$I_b \simeq \frac{E_b}{R_x + R_1} = \frac{1.3\text{ V}}{0 + 15\ \text{k}\Omega}$$
$$= 86.67\ \mu\text{A},$$
$$I_m = 50\ \mu\text{A (FSD)},$$
$$I_2 = I_b - I_m = 86.67\ \mu\text{A} - 50\ \mu\text{A}$$
$$= 36.67\ \mu\text{A},$$
$$V_m = I_m R_m = 50\ \mu\text{A} \times 50\ \Omega$$
$$= 2.5\ \text{mV},$$
$$R_2 = \frac{V_m}{I_2} = \frac{2.5\text{ mV}}{36.67\ \mu\text{A}}$$
$$= 68.18\ \Omega.$$

At $\frac{1}{2}$ FSD:

$$I_m = 25\ \mu\text{A},$$
$$V_m = 25\ \mu\text{A} \times 50\ \Omega$$
$$= 1.25\ \text{mV},$$
$$I_2 = \frac{V_m}{R_2} = \frac{1.25\text{ mV}}{68.18\ \Omega}$$
$$= 18.33\ \mu\text{A},$$
$$I_b = I_m + I_2 = 25\ \mu\text{A} + 18.33\ \mu\text{A}$$
$$= 43.33\ \mu\text{A},$$
$$R_x + R_1 = \frac{V_m}{I_b} = \frac{1.3\text{ V}}{43.33\ \mu\text{A}}$$
$$= 30\ \text{k}\Omega,$$
$$R_x = 30\ \text{k}\Omega - 15\ \text{k}\Omega$$
$$= 15\ \text{k}\Omega.$$

At $\frac{3}{4}$ FSD:

$$I_m = 0.75 \times 50\ \mu\text{A} = 37.5\ \mu\text{A},$$
$$V_m = 37.5\ \mu\text{A} \times 50\ \Omega$$
$$= 1.875\ \text{mV},$$
$$I_2 = \frac{1.875\text{ mV}}{68.18\ \Omega} = 27.5\ \mu\text{A},$$
$$I_b = 37.5\ \mu\text{A} + 27.5\ \mu\text{A} = 65\ \mu\text{A},$$
$$R_x + R_1 = \frac{V_m}{I_b} = \frac{1.3\text{ V}}{65\ \mu\text{A}} = 20\ \text{k}\Omega,$$
$$R_x = 20\ \text{k}\Omega - 15\ \text{k}\Omega$$
$$= 5\ \text{k}\Omega.$$

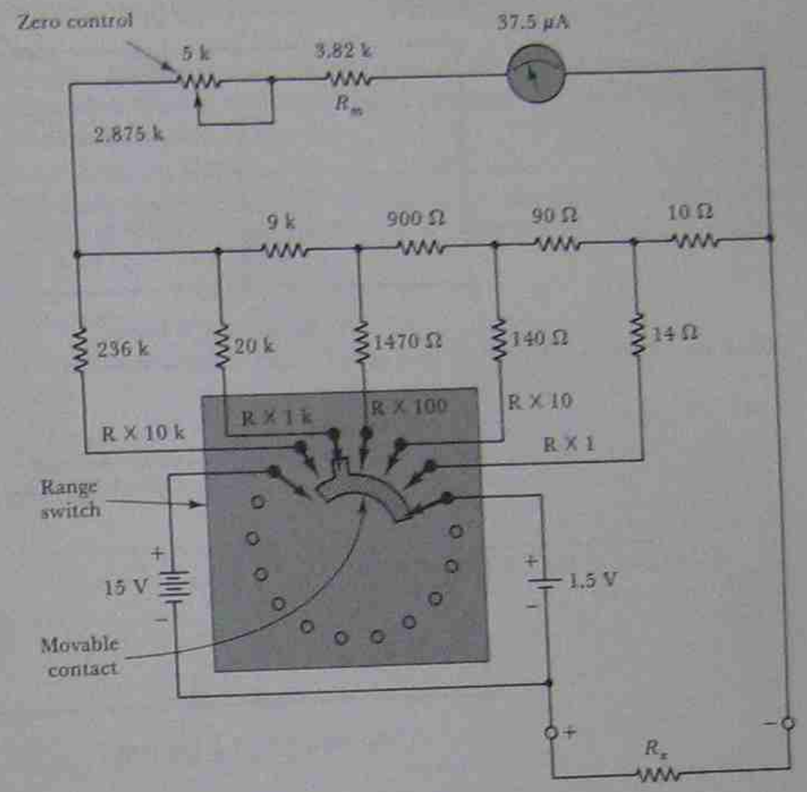
3-2 MULTIRANGE SHUNT OHMMETER

The series ohmmeter circuit discussed in Section 3-1 could be converted to a multirange ohmmeter by employing several values of standard resistor (R_1 in Figure 3-2) and a rotary switch. The major inconvenience of such a circuit is the fact that a large adjustment of the zero control (R_2 in Figure 3-2) would have to be made every time the resistance range is changed. In the *shunt ohmmeter* circuit, this adjustment is not necessary; once zeroed, the instrument can be switched between ranges with only minor zero adjustments.

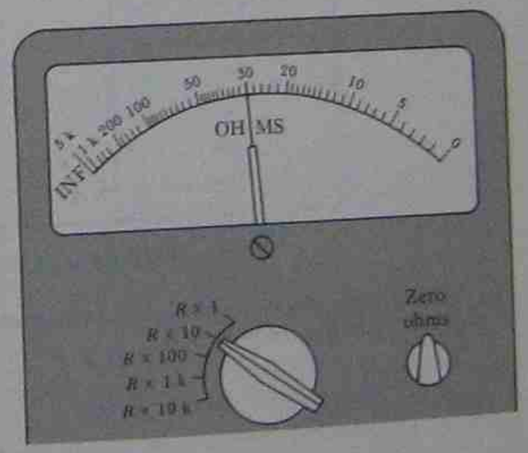
Figure 3-3(a) shows the circuit of a typical multirange shunt ohmmeter as found in good quality multifunction deflection instruments. The deflection meter used gives FSD when passing 37.5 μA, and its resistance (R_m) is 3.82 kΩ. The zero control is a 5-kΩ variable resistance, which is set to 2.875 kΩ when the battery voltages are at the normal levels. Two batteries are included in the circuit; a 1.5-V battery used on all ranges except the $R \times 10$-kΩ range, and a 15-V battery solely for use on the $R \times 10$-kΩ range. R_x, the resistance to be measured, is connected at the terminals of the circuit. The terminals are identified as + and − because the ohmmeter circuit is part of an instrument which also functions as an ammeter and as a voltmeter. It is important to note that the *negative* terminal of each battery is connected to the + terminal of the multifunction instrument.

The range switch in Figure 3-3(a) has a movable contact which may be step-rotated clockwise or counterclockwise. The battery terminals on the rotary switch are seen to be longer than any other terminals so that they make contact with the largest part of the movable contact, while the other (short) terminals reach only to the tab of the moving contact. In the position shown, the $R \times 1$K terminal is connected (via the movable contact) to the + terminal of the 1.5-V battery. If the movable contact is step-rotated clockwise it will connect the 1.5-V battery in turn to $R \times 100$, $R \times 10$, and $R \times 1$ terminals. When rotated one step counterclockwise from the position shown, the movable contact is disconnected from the 1.5-V battery, and makes contact between the $R \times 10$K terminal and the + terminal of the 15-V battery.

In Figure 3-3(b) the typical scale and controls for this type of ohmmeter are illustrated. When the range switch is set to $R \times 1$, the scale is read directly in ohms. On any other range the scale reading is multiplied by the range factor. On $R \times 100$, for example, the pointer position illustrated would be read as $30\ \Omega \times 100 = 3\ \text{k}\Omega$. The instrument must be *zeroed* before use to take care of battery voltage variation. This can be performed on any range, simply by short-circuiting the + and − terminals and adjusting the zero control until the pointer indicates exactly 0 Ω. When changing to or from the $R \times 10$-kΩ range, the ohmmeter zero must always be checked because the circuit supply is being switched between the 15-V and 1.5-V batteries.

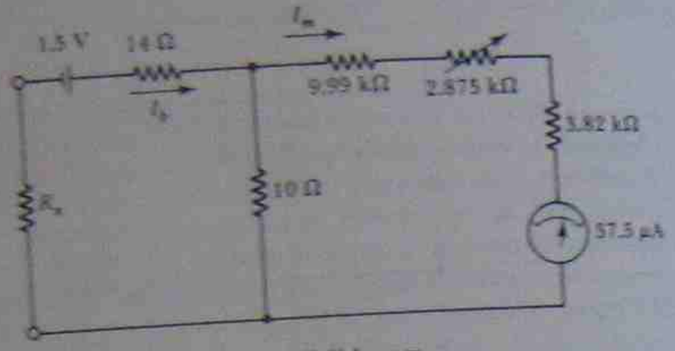


(a) Multirange ohmmeter circuit

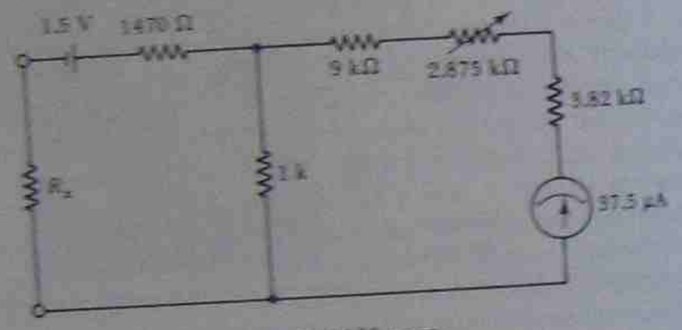


(b) Range switch and scale

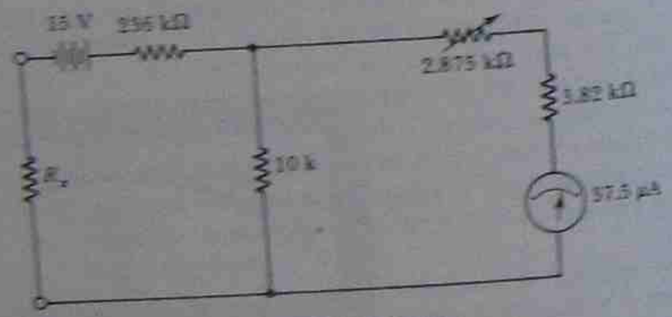
FIGURE 3-3. Circuit, scale, and controls for a typical multirange ohmmeter.



(a) Circuit for $R \times 1$ range



(b) Circuit for $R \times 100$ range



(c) Circuit for $R \times 10$ k range

FIGURE 3-4 Equivalent circuits of the ohmmeter [Figure 3-3(a)] for various positions of the range switch.

The ohmmeter equivalent circuits for three of its ranges are shown in Figure 3-4. Current and resistance calculations for each of these ranges are made in Examples 3-4 and 3-5.

EXAMPLE 3-4 Calculate the meter current and indicated resistance for the ohmmeter circuit of Figure 3-3(a) on its $R \times 1$ range when: (a) $R_x = 0$ and (b) $R_x = 24\ \Omega$.

SOLUTION

The equivalent circuit in Figure 3-4(a) is derived from Figure 3-3(a), for the $R \times 1$ range.

When $R_x = 0$:

battery current,

$$I_s = \frac{1.5\ \text{V}}{14\ \Omega + [10\ \Omega \| (9.99\ \text{k}\Omega + 2.875\ \text{k}\Omega + 3.82\ \text{k}\Omega)]}$$

$$= \frac{1.5\ \text{V}}{14\ \Omega + (10\ \Omega \| 16.685\ \text{k}\Omega)}$$

$$= 62.516\ \text{mA}.$$

Using the current divider rule:

$$\text{meter current } I_m = 62.516\ \text{mA} \times \frac{10\ \Omega}{(10\ \Omega + 16.685\ \text{k}\Omega)}$$

$$= 37.5\ \mu\text{A}$$

$$= \text{full scale} = 0\ \Omega.$$

When $R_x = 24\ \Omega$:

$$I_s = \frac{1.5\ \text{V}}{24\ \Omega + 14\ \Omega + (10\ \Omega \| 16.685\ \text{k}\Omega)}$$

$$= 31.254\ \text{mA},$$

$$I_m = 31.254\ \text{mA} \times \frac{10\ \Omega}{(10\ \Omega + 16.685\ \text{k}\Omega)}$$

$$= 18.72\ \mu\text{A}$$

$$\simeq (\text{half scale} = 24\ \Omega).$$

EXAMPLE 3-5 Calculate the meter current for the $R \times 100$ and $R \times 10$K ranges of the ohmmeter in Figure 3-3(a) when $R_x = 0$.

SOLUTION

Equivalent circuits in Figure 3-4(b) and (c) are derived from Figure 3-3(a)

$R \times 100$ range:

$$I_b = \frac{1.5\text{ V}}{1470\,\Omega + [1\text{ k}\Omega \| (9\text{ k}\Omega + 2.875\text{ k}\Omega + 3.82\text{ k}\Omega)]}$$

$$= \frac{1.5\text{ V}}{1470\,\Omega + (1\text{ k}\Omega \| 15.695\text{ k}\Omega)}$$

$$= 622.38\,\mu\text{A},$$

$$I_m = 622.38\,\mu\text{A} \times \frac{1\text{ k}\Omega}{1\text{ k}\Omega + 15.695\text{ k}\Omega}$$

$$\simeq 37.5\,\mu\text{A (Full scale)}.$$

$R \times 10$ kΩ range:

$$I_b = \frac{15\text{ V}}{236\text{ k}\Omega + [10\text{ k}\Omega \| (2.875\text{ k}\Omega + 3.82\text{ k}\Omega)]}$$

$$= \frac{15\text{ V}}{236\text{ k}\Omega + (10\text{ k}\Omega \| 6.695\text{ k}\Omega)}$$

$$= 62.5\,\mu\text{A},$$

$$I_m = 62.5\,\mu\text{A} \times \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 6.695\text{ k}\Omega}$$

$$\simeq 37.5\,\mu\text{A (Full scale)}.$$

3-3 OHMMETER ACCURACY

Referring to Figure 3-3(b), it is clear that the ohmmeter scale is nonlinear. On the $R \times 1$ range the pointer indicates 24 Ω at $\frac{1}{2}$ FSD. At 0.9 FSD, the indicated resistance is 2.6 Ω, and at 0.1 FSD the resistance measured is 216 Ω. (Although they are not marked on the scale, these resistance values can be calculated for 0.9 and 0.1 FSD.) Therefore, in the range 0.1 to 0.9 FSD, resistance values from 2.6 Ω to 216 Ω can be measured. But the portion of the scale from 0.1 FSD to zero deflection includes all resistance values from 216 Ω to infinity. Also, that part of the scale from 0.9 FSD to FSD covers all resistance values from 2.6 Ω to 0 Ω. Clearly, on this range of the ohmmeter, resistance values from 0 to 2.6 Ω and from 216 Ω to infinity cannot be measured or even roughly estimated. For example, at what points on the scale would 0.01 Ω and 200 kΩ be found? *The useful range of the ohmmeter scale is seen to be approximately from 10% to 90% of FSD.* Now consider the actual accuracy of the resistance measurement.

As already demonstrated in Sections 3-1 and 3-2, an ohmmeter indicates $\frac{1}{2}$ FSD when the measured resistance R_x is equal to the ohmmeter internal resistance. Also, it was explained in Section 1-6 that the current meter accuracy is usually specified as a percentage of full scale. Now determine the errors that may occur in resistance measurement by an ohmmeter which uses an instrument with an accuracy of $\pm 1\%$.

At $\frac{1}{2}$ FSD, the accuracy of pointer deflection is $\pm 1\%$ of FSD, which, when used as a current meter, is $\pm 2\%$ of the indicated current. Also, at $\frac{1}{2}$ FSD, (measured resistance R_x) = (ohmmeter internal resistance R_1) and

$$I_b = \frac{E_b}{R_1 + R_x}.$$

Since the current meter accuracy (at $\frac{1}{2}$ FSD) is $\pm 2\%$ of the indicated current, the accuracy of I_b is $\pm 2\%$. Consequently, the accuracy of the total circuit resistance is $\pm 2\%$ (assuming the ohmmeter was initially zeroed to suit the battery voltage). If R_1 is made up of precision resistors, then virtually none of the $\pm 2\%$ resistance error can be assumed to reside in R_1. All of the resistance error must exist in R_x, the measured resistance.

The total resistance error is $\pm 2\%$ of $R_1 + R_x$. Since $R_1 = R_x$ at $\frac{1}{2}$ FSD, the total error in R_x is = $\pm 2\%$ of $(2R_x) = \pm 4\%$ of R_x.

Thus, an ohmmeter which uses precision internal resistors, and a current meter with an accuracy of $\pm 1\%$ of FSD, measures resistance at $\frac{1}{2}$ FSD with an accuracy of $\pm 4\%$.

EXAMPLE 3-6 Analyze the ohmmeter accuracy when the pointer is at 0.8 FSD and at 0.2 FSD.

SOLUTION

At 0.8 FSD:

$$R_x + R_1 = \frac{E_b}{0.8 I_{\text{FSD}}}$$

$$= \frac{R_1}{0.8} = 1.25R_1,$$

or

$$1.25R_1 - R_1 = R_x,$$

$$0.25R_1 = R_x,$$

$$R_1 = 4R_x,$$

$$\text{total error} = 1\% \text{ of FSD}$$

$$= \frac{1\%}{0.8} \text{ of pointer indication}$$

$$= 1.25\% \text{ of pointer indication},$$

$$\text{total } R_x \text{ error} = 1.25\% \text{ of } (R_1 + R_x)$$

$$= 1.25\% \text{ of } (4R_x + R_x)$$

$$= 6.25\% \text{ of } R_x.$$

At 0.2 FSD:

$$R_x + R_1 = \frac{E_b}{0.2I_{FSD}}$$

$$= \frac{R_1}{0.2} = 5R_1,$$

or

$$R_1 = \frac{R_x}{4},$$

$$\text{total error} = 1\% \text{ of FSD}$$

$$= \frac{1\%}{0.2} \text{ of pointer indication}$$

$$= 5\% \text{ of pointer indication,}$$

$$\text{total } R_x \text{ error} = 5\% \text{ of } (R_1 + R_x)$$

$$= 5\% \text{ of } \left(\frac{R_x}{4} + R_x\right)$$

$$= 6.25\% \text{ of } R_x.$$

The above analysis demonstrates that when indicating half-scale deflection, the ohmmeter error is ±4 (current meter error). Also, at 0.8 FSD the ohmmeter error is ±6.25 (meter error). Similarly, at 0.2 FSD the ohmmeter error is again ±6.25 (meter error). It is seen that *for greatest accuracy the ohmmeter range should always be selected to give an indication as close as possible to* ½ FSD.

3-4 THE VOLT-OHM-MILLIAMMETER OR MULTIMETER

The VOM is a multifunction instrument which can be used to measure dc or ac voltages, dc or ac current, and resistance. Some VOMs are also capable of decibel measurement, and some (with the use of adaptors) can measure inductance and capacitance.

The VOM circuitry for each function is essentially the voltmeter, ammeter, and ohmmeter multirange circuitry already discussed in Chapter 2 and Section 3-2. The precision resistors used in the instrument normally serve (as far as possible) in all functions of the instrument. The circuitry is simply rearranged (as a voltmeter, ammeter, or ohmmeter) by setting switches to the appropriate positions.

The front panel and scales for a typical good quality deflection VOM are illustrated in Figure 3-5. The *function switch* facilitates selection of DC mA (dc milliamps), DC V (dc volts), *R* (resistance), AC V (ac volts), and AC mA (ac milliamps). Moving clockwise around the range switch, the 0.1 through 1000 ranges apply to all current and voltage ranges, with the exception that ac current and voltage ranges commence at 1 mA and 1 V



FIGURE 3-5. Typical deflection type volt-ohm-milliameter (Courtesy of Thorn EMI Instruments Limited).

respectively. Thus, using the + and − terminals the instrument can measure the following:

1. *Direct current* on twelve ranges from 0 to 100 μA through 0 to 1 A. (Note that the 0.1-V dc range can also be employed as a 50-μA dc range.)
2. *Direct voltage* on twelve ranges from 0 to 100 mV through 0 to 1000 V.
3. *Resistance* on five ranges extending from 1 Ω to 50 MΩ.
4. *Alternating voltage* on ten ranges from 0 to 1 V through 0 to 1000 V.
5. *Alternating current* on ten ranges from 0 to 1 mA through 0 to 1 A.

The terminals marked + and − are those normally employed for all voltage, current, and resistance measurements. The 10-A DC terminal is used as the + terminal when dc levels ranging from 1 A to 10 A are to be measured. The − terminal is the other terminal of the instrument in this circumstance. For ac measurements between 1 A and 10 A, the 10-A AC terminal and the − terminal are employed. Similarly, for measurement of voltages between 1000 V and 2500 V, the − terminal and either the 2500-V DC terminal or the 2500-V AC terminal are used. The current and voltage ranges of the VOM can be further extended by the use of externally connected shunts and high voltage adapters.

The instrument illustrated in Figure 3-5 is equipped with an overload protection circuit. When current in the meter exceeds a maximum safe level, the overload device open-circuits the instrument internally, and the CUT-OUT RESET button pops up. The circuitry is reset by pushing the CUT-OUT button down. A REVERSE METER control also appears on the front panel illustrated. This is useful when a dc current or voltage is not connected with the correct polarity. Pushing (and holding) the REVERSE METER button reverses the meter polarity, so that a positive (i.e., right of zero) deflection is obtained. Instead of this control, some instruments have a function switch with dc + and dc − positions. Polarity reversal is obtained by switching between these two positions.

The mechanical zero control, or zero-position-control (see Section 1-2), is a recessed slotted control for screwdriver adjustment of the pointer zero position when the meter is not connected. The *zero-ohm* control used with the ohmmeter function is adjusted until the pointer indicates exactly zero on the resistance scale (i.e., right-hand side).

The multifunction instrument in Figure 3-5 has a knife-edge pointer and mirror scale to avoid parallax error (see Section 1-6-2). The top scale is employed only for resistance measurements. When the $R \times 1$ range is selected, the indicated resistance is read directly in ohms. On all other ranges the scale reading must be multiplied by the appropriate factor. For example, on the $R \times 10$ range, all scale readings (in ohms) should be multiplied by 10. The scale marked 0 to 25 is used on all current and voltage ranges which are a multiple of 25. On the 25-V range or the 25-mA range, this scale is read directly in volts or milliamps. On the 2.5-V range, FSD represents 2.5 V; thus all readings must be divided by 10. When set to the 250-V range all readings (on the 0 to 25 range) must be multiplied by 10. Similarly, the 0 to 10 and 0 to 50 scales must be multiplied by a factor appropriate to range selection.

Typical VOM measurement accuracies are 2% of full scale on dc voltage and current ranges, 2% of full scale on ac current ranges, and 3% of full scale on ac voltage ranges. The instrument can be used for ac measurements up to a frequency of about 100 kHz. Beyond that frequency, internal capacitance and inductance effects add increasing errors.

As well as resistance, voltage, and current scales, the instrument in Figure 3-5 has a decibel (dB) scale, a CAP (capacitance) scale, and an IND (inductance) scale. The use of the decibel scale is explained in Section 3-7, and capacitance and inductance measurements by the VOM are discussed in Section 3-8.

3-5 USING THE VOM AS AN AMMETER

dc Ammeter

1. Set the function switch to the *dc current* position—DC mA on the instrument in Figure 3-5.

2. If necessary, adjust the mechanical zero control to set the pointer exactly at zero on the scale. Tap the instrument gently to relieve friction when zeroing.
3. Set the range switch to its highest current position.
4. Connect the instrument in series with the circuit or component in which current is to be measured. Connection polarity should be such that (conventional) current direction is into the positive terminal and out of the negative terminal.
5. Adjust the range switch to give the greatest possible on-scale deflection.
6. Tap the instrument gently to relieve friction when reading the pointer position.

ac Ammeter

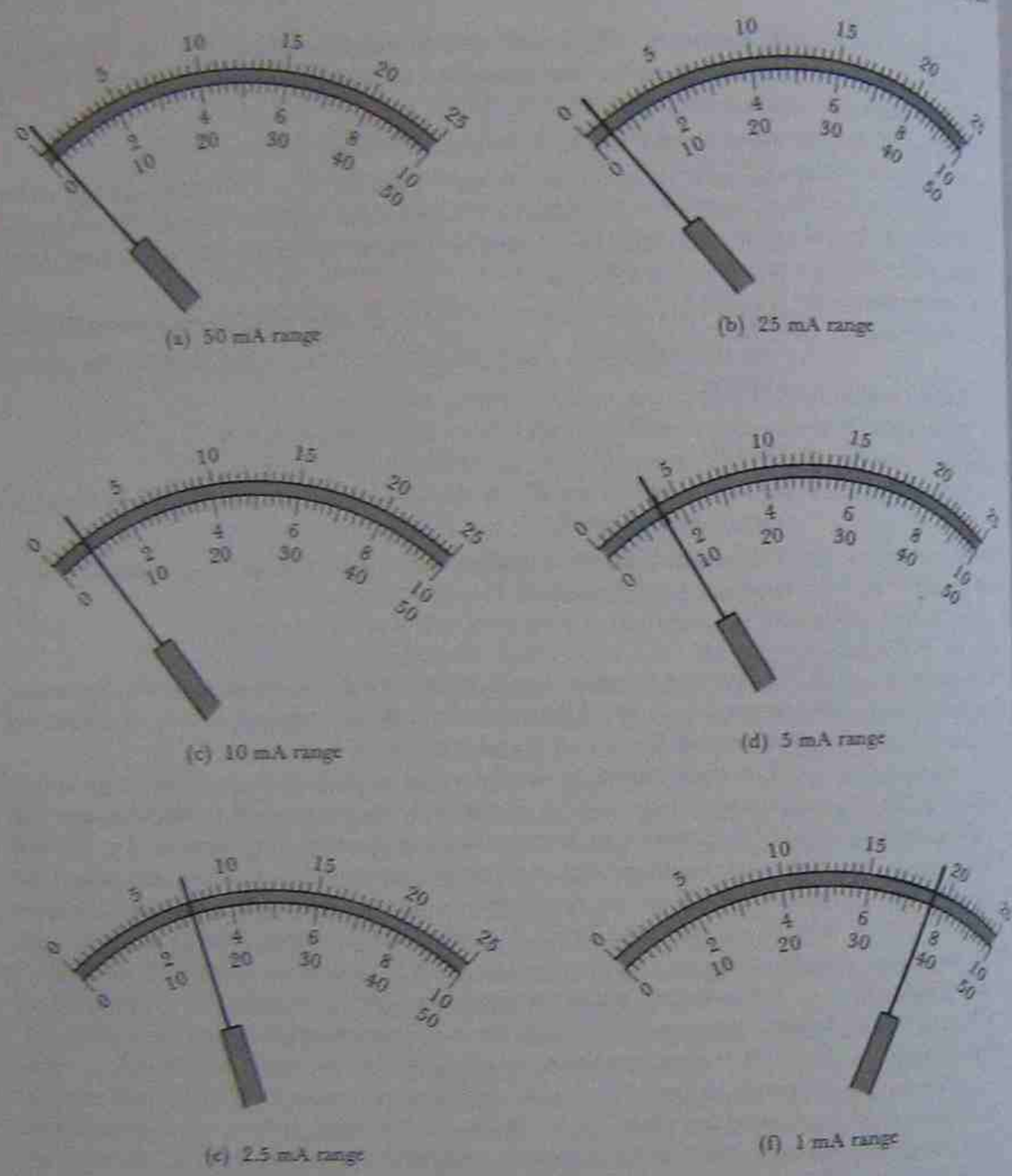
1. Set the function switch to the ac current position—AC mA on the instrument in Figure 3-5.
2. Continue as for a dc ammeter, with the exception that terminal polarity need not be observed.

It is important to remember that the VOM uses rectifiers when measuring ac quantities. It is calibrated to indicate the rms value only of sinusoidal quantities (see Sections 2-3 and 2-4).

The requirement to set the meter to its highest possible range before connecting it into a circuit is obviously to prevent instrument damage that could be caused by excessive voltage or current. For example, if a 100-mA current is passed through the instrument when it is set at a 1-mA range, the pointer would be deflected very rapidly beyond full scale, and it would almost certainly be bent. A continuous excessive flow of current may generate enough heat to destroy the thin insulation on the coil winding.

For accurate measurement of voltage or current, it is necessary to adjust the range switch until the maximum on-scale deflection is obtained. Figure 3-6 illustrates the effect of measuring a current of 0.76 mA on each of several ranges. On the 50- and 25-mA ranges, the pointer indication is something less than 1 mA. On the 10-mA range, the reading appears to be 0.8 mA. The 5-mA range gives a slightly more accurate indication between 0.7 and 0.8 mA. The 2.5-mA range is even better with the pointer showing just about 0.75 mA on the scale. Most accurate of all, the 1-mA range shows the current measurement as 0.76 mA.

The most accurate measurement is obviously made on the range that gives the greatest on-scale deflection. This is true for both ammeter and voltmeter applications of the VOM (ac or dc). It is *not* true when using the VOM as an ohmmeter. Greatest ohmmeter accuracy is obtained when the pointer is closest to $\frac{1}{2}$ FSD (see Section 3-3).



(a) 50 mA range (b) 25 mA range

(c) 10 mA range (d) 5 mA range

(e) 2.5 mA range (f) 1 mA range

FIGURE 3-6. 0.76 mA indicated on each of several ranges.

3-6 USING THE VOM AS A VOLTMETER

dc Voltmeter

1. Set the function switch to the dc *voltage* position—DC V on the instrument in Figure 3-5.
2. If necessary, adjust the mechanical zero control to set the pointer exactly at zero on the scale. Tap the instrument gently to relieve friction when zeroing.

3. Set the range switch to its highest voltage position.
4. Connect the instrument *in parallel* with the circuit or component which is to have its voltage measured. The positive (+) terminal of the voltmeter should be connected to the most positive of the two points at which voltage is to be measured. The negative (−) voltmeter terminal is connected to the most negative of the two points.
5. Adjust the range switch to give the greatest on-scale deflection.
6. Tap the instrument gently to relieve friction when reading the pointer position.

ac voltmeter

1. Set the function switch to the ac voltage position—AC V in Figure 3-5.
2. Continue as for a dc voltmeter, with the exception that terminal polarity need not be observed.

As for ac current measurements, it is important to remember that the VOM uses rectifiers when measuring ac voltages. It is accurate only for purely sinusoidal ac quantities (see Sections 2-3 and 2-4).

The reasons why the instrument should be initially set to its highest range and then adjusted to obtain maximum deflection are explained in Section 3-5.

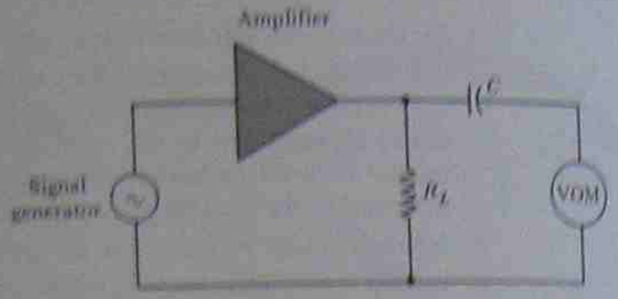
When using the instrument illustrated in Figure 3-5 as a dc voltmeter, its sensitivity is 20 000 Ω/V. This is printed on the lower left-hand side of the scale as 20 000 o.p.v DC. As discussed in Section 2-2-4, the total resistance of the voltmeter is calculated as resistance = sensitivity × range. Thus, on a 5-V range, the total resistance of the instrument is 20 kΩ/V × 5 V = 100 kΩ.

As an ac voltmeter, the instrument sensitivity is 2000 Ω/V (see Figure 3-5). For this particular instrument, the manufacturer's specification states that the sensitivity of 2000 Ω/V applies only to ac ranges of 25 V and above. On the 10-V ac range the sensitivity is 200 Ω/V. On the 5- and 2.5-V ac ranges the sensitivity is 100 Ω/V, and the 1-V ac range has a sensitivity of only 40 Ω/V. Obviously, it is important to check the manufacturer's specification on an instrument before calculating its resistance from the sensitivity figure printed on the scale.

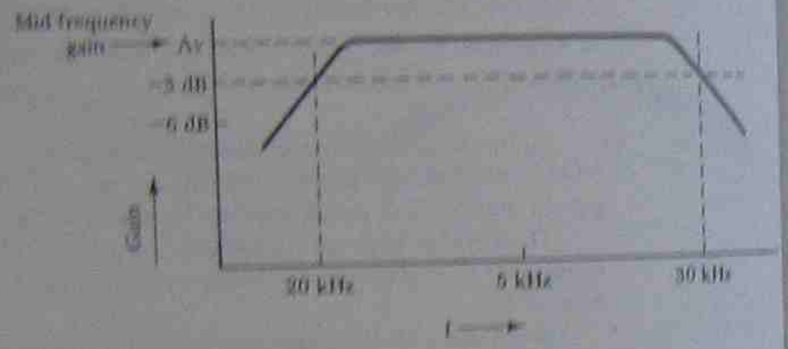
The importance of voltmeter resistance is explained in Section 2-2-4.

3-7 DECIBEL MEASUREMENT BY VOM

The decibel scale on a VOM is employed typically to monitor the output power of an audio amplifier. The VOM is set to its ac voltage function and to the highest possible range before connecting it to the amplifier. A capacitor must be connected in series with one terminal of the instrument to isolate it from any dc voltage that may be present at the amplifier output [see Figure 3-7(a)]. The range is progressively switched lower until a suitably large on-scale deflection is obtained. Amplifier power output



(a) Circuit for testing amplifier frequency response



(b) Typical audio amplifier frequency response

FIGURE 3-7. Use of a VOM for audio amplifier testing.

measurements are made for various input frequencies with the input amplitude maintained constant. A plot of output power versus frequency gives the amplifier frequence response graph [Figure 3-7(b)].

The dB scale on the instrument in Figure 3-5 is based upon the 10-V ac scale and upon the voltage developed across a 600-Ω load. Zero dB is taken as 1 mW dissipated into 600 Ω. Thus, if R_L in Figure 3-7 is 600 Ω, the voltage developed across R_L when 1 mW is dissipated can be calculated:

$$P = V^2/R_L$$

or

$$V = \sqrt{PR_L}$$
$$= \sqrt{1\text{ mW} \times 600\ \Omega}$$
$$= 0.775\text{ V}.$$

Referring to Figure 3-5, it is seen that when the pointer indicates 0 dB it also extends over the 0.775-V position on the 10-V ac scale.

The dB scale on the VOM in Figure 3-5 may be read directly only when the instrument is set to its 10-V ac range, and when $R_L = 600\ \Omega$. Where another voltage range is employed, an appropriate dB quantity must be added to *each* reading. For example, suppose a reading is taken on the 50-V range. The dB quantity that must be added is determined simply from the dB ratio of 50 to 10 V:

$$\textit{for 50-V range, add}\left(20\log_{10}\frac{50\text{ V}}{10\text{ V}} = 14\text{ dB}\right).$$

If the 25-V range is used, the quantity to be added is calculated similarly:

$$\textit{for 25-V range, add}\left(20\log_{10}\frac{25\text{ V}}{10\text{ V}} = 8\text{ dB}\right).$$

For the dB scale on the instrument in Figure 3-5, the value of R_L (as already stated) is 600 Ω. Where the load resistance is other than 600 Ω the actual dB levels indicated are not correct. A correction factor can be calculated for the particular load resistance value employed; however, usually this is not necessary. Usually, it is only the *changes* in output power of an amplifier (or other piece of equipment) that are monitored, rather than the absolute values. The dB changes (as the signal frequency is altered) can be read directly from the dB scale without any consideration of the actual value of R_L. Suppose the indicated output of the amplifier is 15 dB (on any scale) when the signal frequency is 5 kHz. Then, when the signal frequency is 30 kHz, the output power on the same scale as before may have fallen to 12 dB. The power output at 30 kHz can now be plotted as 3 dB below the output at 5 kHz [see Figure 3-7(b)].

To avoid measurement errors, the impedance of the capacitor employed to couple the amplifier output to the VOM must be very much smaller than the VOM impedance. This is because the amplifier output is potentially divided across the capacitor and the VOM. If the capacitor value is calculated at the lowest signal frequency, its impedance will be negligible at all other frequencies.

A VOM can be used in the manner described for testing audio amplifiers because most VOMs can accurately measure sinusoidal voltages up to a maximum frequency of 100 kHz. This is well beyond the highest frequency that any audio amplifier might be expected to process. Obviously, amplifiers which operate at frequencies in excess of 100 kHz cannot be tested by a VOM.

When there is no decibel scale on a VOM, the ac voltage ranges of the instrument can be used for dB measurements. Example 3-7 demonstrates the procedure.

EXAMPLE 3-7 A VOM is to be used for determining the power output and frequency response of an amplifier, as in Figure 3-7. The amplifier load resistance is 160 Ω, the output voltage is 24 V at 5 kHz, and the frequency range is 30 Hz to 30 kHz. For the VOM shown in Figure 3-5, determine the minimum size of coupling capacitor that must be used. Also, calculate the amplifier power output at 5 kHz, and the indicated voltage when the output is 1 dB below that at 5 kHz.

SOLUTION

Using the 25-V ac range of the VOM, *its resistance is:*

$$\begin{aligned} R_v &= \textit{Range} \times \textit{sensitivity} \\ &= 25\ \text{V} \times 2000\ \Omega/\text{V} \\ &= 50\ \text{k}\Omega. \end{aligned}$$

Let $X_c = R_v/10$ at $f = 30$ Hz:

$$X_c = \frac{1}{2\pi fC} = \frac{R_v}{10}$$

or,
$$C = \frac{1}{2\pi f \times R_v/10}$$

$$= \frac{1}{2\pi \times 30\ \text{Hz} \times 50\ \text{k}\Omega/10}$$

$$= 1.06\ \mu\text{F (use a 1-}\mu\text{F standard value).}$$

At 5 kHz:

$$P_o = \frac{V_L^2}{R_L} = \frac{(24\ \text{V})^2}{160\ \Omega}$$

$$= 3.6\ \text{W}.$$

At −1 dB *from* 3.6 W:

$$-1\ \text{dB} = 20 \log_{10} \frac{V_2}{V_1},$$

$$\text{or } \frac{V_2}{V_1} = \text{antilog}\left(\frac{-1}{20}\right),$$

$$V_2 = V_1 \text{antilog}\left(\frac{-1}{20}\right)$$

$$= 24\ \text{V} \times 0.89$$

$$= 21.39\ \text{V}.$$

3-8 VOM ADAPTERS AND PROBES

Volt-ohm-milliammeter applications can be extended by the use of adapters and probes. Some of these are:

ADAPTER FOR MEASURING INDUCTANCE (L) AND CAPACITANCE (C). This is a piece of equipment which applies an ac voltage or current to the inductor or capacitor under test. The impedance of the component is measured in terms of its voltage drop or in terms of the current flow. The circuitry of this LC adapter can be similar to that discussed in Section 10-10.

RADIO FREQUENCY PROBE. The voltage level of a radio frequency (RF) signal cannot be measured directly on a VOM because the upper frequency limit of the VOM is far below radio frequency. In an RF probe, the radio frequency voltage is rectified and converted to a dc quantity equal to the peak level of the signal. The dc voltage produces meter deflection and can be read from a scale calibrated to indicate rms values. *Peak detector probes* are discussed further in Section 8-9-2.

HIGH VOLTAGE PROBE. This is essentially a suitably insulated potential divider which reduces the high voltage down to a level that can be safely measured on the VOM.

REVIEW QUESTIONS AND PROBLEMS

3-1. Sketch the circuit of a multirange series ohmmeter. Explain the operation of the circuit, and discuss the purpose of each component.

3-2. Calculate the range of resistance that may be measured by an ohmmeter which has the following components: supply voltage $E_B = 3$ V, series resistor $R_1 = 30$ kΩ, meter shunt resistor $R_2 = 50$ Ω, meter FSD = 50 μA, and meter resistance $R_m = 50$ Ω. Draw a scale for the instrument, showing the values of resistance at 0, $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{3}{4}$ of FSD.

3-3. A series ohmmeter has a standard internal resistance R_1 of 50 kΩ and uses a meter with FSD = 75 μA and $R_m = 100$ Ω. The meter shunt resistance is $R_2 = 300$ Ω, and the battery voltage is 5 V. Draw a scale for the instrument showing the resistance measured at: 0, 25%, 50%, 75%, and 100% of FSD.

3-4. For the circuit in Question 3-2, determine the new value to which R_2 must be adjusted when E_B falls to 2.5 V. Also, determine the measured resistance at $\frac{1}{2}$ and $\frac{3}{4}$ of full scale.

3-5. If the deflection meter in Question 3-2 has an accuracy of ±2% of full scale, calculate the accuracy of resistance measurements at $\frac{1}{4}$ and $\frac{3}{4}$ of full scale.

3-6. Design a series ohmmeter circuit to have a range of 1 kΩ to 100 kΩ. The available meter has $I_m = 100\ \mu A$ at full scale and $R_m = 100\ \Omega$. The battery to be used has $E_B = 4.5$ V.

3-7. Calculate the meter current and the indicated resistance for the ohmmeter circuit in Figure 3-3(a) on its $R \times 10$ range: (a) when $R_x = 0$, (b) when $R_x = 500\ \Omega$, (c) when $R_x = 70\ \Omega$.

3-8. List the procedure for using the VOM in Figure 3-5 as: (a) a dc ammeter, (b) an ac ammeter. State any limitations to the use of the instrument on its ac ranges.

3-9. List the procedure for using the VOM in Figure 3-5 as: (a) a dc voltmeter, (b) an ac voltmeter. Calculate the voltmeter resistance on its 50-V dc range and on its 250-V ac range.

3-10. A VOM is used to determine the power output and frequency response for an amplifier. The amplifier load resistance is 12 Ω, and the measured output voltage is 15 V at 8 kHz. The frequency range is determined as 50 Hz to 25 kHz. For the VOM in Figure 3-5, determine the minimum size of coupling capacitor that must be used. Also, calculate the output voltage when the output power is 1.5 dB below the level at 8 kHz.

3-11. List the probes and adapters that are available for use with a VOM. Briefly describe each device and its purpose.

4

ERRORS IN MEASUREMENTS

INTRODUCTION No electronic component or instrument is perfectly accurate; all have some error or inaccuracy. It is important to understand how these errors are specified, and how they combine to create even greater errors in measurement systems. Although it is possible that in some cases errors might almost completely cancel each other out, the worst case combination of errors must always be assumed.

Apart from equipment errors, some operator or observer error is inevitable. Also, even when equipment errors are very small, the system of using the instruments can introduce a *systematic error*. Errors of unexplainable origin are classified as *random errors*. Where accuracy is extremely important, some errors can be minimized by taking many readings of each instrument and determining mean values.

4-1 ABSOLUTE AND RELATIVE ERRORS

If a resistor is known to be 100 Ω and has a possible error of ±10 Ω the ±10 Ω is an *absolute error*. The error may be expressed as a percentage, or sometimes as a fraction, of the total resistance. In this case it becomes a *relative error*.

Expressing the error relative to the total resistance, 10 Ω can be stated as 1/10 of 100 Ω or as 10% of 100 Ω. Thus the resistance could be written as

$$100\ \Omega \pm 1/10 \quad \text{or} \quad 100\ \Omega \pm 10\%.$$

Percentages are usually employed to express errors in resistances and other electrical quantities. The terms *accuracy* and *tolerance* are also used, particularly when referring to resistor errors. A resistor with a possible error of $\pm 10\%$ is said to be *accurate to* $\pm 10\%$. Alternatively, the resistor may be said to be constructed to be 100 Ω with a *tolerance of* $\pm 10\%$. Tolerance is the term usually employed by component manufacturers.

When a voltage is measured as 100 V using an instrument which is known to have an error of ± 1 V, the voltage measurement is usually said to be accurate to $\pm 1\%$, meaning that there is a possible error of $\pm 1\%$ in the measured 100 V.

Another method of expressing an error is to refer to it in *parts per million* relative to the total quantity. For example, the temperature coefficient of a resistor may be stated as 100 parts per million per degree Celsius, usually written 100 PPM/°C. Suppose a 1-MΩ resistance is involved. One millionth of 1 MΩ is 1 Ω; consequently, 100 PPM of 1 MΩ is 100 Ω. Therefore, a 1-MΩ resistor with a temperature coefficient of ± 100 PPM/°C increases or decreases in resistance by 100 Ω for each 1°C change in temperature.

EXAMPLE 4-1 A component manufacturer constructs certain resistances to be anywhere between 1.14 kΩ and 1.26 kΩ and classifies them to be 1.2 kΩ resistors. What tolerance should be stated? If the resistance values are specified at 25°C and the resistors have a temperature coefficient of +500 PPM/°C, calculate the maximum resistance that one of these components might have at 75°C.

SOLUTION

$$\textit{absolute error} = 1.26\ \text{k}\Omega - 1.2\ \text{k}\Omega = +0.06\ \text{k}\Omega$$

or

$$= 1.2\ \text{k}\Omega - 1.14\ \text{k}\Omega = -0.06\ \text{k}\Omega$$

$$= \pm 0.06\ \text{k}\Omega$$

$$\textit{tolerance} = \frac{\pm 0.06\ \text{k}\Omega}{1.2\ \text{k}\Omega} \times 100\%$$

$$= \pm 5\%$$

Largest possible resistance at 25°C:

$$R = 1.2\ \text{k}\Omega + 0.06\ \text{k}\Omega$$

$$= 1.26\ \text{k}\Omega,$$

Resistance change per °C:

$$500\ \text{PPM of}\ R = \frac{1.26\ \text{k}\Omega}{1\,000\,000} \times 500$$

$$= 0.63\ \Omega/°\text{C}.$$

Temperature increase:

$$\Delta T = 75°\text{C} - 25°\text{C}$$

$$= 50°\text{C}.$$

Total resistance increase:

$$\Delta R = 0.63\ \Omega/°\text{C} \times 50°\text{C}$$

$$= 31.5\ \Omega.$$

Maximum resistance at 75°C:

$$R + \Delta R = 1.26\ \text{k}\Omega + 31.5\ \Omega$$

$$= 1.2915\ \text{k}\Omega.$$

4-2 OBSERVER ERRORS

Perhaps the most common observer error is a simple misreading of the exact pointer position on a deflection instrument. Even when a mirror-scale and knife-edge pointer are provided, two observers may disagree about the precise position of the pointer.

A more serious observer error occurs when an operator reads the pointer position on the wrong scale of a multiscale instrument. Sometimes a meter is read correctly, but the reading is incorrectly recorded, or perhaps recorded in a wrong column. Everyone makes these kinds of mistakes at some time or other. Obviously, they can be avoided only by carefully using and reading all instruments and by thinking about whether or not each reading makes sense. Substituting instrument readings into an appropriate equation, or plotting a few points of a graph that is to eventually be drawn, also helps to check the validity of recorded quantities while measurements are still in progress.

4-3 ACCURACY, PRECISION, AND RESOLUTION

Suppose an ammeter with an error of $\pm 1\%$ of full scale indicates exactly 1 A at full scale. The true value of the measured current is somewhere between 1 A − 1% and 1 A + 1%, i.e., between 0.99 and 1.01 A. Thus, the measurement *accuracy* of $\pm 1\%$ defines how close the measurement is to true value.

Precision is something different from accuracy, although accuracy and precision are related. When an instrument has a mirror-scale and a knife-edge pointer, the pointer position may be read very precisely. For example, on the 10-V scale in Figure 3-5 the pointer position can be read to within perhaps one-fourth of the smallest scale division. On the 10-V range, the smallest scale division represents 0.2 V. Therefore, in this case the voltage could be measured to within 0.2 V/4 or 0.05 V. This (0.05 V)

refers to the precision of the measurement; however, it does not take the instrument accuracy into account.

Suppose the voltmeter has a specified accuracy of ±2%, relating to the actual PMMC instrument and to the internal multiplier resistors. Then, if a potential difference of 10 V were measured to a precision of 0.05 V, the measurement would still be accurate to ±2% of 10 V, i.e., to ±0.2 V.

When an instrument such as the one discussed above has not been calibrated for some time, its accuracy may be worse than the specified ±2%. Worse still, an instrument that was not correctly zeroed before use may give an even greater error, although its pointer position may be read just as precisely as ever. Clearly, there is little value in precise readings of incorrect quantities.

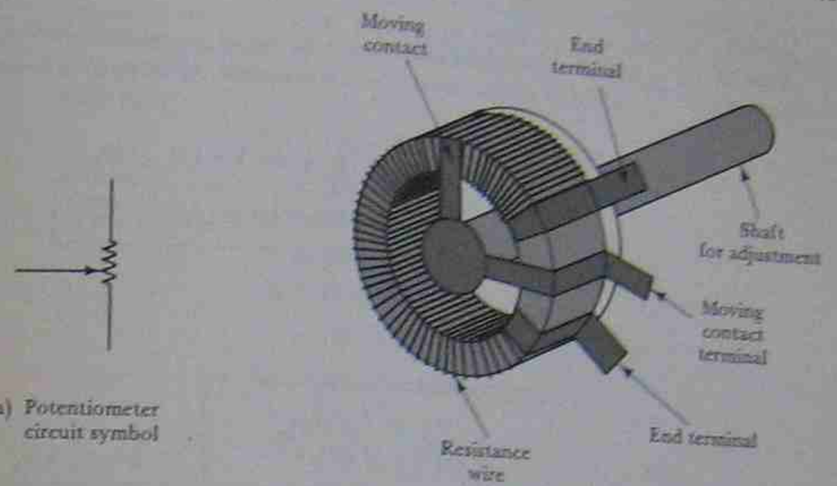
It is seen that precise measurements may not always be accurate measurements, although precision is necessary for accuracy.

Resolution is related to precision, and, consequently, it is also related to accuracy. In the case of the 10-V instrument scale that could be read to 0.05 V, it might be stated that the resolution of the scale is 0.05 V. Another way of stating the same things is to say that a voltage *change* of 0.05 V can be observed. If this is so, then it might also be said that the voltmeter is *sensitive* to a voltage change of 0.05 V, although voltmeter sensitivity is something else (see Section 2-2-4).

Consider the *potentiometer* illustrated in Figure 4-1. The circuit symbol in Figure 4-1(a) illustrates a resistor with two terminals and a contact which can be moved anywhere between the two. The construction shown in Figure 4-1(b) reveals that the movable contact slides over a track on one side of a number of turns of resistance wire. The contact does not slide along the whole length of the wire but *jumps* from one point on one turn of the wire to a point on the next turn. Suppose the total potentiometer resistance is 100 Ω and further assume that there are 1000 turns of wire. Each turn has a resistance of

$$\frac{100\ \Omega}{1000} = 0.1\ \Omega.$$

When the contact moves from one turn to the next, the resistance from any end to the moving contact changes by 0.1 Ω. It can now be stated that the resistance from one end to the moving contact can be adjusted from 0 to 100 Ω with a *resolution* of 0.1 Ω, or a resolution of 1 in 1000. In the case of the potentiometer, the resolution defines how precisely the resistance may be set. It also defines how precisely the variable voltage from the potentiometer moving contact may be adjusted when a potential difference is applied across the potentiometer.



(a) Potentiometer circuit symbol

(b) Potentiometer construction

FIGURE 4-1. Potentiometer circuit symbol and construction.

4-4 SYSTEMATIC ERRORS

Errors which are due to the measurement system used, or which are due to instrument inaccuracy, are defined as *systematic errors*. For example, when a voltmeter is used to measure the potential difference between two points in a circuit, the voltmeter loading effect (see Section 2-2-4) may alter the voltage. This is a systematic error. Similarly, an ammeter resistance may alter the level of a current and thus introduce a systematic error.

Errors due to the specified accuracy of instruments are also systematic errors, as are errors due to incorrect calibration or neglect in zeroing the instrument before use. Additional systematic errors can result from instrument inaccuracies due to temperature extremes, excess humidity, and stray electric or magnetic fields.

Some systematic errors obviously cannot be avoided. Others can be minimized by careful use of instruments, and by such precautions as the use of a high resistance voltmeter where voltmeter loading may occur, i.e., by planning. Where more than one measurement is made, or where more than one instrument is involved, the errors due to instrument inaccuracy tend to accumulate. The overall measurement error is then usually larger than the error in any one instrument. When estimating the effect of errors due to more than one source, it should always be assumed that the errors combine in the worst possible way.

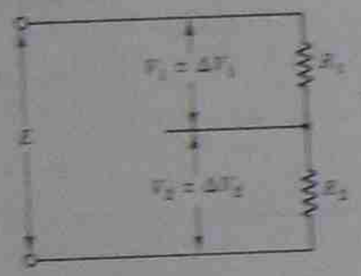
4-4-1 Sum of Quantities

Where a quantity is determined as the sum of two measurements, the total error is the sum of the absolute errors in each measurement. As illustrated in Figure 4-2(a),

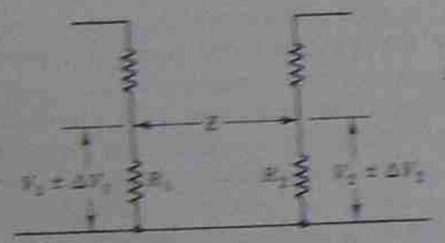
$$E = (V_1 \pm \Delta V_1) + (V_2 \pm \Delta V_2),$$

giving

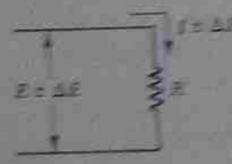
$$\boxed{E = (V_1 + V_2) \pm (\Delta V_1 + \Delta V_2).} \tag{4-1}$$



(a) Error in sum of quantities equals sum of errors



(b) Error in difference of quantities equals sum of errors



(c) Percentage error in product or quotient of quantities equals sum of percentage errors

FIGURE 4-2 Errors in sum, difference, product, and quotient of quantities

EXAMPLE 4-2 Calculate the maximum percentage error in the sum of two voltage measurements when $V_1 = 100\text{ V} \pm 1\%$ and $V_2 = 80\text{ V} \pm 5\%$.

SOLUTION

$$\begin{aligned}
V_1 &= 100\text{ V} \pm 1\% \\
&= 100\text{ V} \pm 1\text{ V}, \\
V_2 &= 80\text{ V} \pm 5\% \\
&= 80\text{ V} \pm 4\text{ V}, \\
E &= V_1 + V_2 \\
&= (100\text{ V} \pm 1\text{ V}) + (80\text{ V} \pm 4\text{ V}) \\
&= 180\text{ V} \pm (1\text{ V} + 4\text{ V}) \\
&= 180\text{ V} \pm 5\text{ V} \\
&= 180\text{ V} \pm 2.8\%.
\end{aligned}$$

In the above example, note that *the percentage error in the final quantity cannot be calculated directly from the percentage errors in the two measured quantities.*

Where more than two measured quantities are summed to determine a final quantity, the absolute values of the errors must again be summed to find the total possible error.

4-4-2 Difference of Quantities

Figure 4-2(b) illustrates a situation in which a potential difference is determined as the *difference* between two measured voltages. Here again, *the errors are additive:*

$$\begin{aligned}
E &= V_1 - V_2 \\
&= (V_1 \pm \Delta V_1) - (V_2 \pm \Delta V_2)
\end{aligned}$$

$$\boxed{E = (V_1 - V_2) \pm (\Delta V_1 + \Delta V_2).} \tag{4-2}$$

EXAMPLE 4-3 Calculate the maximum percentage error in the difference of two measured voltages, when $V_1 = 100\text{ V} \pm 1\%$ and $V_2 = 80\text{ V} \pm 5\%$.

SOLUTION

$$\left.\begin{aligned} V_1 &= 100\text{ V} \pm 1\text{ V} \\ \text{and}\quad V_2 &= 80\text{ V} \pm 4\text{ V} \end{aligned}\right\} \text{(as in Example 4-2)},$$

$$\begin{aligned}
E &= (100\text{ V} \pm 1\text{ V}) - (80\text{ V} \pm 4\text{ V}) \\
&= 20\text{ V} \pm 5\text{ V} \\
&= 20\text{ V} \pm 25\%.
\end{aligned}$$

Example 4-3 demonstrates that *the percentage error in the difference of two quantities can be very large*. If the difference was smaller, the percentage error would be even larger. Obviously, measurement systems involving the difference of two quantities should be avoided.

4-4-3 Product of Quantities

When a calculated quantity is the product of two or more quantities, *the percentage error is the sum of the percentage errors in each quantity* [consider Figure 4-2(c)]:

$$\begin{aligned} P &= EI \\ &= (E \pm \Delta E)(I \pm \Delta I) \\ &= EI \pm E\Delta I \pm I\Delta E \pm \Delta E\Delta I. \end{aligned}$$

Since $\Delta E\,\Delta I$ is very small,

$$P = EI \pm (E\Delta I + I\Delta E),$$

$$\text{percentage error} = \frac{E\Delta I + I\Delta E}{EI} \times 100\%$$

$$= \left(\frac{E\Delta I}{EI} + \frac{I\Delta E}{EI}\right) \times 100\%$$

$$= \left(\frac{\Delta I}{I} + \frac{\Delta E}{E}\right) \times 100\%:$$

$$\boxed{\%\ \text{error in } P = (\%\ \text{error in } I) + (\%\ \text{error in } E).} \tag{4-3}$$

Thus, when a voltage is measured with an accuracy of $\pm 1\%$, and a current is measured with an accuracy of $\pm 2\%$, the calculated power has an accuracy of $\pm 3\%$.

4-4-4 Quotient of Quantities

Here again it can be shown that the percentage error is the sum of the percentage errors in each quantity. In Figure 4-2(c):

$$\boxed{\%\ \text{error in } E/I = (\%\ \text{error in } E) + (\%\ \text{error in } I).} \tag{4-4}$$

4-4-5 Quantity Raised to a Power

When a quantity A is raised to a power B, the percentage error in A^B can be shown to be:

$$\boxed{\%\ \text{error} = B(\%\ \text{error in } A).} \tag{4-5}$$

For a current I with an accuracy of $\pm 3\%$, the error in I^2 is $2(\pm 3\%) = \pm 6\%$

EXAMPLE 4-4 An 820-Ω resistance with an accuracy of ±10% carries a current of 10 mA. The current was measured by an ammeter on a 25-mA range with an accuracy of ±2% of full scale. Calculate the power dissipated in the resistor, and determine the accuracy of the result.

SOLUTION

$$\begin{aligned} P &= I^2R, \\ P &= (10\text{ mA})^2 \times 820\ \Omega \\ &= 82\text{ mW}, \\ \text{error in } R &= \pm 10\%, \\ \text{error in } I &= \pm 2\% \text{ of } 25\text{ mA} \\ &= \pm 0.5\text{ mA} \\ &= \frac{\pm 0.5\text{ mA}}{10\text{ mA}} \times 100\% \\ &= \pm 5\%, \\ \%\ \text{error in } I^2 &= 2(\pm 5\%) \\ &= \pm 10\%, \\ \%\ \text{error in } P &= (\%\ \text{error in } I^2) + (\%\ \text{error in } R) \\ &= \pm(10\% + 10\%) \\ &= \pm 20\%. \end{aligned}$$

4-4-6 Summary

For $X = A \pm B$,

$$\text{error in } X = \pm\,[(\text{error in } A) + (\text{error in } B)].$$

For $X = AB$,

$$\%\ \text{error in } X = \pm\,[(\%\ \text{error in } A) + (\%\ \text{error in } B)].$$

For $X = A/B$,

$$\%\ \text{error in } X = \pm\,[(\%\ \text{error in } A) + (\%\ \text{error in } B)].$$

For $X = A^B$,

$$\%\ \text{error in } X = \pm B(\%\ \text{error in } A).$$

4-5 RANDOM ERRORS

Random errors are the result of chance or accidental events. They may be human errors caused by fatigue. They may also be produced by such occurrences as a surge in ac supply voltage, a brief draft upon equipment, or a variation in frequency. Whenever a particular measurement is very

important, the random errors may be almost completely eliminated by taking a large number of readings and finding the mean value.

When determining the mean value of a number of readings, it is sometimes found that one or two measurements differ from the mean by a much larger amount than all of the others. In this case, it is justifiable to assume that these few readings are due to mistakes rather than random errors. Such readings may be rejected, and the average value calculated from the other measurements. This action can be taken only where there are a few readings which seem in serious error when compared to many other measurements. Where more than a small number of measurements differ greatly from the mean value, the experimental conditions are likely to have been unsatisfactory, and the whole series of readings should be repeated.

When the mean value of a large number of measurements is calculated, statistical analysis methods may be applied to determine the *probable error* in the result. However, even when this is done and a very small probable error is determined, the systematic error is not altered. The systematic error (or maximum possible error) in the result is still dependent upon the accuracy of equipment and upon the measurement system employed.

REVIEW QUESTIONS AND PROBLEMS

4-1. A batch of resistors with nominal values of 330 Ω are to be tested and classified into ±5% and ±10% components. Calculate the maximum and minimum absolute resistances in each case.

4-2. The resistors in Question 4-1 are specified at 25°C, and their temperature coefficient is −300 PPM/°C. Calculate the maximum and minimum resistance that one of these components might have at 100°C.

4-3. A 1-kΩ potentiometer, which has a resolution of 0.5 Ω, is used as a potential divider with a 10-V supply. Determine the precision of the output voltage.

4-4. Three of the resistors referred to in Question 4-1 are connected in series. One is a ±5% component, and the other two have ±10% tolerance. Calculate the maximum and minimum values of the total resistance.

4-5. A dc power supply provides current to four electronic circuits. The currents are: 37 mA, 42 mA, 13 mA, and 6.7 mA. The first two are measured with an accuracy of ±3%, and the other two are measured with ±1% accuracy. Calculate the maximum and minimum possible current drawn from the supply.

4-6. Two currents, I_1 and I_2, from different sources flow in opposite directions through a resistor R_1. I_1 is measured as 79 mA on ammeter A_1, which is set to its 100-mA range. The accuracy of A_1 is ±3%. I_2 is measured as 31 mA on ammeter A_2 set to a 50-mA range. The accuracy of A_2 is ±1%. Determine the maximum and minimum levels of current in R_1.

4-7. A resistor R_1 has a potential of $V_1 = 12$ V (with respect to ground) applied to one of its terminals. At the other terminal, the potential is $V_2 = 5$ V. $R_1 = 470\ \Omega$ ±5%. The voltmeters monitoring V_1 and V_2 each have an accuracy of ±2%. V_1 is measured on a 25-V range, while V_2 is measured on a 5-V range. Calculate the nominal level and accuracy of the current flowing in R_1.

4-8. When a potential of 25 V is applied to a certain resistor, a current of 63 mA flows. The voltage is measured on a voltmeter with an accuracy of ±5% and set to a range of 30 V. The current is measured on an ammeter with ±1% accuracy on its 100-mA range. Calculate the value of the resistance and its tolerance.

4-9. Calculate the maximum and minimum levels of power dissipated in resistor R_1 in Question 4-7.

4-10. Calculate the maximum and minimum power dissipation in the resistor in Question 4-8.

4-11. A 12-V supply is applied to a 470 Ω resistor with a tolerance of ±10%. The supply voltage is measured on the 25-V range of a voltmeter with an accuracy of ±3%. Determine the nominal power dissipation in the resistor and state its accuracy.

5

THE dc POTENTIOMETER AND INSTRUMENT CALIBRATION

INTRODUCTION All voltmeters, ammeters, and wattmeters must be calibrated by the use of a more accurate instrument. The *dc potentiometer* is the instrument used for this purpose. The potentiometer is itself calibrated by means of a *standard cell*, which has an extremely accurate terminal voltage.

In its very basic form, the potentiometer is simply a long resistance wire passing a precisely determined current, so that the voltage drop per centimeter is accurately known. A galvanometer is employed to detect the point on the resistance wire which has a voltage equal to the voltage to be measured. The measured voltage is then determined in terms of the length of wire involved. More complex instruments employ switched resistors as well as a resistance wire, and the measured voltage is read directly from voltage scales.

5-1 STANDARD CELL

The *standard cell* (*also known as the mercury cadmium cell and as the Weston cadmium cell*) is an extremely accurate voltage cell. It is used exclusively as a voltage reference source never supplying a current greater than about 20 μA. As a voltage reference, it is an important part of the dc potentiometer.

The construction of a standard cell is illustrated in Figure 5-1. The sealed H-shaped tube contains electrolyte and has electrodes at the bottom of each leg of the tube. The positive electrode is mercury, the negative

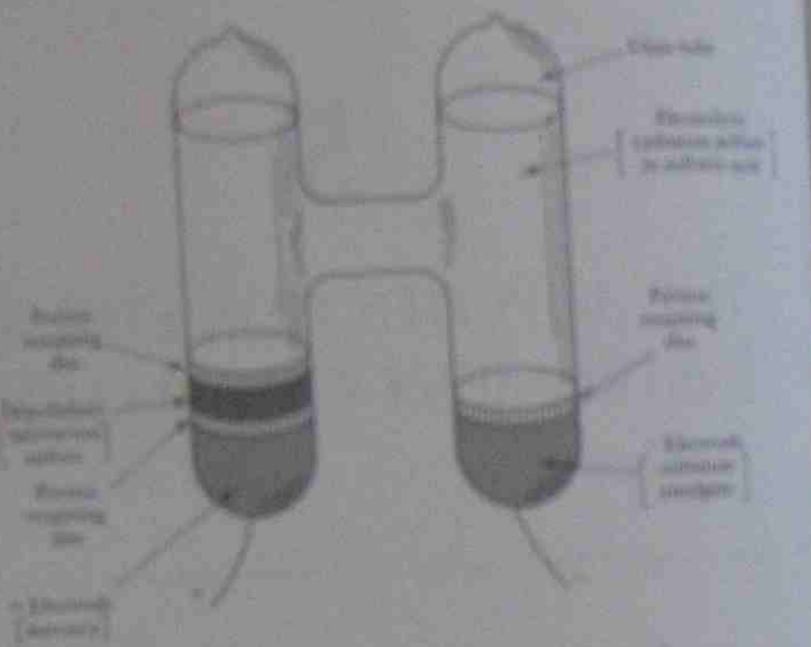


FIGURE 5-1. Mercury-cadmium standard cell.

electrode is cadmium amalgam, and the electrolyte is a solution of cadmium sulfate ($CdSO_4$). Both electrodes are held in position by porous spacers. As illustrated, the positive electrode has a layer of mercurous sulfate paste (Hg_2SO_4) which acts as a depolarizer. Another porous spacer holds the depolarizer in position. Connections to the electrodes are made by platinum wires passing through the glass tube. For laboratory use, the cell is usually contained in a protective metal enclosure with the connecting leads brought out to two terminals.

The type of standard cell shown in Figure 5-1 has a nominal voltage ranging from 1.0180 to 1.0200 V. When correctly constructed by different people working to the same specification, the cell terminal voltages differ by only microvolts. The actual terminal voltage of a given cell is usually specified by the manufacturer. The cell has a temperature coefficient of around 5 μV/°C, and, when carefully treated, its terminal voltage drops by approximately 30 μV per year. Thus, a standard cell is an accurate reliable voltage reference source.

The standard cell described above is referred to as an *unsaturated cell*. It distinguishes it from an even more accurate *saturated cell* (or *normal cell*) usually found in standards laboratories. The saturated cell has an electrolyte which is saturated with cadmium, and includes cadmium sulfate crystals to keep it saturated. Its terminal voltage is 1.01865 V. To maintain

this extremely accurate terminal voltage, the saturated cell must be treated so carefully that it is impractical for use outside a standards laboratory environment.

The standard cell is strictly a potential device. A current of only 100 μA drawn from the cell for a few minutes can cause a slight drop in cell terminal voltage. The cell may take several hours to recover from this. Usually, it is best to include a resistance in series with the terminals to limit the maximum current to 10 μA. The use of a voltmeter to measure the cell terminal voltage may cause excessive current. Any cell that is short-circuited even for a brief time is rendered useless for precise measurement applications.

Standard cells must always be used in an upright position and should be handled with care. If a cell is dropped it may be permanently damaged or destroyed. Cells should be protected from droughts and vibrations, and maintained in a temperature of 4°C to 40°C.

5-2 BASIC dc POTENTIOMETER

Figure 5-2 shows the basic circuit of a dc potentiometer. A resistance wire (AB) having a uniform resistance per unit length is placed alongside a calibrated scale such as a meter stick. A current I supplied from a battery

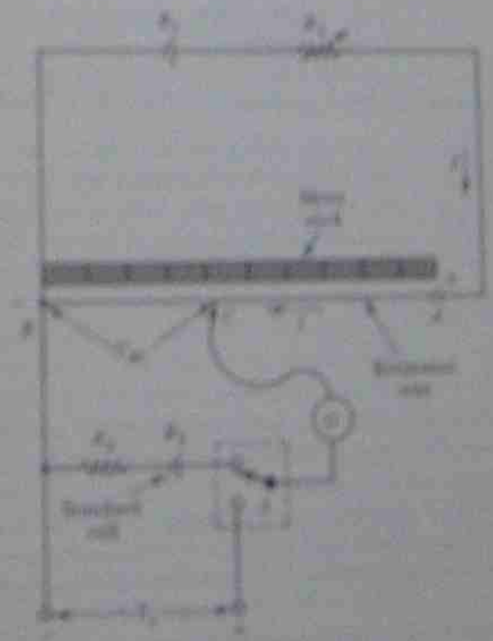


FIGURE 5-2. Basic dc potentiometer.

(B_1) flows through the wire. The current level is controlled by a variable resistance (R_1). A sensitive galvanometer (G) is connected to the resistance wire via a sliding contact (C). The other terminal of the galvanometer is connected to a switch (S), which facilitates contact to either a standard cell (B_2) or to a voltage to be measured (V_x). Resistor R_2 protects the standard cell against excessive current flow.

The potentiometer must be *calibrated* before it can be used to measure voltage. This is done by setting the switch to connect the standard cell to the galvanometer. The sliding contact is set to the position on the resistance wire (or *slide wire*) which should have a voltage exactly equal to that of the standard cell. Then, R_1 is adjusted until the galvanometer indicates zero (or null), i.e., until $V_{BC} = V_{B2}$.

Suppose the resistance wire is exactly 100 cm in length, and assume that the moving contact is set to 50.95 cm from terminal B. When R_1 is adjusted for null on the galvanometer, the voltage across the 50.95 cm is exactly equal to the standard cell voltage. With a standard cell voltage of 1.0190 V, V_{BC} equals 1.0190 V. Thus, the resistance wire now has

$$\text{voltage/unit length} = \frac{1.0190\ \text{V}}{50.95\ \text{cm}} = 20\ \text{mV/cm}.$$

When the potentiometer has been calibrated, S can be switched to V_x, then the sliding contact is adjusted to again null the galvanometer. Voltage V_x is now determined by measuring the length of wire from terminal B to the new position of C.

$$V_x = (\text{length } BC) \times 20\ \text{mV/cm}.$$

If the sliding contact can be set to an accuracy of ± 1 mm, the resolution of the instrument is the slide wire voltage per mm, i.e., (20 mV per cm)/10 = 2 mV. This is another way of saying that V_x can be measured with a precision of ± 2 mV. If there are no other sources of error, the measurement accuracy is also ± 2 mV.

The dc potentiometer measures the unknown voltage by comparing it (via the potentiometer) to the standard cell voltage. Because a galvanometer is used to detect null when calibrating, no current is drawn from the standard cell. Also, since null is again detected when measuring the unknown voltage, no current is drawn from V_x, and its open-circuit terminal voltage is accurately measured.

EXAMPLE 5-1 The resistance of wire AB in a simple dc potentiometer (as in Figure 5-2) is 100 Ω, and its length is 100 cm. Battery B_1 has a terminal voltage of 3 V and negligible internal resistance. The standard cell voltage is 1.0190 V, and R_1 is adjusted to calibrate the potentiometer when BC is 50.95 cm.

(*a*) Determine the current through AB and the resistance of R_1 when the potentiometer is calibrated.

(*b*) Calculate V_x when null is obtained at 94.3 cm.

(*c*) Determine the resistance of R_2 to limit the standard cell current to a maximum of 20 μA.

SOLUTION

(*a*) *at calibration:*

$$V_{BC} = V_{B2} = 1.0190\ \text{V},$$

$$\text{Volts per unit length} = \frac{1.0190\ \text{V}}{50.95\ \text{cm}}$$

$$= 20\ \text{mV/cm},$$

$$V_{AB} = 100\ \text{cm} \times 20\ \text{mV/cm}$$

$$= 2\ \text{V},$$

$$I = \frac{V_{AB}}{R_{AB}} = \frac{2\ \text{V}}{100\ \Omega}$$

$$= 20\ \text{mA},$$

$$V_{R1} = V_{B1} - V_{AB}$$

$$= 3\ \text{V} - 2\ \text{V} = 1\ \text{V},$$

$$R_1 = \frac{1\ \text{V}}{20\ \text{mA}} = 50\ \Omega.$$

(*b*) $V_x = 94.3\ \text{cm} \times 20\ \text{mV/cm} = 1.886\ \text{V}.$

(*c*) *At worst, the terminal voltage of B_2 or B_1 may be reversed, R_1 may be set to zero, and C set to terminal A. The total voltage producing current flow through the standard cell is now:*

$$V_{B2} + V_{B1} = 3\ \text{V} + 1.019\ \text{V}$$

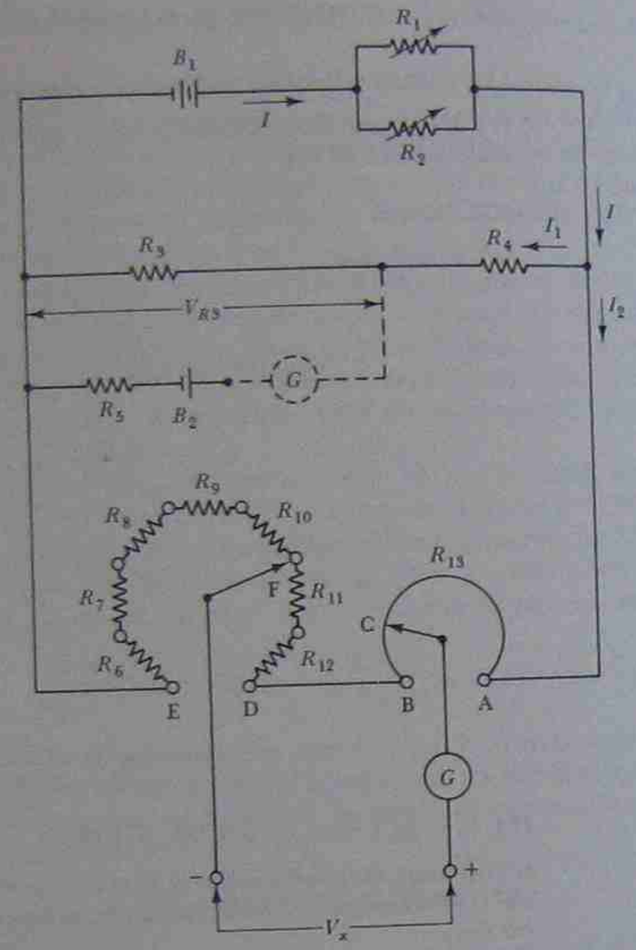
$$= 4.019\ \text{V},$$

$$R_2 = \frac{4.019\ \text{V}}{20\ \mu\text{A}} = 200\ \text{k}\Omega.$$

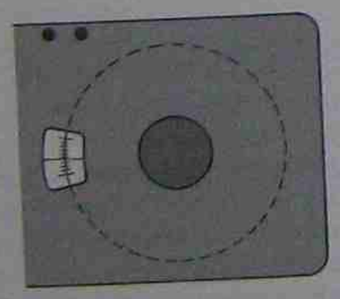
5-3 POTENTIOMETER WITH SWITCHED RESISTORS

The simple dc potentiometer described in Section 5-2 can measure voltage with a maximum accuracy of approximately ± 2 mV. The more complex circuit shown in Figure 5-3(a) employs resistors in addition to the slide wire to extend the accuracy of the instrument. As illustrated, R_6 through R_{12} are precision resistors connected to a rotary switch. With the switch contact in the position shown when null is obtained on the galvanometer, the measured voltage is $V_x = V_{R11} + V_{R12} + V_{BC}$.

Since the slide wire is arranged in a circle, a circular scale and pointer can be used to indicate the exact position of the sliding contact. Similarly,



(a) Circuit diagram



(b) Rotating scale and window

FIGURE 5-3. dc potentiometer with switched resistors.

a pointer and circular scale can be used to indicate the position of switched contact F. Instead of pointers and fixed circular scales, rotatable scales are usually employed, with windows and lines to indicate the scale positions [see Figure 5-3(b)]. Also, rather than giving the positions of the moving contacts, the corresponding voltages (when calibrated) are indicated on the scales.

Two additional precision resistors R_3 and R_4 are included to permit fast calibration. These resistances are selected so that the instrument is calibrated when V_{R3} is exactly equal to the standard cell voltage. By a push-button switching arrangement (not shown) the galvanometer is disconnected from V_x and the slide wire, and reconnected in series with standard cell B_2 and the junction of R_3 and R_4. This position is shown by broken lines in Figure 5-3(a).

Current to the potentiometer is provided from battery B_1 via variable resistors R_1 and R_2. R_1 may have a low resistance value, so that it acts as a *coarse* control of current I. R_2 should have a resistance many times greater than R_1. Thus, a relatively large adjustment of R_2 has only a small effect on the combined resistance of R_1 and R_2 in parallel. Consequently, R_2 has a correspondingly small effect on I, and it acts as a *fine* control to set I to the exact level required for calibration, after it has been set approximately by R_1.

To calibrate the circuit, the push-button switch (discussed above) is depressed, and R_1 and R_2 are adjusted as explained to obtain null on the galvanometer. The push button is then released to connect V_x and the galvanometer into position for measuring V_x. The switched contact F is moved as necessary until the galvanometer approaches null. Then the sliding contact C is adjusted to achieve a precise null. When null is obtained, the push-button switch is again depressed to check the potentiometer calibration. This is necessary because the battery voltage is always falling slightly, causing the potentiometer to drift away from calibration. Adjustment of R_2 is made as required, to recalibrate. With the instrument recalibrated, the push button is released and contact C is once more adjusted to achieve null. Then, calibration is once again checked and reset if required, before once more checking for galvanometer null with V_x in the circuit. This procedure is repeated until null is obtained both when calibration is checked (push button depressed) and when V_x is being measured (push button released). Finally, the scales of the potentiometer are read to determine V_x.

EXAMPLE 5-2

The dc potentiometer shown in Figure 5-3 has a 100 Ω-slide wire (R_{13}) and resistors R_6 through R_{12} are each exactly 100 Ω. R_3 is 509.5 Ω and R_4 is 290.5 Ω. If the standard cell voltage is 1.0190 V, determine the maximum voltage that may be measured by the potentiometer. Assuming that the slide wire is 100 cm in length and that the sliding contact position can be read within ±1 mm, calculate the instrument resolution.

SOLUTION

$$V_{R3} = V_{B2} = 1.0190 \text{ V},$$
$$I_1 = \frac{V_{B2}}{R_3} = \frac{1.0190 \text{ V}}{509.5\ \Omega}$$
$$= 2 \text{ mA}.$$

Maximum voltage measurable:

$$V_{AE} = I_1(R_3 + R_4)$$
$$= 2 \text{ mA}(290.5\ \Omega + 509.5\ \Omega)$$
$$= 1.6 \text{ V},$$

Resolution:

$$I_2 = V_{AE}/(R_6 + R_7 \text{ through } R_{13})$$
$$= \frac{1.6 \text{ V}}{8 \times 100\ \Omega}$$
$$= 2 \text{ mA},$$
$$V_{AB} = I_2 R_{13} = 2 \text{ mA} \times 100\ \Omega$$
$$= 200 \text{ mV}.$$

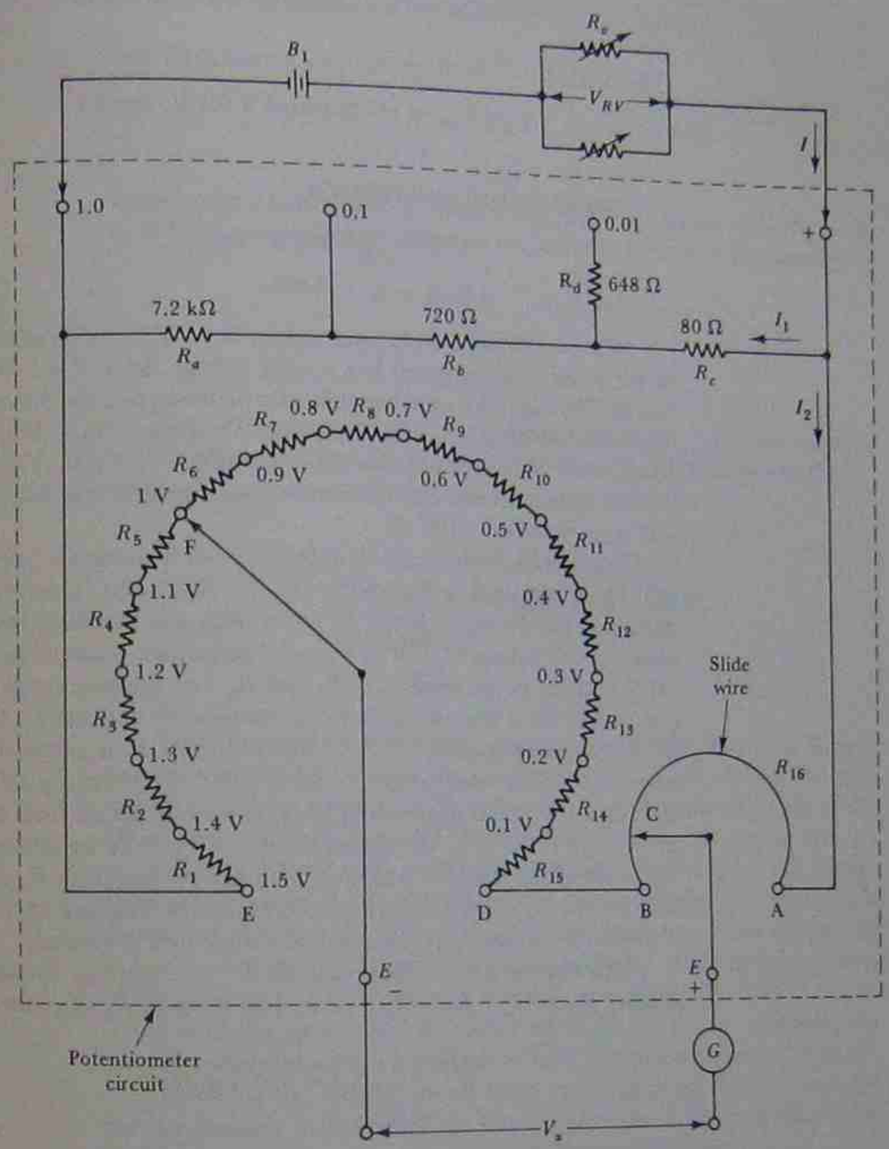
slide wire volts/unit length $= 200 \text{ mV}/100 \text{ cm}$
$= 2 \text{ mV/cm}$
$= 0.2 \text{ mV/mm},$

instrument resolution $= \pm 0.2 \text{ mV}.$

5-4 MULTIRANGE POTENTIOMETER

The circuit of a potentiometer with three measurement ranges is shown in Figure 5-4. R_1 through R_{15} are each 50-Ω resistors connected to the terminals of a rotary switch. R_{16} is a 50-Ω slide wire. As will be explained, resistors R_a, R_b, R_c, and R_d are solely for the purpose of range changing. Battery B_1 and current control resistors R_s are initially connected to the + and 1.0 terminals of the potentiometer circuit, as shown. The E_- and E_+ terminals are used both for calibration and for connection of the voltage to be measured.

With the battery and R_s connected to the + and 1.0 terminals, and the potentiometer calibrated, there is a 0.1-V drop across each of the 50-Ω resistors and across the slide wire terminals. Measuring from terminal *D*, the total voltage drop along R_1 to R_{15} is indicated in Figure 5-4: 0.1 V, 0.2 V, etc. The maximum voltage that can be measured by the potentiometer



Potentiometer circuit, supply, and galvanometer

FIGURE 5-4. Multirange potentiometer (Courtesy of Leeds & Northrup).

is calculated:

$$V_{max} = (16 \text{ resistors}) \times 0.1 \text{ V/resistor}$$
$$= 1.6 \text{ V}.$$

The current through each resistor is

$$I_2 = 0.1 \text{ V}/50 \ \Omega$$
$$= 2 \text{ mA}.$$

When the total potentiometer voltage is 1.6 V, the slide wire (like each of the other 50-Ω resistors) has a total voltage drop of 0.1 V along its length. The slide wire scale has 100 main divisions, and the moving contact can be set to within $\pm 1/10$ of a division. Thus, the voltage drop from B to C can be set with a resolution of ± 0.1 V/1000, i.e., ± 100 μV. This means that the potentiometer can measure voltages up to a maximum of 1.6 V with a precision of ± 100 μV.

To calibrate the instrument, a standard cell is connected in place of V_x with its + terminal to E_+ and − to E_-. As always, a current-limiting resistance should be included in series with the standard cell. With a standard cell voltage of 1.0190 V, switched contact F should be set to the 1.0-V position at the junction of R_5 and R_6, i.e., the position illustrated in Figure 5-4. Thus the voltage between terminal D and the E_- terminal is 1.0 V (when calibrated). The additional 0.019 V is obtained between terminal B and moving contact C. If the slide wire is exactly 100 cm long and has 0.1 V across it, C should be set at exactly 19 cm from terminal B to give $V_{BC} = 0.019$ V. Of course, this is done simply by setting the slide wire scale to the 0.019-V position. The total voltage from E_- to E_+ now becomes exactly 1.019 V when the potentiometer is calibrated. Calibration is effected by adjusting R_c until galvanometer null is obtained.

With exactly 1.6 V across resistors R_1 through R_{16}, the same 1.6 V appears across $R_a + R_b + R_c$. The current through R_a, R_b, and R_c is

$$I_1 = \frac{1.6 \text{ V}}{7.2 \text{ k}\Omega + 720 \ \Omega + 80 \ \Omega}$$
$$= 0.2 \text{ mA}.$$

The battery current is

$$I_1 + I_2 = 0.2 \text{ mA} + 2 \text{ mA} = 2.2 \text{ mA}.$$

The total resistance of R_1 through R_{16} is

$$R_T = 16 \times 50 \ \Omega$$
$$= 800 \ \Omega.$$

The three resistors R_a, R_b, and R_c are connected in parallel with R_T, and

these three have a total resistance of

$$R_a + R_b + R_c = 7.2 \text{ k}\Omega + 720 \ \Omega + 80 \ \Omega$$
$$= 8 \text{ k}\Omega.$$

Therefore, the battery and R_c have a load of R_T in parallel with $(R_a + R_b + R_c)$. Or, potentiometer resistance between the 1.0 and + terminals is

$$R = R_T \| (R_a + R_b + R_c)$$
$$= 800 \ \Omega \| 8 \text{ k}\Omega$$
$$= 727.27 \ \Omega.$$

Now consider what happens when (after the potentiometer is calibrated) the battery circuit is switched from the 1.0 terminal to the 0.1 terminal. The battery is now "looking into" a resistance:

$$R = (R_a + R_T) \| (R_b + R_c)$$
$$= (7.2 \text{ k}\Omega + 800 \ \Omega) \| (720 \ \Omega + 80 \ \Omega)$$
$$= 8 \text{ k}\Omega \| 800 \ \Omega$$
$$= 727.27 \ \Omega.$$

Thus, the load on the battery circuit is unchanged. The total battery current remains 2.2 mA and the voltage drop V_{RV} is not altered. But now the 1.6 V appears across $R_b + R_c$ and across $R_a + R_T$. Since $R_b + R_c = 800$ Ω the current that flows is 1.6 V/800 Ω = 2 mA. Also, the current through $R_a + R_T$ is 1.6 V/(7.2 kΩ + 800 Ω) = 0.2 mA. This 0.2 mA is the current flowing in resistors R_1 through R_{16}, and it gives a voltage drop across each resistor of 0.2 mA × 50 Ω = 0.01 V. The total potentiometer voltage across R_1 through R_{16} is now 16 × 0.01 V = 0.16 V. Also, the voltage drop along 1/10 of a main division of the slide wire is 0.01 V/1000 = 10 μV. Thus, with the battery and R_c connected to the 0.1 and + terminals, the potentiometer measures a maximum of 0.16 V with a precision of ±10 μV.

Switching the battery circuit (after calibration) to the 0.01 terminal further changes the range of the potentiometer by a factor of 10. At the 0.01 and + terminals the battery is "looking into" a resistance:

$$R = R_d + R_c \| (R_b + R_a + R_T)$$
$$= 648 \ \Omega + 80 \ \Omega \| (720 \ \Omega + 7.2 \text{ k}\Omega + 800 \ \Omega)$$
$$= 727.27 \ \Omega.$$

Once again, the load on the battery circuit is unchanged: I remains constant and V_{RV} does not change.

I flows through R_x and then divides between R_s and $(R_a + R_b + R_T)$. Using the current divider rule, the current through $(R_a + R_b + R_T)$ is

$$I_p = I\frac{R_s}{R_s + (R_a + R_b + R_T)}$$
$$= 2.2\text{ mA}\left(\frac{80\ \Omega}{80\Omega + 720\ \Omega + 7.2\text{ k}\Omega + 800\ \Omega}\right)$$
$$= 0.02\text{ mA}$$

This current flows in R_1 through R_{10}, giving a voltage drop across each of $50\ \Omega \times 0.02\text{ mA} = 0.001$ V. Now the total voltage across R_1 through R_{16} is $16 \times 0.001\text{ V} = 0.016$ V. The voltage drop along 1/10 of a main division on the slide wire is $0.001\text{ V}/1000 = 1\ \mu$V. It is seen that connecting the battery circuit to the 0.01 and + terminals permits the potentiometer to measure up to 0.016 V with a precision of $\pm 1\ \mu$V.

The precision of voltage measurement would seem to also define the accuracy of measurements. However, there are other sources of error, mainly contact resistances. The manufacturer of the circuit illustrated in Figure 5-4 specifies its accuracy as

RANGE	ACCURACY
0 to 1.6 V	$\pm 500\ \mu$V
0 to 0.16 V	$\pm 100\ \mu$V
0 to 0.016 V	$\pm 10\ \mu$V

5-5 dc AMMETER CALIBRATION BY POTENTIOMETER

An ammeter may be calibrated by connecting it in series with a precision resistor, and then accurately measuring the resistor voltage drop. The level of ammeter current is determined by dividing the resistor voltage drop by its resistance value. When the resistor value is precisely known, and voltage drop is measured by a dc potentiometer, the level of ammeter current can be determined with great accuracy.

Figure 5-5 shows the circuit for using a potentiometer to calibrate an ammeter. Current through the ammeter is supplied from a power supply via a current-limiting resistor. Because the total resistance of the ammeter and precision resistor is likely to be quite low, the current-limiting resistor is usually required to give good power supply control over the current. An alternative to this is to use a power supply equipped with a current limit control.

The power supply is adjusted to set the ammeter pointer exactly at each major scale division. For each pointer position, the resistor voltage drop is measured by the potentiometer, and the precise current level is calculated.

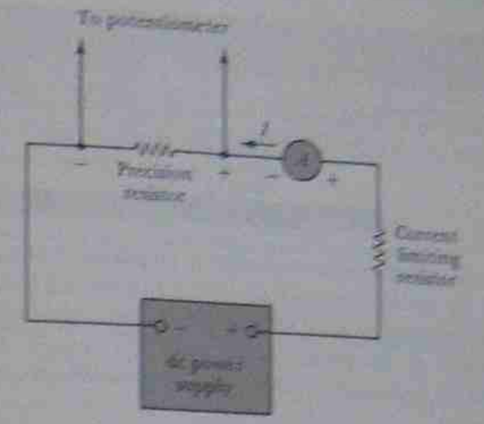


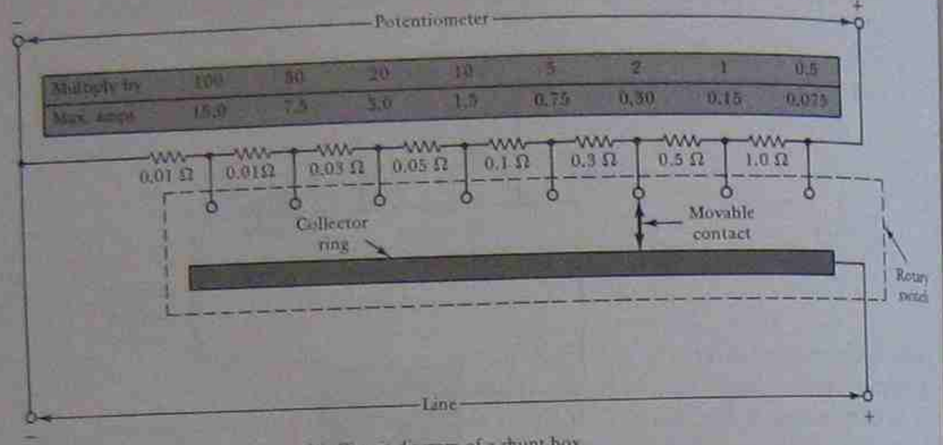
FIGURE 5-5. Ammeter calibration by dc potentiometer.

Precision resistors are available in *shunt boxes* solely for the purpose of calibrating ammeters by means of a dc potentiometer. Figure 5-6(a) shows the circuit of a typical shunt box, and Figure 5-6(b) shows its controls and connecting terminals. The shunt box resistors are actually connected in a circular fashion around the terminals of a rotary switch. In Figure 5-6(a) the resistors and rotary switch are shown in a straight line formation. The *line* terminals of the shunt box are connected in series with ammeter, and the shunt box potentiometer terminals go to the *potentiometer*.

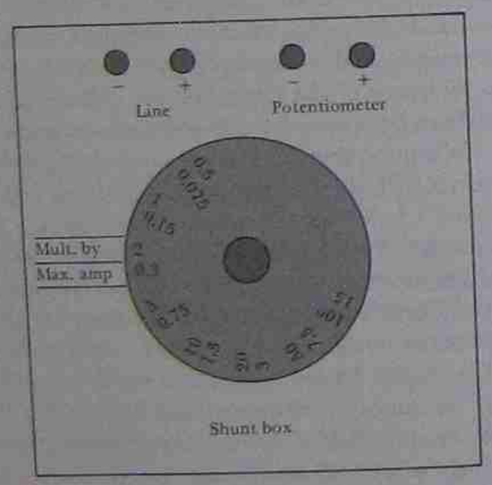
When the shunt box is set to the multiply by 1 position, the resistances in series with the line terminals add up to 1 Ω. If the measured voltage is exactly 1.5 V, the ammeter current is 1.5 V/1 Ω = 1.5 A or 1.5 × (multiplier 1) = 1.5 A. When the shunt box is at the multiply by 0.5 position, the total resistance is 2 Ω. The ammeter current is now calculated as (measured voltage) × 0.5 A. Similarly, at all other shunt box positions, the current in amperes is (measured voltage) × multiplier.

In Figure 5-6(a), with the movable contact in the position shown, the total resistance in series with the ammeter is 0.5 Ω (i.e., the total of all resistors to the left of the movable contact). Note also that the resistors to the right of the movable contact are actually in series with the galvanometer of the dc potentiometer. These total only 1.5 Ω (for the contact position shown) which is much smaller than the galvanometer resistance. Also, at null there is no current flowing in the galvanometer circuit, and there is no voltage drop across the 1.5-Ω resistance. So these resistors have no effect upon the measurement.

For every multiplier position on the shunt box, there is a maximum current level, identified as *MAX AMPS*. In each case, this current multiplied by the resistance in series with the line terminals gives an output (to the potentiometer) of 150 mV from the shunt box. At the multiply by 100



(a) Circuit diagram of a shunt box



(b) Controls and terminals of a shunt box

FIGURE 5-6. Shunt box used for potentiometer calibration of an ammeter

position, the maximum current is 15 A. Thus, the output voltage is 15 A × 0.01 Ω = 150 mV. At the multiply by 5 position, the 0.75-A maximum current gives the output voltage 0.75 A × (0.1 + 0.05 + 0.03 + 0.01 + 0.01)Ω = 150 mV. The maximum current level is selected to minimize resistor power dissipation and the temperature errors that may occur when the resistors are heated.

5-6 dc VOLTMETER CALIBRATION BY POTENTIOMETER

The precise voltage applied to a voltmeter can be directly measured by the potentiometer if the voltmeter range is not greater than 1.5 V. For higher ranges, two precision resistors should be used as a potential divider, as illustrated in Figure 5-7. The voltage across R_1 is measured by the potentiometer, and the precise voltmeter potential is determined as $E = V_{R1}(R_1 + R_2)/R_1$.

As in the case of the ammeter calibration, the power supply is adjusted to set the voltmeter pointer to each major scale division. For each pointer position, the voltage across R_1 is measured and the precise voltmeter potential is calculated.

Like the shunt box for use in ammeter calibration, a *volt box* contains the necessary potential divider resistors for potentiometer calibration of voltmeters. The circuit and the controls and terminals of a volt box are illustrated in Figure 5-8. Once again, the rotary switch and resistors are shown in a straight-line formation. The potentiometer always measures the

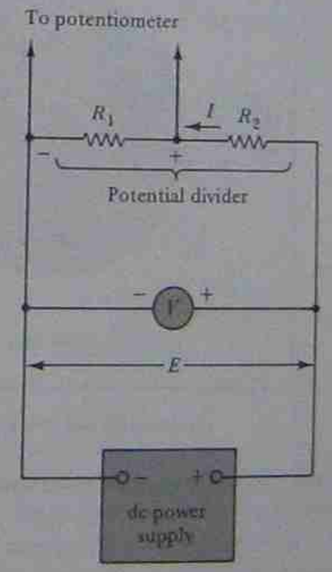
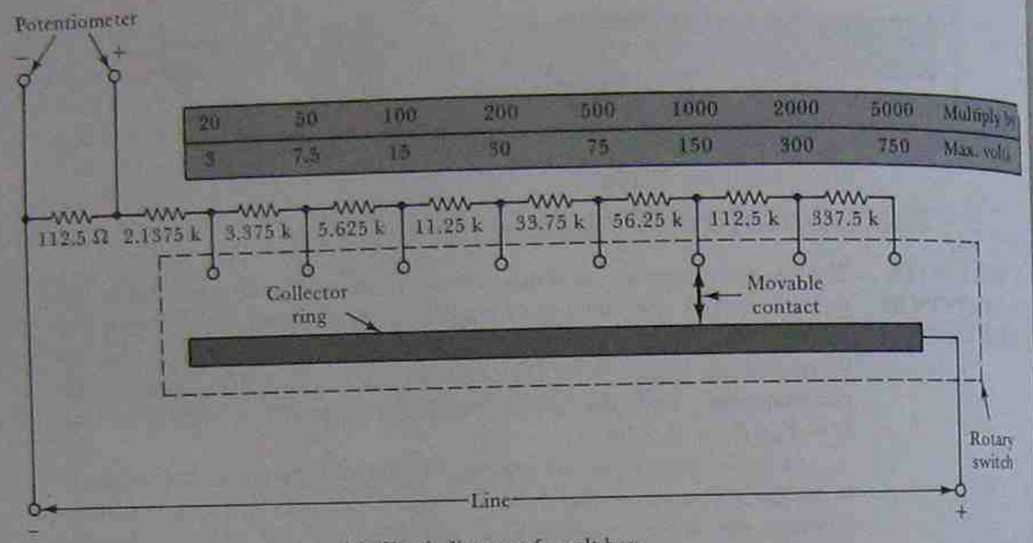
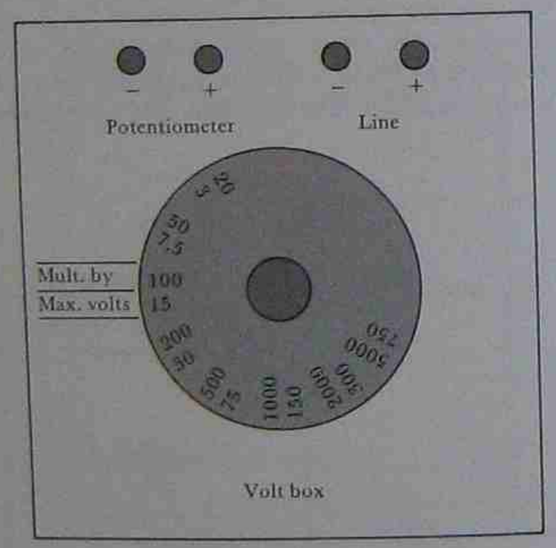


FIGURE 5-7. Voltmeter calibration by dc potentiometer.



(a) Circuit diagram of a volt box



(b) Controls and terminals of a volt box

FIGURE 5-8. Volt box used for potentiometer calibration of a voltmeter.

voltage drop across the 112.5 Ω (left-hand side) resistor in Figure 5-8(a). As illustrated, the *line voltage* (which is the voltmeter potential) is applied across the 112.5-Ω resistor and at least one other series-connected resistor. The voltage division ratio is altered by switching the moving contact.

When the volt box is set to the *multiply by 20* position, the voltage division ratio is:

$$\frac{\text{line voltage}}{\text{potentiometer voltage}} = \frac{112.5\ \Omega + 2.1375\ \text{k}\Omega}{112.5\ \Omega} = \frac{20}{1}.$$

Thus, the precise line voltage (or voltmeter potential) is determined by multiplying the potentiometer (measured) voltage by 20. Similarly, at all other volt box positions, the voltmeter potential is (measured voltage) × multiplier.

Every multiplier position on the volt box has a *MAX VOLTS* level stated. This is the maximum line voltage that should be applied to the volt box in each case. When the maximum voltage is applied, the volt box output (to the potentiometer) is always 150 mV. Like the shunt box maximum current, the maximum voltage levels are intended to minimize power dissipation and heating in the volt box resistors. Taking the maximum voltage and total resistance at any setting, the sensitivity of the volt box is calculated as 750 Ω/V, and the maximum current comes out to 1.33 mA. For example, at the *multiply by 20* position, the maximum voltage is 3 V, and the total resistance is

$$\begin{aligned} R &= 112.5\ \Omega + 2.1375\ \text{k}\Omega \\ &= 2.25\ \text{k}\Omega, \\ \textit{sensitivity} &= \frac{R}{V} = \frac{2.25\ \text{k}\Omega}{3\ \text{V}} \\ &= 750\ \Omega/\text{V}, \end{aligned}$$

and

$$\begin{aligned} I_{\max} &= \frac{V_{\max}}{R} = \frac{3\ \text{V}}{2.25\ \text{k}\Omega} \\ &= 1.33\ \text{mA}. \end{aligned}$$

5-7 WATTMETER CALIBRATION BY POTENTIOMETER

Wattmeter calibration is simply a combination of ammeter and voltmeter calibration methods. Figure 5-9 shows the wattmeter current coil supplied from one dc power supply, and voltage applied to the voltage coil from another power supply. A shunt box is connected in series with the current coil so that the current can be measured by a dc potentiometer. Similarly,

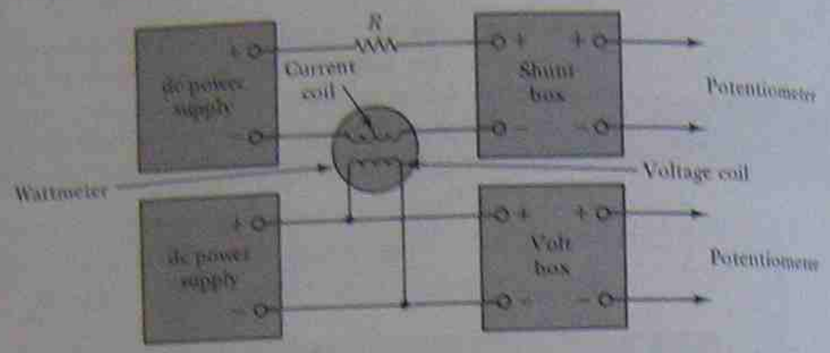


FIGURE 5-9. Wattmeter calibration by dc potentiometer.

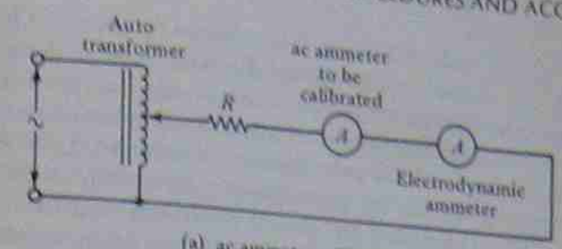
a volt box is connected in parallel with the voltage coil to facilitate potentiometer measurement of the applied voltage. Once the precise voltage and current levels are determined for a wattmeter indicated power, the exact power level is (measured voltage) × (measured current).

To calibrate the wattmeter, either or both of the power supplies may be adjusted to set the pointer in turn to each of the major scale divisions. Care should be taken to avoid the wattmeter maximum voltage and current levels (see Section 2-6-3). At each wattmeter pointer position the power level is determined from the potentiometer measurements, as described.

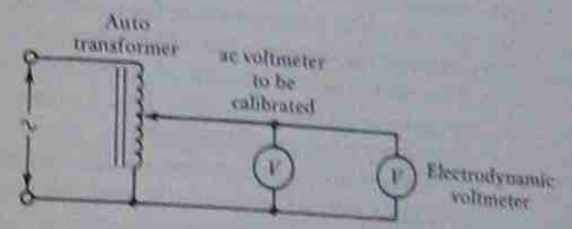
5-8 CALIBRATION OF ac INSTRUMENTS

Alternating current potentiometers are available, and in many ways they are similar to dc potentiometers. However, there is no ac equivalent to a standard cell. Consequently, the calibration procedure for ac potentiometers involves the use of a transfer instrument (e.g., an electrodynamic voltmeter). The scale of the transfer instrument can be read either as average voltage on dc or as rms voltage on ac. The instrument is calibrated using a dc potentiometer, and then used to calibrate the ac potentiometer.

Instead of using an ac potentiometer for calibration of an ac instrument, it makes more sense to use a transfer instrument directly to calibrate the instrument. Thus, ac ammeters can be calibrated by connecting them in series with an electrodynamic ammeter that has already been calibrated on a dc potentiometer [see Figure 5-10(a)]. The current level is adjusted (by the auto transformer) to set the pointer to each scale division on the instrument to be calibrated. Then the precise current level is read from the electrodynamic ammeter which was previously calibrated by a dc potentiometer. Similarly, an ac voltmeter to be calibrated is connected in parallel with an already calibrated electrodynamic voltmeter [Figure 5-10(b)]. The applied voltage is adjusted to indicate each scale division on the instrument to be calibrated, and the precise voltage levels are read from the electrodynamic voltmeter. This same procedure is also frequently



(a) ac ammeter calibration



(b) ac voltmeter calibration

FIGURE 5-10. Circuits for ac ammeter and voltmeter calibration by use of a transfer instrument.

used when calibrating dc ammeters and voltmeters. A standard instrument is carefully calibrated using the dc potentiometer, then this instrument is used to calibrate other instruments, as described above.

5-9 INSTRUMENT CALIBRATION PROCEDURES AND ACCURACY

Before attempting to calibrate any instrument, the instrument should be cleaned and all necessary repairs made (e.g., straightening bent pointers). The calibration circuitry should be set up and the potentiometer calibrated.

The pointer zero position on the instrument should be checked, and the mechanical zero control adjusted if necessary, while tapping the instrument gently to relieve friction. The supply voltage is adjusted to increase the instrument voltage or current, progressively setting the pointer to each major scale division (or *cardinal points*). Again, the instrument should be lightly tapped to relieve friction when setting the pointer. At each pointer position, the potentiometer calibration is checked, and then a potentiometer measurement is made of the volt box or shunt box output. This procedure is followed for each major scale division on the instrument, first going up-scale to FSD, and then going down-scale to zero.

When the precise levels of the indicated quantities are determined from the potentiometer measurements, a calibration chart is prepared for the instrument, showing the actual current or voltage levels alongside the

indicated levels. The *correction* or difference between indicated and actual levels is also charted. Each correction is designated + or −, showing that the figure should either be added to or subtracted from the instrument reading. Table 5-1 is an example of an ammeter calibration chart.

As already discussed in Section 5-8, not all instruments are calibrated directly by potentiometer. Frequently, a laboratory *standard instrument* is calibrated by potentiometer and then used for comparison with other instruments. The standard instrument should have a long scale with a mirror alongside for accurately reading the pointer position. Its accuracy should be ±0.1% for calibration of lower accuracy instruments.

The best potentiometers have a measurement accuracy of ±0.01% and the accuracy of volt boxes and shunt boxes is typically ±0.02%. Therefore, the combination of potentiometer and volt box or shunt box gives an accuracy of ±0.03%. This is satisfactory for calibration of ±0.1% laboratory standard instruments.

Where an instrument does not have a long mirror-scale, there is always a reading error of at least 0.1%, and this must be added to the calibration error whenever the instrument accuracy is calculated. Suppose such an instrument is calibrated by comparison with a 0.1% instrument. When calibrating, the pointer position is determined with an accuracy not better than ±0.1%, and, therefore, the calibration errors add up: (±0.1% for the standard instrument) + (±0.1% reading error) = ±0.2%. Now when the instrument is used for measurements, there is a further reading error of ±0.1%, giving a total measurement accuracy of ±0.3%. This is the best accuracy that may be expected from a good quality instrument that does not have a long mirror-scale. Usually, of course, even very good quality instruments with mirror-scales have a specified accuracy no better than ±2%.

TABLE 5-1. Calibration Chart for a dc Ammeter

SCALE READING (mA)	PRECISE CURRENT LEVEL (mA)	CORRECTION (mA)
100	103	+3
90	93	+3
80	82.5	+2.5
70	72	+2
60	62	+2
50	51.7	+1.7
40	41.5	+1.5
30	31	+1
20	19.7	−0.3
10	9.5	−0.5
0	0.0	0.0

5-10 SELF-BALANCING POTENTIOMETER

Carefully adjusting a potentiometer for galvanometer null whenever a voltage is to be measured can be impossibly time consuming in certain circumstances. One example is when a changing voltage is to be monitored constantly. In this situation a potentiometer which automatically balances itself is required. The basic circuit of a self-balancing potentiometer is illustrated in Figure 5-11.

Instead of using a galvanometer for detecting null, the difference between V_x and the potentiometer voltage (V_{BC}) is applied to the input of an amplifier. The amplifier output drives a motor which controls the position of slide wire contact C. If V_x is larger than the potentiometer voltage, the polarity of the difference voltage at the amplifier input is such

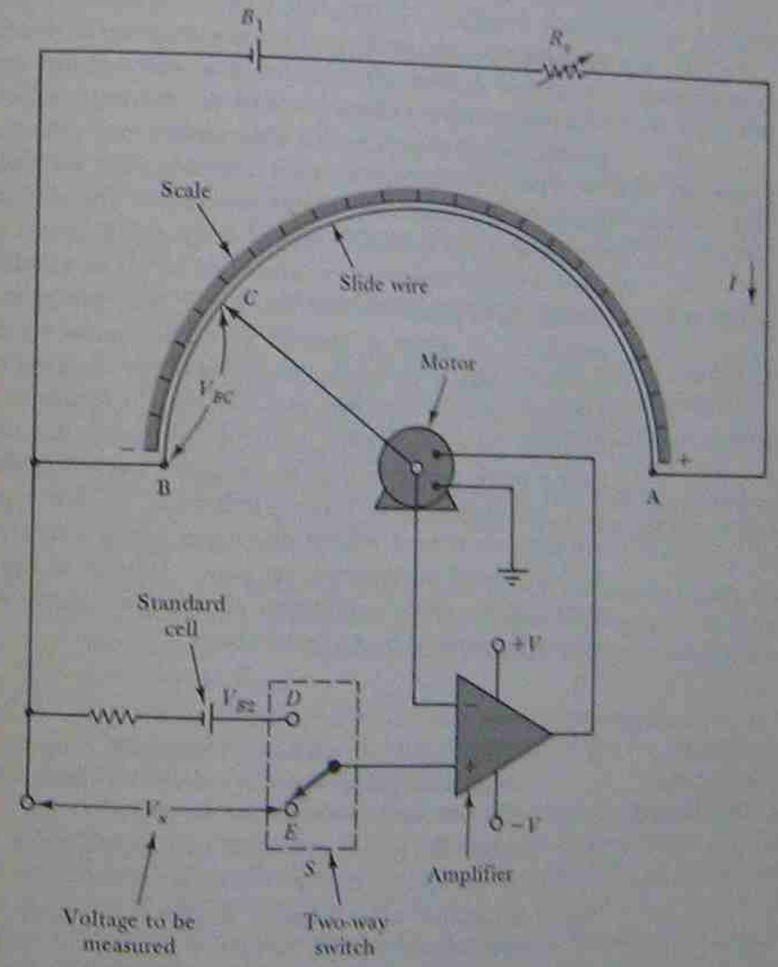


FIGURE 5-11. Basic circuit of self-balancing potentiometer.

that the motor rotates in a clockwise direction, increasing V_{BC} until V_{BC} equals V_x. Then, when there is no difference voltage at the amplifier input, the output voltage to the motor is zero, and contact C remains stationary. When V_x is smaller than V_{BC}, the motor rotates in a counterclockwise direction until the difference voltage is again reduced to zero, i.e., until $V_{BC} = V_x$. The measured voltage may be read from a scale alongside the slide wire, or possibly it may be indicated on a rotating scale, as explained in Section 5-3.

To calibrate the potentiometer, two-way switch S is switched from position E to position D. The voltage applied to the amplifier input is now the difference between potentiometer voltage V_{BC} and standard cell voltage V_{B2}. As before, the motor moves contact C until V_{BC} is equal to V_{B2}. At this point, if V_{B2} is 1.0190 V, the scale position of C should indicate that V_{BC} is exactly 1.0190 V. If the scale position of C is not precisely equal to the standard cell voltage, R_1 is adjusted to increase or decrease the potentiometer current I, thus adjusting the slide wire voltage drop per unit length. The instrument is calibrated when the moving contact settles at the scale position which exactly equals the standard cell voltage.

The practical circuit of a self-balancing dc potentiometer is more complex than the basic circuit illustrated. The difference voltage at the amplifier input is usually *chopped* to convert it into a pulse waveform (see Section 8-11), which is then amplified by an ac amplifier. This is to avoid voltage drift problems that can occur with precision dc amplifiers. The amplified ac signal is applied to an ac motor to move the slide wire contact. Usually the motor is mechanically coupled to a pen on a chart recorder. (Chart recorders are discussed in Chapter 13.) The chart now becomes the voltage scale, and the pen traces out the voltage variation over a given period of time as the paper moves slowly. Furnace temperature monitoring is a major application of this type of instrument. A temperature related voltage developed across a thermocouple (see Section 2-7) is charted continuously on paper. Instead of voltage, the chart has a temperature scale. Calibration of this instrument would be performed regularly, perhaps on an hourly basis.

REVIEW QUESTIONS AND PROBLEMS

5-1. Sketch the construction of a standard cell, and identify the various component parts. State a typical terminal voltage for a standard cell, and list precautions for its use.

5-2. Sketch the circuit of a basic dc potentiometer, and explain how it is calibrated and how a voltage is measured by the potentiometer.

5-3. A basic dc potentiometer, as shown in Figure 5-2, has the following components: a 3-V battery, a 150-Ω slide wire 1.5 meters long, a standard cell with a voltage of 1.0195 V, and variable resistor R_1.

(a) Calculate the slide wire current and the value of R_1 when the potentiometer is calibrated.
(b) Determine the slide wire position BC at which the sliding contact should be set for calibration.
(c) Calculate the measured voltage V_x when null is obtained at 72.5 cm.
(d) Calculate the value of resistor R_2 to be connected in series with the standard cell to limit the maximum current to 20 μA.

5-4. A basic dc potentiometer has a 200-cm slide wire with a resistance of 100 Ω. A 4-V battery in series with a variable resistor R_1 provides current through the slide wire. The standard cell potential is 1.018 V, and the potentiometer is calibrated when the sliding contact is set to 101.8 cm from the zero voltage end of the slide wire.
(a) Calculate R_1 and the current flowing through R_1.
(b) Determine the value of resistance that must be connected in series with the standard cell to limit its current to 20 μA.
(c) What is the measured voltage when zero galvanometer deflection is obtained with the slide wire at 94.3 cm from the zero voltage end?

5-5. A dc potentiometer, as in Figure 5-3, has a 50-Ω slide wire (R_{15}) and seven 50-Ω resistors (R_6 through R_{12}). The standard cell voltage is 1.018 V, and resistors R_3 and R_4 are $R_3 = 470$ Ω and $R_4 = 84.028$ Ω.
(a) Determine the maximum voltage that can be measured on the potentiometer.
(b) If the slide wire is 150 cm long, and the sliding contact can be set to within ±1 mm, determine the instrument resolution.
(c) Calculate the value of series resistance ($R_1 \| R_2$ in Figure 5-3) when the supply battery has $V_B = 3$ V.

5-6. Sketch the circuit of the potentiometer described in Question 5-4, and show how a standard cell should be connected for calibrating the potentiometer.

5-7. Refer to the potentiometer circuit in Figure 5-4, and show that it can measure a maximum of 1.6 V when the supply is connected to the + and 1.0 terminals. If a 3-V supply battery is used, calculate the value of R_x.

5-8. For Figure 5-4, show that the maximum measurable voltage is 0.16 V and 0.016 V when the supply is connected to the + and the 0.1 and 0.01 terminals respectively.

5-9. Draw a sketch to show how a galvanometer and standard cell should be connected for calibrating the potentiometer in Figure 5-4. If the standard cell voltage is 1.0183 V, at what points should the moving contacts be set?

5-10. Sketch a circuit to show how a dc ammeter should be calibrated by means of a dc potentiometer. Briefly explain.

5-11. A 100-mA (FSD) ammeter is to be calibrated by means of the potentiometer in Figure 5-4. Determine a suitable value of precision resistor and its maximum power dissipation.

5-12. Sketch the circuit of a shunt box, and briefly explain how it is used together with a dc potentiometer for ammeter calibration. State any precautions that must be observed.

5-13. Sketch a circuit to show how a dc potentiometer and two precision resistors can be used to calibrate a dc voltmeter. Briefly explain.

5-14. A 30-V (FSD) voltmeter is to be calibrated by means of the potentiometer in Figure 5-4. Determine the ratio of suitable precision resistors (as in Question 5-13).

5-15. Sketch the circuit of a volt box, and briefly explain how it is used together with a dc potentiometer for voltmeter calibration. State any precautions that must be observed.

5-16. Sketch a circuit to show how a wattmeter may be calibrated by use of a dc potentiometer.

5-17. Sketch circuits to show how ac ammeters and voltmeters can be calibrated. Briefly explain in each case.

5-18. Discuss the procedures used in calibrating instruments. Prepare a calibration chart for use in calibrating a voltmeter. Discuss the accuracy achieved in calibrating instruments.

5-19. Sketch the circuit of a self-balancing potentiometer. Explain its operation and briefly discuss its application.

6

PRECISE RESISTANCE MEASUREMENTS

INTRODUCTION

Although the ohmmeter is convenient for measuring resistance, it is not very accurate. More precise resistance measurements can be made using comparison methods, the dc potentiometer, or the *Wheatstone bridge*. The Wheatstone bridge in particular can be very accurate, although it is not suitable for measuring very small resistance values. The bridge circuit consists of a supply voltage, a galvanometer, and four resistors. One of the four is the resistance to be measured. The galvanometer is used as a *null detector*, and the unknown resistance is determined in terms of the three known resistance values.

For accurate measurements of very low resistances, such as ammeter shunts, the *Kelvin bridge* is used. This is a modified version of the Wheatstone bridge. Measurement of very high (insulation) resistance requires high voltages, low current ammeters, and special techniques to separate surface leakage resistance from volume resistance.

6-1 VOLTMETER AND AMMETER METHODS

One way of determining the value of a resistance is simply to apply a voltage across its terminals and use an ammeter and voltmeter to measure the current and voltage. The measured quantities may then be substituted into Ohm's law to calculate the resistance $R = E/I$. Although very accurate measuring instruments may be used, there can be serious error in the resistance value arrived at in this way.

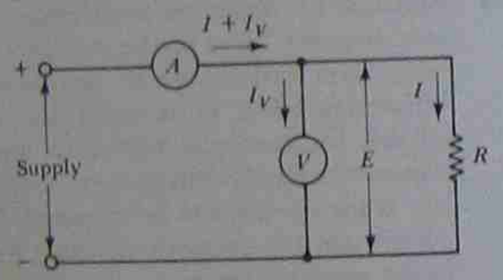
Consider the circuit in Figure 6-1(a). The voltmeter measures the voltage E across the terminals of the resistor, but the ammeter indicates the resistor current I *plus* the voltmeter current I_v. The calculated resistance now comes out as

$$R = \frac{E}{I + I_v}. \tag{6-1}$$

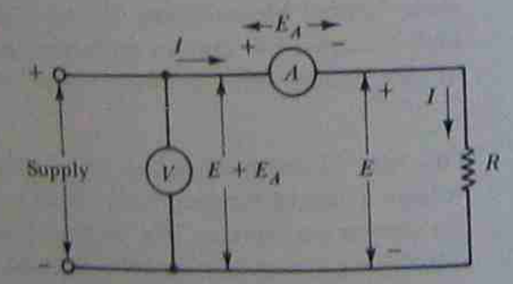
Since it is obvious that R actually equals E/I, the presence of I_v constitutes an error. Of course, if I_v is very much smaller than I, the error may be negligible.

Now look at Figure 6-1(b) in which the ammeter is directly in series with resistor R. In this case the ammeter measures only the resistor current I; the voltmeter current I_v is not involved. However, the voltmeter now indicates the resistor voltage E *plus* the ammeter voltage drop E_A. Consequently, the calculated resistance is

$$R = \frac{E + E_A}{I}. \tag{6-2}$$



(a) Voltmeter connected across load



(b) Voltmeter connected across supply

FIGURE 6-1. Ammeter and voltmeter method of resistance measurement

Once again this is not the same as $R = E/I$, and an error results because of the presence of E_A. Clearly, if E_A is very much smaller than E, the error may be small enough to neglect.

The circuit in Figure 6-1(a) is accurate when resistor R has a value very much smaller than the voltmeter resistance. When this is the case, I_v is very much smaller than I, and

$$R = \frac{E}{I + I_v} \simeq \frac{E}{I}.$$

The arrangement in Figure 6-1(b) is most suitable where the value of R is very much larger than the ammeter resistance. This makes E_A very small compared to E, and gives

$$R = \frac{E + E_A}{I} \simeq \frac{E}{I}.$$

To select the best circuit [(a) or (b)] for measuring any given resistance, first connect up the instruments as shown in Figure 6-1(a). Carefully note the ammeter indication, then disconnect one terminal of the voltmeter. If the ammeter indication does not appear to change when the voltmeter is disconnected, then I_v is very much less than I, and Figure 6-1(a) is the correct connection for accurately measuring R. If the indicated current drops noticeably when the voltmeter is disconnected, I_v is *not* very much smaller than I. In this case, the circuit in Figure 6-1(b) affords the most accurate determination of R.

A very simple method of measuring resistance is illustrated in Figure 6-2. In Figure 6-2(a) the resistor R which is to be measured is connected in series with an ammeter and a dc supply. The ammeter is adjusted to a suitable range, and its pointer position on the scale is carefully noted. The resistor is now disconnected and a *decade* resistance box (a precision variable resistor) is connected in its place. The decade resistance box should initially be set to its highest possible value. Once in the circuit, the decade box is

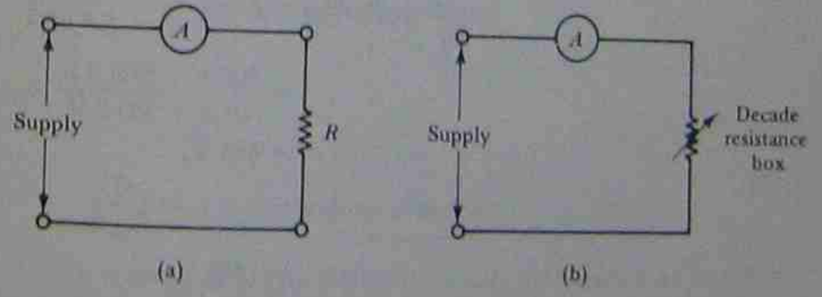


FIGURE 6-2. Ammeter and variable resistance method of resistance measurement.

adjusted until the ammeter precisely indicates the same level of current as when R was in the circuit. The resistance of the decade box (indicated by the switch positions) is now exactly equal to R.

EXAMPLE 6-1 A resistance is measured by the ammeter and voltmeter circuit illustrated in Figure 6-1(b). The measured current is 0.5 A, and the voltmeter indication is 500 V. The ammeter has a resistance of $R_a = 10\ \Omega$, and the voltmeter on a 1000-V range has a sensitivity of 10 kΩ/V. Calculate the value of R.

SOLUTION

$$E + E_A = 500\ \text{V},$$
$$I = 0.5\ \text{A},$$
$$R_a + R = \frac{E + E_A}{I}$$
$$= \frac{500\ \text{V}}{0.5\ \text{A}} = 1000\ \Omega,$$
$$R = 1000\ \Omega - R_a$$
$$= 1000\ \Omega - 10\ \Omega$$
$$= 990\ \Omega.$$

EXAMPLE 6-2 If the ammeter, voltmeter, and resistance R in Example 6-1 are reconnected in the form of Figure 6-1(a), determine the ammeter and voltmeter indications.

SOLUTION

$$R_v = 1000\ \text{V} \times 10\ \text{k}\Omega/\text{V}$$
$$= 10\ \text{M}\Omega,$$
$$R_v \| R = 10\ \text{M}\Omega \| 990\ \Omega$$
$$= 989.9\ \Omega,$$
$$\text{supply voltage} = 500\ \text{V}, (E + E_A \text{ in Example 6-1})$$
$$\text{voltmeter reading} = E = \frac{500\ \text{V} \times (R_v \| R)}{R_a + (R_v \| R)}$$
$$= \frac{500\ \text{V} \times 989.9\ \Omega}{10\ \Omega + 989.9\ \Omega}$$
$$= 493\ \text{V},$$
$$\text{ammeter reading} = I + I_v = \frac{E}{R_v \| R}$$
$$= \frac{493\ \text{V}}{989.9\ \Omega}$$
$$= 0.5\ \text{A}.$$

EXAMPLE 6-3 Referring to Examples 6-1 and 6-2, determine which of the two circuits, Figure 6-1(a) or Figure 6-1(b), gives the most accurate measurement of R for this particular case, when R is calculated without taking R_a and R_v into account.

SOLUTION

For Figure 6-1(a) (Example 6-2):

$$\text{voltmeter reading} = 493\ \text{V},$$
$$\text{ammeter reading} = 0.5\ \text{A},$$
$$R = \frac{493\ \text{V}}{0.5\ \text{A}} = 986\ \Omega.$$

For Figure 6-1(b) (Example 6-1):

$$\text{voltmeter reading} = 500\ \text{V},$$
$$\text{ammeter reading} = 0.5\ \text{A},$$
$$R = \frac{500\ \text{V}}{0.5\ \text{A}} = 1000\ \Omega.$$

In this case, the circuit of Figure 6-1(a) gives the most accurate determination of R.

6-2 RESISTANCE MEASUREMENT BY POTENTIOMETER

A dc potentiometer can be used to make very accurate resistance measurements. The process is similar to that used in the calibration of ammeters (Section 5-5). The resistance to be measured is connected in series with a known standard resistor and supplied with current from a power supply via a current limiting resistor (see Figure 6-3). The voltage across resistor R is measured by the potentiometer, and the current flow is adjusted to give a convenient level of V_R. With the current remaining constant, the precision resistor voltage V_{RS} is next measured by potentiometer. Because, $I = V_R/R$ and $I = V_{RS}/R_S$:

$$\frac{V_R}{R} = \frac{V_{RS}}{R_S}$$

and

$$\boxed{R = \frac{V_R}{V_{RS}} R_S} \tag{6-3}$$

With a precisely known standard resistor, the accuracy of determination of R is as good as the accuracy of calibration of an ammeter (Section 5-9).

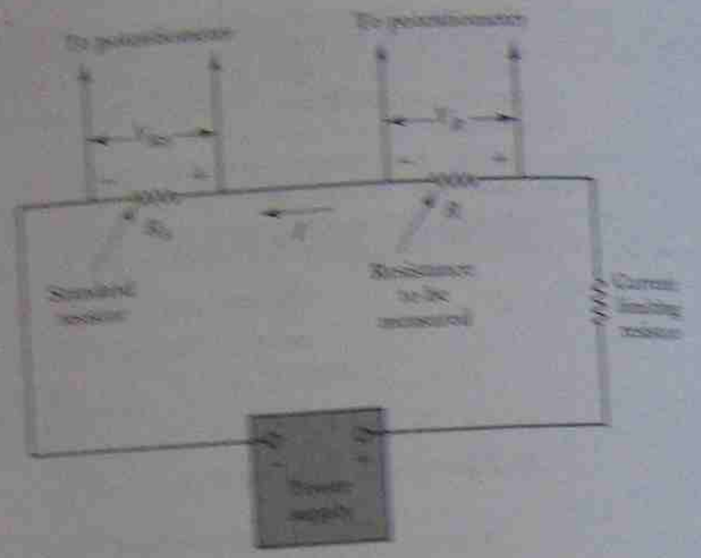


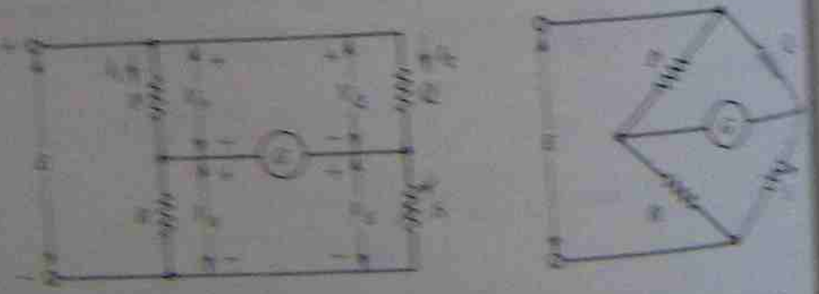
FIGURE 6-5. Resistance measurement by potentiometer.

6-3 THE WHEATSTONE BRIDGE

Very accurate resistance measurements can be made by use of a Wheatstone bridge. The bridge circuit shown in Figure 6-6(a) consists of two precision resistors P and Q, an adjustable precision resistor S, resistance R to be measured, and a galvanometer G. A supply voltage E causes the flow of currents I_1 and I_2. The circuit in Figure 6-6(b) is exactly the same as that in Figure 6-6(a). Figure 6-6(b) shows the usual way that a Wheatstone bridge circuit is drawn.

6-3-1 Operation

To determine the unknown resistance R, variable resistance S is adjusted until the galvanometer indicates null. Initially the galvanometer should be shunted to protect it from excessive current levels, see Figure



(a) Wheatstone bridge circuit

(b) Usual way to draw Wheatstone bridge circuit

FIGURE 6-6. Wheatstone bridge circuit.

6-10. As null is approached, the shunting resistance is made larger and larger, until eventually the galvanometer indicates zero with the shunting resistor open-circuited. The Wheatstone bridge is now said to be *balanced*, or *nulled*. Before galvanometer null is achieved, the bridge is said to be in an *unbalanced* state.

When the galvanometer indicates zero, the voltages at each of its terminals must be equal. Thus, in Figure 6-6(a),

$$V_P = V_Q \quad \text{and} \quad V_R = V_S.$$

Also, because there is no current flow through the galvanometer, I_1 flows through both P and R, and I_2 flows through Q and S. Therefore,

$$I_1 R = I_2 S, \tag{1}$$

and

$$I_1 P = I_2 Q. \tag{2}$$

Dividing Equation 1 by Equation 2 gives

$$\frac{I_1 R}{I_1 P} = \frac{I_2 S}{I_2 Q} \quad \text{or} \quad \frac{R}{P} = \frac{S}{Q}$$

which gives the unknown resistance,

$$\boxed{R = \frac{SP}{Q}} \tag{6-6}$$

With the precise values of S, P, and Q known, resistance R can be accurately determined.

Note that the supply voltage E is not involved in the calculation. As will be explained, the supply voltage does affect the bridge sensitivity.

EXAMPLE 6-8 A Wheatstone bridge as in Figure 6-6 has $P = 3.5\ \text{k}\Omega$, $Q = 7\ \text{k}\Omega$, and galvanometer null is obtained when $S = 5.51\ \text{k}\Omega$. Calculate the value of R. Also, determine the resistance measurement range for the bridge if S is adjustable from 1 kΩ to 9 kΩ.

SOLUTION

Equation 6-6,

$$R = \frac{SP}{Q}$$

$$= \frac{5.51\ \text{k}\Omega \times 3.5\ \text{k}\Omega}{7\ \text{k}\Omega}$$

$$= 2.755\ \text{k}\Omega.$$

When $S = 1$ kΩ:

$$R = \frac{1\ \text{k}\Omega \times 3.5\ \text{k}\Omega}{7\ \text{k}\Omega}$$
$$= 500\ \Omega.$$

When $S = 8$ kΩ:

$$R = \frac{8\ \text{k}\Omega \times 3.5\ \text{k}\Omega}{7\ \text{k}\Omega}$$
$$= 4\ \text{k}\Omega.$$

Measurement range = 500 Ω to 4 kΩ.

6-3.2 Accuracy

In Chapter 4 it is explained that the maximum possible error in the product and quotient of quantities is the sum of the errors in all components involved. Thus, in the case of the Wheatstone bridge, where $R = SP/Q$, the percentage error in R is the sum of the percentage errors in each of S, P, and Q.

EXAMPLE 6-5 In Example 6-4, P and Q have accuracies of ±0.05%, and S has an accuracy of ±0.1%. Calculate the accuracy of R and its upper and lower limits for the P, Q, and S values stated.

SOLUTION

$$\text{error in } R = (P \text{ error}) + (Q \text{ error}) + (S \text{ error})$$
$$= \pm (0.05\% + 0.05\% + 0.1\%)$$
$$= \pm 0.2\%,$$
$$R = 2.755\ \text{k}\Omega \pm 0.2\%$$
$$= 2.755\ \text{k}\Omega \pm 5.5\ \Omega$$
$$= 2.7495\ \text{k}\Omega \text{ to } 2.7605\ \text{k}\Omega.$$

6-3.3 Sensitivity

Refer to Figure 6-4 and to Example 6-4 once again. When $R = 2$ kΩ, galvanometer null is obtained by setting S to:

$$S = \frac{QR}{P} = \frac{7\ \text{k}\Omega \times 2\ \text{k}\Omega}{3.5\ \text{k}\Omega}$$
$$= 4\ \text{k}\Omega.$$

If S is a decade resistance box, its lowest adjustment decade might be 0 to 10 Ω in 1 Ω steps. A more precise decade box could have a decade 0 to 1 Ω in 0.1 Ω steps.

If the galvanometer pointer is clearly deflected from zero when S is adjusted by ±0.1 Ω, then the bridge can be described as sensitive to ±0.1 Ω in S. The deflection from zero may be as small as 1 mm, so long as the pointer clearly moves off zero when S is adjusted by 0.1 Ω, and moves back again to zero when S is readjusted.

The bridge sensitivity to the measured resistance R may be calculated as

$$\Delta R = \frac{\Delta S P}{Q} = \frac{0.1\ \Omega \times 3.5\ \text{k}\Omega}{7\ \text{k}\Omega} = 0.05\ \Omega.$$

Now it can be stated that the sensitivity of this particular bridge to measured resistances is ±0.05 Ω. As explained in Section 4-3, this sensitivity is also a definition of the *precision* with which the bridge makes resistance measurements. The accuracy of measurements is still dependent upon the accuracies of the individual components, as demonstrated in Example 6-5. However, the error due to bridge sensitivity (in this case ±0.05 Ω) should always be much less than that due to the component accuracies.

The sensitivity of a Wheatstone bridge depends upon the current sensitivity of the galvanometer (see Section 1-5), galvanometer resistance, and the bridge supply voltage. To calculate the bridge sensitivity it is necessary to "look into" the bridge circuit from the galvanometer terminals. The bridge circuit is replaced with its *Thevenin equivalent circuit*, i.e., by its open-circuit output voltage in series with its internal resistance. The effect of minimum detectable galvanometer current can now be calculated.

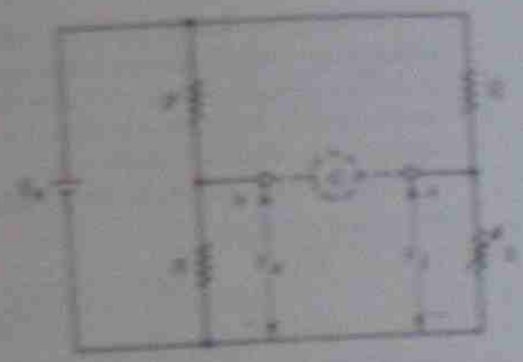
Figure 6-5(a) shows the bridge with the galvanometer removed. The open-circuit output voltage across the terminals at which the galvanometer is connected is

$$V_a - V_b = \frac{E_s R}{R + P} - \frac{E_s S}{Q + S},$$

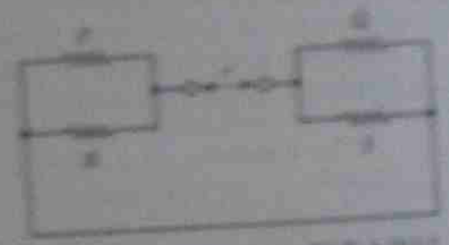
$$\boxed{V_a - V_b = E_s \left[\frac{R}{R + P} - \frac{S}{Q + S} \right].} \tag{6-5}$$

The internal resistance of the bridge (i.e., "seen" from the galvanometer terminals) is determined by first assuming that the voltage supply E_s has an internal resistance which is very much smaller than the resistance of the bridge components. This assumption gives the circuit of Figure 6-5(b) when E_s is replaced with a short circuit. Thus, it is seen that the internal resistance of the bridge is

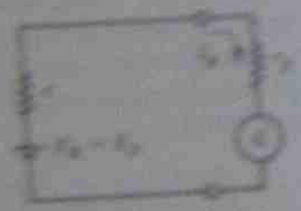
$$\boxed{r = P \| R + Q \| S.} \tag{6-6}$$



(a) Open-circuit voltage at the galvanometer terminals is $(V_R - V_S)$



(b) Internal resistance is $r = P(R + Q)/S$



(c) Thevenin equivalent circuit

FIGURE 6-5. Development of Thevenin equivalent circuit for Wheatstone bridge sensitivity analysis.

The complete equivalent circuit of the bridge and galvanometer is drawn in Figure 6-5(c). The galvanometer current is now

$$\boxed{I_g = \frac{V_R - V_S}{r + r_g}} \qquad (6\text{-}7)$$

Example 6-6 demonstrates the procedure for calculation of the bridge sensitivity.

EXAMPLE 6-6 A Wheatstone bridge has $P = 3.5\ \text{k}\Omega$, $Q = 7\ \text{k}\Omega$, and $S = 4\ \text{k}\Omega$ when $R = 2\ \text{k}\Omega$. The supply is $E_a = 10\ \text{V}$, and the galvanometer has a current sensitivity of 1 μA/mm and a resistance $r_g = 2.5\ \text{k}\Omega$. Calculate the minimum change in R which is detectable by the bridge.

SOLUTION

Equation 6-6,

$$\begin{aligned} r &= P(R + Q)/S \\ &= 3.5\ \text{k}\Omega(2\ \text{k}\Omega + 7\ \text{k}\Omega)/4\ \text{k}\Omega \\ &= 3.82\ \text{k}\Omega. \end{aligned}$$

From Equation 6-7,

$$\begin{aligned} V_R - V_S &= I_g(r + r_g) \\ &= 1\ \mu\text{A}(3.82\ \text{k}\Omega + 2.5\ \text{k}\Omega) \\ &= 6.32\ \text{mV}. \end{aligned}$$

From Equation 6-5,

$$\begin{aligned} \frac{R}{R+P} - \frac{S}{Q+S} &= \frac{V_R - V_S}{E_a} \\ &= \frac{6.32\ \text{mV}}{10\ \text{V}} \\ &= 632 \times 10^{-6}. \end{aligned}$$

If a change in R of ΔR is detectable, then

$$\frac{R + \Delta R}{R + P} - \frac{S}{Q + S} = 632 \times 10^{-6},$$

or

$$\frac{2\ \text{k}\Omega + \Delta R}{2\ \text{k}\Omega + 3.5\ \text{k}\Omega} - \frac{4\ \text{k}\Omega}{7\ \text{k}\Omega + 4\ \text{k}\Omega} = 632 \times 10^{-6},$$

$$\frac{2\ \text{k}\Omega + \Delta R}{5.5\ \text{k}\Omega} - \frac{4\ \text{k}\Omega}{11\ \text{k}\Omega} = 632 \times 10^{-6},$$

$$\frac{2(2\ \text{k}\Omega + \Delta R) - 4\ \text{k}\Omega}{11\ \text{k}\Omega} = 632 \times 10^{-6},$$

$$2\Delta R = 0.632 \times 10^{-6} \times 11\ \text{k}\Omega,$$

$$\Delta R = \frac{0.632 \times 11}{2}$$

$$= 3.5\ \Omega.$$

Referring to Equation 6-7, it is seen that if the difference between V_2 and V_1 is increased, the galvanometer current I_g is increased. $V_2 - V_1$ can be increased by using a larger supply voltage E_B. Also from Equation 6-7, if I_g is made smaller by using a more sensitive galvanometer, then $V_2 - V_1$ can be reduced. Thus, the bridge sensitivity can be improved either by increasing E_B or by using a more sensitive galvanometer.

6-3-4 Range of Measurement

For accurate resistance measurements by the Wheatstone bridge, the resistances to be measured must always be much greater than contact and connecting-lead resistances. When these quantities are an appreciable fraction of the resistance to be measured, then the lower limit of the bridge has been reached. Figure 6-6 illustrates the effect of connecting-lead resistance. The galvanometer could be connected to terminal a or b. If the connecting lead resistance is $Y\ \Omega$, then the measured resistance is either

$$R = \frac{(S + Y)P}{Q} \quad \text{or} \quad R = \frac{SP}{Q + Y}.$$

The practical lower limit for accurate resistance measurement by the Wheatstone bridge is found to be approximately 5 Ω.

Very low resistance measurement requires special techniques and a different kind of resistance bridge. This is discussed in Section 6-4. The Wheatstone bridge may be used for measurement of very high resistance, although again special techniques are required (see Section 6-5). The upper limit of measurement for the Wheatstone bridge is around 10^{11} Ω.

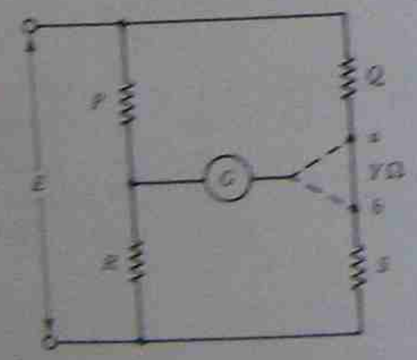


FIGURE 6-6. Connecting leads can cause errors in a Wheatstone bridge when measuring very low resistances.

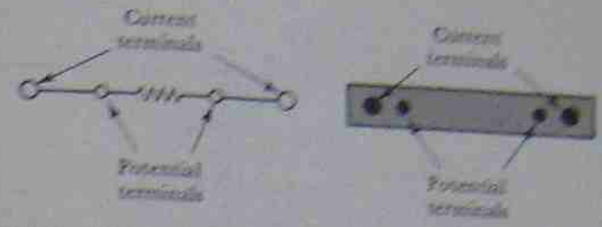


FIGURE 6-7. Circuit symbol and construction of a four-terminal resistor.

6-4 LOW RESISTANCE MEASUREMENT

Low-value resistors such as ammeter shunts must have the resistor terminals accurately defined. This is to avoid errors introduced by contacts which are carrying heavy currents. Two sets of terminals are provided, *current terminals* and *potential terminals* (see Figure 6-7). The current terminals are the largest and are at the outer extremes of the resistor. Leads which carry large currents are connected to the current terminals. The potential terminals are situated between the two current terminals, and these normally handle currents in the microampere or milliampere range. Thus, there is no significant contact voltage drop at the potential terminals. The resistance of the component is defined as that existing between the potential terminals.

6-4-1 Four Terminal Resistors

6-4-2 The Kelvin Bridge

Referring to Figure 6-6, it was explained that the voltage drop across the connecting lead between a and b introduces serious error when measuring low-value resistances. The Kelvin Bridge in Figure 6-8 shows essentially the same circuit as Figure 6-6, with additional resistors p and r. If the ratio p/r is exactly the same as P/R, then the error due to the voltage drop across Y is eliminated. The balance equation for this bridge is a little more difficult to derive than that for the Wheatstone bridge.

When the galvanometer indicates null, there is zero current through the galvanometer, and the galvanometer terminal voltage is $V_g = 0$, as illustrated. With the bridge in this condition, a current i_1 flows through P, and the same current passes through R. Also, a current I flows through Q. This splits up at terminal a, so that i_2 flows through p and r, and $I - i_2$ flows through Y. The current flowing in S is again I.

Since there is no potential difference between the galvanometer terminals when the bridge is balanced, the voltage across R is equal to the sum of the voltage drops across r and S:

$$i_1 R = i_2 r + IS,$$

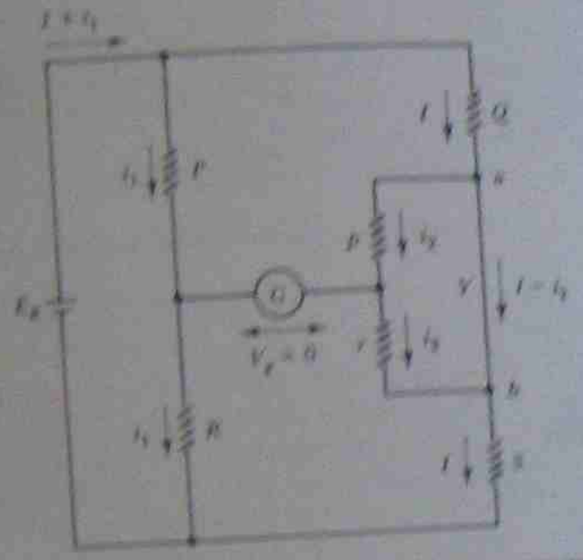


FIGURE 6-8 Kelvin bridge for low resistance measurement.

from which

$$IS = i_1R - i_3r \tag{1}$$

or

$$IS = R(i_1 - i_3r/R).$$

Also, the voltage drop across P equals the sum of the voltage drops across p and Q:

$$i_1P = i_2p + IQ,$$

which gives

$$IQ = i_1P - i_2p, \tag{2}$$

or

$$IQ = P(i_1 - i_2p/P).$$

Dividing Equation (2) by (1) gives

$$\frac{IQ}{IS} = \frac{P(i_1 - i_2p/P)}{R(i_1 - i_3r/R)},$$

and $p/r = P/R$ or $p/P = r/R$. Therefore, $Q/S = P/R$,

$$\boxed{Q = \frac{SP}{R}} \tag{3}$$

giving

S is usually a standard low-value resistance, and P, R, p, and r are

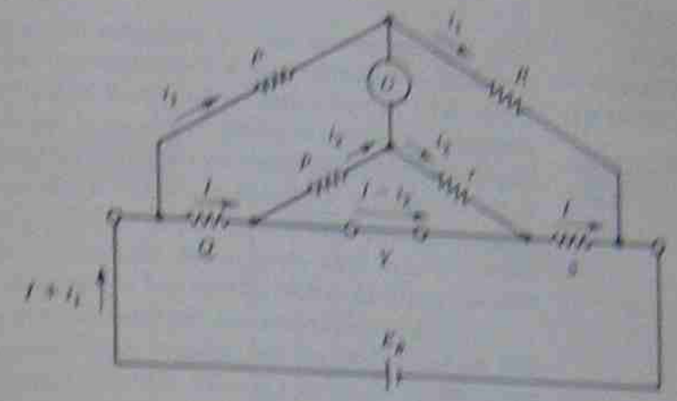


FIGURE 6-9 Kelvin bridge circuit showing four terminal resistors Q and S.

adjustable resistances. The bridge may be balanced by adjustment of P, R, p, and r, always maintaining the ratio $p/r = P/R$. Then, the unknown low-value resistance can be determined by substituting into Equation 6-8.

Figure 6-9 shows the usual way that the Kelvin bridge circuit is shown. S and Q are seen to be four terminal resistors, and P, p, R, and r are connected at their potential terminals.

The range of measurement of a Kelvin bridge is typically from 10 $\mu\Omega$ (or 0.00001 Ω) to 1 Ω. Depending upon the component accuracies, the bridge measurement accuracy can be $\pm 0.2\%$. Even lower resistance values (down to 0.1 $\mu\Omega$) can be measured with reduced accuracy.

Like the Wheatstone bridge, the current sensitivity of the galvanometer is important in determining the measurement sensitivity (and precision) of the Kelvin bridge. The sensitivity of a Kelvin bridge is determined essentially by the same method as used for a Wheatstone bridge.

EXAMPLE 6-7 A four-terminal resistor with an approximate value of 0.15 Ω is to be measured by use of a Kelvin bridge. A standard resistor of 0.1 Ω is available. Determine the required ratio of R/P and r/p.

SOLUTION

$$S = 0.1\ \Omega,$$
$$Q = 0.15\ \Omega.$$

From Equation 6-8:

$$\frac{R}{P} = \frac{S}{Q} = \frac{0.1}{0.15}$$
$$= \frac{10}{15}$$

6-5 HIGH RESISTANCE MEASUREMENT

Very high resistances, such as insulation resistances, can be measured by means of a voltmeter and a microammeter connected, as illustrated in Figure 6-10. A high voltage supply must be used to produce a measurable current. The current is extremely low, so a microammeter is necessary for current measurement. The voltmeter must be connected across the supply. If the voltmeter is connected across the resistance, the microammeter will measure the voltmeter current, which is likely to be much greater than the resistor current. The value of the resistance is, of course, determined by substituting the measured current and voltage into Ohm's law.

A problem that occurs with the measurement of very high resistances is that normally there are two resistive components: a *volume resistance* and a *surface leakage resistance*. Consider the metal-sheathed cable illustrated in Figure 6-11(a). When a voltage is applied, there are two components of current: a volume current I_v which flows from the core through the insulation to the metal sheath, and a surface leakage current I_s which flows across the surface of the insulation. Both currents flow through the microammeter. The consequence of this is that the resistance calculated from the instrument readings is the parallel combination of volume resistance and surface leakage resistance. For most practical purposes, this combined surface and volume resistance is the effective resistance of the insulation. However, in some circumstances, the two resistances must be separated.

To separate the two resistive components, a *guard wire* is employed, as illustrated in Figure 6-11(b). This is simply several turns of wire wrapped tightly around the insulation. The guard wire is connected to the supply, so I_s (from the guard ring to the sheath) no longer flows through the microammeter. There is no significant surface leakage current between the conductor and the guard wire, because the potential difference between conductor and guard wire is only the voltage drop across the microammeter. All of the supply voltage appears across the insulation between the guard wire and sheath, so the surface leakage current here is still relatively large.

Since the microammeter measures only I_v, in the arrangement shown in Figure 6-11(b), the volume resistance of the insulation is easily

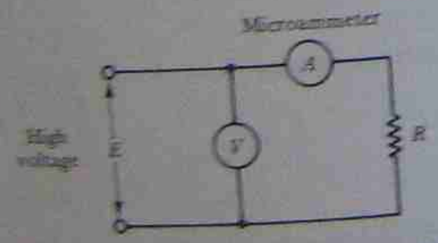
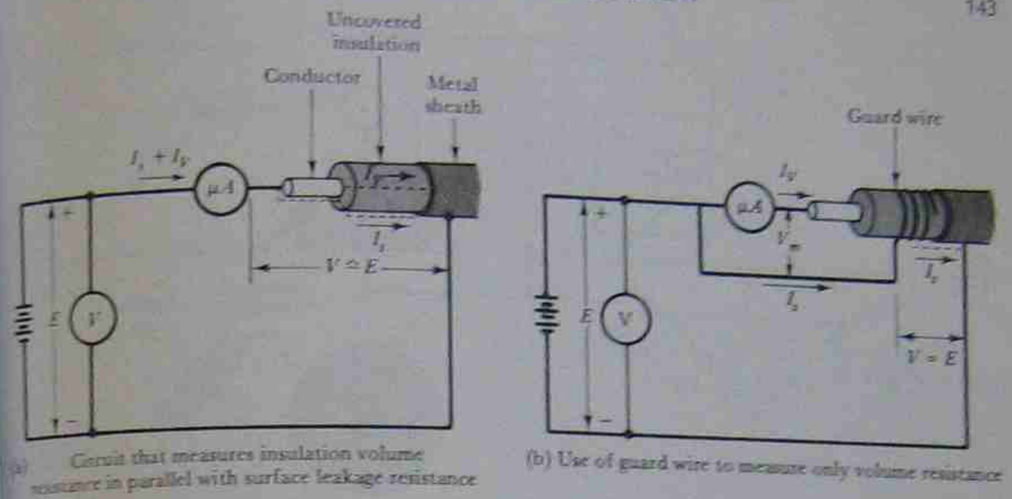


FIGURE 6-10. Circuit for measurement of very high resistances.



(a) Circuit that measures insulation volume resistance in parallel with surface leakage resistance

(b) Use of guard wire to measure only volume resistance

FIGURE 6-11. Guard wire method of measuring the insulation resistance of a cable.

calculated:

$$r_v = \frac{E}{I_v} \tag{6-9}$$

EXAMPLE 6-8 The insulation of a metal-sheathed electric cable is tested using a 10 000 V supply and a microammeter. A current of 5 μA is measured when the components are connected as in Figure 6-11(a). When the circuit is arranged, as in Figure 6-11(b), the current is 1.5 μA. Calculate the volume resistance of the cable insulation. Also calculate the surface leakage resistance.

SOLUTION

Volume resistance:

$$I_v = 1.5\ \mu\text{A},$$

$$r_v = \frac{E}{I_v} = \frac{10\,000\ \text{V}}{1.5\ \mu\text{A}} = 6.7 \times 10^9\ \Omega.$$

Surface leakage resistance:

$$I_v + I_s = 5\ \mu\text{A},$$

$$I_s = 5\ \mu\text{A} - I_v = 5\ \mu\text{A} - 1.5\ \mu\text{A}$$

$$= 3.5\ \mu\text{A},$$

$$r_s = \frac{E}{I_s} = \frac{10\,000\ \text{V}}{3.5\ \mu\text{A}} = 2.9 \times 10^9\ \Omega.$$

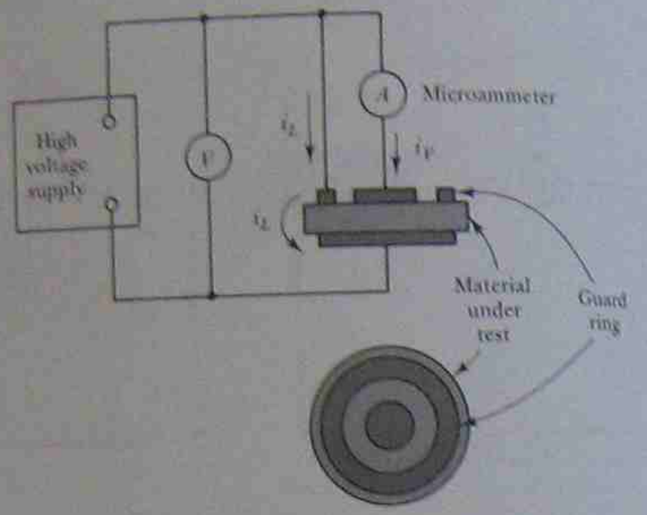


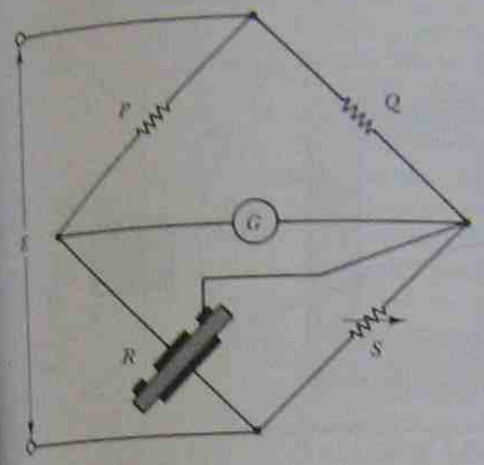
FIGURE 6-12. Measurement of the resistance of a sample of insulating material using the guard-ring method.

Figure 6-12 shows a disc-shaped sample of insulation material under test, using two metal plates and a *guard ring*. Like the guard wire in Figure 6-11, the *guard ring* removes the surface leakage current from the microammeter.

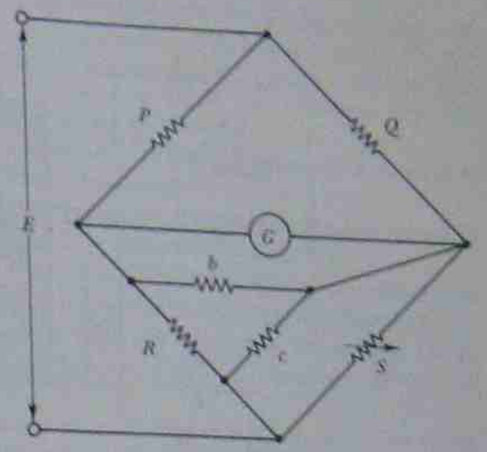
Figure 6-13(a) shows a Wheatstone bridge employed for measurement of insulation resistance. In this case the guard ring is connected to the opposite side of the galvanometer from the upper plate. When the bridge is balanced, the galvanometer indicates null, and there is zero potential difference across its terminals. Thus, there is zero potential difference between the upper plate and the guard ring, and consequently no surface leakage current flows from the upper plate to the guard ring.

In Figure 6-13(b) the insulation sample is replaced by its equivalent circuit. Resistance R represents the volume resistance of the material. Resistance b represents the surface resistance between the upper plate and the guard ring, while c is the surface resistance between the guard ring and lower plate. As already stated, when the bridge is in balance, there is zero voltage across b, so it can be ignored. Resistance c appears in parallel with the bridge resistor S. If c is very much larger than S (which it usually is) then c too can be ignored. The bridge is now reduced to its usual four components, with volume resistance R being the unknown value to be determined. Once again, Equation 6-4 is applicable.

When used for high resistance measurements, a Wheatstone bridge must have a very high supply voltage. All components and terminals must be well insulated, and great care should be exercised to avoid electric shock.



(a) Insulation resistance measurement with guard ring connected to opposite side of galvanometer from upper plate



(b) Showing equivalent circuit of volume resistance (R) and surface resistances (b and c)

FIGURE 6-13. Application of Wheatstone bridge to measurement of very high resistances.

6-6 THE MEGOHMMETER

The *Megohmmeter* or *megger* is a portable deflection instrument widely used to check the insulation resistance of electrical cables and equipment. The instrument has an internal source of high voltage provided from a hand-cranked generator. This voltage may be anything from 100 V to 5000 V. The circuit diagram of a megger is shown in Figure 6-14.

As illustrated, the pointer is deflected by a PMMC system with two coils. There is no mechanical controlling force; instead, the coils are connected to oppose each other. One coil is identified as a *control coil* and the other as a *deflection coil*.

The control coil is supplied from the generator via standard resistor R_1, so that the controlling force is proportional to the generator voltage divided by R_1. The deflecting coil is supplied via R_x, the resistance to be measured, and R_2, the internal deflection circuit resistance. The deflecting force is proportional to the generator voltage divided by $R_x + R_2$. Deflection is proportional to the difference between R_1 and $R_x + R_2$, and the instrument scale can be calibrated to directly indicate R_x.

When the megger is measuring an open-circuit, no current flows in the deflecting coil. In this case, the force from the control coil causes the pointer to be deflected to one end of the scale. This end is marked *infinity*

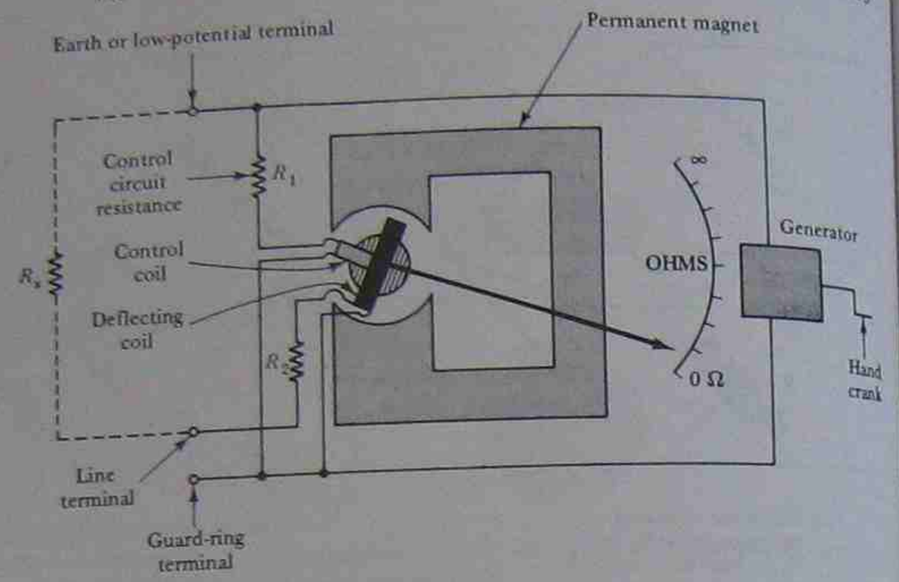


FIGURE 6-14. The megohmmeter.

(∞). When measuring a short-circuit, the deflecting coil force is very much greater than that from the control coil. Consequently, the pointer is deflected to the opposite end of the scale from infinity, and this end is marked 0 Ω. When the pointer is stationary at the center of the scale, the deflecting and control forces are equal, and $R_x + R_2 = R_1$, or $R_x = R_1 - R_2$. The scale is marked equal to $(R_1 - R_2)$ Ω at this point and is proportionately marked at other points. Range changing can be effected by switching to different values of R_2.

In Figure 6-14, note that a guard-ring terminal is provided to facilitate measurement of volume resistance.

REVIEW QUESTIONS AND PROBLEMS

6-1. Show how you would connect an ammeter and voltmeter to measure: (a) a very high resistance, (b) a very low resistance. Briefly explain.

6-2. An ammeter is connected in series with an unknown resistance (R_x), and a voltmeter is connected directly across the supply. The ammeter resistance is $R_a = 10$ Ω, and the voltmeter sensitivity is 10 kΩ/V. Each instrument is accurate to ±1%. Find the maximum and minimum values of R_x if the ammeter indicates 0.5 A on a 1-A range, and the voltmeter reading is 500 V on a 1000-V range.

6-3. A voltmeter is connected directly in parallel with an unknown resistance (R_x), and an ammeter is connected in series with the supply. The ammeter resistance is 0.1 Ω. The voltmeter is on its 5-V range and has a sensitivity of 10 000 Ω/V. When the voltmeter was indicating exactly 5 V, the ammeter reading was 0.6 mA on a 1-mA range. Find: (a) the nominal resistance of R_x, (b) the maximum and minimum resistances that R_x can be if the voltmeter and the ammeter each have an accuracy of ±1%.

6-4. Show how you could measure a resistance by means of: a dc supply, an ammeter, and a decade resistance box.

6-5. Show how a potentiometer, a standard resistor, and a power supply could be used to measure an unknown resistance.

6-6. Sketch the circuit of a Wheatstone bridge. Explain the operation of the bridge, and derive an equation for the unknown resistance.

6-7 The Wheatstone bridge in Figure 6-4 has: $P = 100$ Ω, $Q = 150$ Ω. The bridge is balanced when $S = 119.25$ Ω. Calculate the value of the unknown resistance.

6-8. A Wheatstone bridge circuit, as in Figure 6-4, can have $P = (1$ kΩ, 5 kΩ, or 10 kΩ), and $Q = (1$ kΩ, 5 kΩ, or 10 kΩ). S can be adjusted from a minimum of 1 kΩ to a maximum of 6 kΩ. Calculate the maximum and minimum values of unknown resistance that can be measured on the bridge.

6-9. A Wheatstone bridge with a 10-V supply and all four resistors equal to 5 kΩ has a galvanometer with a sensitivity of 0.005 μA/mm. The galvanometer resistance is 25 Ω. Determine the minimum detectable change in the unknown resistance.

6-10. A Wheatstone bridge has $Q = 100$ Ω, 1 kΩ, or 100 kΩ and $P = 1$ kΩ. S can be adjusted from 1 kΩ to 5 kΩ. Determine the maximum and minimum values of unknown resistance that can be measured.

6-11. The bridge in Question 6-10 has a galvanometer with a sensitivity of 0.005 μA/mm, and a resistance of 100 Ω. What is the minimum unbalance Δr of the unknown resistance (R) that can be detected when all bridge resistors are 1 kΩ and the supply voltage is 20 V?

6-12. A Wheatstone bridge has ratio arms P and Q that are accurate to ±0.025% and adjustable arms accurate to ±0.05%. What is the maximum possible error in resistance measurements made on this bridge?

6-13. Sketch the circuit of a bridge that can be employed for the measurement of very low resistances. Derive an expression for the unknown resistance in terms of the other bridge components.

6-14. A four-terminal resistor with an approximate resistance of 0.025 Ω is to be measured on a Kelvin bridge (as in Figure 6-9). A standard resistor of 0.01 Ω is available. Determine the required ratio of R/P and r/p.

6-15. A Kelvin bridge, as in Figure 6-9, has: $P = 12$ kΩ, $R = 3.673$ kΩ, $p = 12$ kΩ, $r = 3.673$ kΩ, and $S = 0.015$ Ω. Calculate the unknown resistance (Q).

6-16. Sketch circuits showing the guard-ring and guard-wire methods of measuring insulation resistance. Briefly explain in each case.

6-17. A 12000-V supply and a microammeter are used to measure the insulation resistance of a disc of material, as in Figure 6-12. With the guard ring not connected, the measured current is 1.2 μA. When the ring is connected directly to the supply, the current falls to 0.9 μA. Calculate the volume resistance and surface leakage resistance of the material.

6-18. Show by means of a sketch how a Wheatstone bridge may be used with the guard-ring method for measurement of insulation resistance. Explain how only the volume resistance of the material is calculated from the bridge balance equation.

6-19. Sketch the circuit diagram of a megohmmeter, and explain its operation.

7

ALTERNATING CURRENT BRIDGES

INTRODUCTION

Alternating current bridges are adoptions of the Wheatstone bridge for measurements of inductance, capacitance, effective resistance, Q factor, dielectric loss, and frequency. An ac power supply must be used and depending upon the application, the frequency may be 60 Hz from a power transformer, or it may be audio frequency or high frequency from a signal generator. The null detector must also be an ac instrument. A simple rectifier voltmeter could be used, but its sensitivity may not be satisfactory. Suitable null detectors include headphones, oscilloscopes, and electronic galvanometers.

With an ac bridge there are two components to be adjusted to obtain balance conditions. One component is first adjusted for the best available null, then the other component is adjusted to further improve the null. The first component is again adjusted and then the second component once more. This process is repeated until the best possible null is obtained.

As in the case of the Wheatstone bridge, several known standard components are employed, and when balance is obtained the parameters of the unknown component are calculated in terms of the known quantities.

7-1 GENERAL ac BRIDGE THEORY

The general circuit of an ac bridge is illustrated in Figure 7-1. This is exactly the same as the Wheatstone bridge circuit (Figure 6-4) except that impedances are shown instead of resistances. Also, an ac supply is used, and the null detector must be an ac instrument.

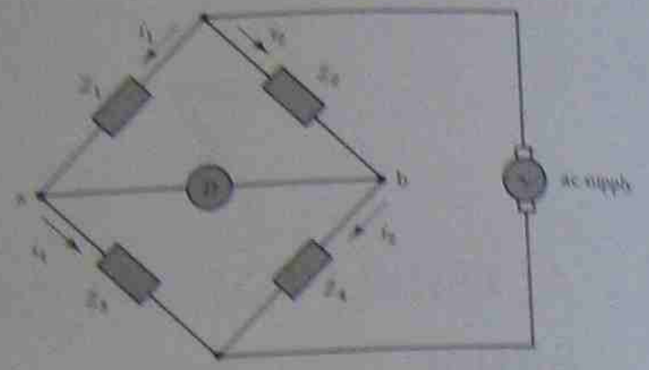


FIGURE 7-1. General ac bridge circuit.

When the null detector indicates zero in the circuit of Figure 7-1, the alternating voltage across points a and b is zero. This means (as in the Wheatstone bridge) that the voltage across Z_1 is exactly equal to that across Z_2, and the voltage across Z_3 equals the voltage drop across Z_4. Not only are the voltages equal in amplitude, they are also equal in phase. If the voltages were equal in amplitude but not in phase, the ac null detector would not indicate zero.

Since
$$V_{Z1} = V_{Z2}, \tag{1}$$
$$i_1 Z_1 = i_2 Z_2,$$
and
$$V_{Z3} = V_{Z4}, \tag{2}$$
or
$$i_1 Z_3 = i_2 Z_4.$$

Dividing Equation (1) by Equation (2):

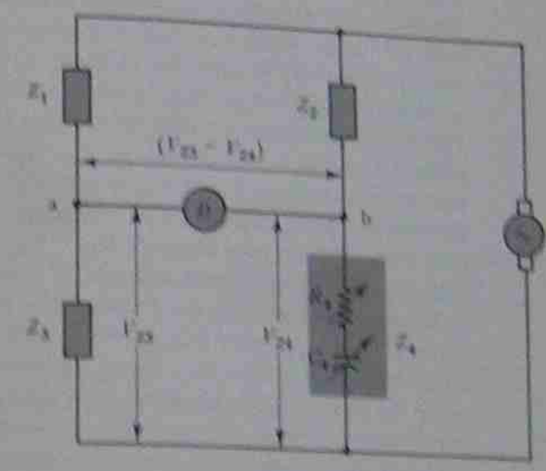
$$\frac{i_1 Z_1}{i_1 Z_3} = \frac{i_2 Z_2}{i_2 Z_4},$$

giving

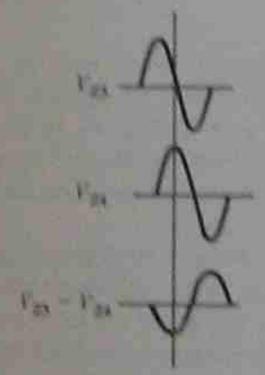
$$\boxed{\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4}}. \tag{7-2}$$

As already stated, the bridge balance is obtained only when the voltages at each terminal of the null detector are equal in phase as well as in magnitude. This results in Equation 7-1 which involves complex quantities. In such an equation, the real parts of the quantities on each side must

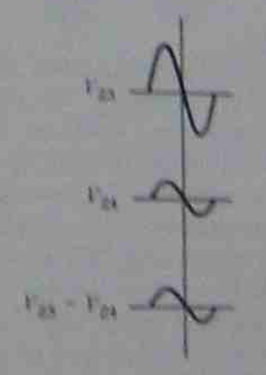
be equal, and the imaginary parts of the quantities must also be equal. Therefore, when deriving the balance equations for a particular bridge, it is best to express the impedances in rectangular form rather than polar form. The real quantities can then be equated to obtain one balance equation, and the imaginary (or j quantities) can be equated to arrive at the other balance equation.



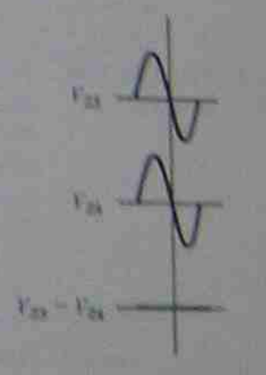
(a) Null detector voltage = $(V_{23} - V_{24})$



(b) V_{23} and V_{24} equal but not in-phase



(c) V_{23} and V_{24} in-phase but not equal in amplitude



(d) V_{23} and V_{24} equal and in-phase

FIGURE 7-2. When an ac bridge is balanced, V_{23} and V_{24} must be in-phase and equal in amplitude.

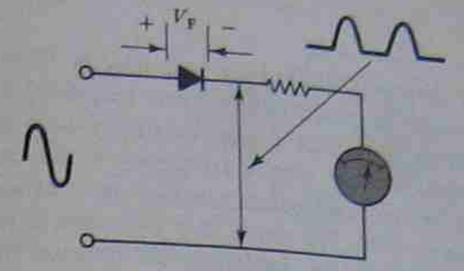
The need for two balance equations arises from the fact that capacitances and inductances are never pure; they must be defined as a combination of R and C or R and L. One balance equation permits calculation of L or C, and the other is used for determining the R quantity.

As already explained, two component adjustments are required to balance the bridge (or obtain a minimum indication on the null detector). These adjustments are *not* independent of each other; one tends to affect the relative amplitudes of the voltages at each terminal of the null detector, and the other adjustment has a marked effect on the relative phase difference of these voltages. For example, Z_4 in Figure 7-1 might consist of a variable capacitor in series with a variable resistor, as illustrated in Figure 7-2(a). Adjustment of C_4 may make V_{Z4} equal in amplitude to V_{Z3} without bringing it into phase with V_{Z3}. The result is, of course, that the null detector voltage $V_{Z3} - V_{Z4}$ is not zero [see Figure 7-2(b)]. Further adjustment of C_4 could alter the phase of V_{Z4} but will also alter its amplitude. If R_4 is now adjusted, $V_{Z3} - V_{Z4}$ might be further reduced by bringing the voltages closer together in phase. However, this cannot be achieved without altering the amplitude of V_{Z4}, which is the voltage drop across R_4 and C_4 [Figure 7-2(c)]. When the best null has been obtained by adjustment of R_4, C_4 is once again adjusted. This is likely to once more make V_{Z4} close to V_{Z3} in amplitude, but again has an unavoidable effect on the phase relationship. The procedure of alternately adjusting R_4 and C_4 to minimize the null detector voltage is continued until the smallest possible indication is obtained. Then, V_{Z4} is equal to V_{Z3} both in magnitude and phase [Figure 7-2(d)].

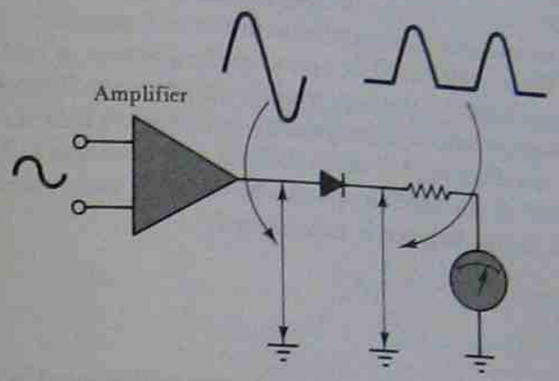
7-2 DETECTORS FOR ac BRIDGES

Figure 7-3 illustrates several instruments which may be used as null detectors in ac bridges. The simplest and least sensitive is the rectifier PMMC instrument illustrated in Figure 7-3(a). As in the case of the Wheatstone bridge, the null detector must be shunted by an adjustable resistor to protect it from excessive current levels when the bridge is off balance (Figure 1-10).

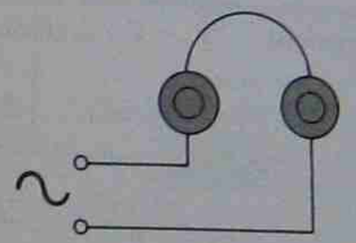
The voltage drop (V_F) across the rectifier [in Figure 7-3(a)] obviously limits the lowest detectable ac voltage to an amplitude greater than V_F. The sensitivity is greatly improved by the use of an amplifier, as shown in Figure 7-3(b). The low-level ac (null) voltage is amplified before rectification. If the PMMC instrument and rectifier alone can detect a minimum voltage amplitude of say 1 V, then by using an amplifier with a gain of 1000 the minimum detectable level is reduced to 1 V/1000 = 1 mV. When the amplifier is included, the instrument essentially becomes an electronic voltmeter or an electronic galvanometer (see Chapter 8). A sensitive ac electronic voltmeter (analog or digital) could be used as an ac bridge null detector. The frequency of the bridge supply must not exceed



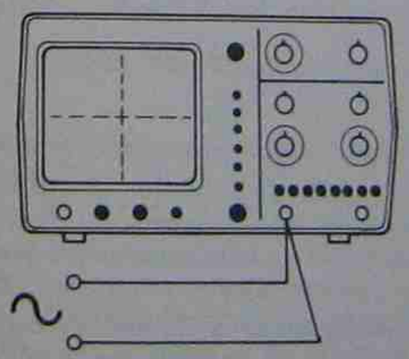
(a) PMMC instrument with rectifier.



(b) Amplifier, PMMC instrument, and rectifier.



(c) Headphones for use at audio frequencies.



(d) An oscilloscope can be used at all frequencies.

FIGURE 7-3. Various null detectors that may be used with ac bridges.

the upper frequency limit of the null detector. This is typically 1 MHz for most electronic instruments. The lower frequency limit is around 20 Hz.

Headphones [Figure 7-3(c)] can be a very suitable detector for ac bridges when using a supply frequency in the 500-Hz to 5-kHz range. When the bridge is off balance, a high level of sound is produced at the headphone outputs. The sound level decreases to zero as bridge balance is approached. When the bridge is off balance the sound level can be adjusted to an acceptable (comfortable hearing) level by controlling the supply voltage to the bridge. Alternatively, an adjustable (shunt) resistor can be connected in parallel with the null detector.

For a wide range of operating frequencies, a cathode-ray oscilloscope [Figure 7-3(d)] is the best possible null detector. The oscilloscope displays a large amplitude voltage when the bridge is off balance and flattens out to a very low level display when the best null is achieved. The *deflection sensitivity* (V/cm) of the oscilloscope can be adjusted for maximum possible sensitivity as bridge balance is approached.

7-3 SIMPLE CAPACITANCE BRIDGE

The circuit of a *simple capacitance bridge* is illustrated in Figure 7-4(a). Z_1 is a standard capacitor C_1, and Z_2 is the unknown capacitance C_x. Z_3 and Z_4 are known variable resistors, such as decade resistance boxes. When the bridge is balanced, $Z_1/Z_3 = Z_2/Z_4$ (Equation 7-1) applies:

$$Z_1 = -j1/\omega C_1, \qquad Z_2 = -j1/\omega C_x,$$
$$Z_3 = R_3 \quad \text{and} \quad Z_4 = R_4.$$

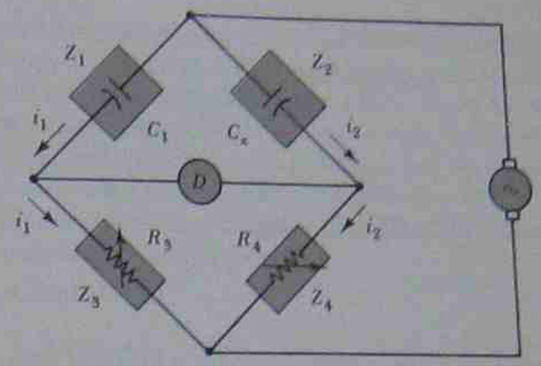
Therefore,
$$\frac{-j1/\omega C_1}{R_3} = \frac{-j1/\omega C_x}{R_4},$$

or
$$\frac{1}{C_1 R_3} = \frac{1}{C_x R_4},$$

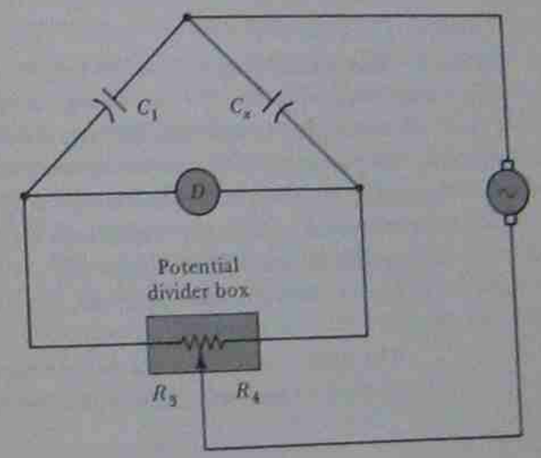
giving

$$\boxed{C_x = \frac{C_1 R_3}{R_4}}. \tag{7-2}$$

The actual values of R_3 and R_4 are not important if their ratio is known. Thus, a capacitance bridge is easily constructed using a potential



(a) Capacitance bridge using standard capacitor (C_1) and two adjustable resistors (R_3 and R_4) to measure unknown capacitance (C_x)



(b) Bridge circuit as in (a) above but with R_3 and R_4 replaced by a potential divider

FIGURE 7-4. Simple capacitance bridge circuits.

divider resistance box and a standard capacitor. The circuit is shown in Figure 7-4(b).

EXAMPLE 7-1 The standard capacitance value in Figure 7-4(b) is $C_1 = 0.1\ \mu F$, and the potential divider box can be set to any ratio between $R_3/R_4 = 100:1$ and $R_3/R_4 = 1:100$. Calculate the range of measurements of unknown capacitance C_x that can be made on the bridge.

SOLUTION

Equation 7-2,

$$C_x = \frac{C_1 R_3}{R_4}$$

For $R_3 / R_4 = 100:1$:

$$C_x = 0.1\ \mu\text{F} \times \frac{100}{1}$$
$$= 10\ \mu\text{F}.$$

For $R_3 / R_4 = 1:100$:

$$C_x = 0.1\ \mu\text{F} \times \frac{1}{100}$$
$$= 0.001\ \mu\text{F}.$$

The phasor diagram for the simple capacitance bridge when balanced is shown in Figure 7-5. The voltage drops across R_3 and R_4 are shown as i_1R_3 and i_2R_4. At balance, they are equal and in phase. Also, since R_3 and R_4 are purely resistive quantities, currents i_1 and i_2 are in phase with i_1X_2 and i_2R_4, as illustrated. The voltage drop across C_1 is i_1X_{c1} or $i_1/\omega C_1$. The impedance X_{c1} is purely capacitive, so the current through it leads the voltage by 90°. i_1 leads i_1X_{c1} by 90°, or i_1X_{c1} lags i_1 by 90°, as shown in the phasor diagram. Similarly, X_{cx} is purely capacitive, and i_2X_{cx} lags i_2 by 90°.

The above analysis of the simple capacitance bridge assumes that the capacitors are absolutely pure, with effectively zero leakage current through

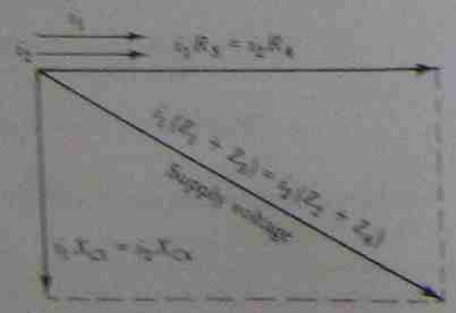


FIGURE 7-5. Phasor diagram for the simple capacitance bridge.

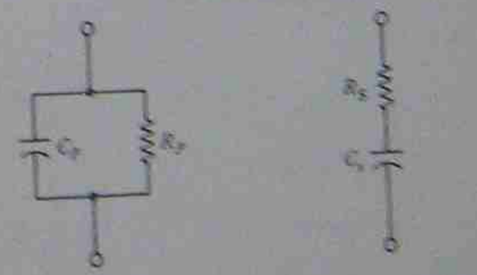
the dielectric. If a resistance were connected in series or in parallel with C_x in Figure 7-4(a), and the rest of the bridge components remain as shown, balance would be virtually impossible to achieve. This is because i_1 and i_2 could not be brought into phase, and, consequently, i_1R_3 and i_2R_4 would not be in phase. As further discussed in Section 7-4, the equivalent circuit of a leaky capacitor is a pure capacitance in parallel with a pure resistance. Thus, the simple capacitance bridge is suitable only for measurement of capacitors with high resistance dielectrics.

7-4 CR AND LR EQUIVALENT CIRCUITS Q FACTOR AND D FACTOR

7-4-1 Capacitor Equivalent Circuits

The equivalent circuit of a capacitor consists of a pure capacitance C_p and a parallel resistance R_p, as illustrated in Figure 7-6(a). C_p represents the actual capacitance value, and R_p represents the resistance of the dielectric or *leakage resistance*. Capacitors which have a high leakage current flowing through the dielectric have a relatively low value of R_p in their equivalent circuit. Very low leakage currents are represented by extremely large values of R_p. Examples of the two extremes are electrolytic capacitors which have high leakage currents (low parallel resistance), and air capacitors which have very low leakage (high parallel resistance).

A parallel *CR* circuit has an equivalent series *CR* circuit [Figure 7-6(b)]. Either one of the two equivalent circuits (series or parallel) may be used to represent a capacitor in a bridge circuit. Usually, one equivalent circuit is more convenient than the other for each particular bridge circuit. It is found that capacitors with a high resistance dielectric are best represented by the series *CR* circuit, while those with low resistance dielectric should be represented by the parallel equivalent circuit. However, when the capacitor is measured in terms of the series C and R



(a) Parallel equivalent circuit (b) Series equivalent circuit

FIGURE 7-6. Capacitor equivalent circuits.

quantities, it is usually desirable to resolve them into the parallel equivalent circuit quantities. This is because the (parallel) leakage resistance between represents the quality of the capacitor dielectric. Equations that relate the series and parallel equivalent circuits are derived below.

Referring to Figure 7-6, the series impedance is

$$Z_s = R_s - jX_s,$$

and the parallel admittance is

$$Y_p = \frac{1}{R_p} + j\frac{1}{X_p} = G_p + jB_p,$$

where G is conductance and B is susceptance. The impedances of each circuit must be equal.

Thus, $$Z_s = \frac{1}{Y_p},$$

giving $$R_s - jX_s = \frac{1}{G_p + jB_p},$$

or $$G_p + jB_p = \frac{1}{R_s - jX_s}$$

$$= \frac{1}{R_s - jX_s}\left(\frac{R_s + jX_s}{R_s + jX_s}\right)$$

giving $$G_p + jB_p = \frac{R_s + jX_s}{R_s^2 + X_s^2}.$$

Equating the real terms,

$$G_p = \frac{R_s}{R_s^2 + X_s^2},$$

or

$$\boxed{R_p = \frac{R_s^2 + X_s^2}{R_s}.} \qquad (7\text{-}3)$$

Equating the imaginary terms,

$$B_p = \frac{X_s}{R_s^2 + X_s^2},$$

or

$$\boxed{X_p = \frac{R_s^2 + X_s^2}{X_s}.} \qquad (7\text{-}4)$$

The above equations can be shown to also apply to equivalent series and parallel LR circuits, as well as CR circuits.

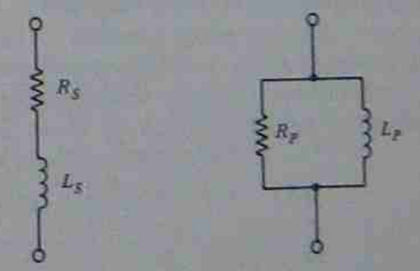
7-4-2 Inductor Equivalent Circuits

Inductor equivalent circuits are illustrated in Figure 7-7. The series equivalent circuit in Figure 7-7(a) represents an inductor as a pure inductance L_s in series with the resistance of its coil. This series equivalent circuit is normally the best way to represent an inductor, because the actual winding resistance is involved and this is an important quantity. Ideally, the winding resistance should be as small as possible, but this depends upon the thickness and length of the wire used to wind the coil. Physically small high-value inductors tend to have large resistance values, while large low inductance components are likely to have low resistances.

The parallel LR equivalent circuit for an inductor [Figure 7-7(b)] can also be used in ac bridge circuits. As in the case of the capacitor equivalent circuits, the bridge balance equations are sometimes more convenient to derive when a parallel LR equivalent circuit is employed rather than a series circuit. The equations relating the two are derived below.

Referring to Figure 7-7 the series circuit impedance is

$$Z_s = R_s + jX_s$$



(a) Series equivalent circuit (b) Parallel equivalent circuit

FIGURE 7-7. Inductor equivalent circuits.

and the parallel circuit admittance is

$$Y_p = \frac{1}{R_p} - j\frac{1}{X_p},$$

$$Y_p = G_p - jB_p,$$

$$Z_s = Z_p,$$

or

$$R_s + jX_s = \frac{1}{G_p - jB_p},$$

$$R_s + jX_s = \frac{1}{G_p - jB_p}\left(\frac{G_p + jB_p}{G_p + jB_p}\right),$$

giving

$$R_s + jX_s = \frac{G_p + jB_p}{G_p^2 + B_p^2}.$$

Equating the real terms:

$$R_s = \frac{G_p}{G_p^2 + B_p^2}$$

$$= \left(\frac{1/R_p}{1/R_p^2 + 1/X_p^2}\right)\left(\frac{R_p^2 X_p^2}{R_p^2 X_p^2}\right)$$

$$\boxed{R_s = \frac{R_p X_p^2}{X_p^2 + R_p^2}} \tag{7-5}$$

Equating the imaginery terms:

$$X_s = \frac{B_p}{G_p^2 + B_p^2}$$

$$= \left(\frac{1/X_p}{1/R_p^2 + 1/X_p^2}\right)\left(\frac{R_p^2 X_p^2}{R_p^2 X_p^2}\right)$$

$$\boxed{X_s = \frac{R_p^2 X_p}{X_p^2 + R_p^2}} \tag{7-6}$$

Like Equations 7-3 and 7-4, Equations 7-5 and 7-6 apply to both *CR* and *LR* circuits.

7-4-3 Q Factor of an Inductor

The quality of an inductor can be defined in terms of its power dissipation. An ideal inductor should have zero winding resistance, and therefore zero power dissipated in the winding. A *lossy* inductor has a relatively high winding resistance; consequently it does dissipate some power. The *quality factor*, or *Q factor*, of the inductor defines the quality of the component as the ratio of component's reactance (at a given frequency) to coil resistance.

$$\boxed{Q = \frac{X_s}{R_s} = \frac{\omega L_s}{R_s}} \tag{7-7}$$

where L_s and R_s refer to the components of an *LR* series equivalent circuit [Figure 7-7(a)].

Ideally, ωL_s should be very much larger than R_s, so that a very large Q factor is obtained. Q factors for typical inductors range from a low of less than 5 to as high as 1000 (depending upon frequency).

As already discussed, an inductor may be represented by either a series equivalent circuit or a parallel equivalent circuit, [Figure 7-7(b)]. When the parallel equivalent circuit is employed, the Q factor can be shown to be

$$\boxed{Q = \frac{R_p}{X_p} = \frac{R_p}{\omega L_p}.} \tag{7-8}$$

7-4-4 D Factor of a Capacitor

The quality of a capacitor can be expressed in terms of its power dissipation. A very pure capacitance has a high dielectric resistance (low leakage current) and virtually zero power dissipation. A *lossy* capacitor, which has a relatively low resistance (high leakage current), dissipates some power. The *dissipation factor* D defines the quality of the capacitor. Like the Q factor of a coil, D is simply the ratio of the component reactance (at a given frequency) to the resistance measurable at its terminals. In the case of the capacitor, the resistance involved in the D factor calculation is that shown in the parallel equivalent circuit. (This differs from the inductor Q factor calculation, where the resistance is that in the series equivalent circuit.) Using the *parallel equivalent circuit*:

$$\boxed{D = \frac{X_p}{R_p} = \frac{1}{\omega C_p R_p}.} \tag{7-9}$$

Ideally, R_p should be very much larger than $1/(\omega C_p)$, giving a very small dissipation factor. Typically, D might range from 0.1 for electrolytic capacitors to less than 10^{-4} for capacitors with a plastic film dielectric (again depending upon frequency).

When a series equivalent circuit is used, the equation for dissipation factor can be shown to be

$$\boxed{D = \frac{R_1}{X_1} = \omega C_1 R_1} \qquad (7.9)$$

Comparing Equation 7.8 to 7.9 and Equation 7.10 to 7.7, it is [illegible] that in each case D is the reverse of Q.

7.3 WIRED-RESISTANCE CAPACITANCE BRIDGE

In the circuit shown in Figure 7.3(a), the unknown capacitance is represented as a pure capacitance C_1 in series with a resistance R_1. A standard adjustable resistance R_2 is connected in series with standard capacitor C_2. The voltage drop across R_1 balances the resistive voltage drop in [illegible] Z_1 when the bridge is balanced. The additional resistor in series with C_1 increases the total resistive component in Z_1, so that inconveniently [illegible] values of R_1 are not required to achieve balance. Bridge balance is [illegible] easily achieved when each capacitive branch has a substantial resistive component. To obtain balance, R_1 and either R_2 or R_3 are adjusted alternately. The [illegible] capacitance bridge is found to be more suitable for capacitors with a high resistance dielectric (very low leakage current and low dissipation factor).

When the bridge is balanced, Equation 7.4 applies:

$$\frac{Z_1}{R_2} = \frac{Z_2}{R_3}$$

giving

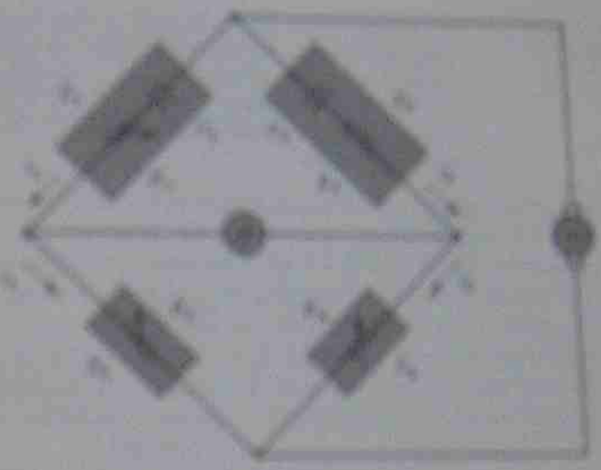
$$\boxed{\frac{R_1 - j(1/\omega C_1)}{R_2} = \frac{R_2 - j(1/\omega C_2)}{R_3}} \qquad (7.11)$$

Equating the real terms in Equation 7.11:

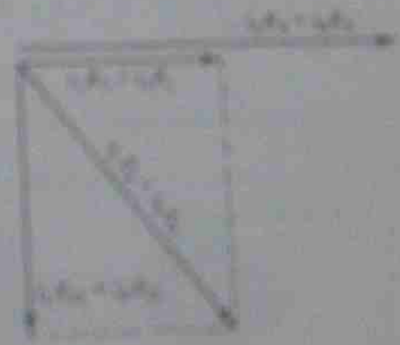
$$\frac{R_1}{R_2} = \frac{R_2}{R_3}$$

giving

$$\boxed{R_1 = \frac{R_2 R_3}{R_3}} \qquad (7.12)$$



(a) Circuit of [illegible] capacitance bridge



(b) Phase diagram for balanced bridge

FIGURE 7.4 The [illegible] capacitance bridge measures an unknown capacitance (C_1) by comparing it to a standard capacitor (C_2).

Equating the imaginary series in Equation 7.11:

$$\frac{1}{\omega C_1 R_2} = \frac{1}{\omega C_2 R_3}$$

which gives

$$\boxed{C_1 = \frac{C_2 R_3}{R_2}} \qquad (7.13)$$

EXAMPLE 7-2 A series-resistance capacitance bridge [as in Figure 7-8(a)] has a 0.4-μF standard capacitor for C_1, and $R_3 = 10\ \text{k}\Omega$. Balance is achieved with a 100-Hz supply frequency when $R_1 = 125\ \Omega$ and $R_4 = 14.7\ \text{k}\Omega$. Calculate the resistive and capacitive components of the measured capacitor and its dissipation factor.

SOLUTION

Equation 7-13,

$$\begin{aligned} C_x &= \frac{C_1 R_3}{R_4} \\ &= \frac{0.1\ \mu\text{F} \times 10\ \text{k}\Omega}{14.7\ \text{k}\Omega} \\ &= 0.068\ \mu\text{F}. \end{aligned}$$

Equation 7-12,

$$\begin{aligned} R_x &= \frac{R_1 R_3}{R_2} \\ &= \frac{125\ \Omega \times 14.7\ \text{k}\Omega}{10\ \text{k}\Omega} \\ &= 183.8\ \Omega. \end{aligned}$$

The capacitor series equivalent circuit consists of:

$$C_x = 0.068\ \mu\text{F}, \qquad R_x = 183.8\ \Omega$$

Equation 7-10,

$$\begin{aligned} D &= \omega C_x R_x \\ &= 2\pi \times 100\ \text{Hz} \times 0.068\ \mu\text{F} \times 183.8\ \Omega \\ &= 0.008. \end{aligned}$$

The phasor diagram for the series-resistance capacitance bridge at balance is drawn in Figure 7-8(b). The voltage drops across Z_3 and Z_4 are i_1R_3 and i_2R_4, respectively. These two voltages must be equal and in phase for the bridge to be balanced. Thus, they are drawn equal and in phase in the phasor diagram. Since R_3 and R_4 are resistive, i_1 is in phase with i_1R_3 and i_2 is in phase with i_2R_4. The impedance of C_1 is purely capacitive, and current leads voltage by 90° in a pure capacitance. Therefore, the capacitor voltage drop i_1X_{C1} is drawn 90° lagging I_1. Similarly, the voltage drop across C_x is i_2X_{Cx} and is drawn 90° lagging I_2. The resistive voltage drops i_1R_1 and i_2R_x are in phase with i_1 and i_2, respectively.

The total voltage drop across Z_1 is the phasor sum of i_1R_1 and i_1X_{C1}, as illustrated in Figure 7-8(b). Also i_2Z_2 is the phasor sum of i_2R_x and i_2X_{Cx}. Since i_2Z_2 must be equal to and in phase with i_1Z_1, i_1R_1 and i_2R_x are equal, as are i_1X_{C1} and i_2X_{Cx}.

7-6 PARALLEL-RESISTANCE CAPACITANCE BRIDGE

The circuit of a *parallel-resistance capacitance bridge* is illustrated in Figure 7-9. In this case, the unknown capacitance is represented by its parallel equivalent circuit; C_p in parallel with R_p. Z_3 and Z_4 are resistors, as before, either or both of which may be adjustable. Z_2 is balanced by a standard capacitor C_1 in parallel with an adjustable resistor R_1. Bridge balance is achieved by adjustment of R_1 and either R_3 or R_4. The parallel-resistance capacitance bridge is found to be most suitable for capacitors with a low resistance dielectric (relatively high leakage current and high dissipation factor).

At balance, Equation 7-1 once again applies:

$$\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4}$$

also

$$\begin{aligned} \frac{1}{Z_1} &= \frac{1}{R_1} - \frac{1}{j(1/\omega C_1)} \\ &= \frac{1}{R_1} + j\omega C_1. \end{aligned}$$

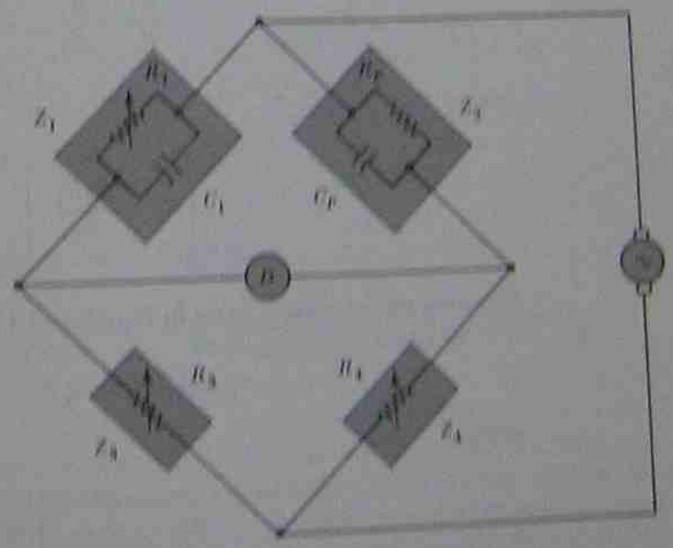


FIGURE 7-9. Parallel-resistance capacitance bridge circuit for measuring the parallel equivalent circuit components (C_p and R_p) of an unknown capacitor.

or $$Z_1 = 1/(1/R_1 + j\omega C_1),$$

and $$\frac{1}{Z_2} = \frac{1}{R_p} - \frac{1}{j(1/\omega C_p)}$$

$$= \frac{1}{R_p} + j\omega C_p,$$

or $$Z_2 = 1/(1/R_p + j\omega C_p).$$

Substituting into Equation 7-1:

$$\frac{1/(1/R_1 + j\omega C_1)}{R_3} = \frac{1/(1/R_p + j\omega C_p)}{R_4},$$

$$\frac{1}{R_3(1/R_1 + j\omega C_1)} = \frac{1}{R_4(1/R_p + j\omega C_p)},$$

or

$$\boxed{R_3(1/R_1 + j\omega C_1) = R_4(1/R_p + j\omega C_p).} \quad (7\text{-}14)$$

Equating the real terms in Equation 7-14:

$$\frac{R_3}{R_1} = \frac{R_4}{R_p},$$

giving

$$\boxed{R_p = \frac{R_1 R_4}{R_3}.} \quad (7\text{-}15)$$

Equating the imaginary terms in Equation 7-14:

$$\omega C_1 R_3 = \omega C_p R_4,$$

giving

$$\boxed{C_p = \frac{C_1 R_3}{R_4}.} \quad (7\text{-}16)$$

Note the similarity between Equation 7-15 and 7-12, and between Equations 7-16 and 7-13.

EXAMPLE 7-3 A parallel-resistance capacitance bridge (as in Figure 7-9) has a standard capacitance value of $C_1 = 0.1\ \mu F$ and $R_3 = 10\ k\Omega$. Balance is achieved at a supply frequency of 100 Hz when $R_1 = 375\ \Omega$, $R_3 = 10\ k\Omega$, and $R_4 = 14.7\ k\Omega$. Calculate the resistive and capacitive components of the measured capacitor and its dissipation factor.

SOLUTION

Equation 7-16,

$$C_p = \frac{C_1 R_3}{R_4}$$

$$= \frac{0.1\ \mu F \times 10\ k\Omega}{14.7\ k\Omega}$$

$$= 0.068\ \mu F.$$

Equation 7-15,

$$R_p = \frac{R_1 R_4}{R_3}$$

$$= \frac{375\ \Omega \times 14.7\ k\Omega}{10\ k\Omega}$$

$$= 551.3\ \Omega.$$

Equation 7-9,

$$D = \frac{1}{\omega C_p R_p}$$

$$= \frac{1}{2\pi \times 100\ Hz \times 0.068\ \mu F \times 551.3\ \Omega}$$

$$= 42.5.$$

EXAMPLE 7-4 Calculate the parallel equivalent circuit for the C_1 and R_1 values determined in Example 7-2. Also determine the component values of R_4 and R_4 required to balance the calculated C_p and R_p values in a parallel-resistance capacitance bridge. Assume that R_3 remains 10 kΩ.

SOLUTION

Equation 7-3,

$$R_p = \frac{R_s^2 + X_s^2}{R_s}.$$

$$R_s^2 = (183.8)^2 = 33.782 \times 10^3,$$

$$X_s = \frac{1}{2\pi f C_s}$$

$$= \frac{1}{2\pi \times 100\ \text{Hz} \times 0.068\ \mu\text{F}} = 23.405 \times 10^3\ \Omega$$

$$X_s^2 = 5.478 \times 10^8,$$

$$R_p = \frac{33.78 \times 10^3 + 5.478 \times 10^8}{183}$$

$$= 2.99\ \text{M}\Omega.$$

Equation 7-4,

$$X_p = \frac{R_s^2 + X_s^2}{X_s}.$$

$$X_p = \frac{33.78 \times 10^3 + 5.478 \times 10^8}{23.405 \times 10^3}$$

$$= 23.41 \times 10^3\ \Omega$$

$$C_p = \frac{1}{2\pi \times 100\ \text{Hz} \times 23.41\ \text{k}\Omega}$$

$$= 0.068\ \mu\text{F}.$$

From Equation 7-16,

$$R_4 = \frac{C_1 R_3}{C_p}$$

$$= \frac{0.1\ \mu\text{F} \times 10\ \text{k}\Omega}{0.068\ \mu\text{F}}$$

$$= 14.705\ \text{k}\Omega.$$

From Equation 7-15,

$$R_1 = \frac{R_3 R_p}{R_4}$$

$$= \frac{10\ \text{k}\Omega \times 2.99\ \text{M}\Omega}{14.705\ \text{k}\Omega}$$

$$= 2.033\ \text{M}\Omega.$$

Consider Examples 7-2, 7-3, and 7-4. In Example 7-2, a capacitor is measured as $C_s = 0.068\ \mu\text{F}$ and $R_s = 183.8\ \Omega$. In Example 7-4 these quantities are converted into the parallel equivalent circuit, giving $C_p = 0.068\ \mu\text{F}$ and $R_p = 2.99\ \text{M}\Omega$. Thus, this capacitor can be described as having a capacitance of 0.068 μF and a leakage resistance of 2.99 MΩ. This is a relatively high leakage resistance, and it gives the capacitor a very low dissipation factor ($D = 0.008$).

Example 7-4 also demonstrates that, if the capacitor in Example 7-2 were measured on a parallel-resistance bridge, the value of R_1 required to achieve bridge balance would be 2.033 MΩ. This is an inconveniently large value for a precision adjustable resistor. Such a resistance value would also keep the current low in branches Z_1 and Z_2 and thus minimize the bridge sensitivity (see Section 7-12).

In Example 7-3 another 0.068-μF capacitor is measured on a parallel-resistance capacitance bridge. In this case the dielectric resistance is $R_p = 551.3\ \Omega$. This is a relatively low dielectric resistance. (For example, if 10 V were applied across this capacitor, the leakage current would be 10 V/551.3 Ω = 18 mA.) The low leakage resistance gives the capacitor a high dissipation factor ($D = 42.5$). This capacitor is easily measured as a parallel equivalent circuit on the parallel-resistance capacitance bridge. Conversion of the C_p and R_p quantities into the equivalent series circuit quantities would demonstrate that this capacitor is not conveniently measured on a series-resistance capacitance bridge.

It is seen that (as already stated) the series-resistance capacitance bridge is most suitable for measurement of capacitors with a high resistance dielectric (low D factor). Also, the parallel-resistance capacitance bridge is best suited to measurement of capacitors with a low resistance dielectric (high D factor). Some capacitors which have neither very low nor very high dielectric resistance may be measured on either type of bridge. In this case it is best to use the parallel-resistance capacitance bridge, because the capacitor is then measured directly in terms of its (preferable) parallel equivalent circuit.

7-7 THE INDUCTANCE COMPARISON BRIDGE

The circuit of the *inductance comparison bridge* shown in Figure 7-10 is similar to the series-resistance capacitance bridge except that inductors are involved instead of capacitors. The unknown inductance, represented by its (series-equivalent circuit) inductance L_x and R_x, is measured in terms of a precise standard value inductor. L_1 is the standard inductor and R_1 is a variable standard resistor to balance R_x. R_3 and R_4, as in other bridges, are standard resistors. Balance of the bridge is achieved by alternately adjusting R_1 and either R_3 or R_4. At balance, Equation 7-1 once again applies:

$$\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4}$$

$$\frac{R_1 + j\omega L_1}{R_3} = \frac{R_x + j\omega L_x}{R_4},$$

or

$$\boxed{\frac{R_1}{R_3} + j\frac{\omega L_1}{R_3} = \frac{R_x}{R_4} + j\frac{\omega L_x}{R_4}.} \tag{7-17}$$

Equating the real components in Equation 7-17:

$$\frac{R_1}{R_3} = \frac{R_x}{R_4},$$

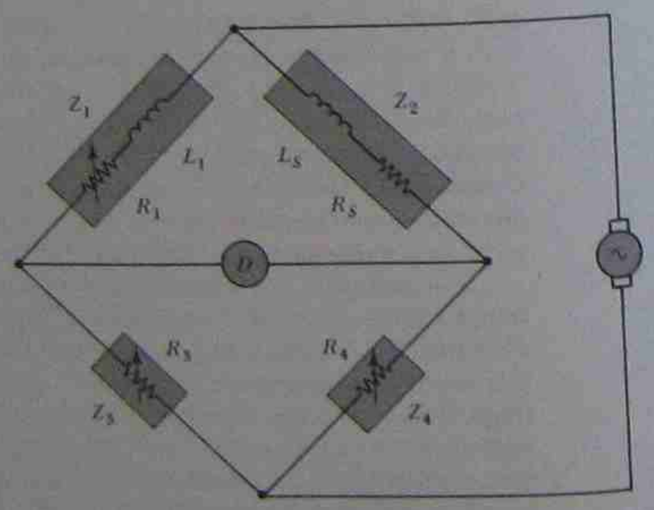


FIGURE 7-10. Inductance comparison bridge for measuring inductance series equivalent circuit components (L_x and R_x) of an unknown inductor.

which gives

$$\boxed{R_x = \frac{R_1 R_4}{R_3}.} \tag{7-18}$$

Equating the imaginary components in Equation 7-17:

$$\frac{\omega L_1}{R_3} = \frac{\omega L_x}{R_4},$$

which gives

$$\boxed{L_x = \frac{L_1 R_4}{R_3}.} \tag{7-19}$$

When the approximate value of an inductance is known, the approximate values of the bridge components at balance can be calculated. The components can then be initially set to the calculated values, and further adjusted for bridge balance. This procedure makes balance easier to achieve, and, of course, it can be applied to all types of bridges.

EXAMPLE 7-5 An inductor with a marked value of 500 mH has a measured resistance of 270 Ω. The inductance is to be measured on an inductance comparison bridge which uses a standard inductance of 100 mH. The bridge also has a standard value of $R_4 = 5$ kΩ. Determine the values of R_1 and R_3 at which balance is likely to occur.

SOLUTION

From Equation 7-19,

$$R_3 = \frac{R_4 L_1}{L_x}$$

$$= \frac{5\ \text{k}\Omega \times 100\ \text{mH}}{500\ \text{mH}}$$

$$= 1\ \text{k}\Omega.$$

From Equation 7-18,

$$R_1 = \frac{R_x R_3}{R_4}$$

$$= \frac{270\ \Omega \times 1\ \text{k}\Omega}{5\ \text{k}\Omega}$$

$$= 54\ \Omega.$$

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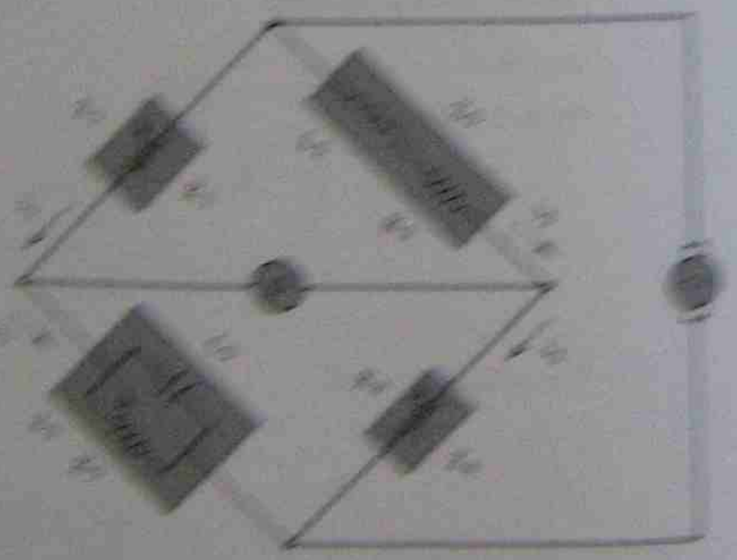

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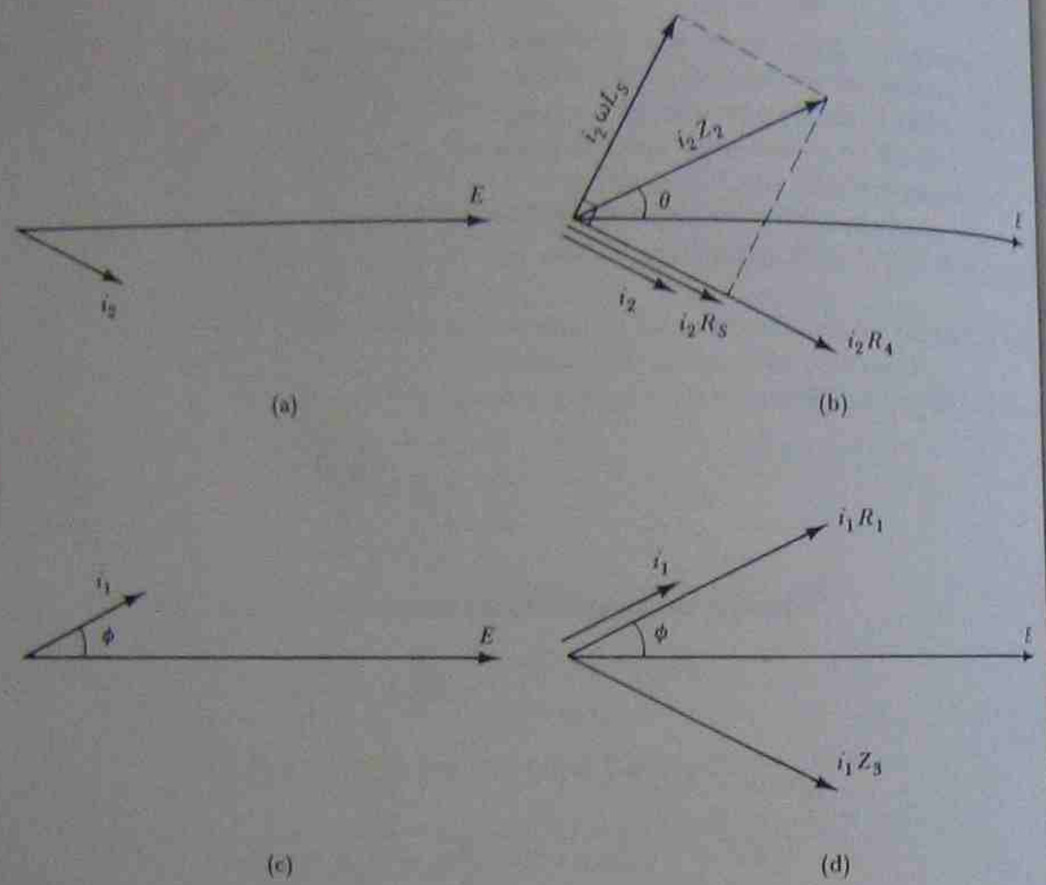

FIGURE 7-12. Phasor diagram for Maxwell bridge.

Phase angles ϕ and θ must also be equal. It can also be stated that $i_1 Z_3$ and $i_2 R_4$ are equal both in magnitude and phase.

EXAMPLE 7-6 A Maxwell inductance bridge using a standard capacitor of $C_3 = 0.1\ \mu F$ operates at a supply frequency of 100 Hz. Balance is achieved when $R_1 = 1.26\ k\Omega$, $R_3 = 470\ \Omega$, and $R_4 = 500\ \Omega$. Calculate the inductance and resistance of the measured inductor, and determine its Q factor.

SOLUTION

Equation 7-22,

$$\begin{aligned} L_s &= C_3 R_1 R_4 \\ &= 0.1\ \mu F \times 1.26\ k\Omega \times 500\ \Omega \\ &= 63\ mH; \end{aligned}$$

Equation 7-21,

$$\begin{aligned} R_s &= \frac{R_1 R_4}{R_3} \\ &= \frac{1.26\ k\Omega \times 500\ \Omega}{470\ \Omega} \\ &= 1.34\ k\Omega; \end{aligned}$$

Equation 7-7,

$$\begin{aligned} Q &= \frac{\omega L_s}{R_s} \\ &= \frac{2\pi \times 100\ Hz \times 63\ mH}{1.34\ k\Omega} \\ &= 0.03. \end{aligned}$$

7-9 THE HAY INDUCTANCE BRIDGE

The *Hay bridge* circuit in Figure 7-13(a) is similar to the Maxwell bridge, except that R_3 and C_3 are connected in series instead of parallel. It is found that this change makes the Hay bridge most suitable for measurement of coils with a high Q factor. However, with R_s and L_s retained as a series circuit, the bridge balance equations turn out to be very awkward. If the unknown inductance is represented as a parallel LR circuit as in Figure 7-13(b), instead of a series circuit, the balance equations are found to be exactly the same as those for the Maxwell bridge. It must be remembered, of course, that the measured L_P and R_P are a parallel equivalent circuit. The equivalent series LR circuit can be determined by substitution into Equations 7-5 and 7-6.

When the bridge in Figure 7-13(b) is balanced, Equation 7-1 once again applies:

$$\frac{Z_1}{Z_3} = \frac{Z_2}{Z_4}$$

$$\frac{1}{Z_2} = \frac{1}{R_P} + \frac{1}{j\omega L_P} = \frac{1}{R_P} - j\frac{1}{\omega L_P},$$

or

$$Z_2 = 1/(1/R_P - j1/\omega L_P),$$

$$Z_3 = R_3 - j\frac{1}{\omega C_3}.$$

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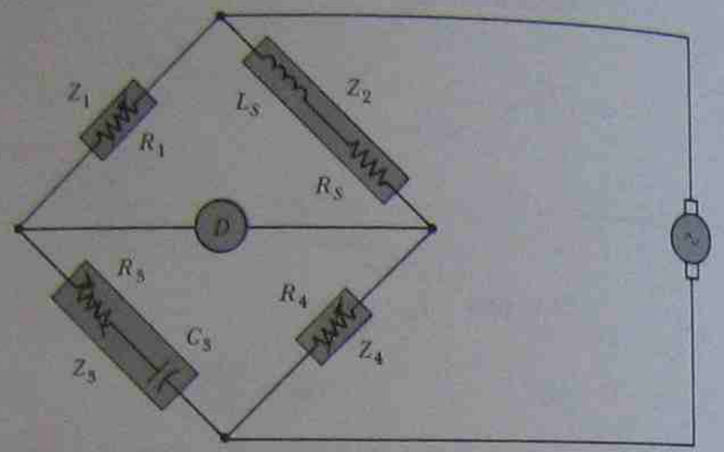
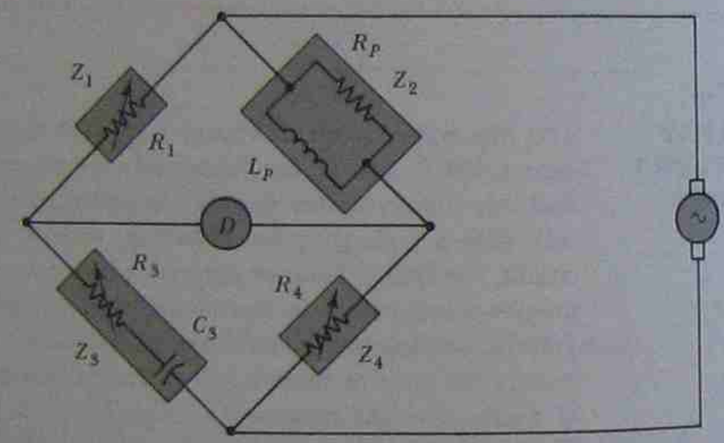


(a) Unknown inductance measured as a series equivalent circuit



(b) Unknown inductance measured as a parallel equivalent circuit

FIGURE 7-13. Two circuit arrangements for the Hay inductance bridge

Substituting into Equation 7-1:

$$\frac{R_1}{R_3 - j1/\omega C_3} = \frac{1/(1/R_P - j1/\omega L_P)}{R_4},$$

$$\frac{R_1}{R_3 - j1/\omega C_3} = \frac{1}{R_4(1/R_P - j1/\omega L_P)},$$

or

$$R_4\left\{1/R_P - j\frac{1}{\omega L_P}\right\} = \frac{R_3 - j1/\omega C_3}{R_1},$$

giving

$$\boxed{\frac{R_4}{R_P} - j\frac{R_4}{\omega L_P} = \frac{R_3}{R_1} - j\frac{1}{\omega C_3 R_1}.} \tag{7-23}$$

Equating the real components in Equation 7-23:

$$\frac{R_4}{R_P} = \frac{R_3}{R_1},$$

or

$$\boxed{R_P = \frac{R_1 R_4}{R_3}.} \tag{7-24}$$

Equating the imaginary components in Equation 7-23:

$$\frac{R_4}{\omega L_P} = \frac{1}{\omega C_3 R_1},$$

giving

$$\boxed{L_P = C_3 R_1 R_4.} \tag{7-25}$$

Equations 7-24 and 7-25 are seen to be similar to Equations 7-21 and 7-22, respectively, except that the quantities now refer to a parallel LR circuit.

EXAMPLE 7-7 A Hay bridge operating at a supply frequency of 100 Hz is balanced when the components are $C_3 = 0.1\ \mu F$, $R_1 = 1.26\ k\Omega$, $R_3 = 75\ \Omega$, and $R_4 = 500\ \Omega$. Calculate the inductance and resistance of the measured inductor. Also determine the Q factor of the coil.

SOLUTION

Equation 7-25,

$$\begin{aligned} L_P &= C_3 R_1 R_4 \\ &= 0.1\ \mu F \times 1.26\ k\Omega \times 500\ \Omega \\ &= 63\ mH \end{aligned}$$

Equation 7-24,

$$\begin{aligned} R_P &= \frac{R_1 R_4}{R_3} \\ &= \frac{1.26\ k\Omega \times 500\ \Omega}{75\ \Omega} \\ &= 8.4\ k\Omega \end{aligned}$$

Equation 7-8,

$$Q = \frac{R_p}{\omega L_p}$$
$$= \frac{8.4\ \text{k}\Omega}{2\pi \times 100\ \text{Hz} \times 63\ \text{mH}}$$
$$= 212.$$

EXAMPLE 7-8 Calculate the series equivalent circuit for the L_p and R_p values determined in Example 7-7. Also determine the component values of R_1 and R_3 required to balance the calculated L_s and R_s values in the Maxwell bridge. Assume that R_4 remains 500 Ω.

SOLUTION

Equation 7-5,

$$R_S = \frac{R_p X_p^2}{X_p^2 + R_p^2}$$

Equation 7-6,

$$X_S = \frac{R_p^2 X_p}{X_p^2 + R_p^2}$$

$R_p = 8.4\ \text{k}\Omega$,

$R_p^2 = 7.056 \times 10^7$,

$X_p = \omega L$

$= 2\pi \times 100\ \text{Hz} \times 63\ \text{mH}$

$= 39.6\ \Omega$,

$X_p^2 = 1.57 \times 10^3$,

$X_p^2 + R_p^2 = 7.056 \times 10^7$,

$$R_S = \frac{8.4\ \text{k}\Omega \times 1.57 \times 10^3}{7.056 \times 10^7}$$
$$= 0.187\ \Omega,$$
$$X_S = \frac{7.056 \times 10^7 \times 39.6}{7.056 \times 10^7}$$
$$= 39.6\ \Omega,$$
$$L_s = \frac{X_s}{\omega} = \frac{39.6\ \Omega}{2\pi \times 100\ \text{Hz}}$$
$$= 63\ \text{mH}$$

From Equation 7-22,

$$R_1 = \frac{L_s}{C_3 R_4}$$
$$= \frac{63\ \text{mH}}{0.1\ \mu\text{F} \times 500\ \Omega}$$
$$= 1.26\ \text{k}\Omega;$$

From Equation 7-21,

$$R_3 = \frac{R_1 R_4}{R_s}$$
$$= \frac{1.26\ \text{k}\Omega \times 500\ \Omega}{0.187\ \Omega}$$
$$= 3.37\ \text{M}\Omega.$$

Example 7-8 demonstrates that the inductor parallel equivalent circuit determined in Example 7-7 actually represents a coil which has an inductance of 63 mH and a coil resistance of 0.187 Ω. The series equivalent circuit more correctly represents the measurable resistance and inductance of a coil. Conversely, the parallel *CR* equivalent circuit represents the measurable dielectric resistance and capacitance of a capacitor more correctly than a series *CR* equivalent circuit.

The (high) calculated value of R_3 in Example 7-8 shows that the low resistance (high Q) coil cannot be conveniently measured on a Maxwell bridge. Thus, the Hay bridge is best for measurement of inductances with high Q. Similarly, it can be demonstrated that the Maxwell bridge is best for measurement of low Q inductances, and that the Hay bridge is not suited to low Q inductance measurements.

Some inductors which have neither very low nor very high Q factors may be easily measured on either type of bridge. In this case it is best to use the Maxwell circuit, because the inductor is then measured directly in terms of its (preferable) series equivalent circuit.

7-10 MULTI-FUNCTION IMPEDANCE BRIDGE

All but one of the capacitance and inductance bridges discussed in the preceding sections can be constructed using a standard capacitor and three adjustable standard resistors. The single exception is the inductance comparison bridge, (Figure 7-10).

Figure 7-14 shows the circuits of five different bridges constructed from the four basic components. These are: a series-resistance capacitance bridge, a parallel-resistance capacitance bridge, a Wheatstone bridge, a

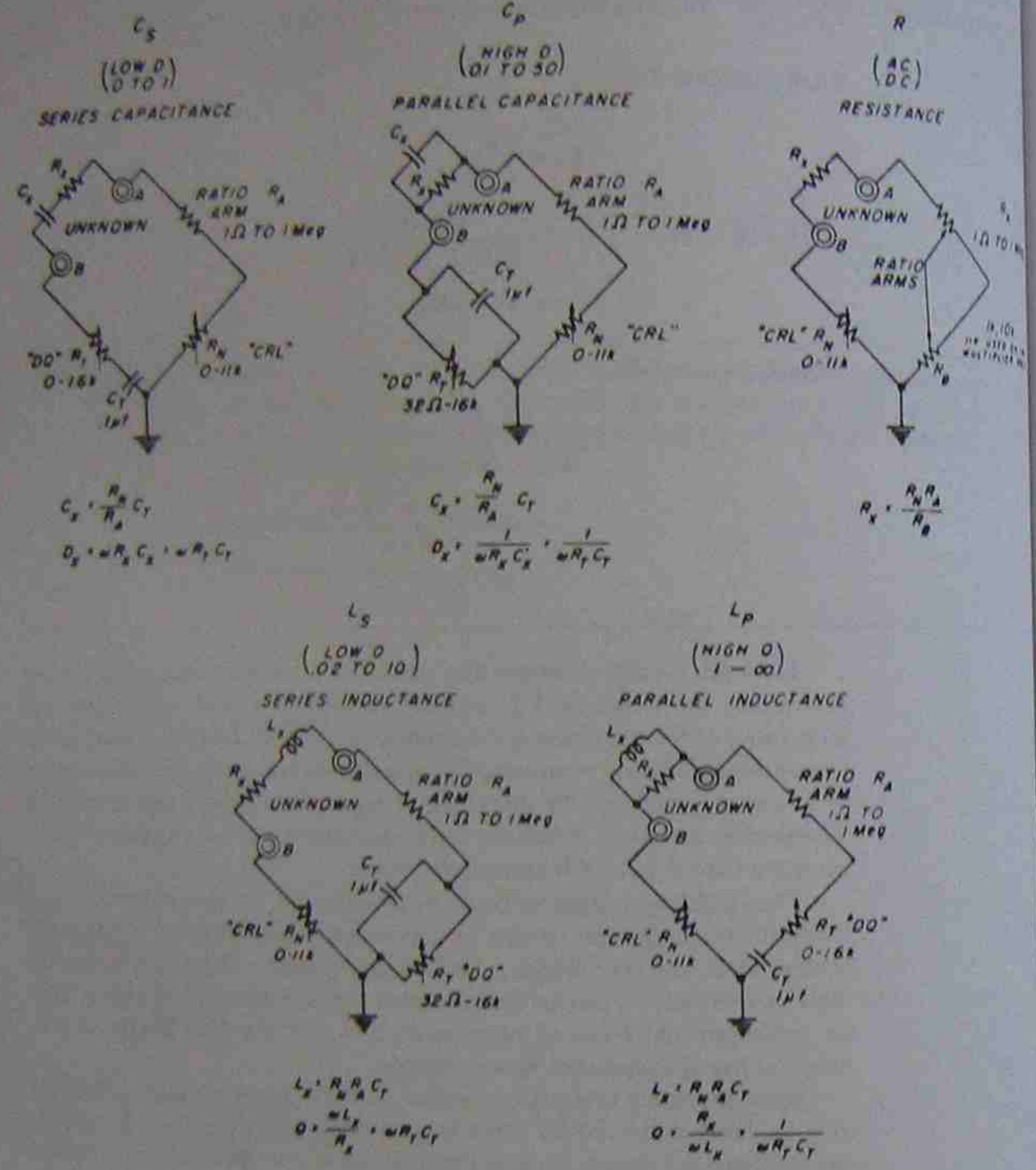


FIGURE 7-14. Bridge circuits used in the GR 1650-A impedance bridge (Courtesy of GenRad, Inc.).

Maxwell bridge, and a Hay bridge. All five circuits are available in the *GenRad (GR) type 1650-A impedance bridge*. This instrument contains the four basic components and appropriate switches to set the components into any one of the five configurations. A null detector and internal ac and dc supplies are also included, and terminals are provided for: the unknown impedance, an external null detector, and an external signal generator.

The GR 1650-A impedance bridge measures inductance ranging from 10μH to 1100 H, capacitance from 10 pF to 1100 μF, and resistance from 0.01 Ω to 11 MΩ. The accuracy on all measurements is typically $\pm 1\%$ with an additional error of ± 1 μH, ± 1 pF, or ± 0.001 Ω. Dissipation factor is measured over a range of 0.005 to 50, with an accuracy of $\pm 5\%$. There is an additional ± 0.001 error in D measurements, which is obviously most important for low D values. The range of Q factor measurement is from 0.02 to 1000, and the accuracy is specified as a percentage of $1/Q$. The $1/Q$ error is $\pm 5\%$, with an additional ± 0.001 error, which is most important at high Q values.

The front panel of the GR 1650-A impedance bridge is shown in Figure 7-15. At the top left-hand side are two terminals for connection of

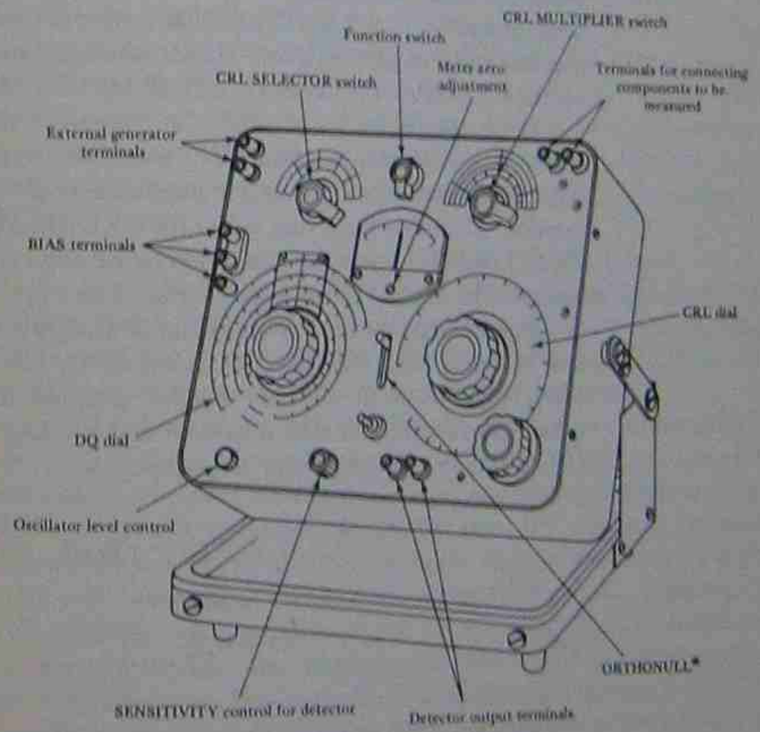


FIGURE 7-15. Front panel of the GR 1650-A impedance bridge (Courtesy of GenRad, Inc.).

an external ac or dc supply when the internal supplies are unavailable. These are identified as EXT GEN AC-DC. The CRL SELECTOR (alongside the EXT GEN terminals) selects the bridge configuration according to the quantity to be measured: C_s (capacitance in its series [illegible] equivalent circuit form), (LOW D); C_p (capacitance in its parallel [illegible] equivalent circuit form), (HIGH D); R (resistance using an ac or dc supply); L_s (inductance in its series LR equivalent circuit form), (LOW Q); L_p (inductance in its parallel equivalent circuit form), (HIGH Q). [illegible] already noted, the circuits for each of these configurations are illustrated in Figure 7-14. Each circuit (in Figure 7-14) is also identified according to the CRL setting.

The function switch at the top center of the front panel is the supply selector, with positions: AC EXT (external ac supply); INT 1kHz (internal 1 kHz ac supply); OFF; INT 6 V DC (internal 6-V dc supply); DC EXT (external dc supply).

To the right of the supply selector is the CRL MULTIPLIER. The setting of this switch gives the factor by which the CRL dial (immediately below) must be multiplied. The units involved are also indicated on the CRL MULTIPLIER switch positions. For example, for measuring capacitance the CRL MULTIPLIER positions are: pF × 100; nF × (1, 10, or 100); and μF × (1, 10, or 100). Similar ranges are indicated for inductance measurements in μH, mH, and H. For resistance measurement, the ranges on the CRL MULTIPLIER are mΩ, Ω, kΩ, and MΩ.

When the bridge is balanced, the position of the CRL dial gives the measured capacitance, resistance, or inductance. As noted, the dial position must be multiplied by the factor indicated at the CRL MULTIPLIER position. The other large dial below the CRL SELECTOR is identified as the DQ dial. This gives the dissipation factor D for a capacitance measurement, or the quality factor Q for an inductance measurement.

Suppose that a capacitor is measured using the internal 1-kHz source and that the CRL SELECTOR is set to C_p HIGH D, and the CRL MULTIPLIER is at 100 μF. Further suppose that bridge balance is achieved when the CR dial is at 0.88 and the DQ dial is at 0.39 on the HIGH D scale. The capacitor is measured as

$$C_p = 0.88 \times 100\ \mu F$$
$$= 88\ \mu F$$

and

$$D = 0.39.$$

With the CRL SELECTOR at C_p, the capacitor has been measured in terms of its parallel circuit. Equation 7-9 may now be applied to calculate

the resistive component of the parallel equivalent circuit:

$$D = \frac{1}{\omega C_p R_p}$$

or

$$R_p = \frac{1}{\omega C_p D}$$

$$= \frac{1}{2\pi \times 1\ kHz \times 88\ \mu F \times 0.39}$$

$$= 4.6\ \Omega.$$

The null detector (approximately at the center of the panel) is a center-zero instrument with a (slot-headed) mechanical zero control. The SENSITIVITY control (left of center at the bottom of the panel) adjusts the sensitivity of the null detector. The null detector functions as a center-zero instrument only when measuring resistance and using a dc supply. When using an ac supply, the null detector deflects to the right when the bridge is off balance. By means of the DETECTOR toggle switch (center of panel near the bottom), the detector can be set for the internal 1 kHz source (1 kc) or for an external source (FLAT).

At the bottom left-hand side of the panel is the level control for the (internal) signal generator, identified as OAC LEVEL. Slightly to the right of center at the bottom of the panel, the DET OUTPUT terminals facilitate the connection of an additional detector, such as headphones or an oscilloscope. This can be useful, for example, when the bridge is supplied from an external signal generator with a frequency other than 1 kHz.

When an external frequency other than 1 kHz is used, the D or Q factor determined from the DQ dial must be multiplied by a factor M. The appropriate factor is marked at the end of each scale on the DQ dial. For low D and low Q, $M = f/1$ kHz. For high D and high Q, $M = 1$ kHz/f, where f is the frequency of the external signal generator.

The inductance of an iron-cored coil can be significantly affected by the level of direct current flowing through the coil. This is because the iron core has a nonlinear B/H characteristic, and inductance is proportional to the slope of the characteristic. In this case, the measured inductance is termed the incremental inductance. Similarly, many capacitors have to operate with a dc bias voltage continuously across the terminals. Depending upon the dielectric material, the actual capacitance may be altered by the presence of the bias. (For example, the capacitance of a semiconductor pn junction varies according to the level of reverse bias voltage.)

Two terminals, identified as BIAS, are located on the left side of the panel below the EXT GEN terminals. These are used when a capacitor is

to be measured while a dc bias voltage is applied to its terminals, or when an inductor is to be measured with a certain level of direct current through its coil. In the case of capacitance measurements, bias can be applied only when the CRL SELECTOR switch is at C_x. For inductance measurements, the CRL SELECTOR must be at the L_p position for bias application. Special methods involving internal bridge terminals must be employed for C_p or L_s measurements involving bias.

When measuring inductors with a low Q factor or capacitors with a high D factor, balance is sometimes very difficult to obtain. This is because the DQ and CRL dial adjustments are interdependent. Each adjustment of the CRL dial for null (after the DQ dial has been adjusted) affects the null setting of the DQ dial, thus requiring further adjustment of the DQ dial. This is the result of the measured capacitance or inductance changing slightly when the current flowing through it is altered by adjustment of a series- or parallel-connected resistor. The effect is known as a *sliding null*.

To overcome the sliding null problem, the GR 1650-A has an ORTHONULL (center of the panel), a mechanical clutch that may be engaged between the CRL and DQ dials by setting the lever to ORTHONULL. When not required, the lever is set to NORMAL. Using the ORTHONULL mechanism, the first null is obtained by adjusting the DQ dial. The CRL dial is then adjusted to obtain an improved null, and the DQ dial follows the CRL dial movements. This procedure is repeated until the best null is obtained. The ORTHONULL makes bridge balance more rapidly obtainable.

EXAMPLE 7-9 An unknown inductor is measured on a GR 1650-A impedance bridge, using the internal 1-kHz ac source. Null is obtained when the CRL dial indicates 1.8 and the DQ dial reading is 7.52 on the HIGH Q scale. The CRL SELECTOR is at L_p, and the CRL MULTIPLIER is at 10 mH. Determine the measured inductance and resistance of the inductor in terms of its series equivalent circuit.

SOLUTION

$$\begin{aligned} L_p &= (\text{CRL dial reading}) \times (\text{CRL MULTIPLIER setting}) \\ &= 1.8 \times 10 \text{ mH} \\ &= 18 \text{ mH} \\ Q &= 7.52. \end{aligned}$$

From Equation 7-8,

$$\begin{aligned} R_p &= \omega L_p Q \\ &= 2\pi \times 1 \text{ kHz} \times 18 \text{ mH} \times 7.52 \\ &= 850.5\ \Omega. \end{aligned}$$

Equation 7-5,

$$\begin{aligned} R_s &= \frac{R_p X_p^2}{X_p^2 + R_p^2}; \\ R_p^2 &= 7.23 \times 10^5, \\ X_p &= 2\pi \times 1 \text{ kHz} \times 18 \text{ mH} \\ &= 113.1, \\ X_p^2 &= 1.279 \times 10^4, \\ R_s &= \frac{850.5\ \Omega \times 1.279 \times 10^4}{1.279 \times 10^4 + 7.23 \times 10^5} \\ &= 14.8\ \Omega. \end{aligned}$$

Equation 7-6,

$$\begin{aligned} X_s &= \frac{R_p^2 X_p}{X_p^2 + R_p^2} \\ &= \frac{7.23 \times 10^5 \times 113.1}{1.279 \times 10^4 + 7.23 \times 10^5} \\ &= 111\ \Omega, \end{aligned}$$

and

$$\begin{aligned} L_s &= \frac{X_s}{\omega} = \frac{111\ \Omega}{2\pi \times 1 \text{ kHz}} \\ &= 17.7 \text{ mH}. \end{aligned}$$

EXAMPLE 7-10 A capacitance is measured on a GR 1650-A impedance bridge using a 100-Hz external supply. At null, the CRL dial is at 3.65, and the DQ reading is 0.21 on the low D scale. The CRL SELECTOR is at C_x, and the CRL MULTIPLIER at 100 pF. Determine the measured capacitance and dielectric resistance in terms of the parallel CR equivalent circuit.

SOLUTION

$$\begin{aligned} C_x &= (\text{CRL dial reading}) \times (\text{CRL MULTIPLIER setting}) \\ &= 3.65 \times 100 \text{ pF} \\ &= 365 \text{ pF}, \\ D &= M \times (DQ \text{ reading}) \\ &= \frac{100 \text{ Hz}}{1 \text{ kHz}} \times 0.21 \\ &= 0.021. \end{aligned}$$

From Equation 7-10,

$$R_1 = \frac{D}{\omega C_1}$$

$$= \frac{0.021}{2\pi \times 100\ \text{Hz} \times 365\ \text{pF}}$$

$$= 91.6\ \text{k}\Omega.$$

Equation 7-3,

$$R_x = \frac{R_2^2 + X_2^2}{R_1};$$

$$R_2^2 = 8.39 \times 10^9,$$

$$X_2 = \frac{1}{2\pi \times 100\ \text{Hz} \times 365\ \text{pF}}$$

$$= 4.36 \times 10^6,$$

$$X_2^2 = 1.9 \times 10^{13},$$

$$R_x = \frac{8.39 \times 10^9 + 1.9 \times 10^{13}}{91.6 \times 10^3}$$

$$= 207.6\ \text{M}\Omega.$$

Equation 7-4,

$$X_x = \frac{R_2^2 + X_2^2}{X_1}$$

$$= \frac{8.39 \times 10^9 + 1.9 \times 10^{13}}{4.36 \times 10^6}$$

$$= 4.36 \times 10^6$$

$$X_x = X_1$$

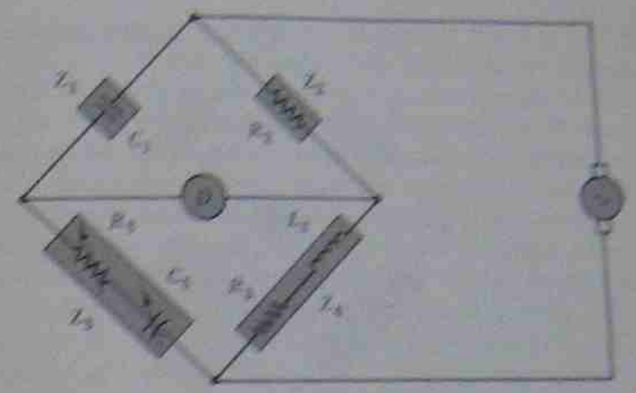
and

$$C_x = C_1 = 365\ \text{pF}$$

7-11 OWEN, SCHERING, AND WIEN BRIDGES

7-11.1 Owen Bridge

Figure 7-16 shows the circuit and balance equations for an *Owen bridge*. This is a bridge for measuring inductance (L_x and R_x) once again in terms of a standard capacitor C_1 and resistance R_2. However, an adjustable calibrated capacitor (decade capacitance box) is also required, and this is the main disadvantage of the bridge. Because the adjustable components R_1 and C_2 do not affect the current flowing in the component to be measured, *sliding nulls* are avoided, and balance is easily achieved.



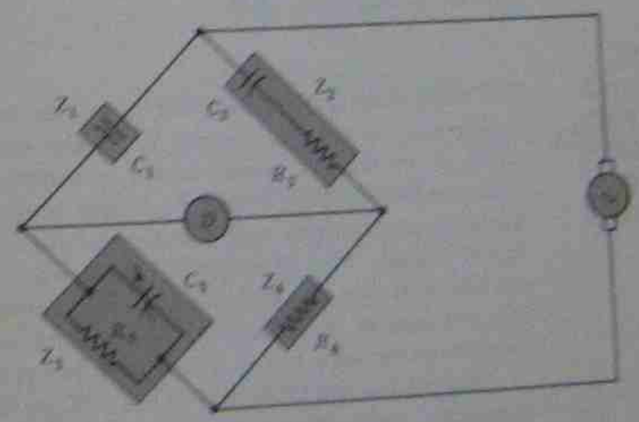
$$L_x = C_1 R_2 R_3$$

$$R_x = \frac{C_1 R_2}{C_2}$$

FIGURE 7-16. Owen bridge circuit used for inductance measurements.

7-11.2 Schering Bridge

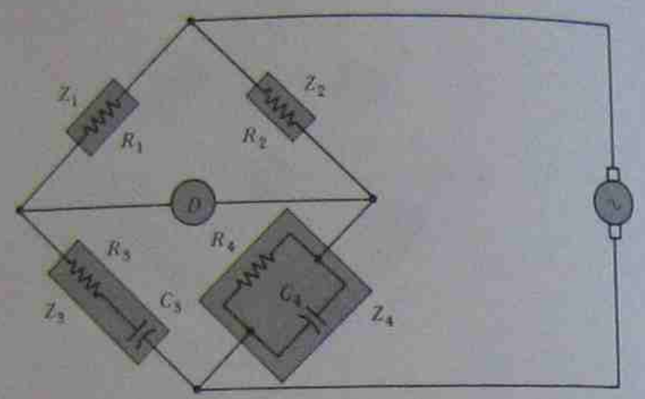
The *Schering bridge* shown in Figure 7-17 is another circuit that uses an adjustable capacitor (C_2). Its most important application is measurement of very small capacitances and high-voltage capacitance measurements.



$$C_x = \frac{C_1 R_2}{R_4}$$

$$R_3 = \frac{C_2 R_4}{C_1}$$

FIGURE 7-17. Schering bridge circuit used for capacitance measurements.



$$f = \frac{1}{2\pi\sqrt{R_3 R_4 C_3 C_4}}$$

FIGURE 7-18. Wien frequency bridge.

7-11-3 Wien Bridge

When the balance equations for the *Wien bridge* (Figure 7-18) are derived, it is found that the supply frequency is involved. Thus, bridge balance is frequency dependent. The balance equations can be rewritten to give an expression for frequency (see Figure 7-18) in terms of the bridge components. This bridge circuit is also employed in an oscillator known as the *Wien bridge* oscillator, which produces an output at the bridge balance frequency (see Section 15-1).

7-12 AC BRIDGE SENSITIVITY, ACCURACY, AND RESIDUALS

The same considerations that determined the sensitivity of a Wheatstone bridge apply to ac bridge circuits. The bridge sensitivity may be defined in terms of the smallest change in the measured quantity that causes the galvanometer to deflect from zero. Bridge sensitivity can be improved by using a more sensitive null detector and/or by increasing the level of supply voltage. The bridge sensitivity is analyzed by exactly the same method used for the Wheatstone bridge, except that impedances are involved instead of resistances. Accuracy of measurements is also determined in the same way as Wheatstone bridge accuracy.

When measuring very small values of C, L, or R, the *stray* capacitance, inductance, and resistance of connecting leads can introduce considerable errors. This is minimized by connecting the unknown component directly to the bridge terminal or by means of very short connecting leads. Even when such precautions are observed, there are still small internal values of L, C, and R in all ac bridges. These are termed *residuals*, and instrument manufacturers normally list the residuals on the bridge specification. The

GR 1650-A impedance bridge has residuals of $R = 1 \times 10^{-3}\ \Omega$, $C = 0.5$ pF, and $L = 0.2\ \mu$H. Obviously, these quantities can introduce serious errors if they are a substantial percentage of any measured quantity.

The errors introduced by strays and residuals can be eliminated by a *substitution technique*. In the case of a capacitance measurement, the bridge is first balanced with a larger capacitor connected in place of the small capacitor to be measured. The small capacitor is then connected in parallel with the larger capacitor, and the bridge is readjusted for balance. The first measurement is the large capacitance C_1 plus the stray and residual capacitance C_r. So the measured capacitance is $C_1 + C_r$. When the small capacitor C_x is connected, the measured capacitance is $C_1 + C_r + C_x$. C_x is found by subtracting the first measurement from the second.

A similar approach is used for measurements of low value inductance and resistance, except that in this case the low value component must be connected in series with the larger L or R quantity. The substitution technique can also be applied to other (nonbridge) measurement methods.

EXAMPLE 7-11 On the bridge in Example 7-3 a new balance is obtained when a small capacitor (C_x) is connected in parallel with the measured capacitor C_p. The new component values for balance are $R_1 = 376\ \Omega$, $R_3 = 10\ \text{k}\Omega$, and $R_4 = 14.66\ \text{k}\Omega$. Determine the value of C_x and its parallel resistive component R_x.

SOLUTION

$$C_x \| C_p = C_x + C_p = \frac{C_1 R_3}{R_4}$$

$$= \frac{0.1\ \mu\text{F} \times 10\ \text{k}\Omega}{14.66\ \text{k}\Omega} = 0.682\ \mu\text{F},$$

$$C_x = 0.0682\ \mu\text{F} - C_p, = 0.0682\ \mu\text{F} - 0.068\ \mu\text{F}$$

$$= 0.0002\ \mu\text{F} = 200\ \text{pF},$$

and

$$R_x \| R_p = \frac{R_1 R_4}{R_3} = \frac{376\ \Omega \times 14.66\ \text{k}\Omega}{10\ \text{k}\Omega}$$

$$= 551.2\ \Omega,$$

$$\frac{1}{R_x} + \frac{1}{R_p} = \frac{1}{551.2\ \Omega},$$

$$\frac{1}{R_x} = \frac{1}{551.2\ \Omega} - \frac{1}{R_p},$$

$$R_x = 1 \Big/ \left\{ \frac{1}{551.2\ \Omega} - \frac{1}{551.3\ \Omega} \right\}$$

$$= 3.04\ \text{M}\Omega.$$

REVIEW QUESTIONS AND PROBLEMS

7-1. Sketch a general ac bridge circuit, derive the balance equation, and discuss the adjustments required to achieve balance.

7-2. List and compare the various types of null detectors that may be used with an ac bridge.

7-3. Sketch the circuit of a simple capacitance bridge. Derive the balance equation for this bridge and discuss its limitations. Sketch an approximate phasor diagram showing the phase relationships between currents and voltages.

7-4. A simple capacitance bridge uses a standard capacitor $C = 0.1\ \mu F$ and two standard resistors that are each adjustable from 1 kΩ to 100 kΩ. Calculate the minimum and maximum values of unknown capacitance that can be measured on the bridge.

7-5. Discuss the series and parallel equivalent circuits for a capacitor. Which of the two circuits should be used in an ac bridge for: (a) a capacitor with a high-resistance dielectric, (b) a capacitor with a low-resistance dielectric. Briefly explain.

7-6. Derive the equations for converting a CR series circuit into its equivalent parallel circuit.

7-7. Which of the two CR equivalent circuits best represents a capacitor? Explain. Define *capacitor dissipation factor*, and write the equation for dissipation factor.

7-8. Discuss the series and parallel equivalent circuits for an inductor. Which of the two is used in an ac bridge for: (a) an inductor with a high-resistance coil, (b) an inductor with a low-resistance coil. Briefly explain.

7-9. Derive the equations for converting an LR parallel circuit into its equivalent series circuit.

7-10. Which of the two LR equivalent circuits best represents an inductor? Explain. Define the quality factor of an inductor, and write the equation for Q factor.

7-11. Sketch the circuit of a series-resistance capacitance bridge. Derive the balance equations for the unknown capacitance and its resistive component.

7-12. Sketch an approximate phasor diagram for the series-resistance capacitance bridge. Briefly explain.

7-13. A series-resistance capacitance bridge, as shown in Figure 7-8(a), uses a 0.1-μF capacitor for C_1. The supply frequency is 1 kHz, and at balance the components are: $R_1 = 100.5\ \Omega$, $R_3 = 1\ k\Omega$, and $R_4 = 2.1\ k\Omega$. Calculate the resistive and capacitive components of the measured capacitor. Also, determine the capacitor dissipation factor.

7-14. Sketch the circuit of a parallel-resistance capacitance bridge. Derive the equations for the resistive and capacitive components of the measured capacitor. Explain the different applications of the parallel-resistance and series-resistance capacitance bridges.

7-15. A parallel-resistance capacitance bridge, as shown in Figure 7-9, uses a 0.1-μF capacitor for C_1, and the supply frequency is 1 kHz. The bridge components at balance are: $R_1 = 547\ \Omega$, $R_3 = 1\ k\Omega$, and $R_4 = 606\ \Omega$. Calculate the resistive and capacitive components of the measured capacitor, and determine the dissipation factor of the capacitor.

7-16. Calculate the parallel equivalent circuit components for the measured capacitor in Question 7-13. Also, determine the component values of R_1 and R_3 required to balance C_x and R_x when the bridge is operated as a parallel-resistance capacitance bridge. Assume that R_4 remains 1 kΩ.

7-17. Sketch the circuit of an inductance comparison bridge. Derive the equations for the resistive and inductive components of the measured inductor.

7-18. An inductance comparison bridge, as shown in Figure 7-10, uses a standard 100-μH inductor for L_1, and a standard 10-kΩ resistor for R_4. When measuring an unknown inductance, null is detected with $R_3 = 37.1\ \Omega$ and $R_2 = 27.93\ k\Omega$. The supply frequency is 1 MHz. Calculate the measured inductance and its resistive component. Also, determine the Q factor of the inductor.

7-19. Sketch the circuit of a Maxwell bridge. Derive the equations for the resistive and inductive components of the measured inductor.

7-20. Sketch an approximate phasor diagram for a Maxwell bridge, and briefly explain. Why is the Maxwell bridge preferable to the inductance comparison bridge?

7-21. An inductor with a marked value of 100 mH and a Q of 21 at 1 kHz is to be measured on a Maxwell bridge. The bridge uses a standard 0.1-μF capacitor and a 1-kΩ resistor for R_1. Calculate the values of R_2 and R_x at which balance is likely to be achieved.

7-22. A Maxwell bridge with a standard capacitor of 0.1 μF operates with a 10-kHz supply frequency. $R_1 = 100\ \Omega$ and R_2 and R_3 can each be adjusted from 100 Ω to 1 kΩ. Calculate the range of inductances and Q factors that can be measured on this bridge.

7-23. Sketch two possible circuits for the Hay bridge. Explain why one circuit is preferable, and derive the equations for the unknown inductance at balance. Explain how the Hay bridge differs from the Maxwell bridge, and discuss the applications of each.

7-24. A Hay bridge, as in Figure 7-13(b), with a supply frequency of 500 Hz has: $C_3 = 0.5\ \mu F$ and $R_4 = 900\ \Omega$. Balance occurs when $R_1 = 466\ \Omega$ and $R_2 = 46.1\ \Omega$. Calculate the inductance, resistance, and Q factor of the measured inductor.

7-25. Calculate the series equivalent circuit components L_s and R_s for the L_p and R_p quantities determined in Problem 7-24. Also calculate the resistances of R_1 and R_2 required to balance the L_s and R_s quantities when connected in a Maxwell bridge. Assume that R_3 remains 900 Ω and $C_3 = 0.5\ \mu F$.

7-26. An inductor is measured on a GR 1650-A impedance bridge using the internal 1-kHz source. Null is obtained with: the CRL SELECTOR at L_p, the CRL MULTIPLIER at 10 mH, the CRL dial at 21, and the DQ dial at 13.5 HIGH Q. Determine the series equivalent circuit inductance and resistance of the measured inductor.

7-27. A GR 1650-A impedance bridge using the internal 1-kHz source gives null with the following control positions: the CRL SELECTOR at L_s, the CRL MULTIPLIER AT 100 mH, the CRL dial at 1.85, and the DQ dial at 0.15 LOW Q. Determine the L_s and R_s quantities for the measured inductor.

7-28. A capacitor is measured on a GR 1650-A impedance bridge using the internal 1-kHz source. Null is obtained with: the CRL SELECTOR at C_p, the CRL MULTIPLIER at 1 μF, the CRL dial at 2.15, and the DQ dial at 7 HIGH D. Determine the C_p and R_p quantities for the measured capacitor.

7-29. If the bridge in Question 7-28 gave balance at the control positions listed when the supply is an external 10-kHz source, calculate C_p and R_p.

7-30. Sketch the circuits of Owen, Schering, and Wien bridges. Comment briefly on each.

7-31. Define residuals in ac bridges. Briefly discuss the sensitivity and accuracy of ac bridges.

7-32. The bridge in Example 7-10 (in the text) gives a new balance when a small capacitor is connected in parallel with the measured capacitor. The new balance positions of the controls are: the CRL dial at 3.69, and the DQ dial at 0.215. Determine the C_p and R_p components of the small capacitor.

8

ANALOG ELECTRONIC INSTRUMENTS

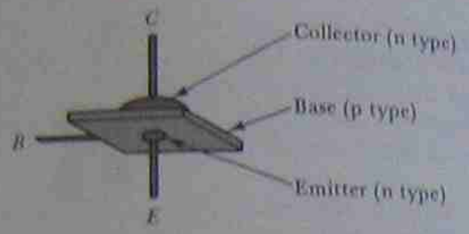
INTRODUCTION

Voltmeters constructed of moving-coil instruments and multiplier resistors (see Chapter 2) have some important limitations. The resistance of such instruments is too low for measurements in high impedance circuitry. Also, the instruments cannot measure very low voltage levels. These limitations can be overcome by the use of electronic devices which offer high input resistance, and which can amplify low voltages to measurable levels. When such devices are employed, the instrument becomes an *electronic voltmeter*, or an *electronic multimeter*. Other designations sometimes used are *VTVM* for *vacuum tube voltmeter* and *TVM* for *transistor voltmeter*.

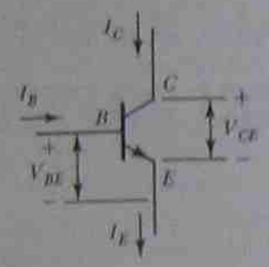
Electronic multimeters can be *analog instruments* in which the measured quantity is indicated by a pointer moving over a calibrated scale. They can also be *digital instruments* which display the measured quantity in numerical form. This chapter covers analog electronic instruments. Digital instruments are treated in Chapters 9 and 10.

8-1 TRANSISTOR OPERATION

A *transistor* is a three-terminal device which can amplify small voltages to higher levels and convert low meter resistances into high resistances. This device is sometimes referred to as a *bipolar junction transistor (BJT)* to distinguish it from the *field effect transistor (FET)* (Section 8-2). The basic construction, graphic symbol, and typical appearance of a low current *npn* transistor is illustrated in Figure 8-1.



(a) npn transistor construction



(b) Graphic symbol for npn transistor

(c) Plastic and metal can enclosed transistors

FIGURE 8-1. npn transistor construction, graphic symbol, and appearance.

An *npn* transistor is a sandwich of *p*-type semiconductor material between two pieces of *n* type (Figure 8-1(a)). *n*-type material has free electrons which can be moved around under the influence of applied voltages to create current flow. *p*-type material has an excess of *holes*, or atomic locations, which can absorb an electron. In *p*-type material current flow consists of electrons moving about from hole to hole.

The three regions and three terminals of a transistor are identified as *emitter* (E), *base* (B), and *collector* (C), as illustrated. Because almost all of the transistor power dissipation occurs at the collector-base junction, the collector-base junction area has to be much larger than that of the emitter-base junction. The three currents are *emitter current* (I_E), *base current* (I_B), and *collector current* (I_C).

The graphic symbol for the transistor has an arrowhead which points from the *p*-type base to the *n*-type emitter [see Figure 8-1(b)]. This

arrowhead also points in the (conventional) direction of current flow across the base-emitter junction when the transistor is operating correctly. Typically, the base-emitter voltage (V_{BE}) is 0.7 V for a silicon transistor, 0.3 V for a germanium device.

The collector of an *npn* transistor must normally always be positive with respect to the emitter. The typical range of collector-emitter voltage (V_{CE}) is 3 to 15 V. The collector current is usually 50 to 200 times the base current.

$$I_C = h_{FE} I_B \tag{8-1}$$

where h_{FE}, known as the *common emitter current gain factor*, typically ranges from 50 to 200. The base is normally the transistor input terminal, so the low level base current controls the much larger collector current.

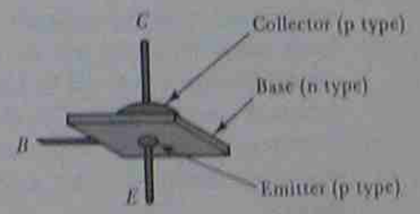
Both I_C and I_B flow into the transistor [see Figure 8-1(b)], and emitter current I_E flows out. Therefore,

$$I_E = I_C + I_B, \tag{8-2}$$

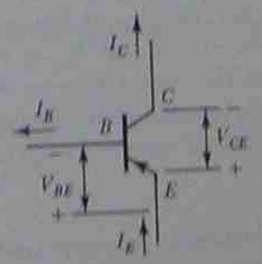
or

$$I_E \approx I_C. \tag{8-3}$$

For the type of low power transistors employed in electronic voltmeters, I_C and I_E could be anywhere between 100 μA and 10 mA. I_B typically ranges from 5 μA to 100 μA.



(a) pnp transistor construction



(b) Graphic symbol for pnp transistor

FIGURE 8-2. pnp transistor construction and graphic symbol.

In Figure 8-2 the construction and graphic symbol of a *pnp* transistor are illustrated. From the practical point of view, a *pnp* transistor operates in exactly the same way as an *npn* device, except all current directions and voltage polarities are reversed [see Figure 8-2(b)].

8-2 FIELD EFFECT TRANSISTORS

The basic construction of an *n*-channel FET is illustrated in Figure 8-3(a). A piece of *n*-type material named the *channel* is sandwiched between two smaller pieces of *p*-type material. Terminals identified as *drain (D)* and *source (S)* are connected at each end of the channel. The two pieces of *p* type are electrically connected together and referred to as the *gate (G)*. The graphic symbol for the *n*-channel FET [Figure 8-3(b)] uses a bar to represent the channel, with drain and source terminals at its ends. The gate terminal has an arrowhead which (as always) points from *p*-type material to *n* type.

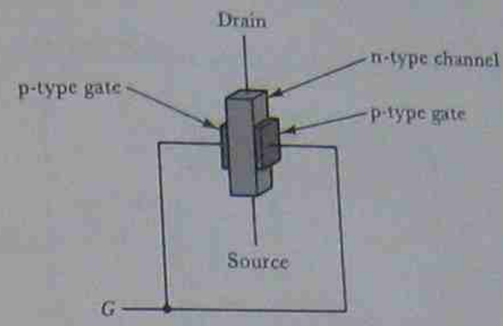
When the FET gate is left unconnected, and the drain is made positive with respect to the source, a drain current (I_D) flows (in the conventional direction) from drain to source. This same current flows out of the source terminal, and at this point it is referred to as the source current (I_S). If the gate terminal is biased negatively with respect to the source, the drain current is progressively reduced as the (negative) gate-source voltage is increased. The gate is normally the input terminal, so the gate-source voltage (V_{GS}) controls the flow of drain current (I_D) and source current (I_S). Note that the gate-channel junction is reverse biased.

For the kind of low current FET used in electronic voltmeters, the drain-source voltage is typically 5 to 25 V. The drain and source current levels range from 100 μA to 10 mA, while the gate-source voltage is usually between 0 and −8 V. Under normal operating conditions, the gate current is around 50 ηA. This means that the FET has a very large input resistance, much larger than that of a bipolar transistor. Another kind of field effect transistor, called a MOSFET, has an even larger input resistance.

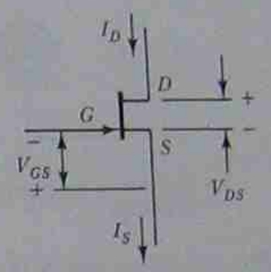
Like *npn* and *pnp* bipolar transistors, there are *p*-channel and *n*-channel FET's. Figure 8-3(c) shows the graphic symbol for the *p*-channel FET. Note the direction of the gate arrowhead on the graphic symbol. The polarity of V_{DS} and V_{GS} is reversed by comparison with the *n*-channel device. This means that the channel current flow is from source to drain. Also the gate is biased positively with respect to the source, so I_D and I_S are progressively reduced as V_{GS} is made more positive.

8-3 TRANSISTOR EMITTER FOLLOWER VOLTMETER

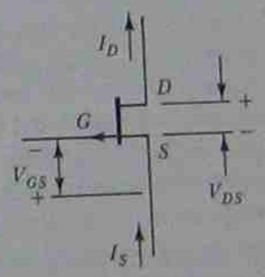
The problem of voltmeter loading (see Section 2-2) can be greatly reduced by using an *emitter follower*. An emitter follower circuit increases the resistance of a voltmeter but does not provide any amplification of the voltage to be measured. The circuit also provides a low output resistance to



(a) Basic construction of n-channel FET

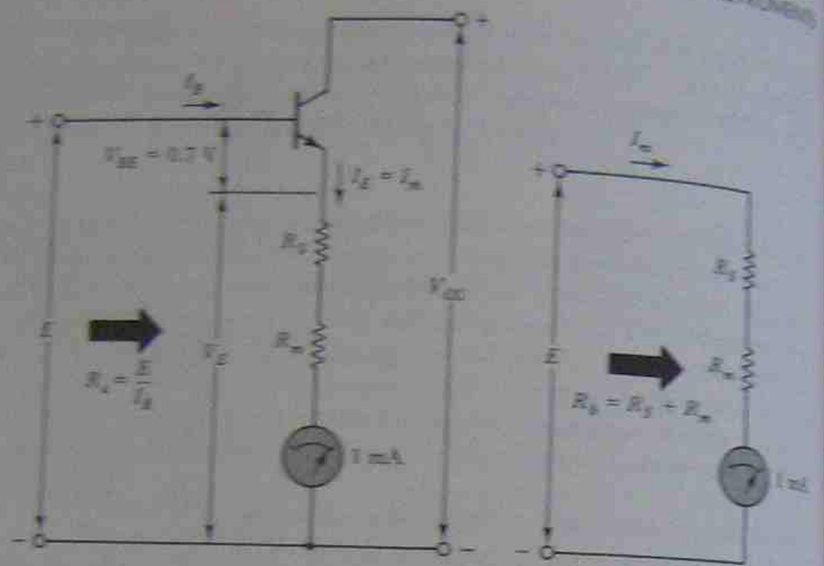


(b) Graphic symbol for n-channel FET



(c) Graphic symbol for p-channel FET

FIGURE 8-3. Basic construction and graphic symbols for field effect transistors.



(a) Basic emitter follower voltmeter

(b) Nonelectronic voltmeter

FIGURE 8-4. Comparison of basic emitter follower voltmeter circuit and simple nonelectronic voltmeter.

8-3-1 Basic Emitter Follower Voltmeter

drive current through the coil of a deflection instrument. Because of its high input resistance and low output resistance, the emitter follower is sometimes called a *buffer amplifier*.

A basic emitter follower voltmeter is illustrated in Figure 8-4(a). A moving-coil instrument and its series multiplier resistance R_S are connected in series with the transistor emitter terminal. Dc supply voltage V_{CC} is connected as illustrated, with its positive terminal to the transistor collector and negative to the deflection meter. Voltage E (to be measured) is applied positive to the transistor base and negative to the same terminal as the power supply negative.

For this particular circuit [Figure 8-4(a)], assume that $V_{CC} = 20$ V, $R_S + R_m = 9.3$ kΩ, and $I_m = 1$ mA at full scale. Also assume that $E = 10$ V. The base-emitter junction of the transistor has a voltage drop of 0.7 V (for a silicon transistor) in the direction of the arrowhead on the symbol. Thus, the transistor emitter terminal is 0.7 V below the voltage at the base.

$$\boxed{V_E = E - V_{BE}} \tag{8-1}$$

$$V_E = 10\text{ V} - 0.7\text{ V}$$
$$= 9.3\text{ V}.$$

The meter current (I_m) is the transistor emitter current (I_E), and

$$I_E = \frac{V_E}{R_S + R_m} = \frac{9.3\text{ V}}{9.3\text{ k}\Omega} = 1\text{ mA}.$$

From Equations 8-1 and 8-3:

$$I_B = \frac{I_E}{h_{FE}}.$$

Assuming that $h_{FE} = 100$,

$$I_B = \frac{1\text{ mA}}{100} = 10\ \mu\text{A}.$$

The input resistance of the emitter follower, or loading resistance on the 10-V source, can now be calculated as

$$R_i = \frac{E}{I_B} = \frac{10\text{ V}}{10\ \mu\text{A}} = 1\text{ M}\Omega.$$

Now refer to the simple nonelectronic dc voltmeter circuit illustrated in Figure 8-4(b). Here again a 1-mA meter is used to measure a voltage of 10 V. In this case the loading resistance offered to the 10-V source is

$$R_i = \frac{E}{I_m} = \frac{10\text{ V}}{1\text{ mA}} = 10\text{ k}\Omega.$$

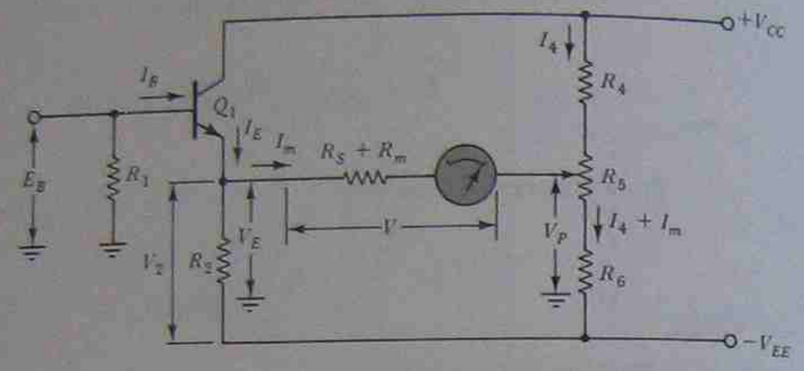
It is seen that the use of the emitter follower circuit increases the voltmeter resistance (in this case, from 10 kΩ to 1 MΩ). Consequently, the voltmeter loading effect is significantly reduced.

The transistor base-emitter voltage drop (V_{BE}) introduces an error in the simple emitter follower voltmeter in Figure 8-4(a) for voltages other than 10 V. For example, when $E = 5$ V the meter pointer should indicate one-half of full scale, i.e., 0.5 mA. However,

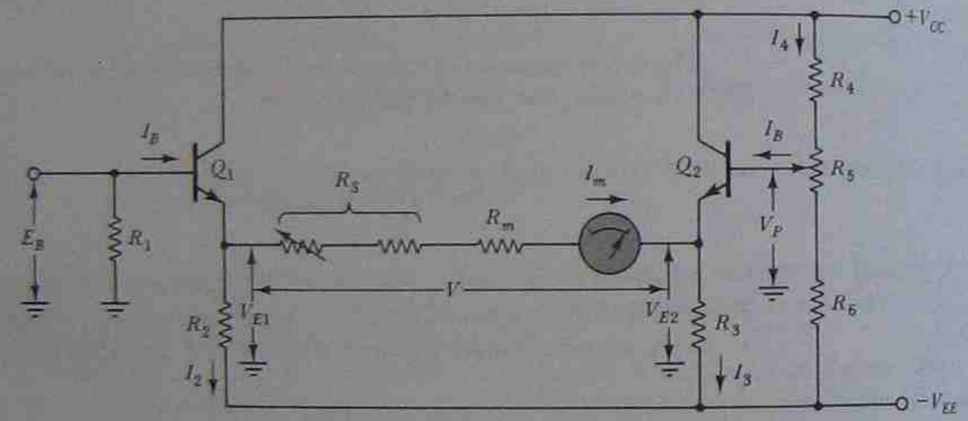
$$V_E = V_B - V_{BE} = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}$$

and,

$$I_E = \frac{V_E}{R_S + R_m} = \frac{4.3\text{ V}}{9.3\text{ k}\Omega} = 0.46\text{ mA}.$$



(a) Emitter follower voltmeter



(b) An additional transistor reduces the meter current effect on potential divider R_4, R_5 and R_6

FIGURE 8-5. Practical emitter follower voltmeter circuits.

This error can be eliminated by using a combination of potential divider and emitter follower circuits, as illustrated in Figure 8-5.

8-3-2 Practical Voltmeter Circuit

In Figure 8-5(a), resistors R_4 and R_6 together with potentiometer R_5 form a potential divider which provides an adjustable voltage V_p. Resistor R_2 carries all of the transistor emitter current I_E when no meter current is flowing. R_1 is a bias resistor which ensures that the transistor base is at ground potential when no input voltage is applied. Note that the circuit

uses a *plus-and-minus* or *dual polarity* supply. In this case, $V_{CC} = +10$ V and $V_{EE} = -10$ V are typical supply voltages.

When no input voltage is applied ($E_B = 0$), the base of transistor Q_1 is at 0 V. The transistor emitter voltage is

$$V_E = V_B - V_{BE} = 0\text{ V} - 0.7\text{ V} = -0.7\text{ V}$$

and

$$V_2 = V_E - V_{EE} = -0.7\text{ V} - (-10\text{ V}) = 9.3\text{ V}.$$

The moving contact at R_5 is adjusted to give $V_P = V_E = -0.7$ V, which gives a meter circuit voltage of

$$V = V_E - V_P = -0.7\text{ V} - (-0.7\text{ V}) = 0\text{ V}.$$

Thus, when $E_B = 0$, $V = 0$ and the meter pointer indicates zero.

Now suppose that an input voltage $E = 5$ V is applied. The transistor emitter voltage becomes

$$V_E = 5\text{ V} - 0.7\text{ V} = 4.3\text{ V}.$$

and

$$V_2 = V_E - V_{EE} = 4.3\text{ V} - (-10\text{ V}) = 14.3\text{ V}.$$

The meter voltage is

$$V = V_E - V_P = 4.3\text{ V} - (-0.7\text{ V}) = 5\text{ V}.$$

It is seen that all of the input voltage to be measured appears across the meter circuit. No part of E_B is lost across the transistor base-emitter junction. This applied for all levels of input voltage.

One assumption made in the above discussion is that the potential divider voltage V_P is not affected by the meter current. This is valid only if the potential divider current (I_4) is very much larger than the maximum meter current (I_m). Fulfilling this requirement may cause a large current drain on the dc power supply which provides V_{CC} and V_{EE}. The difficulty is overcome by using an additional emitter follower circuit, as illustrated in Figure 8-5(b). Now, I_4 has only to be much larger than I_B, which, as already shown, is very much smaller than I_E flowing in the transistor emitter. Example 8-1 demonstrates the circuit operation.

EXAMPLE 8-1 An emitter follower voltmeter as in Figure 8-5(b) has the following components: $R_2 = 3.9\text{ k}\Omega$, $R_3 = 3.9\text{ k}\Omega$, $R_4 = 2.7\text{ k}\Omega$, $R_5 = 1\text{ k}\Omega$, $R_6 = 2.2\text{ k}\Omega$, and $R_S + R_m = 1\text{ k}\Omega$. The meter current is $I_m = 1$ mA at full scale. $V_{CC} = +12$ V, $V_{EE} = -12$ V, and the (silicon) transistors have $h_{FE} = 100$. Determine V_P, I_{E1}, I_{E2}, I_4, and I_B when $E_B = 0$ V.

SOLUTION

When $E_g = 0$ V:

$$V_{B2} = V_{B1} = 0 \text{ V},$$
$$V_p = V_{B2} = 0 \text{ V}$$
$$V_{R2} = E_g - V_{BE} - V_{EE}$$
$$= 0 - 0.7 \text{ V} - (-12 \text{ V})$$
$$= 11.3 \text{ V},$$
$$I_{E2} = I_2 = \frac{V_{R2}}{R_2}$$
$$= \frac{11.3 \text{ V}}{3.9 \text{ k}\Omega} = 2.9 \text{ mA},$$
$$I_{E1} = I_{B1} = 2.9 \text{ mA}$$
$$I_1 = \frac{V_{CC} - V_{EE}}{R_4 + R_5 + R_6} \text{ (assuming } I_B \ll I_1\text{)}$$
$$= \frac{12 \text{ V} - (-12 \text{ V})}{2.7 \text{ k}\Omega + 1 \text{ k}\Omega + 2.2 \text{ k}\Omega}$$
$$= 4.07 \text{ mA}.$$

From Equations 8-1 and 8-2:

$$I_B = \frac{I_E}{h_{FE}} = \frac{2.9 \text{ mA}}{100}$$
$$= 29 \ \mu\text{A}.$$

($I_B \ll I_1$ *as assumed above*).

EXAMPLE 8-2 For the circuit in Example 8-1, determine the meter readings when $E_g = 1$ V and when $E_g = 0.5$ V.

SOLUTION

When $E_g = 1$ V:

$$V_{B1} = E_g - V_{BE} = 1 \text{ V} - 0.7 \text{ V}$$
$$= 0.3 \text{ V},$$
$$V_{R2} = V_p - V_{BE} = 0 - 0.7 \text{ V}$$
$$= -0.7 \text{ V},$$

$$V = V_{B1} - V_{B2} = 0.3 \text{ V} - (-0.7 \text{ V})$$
$$= 1 \text{ V} = E_g,$$
$$I_m = \frac{V}{R_3 + R_m} = \frac{1 \text{ V}}{1 \text{ k}\Omega}$$
$$= 1 \text{ mA } (\textit{full scale on the meter}).$$

When $E = 0.5$ V:

$$V_{B1} = E_g - V_{BE} = 0.5 \text{ V} - 0.7 \text{ V}$$
$$= -0.2 \text{ V},$$
$$V_{B2} = -0.7 \text{ V } (\textit{as before}),$$
$$V = V_{B1} - V_{B2} = -0.2 \text{ V} - (-0.7 \text{ V})$$
$$= 0.5 \text{ V} = E_g \textit{ once again},$$
$$I_m = \frac{V}{R_3 + R_m} = \frac{0.5 \text{ V}}{1 \text{ k}\Omega}$$
$$= 0.5 \text{ mA } (\textit{half scale on the meter}).$$

It is seen that the meter full scale represents 1 V, and half scale is read as 0.5 V.

Although a definite value of h_{FE} has been assumed for both transistors in Example 8-1, h_{FE} can vary widely from one transistor to another, even among transistors having the same type number. However, the actual value of h_{FE} is not important in emitter follower circuits so long as it is large enough to make I_B very much less than I_E.

Example 8-2 demonstrates that the voltage to be measured always appears across the meter circuit. When E is greater than zero, the voltage across R_2 is obviously increased, and consequently I_{E1} increases. Q_1 also supplies the meter current I_m, and this flows through resistor R_3. But since Q_2 emitter remains at -0.7 V, I_{E1} must decrease when I_m flows through R_3. The emitter followers are in fact operating as voltage sources with very low output resistances. The output resistance of such circuits is not zero. However, when the emitter current is larger than the maximum meter current, the output resistance of the emitter followers can be taken as zero.

As well as measuring positive levels of input voltage, the circuit in Figure 8-5(b) can just as easily measure negative input voltages. To facilitate dual polarity measurements, the meter circuit should include a two-way reversing switch.

It might be thought that the potential divider circuit (R_4, R_5, and R_6) could be replaced with a fixed nonadjustable potential divider using only two resistors. This would be true if $+V_{CC}$ and $-V_{EE}$ could be guaranteed to remain exactly equal, and if Q_1 and Q_2 were perfectly matched. R_5 is

an *electrical zero control* which affords adjustments to take care of differences between Q_1 and Q_2 and differences between V_{CC} and V_{EE}. The correct method for zero adjustment on any analog electronic meter is

1. With the power supply switched off, adjust the mechanical zero control on the deflection instrument to set the pointer to zero.
2. With the power supply switched on and the input terminals short-circuited, adjust the electrical zero control to set the pointer to zero.

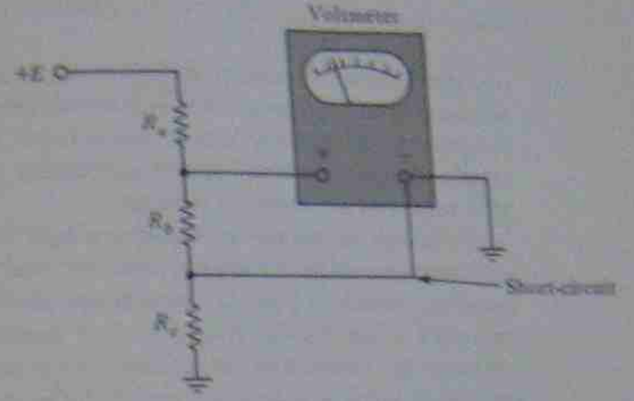
In Figure 8-5(b) R_5 is shown as a fixed resistor in series with an adjustable resistor. This is to provide a calibration control for the voltmeter. This control would normally require a screwdriver for adjustment rather than a control knob. It might also be accessible only by removal of a cover on the instrument cabinet. The normal procedure for calibrating the instrument is:

1. Zero the instrument pointer mechanically and electrically as described above.
2. Apply a precise known voltage to the instrument terminals. This should be measured by means of a dc potentiometer, as explained in Section 5-6.
3. Adjust R_5 until the instrument precisely indicates the applied voltage level.

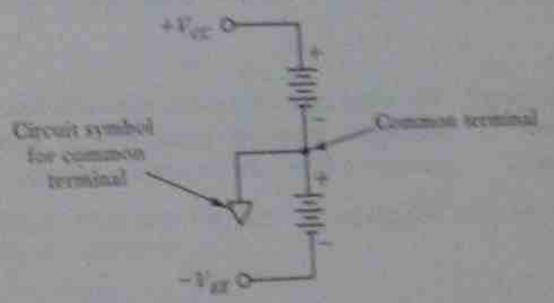
8-3-3 Ground Terminals and Floating Power Supplies

The circuits in Figure 8-5 show the input voltage E_g as being measured with respect to ground. However, this may not always be convenient. For example, suppose the voltage across resistor R_3 in Figure 8-6(a) were to be measured by a voltmeter with its negative terminals grounded. The voltmeter ground would short-circuit resistor R_C, and seriously affect the voltage and current conditions in the resistor circuit. Clearly, the voltmeter should *not* have one of its terminals grounded.

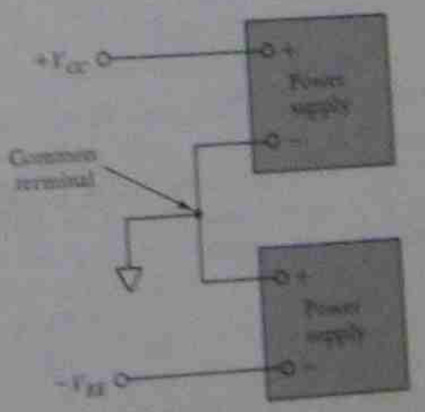
For the circuits in Figure 8-5 to function correctly, the lower end of R_1 must be at zero volts with respect to $+V_{CC}$ and $-V_{EE}$. The + and − supply voltage may be derived from two batteries [Figure 8-6(b)] or from two dc power supply circuits [Figure 8-6(c)]. In both cases, the negative terminal of the positive supply is connected to the positive terminal of the negative supply. For ±9-V supplies, V_{CC} is +9 V with respect to the common terminal, and V_{EE} is −9 V with respect to the common terminal. In many electronic circuits, the power supply common terminal is grounded. In electronic voltmeter circuits, this terminal is not grounded, simply to avoid the kind of problem already discussed. When left without any grounded terminal, the voltmeter supply voltages are said to be *floating*. This means that the common terminal assumes the absolute voltage (with respect to ground) of any terminal to which it may be connected.



(a) A voltmeter with one of its terminals grounded can short-circuit a component in a circuit in which voltage is being measured.



(b) ± supply using batteries



(c) ± supply using power supplies

FIGURE 8-6. The plus-and-minus supply voltages used in an electronic voltmeter must *not* have the common terminal grounded.

An inverted triangular symbol is employed to identify the common terminal or *zero voltage terminal* in a circuit [see Figure 8-6(b),(c)]. This is convenient for showing circuit components that are connected to the supply common terminal, or for identifying voltages that are measured with respect to the common terminal.

Although the electronic voltmeter supply voltages are allowed to float, some instruments have their common terminal connected to ground via a capacitor, usually 0.1 μF. If batteries are used as supply, the capacitor is connected to the chassis. Where a 115-V power supply is included in the voltmeter, the chassis and the capacitor are grounded. Thus, when measuring voltage levels in a transistor circuit, for example, the common terminal introduces a capacitance to ground wherever it is connected in the circuit. To avoid any effect on conditions within the circuit (oscillations or phase shifts), the voltmeter common terminal should always be connected to the transistor circuit ground or zero voltage terminal. All voltages are then measured with respect to this point.

8-3-4 Range Changing and Input Resistance

The input resistance to the transistor base can be increased by the use of an additional transistor connected, as illustrated in Figure 8-7. The base current of Q_1 is now the emitter current of Q_3. So, from Equations 8-1 and 8-3,

$$I_{B1} \simeq \frac{I_E}{h_{FE1}},$$

and

$$I_{B3} \simeq \frac{I_{B1}}{h_{FE3}} = \frac{I_E}{h_{FE1} \times h_{FE3}}.$$

Thus, for an emitter current of 2.9 mA (as in Example 8-1) and $h_{FE3} = h_{FE1} = 100$:

$$I_{B3} = \frac{2.9\text{ mA}}{100 \times 100} = 0.29\ \mu\text{A}.$$

With Q_1 in the circuit:

$$I_{B1} = \frac{2.9\text{ mA}}{100} = 29\ \mu\text{A},$$

and with $E_B = 1$ V, this represents a transistor input resistance of

$$R = \frac{1\text{ V}}{29\ \mu\text{A}} \simeq 34\ \text{k}\Omega.$$

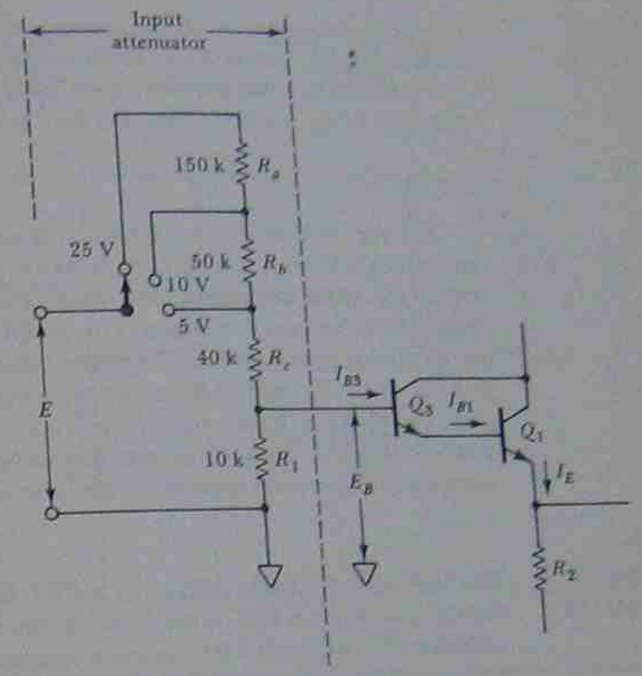


FIGURE 8-7. Input attenuator for range changing and additional transistor for increasing input resistance.

When Q_3 is included, the input resistance to the transistor base becomes

$$R = \frac{1\text{ V}}{0.29\ \mu\text{A}} \simeq 3.4\ \text{M}\Omega.$$

The potential divider constituted by resistors R_1, R_a, R_b, and R_c in Figure 8-7 allows large input voltages to be measured on an emitter follower voltmeter. This network, called an *input attenuator*, accurately divides the voltage to be measured before it is applied to the input transistor. When the maximum voltage is applied to any one of the inputs, the maximum level of E_B is always 1 V. For example, on the 25-V range:

$$E_B = E\frac{R_1}{R_1 + R_a + R_b + R_c}$$

$$= 25\text{ V} \times \frac{10\text{ k}\Omega}{10\text{ k}\Omega + 150\text{ k}\Omega + 50\text{ k}\Omega + 40\text{ k}\Omega}$$

$$= 1\text{ V}.$$

Thus, depending upon the selected input range, the instrument full-scale position is read as 25 V, 10 V, or 5 V.

It should be noted that the circuit input resistance is now much smaller than that at the transistor base. On the 25-V range, the input resistance is

$$R = R_a + R_b + R_c + R_1 = 250\ \text{k}\Omega.$$

On the 10-V range, the input resistance is $R_b + R_c + R_1 = 100$ kΩ, and on the 5-V range it is $R_c + R_1 = 50$ kΩ. If R_1 could be made ten times the 10-kΩ value illustrated, then each of the other attenuator resistors could also be increased ten times. This would result in a tenfold increase in the voltmeter input resistance. However, the transistor input resistance is in parallel with R_1, and this introduces some error into the attenuator network. If R_1 is made much larger than 10 kΩ, this error becomes unacceptable. A means of greatly increasing the input resistance of an electronic voltmeter is explained in the next section.

8-4 FET INPUT VOLTMETER

The high input resistance offered by a FET has already been discussed in Section 8-2. When a FET is connected at the input of an emitter follower voltmeter (Q_3 in Figure 8-8), the input resistance of the electronic voltmeter is significantly increased. Because the FET gate current is less than 50 ηA, a maximum resistance of 1 MΩ is typically employed to bias the gate of the FET to the zero voltage level. In Figure 8-8, the attenuator resistors R_a through R_d have a total resistance of 1 MΩ. When the attenuator is arranged as illustrated, the input resistance of the electronic voltmeter is always 1 MΩ. Also, the resistance at Q_3 gate is never larger than 1 MΩ.

Calculation shows that the FET input voltage is always 1 V when the maximum input is applied on any range. For example, on the 5-V range,

$$E_G = 5\ \text{V} \times \frac{R_b + R_c + R_d}{R_a + R_b + R_c + R_d}$$

$$= 5\ \text{V} \times \frac{100\ \text{k}\Omega + 60\ \text{k}\Omega + 40\ \text{k}\Omega}{800\ \text{k}\Omega + 100\ \text{k}\Omega + 60\ \text{k}\Omega + 40\ \text{k}\Omega}$$

$$= 1\ \text{V}.$$

The input resistance offered by this circuit to a voltage being measured is the total resistance of the attenuator, which is 1 MΩ. A 9-MΩ resistor could be included in series with the input terminal to raise the input resistance to 10 MΩ. This would further divide the input voltage by a factor of 10 before it is applied to the gate terminal.

Consider the voltage levels in the circuit of Figure 8-8. When $E = 0$ V, the FET gate is at the zero voltage level. But the gate of an *n*-channel FET must always be negative with respect to its source terminal. This is the same as stating that the source must be positive with respect to the gate. If V_{GS} is to be -5 V, and $E_G = 0$ V, the source terminal must be at $+5$ V. This means that the base terminal of Q_1 is at $+5$ V, and, since Q_2 base voltage must be equal to Q_1 base voltage, Q_2 base must also be at $+5$ V. As in the circuit of Figure 8-5(b), R_5 in Figure 8-8 is used to zero the meter when the input voltage is 0 V.

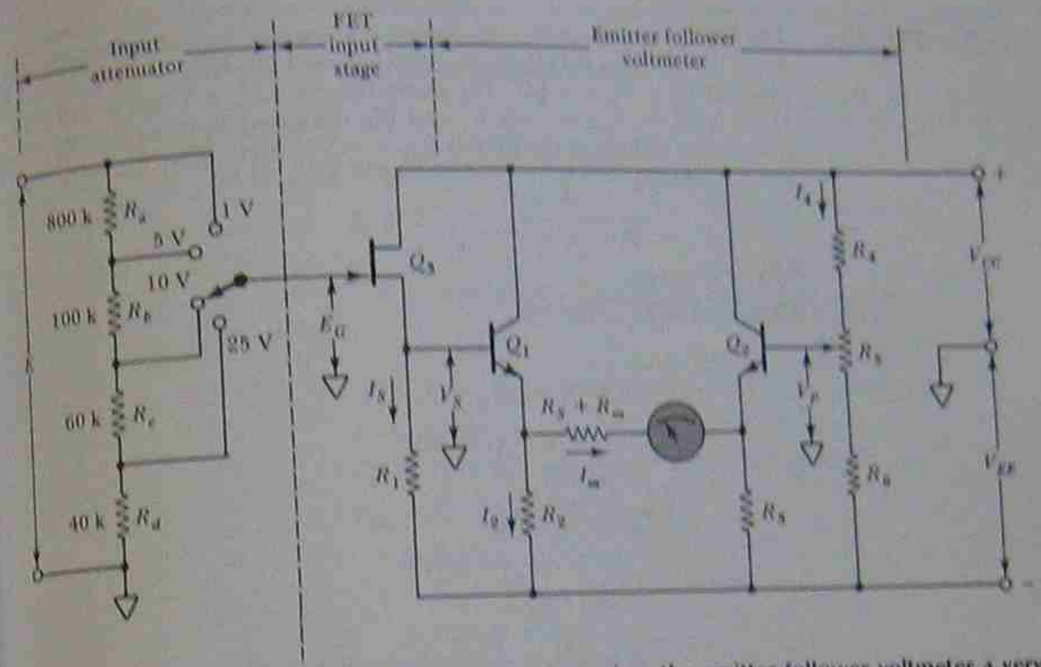


FIGURE 8-8. A FET input stage gives the emitter follower voltmeter a very high input resistance.

Now consider what occurs when a voltage to be measured is applied to the circuit input. With the attenuator shown, E_G will be a maximum of 1 V. This causes the FET source terminal to increase until V_{GS} is again -5 V. That is, V_S goes from $+5$ to $+6$ V to maintain V_{GS} equal to -5 V. The V_S increase of 1 V is also a 1-V increase in the base voltage of Q_1. As already explained in Section 8-3-2, all of this (1 V) increase in the base voltage of Q_1 appears across the meter circuit.

Because the source terminal voltage changes by the same amount as the voltage at the FET gate terminal, the FET circuit is called a *source follower*. It is similar to the bipolar transistor emitter follower, except that its input resistance is very much higher. It should be noted that, although a gate-source voltage of $V_{GS} = -5$ V has been assumed for the FET in Figure 8-8, V_{GS} could be anything from perhaps -2 V to -9 V, and the circuit would still function as described.

EXAMPLE 8-3 The FET input voltmeter in Figure 8-8 has the following components: $R_1 = 10\,\text{k}\Omega$, $R_2 = 5.6\,\text{k}\Omega$, $R_3 = 5.6\,\text{k}\Omega$, $R_4 = 1.2\,\text{k}\Omega$, $R_5 = 2\,\text{k}\Omega$, $R_6 = 2.7\,\text{k}\Omega$, and $R_S + R_m = 1\,\text{k}\Omega$. The meter current is $I_m = 1$ mA at full scale. $V_{CC} = +12$ V, $V_{EE} = -12$ V, and the transistors have $h_{FE} = 100$. The gate-source voltage of the FET is $V_{GS} = -5$ V. Determine V_P, I_S, I_{E1}, I_{E2}, and I_4 when $E_G = 0$ V.

SOLUTION

When $E_G = 0$ V:

$$
\begin{aligned}
V_S &= E_G - V_{GS} \\
&= 0\,\text{V} - (-5\,\text{V}) \\
&= 5\,\text{V}, \\
V_{R1} &= V_S - V_{EE} \\
&= 5\,\text{V} - (-12\,\text{V}) \\
&= 17\,\text{V}, \\
I_S &\simeq \frac{V_{R1}}{R_1} = \frac{17\,\text{V}}{10\,\text{k}\Omega} \text{ (assuming } I_B \ll I_S\text{)} \\
&= 1.7\,\text{mA}, \\
V_P &= V_S = 5\,\text{V}, \\
V_{R2} &= V_S - V_{BE} - V_{EE} \\
&= 5\,\text{V} - 0.7\,\text{V} - (-12\,\text{V}) \\
&= 16.3\,\text{V}, \\
I_{E1} &= I_2 = \frac{V_{R2}}{R_2} \\
&= \frac{16.3\,\text{V}}{5.6\,\text{k}\Omega} \simeq 2.9\,\text{mA}, \\
I_{E2} &= I_{E1} \simeq 2.9\,\text{mA}, \\
I_B &\simeq \frac{I_E}{h_{FE}} = \frac{2.9\,\text{mA}}{100} \\
&= 29\,\mu\text{A}, \\
I_4 &\simeq \frac{V_{CC} - V_{EE}}{R_4 + R_5 + R_6} \text{ (assuming } I_B \ll I_4\text{)} \\
&= \frac{12\,\text{V} - (-12\,\text{V})}{1.2\,\text{k}\Omega + 2\,\text{k}\Omega + 2.7\,\text{k}\Omega} \\
&\simeq 4.1\,\text{mA}.
\end{aligned}
$$

EXAMPLE 8-4 For the circuit in Example 8-3, determine the meter reading when $E = 7.5$ V and the meter is set to its 10-V range.

SOLUTION

On the 10-V range:

$$
\begin{aligned}
E_G &= E\frac{R_c + R_d}{R_a + R_b + R_c + R_d} \\
&= 7.5\,\text{V} \times \frac{60\,\text{k}\Omega + 40\,\text{k}\Omega}{800\,\text{k}\Omega + 100\,\text{k}\Omega + 60\,\text{k}\Omega + 40\,\text{k}\Omega} \\
&= 0.75\,\text{V}, \\
V_S &= E_G - V_{GS} = 0.75\,\text{V} - (-5\,\text{V}) \\
&= 5.75\,\text{V}, \\
V_{E1} &= V_S - V_{BE} = 5.75\,\text{V} - 0.7\,\text{V} = 5.05\,\text{V}, \\
V_{E2} &= V_P - V_{BE} = 5\,\text{V} - 0.7\,\text{V} \\
&= 4.3\,\text{V}, \\
V &= V_{E1} - V_{E2} = 5.05\,\text{V} - 4.3\,\text{V} \\
&= 0.75\,\text{V} = E_G, \\
I_m &= \frac{V}{R_S + R_m} = \frac{0.75\,\text{V}}{1\,\text{k}\Omega} \\
&= 0.75\,\text{mA (75\% of full scale)}.
\end{aligned}
$$

On the 10-V range, full scale represents 10 V, and 75% of full scale would be read as 7.5 V.

8-5 TRANSISTOR AMPLIFIER VOLTMETERS

The instruments discussed so far can measure a maximum of around 25 V. This could be extended further, of course, simply by modifying the input attenuator. The *minimum* (full-scale) voltage measurable by the electronic voltmeter circuits considered so far is 1 V. This too can be altered to perhaps a minimum of 100 mV by selection of a meter which will give FSD when 100 mV appears across $R_s + R_m$. Thus, FSD would be obtained when E_B (or E_G) in Figures 8-5 or 8-8 is 100 mV. However, for accurate measurement of low voltage levels, the voltage must be amplified before it is applied across $R_s + R_m$.

8-5-1 Difference Amplifier Voltmeter Circuit.

Transistors Q_1 and Q_2 together with R_2, R_5, and R_4 in Figure 8-9 constitute a *differential amplifier*, or *emitter coupled amplifier*. The circuit as a whole is known as a *difference amplifier voltmeter*. This is because when the voltage at the base of Q_2 is zero, and an input voltage (E) is applied to Q_1

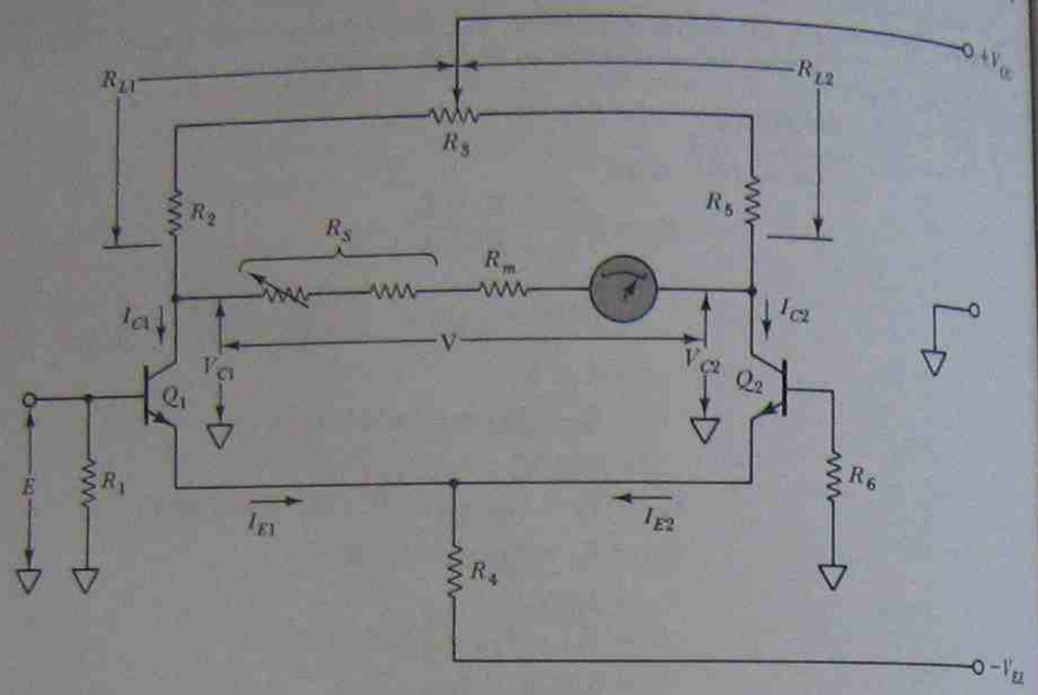


FIGURE 8-9. Difference amplifier type of transistor voltmeter for measurement of very small voltages.

base, the difference between the two base voltages is amplified and applied to the meter circuit.

When both Q_1 and Q_2 bases are at zero level, the voltage drop across emitter resistor R_4 is

$$V_{R4} = 0 - V_{BE} - (-V_{EE}),$$

and the current through R_4 is

$$I_{E1} + I_{E2} = V_{R4}/R_4.$$

The emitter currents I_{E1} and I_{E2} are equal when $E = 0$. Since $I_C \simeq I_E$,

$$I_{C1} = I_{C2} \simeq (I_{E1} + I_{E2})/2.$$

The voltage drop across R_{L1} is

$$V_{RL1} = I_{C1}R_{L1}$$

where $$R_{L1} = (R_2 + \tfrac{1}{2}R_3),$$

and $$V_{RL2} = I_{C2}R_{L2},$$

where $$R_{L2} = (R_5 + \tfrac{1}{2}R_3).$$

Therefore, the collector voltage of each transistor is

$$V_{C1} = V_{CC} - I_{C1}R_{L1},$$

and

$$V_{C2} = V_{CC} - I_{C2}R_{L2}.$$

The meter circuit voltage is

$$V = V_{C1} - V_{C2}.$$

When $E = 0$, $I_{C1} = I_{C2}$ and $V_{C1} = V_{C2}$, and the meter circuit voltage is $V = 0$.

Potentiometer R_3 is an alternative method of providing meter-zero adjustment. Q_2 base control, as in Figure 8-5(b), could also be used in the circuit of Figure 8-9. When the movable contact of R_3 is adjusted to the right, the portion of R_3 added to R_2 to make up R_{L1} is increased. Also, the portion of R_3 added to R_{L2} is reduced when R_3 moving contact is adjusted to the right. When the contact is moved left, the reverse is true. Thus, V_{C1} and V_{C2} can be adjusted differentially by means of R_3, and the meter voltage can be set to zero.

When a small positive voltage (E) is applied to the base of Q_1 in Figure 8-9, the current through Q_1 is increased, and that through Q_2 is decreased. An increase in I_{C1} causes $I_{C1}R_{L1}$ to increase and thus produces a fall in voltage V_{C1}. Similarly, a decrease in I_{C2} produces a rise in V_{C2}. The consequence of this is that the voltage across the meter circuit increases positively at the right-hand side and negatively at the left. This meter voltage (V) is directly proportional to the input voltage (E). The resultant meter current is directly proportional to the voltage to be measured.

It can be shown that the voltage gain from Q_1 base to the collector terminals is

$$\boxed{A_v = \frac{h_{FE}R_L}{h_{ie}},} \tag{8-5}$$

where h_{FE} is the transistor current gain (already discussed) and h_{ie} is the transistor base-emitter resistance as "seen" from the base terminal. To measure this (h_{ie}) parameter, the base-emitter voltage is changed by a small amount ΔV_{BE}, and the corresponding change in base current ΔI_B is noted. Then $h_{ie} = \Delta V_{BE} / \Delta I_B$. Typically, h_{ie} ranges from 1 kΩ to 2 kΩ. This is *not* the dc resistance offered to the voltage to be measured; rather it is an ac input resistance.

The meter voltage is

$$\boxed{V = A_v E.} \tag{8-6}$$

EXAMPLE 8-5 The circuit in Figure 8-9 has $R_2 = R_5 = 4.7\ \text{k}\Omega$, $R_3 = 500\ \Omega$, $R_4 = 3.3\ \text{k}\Omega$, $V_{CC} = +15\ \text{V}$, and $V_{EE} = -15\ \text{V}$. Determine the current and voltage levels throughout the circuit when $E = 0$.

SOLUTION

When V_{B1} and $V_{B2} = 0$:

$$I_{E1} + I_{E2} = \frac{0\ \text{V} - V_{BE} - V_{EE}}{R_4}$$
$$= \frac{0 - 0.7\ \text{V} - (-15\ \text{V})}{3.3\ \text{k}\Omega}$$
$$= 4.33\ \text{mA},$$

and
$$I_{E1} = I_{E2} = \frac{4.33\ \text{mA}}{2}$$
$$= 2.17\ \text{mA},$$
$$I_{C1} = I_{C2} = I_E$$
$$= 2.17\ \text{mA},$$
$$V_{RL1} = V_{RL2} = I_C(R_2 + \tfrac{1}{2}R_3)$$
$$= 2.17\ \text{mA}\left(4.7\ \text{k}\Omega + \frac{500\ \Omega}{2}\right)$$
$$= 10.7\ \text{V},$$
$$V_{C1} = V_{C2} = V_{CC} - V_{RL}$$
$$= 15\ \text{V} - 10.7\ \text{V}$$
$$= 4.3\ \text{V}.$$

EXAMPLE 8-6 The circuit described in Example 8-5 has transistors with $h_{FE} = 80$ and $h_{ie} = 1.5\ \text{k}\Omega$. The meter used gives FSD when $I_m = 100\ \mu\text{A}$, and its coil resistance is 1.2 kΩ. Calculate the resistance of R_s to give FSD when $E = 10\ \text{mV}$.

SOLUTION

Equation 8-5,

$$A_v = \frac{h_{FE}R_L}{h_{ie}} = \frac{h_{FE}(R_2 + \tfrac{1}{2}R_3)}{h_{ie}}$$
$$= \frac{80(4.7\ \text{k}\Omega + 250)}{1.5\ \text{k}\Omega}$$
$$= 264,$$

Equation 8-6,

$$V = A_v E = 264 \times 10\ \text{mV}$$
$$= 2.64\ \text{V},$$
$$I_m = \frac{V}{R_s + R_m},$$

or
$$R_s = \frac{V}{I_m} - R_m$$
$$= \frac{2.64\ \text{V}}{100\ \mu\text{A}} - 1.2\ \text{k}\Omega$$
$$= 25.2\ \text{k}\Omega.$$

One disadvantage of the difference amplifier voltmeter is that the voltage gain is a little unpredictable because of the wide spread in values of h_{FE}. This requires the facility for a large adjustment in R_s to compensate for the resultant wide range of A_v values from one voltmeter circuit to another. In Example 8-6, if h_{FE} were 40 or 160 instead of 80, R_s would have to be halved or doubled respectively. The feedback amplifier voltmeter discussed next uses a circuit with a precisely predictable voltage gain.

8-5-2 Feedback Amplifier Voltmeter

The circuit shown in Figure 8-10 can be designed to accurately amplify low voltages to measurable levels. Transistors Q_1 and Q_2 are connected as a differential amplifier, and they share a common *constant current source* connected to their emitters. The constant current source is simply a one-transistor circuit which does exactly what is expected; it provides a constant level of current. This current normally divides equally between the emitters of Q_1 and Q_2. Note that the base of Q_1 is biased to the zero voltage level via resistor R_1. As will become clear later, the base of Q_2 is also at the same voltage level as Q_1 base.

The constant current source can easily be set to a level of 2 mA, so that I_{C1} and I_{C2} are normally each 1 mA. If $I_{C1} = 1\ \text{mA}$,

$$V_{R2} = I_{C1}R_2 = 1\ \text{mA} \times 8.2\ \text{k}\Omega$$
$$= 8.2\ \text{V}.$$

So the collector voltage of Q_1 is

$$V_{C1} = V_{CC} - V_{R2} = 12\ \text{V} - 8.2\ \text{V}$$
$$= 3.8\ \text{V}.$$

This (3.8 V) is also the base voltage of Q_3, since Q_3 base is connected to Q_1 collector. The emitter of (*pnp* transistor) Q_3 is provided with 4.5 V

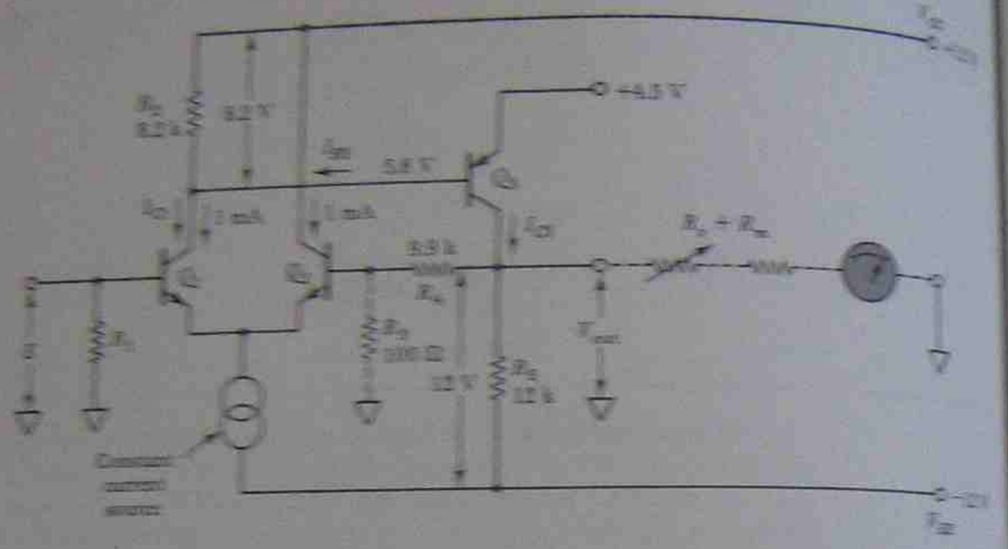


FIGURE 8-10 The transistor feedback amplifier voltmeter accurately amplifies small voltages to measurable levels.

derived from the circuit power supply. This means that the base-emitter junction of Q_3 is 0.7 V, as required for a silicon device.

If the circuit is designed for a 1-mA collector current in Q_3, the voltage drop across R_3 is

$$\begin{aligned} V_{R3} &= I_{C3}R_3 = 1\text{ mA} \times 12\text{ k}\Omega \\ &= 12\text{ V}. \end{aligned}$$

Therefore, the collector voltage of Q_3 is 12 V above V_{EE}, or,

$$\begin{aligned} V_{C3} &= V_{EE} + 12\text{ V} = -12\text{ V} + 12\text{ V} \\ &= 0\text{ V}. \end{aligned}$$

Since the base of Q_4 is connected to the collector of Q_3 via resistor R_4, Q_4 base voltage is also zero volts. This is the same level as that at the base of Q_1, as stated earlier.

Consider what would happen if the base voltage of Q_4 was not exactly equal to the base voltage of Q_1. Suppose Q_4 base was slightly below Q_1 base. This would cause Q_4 to take a reduced share of the constant emitter current and produce a corresponding increase in the current through Q_3. The increased current flow through Q_3 would increase the voltage drop across R_3 and produce an increase in base current I_{B3} to transistor Q_3. The increase in I_{B3} would, in turn, result in an increased level of I_{C3}. The

would increase the voltage drop across R_3 and raise the voltage level at the base of Q_2 until it again equals the level of Q_1 base voltage. Similarly, if the base of Q_4 were to become *higher* than Q_1 base voltage, I_{C3} would be reduced, causing I_{B3} and I_{C3} to decrease. Consequently, V_{R3} would drop, and the base of Q_4 would go down until it returns to the same level as Q_1 base.

It is seen that this circuit arrangement always stabilizes the base voltage of Q_4 to be exactly equal to that of Q_1. If the base of Q_1 is raised above or reduced below the zero level, the base of Q_4 follows it faithfully. Thus the output at Q_3 collector follows the input at Q_1 base. If a meter is connected to the output of the circuit, as illustrated broken in Figure 8-10, the circuit functions as an excellent emitter follower voltmeter. For satisfactory performance of this circuit it is important that Q_3 and Q_4 be *matched transistors*. V_{BE} and I_B can differ from one transistor to another even though their collector currents may be equal. Matched transistors have closely equal base-emitter voltages and base currents.

Now consider what happens when additional resistor R_5 is included, as shown broken in Figure 8-10. Note that $R_5 = 100\ \Omega$ and $R_4 = 9.9\ \text{k}\Omega$. Once again, the output voltage will be exactly at the zero level while the input voltage remains zero. When an input of $E = 10$ mV is applied to the base of Q_1, the output increases until V_{R5} also equals 10 mV. This means that the voltage across R_5 is 10 mV. Since R_5 and R_4 are a potential divider, the voltage across $R_5 + R_4$ is

$$V_{out} = 10\text{ mV} \times \frac{R_5 + R_4}{R_5},$$

or

$$\begin{aligned} V_{out} &= V_{in}\frac{R_5 + R_4}{R_5} \\ &= 10\text{ mV} \times \frac{9.9\text{ k}\Omega + 100\ \Omega}{100\ \Omega} \\ &= 1\text{ V}. \end{aligned}$$

It is seen that an input of 10 mV is amplified to an output of 1 V. The 1-V output can now be applied to a meter circuit to produce pointer deflection. The amplification, or gain, of the circuit is

$$\boxed{A_v = \frac{R_5 + R_4}{R_5}}. \tag{8-7}$$

If precision resistors are used the gain will always be precise.

When the circuit is carefully analyzed, the internal gain of the circuit can be shown to be a very large quantity. This is reduced to the desired

gain by the use of R_3 and R_4. Because R_3 and R_4 reduce and stabilize the circuit gain, they are said to provide *negative feedback*.

A FET could be used at the input of the circuit in Figure 8-10 (or in Figure 8-9) to give a very high input resistance. This would be connected just like Q_3 in Figure 8-8, and it would necessitate some changes in voltage and current levels throughout Figure 8-10. An electrical zero control [like Q_2 and its associated components in Figure 8-5(b)] could also be included in the feedback amplifier voltmeter instead of directly connecting one side of the deflection meter to the common terminal of the supply. The zero control would afford adjustments for gate-source voltage differences in FETs and for any other component variations.

EXAMPLE 8-7 The feedback amplifier voltmeter in Figure 8-10 uses a deflection meter which gives FSD when $I_m = 1$ mA. The meter circuit resistance is $R_s + R_m = 1$ kΩ. Calculate the input voltage measured when the meter is indicating 25% of full scale. Also determine the collector current of Q_3 at this point.

SOLUTION

At 25% of full scale:

$$\begin{aligned} I_m &= 25\% \text{ of } I_m \\ &= 25\% \text{ of } 1 \text{ mA} \\ &= 0.25 \text{ mA}, \\ V_{out} &= I_m(R_s + R_m) \\ &= 0.25 \text{ mA} \times 1 \text{ k}\Omega \\ &= 250 \text{ mV}, \end{aligned}$$

input voltage,

$$\begin{aligned} E = V_{R3} &= V_{out}\frac{R_3}{R_3 + R_4} \\ &= 250 \text{ mV} \times \frac{100\ \Omega}{100\ \Omega + 9.9\ \text{k}\Omega}, \\ E &= 2.5 \text{ mV}, \\ I_{C3} &= I_{R4} + I_{R5} + I_m \\ &= \frac{V_{out}}{R_3 + R_4} + \frac{V_{out} - V_{EE}}{R_5} + I_m \\ &= \frac{250 \text{ mV}}{100\ \Omega + 9.9\ \text{k}\Omega} + \frac{250 \text{ mV} - (-12 \text{ V})}{12\ \text{k}\Omega} + 0.25 \text{ mA} \\ &\approx 1.3 \text{ mA}. \end{aligned}$$

8-6 INTEGRATED CIRCUIT OPERATIONAL AMPLIFIERS IN VOLTMETERS

8-6-1 Integrated Circuit Operational Amplifiers

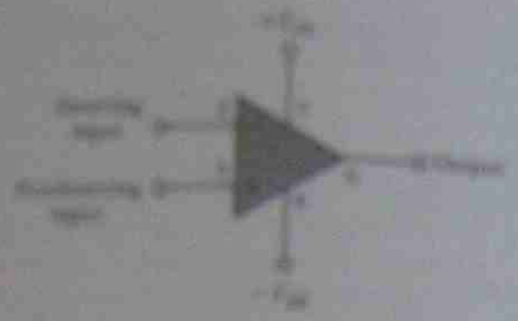
An *integrated circuit (IC) operational amplifier* consists of many transistors and resistors interconnected to form a complete circuit, all contained in one small package. An *operational amplifier* has two input terminals and one output. The inputs are identified as *inverting input* and *noninverting input*, and they each have a very high input resistance. The output resistance of the circuit is very low, and the amplifier internal gain is very high.

Look again at the transistor amplifier voltmeter circuit in Figure 8-10. When the input voltage E is increased, the output (V_{out}) increases. Therefore, the input terminal at the base of Q_1 could be identified as a *noninverting input*. This simply means that the output is not inverted by comparison with the input. Now suppose that resistor R_4 is removed, and that an input voltage is applied to the base of transistor Q_2. If the input to Q_2 base is positive, Q_2 emitter takes an increased share of the constant current common to the emitters of Q_1 and Q_2. This means current flow through Q_1 emitter and collector terminals is reduced. The reduced level of I_{C1} produces a reduction in V_{R2} and I_{B3}, and this results in a reduction in I_{C3}. The fall in I_{C3} causes a drop in the voltage across R_5, which is also a drop in V_{out}. It is seen that a positive-going input at Q_2 base results in a negative-going output at Q_3 collector. Similarly it can be shown that a negative-going input at Q_2 base produces a positive-going output voltage. The output is inverted with respect to inputs at Q_2 base, and so Q_2 base can be identified as an *inverting input* terminal.

In Section 8-5-2, it has already been explained that the amplifier in Figure 8-10 has a very high internal gain which is controlled by R_3 and R_4. Thus, omitting the meter circuit and resistor R_4, Figure 8-10 is the basic circuit of an operational amplifier. It has a high gain, one output terminal, and two (inverting and noninverting) inputs. It should be noted that IC operational amplifier circuits are much more complex than the circuit in Figure 8-10. Also, the internal gain of an *IC op-amp* is typically 200 000, which is much larger than the internal gain normally possible with the three transistors in Figure 8-10.

The input resistance of IC op-amps is very high. Those with bipolar transistor input stages have typical input currents on the order of 0.2 μA. FET input op-amps are also available with very much lower input current levels, i.e., extremely high input resistances. The output resistance of an op-amp is always very low, so that the circuit can easily supply the necessary current to a deflection instrument.

Figure 8-11 shows the triangular graphic symbol used for an operational amplifier. Note that *plus-and-minus* supply voltages are normally required, although some IC op-amps can operate with only a single polarity supply. Typical supply voltages range from ±5 V to ±22 V. The inverting input is identified with a *minus* (−) sign, and the noninverting with a *plus* (+) sign, as illustrated. Two typical IC op-amp packages are also shown in Figure 8-11. The *dual-in-line* plastic package is the most frequently used of the two.



Circuit symbol



FIGURE 8-11 IC operational amplifier circuit symbol and typical package

8-6-2 Voltage Follower

The IC operational amplifier voltage follower shown in Figure 8-12 can be compared to the circuit in Figure 8-10 where R_1 is removed from Figure 8-10, as explained in Section 8-3-2, where R_1 is left out of the circuit the output voltage equals the input voltage, and V_{out} precisely follows all changes in E. The voltage follower is analogous to the single transistor emitter follower circuit. However, unlike the emitter follower, there is no base-emitter voltage drop from input to output. So the voltage follower accurately reproduces the input at its output terminal. The voltage follower also has much higher input resistance and lower output resistance than its emitter follower.

The meter circuit in Figure 8-12 is connected exactly the same as that in Figure 8-10. The input attenuator is similar to the one shown in Figure 8-7 and discussed in Section 8-3-4. It is seen that voltage to be measured is potentially divided by the input attenuator and then measured directly at the deflection meter. The voltage follower eliminates the voltmeter loading effect that the deflection instrument would normally offer to the attenuator.

Apart from any error due to the deflection instrument or inaccuracy in the resistor employed, there is a small error introduced by the operational amplifier. As demonstrated by Example 8-8, this error is inversely proportional to the amplifier internal gain.

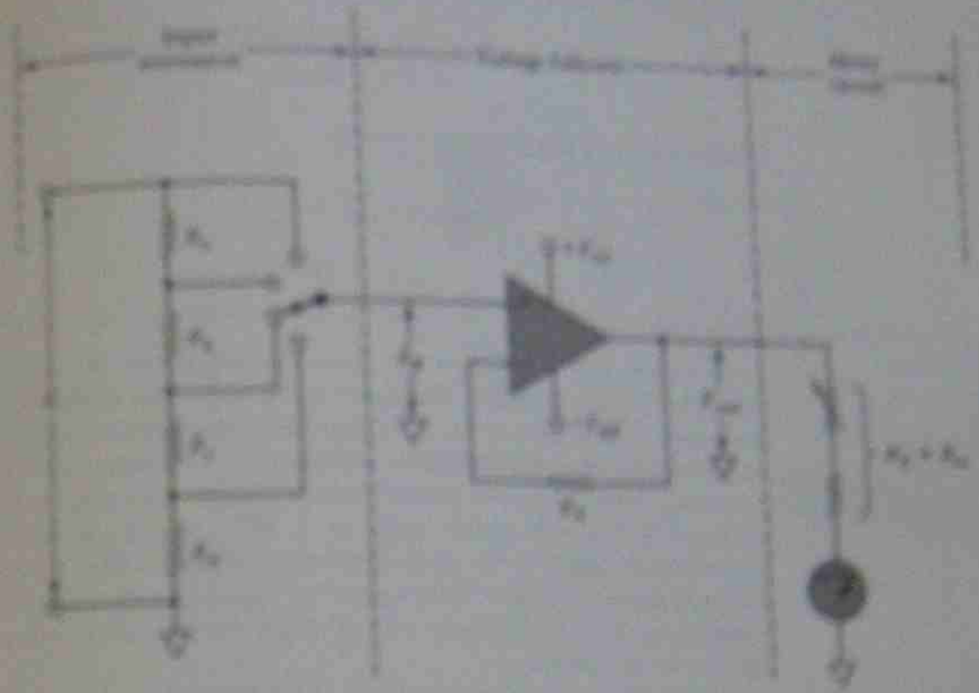


FIGURE 8-12 IC operational amplifier voltage follower voltmeter

EXAMPLE 8-8 A voltage follower voltmeter uses an IC operational amplifier with an internal voltage gain of 200 000. The maximum voltage applied directly to the noninverting input is $E_{in} = 1$ V. Calculate the percentage error in the measured voltage due to the operational amplifier.

SOLUTION

$$V_{out} = E_{in} = 1 \text{ V}$$

To produce V_{out}, there must be a difference between the inverting and noninverting inputs. If there were no difference, there would be no output voltage change.

$$\text{Input difference} = \frac{V_{out}}{\text{amplifier internal gain}}$$

$$= \frac{1 \text{ V}}{200\,000}$$

$$= 5 \mu\text{V},$$

and measuring input = E_{in} while inverting input = V_{out}.

Input difference $= E_B - V_{out}$, or

$$V_{out} = E_B - \textit{input difference}$$
$$= 1\text{ V} - 5\ \mu\text{V}.$$

Output error due to amplifier gain $= 5\ \mu$ V;

$$\textit{error} = \frac{5\ \mu\text{V}}{1\text{ V}} \times 100\%$$
$$= (5 \times 10^{-4})\%.$$

Example 8-8 shows that the error introduced by the operational amplifier is quite negligible compared to the error due to the deflection instrument. The design of an IC voltage follower voltmeter involves only the calculation of meter multiplier resistance R_s, and selection of suitable attenuator resistors for the desired voltage ranges. The total attenuator resistance is normally made equal to 1 MΩ, and R_4 is selected as approximately equal to the total attenuator resistance. This is to ensure that each input terminal is "looking out" at approximately the same series resistance, so that small resistive voltage drops due to I_B are equal at each input as far as possible.

8-6-3 Amplifier Type Operational Amplifier Voltmeter

Like a transistor amplifier, an IC operational amplifier can be used to amplify low voltages to levels measurable by a deflection instrument. Figure 8-13 shows a circuit suitable for this purpose. Like the voltage follower, this circuit may also be compared to the transistor circuit in Figure 8-10. Input voltage E is applied to the noninverting input, and the output voltage is potentially divided across resistors R_3 and R_4, and then fed back to the inverting input terminal. Therefore, the circuit in Figure 8-13 operates exactly as described for Figure 8-10, when R_3 is included in Figure 8-10.

The operational amplifier circuit in Figure 8-13 is known as a *noninverting amplifier*, because its output is positive going when a positive-going input is applied, and vice versa. Its input resistance is very high, and, as with other op-amp circuits, it has a very low output resistance. The gain of the circuit is calculated from Equation 8-7 by

$$A_v = \frac{R_3 + R_4}{R_3}.$$

A noninverting amplifier is very easily designed. The potential divider current (I_4) is selected very much larger than the input current (I_B), so that I_B has no significant effect upon the fed-back voltage. The total

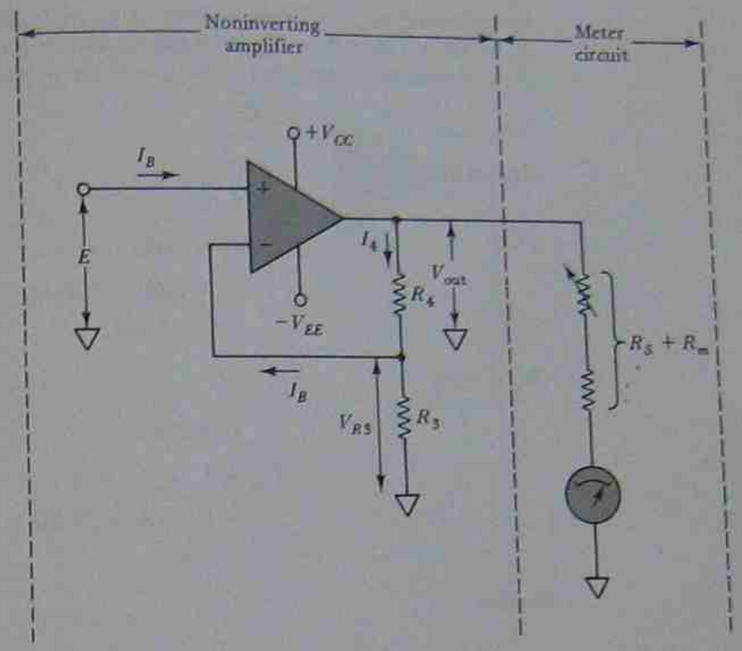


FIGURE 8-13. Noninverting amplifier voltmeter for measurement of very small voltages.

resistance ($R_3 + R_4$) is calculated as

$$\boxed{R_3 + R_4 = \frac{V_{out}}{I_4}.} \qquad (8\text{-}8)$$

Then, since $V_{R3} = E$,

$$\boxed{R_3 = \frac{E}{I_4}.} \qquad (8\text{-}9)$$

As with the voltage follower circuit, a small error is introduced by the internal gain of the operational amplifier. Once again, this can be shown to be negligible compared to the normal deflection meter error.

EXAMPLE 8-9 An IC operational amplifier has an internal voltage gain of 200 000 and input bias currents of 0.2 μA. The op-amp is to be used as a noninverting amplifier in the electronic voltmeter circuit of Figure 8-13. The voltage to

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be measured has a maximum level of 20 mV, and the meter circuit has $I_m = 100\ \mu A$ and $R_s + R_m = 10\ k\Omega$. Calculate suitable values for R_3 and R_4 and determine the input resistance of the voltmeter.

SOLUTION

Refer to Figure 8-13:

$$I_4 \gg I_B.$$

$$\text{Let } I_4 = 1000 \times I_B$$
$$= 1000 \times 0.2\ \mu A$$
$$= 0.2\ mA.$$

At full scale:

$$I_m = 100\ \mu A,$$

and

$$V_{out} = I_m(R_s + R_m)$$
$$= 100\ \mu A \times 10\ k\Omega$$
$$= 1\ V.$$

Equation 8-8,

$$R_3 + R_4 = \frac{V_{out}}{I_4} = \frac{1\ V}{0.2\ mA}$$
$$= 5\ k\Omega.$$

Equation 8-9,

$$R_3 = \frac{E}{I_4} = \frac{20\ mV}{0.2\ mA}$$
$$= 100\ \Omega,$$
$$R_4 = (R_3 + R_4) - R_3$$
$$= 5\ k\Omega - 100\ \Omega$$
$$= 4.9\ k\Omega.$$

Input resistance,

$$R = \frac{E}{I_B} = \frac{20\ mV}{0.2\ \mu A}$$
$$= 100\ k\Omega.$$

8-6-4 Voltage-to-Current Converter

The circuit shown in Figure 8-14 can be compared to Figure 8-13. Instead of connecting the meter between the op-amp output and ground, the meter is substituted in place of resistor R_4. There is no meter series resistor R_s;

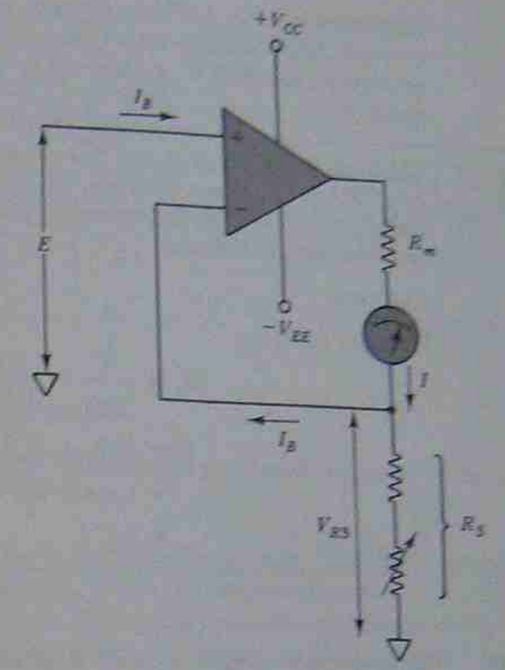


FIGURE 8-14. Voltmeter using a voltage-to-current converter circuit.

however, R_3 is now partially adjustable. As already explained for the noninverting amplifier circuit, the voltage drop across R_3 is always equal to input voltage E. If the input increases or decreases, V_{R3} follows it precisely. This means that current I, which flows through R_3 and the meter, is

$$I = \frac{E}{R_3}.$$

Suppose an input voltage of 100 mV is to give FSD on the instrument. R_3 is calculated as

$$\boxed{R_3 = \frac{E}{I_{FSD}}.} \qquad (8\text{-}10)$$

Part of R_3 is made adjustable so that the instrument can be calibrated. A precise known level of input voltage is applied, then R_3 is adjusted until the meter pointer indicates the applied voltage.

For this *voltage-to-current converter* circuit to function correctly, the voltage developed across $R_m + R_3$ must always be less than the supply voltage. The output terminal of the operational amplifier can be made to go up to

be measured has a maximum level of 20 mV, and the meter circuit has $I_m = 100\ \mu A$ and $R_s + R_m = 10\ k\Omega$. Calculate suitable values for R_3 and R_4 and determine the input resistance of the voltmeter.

SOLUTION

Refer to Figure 8-13:

$$I_4 \gg I_B.$$

$$\text{Let } I_4 = 1000 \times I_B$$
$$= 1000 \times 0.2\ \mu A$$
$$= 0.2\ mA.$$

At full scale:

$$I_m = 100\ \mu A,$$

and

$$V_{out} = I_m(R_s + R_m)$$
$$= 100\ \mu A \times 10\ k\Omega$$
$$= 1\ V.$$

Equation 8-8,

$$R_3 + R_4 = \frac{V_{out}}{I_4} = \frac{1\ V}{0.2\ mA}$$
$$= 5\ k\Omega.$$

Equation 8-9,

$$R_3 = \frac{E}{I_4} = \frac{20\ mV}{0.2\ mA}$$
$$= 100\ \Omega,$$
$$R_4 = (R_3 + R_4) - R_3$$
$$= 5\ k\Omega - 100\ \Omega$$
$$= 4.9\ k\Omega.$$

Input resistance,

$$R = \frac{E}{I_B} = \frac{20\ mV}{0.2\ \mu A}$$
$$= 100\ k\Omega.$$

8-6-4 Voltage-to-Current Converter

The circuit shown in Figure 8-14 can be compared to Figure 8-13. Instead of connecting the meter between the op-amp output and ground, the meter is substituted in place of resistor R_4. There is no meter series resistor R_s;

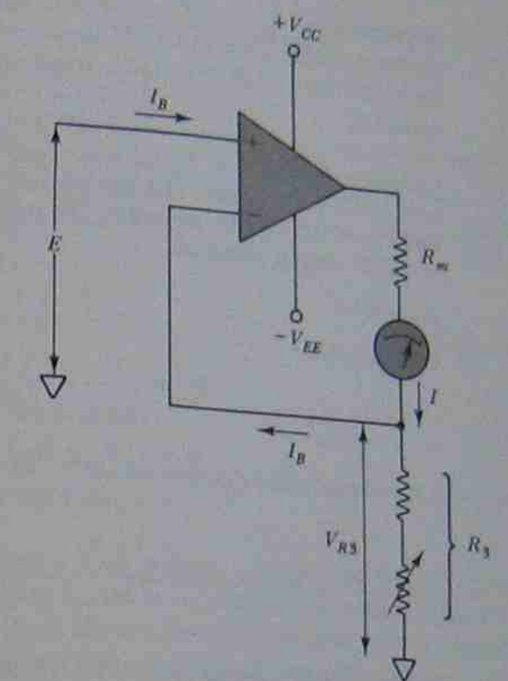


FIGURE 8-14. Voltmeter using a voltage-to-current converter circuit.

however, R_3 is now partially adjustable. As already explained for the noninverting amplifier circuit, the voltage drop across R_3 is always equal to input voltage E. If the input increases or decreases, V_{R3} follows it precisely. This means that current I, which flows through R_3 and the meter, is

$$I = \frac{E}{R_3}.$$

Suppose an input voltage of 100 mV is to give FSD on the instrument. R_3 is calculated as

$$\boxed{R_3 = \frac{E}{I_{FSD}}.} \qquad (8\text{-}10)$$

Part of R_3 is made adjustable so that the instrument can be calibrated. A precise known level of input voltage is applied, then R_3 is adjusted until the meter pointer indicates the applied voltage.

For this *voltage-to-current converter* circuit to function correctly, the voltage developed across $R_m + R_3$ must always be less than the supply voltage. The output terminal of the operational amplifier can be made to go up to

approximately $V_{cc} - 2$ V, or down to approximately $-(V_{ee} - 2\text{V})$ V. For example, when using a ±15-V supply, the output cannot be expected to go higher than +13 V or lower than −13 V, if the circuit is to function correctly.

EXAMPLE 8-10 Calculate the value of R_s for the circuit in Figure 8-14, if $E = 1$ V is to drive FSD on the meter. The moving-coil meter has $I = 1$ mA at full-scale and $R_m = 100\ \Omega$. Also determine the maximum voltage at the operational amplifier output terminal.

SOLUTION

Equation 8-10,

$$R_s = \frac{E}{I_{(FSD)}} = \frac{1\text{ V}}{1\text{ mA}} = 1\text{ k}\Omega,$$

$$V_o = I(R_s + R_m)$$
$$= 1\text{ mA}(1\text{ k}\Omega + 100\ \Omega)$$
$$= 1.1\text{ V}.$$

8-7 VACUUM TUBE VOLTMETERS

The vacuum tube voltmeter (VTVM) is an older instrument than transistor or integrated circuit voltmeters. It is unlikely that new VTVMs are currently in production; however, existing equipment does not vanish when new methods are developed. There are still vacuum tube instruments in service, so it is important for students of electronic technology to understand VTVMs.

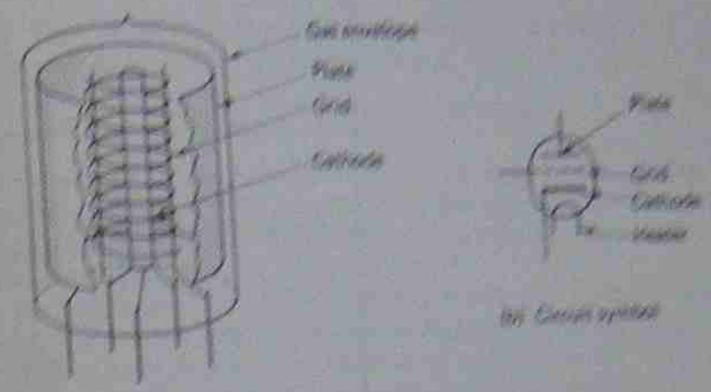
8-7-1 The Vacuum Triode

The vacuum triode is comparable to an n-channel field effect transistor. It has three electrodes: plate, cathode and grid. When the plate is positive with respect to the cathode, a plate current flows. The level of this current is controlled by the grid, which is normally maintained at a negative potential with respect to the cathode. When the (negative) grid-cathode voltage, $-V_{GK}$, is increased, the plate current I_p is reduced. When $-V_{GK}$ is reduced, I_p is increased.

The construction of a vacuum triode is illustrated in Figure 8-15(a). The plate is a nickel cylinder with the cathode as a much smaller cylinder at its center. Between the cathode and the plate a wire grid is situated. This is the grid. The cathode has an electrical heater which requires a separate supply. The three electrodes are contained in a glass envelope from which the air has been evacuated. Connecting leads to the electrode and for the cathode heater are brought to pins which project through the base of the tube, as illustrated.

When the cathode is heated, electrons are emitted from its surface, forming an electron cloud around it. The electrons are attracted through the grid to the plate which has a high positive voltage. The flow of electrons constitutes the plate current. I_p can be increased or decreased or cut off completely by appropriate levels of (negative) grid-cathode voltage. Since no grid current flows, the cathode current I_K equals the plate current.

The graphic symbol for the vacuum triode is illustrated in Figure 8-15(b). Typical plate-to-cathode voltage levels are 25 V to 300 V. For a low current triode, plate currents range from a few milliamps to perhaps 100 mA. Grid-to-cathode voltages are usually between 0 and −10 V. The heater supply is normally 6.3 V, and for simplicity connecting cables to the heaters are not usually shown on vacuum tube circuit diagrams.



(a) Construction (b) Circuit symbol

FIGURE 8-15 Construction and circuit symbol of triode vacuum tube.

8-7-2 Cathode Follower VTVM

The cathode follower is the vacuum tube version of the transistor emitter follower and the FET source follower circuit. All of these circuits provide high input resistance, low output resistance, and a voltage gain of 1. The cathode follower VTVM in Figure 8-16 is similar to the transistor emitter follower voltmeter circuit in Figure 8-5(b). A plus-and-minus supply is again used, but in this case the supply voltage might typically be ±100 V. When $E = 0$ V, the grid of Q_1 is at the zero potential level. The grid of Q_1 can be adjusted to zero by means of potentiometer R_2. The cathodes of Q_1 and Q_2 might typically be at +3 V, so that the (zero level) grids are at −3 V with respect to the cathodes. With both cathodes at the same potential, the meter voltage (V) is zero and no meter current flows.

A positive voltage (E) applied to the input terminal of the circuit in Figure 8-16 produces a grid voltage (E_{G1}) on Q_1. This causes the cathode current I_{K1} to increase, producing an increased voltage drop across R_1, which makes V_{G1K} once again equal to −3 V. If $E_{G1} = 1$ V, V_{K1} increases by 1 V, from 3 to 4 V, or the cathode follows the voltage change on the

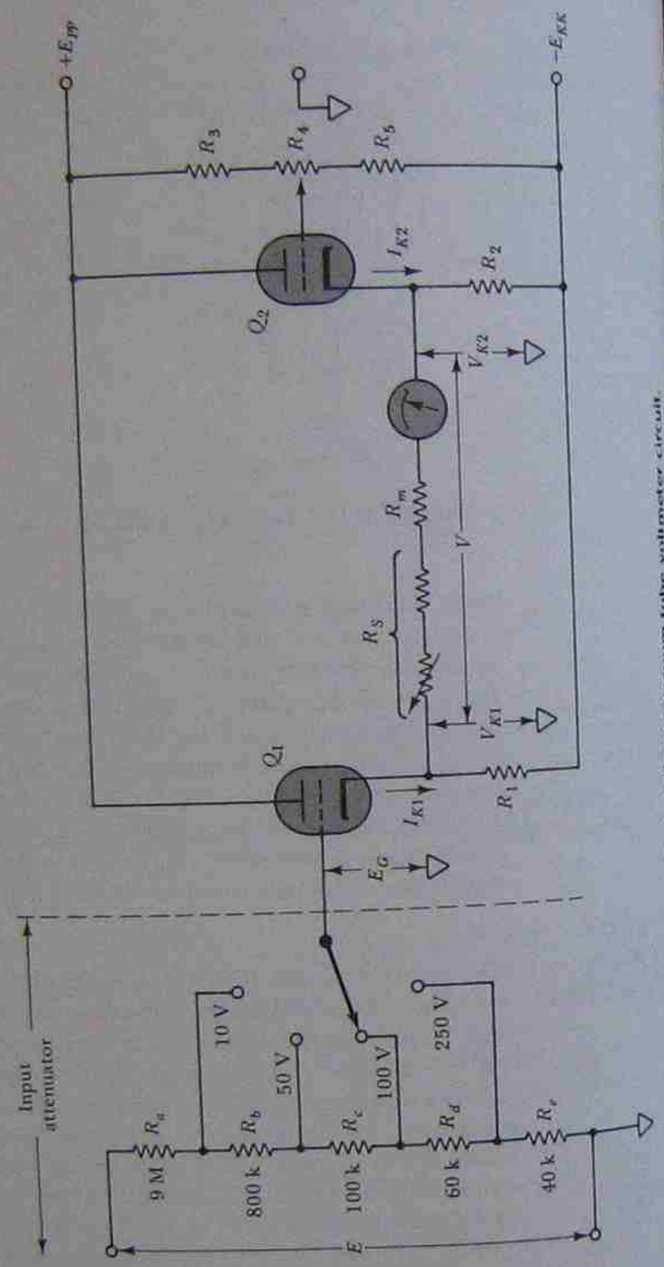


Figure 8-16. Cathode follower vacuum tube voltmeter circuit.

grid. There is no corresponding voltage change at the cathode of Q_2, which remains at +3 V. The meter voltage is

$$V = V_{K1} - V_{K2} = 4\text{ V} - 3\text{ V} = 1\text{ V}.$$

As in the case of the similar transistor circuit, all of the input voltage to a cathode follower VTVM appears across the meter circuit. The meter multiplier resistor (R_s) can be calculated to give FSD for any desired level of input voltage.

Because no grid current flows, the input resistance of a vacuum tube is extremely high. The maximum attenuator resistance connecting the grid of Q_1 to the zero voltage level in Figure 8-16 is $R_a + R_c + R_d + R_e$ which adds up to 1 MΩ. This (1 MΩ) is a typical maximum resistance used to bias a vacuum triode grid to the zero level (or to any other potential). Like transistors, perfect matching of vacuum tubes is not possible. The grid-cathode voltages of the two tubes may differ slightly when the cathode currents are equal. Potentiometer R_4, together with resistors R_3 and R_5, provides adjustment to take care of such differences.

The circuit in Figure 8-16 offers an input resistance of 10 MΩ to the voltage being measured. The input voltage is potentially divided by the attenuator to a maximum of 1 V on every range. This voltage is then applied to the meter circuit via the cathode followers which can easily supply the required meter current.

8-7-3 Difference Amplifier VTVM Circuit

The difference amplifier VTVM circuit in Figure 8-17 operates in exactly the same way as the similar transistor circuit described in Section 8-5-1. Potentiometer R_3 is a zero control which equalizes the voltage drops across R_{L1} and R_{L2} when the grids of both tubes are at the zero level. R_s is a multiplier resistor in series with the meter, and part of it is adjustable for meter calibration. In this vacuum tube circuit the voltage again from the input to the tube plates is

$$A_v = \frac{\mu R_L}{r_p + R_L}. \tag{8-11}$$

Here, μ is the *amplification factor* for each tube, and r_p is the *plate resistance*. When the triode grid-cathode voltage is changed by ΔV_{GK}, it produces a change in the plate-cathode voltage ΔV_{PK}. The amplification factor is the ratio of these changes: $\mu = \Delta V_{PK}/\Delta V_{GK}$. A change in plate-cathode voltage produces a change in plate current. The ratio of these two is the plate resistance: $r_p = \Delta V_{PK}/\Delta I_P$. Typical values of μ for triodes range from 5 to 100. Typical plate resistances are 250 Ω to 70 kΩ.

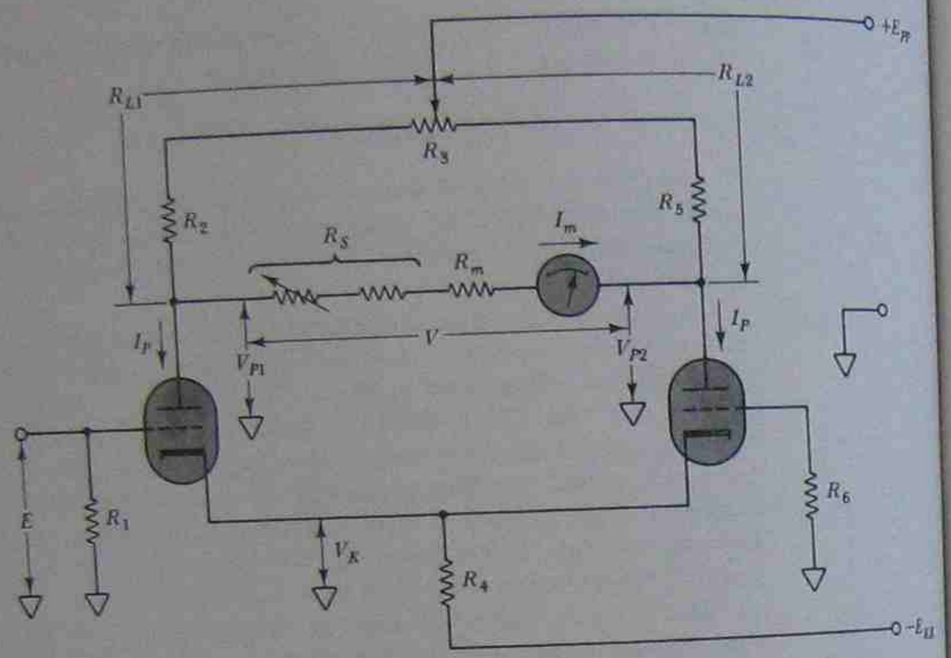


FIGURE 8-17. Difference amplifier VTVM circuit.

EXAMPLE 8-11 A difference amplifier VTVM as in Figure 8-17 has the following components: $R_1 = 1\ \text{M}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_3 = 2\ \text{k}\Omega$, $R_4 = 12\ \text{k}\Omega$, $R_5 = 10\ \text{k}\Omega$, and $R_6 = 1\ \text{M}\Omega$. The supply voltages are $E_{PP} = 100$ V and $E_{KK} = -100$ V. The vacuum tubes have $\mu = 60$ and $r_p = 9\ \text{k}\Omega$, and the meter current is 100 μA at full scale with a coil resistance of 1.7 kΩ. When $E = 0$, the device voltages are measured as $V_{P1} = V_{P2} = 52.8$ V and $V_K = +3$ V. Determine I_{P1}, I_{P2}, and I_K. Also calculate the required resistance of R_s to give FSD when $E = 1$ V.

SOLUTION

$$R_{L1} = R_{L2} = R_2 + \tfrac{1}{2}R_3$$
$$= 10\ \text{k}\Omega + \frac{2\ \text{k}\Omega}{2}$$
$$= 11\ \text{k}\Omega,$$
$$I_{P1} = I_{P2} = \frac{E_{PP} - V_P}{R_L} = \frac{100\ \text{V} - 52.8\ \text{V}}{11\ \text{k}\Omega}$$
$$= 4.3\ \text{mA},$$
$$I_K = \frac{V_K - E_{KK}}{R_4}$$
$$= \frac{3\ \text{V} - (-100\ \text{V})}{12\ \text{k}\Omega}$$
$$= 8.6\ \text{mA},$$

and
$$I_K = I_{P1} + I_{P2}$$
$$= 8.6\ \text{mA}.$$

Equation 8-11,

$$A_v = \frac{\mu R_L}{r_P + R_L}$$
$$= \frac{60 \times 11\ \text{k}\Omega}{9\ \text{k}\Omega + 11\ \text{k}\Omega}$$
$$= 33,$$
$$V = A_v E$$
$$= 33 \times 1\ \text{V}$$
$$= 33\ \text{V},$$
$$R_s + R_m = \frac{V}{I_m} = \frac{33\ \text{V}}{100\ \mu\text{A}}$$
$$= 330\ \text{k}\Omega,$$
$$R_s = 330\ \text{k}\Omega - R_m$$
$$= 330\ \text{k}\Omega - 1.7\ \text{k}\Omega$$
$$= 328.3\ \text{k}\Omega.$$

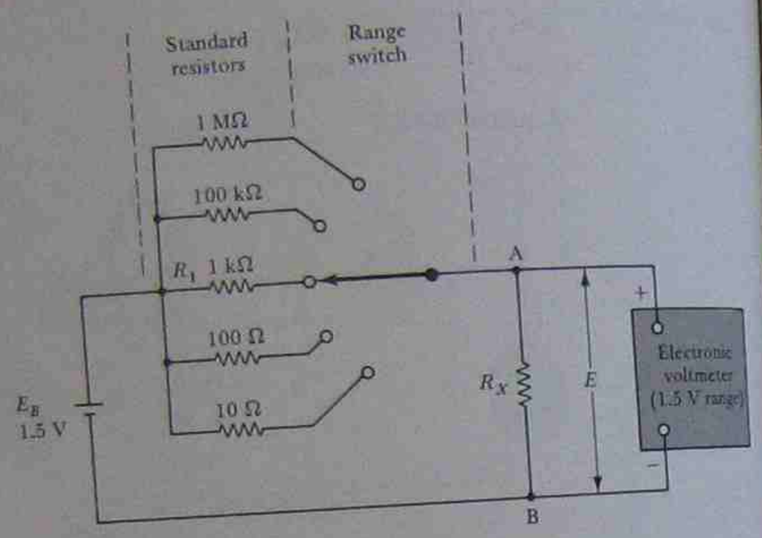
8-8 THE OHMMETER FUNCTION IN ELECTRONIC MULTIMETERS

Since analog electronic instruments contain a moving-coil deflection meter, there is no reason why they cannot be made to function as an ohmmeter in exactly the same way as described in Chapter 3. All that would be required is a battery, several standard resistors, and a suitable switching arrangement. The resistance scale on the instrument would then be exactly the same as for the VOM in Section 3-4, with zero ohms being on the right-hand side and infinity at the left of the scale. This method is not usually employed in electronic instruments. Instead, one of the three systems described below is normally used.

8-8-1 Series Ohmmeter Circuit

The circuit shown in Figure 8-18(a) uses the electronic voltmeter on a 1.5-V range. A 1.5-V battery and several standard resistors are included, as illustrated. The unknown resistance (R_x) is connected across terminals A and B, so that the voltmeter input (E) is the voltage drop across R_x.

Suppose the range switch is set, as shown, to the 1-kΩ standard resistor (R_1). With terminals A and B open-circuited (R_x not connected), the voltmeter should indicate full scale of 1.5 V. Therefore, FSD (right-hand side of the scale) represents $R_x = \infty$ [see Figure 8-18(b)]. If terminals A and B are short-circuited, E becomes zero, and the pointer is at the left-hand side of the scale. Thus, the left-hand side represents $R_x = 0\ \Omega$.



(a) Series ohmmeter circuit for electronic instrument



(b) Ohmmeter scale for electronic instrument

FIGURE 8-18. Series ohmmeter circuit and ohmmeter scale for analog electronic instrument.

Now suppose an unknown resistance greater than zero but less than infinity is connected to terminals A and B. The battery voltage (E_B) is potentially divided across R_1 and R_x, giving

$$E = E_B \frac{R_x}{R_1 + R_x}. \tag{8-12}$$

When $R_x = R_1 = 1\ \text{k}\Omega$

$$E = 1.5\ \text{V} \times \frac{1\ \text{k}\Omega}{1\ \text{k}\Omega + 1\ \text{k}\Omega}$$
$$= 0.75\ \text{V}.$$

So the meter indicates one-half of full scale, and the center of the resistance scale is marked 1. The meter will always indicate half scale when $R_x = R_1$ on whatever range is selected.

EXAMPLE 8-12 For the circuit shown in Figure 8-18, determine the resistance scale markings at $\frac{1}{3}$ and $\frac{2}{3}$ of full scale.

SOLUTION

From Equation 8-12,

$$\frac{E}{E_B} = \frac{R_x}{R_1 + R_x};$$

inverting,

$$\frac{E_B}{E} = \frac{R_1 + R_x}{R_x} = \frac{R_1}{R_x} + 1,$$

or
$$\frac{E_B}{E} - 1 = \frac{R_1}{R_x},$$

giving
$$R_x = \frac{R_1}{\frac{E_B}{E} - 1}.$$

At FSD:

$$E = E_B.$$

At $\frac{1}{3}$ FSD:

$$E = \frac{E_B}{3},$$

$$\text{and } R_x = \frac{R_1}{\left[\frac{E_B \times 3}{E_B} - 1\right]}$$
$$= \frac{R_1}{2}$$
$$= 0.5\,R_1.$$

At $\frac{1}{2}$ FSD:

$$E = \tfrac{1}{2}E_g,$$

$$\text{and } R_x = \frac{R_1}{\left[\dfrac{E_g \times 3}{2E_g} - 1\right]}$$

$$= \frac{R_1}{0.5}$$

$$= 2R_1.$$

The two points calculated in Example 8-12 are shown on the resistance scale in Figure 8-18(b). Further calculations demonstrate that the scale becomes progressively cramped at both extremeties. Thus, as in the case of the nonelectronic ohmmeter, this instrument measures resistance most accurately when indicating close to half-scale deflection.

The above discussion assumes that the electronic voltmeter is operating on its 1.5-V range, and that the battery voltage (E_g) is precisely 1.5 V. A battery voltage slightly larger or slightly smaller than this is easily taken care of by adjusting the meter series (calibrating) resistance (R_1) [see Figure 8-12, for example]. If $E_g = 1.4$ V, R_1 is adjusted to give FSD for 1.4 V when terminals A and B are open-circuited. Then when $R_x = R_1$, $E = \frac{1}{2}E_g$, as before, and the pointer once again indicates half scale. All points on the scale are correct once the meter has been adjusted for full scale with terminal A and B *open-circuited*.

It should be noted that the resistance measuring system described above requires two adjustments before use. First, the voltmeter must be zeroed electrically when the terminals are short-circuited. After that, the calibration control must be adjusted to give FSD when the terminals are open-circuited. The unknown resistance can be measured only after both adjustments have been made.

8-8-2 Shunt Ohmmeter Circuit

A *shunt-type ohmmeter* circuit for use with an electronic instrument is illustrated in Figure 8-19. In this case a regulated power supply (see Chapter 14) is used to provide a stable 6-V supply, instead of employing a battery. This eliminates the need to adjust the voltmeter calibrating control, because, unlike a battery, the regulated power supply voltage does not drop with use.

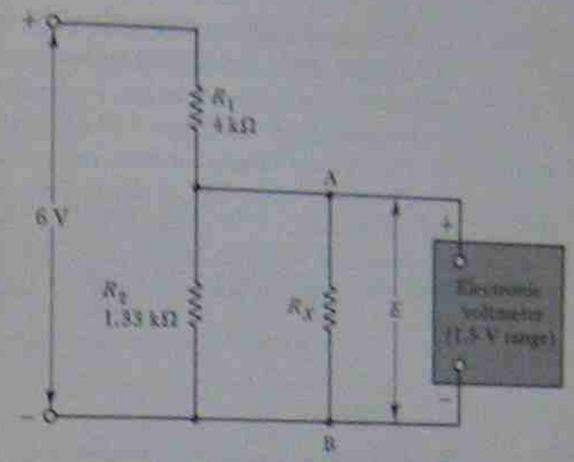


FIGURE 8-19. Shunt ohmmeter circuit for electronic instrument.

With terminals A and B in Figure 8-19 open-circuited, $R_x = \infty$ and

$$E = E_g \frac{R_2}{R_1 + R_2}$$

$$= 6\text{ V} \times \frac{1.33\text{ k}\Omega}{4\text{ k}\Omega + 1.33\text{ k}\Omega}$$

$$= 1.5\text{ V}.$$

Therefore, in this circuit the voltmeter is once again on a 1.5-V range to give FSD when $R_x = \infty$.

When $R_x = 0\ \Omega$ (A and B short-circuited), $E = 0$ V. Here again the pointer is at the left-hand side for $R_x = 0\ \Omega$.

At any value of R_x:

$$\boxed{E = E_g \frac{R_2 \| R_x}{R_1 + R_2 \| R_x}.} \qquad (8\text{-}13)$$

For $R_x = 1\text{ k}\Omega$

$$E = 6\text{ V} \times \frac{1\text{ k}\Omega \| 1.33\text{ k}\Omega}{4\text{ k}\Omega + (1\text{ k}\Omega \| 1.33\text{ k}\Omega)}$$

$$= 0.75\text{ V}.$$

This is one-half of FSD. Now note that

$$R_1 \| R_2 = 4\text{ k}\Omega \| 1.33\text{ k}\Omega$$

$$= 1\text{ k}\Omega.$$

The meter indicates half scale when $R_x = R_1 \| R_2$. The values of R_1 and R_2 used above obviously gives the instrument a 1-kΩ range. Resistance values ten times larger would give a 10-kΩ range. Similarly, resistances ten times smaller (than 4 kΩ and 1.33 kΩ) give a 100-Ω range. The scale on the instrument is exactly the same as that in Figure 8-18(b).

The major advantage of this system over the series ohmmeter previously described is that (because of the stable supply voltage) only one adjustment is required before resistance measurements are made. The ohmmeter terminals are short-circuited, and the instrument is electrically zeroed.

8-8-3 Linear Ohmmeter

In the circuit of Figure 8-20, transistor Q_1 together with resistors R_1, R_2, and R_E operates as a *constant current circuit*. Resistors R_1 and R_2 potentially divide the supply voltage to give 5.7 V across R_1. When applied to the base of *pnp* transistor Q_1, this gives 5.7 V $- V_{BE} = 5$ V across resistor R_E. So the current I_E is 5 V/R_E, and this is a constant quantity. Since $I_C = I_E$ the collector current is also a constant quantity. This constant current is passed through the unknown resistance R_x, and the voltage across R_x is measured by the voltmeter. The voltmeter scale can now be multiplied by an appropriate factor and used directly as a resistance scale.

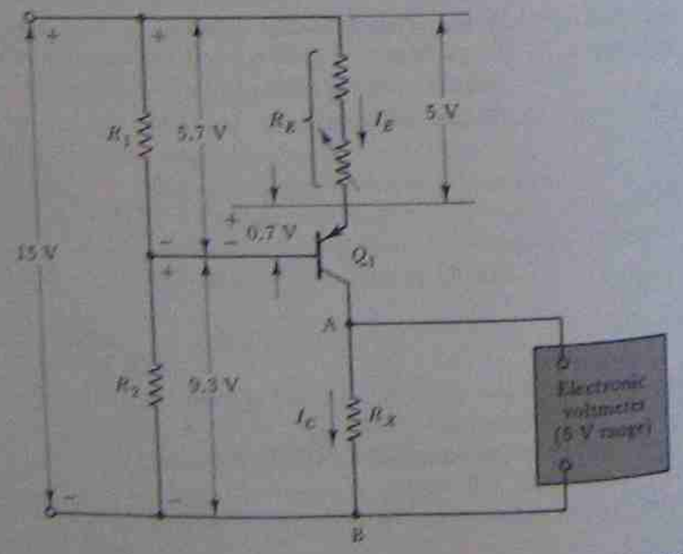


FIGURE 8-20. Linear ohmmeter circuit for use with electronic instruments.

Suppose R_E is adjusted to give a collector current of exactly 1 mA. If the voltmeter indicates exactly 5 V, then

$$R_x = \frac{5\text{ V}}{1\text{ mA}} = 5\text{ k}\Omega.$$

When the voltmeter indicates 3 V, R_x is exactly 3 kΩ. Thus, the 0- to 5-V scale is a *linear* 0- to 5-kΩ resistance scale.

Another standard resistor substituted in place of R_E can reduce I_C to 100 μA, or increase it to 10 mA. When $I_C = 100$ μA, the maximum resistance measurable on the 5-V range is now

$$R_x = \frac{5\text{ V}}{100\ \mu\text{A}} = 50\text{ k}\Omega.$$

With $I_C = 10$ mA, the maximum value of R_x becomes 500 Ω.

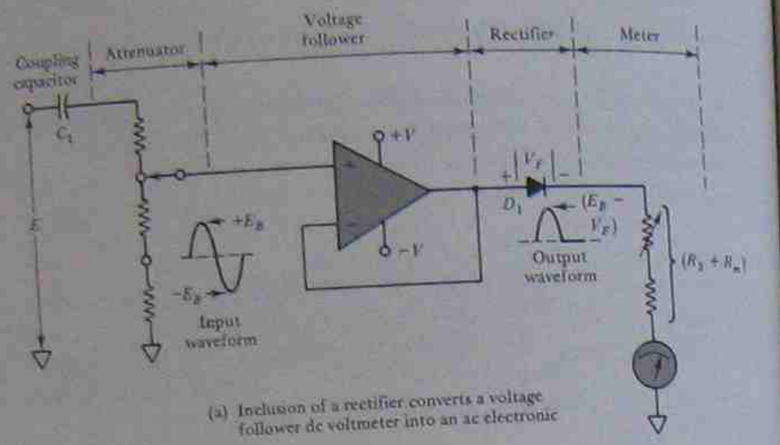
For multirange operations, a switching arrangement must be provided for selection of R_E from several standard resistor values. Some series adjustment for calibration of each range is necessary. Calibration is easily effected by connecting a known standard resistor in place of R_x and adjusting R_E for the appropriate deflection.

8-9 ac ELECTRONIC VOLTMETERS

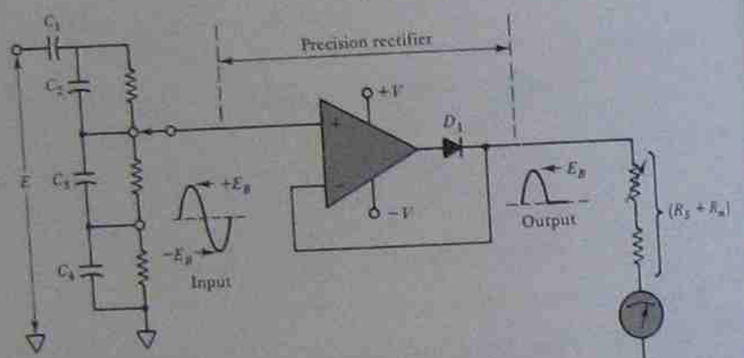
8-9-1 Rectifier Voltmeter Circuits

The IC op-amp voltage follower voltmeter described in Section 8-6-2 is a dc instrument. Connecting a rectifier in series with the meter circuit of this instrument, as shown in Figure 8-21(a), converts it into a half-wave rectifier voltmeter. The output from the voltage follower is exactly the same as the input. So the voltage fed to the meter circuit is simply a half-wave rectified version of the input voltage E_s from the attenuator. The operation of this circuit and the design calculations are just as described in Section 2-3-3 for the nonelectronic half-wave rectifier voltmeter. The difference between the nonelectronic instrument and the electronic ac voltmeter circuit in Figure 8-21(a) is, of course, that the electronic instrument has a very high input impedance. Note the coupling capacitor (C_1) in Figure 8-21(a). This is usually provided at the input of an ac voltmeter to block unwanted dc voltages.

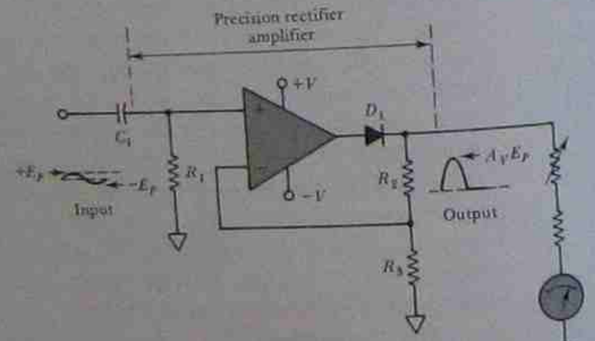
The voltage drop (V_F) across the rectifier is a source of error in the circuit in Figure 8-21(a). V_F can be taken into account in design calculations when the instrument is indicating full scale. However, at other points on the scale an error occurs due to V_F. Also, the rectifier voltage drop is not always exactly 0.7 V, as usually assumed for a silicon diode, and it varies with temperature change. To avoid these errors, the voltage follower feedback connection to the inverting terminal is taken from the cathode of rectifier D_1 instead of from the amplifier output [see Figure 8-21(b)]. The



(a) Inclusion of a rectifier converts a voltage follower dc voltmeter into an ac electronic



(b) Use of a precision rectifier improves the accuracy of the ac electronic voltmeter.



(c) An amplifier with rectifiers amplifies and rectifies low level ac voltages prior to measurement.

FIGURE 8-21. Half-wave rectifier circuits for use with ac electronic voltmeters.

result is that the half-wave rectified output precisely follows the positive half cycle of the input voltage. There is *no* rectifier voltage drop from input to output. This is because, in the operational amplifier voltage follower, the inverting terminal follows the input to the noninverting terminal. With the inverting terminal connected to D_1 cathode, the potential at this point always follows the potential at the input while D_1 is forward biased.

The procedure for calculation of series resistance R_S for this circuit is just as explained in Section 2-3-4, with one exception. No diode voltage drop is involved. Note that capacitors C_2, C_3, and C_4 are connected across the attenuator resistors in Figure 8-21(b). These are normally employed with the attenuators on ac electronic voltmeters in order to compensate for the input capacitance of the amplifier. This input capacitance problem also occurs with oscilloscopes. Compensation capacitors are further discussed in Section 11-9-2.

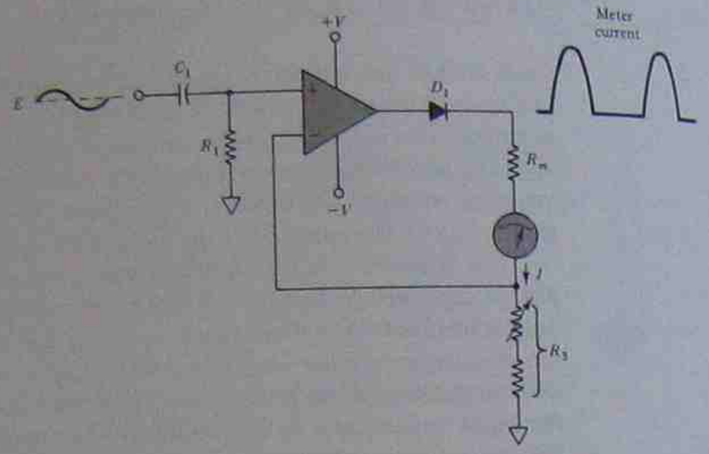
Low-level ac voltages should be accurately amplified before being rectified and applied to a meter circuit. Amplification is combined with half-wave rectification in the circuit shown in Figure 8-21(c). When the diode is omitted the op-amp circuit is a noninverting amplifier, as described in Section 8-6-3. Inclusion of D_1 causes the positive half cycles of the input to be amplified by a factor $A_v = (R_2 + R_3)/R_3$. The amplification is precise and here again there is no rectifier voltage drop involved.

The procedure for calculating the meter series resistance in the circuit in Figure 8-21(c) is the same as described in section 2-3-3. However, in this case the peak voltage applied to the meter and its series resistance is $A_v E_p$, and again the rectifier voltage drop does not enter into the calculations.

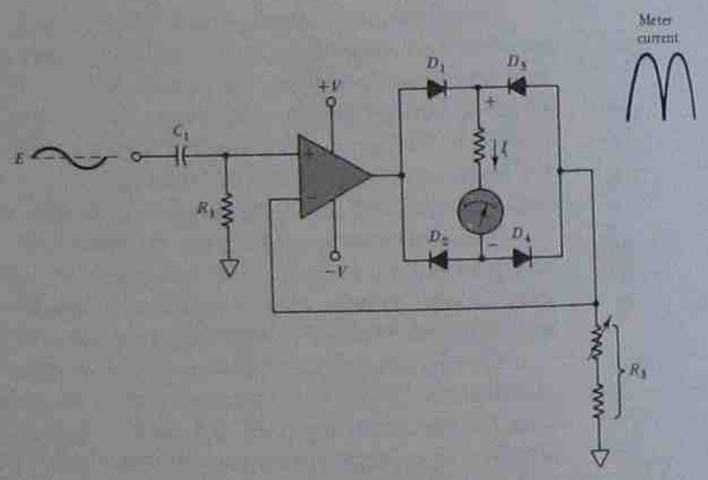
The circuit in Figure 8-22(a) is a *voltage-to-current converter* with half-wave rectification. The circuit functions exactly as explained in Section 8-6-4, with the exception that only the positive half-cycles of the ac input are effective in passing current through the meter. During the negative half cycle, the diode is reverse biased and no current flows through the meter or through resistor R_3. The meter peak current is $I_p = E_p/R_3$, and the average meter current is $I_{av} = \frac{1}{2}(0.637\, I_p)$.

A full-wave bridge rectifier is employed in the circuit of Figure 8-22(b). When the input voltage is positive, the operational amplifier output is positive. Diodes D_1 and D_4 are forward biased so that current flows through the meter from top (+) to bottom (−). When the input is negative, D_2 and D_3 are forward biased. Once again current passes through the meter from the + to the − terminal. Whether the input is positive or negative, the meter peak current is again limited to $I_p = E_p/R_3$. The average meter current in the full-wave rectifier circuit is $I_{av} = 0.637\, I_p$.

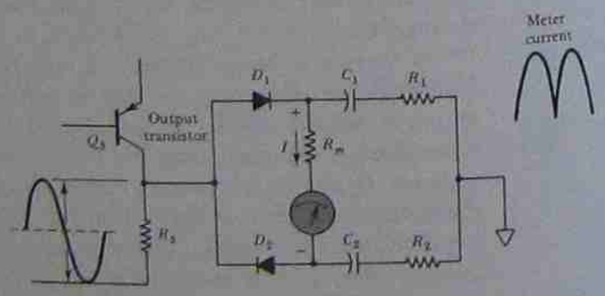
Instead of a full-wave bridge rectifier, some electronic instruments use the half-bridge full-wave circuit in Figure 2-13(b). As explained in Section 2-3-5, this arrangement helps to correct for differences in the diodes. However, the circuit in Figure 8-22(b) tends to be unaffected by diode



(a) Voltage-to-current converter with half-wave rectifier



(b) Voltage-to-current converter with full-wave rectification



(c) Half-bridge full-wave rectifier circuit with dc blocking capacitors

FIGURE 8-22. Electronic analog ac voltmeters using half-wave and full-wave rectification.

differences, because the meter current is stabilized by the amplifier feedback circuitry. So the half-bridge circuit would not improve the performance of an IC op-amp voltage-to-current converter type of voltmeter. A half-bridge rectifier could be useful in an electronic voltmeter that uses a transistor amplifier.

Figure 8-22(c) shows a half-bridge rectifier circuit connected to the output stage of a transistor amplifier. Output transistor Q_3 passes direct current through resistor R_5, producing a dc voltage at the collector of the transistor which might be above or below the zero voltage level. Capacitors C_1 and C_2 block the direct current from the meter circuit and pass the alternating current when an ac voltage appears at the amplifier output. The circuit then functions exactly as described in Section 2-3-5.

EXAMPLE 8-13 The half-wave rectifier electronic voltmeter circuit in Figure 8-22(a) uses a meter with a FSD current of 1 mA. The meter coil resistance is 1.2 kΩ. Calculate the value of R_3 which will give meter full-scale pointer deflection when the ac input voltage is 100 mV (rms). Also determine the meter deflection when the input is 50 mV.

SOLUTION

For FSD, *the average meter current is:*

$$I_{av} = 1 \text{ mA}.$$

With half-wave rectification,

$$I_{av} = \frac{0.637}{2} I_p,$$

or

$$I_p = \frac{2}{0.637} I_{av}$$

$$= \frac{2}{0.637} \times 1 \text{ mA}$$

$$= 3.14 \text{ mA}.$$

Peak value of E_{R3} = input peak voltage:

$$E_p = \frac{E}{0.707} = \frac{100 \text{ mV}}{0.707}$$

$$= 141.4 \text{ mV},$$

$$R_3 = \frac{E_p}{I_p} = \frac{141.4 \text{ mV}}{3.14 \text{ mA}}$$

$$= 45 \Omega.$$

When $E = 50$ mV:

$$E_p = \frac{50 \text{ mV}}{0.707}$$
$$= 70.7 \text{ mV},$$
$$I_p = \frac{70.7 \text{ mV}}{45\ \Omega}$$
$$= 1.57 \text{ mA},$$
$$I_{av} = \frac{0.637}{2} \times 1.57 \text{ mA}$$
$$= 0.5 \text{ mA (half scale)}.$$

8-9-2 Peak Response Voltmeter

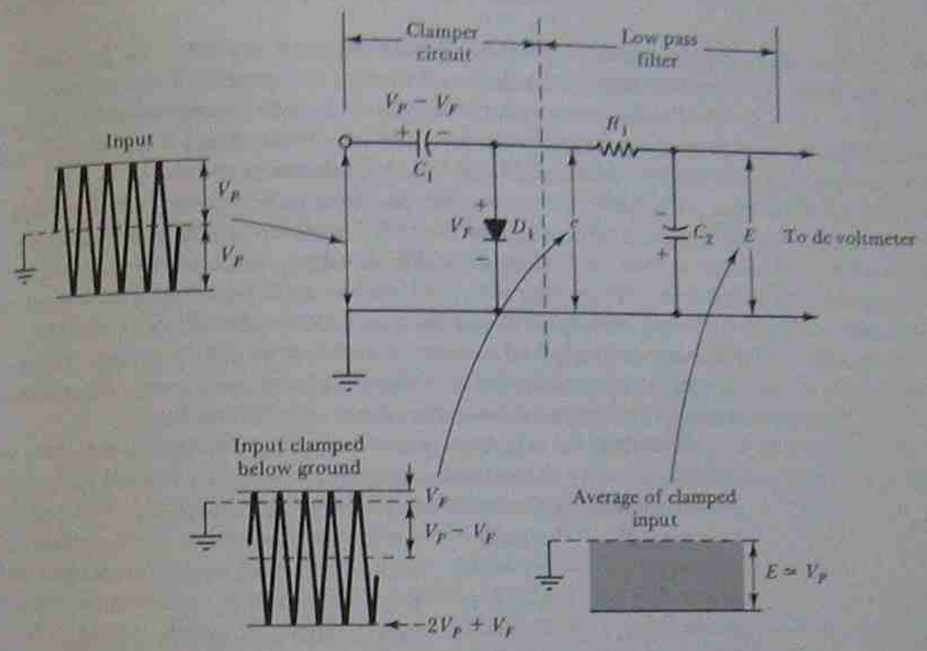
The rectifier voltmeter circuits discussed in Section 8-9-1 respond to the average value of the rectified waveform. This applies also to those described in Section 2-3. In every case, of course, the instruments are calibrated to indicate rms voltages. Instead of passing the rectified waveform directly to the deflection meter, it is possible to detect the peak level of the input and apply this as a constant voltage to the meter. Figure 8-23(a) shows a *peak detector circuit*, as used with a *peak response voltmeter*.

Capacitor C_1 in series with the input terminal [in Figure 8-23(a)] blocks dc input voltages and passes the ac voltage. When the input goes to its positive peak level, D_1 is forward biased and C_1 charges up to $V_p - V_F$ with the polarity shown. (The voltage developed across D_1 obviously cannot go above the level of $+V_F$ with respect to ground.) C_1 retains its charge, and when the input voltage goes negative diode D_1 is reverse biased. At the negative peak of the input, the voltage at the anode of D_1 is the sum of the input and the capacitor voltages:

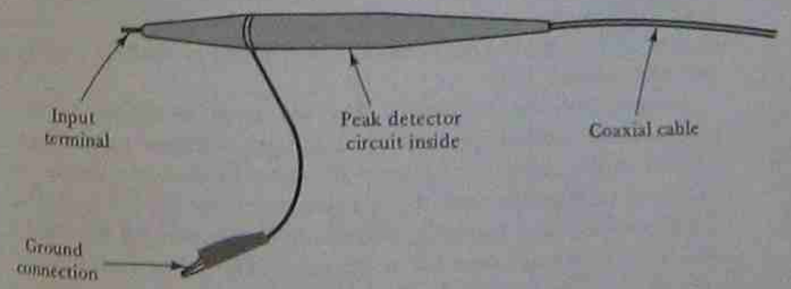
$$e = -V_p - V_{C1}$$
$$= -V_p - (V_p - V_F)$$
$$\simeq -2V_p + V_F.$$

The alternating voltage developed across the diode has exactly the same waveform and amplitude as the input. The important difference is that the positive peak of the waveform is now *clamped* to $+V_F$ above ground level [see the waveforms in Figure 8-23(a)]. Capacitor C_1 and diode D_1 constitute a *clamping circuit*.

The alternating voltage passed to R_1 and C_2 is the same as the input except that any dc input voltage is blocked and the ac wave is virtually all below ground level. Neglecting the diode voltage drop, this wave now has a (negative) average value of approximately one-half its peak-to-peak



(a) Peak detector circuit converts high frequency voltage into dc peak-equivalent level for measurement



(b) Peak detector probe

FIGURE 8-23. Peak detector circuit and probe used with a peak response voltmeter.

voltage, (see illustration). Resistor R_1 and capacitor C_2 function as a low-pass filter to block the alternating component of the voltage and to pass the dc (average) level. The dc level which is (approximately) the peak value of the input (one-half the peak-to-peak voltage) is now passed to a dc voltmeter which is calibrated to indicate rms quantities.

The peak detector circuitry obviously passes a constant voltage level to the voltmeter, rather than a rectified waveform. This is not significant at low or medium frequencies within the upper and lower frequency limits of the moving-coil instrument. However, at high frequencies beyond the frequency range of the deflection instrument, the peak detector still functions correctly and produces a measurable output voltage. Therefore, the *peak response voltmeter* is a high-frequency instrument. Its maximum frequency of measurement generally exceeds 500 MHz.

Electronic ac voltmeters which use peak detection always have the detector circuitry in a separate *probe* on one end of a coaxial cable which plugs in to the voltmeter terminals [see Figure 8-23(b)]. This puts the detector right at the point of measurement, instead of at the opposite end of connecting cables which might have considerable capacitance and inductance. Such cable capacitance and inductance (prior to the detector) could have a serious effect on the circuit in which voltage is being measured. With the high frequency voltage converted to a direct quantity, the connecting cable impedance is no longer of any consequence.

Any dc electronic voltmeter can be made to operate as a high-frequency peak response instrument by use of a suitable peak detector probe. The output of the peak detector must be potentially divided to 0.707 of the peak level to give an rms indication on the dc meter. As in the case of rectifier voltmeters, the peak response instrument is accurate only for pure sine wave inputs.

Some electronic voltmeters that use peak detection circuitry are calibrated to indicate peak or peak-to-peak voltages rather than rms. Instead of the circuit in Figure 8-23, some instruments simply employ full-wave rectification with a capacitor connected at the output of the bridge rectifier. The capacitor charges up to the peak of the input wave and holds its voltage constant at this level. The meter then indicates the peak value of the measured voltage.

8-9-3 True rms Voltmeter

Peak-response instruments and all rectifier voltmeters operate satisfactorily only when measuring inputs which have purely sinusoidal waveforms. The meter current is proportional to either the peak value of the input voltage or the average value of the rectified waveform. Each meter scale is calibrated to indicate rms values on the assumption that the input is a pure sine wave. Where the waveform of the input is not sinusoidal, peak- and

average-response instruments do *not* indicate the true rms value of the measured voltage. In fact, such instruments are virtually useless for measuring voltages with nonsinusoidal waveforms.

In Section 2-7 it is explained that the output voltage from a thermocouple is directly proportional to the rms value of the current through its heater, no matter what the waveform of the heater current. In Figure 8-24, a voltage E with a nonsinusoidal waveform is amplified to $A_v E$, by means of *video amplifier* A_1. A video amplifier operates over a wide frequency range from audio to very high frequencies. Therefore, the input waveform is faithfully reproduced in the amplified output. The amplifier also has a high input impedance to avoid loading the source of the voltage to be measured. The current passed from A_1 to resistor R_1 has the same waveform as the input voltage. Consequently, the heat generated in R_1 is directly proportional to the rms value of the voltage to be measured. Since R_1 is the heater for thermocouple T_1, the output voltage e_1 (from T_1) is also directly proportional to the rms value of input E.

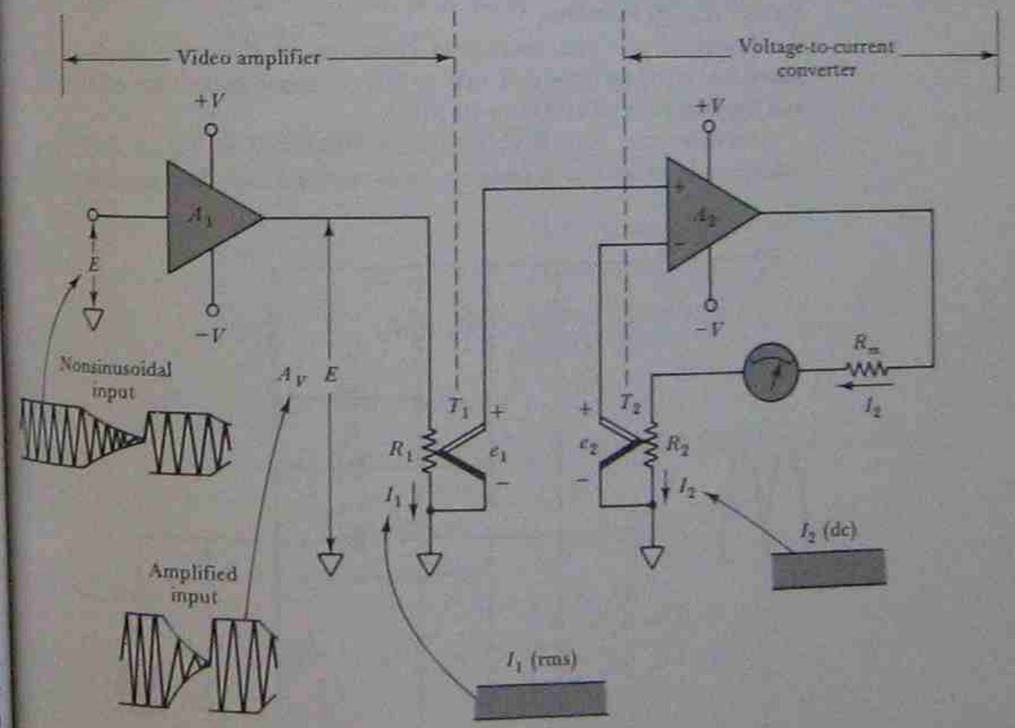


FIGURE 8-24. Basic circuit and waveforms for a true rms electronic voltmeter using thermocouples.

Recall from the descriptions of the voltage follower and the noninverting amplifier, that in each case the feedback from the output provides a voltage at the op-amp inverting terminal which equals that at the noninverting terminal. Now look at operational amplifier A_2 in Figure 8-24. A_2 functions as a voltage-to-current converter which passes an output current I_2 through a deflection meter and through resistor R_2. R_2 is the heater for thermocouple T_2, and the output of T_2 is voltage e_2 which is directly proportional to the heating effect of I_2.

The input to the metering stage is voltage e_1 derived from thermocouple T_1, and the fed-back voltage is e_2 from thermocouple T_2. The output current of A_2 settles down at a level which makes e_2 exactly equal to e_1. If e_2 exceeds e_1, the output of A_2 falls, I_2 is reduced, and, consequently, e_2 becomes smaller. If e_2 is less than e_1, A_2 output increases, increasing I_2 until its heating effect raises e_2 to the same level as e_1. Thus, if the thermocouples are similar devices, the heating effect of current I_2 must be equal to the heating effect of I_1. This means that the direct current I_2 indicated on the meter is equal to the rms value of I_1. Since I_1 is directly proportional to the rms value of input E, the instrument measures the rms value of E no matter what its waveform.

A typical true rms instrument operating on the principle described above has a *voltage range* of 1 mV to 300 V, input impedance of 10 MΩ, and *frequency range* of 10 Hz to 10 MHz.

Another type of true rms meter is illustrated in Figure 8-25. The voltage to be measured is first full-wave rectified, and then applied to the

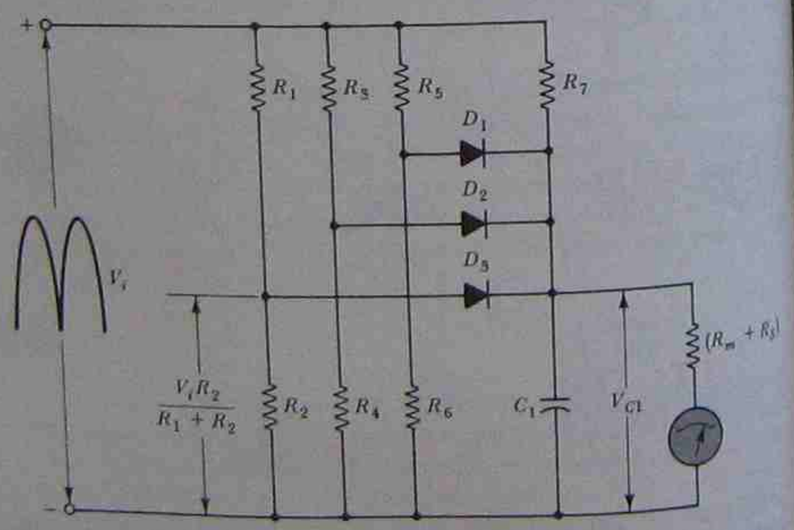


FIGURE 8-25. True rms meter using diode-resistor nonlinear circuit.

input of the diode-resistor circuit shown. At the circuit output the voltage across capacitor C_1 is applied to the meter. When the (rectified) input is low, current flows through all three diodes, and through resistor R_7, to charge C_1. But the voltage applied at the anode of D_3 is V_i potentially divided across R_2 and R_1, and when V_{C1} becomes large enough D_3 is reverse biased. Similarly, D_2 and D_1 become reverse biased in turn as V_{C1} grows. The result of this action is that C_1 is charged in a nonlinear fashion. By suitable selection of resistors, the capacitor voltage can be made proportional to the rms value of many common distorted waveforms. This kind of rms measuring circuit cannot be expected to be as accurate as thermocouples on all waveforms. The manufacturer of one instrument that uses this type of nonlinear circuit for rms measurements states that the probable error is only ±2% on most common waveforms.

EXAMPLE 8-14 Alternating voltages are measured by three electronic voltmeters connected in parallel: a full-wave rectifier instrument, a peak response instrument, and a true rms voltmeter. Determine the indicated voltage on each for the following inputs: (a) A 30-V peak-to-peak sine wave and (b) a positive pulse wave with peak value = 30 V, pulse width (PW) = 1 ms, and time period (T) = 10 ms.

SOLUTION

a. *30-V peak-to-peak sine wave:*

Full-wave rectifier instrument

$$V = 1.11 \times V_{av} \text{ of rectified wave}$$
$$= 1.11 \times 0.637 \times V_p$$
$$= 1.11 \times 0.637 \times 15 \text{ V}$$
$$= 10.6 \text{ V}.$$

Peak response instrument

$$V = -0.707 \text{ of } V_{av} \text{ of entire wave shifted below ground}$$
$$= -0.707 \text{ of } -15 \text{ V}$$
$$= 10.6 \text{ V}.$$

True rms *instrument*

$$V = 0.707 \text{ of } V_p$$
$$= 0.707 \times 15 \text{ V}$$
$$= 10.6 \text{ V}.$$

b. *30-V pulse with PW = 1* ms *and T = 10* ms

full-wave rectifier instrument

Because of the coupling capacitor, the zero level of the waveform is moved up to its average value before rectification [see Figure 8-26(a)]

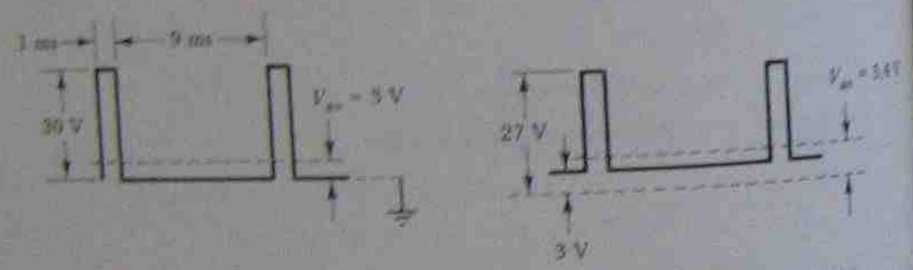
$$V_{av} = \frac{30 \times 1 \text{ ms}}{10 \text{ ms}} = 3 \text{ V}.$$

When rectified the wave is a 27-V positive pulse with $PW = 1$ ms followed by a positive 3-V pulse with $PW = 9$ ms [see Figure 8-26(b)].

$$V_{av} = \frac{(27 \text{ V} \times 1 \text{ ms}) + (3 \text{ V} \times 9 \text{ ms})}{10 \text{ ms}}$$
$$= 5.4 \text{ V}$$
$$V = 1.11 \times 5.4 \text{ V}$$
$$\approx 6 \text{ V}.$$

peak response instrument
$V = 0.707$ of V_{av} of entire wave shifted below ground [see Figure 8-26(c)].

$$V = 0.707 \text{ of} \left(\frac{30 \times 9 \text{ ms}}{10 \text{ ms}} \right) \approx 19.1 \text{ V}.$$



(a) Average of a positive pulse wave is a positive quantity

(b) Same pulse wave as in (a) after capacitive coupling and full-wave rectification in rectifier voltmeter



(c) Same pulse wave as in (a) after the clamping circuit in a peak response voltmeter

FIGURE 8-26. Effects of rectifier voltmeter and peak response voltmeter upon positive pulse waveform.

true rms instrument

$$V = \sqrt{(30)^2(1/10)} = 9.5 \text{ V}.$$

Example 8-14 clearly demonstrates that measurements of nonsinusoidal waveforms should be made only on true rms voltmeters.

8-10 CURRENT MEASUREMENT WITH ANALOG ELECTRONIC INSTRUMENTS

Recall that the two reasons for introducing electronic devices into voltmeters are: (1) to produce a very high input resistance and (2) to amplify very small voltages to measurable levels. Item (1) does not apply in the case of current measurement. On the contrary, ammeters should normally have the lowest possible resistance. Item (2) can apply in the case of very low current levels.

The basic circuit of an analog electronic ammeter for measurement of very low currents is shown in Figure 8-27. The small voltage drop across shunt resistor R_s is amplified before being applied to the deflection instrument. This approach is just as applicable to the measurement of low-level alternating currents as it is to direct current measurements. For alternating currents, an ac electronic voltmeter using rectifiers or thermocouples (see Section 8-9) is used instead of a dc instrument.

For medium or high current measurements there is no need to use electronic amplifiers. In fact, any electronic voltmeter could have several current measurement ranges, if appropriate shunts and rectifiers are included, as explained in Sections 2-1 and 2-4. The deflection instrument would be involved, but the electronic circuitry could be switched-out.

Since there is no advantage to using an electronic device in medium or high current measurements, many electronic multirange instruments do not have any current measurement function. Those that measure currents generally have very low-level current ranges. Such instruments also tend to have relatively high resistances when operating as electronic ammeters. For example, one typical instrument has several direct current ranges from 1.5 μA full scale to 150 mA full scale. On the 1.5 μA range the resistance of the instrument is 9 kΩ. This decreases progressively to 300 Ω on the 150-mA range. These resistances are very high by comparison with ammeter resistances discussed in Section 2-1. Such high resistance values must be taken into account when an electronic ammeter is connected in series with a circuit in which current is to be measured. Many low current circuits would not be affected by the high instrument resistance. For example, a circuit which draws a current of 1 μA from a 10-V supply would have a resistance of 10 V/1 μA = 10 MΩ. Clearly, the 9-kΩ instrument resistance would not alter the current significantly. On the other hand, an additional 300 Ω could seriously alter the current level in a circuit normally passing 10 mA from a 10-V supply.

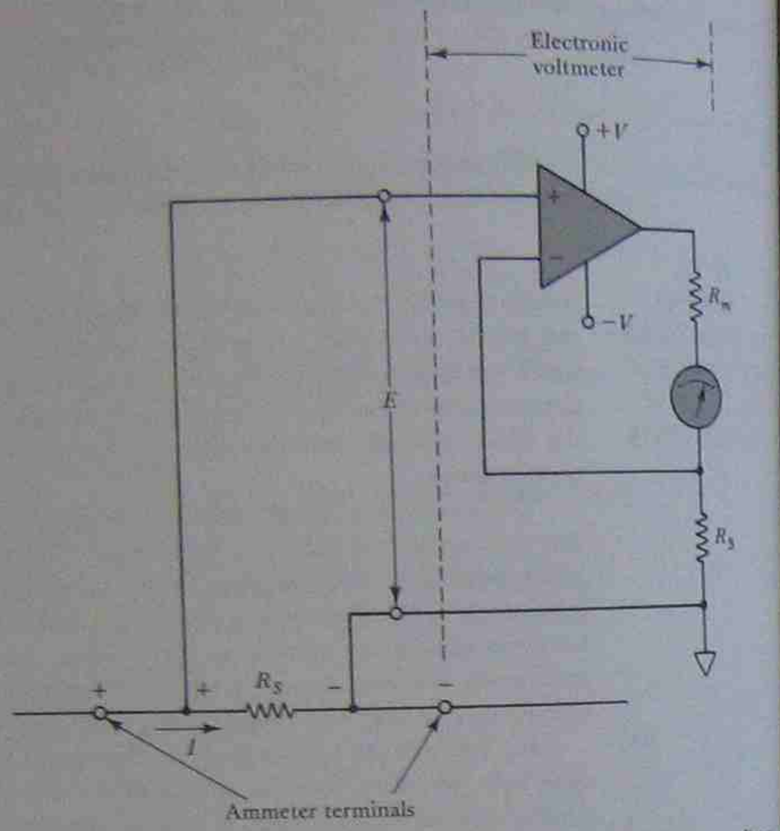


FIGURE 8-27. An electronic voltmeter connected to measure the voltage drop across a shunt resistor (R_s) functions as an ammeter.

8-11 ELECTRONIC GALVANOMETERS

An *electronic galvanometer* is simply a low-level electronic voltmeter or ammeter equipped with a center-zero scale so that it may be used as a null detector. Most of the electronic voltmeter and ammeter circuits already discussed could be used in electronic galvanometers; however, they may not give great enough sensitivity for some galvanometer applications. When the instrument is to detect *picoamp* (pA) levels, devices which require input currents in the *microamp* or *nanoamp* range must be avoided. Consequently, amplifier input devices for electronic galvanometers should be FETs or vacuum tubes.

A problem that occurs when amplifying very low voltage levels with the kinds of circuits already discussed is that small drifts in bias conditions within the circuits have the same effect as changes in input voltage. They are amplified and produce serious errors in measurements at the circuit output. If the direct voltages to be measured could be amplified by

capacitor coupled amplifiers, the problem could be eliminated, or at least minimized. Capacitor coupling at input and output, and between the stages of an amplifier, passes alternating voltage signals but blocks direct voltages. The capacitors also block dc drift voltages. A *chopper stabilized* or *modulated* dc amplifier, as used in the most sensitive electronic galvanometers, actually amplifies dc voltages by means of an ac amplifier.

The diagram in Figure 8-28 illustrates the operating system of a chopper stabilized electronic galvanometer. The input stage may be a voltage follower circuit for high input resistance. The low-level dc voltage to be measured is passed from the voltage follower to a switching circuit controlled by an oscillator operating at a constant frequency. The switching circuit opens and closes, alternately blocking and passing the voltage to be measured. This results in a pulse waveform, or *chopped dc voltage*, as illustrated.

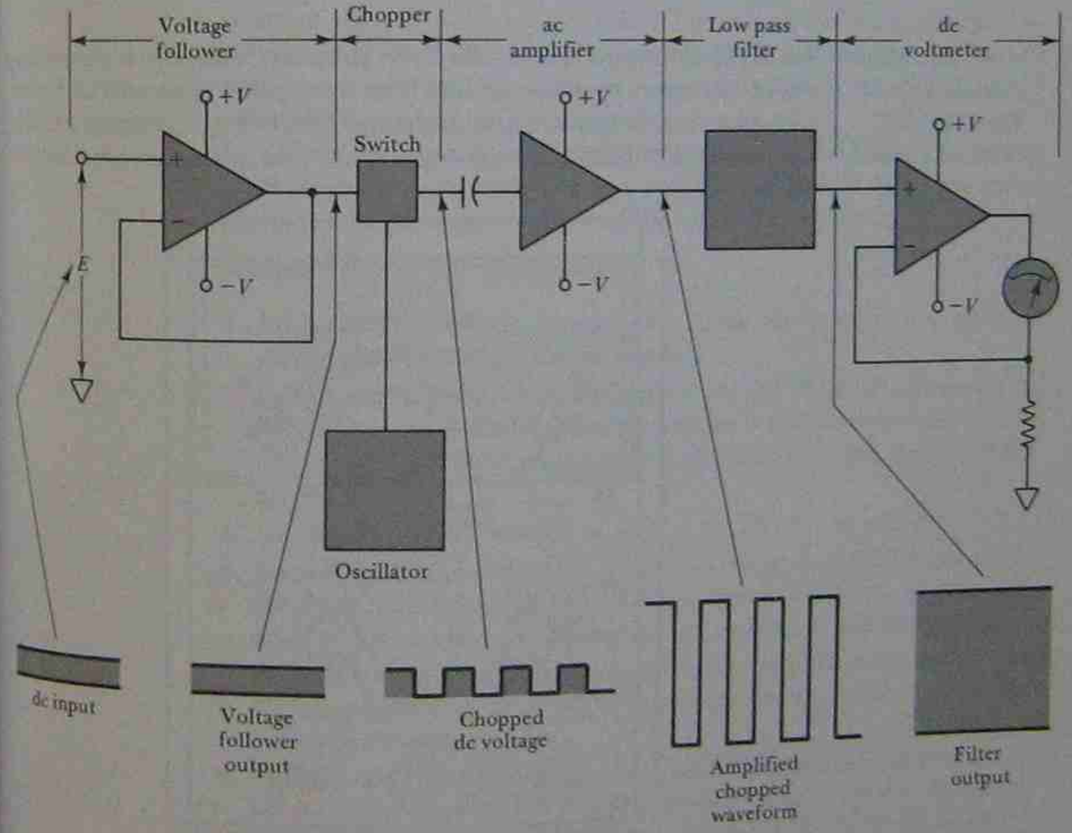


FIGURE 8-28. Chopper stabilized system for measuring low-level dc voltages.

Since the chopped dc voltage is an alternating quantity, it is passed by the coupling capacitor and amplified by the ac amplifier. Once amplified, the waveform is passed through a *low-pass filter*. This allows dc and low-frequency ac voltages to get through, but severely attenuates ac quantities which have the same frequency as the *chopping oscillator*. The amplified ac waveform is made up of a dc voltage (amplified V_i) and an ac (chopping frequency) component. The dc voltage is passed by the low-pass filter and the ac quantity is blocked. After filtering, the amplified dc voltage is fed to the measuring stage, where it produces pointer deflection.

The kind of instrument described above is essentially a low-level voltmeter. With suitable input resistors it can also function as a low-level ammeter. A typical center-zero electronic galvanometer might have a voltage sensitivity of 10 μV/scale division (for perhaps 2-mm divisions). If the input resistance is 10 MΩ, this translates into a current sensitivity of 1 pA/scale division.

8-12 MULTIRANGE ANALOG ELECTRONIC VOLTMETER

The Hewlett-Packard (HP) model 427A electronic voltmeter is representative of laboratory type instruments. The front panel illustrated in Figure 8-29 shows that it can measure dc voltage (*DCV* ±), ac voltage (*ACV*), and resistance (*OHMS*). A knife-edge pointer and mirror are provided for

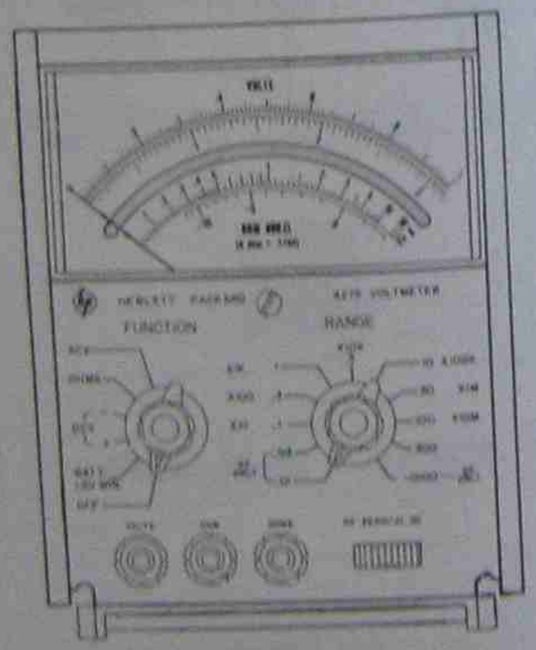


FIGURE 8-29. Front panel of the Hewlett-Packard Model 427A electronic voltmeter (Courtesy of Hewlett-Packard).

precise reading on two voltage scales: 0 to 1 and 0 to 3. The ohmmeter scale has its 1 position at the scale center, as in Figure 8-18(b). A decibel scale (DBM) is also provided. Voltage measurements are made using the VOLTS and COM (common) terminals. For resistance measurements, the COM and OHMS terminals are employed. An electrical zero control (DC ZERO/Ω∞) is included on the front panel, as well as a mechanical zero control for the pointer.

The HP 427A has nine dc voltage ranges, from 0.1 V (full scale) to 1000 V. The ±DCV positions on the FUNCTION SWITCH permits either positive or negative polarity voltages to be measured. The measurement accuracy is ±2% of full scale, and the input resistance is 10 MΩ on all ranges. There are ten ac voltage ranges, the lowest being 10 mV, and the highest 300 V. The frequency range for ac voltage measurements is 10 Hz to 1 MHz. This can be extended by the use of a high-frequency probe which has a peak detector circuit. The available probe is designed for use with voltages ranging from 0.25 to 30 V, and it extends the frequency range of the HP 427A to 500 MHz. The measurement accuracy for ac voltages is ±2% of full scale. However, the input impedance is stated as *10 MΩ shunted by a 40-pF capacitance* on ranges up to and including 1 V, and *10 MΩ shunted by 20 pF* on 3 V and greater ranges.

There are seven resistance-measuring ranges on the HP 427A, starting at 10 Ω (center scale) and going to a maximum of 10 MΩ. The accuracy of resistance measurements is ±5% of the reading at mid-scale.

Procedure for dc Voltage Measurements:

1. With the instrument switched off, check the pointer zero position. Adjust the mechanical zero as required.
2. If the instrument is battery operated, set the FUNCTION switch to BATT, and check that the battery voltage is a minimum of 1.5 V. For instruments with an internal power supply and line cord, this step is not necessary.
3. Set the FUNCTION switch to DCV + or DCV − as required.
4. Set the RANGE switch to 0.1, and short-circuit the VOLTS and COM terminals. Adjust the DC ZERO/Ω∞ control to set the pointer precisely to zero on the scale, then remove the short circuit connection.
5. Select a voltage range greater than the voltage to be measured. Where the approximate value of the voltage is not known, rotate the RANGE switch to the highest range.
6. Connect the input voltage to the VOLTS and COM terminals, and adjust the range switch to give the greatest on-scale pointer deflection. (Where there is a grounded point in a circuit, the COM terminal should be connected to that point. Where there is more than one electronic instrument involved, all of the COM terminals should be connected to a single point. The reasons for this are discussed in Section 8-3.3).

The procedure for ac voltage measurements is exactly as for dc voltage, but with the FUNCTION switch set to ACV and no need for DC ZERO adjustment.

Resistance Measurement Procedure:

1. With the instrument switched off, check the pointer zero and adjust the mechanical zero control as necessary.
2. Check the battery voltage as explained for dc voltage measurements.
3. Set the FUNCTION switch to OHMS, and with the instrument terminals *open-circuited*, adjust the DC ZERO/Ω∞ control until the pointer indicates infinity (∞) on the resistance scale.
4. Select a resistance range to suit the approximate value of the resistance to be measured.
5. Connect the resistance to the COM and OHMS terminals, and adjust the RANGE control to give a resistance reading as close as possible to *center scale*.

Decibel (dB) and Decibel-milliwatt (dBm) Measurements:

As discussed in Section 3-7, decibel measurement is essentially the same as ac voltage measurements. On the HP427A the decibel scale is read directly when the instrument is set to the 1 V (ACV) range. Since each range position above 1 V is 10 dB above 1 V, 10 dB must be added to the scale reading. For each range position below 1 V, 10 dB must be subtracted from the dB measurements. For example, if the pointer is indicating −1 dB on the 10-V range, the dB measurement is −1 dB + 20 dB = 19 dB. A −5-dB scale reading on the 0.3 V range represents (−5 dB −10 dB) = −15 dB.

Like the VOM described in Section 3-7, the decibel scale on the HP427A is based upon zero dB as 1 mW dissipated in a 600-Ω load resistance. Where the load resistance is other than 600 Ω, the scale reading must be corrected to obtain the absolute dB measurements. However, scale changes can be read directly as changes in dB levels (see Section 3-7).

The *decibel-milliwatt* (dBm) term is sometimes employed because the absolute dB measurements are measurements of *changes* in power level from a starting point of 1 mW power dissipation.

REVIEW QUESTIONS AND PROBLEMS

8-1. Sketch the construction and circuit symbol of a npn bipolar transistor. Identify the various terminals and the terminal currents. Also identify the voltages between terminals, and state typical voltage levels. Write the equations relating the terminal currents. Briefly explain.

8-2. Repeat Question 8-1 for a pnp bipolar transistor.

8-3. Sketch the construction and circuit symbol for an n-channel FET. Identify the various terminals and the terminal currents. Identify the voltages between terminals, and state typical voltages. Briefly explain. Also state the major advantage of FETs as compared to bipolar transistors.

8-4. Sketch the circuit of a basic emitter follower voltmeter. Explain its operation, and compare it to a nonelectronic voltmeter.

8-5. Sketch the circuit of a practical emitter follower voltmeter, and carefully explain its operation.

8-6. An emitter follower voltmeter, as shown in Figure 8-5(b), has the following components: $R_2 = 2.7$ kΩ, $R_3 = 2.7$ kΩ, $R_4 = 3.3$ kΩ, $R_5 = 500$ Ω, $R_6 = 3.3$ kΩ, $(R_S + R_m) = 10$ kΩ. The meter current is 100 μA at FSD. $V_{CC} = +9$ V, $V_{EE} = -9$ V, and the transistors used are silicon with $h_{FE} = 75$. Determine: V_P, I_{E1}, I_{E2}, I_4, and I_B when $E_B = 0$ V.

8-7. For the circuit in Question 8-6, determine the meter readings when $E_B = 0.6$ V, 0.75 V, and 1 V.

8-8. If the transistors in the circuit of Question 8-6 have $V_{BE1} = 0.75$ V and $V_{BE2} = 0.65$ V, determine V_P. Also calculate the range of adjustment for V_P afforded by R_5. Explain how R_5 functions as an electrical zero control.

8-9. List the procedure for using an analog electronic instrument. Also list the calibration procedure.

8-10. Using illustrations, explain a *floating* power supply. Discuss why such supplies must be used in electronic instruments.

8-11. Sketch and explain the circuit of an input attenuator for use with an emitter follower voltmeter.

8-12. Show how an additional input transistor can be used to increase the input resistance of an emitter follower voltmeter. Explain. For the circuit described in Question 8-6, calculate the new input (base) current when an additional transistor with $h_{FE} = 100$ is used to increase the circuit input resistance.

8-13. Sketch the complete circuit of an emitter follower voltmeter using a FET input stage. Explain the operation of the circuit, and explain the effect of the FET.

8-14. A FET input voltmeter as in Figure 8-8 has the following components: $R_1 = 6.8$ kΩ, $R_2 = 4.7$ kΩ, $R_3 = 4.7$ kΩ, $R_4 = 1.5$ kΩ, $R_5 = 500$ Ω, $R_6 = 3.3$ kΩ, $(R_S + R_m) = 20$ kΩ. The meter current is $I_m = 50$ μA FSD, $V_{CC} = +10$ V, $V_{EE} = -10$ V, and the transistors have $h_{FE} = 80$. The gate-source voltage of the FET is $V_{GS} = -3$ V. Calculate: V_P, I_S, I_{E1}, I_{E2}, and I_4 when $E_G = 0$.

8-15. For the circuit described in Question 8-14, calculate the meter indications for 1 V, 3 V, and 4 V inputs when the attenuator is set to its 5-V range.

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8-16. Sketch the circuit of a difference amplifier type of transistor voltmeter. Explain the operation of the circuit, and write the equation for meter circuit voltage in terms of input voltage.

8-17. The difference amplifier voltmeter in Figure 8-9 has the following components: $R_2 = R_5 = 3.9$ kΩ, $R_3 = 300$ Ω, $R_4 = 2.7$ kΩ, $R_1 = R_6 = 10$ kΩ, $V_{CC} = +12$ V, $V_{EE} = -12$ V. Calculate the transistor collector voltage levels when $E = 0$.

8-18. The circuit in Question 8-17 uses transistors with $h_{FE} = 100$ and $h_{ie} = 1.2$ kΩ. The meter has a resistance of $R_m = 750$ Ω and an FSD current of $I_m = 50$ μA. If $R_s = 33$ kΩ, determine the input voltage (E) that will give FSD.

8-19. Sketch the circuit of a transistor amplifier voltmeter, explain its operation, and write the equation for voltage gain. Discuss the advantage of this instrument compared to the difference amplifier type.

8-20. The transistor feedback amplifier voltmeter in Figure 8-10 has $(R_3 + R_m) = 10$ kΩ and $I_m = 100$ μA at FSD. All other components are as illustrated. Calculate the meter deflection when the input voltage is: (a) 10 mV, (b) 3.3 mV.

8-21. For Question 8-20, determine the new meter deflections (a) and (b) when R_2 is changed to 341 Ω.

8-22. Describe an IC operational amplifier. Comment on input terminals, input and output resistance, and voltage gain.

8-23. Sketch and explain the operation of an IC op-amp voltage follower voltmeter.

8-24. A voltage follower voltmeter, as shown in Figure 8-12, uses an IC op-amp with an internal gain of 500 000. A maximum input of 5 V is applied to the noninverting input terminal. Determine the percentage error in the measured voltage due to the operational amplifier.

8-25. Sketch the circuit of a noninverting amplifier voltmeter using an IC op-amp. Explain the operation of the circuit.

8-26. An IC op-amp with an internal gain of 50 000 and an input bias current of 300 nA is to be used as a noninverting amplifier voltmeter as in Figure 8-13. A deflection meter with $I_m = 50$ μA (FSD) and $(R_3 + R_m) = 100$ kΩ is to be used. The meter is to give FSD when the input voltage is 300 mV. Calculate suitable values for resistors R_3 and R_4. Also determine the voltmeter input resistance.

8-27. Sketch a voltage-to-current converter circuit using an IC op-amp. Explain its operation.

8-28. The circuit in Figure 8-14 uses a meter with $I_m = 37.5$ μA (FSD) and $R_m = 900$ Ω. If $R_3 = 80$ kΩ, determine the input voltages that give FSD and 0.5 FSD on the meter.

8-29. Sketch the construction and circuit symbol for a vacuum triode. Explain the operation of the device, and state typical terminal voltages and currents.

8-30. Sketch the circuit of a cathode follower VTVM. Explain the operation of the circuit, and discuss its advantages and disadvantages.

8-31. The VTVM circuit in Figure 8-16 has the following components and voltage levels: $E_{PP} = +50$ V, $E_{KK} = -50$ V, $R_1 = R_2 = 2.2$ kΩ, $V_{K1} = V_{K2} = +6$ V when $E = 0$, $(R_s + R_m) = 100$ kΩ and $I_m = 100$ μA (FSD). Calculate I_{K1} and I_{K2} when $E_G = 0$. Also determine the meter deflection when $E_G = 7.5$ V.

8-32. Sketch a difference amplifier type VTVM and explain its operation. Write the equation for voltage gain from the input to the meter circuit.

8-33. The difference VTVM in Figure 8-17 has the following components: $R_1 = R_6 = 1$ MΩ, $R_2 = R_5 = 8.2$ kΩ, $R_3 = 1$ kΩ, $R_4 = 6.3$ kΩ. The supply voltages are $E_{PP} = 120$ V and $E_{KK} = -120$ V. The meter current is $I_m = 50$ μA FSD, and $R_m = 1.5$ kΩ. The tubes have $\mu = 50$ and $r_p = 5$ kΩ. When input voltage $E = 0$, the common cathode voltage is measured as +6 V. If the meter indicates zero, calculate the plate voltages. Also calculate the value of R_s to give FSD when the input is 500 mV.

8-34. Sketch the circuit of a series ohmmeter as used with an analog electronic instrument. Explain the circuit operation. Also sketch and discuss the ohmmeter scale, and discuss the instrument zero adjustment procedure.

8-35. Calculate the resistance scale markings at 1/4 and 3/4 of FSD for the circuit shown in Figure 8-18.

8-36. Sketch the circuit of a shunt ohmmeter as used with an analog electronic instrument. Explain its operation, and compare it to the series ohmmeter in Question 8-34.

8-37. Calculate the meter deflection for the circuit of Figure 8-19 when $R_x = 2$ kΩ and when $R_x = 300$ Ω.

8-38. Sketch a linear ohmmeter circuit for use with an analog electronic instrument. Explain its operation, and compare it to the series and shunt ohmmeters in Questions 8-34 and 8-36.

8-39. Sketch half-wave rectifier electronic voltmeter circuits using: (a) an IC op-amp voltage follower, (b) a precision rectifier. Explain and compare the operation of each circuit.

8-40. Sketch the circuit of a half-wave rectifier electronic voltmeter using a precision rectifier with amplification. Explain the circuit operation, and write the equation relating peak input voltage and amplifier peak output.

8-41. Sketch a voltage-to-current converter circuit with half-wave rectification. Explain its operation, and write an equation relating instantaneous meter current to instantaneous input voltage.

8-42. A half-wave rectifier electronic voltmeter circuit, as shown in Figure 8-22(a), uses a meter with $I_m = 5$ mA FSD and $R_m = 400$ Ω. Calculate the value of R_1 that will give FSD when the ac input is 300 mV rms. Also determine the meter deflection when the input is 100 mV and 200 mV.

8-43. Sketch the circuit of an ac electronic voltmeter using a voltage-to-current converter with full-wave rectification. Explain the operation of the circuit.

8-44. Sketch a half-bridge full-wave rectifier circuit with dc blocking capacitors, as used with an electronic voltmeter. Explain the circuit operation.

8-45. Sketch a peak detector circuit for use with a peak response electronic voltmeter. Show the voltage waveforms at the points throughout the circuit, and explain its operation. Discuss the need for the peak detector probe.

8-46. Sketch the circuit of a true rms electronic voltmeter using thermocouples. Explain the operation of the circuit.

8-47. Sketch the circuit of a true rms meter using a diode-resistor nonlinear circuit. Explain the operation of the circuit.

8-48. Two waveforms displayed on an oscilloscope have their rms values measured on three different ac voltmeters. The waveforms are: (a) a sine wave with amplitude of 20 V peak-to-peak, and (b) a pulse wave with peak voltage of 20 V, pulse width of 2 ms, and time period of 5 ms. Determine the indicated voltage for each waveform when measured on: (1) a peak response instrument, (2) a full-wave rectifier instrument, (3) a true rms voltmeter.

8-49. Sketch a circuit to show how currents can be measured on an analog electronic voltmeter. Briefly explain.

8-50. Sketch the circuit of a chopper-stabilized electronic voltmeter. Show the voltage waveforms at various points in the circuit, and explain the circuit operation.

8-51. Discuss procedures and precautions for using electronic voltmeters for measurement of: (a) voltage, (b) resistance, and (c) dB.

9

BASICS OF DIGITAL INSTRUMENTS

INTRODUCTION

Before the operation, performance, and applications of digital instruments can be studied, a basic understanding of digital counting circuits must be achieved. These involve the use of the transistor as a switch, in which it is either *on* (conducting) or *off* (not conducting). Transistors and diodes are connected to form *logic gates* and *flip flops*. The flip flop is basically a two-transistor circuit that has two states: Q_1 *on* and Q_2 *off*, or Q_1 *off* and Q_2 *on*. One flip flop may be used to count up to 2, and a cascade of four flip flops can count to 16. Four flip flops may also be connected as a decade counter or scale-of-ten. Three decade counters and one additional flip flop may be cascaded to count to 2000. As well as counting, digital circuits must be able to display the count. Seven-segment light-emitting-diode (LED) displays and liquid-crystal (LCD) displays are available for this purpose.

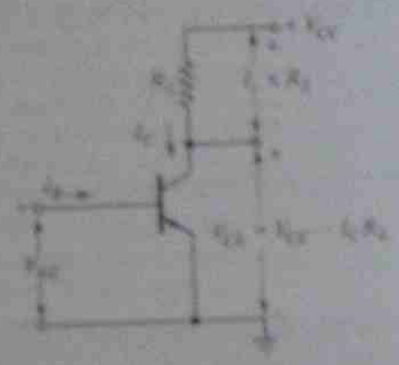
9-1 TRANSISTOR SWITCHING

The transistors in the circuits discussed in Chapter 8 all function as *linear* devices. Each transistor is biased *on*, and in every case the collector current and voltage increase and decrease linearly in relation to the base current. A transistor can also be switched *off* by providing a reverse voltage at its base-emitter junction, or simply by making the base potential equal to the emitter voltage. Similarly, a transistor can be switched *on* into a *saturated*

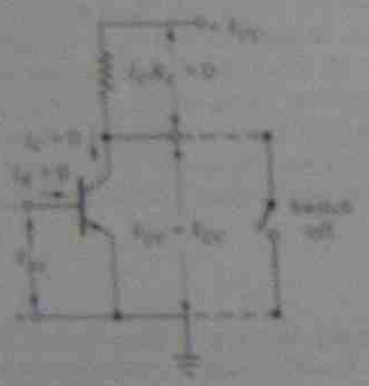
condition, where its collector-emitter voltage is held constant at a level of approximately 0.2 V. In digital circuits, transistors are usually either *on* (saturated) or *off*.

Figure 9-1(a) shows a transistor arranged to function as a switch. A load resistor R_L is connected from supply voltage V_{CC} to the transistor collector. The emitter terminal is grounded. The base-emitter voltage controls the transistor. When $V_{BE} = 0.7$ V (for a silicon transistor) the device is *on*. When $V_{BE} = 0$, or when V_{BE} is negative, the transistor is *off*. The transistor collector-emitter voltage is

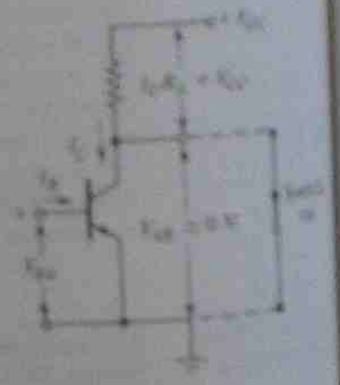
$$V_{CE} = V_{CC} - I_C R_L \tag{9-1}$$



(a) Transistor currents and voltages



(b) Transistor in *off* condition



(c) Transistor in *on* condition

FIGURE 9-1 Transistor switching.

When V_{BE} is zero (or negative) no base current flows [Figure 9-1(b)]. Since $I_C = h_{FE} I_B$ (see Section 8-1), I_C is also zero when $I_B = 0$. The transistor is *off*, there is no voltage drop across R_L, and the transistor collector-emitter voltage equals supply voltage V_{CC}. From Equation 9-1,

$$V_{CE} = V_{CC} - (0 \times R_L) = V_{CC}$$

The transistor is switched *on* when its base-emitter junction is forward biased [Figure 9-1(c)]. Sufficient base current flows to make I_C large enough that $I_C R_L \approx V_{CC}$. Then Equation 9-1 gives

$$V_{CE} = V_{CC} - V_{CC} = 0 \text{ V}$$

A practical transistor cannot have $V_{CE} = 0$ when it is biased *on*. There is always a small saturation *voltage* ($V_{CE(sat)}$):

$$V_{CE(sat)} = 0.2 \text{ V}$$

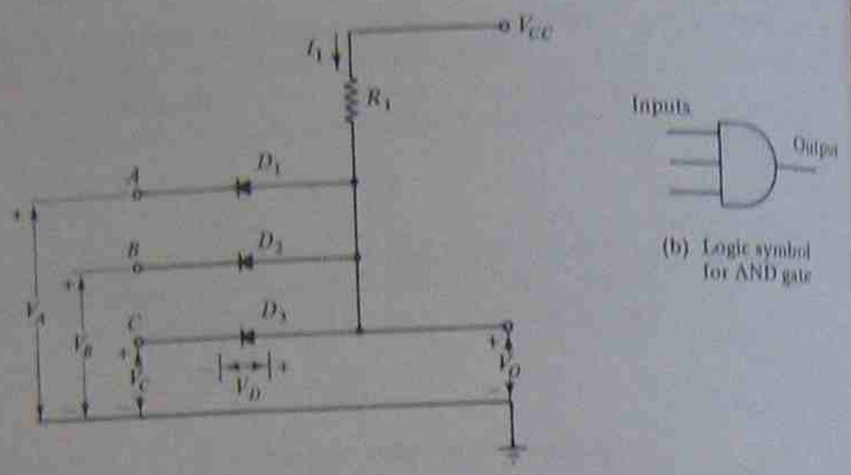
In digital applications transistors are normally either *off* or *on*, and their collector voltages are referred to as either *high* or *low*. Depending upon the supply voltage and the particular circuit, a high voltage level might be between 3 V and 6 V, while a low level might be 1 V or less. To conveniently indicate the *on-off* state of several transistors in a circuit, the high level is usually designated 1, and the low level is designated 0.

There are many important aspects of transistor switching circuits, such as switching speed, power dissipation, and maximum load current. However, an understanding of how digital instrument circuits operate can be achieved without studying these details.

9-2 BASIC LOGIC GATES

The circuit of a diode *AND* gate with three input terminals is shown in Figure 9-2(a). If one or more of the input terminals (i.e., diode cathodes) is grounded, then the diodes are forward biased. Consequently, current I_L flows from V_{CC}, and the output voltage V_o is equal to the diode forward voltage drop V_D. Suppose the supply is $V_{CC} = 5$ V, and an input of 5 V is applied to terminal *A*, while terminals *B* and *C* are grounded. Diode D_1 is reverse biased while D_2 and D_3 remain forward biased, and V_o remains equal to V_D. If levels of 5 V are applied to all three inputs, no current flows through R_L, and $V_o = V_{CC} = 5$ V. Thus, a *high* output voltage is obtained from the *AND* gate only when high input voltages are present at input *A*, *AND* at input *B*, *AND* at input *C*. Hence the name *AND* gate.

An *AND* gate may have as few as two, or a great many input terminals. In all cases an output is obtained only when the correct input voltage level is provided simultaneously at every input terminal.



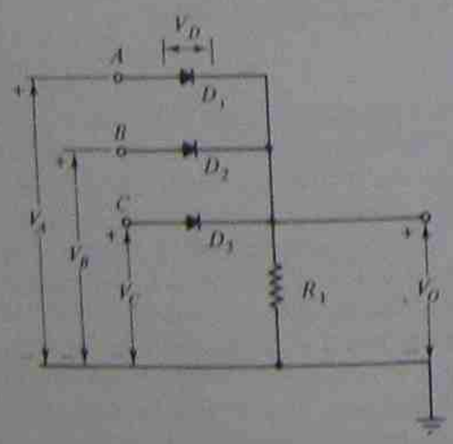
(a) Circuit diagram of AND gate

(b) Logic symbol for AND gate

FIGURE 9-2. Circuit of a three-input diode AND gate and logic symbol for the AND gate.

Figure 9-2(b) shows the graphic symbol employed to represent an AND gate in logic system diagrams.

A three-input diode *OR* gate and its logic symbol are shown in Figure 9-3. It is obvious from the gate circuit that the output is zero when all three inputs are at ground level. If a 5-V input is applied to terminal A, diode D_1 is forward biased, and V_o becomes $(5\text{ V} - V_D)$. If terminals B and C are



(a) Circuit diagram for OR gate



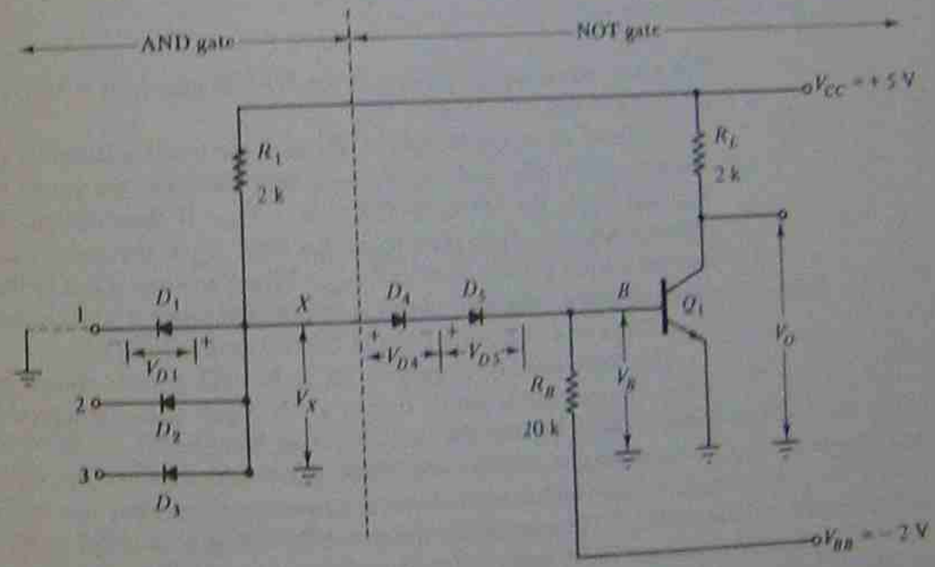
(b) Logic symbol for OR gate

FIGURE 9-3. Circuit of a three-input diode OR gate and logic symbol for the OR gate.

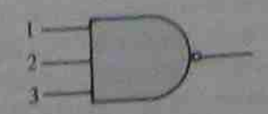
grounded at this time, diodes D_2 and D_3 are reverse biased. Instead of terminal A, the positive input might be applied to terminal B or C to obtain a positive output voltage. A *high* output voltage is obtained from an OR gate, when a high input is applied to terminal A, OR to terminal B, OR to terminal C; hence the name *OR* gate. As in the case of the AND gate, an OR gate may have only two or a great many input terminals.

As already explained, a diode AND gate has a low voltage output when one or more of its inputs are low, and a high output when all inputs are high. If a transistor is connected to invert the output of the AND gate [Figure 9-4(a)], the transistor output is *high* when one or more of the AND gate inputs are low, and *low* when all AND gate inputs are high. Used in this fashion, the inverting stage is termed a *NOT* gate. The combination of the NOT gate and the AND gate is then referred to as a *NOT-AND* gate, or *NAND* gate.

Figure 9-4(a) shows an integrated circuit *diode transistor logic* (*DTL*) NAND gate composed of a diode AND gate and a transistor *inverter*. R_1,



(a) DTL NAND gate



(b) Logic symbol for NAND gate

FIGURE 9-4. Diode transistor NAND gate and logic symbol.

D_1, D_2, and D_3 constitute the AND gate. The inverter is formed by transistor Q_1 with load resistor R_L and bias resistor R_B. When all input terminals are at ground level, the voltage at point X is the voltage drop across the input diodes (i.e., $V_x = V_D$). If diodes D_4 and D_5 were not present, V_x would be sufficient to forward bias the base-emitter junction of Q_1. The negative supply $(-V_{BB})$ keeps diodes D_4 and D_5 forward biased so that when the inputs are at 0 V the transistor base voltage is

$$\begin{aligned} V_B &= V_x - (V_{D4} + V_{D5}) \\ &= V_{D1} - V_{D4} - V_{D5}. \end{aligned}$$

For silicon devices,

$$\begin{aligned} V_B &\simeq 0.7\text{ V}–0.7\text{ V} - 0.7\text{ V} \\ &= -0.7\text{ V}. \end{aligned}$$

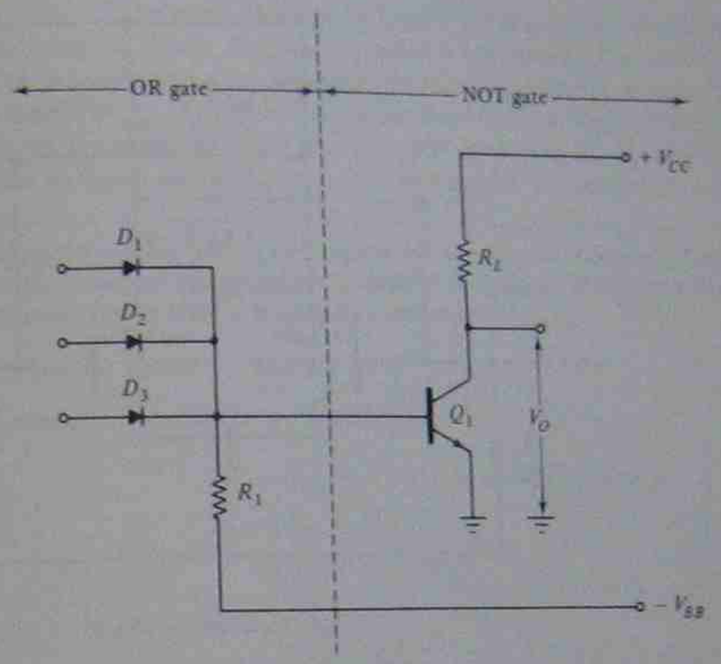
Therefore, when any one input to the NAND gate is at 0 V, Q_1 is biased off, and the output voltage is V_{CC}.

Suppose all inputs to the NAND gate are made sufficiently positive to reverse-bias D_1, D_2, and D_3. Now V_B depends upon the values of R_1 and R_B, and upon the levels of V_{CC} and $-V_{BB}$. If these quantities are all correctly selected, V_B is positive at this time, Q_1 is driven into saturation, and the output voltage goes to $V_{CE(sat)}$. When any one input to the NAND gate is at logic 0, the gate output is at 1. When input A AND input B AND input C are at 1, the output of the NAND gate is level 0.

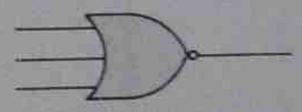
The logic symbol employed for a NAND gate is shown in Figure 9-4(b). The symbol is simply that of a AND gate with a small circle at the output to indicate that the output voltage is inverted.

A transistor inverter (or NOT gate) connected at the output of a positive logic OR gate produces a zero output when any one of the inputs is positive. The circuit is termed a *NOT-OR* gate or *NOR* gate. A diode transistor NOR gate is shown in Figure 9-5(a), with its logic symbol in Figure 9-5(b). As in the case of the NAND gate, a small circle is employed to denote the polarity inversion at the output.

The above brief introduction to logic gates refers only to *diode circuits* and DTL circuits. There are several other families of logic gates, for example, *transistor transistor logic (TTL)*, *emitter coupled logic (ECL)*, and *complementary MOSFET logic (CMOS)*. Each type has its own particular advantages and disadvantages. To study the operation of digital instruments, only an understanding of basic logic gates is required.



(a) DTL NOR gate



(b) Logic symbol for NOR gate

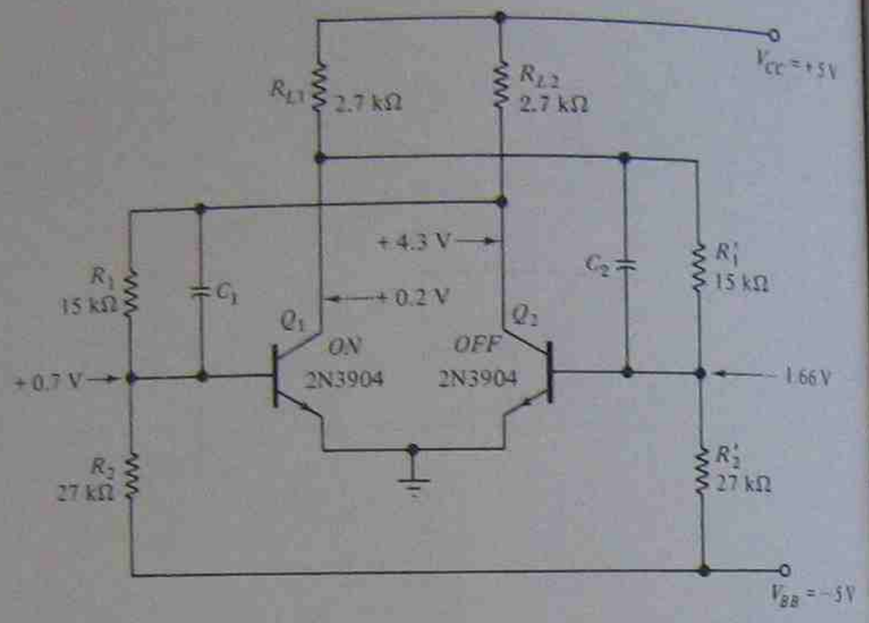
FIGURE 9-5. Diode transistor NOR gate and logic symbol.

9-3 THE FLIP-FLOP

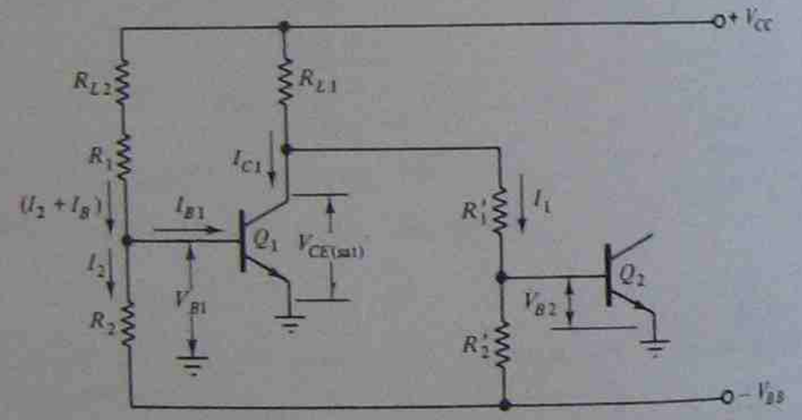
9-3-1 Circuit Operation

The *flip-flop* or *bistable multivibrator* circuit in Figure 9-6(a) has two stable states. Either Q_1 is *on* and Q_2 is *off*; or Q_2 is *on* and Q_1 is biased *off*. The circuit is completely symmetrical. Load resistors R_{L1} and R_{L2} are equal, and potential dividers (R_1, R_2) and (R_1', R_2') form similar bias networks at the transistor bases. Each transistor base is biased from the collector of the other device. When either transistor is *on*, the other transistor is biased *off*.

Consider the condition of the circuit when Q_1 is *on* and Q_2 is *off*. With Q_2 *off*, there is no collector current flowing through R_{L2}. Therefore, as shown in Figure 9-6(b), R_{L2}, R_1, and R_2 can be treated as a potential divider biasing Q_1 base from supply voltages V_{CC} and $-V_{BB}$. With Q_1 *on* in saturation, its collector voltage is $V_{CE(sat)}$, and R_1' and R_2' bias V_{B2} below ground level. Since the emitters of the transistors are grounded, Q_2 is *off*.



(a) Basic flip-flop circuit



(b) Q_1 on, Q_2 off

FIGURE 9-6. Basic circuit of flip-flop or bistable multivibrator and circuit condition when Q_1 is *on* and Q_2 is *off*.

The circuit can remain in this condition (Q_1 *on*, Q_2 *off*) indefinitely. When Q_1 is triggered *off*, Q_2 switches *on*, and remains *on* with its base biased via R_{L1}, R_1', and R_2'. At this time, the base of Q_1 is biased negatively from Q_2 collector. Thus Q_1 remains *off* and Q_2 remains *on* indefinitely. The output voltage at each collector is *high* (logic 1) when the transistor is *off*, and *low* (logic 0) when *on*.

The voltage levels indicated in Figure 9-6(a) are easily determined by analyzing the circuit. The level of collector current (I_{C1}) necessary for Q_1 to be *on* in saturation can be calculated from V_{CC} and R_{L1}. For this current to flow, $\left[h_{FE(\min)} I_{B1}\right]$ must be greater than I_{C1}, [see Figure 9-6(b)]. Also, the voltage at the base of Q_2 can be determined from R_1', R_2', and V_{BB}. V_{B2} must be below the level of the transistor emitter voltage for Q_2 to be *off*.

EXAMPLE 9-1 Using the resistor values and supply voltages shown, calculate the transistor base and collector voltages in the flip-flop circuit in Figure 9-6(a). The transistors each have a minimum current gain $h_{FE(\min)} = 70$.

SOLUTION

Assume Q_1 is on and refer to Figure 9-6(b):

$$V_{B1} = V_{BE} = 0.7\text{ V}\ (\textit{for a silicon transistor}),$$

$$V_{R2} = V_{B1} - V_{BB}$$
$$= 0.7\text{ V} - (-5\text{ V})$$
$$= 5.7\text{ V},$$

$$I_2 = \frac{V_{R2}}{R_2} = \frac{5.7\text{ V}}{27\text{ k}\Omega}$$
$$= 211\ \mu\text{A},$$

$$V_{RL2} + V_{R1} = V_{CC} - V_{B1}$$
$$= 5\text{ V} - 0.7\text{ V}$$
$$= 4.3\text{ V},$$

$$(I_2 + I_B) = \frac{V_{RL2} + V_{R1}}{R_{L2} + R_1} = \frac{4.3\text{ V}}{2.7\text{ k}\Omega + 15\text{ k}\Omega}$$
$$= 243\ \mu\text{A},$$

$$I_B = (I_2 + I_B) - I_2$$
$$= 243\ \mu\text{A} - 211\ \mu\text{A}$$
$$= 32\ \mu\text{A},$$

$$I_C = h_{FE} I_B$$
$$= 70 \times 32\ \mu\text{A}$$
$$= 2.24\text{ mA},$$

for saturation,

$$I_{C(\min)} = \frac{V_{CC} - V_{CE(\text{sat})}}{R_{L1}}$$
$$= \frac{5\text{ V} - 0.2\text{ V}}{2.7\text{ k}\Omega}$$
$$= 1.78\text{ mA},$$

$h_{FE}I_B > I_C(\text{min})$, *therefore* Q_1 *is saturated.*

With Q_1 *saturated,*

$$V_{C1} = V_{CE(sat)} = 0.2\ \text{V}\ (\textit{as illustrated}),$$
$$V_{R'1} + V_{R'2} = V_{C1} - V_{BB}$$
$$= 0.2\ \text{V} - (-5\ \text{V})$$
$$= 5.2\ \text{V},$$
$$I_1 = \frac{V_{R'1} + V_{R'2}}{R'_1 + R'_2} = \frac{5.2\ \text{V}}{15\ \text{k}\Omega + 27\ \text{k}\Omega}$$
$$\approx 124\ \mu\text{A},$$
$$V_{R'1} = I_1 R'_1 = 124\ \mu\text{A} \times 15\ \text{k}\Omega$$
$$= 1.86\ \text{V},$$
$$V_{B2} = V_{C1} - V_{R1}$$
$$= 0.2\ \text{V} - 1.86\ \text{V}$$
$$= -1.66\ \text{V}\ (\textit{as illustrated}),$$
$$V_{BE2} = V_{B2} - V_E$$
$$= -1.66\ \text{V} - 0$$
$$= -1.66\ \text{V},\ Q_2\ \textit{is biased off.}$$

With Q_2 *off,*

$$I_{C2} = 0$$

and

$$I_{RL2} = (I_2 + I_b)$$
$$= 243\ \mu\text{A}$$
$$V_{C2} = V_{CC} - I_{RL2}R_{L2}$$
$$= 5\ \text{V} - (243\ \mu\text{A} \times 2.7\ \text{k}\Omega)$$
$$\approx 4.3\ \text{V}\ (\textit{as illustrated}).$$

Example 9-1 shows that the collector voltage of the *on* transistor is 0.2 V and that of the *off* transistor is 4.3 V. Also, the base voltage of the *on* transistor is 0.7 V, while that at the base of the *off* transistor is −1.66 V. Although Q_1 is shown as *on* and Q_2 as *off* in Figure 9-6, Q_2 could be *on* and Q_1 *off*.

Capacitors C_1 and C_2 in Figure 9-6(a) are equal in value and are known as *commutating capacitors* or *memory capacitors*. The voltages across C_1 and C_2 are easily determined from the collector and base voltages calculated in Example 9-1:

$$E_{C1} = V_{C2} - V_{B1}$$
$$= 4.3\ \text{V} - 0.7\ \text{V}$$
$$= 3.6\ \text{V}$$
$$E_{C2} = V_{C1} - V_{B2}$$
$$= 0.2\ \text{V} - (-1.66\ \text{V})$$
$$= 1.86\ \text{V}.$$

It can be stated that the voltage on the capacitor connected to the base of the *on* transistor is 3.6 V, and that on the capacitor connected to the base of the *off* transistor is 1.86 V. These capacitor voltage levels are important when the flip-flop is to be triggered from one state to another.

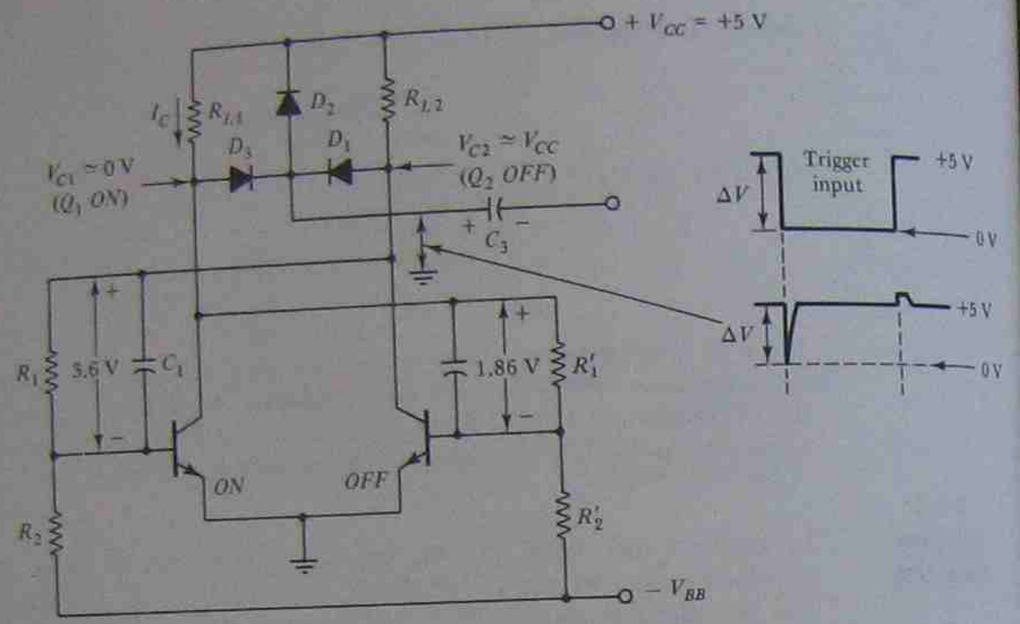
9-3-2 Flip-Flop Triggering

In Figure 9-7(a) diodes D_1, D_2, and D_3 together with capacitor C_3 constitute a *triggering circuit*. Note that Q_1 is *on* and Q_2 is *off*. This means that the voltage across C_1 is 3.6 V, and that on C_2 is 1.8 V, as determined above. Also note that the collector voltage of Q_1 is approximately zero, and that of Q_2 is approximately $V_{CC} = 5$ V. When the trigger input voltage is +5 V, D_3 is reverse biased, and D_1 and D_2 are neither forward nor reverse biased. At this time there is no charge on C_3.

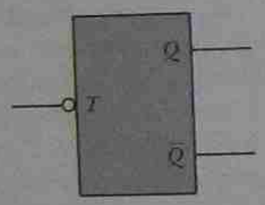
Now consider what happens when the trigger input voltage suddenly goes from +5 V to 0. The junction of the three diodes is rapidly pulled down by $\Delta V = 5$ V, as illustrated. C_3 charges quickly, so that a negative-going voltage spike actually occurs at the cathodes of D_3 and D_1 and the anode of D_2. At the peak of this spike, the cathodes of D_3 and D_1 are at 0 V. Since the anode of D_3 is at $V_{C1} = 0$ V, D_3 is *not* forward biased at this time. However, D_1 *is* forward biased when its cathode is pulled to 0 V, and it pulls the collector of Q_2 down to approximately 0.7 V above ground level. Because C_1 is connected to Q_2 collector, the base of Q_1 is pushed down to

$$V_{B1} = V_{C2} - E_{C1}$$
$$= 0.7\ \text{V} - 3.6\ \text{V}$$
$$= -2.9\ \text{V}.$$

At this instant, both Q_1 and Q_2 are biased *off*. As the spike voltage at the cathodes of D_1 and D_3 rises towards +5 V, the collector and base voltages of both transistors also rise. Because $E_{C2} = 1.86$ V and $E_{C1} = 3.6$ V, Q_2 base rises above ground before Q_1 base gets there. Thus, (the formerly *off*) Q_2 switches *on* before Q_1. As soon as Q_2 switches *on*, its collector voltage drops to approximately zero. This causes Q_1 base to be biased below ground level via R_1 and R_2.



(a) Flip-flop with a triggering circuit



(b) Logic symbol for toggled flip-flop

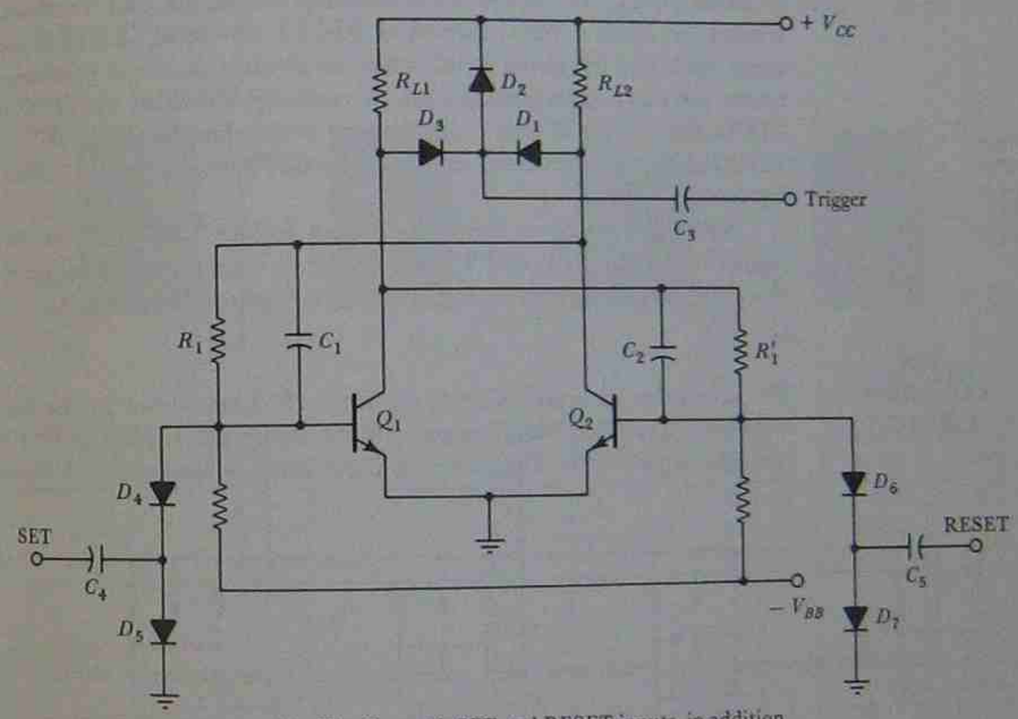
FIGURE 9-7. Triggered (or toggled) flip-flop circuit and logic symbol.

It is seen that the action of the negative-going spike causes Q_2 to switch from *off* to *on* and Q_1 to switch from *on* to *off*. When switch-over occurs, E_{C1} becomes 1.86 V and E_{C2} becomes 3.6 V. Now, another negative-going spike would switch Q_1 *on* and Q_2 *off* again. Before another negative spike can be generated C_3 must be discharged. This is done via diode D_2 as the trigger input returns to +5 V. At this instant the charge on C_3 (+ on the left, − on the right) forward biases D_2, and a *clipped* positive spike is generated, as illustrated in Figure 9-7(a).

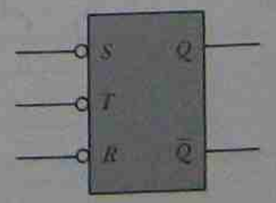
Note that the trigger input voltage levels in Figure 9-7(a) (0 V and +5 V) are the same as the flip-flop (output) collector voltages. So the triggering input can be derived as an output from a similar flip-flop circuit.

Figure 9-7(b) shows the logic symbol for a *triggered* (or *toggled*) flip-flop. The terminals identified as Q and $\bar{Q}$ are the outputs from the transistor collectors. The toggle input (T) has a small circle to indicate that negative-going inputs are required for triggering. Other flip-flops which trigger on positive-going inputs would not have a circle at the T input.

In Figure 9-8(a) two additional diodes and a capacitor are shown connected to each transistor base in the flip-flop circuit. A negative input spike applied via C_4 pulls the cathode of D_4 down and causes the base of Q_1 to be pulled below ground. Thus, Q_1 is set to its *off* condition, and



(a) Flip-flop with SET and RESET inputs, in addition to the trigger (or toggle) input



(b) Logic symbol for RST flip-flop

FIGURE 9-8. Circuit and logic symbol of *RESET-SET-TOGGLE* flip-flop.

consequently Q_2 is *on*. If Q_1 was already *off*, the input via C_4 has no effect. Similarly, a negative spike to Q_2 base via C_5 and D_6 causes Q_2 to switch *off* and Q_1 to go *on*. Once again, if the transistors were already in this condition, the input to C_5 has no effect. Diodes D_5 and D_7 (like diode D_1) discharge the capacitors when the negative inputs return to the normal levels.

When Q_1 is *off*, its collector voltage output is (*high*) logic 1, and Q_2 is *on* with its output (*low*) logic 0. If this condition is identified as a desired initial condition for the flip-flop, it is referred to as a *SET* condition. So the input terminal at C_4 is identified as the *SET* input. The other input terminal (to C_5) which resets the flip-flop out of its SET condition is termed the *RESET* input. Instead of RESET, the term *CLEAR* is sometimes used. The triggering input, which as already discussed, continuously causes the flip-flop to change state, is variously identified as: *TRIGGER*, *TOGGLE*, or *CLOCK* input. A flip-flop which has RESET, SET, and TOGGLE input terminals is known as an *RST flip-flop*, or as a *clocked SC flip-flop*.

Figure 9-8(b) shows the logic symbol for an RST flip-flop. As in Figure 9-7(b), the *R*, *S*, and *T* input terminals each have a small circle to show that negative-going input voltages are required for triggering.

9-4 COUNTING CIRCUITS

The schematic diagram of four flip-flops (FF) connected in cascade is shown in Figure 9-9. Negative-going input pulses are applied to FF 1 via coupling capacitor C_1. Each time an input pulse is applied, FF 1 changes

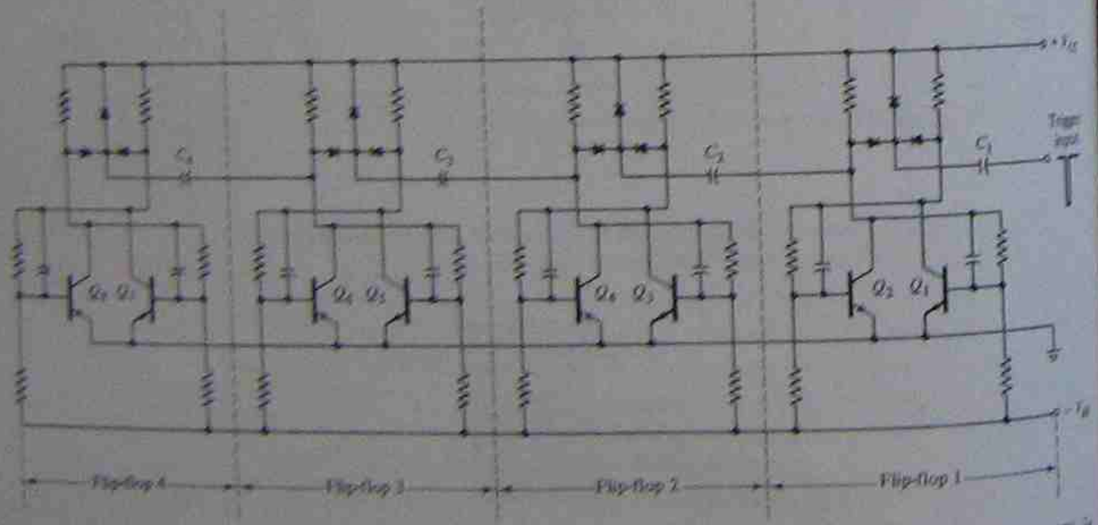
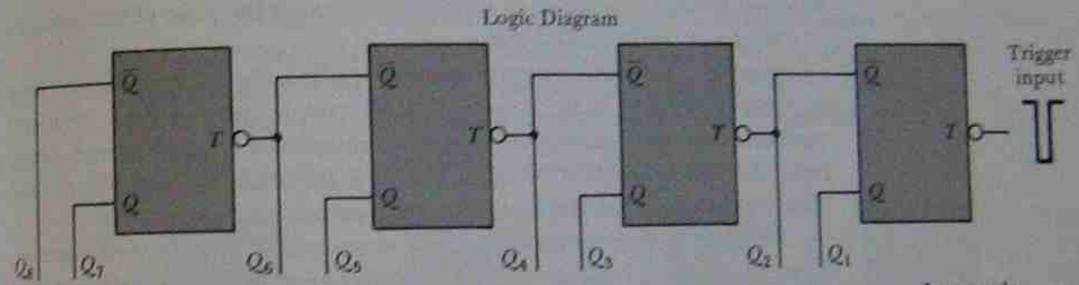


FIGURE 9-9. Four flip-flops connected in cascade. Flip-flop #2 (FF2) is triggered by the output of FF1. FF3 is triggered by FF2, and FF4 is triggered by FF3.

9-4-1 Scale-of-Sixteen Counter

state. The triggering circuit for FF 2 is coupled via capacitor C_2 to transistor Q_2 in FF 1. When Q_2 switches *off*, its collector voltage rises, applying a positive voltage step to C_2. Since a negative-going voltage is required to trigger these flip-flops (see Section 9-3), FF 2 is not affected by the positive-going voltage. When Q_2 switches *on*, its collector voltage drops, thus applying a negative voltage step to FF 2 via C_2. This negative voltage change triggers FF 2. In a similar way, FF 3 is triggered from FF 2, and FF 4 is triggered from FF 3. It is seen that each flip-flop is triggered from each preceding stage.

The four-stage cascade in Figure 9-9 is represented by the logic diagram in Figure 9-10. The various combinations of flip-flop states that



Truth Table

Q_{8C}	Q_{4C}	Q_{2C}	Q_{1C}	Binary count	Decimal count
0	0	0	0	0000	0
0	0	0	1	0001	1
0	0	1	0	0010	2
0	0	1	1	0011	3
0	1	0	0	0100	4
0	1	0	1	0101	5
0	1	1	0	0110	6
0	1	1	1	0111	7
1	0	0	0	1000	8
1	0	0	1	1001	9
1	0	1	0	1010	10
1	0	1	1	1011	11
1	1	0	0	1100	12
1	1	0	1	1101	13
1	1	1	0	1110	14
1	1	1	1	1111	15
0	0	0	0	0000	16

FIGURE 9-10. Logic diagram and truth table for four flip-flops in cascade or scale-of-sixteen counter.

can exist in the four-stage circuit are indicated in the *truth table* in Figure 9-10.

The state of each of the four flip-flops is best indicated by using the *binary* number system, where 0 represents a voltage at or near ground level and 1 represents a positive voltage level. When a transistor is *on*, its collector voltage is low and is represented by 0. An *off* transistor has a high collector voltage and is designated 1. In the decimal system, counting goes from 0 to 9, then the next count is indicated by 0 in the first column and 1 in the next leftward column. In the binary system, the count in all columns can go only from 0 to 1. Thus the count for 1 in both binary and decimal systems is 1. In the binary system, the count for decimal 2 is indicated by 0 in the first column and 1 in the next leftward column. So binary 10 is equivalent to *decimal* 2. The next count in a binary system is 11 and is followed by 100. The table of 0's and 1's showing the state of the flip-flops at each count is the truth table.

Suppose that, before any pulses are applied, the state of the flip-flops in Figures 9-9 and 9-10 is such that all even-numbered (i.e., left-hand) transistors are *on*. Reading only the even-numbered transistors from left to right, the binary count is 0000. At this time the decimal count is 0 and the binary count is 0. See the first horizontal column in Figure 9-10.

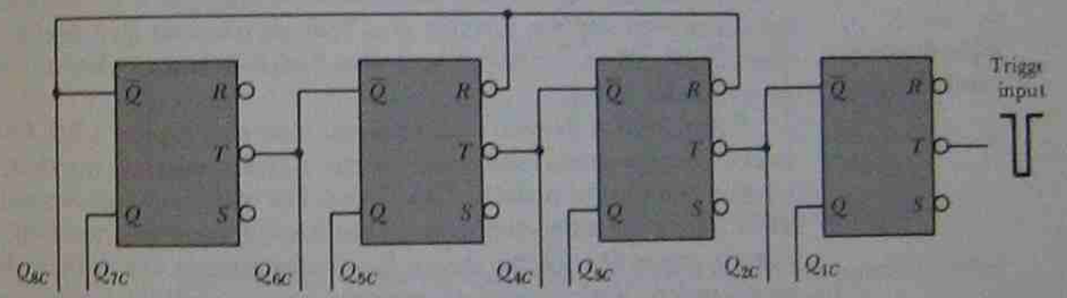
The first trigger pulse causes Q_1 to switch *on* and Q_2 to switch *off*. Thus, Q_2 reads as 1 (positive), and the binary count and decimal count are both 1 (second horizontal column in Figure 9-10). The second input trigger pulse causes FF 1 to change state again, so that Q_1 goes *off* and Q_2 switches *on*. When Q_2 switches *on*, its collector voltage goes low, applying a negative step to FF 2 which triggers Q_3 *on* and Q_4 *off*. Now the binary count is 10, and the decimal count is 2. The third input pulse triggers Q_1 *on* and Q_2 *off* once again. This produces a positive output from FF 1, which does not affect FF 2. At this time, the binary count is 11, for a decimal count of 3. The fourth trigger pulse applied to the input switches Q_1 *off* and Q_2 *on*. Q_2 coming *on* produces a negative step which causes Q_3 to go *off* and Q_4 to switch *on*. Q_4 switch-*on*, in turn, produces a negative voltage step which switches Q_5 *on* and Q_6 *off*. Now the binary count is read from the flip-flops as 100, and the decimal count is 4.

The counting process is continued with each new pulse until the maximum binary count of 1111 is reached. This occurs when 15 input pulses have been applied. The 16th input switches Q_2 *on* once more, producing a negative pulse which triggers Q_4 *on*. Q_4 output is a negative pulse which triggers Q_6 *on*, and Q_6 output triggers Q_8 *on*. Thus, the four flip-flops have returned to their original states, and the binary count has returned to 0000. It is seen that the four flip-flops in cascade have 16 different states, including the zero condition. Therefore, the circuit is termed a *scale-of-sixteen counter* or *modulus sixteen* counter.

9-4-2 Decade Counter

A *scale-of-ten counter*, or *decade counter* is produced by modifying the scale-of-sixteen circuit. Six states of the sixteen must be eliminated to leave only ten possible states. In the method shown in Figure 9-11, the first six states are eliminated leaving the last ten as the only possible circuit conditions. Note that RST flip-flops are employed, so that *reset* and *set* inputs are available. A connection is made from Q_8 (FF 4 output) to the reset terminals in FF 2 and FF 3.

The initial condition of the flip-flops in the decade counter in Figure 9-11 is binary 0110, or decimal 6 (see Figure 9-10). To obtain this condition, transistors Q_4 and Q_6 must be in the *off* state. The first input pulse changes the state of FF 1, causing Q_2 to switch *off*. Thus the collector of Q_2 becomes 1 (i.e., high positive), and the condition of the counter is 0111 (see the truth table in Figure 9-11). The second input pulse (decimal 2) again changes the state of FF 1, this time causing Q_2 to switch *on*. The output from Q_2 is a negative step which triggers FF 2, switching Q_4 *on*. This, in turn, produces a negative step which triggers FF 3 from Q_6 *off* to



Truth Table

Q_{8C}	Q_{6C}	Q_{4C}	Q_{2C}	Decimal count
0	1	1	0	0
0	1	1	1	1
1	0	0	0	2
1	0	0	1	3
1	0	1	0	4
1	0	1	1	5
1	1	0	0	6
1	1	0	1	7
1	1	1	0	8
1	1	1	1	9
Reset 0	0	0	0	10 Reset
0	1	0	0	0

FIGURE 9-11. Logic diagram and truth table for decade counter.

Q_6 *on*. The output from FF 3 triggers FF 4. Counting continues in this way, exactly as explained for the scale-of-sixteen counter, until the tenth pulse. The ninth pulse sets the counter at 1111, and the tenth pulse changes it to 0000. However, as Q_8 switches *on*, it provides the negative output step which resets FF 2 and FF 3 to put Q_4 and Q_6 *off*. The flip-flops have now returned to their initial conditions of 0110, and it is seen that the circuit has only ten different states.

Although the states of the outputs from the decade counter are represented by binary numbers, the numbers no longer correspond with the decimal count, as in the scale-of-sixteen counter. Thus, the numbers representing the outputs from the decade counter are termed *binary coded decimal* (BCD) numbers.

9-5 DIGITAL DISPLAYS OR READOUTS

9-5-1 Light-Emitting Diode Display

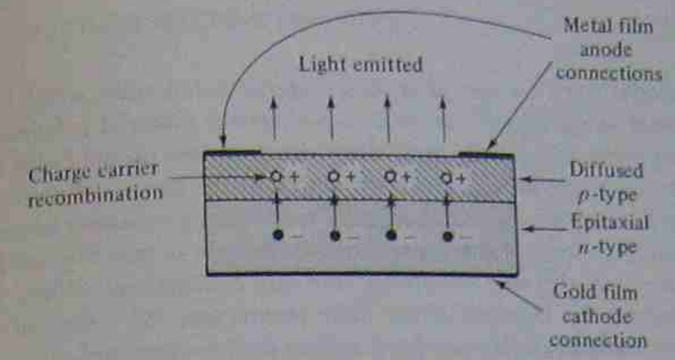
Charge carrier recombination occurs at a forward-biased *pn*-junction as electrons cross from the *n*-side and recombine with *holes* on the *p*-side. When recombination takes place, the charge carriers give up energy in the form of heat and light. If the semiconductor material is translucent, the light is emitted and the junction is a light source, that is, a *light-emitting diode* (LED). When forward biased, the device is *on* and glowing. When reverse biased it is *off*.

Figure 9-12(a) shows a cross-sectional view of a typical LED. Charge carrier recombinations take place in the *p*-type material; therefore, the *p*-region becomes the surface of the device. For maximum light emission, a metal film anode is deposited around the edge of the *p*-type material. The cathode connection for the device is a metal film at the bottom of the *n*-type region. Various types of semiconductor material are used to give red, yellow, or green light emission.

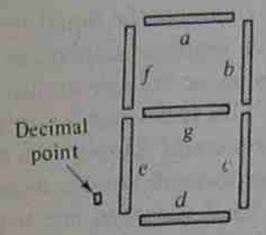
Figure 9-12(b) illustrates the arrangement of a *seven-segment* LED numerical display. Passing a current through the appropriate segments allows any numeral from 0 to 9 to be displayed. The LEDs in a seven-segment display either have all of the anodes connected together, *common anode* [see Figure 9-12(c)], or all of the cathodes connected, *common cathode*. The typical voltage drop across a forward-biased LED is 1.2 V, and typical forward current for reasonable brightness is about 20 mA. This relatively large current requirement is a major disadvantage of LED displays. Some advantages of LEDs over other types of displays are: the ability to operate from a low voltage dc supply, ruggedness, rapid switching ability, and small physical size.

9-5-2 Liquid Crystal Displays

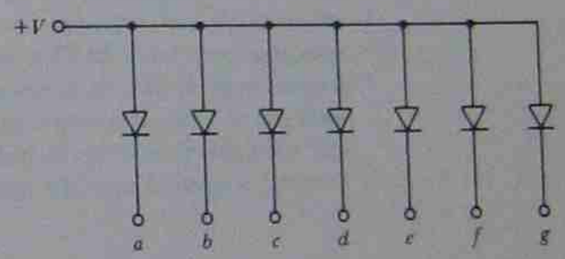
Liquid crystal cell displays (LCD) are usually arranged in the same seven-segment numerical format as the LED display. The cross-section of a *field effect* type liquid crystal cell is illustrated in Figure 9-13(a). The liquid crystal



(a) LED cross-section

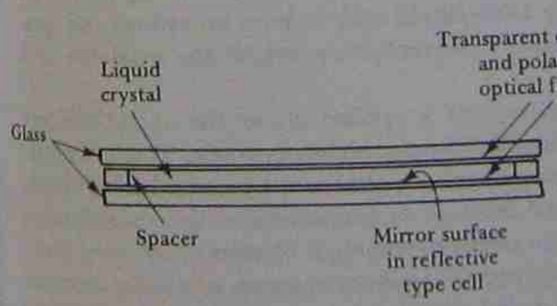


(b) LED numerical display

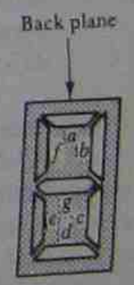


(c) Common anode circuit

FIGURE 9-12. Light-emitting diode cross-section, seven-segment numerical display, and common anode circuit of seven-segment display.



(a) Construction of liquid crystal cell



(b) Liquid crystal cell seven-segment display

FIGURE 9-13. Liquid-crystal cell construction and seven-segment display.

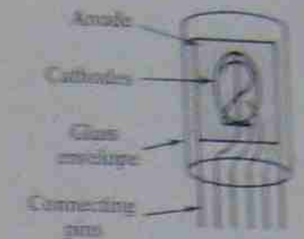
material may be one of several organic compounds which exhibit the optical properties of a crystal. Liquid crystal material is layered between glass sheets with transparent electrodes deposited on the inside faces. Two thin polarizing optical filters are placed at the surface of each glass sheet. The liquid crystal material actually twists the light passing through the ol when the cell is not energized. This allows light to pass through the optical filters, and the cell disappears into the background. When the cell is energized, no twisting of the light occurs and the energized cells in a seven-segment display stand out against their background.

Since liquid crystal cells are light reflectors or transmitters rather than light generators, they consume very small amounts of energy. The only energy required by the cell is that needed to activate the liquid crystal. The total current flow through four small seven-segment displays is typically about 300 μA. However, the LCD requires an ac voltage supply, either in the form of a sine wave or a square wave. This is because a direct current produces plating of the cell electrodes which could damage the device. A typical supply for a LCD is an 8-V peak-to-peak square wave with a frequency of 60 Hz. As in seven-segment LED displays, one terminal of each cell in a liquid crystal display is commoned. In the LCD display the cell terminals cannot be identified as anodes or cathodes; the common terminal is referred to as the *back plane* [see Figure 9-13(*b*)].

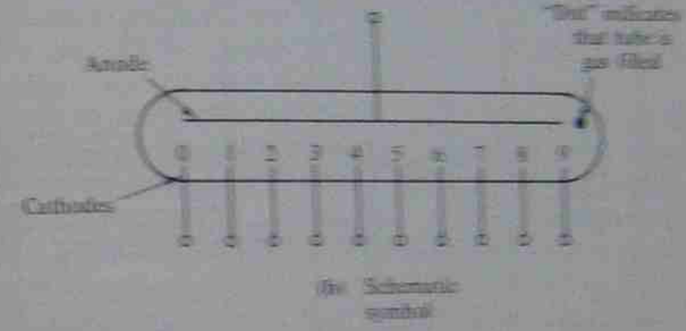
9-5-3 Digital Indicator Tube

The basic construction of a *digital indicator tube* is shown in Figure 9-14(*a*) and its schematic symbol is illustrated in Figure 9-14(*b*). A flat metal plate with a positive voltage supply functions as an anode, and there are ten separate wire cathodes, each in the shape of a numeral from 0 to 9. The electrodes are enclosed in a gas-filled glass tube with connecting pins at the bottom. Neon gas usually is employed and it gives an orange-red glow when the tube is activated; however, other colors are available with different gases.

When a high enough voltage is applied across the anode and one cathode, electrons are accelerated from cathode to anode. These electrons collide with gas atoms and cause other electrons to be emitted from the gas atoms. The effect is termed *emission by collision*. Since the ionized atoms have lost electrons, they are positively charged. Consequently, they accelerate toward the (negative) cathode, where they cause secondary electrons to be emitted when they strike. The secondary emitted electrons cause ionization and electron-atom recombination in the region close to the cathode. This results in energy being released in the form of light and produces a visible glow around the cathode. Since the cathodes are in the shape of numerals, a glowing numeral appears depending upon which cathode is energized.



(*a*) Construction



(*b*) Schematic symbol

FIGURE 9-14. Digital indicator tube, construction, and schematic symbol.

High supply voltages (140 to 200 V) are required for these tubes, and in general they are much bulkier than comparable seven-segment devices. Gas discharge displays are also available in seven-segment format comparable in size to LED displays.

9-6 DISPLAY DRIVERS

As already explained, the state of a decade counter is read in binary form by identifying each collector voltage as either 1 (high) or 0 (low). For display purposes it is necessary to convert the binary output to decimal form. In Figure 9-15 the various states of the decade counter are reproduced from Figure 9-11. In Figure 9-11, only the states of the even-numbered transistors are shown. In Figure 9-15 the states of the odd-numbered transistors are also shown alongside the even-numbered transistor states. The corresponding decimal count of input pulses to the decade counter is also shown.

The lower portion of Figure 9-15 shows ten NAND gates (see Section 9-2) each of which has its output connected to one cathode of a digital

Voltage levels at collectors									Decimal count
0	1	1	0	1	0	0	1		0
0	1	1	0	1	0	1	0		1
0	1	1	0	1	0	1	0	1	2
1	0	0	1	0	1	1	0		3
1	0	0	1	0	1	1	0	1	4
1	0	0	1	1	0	0	1		5
1	0	0	1	1	0	1	0		6
1	0	1	0	0	1	0	1		7
1	0	1	0	0	1	1	0		8
1	0	1	0	1	0	0	1		9
1	0	1	0	1	0	1	0		

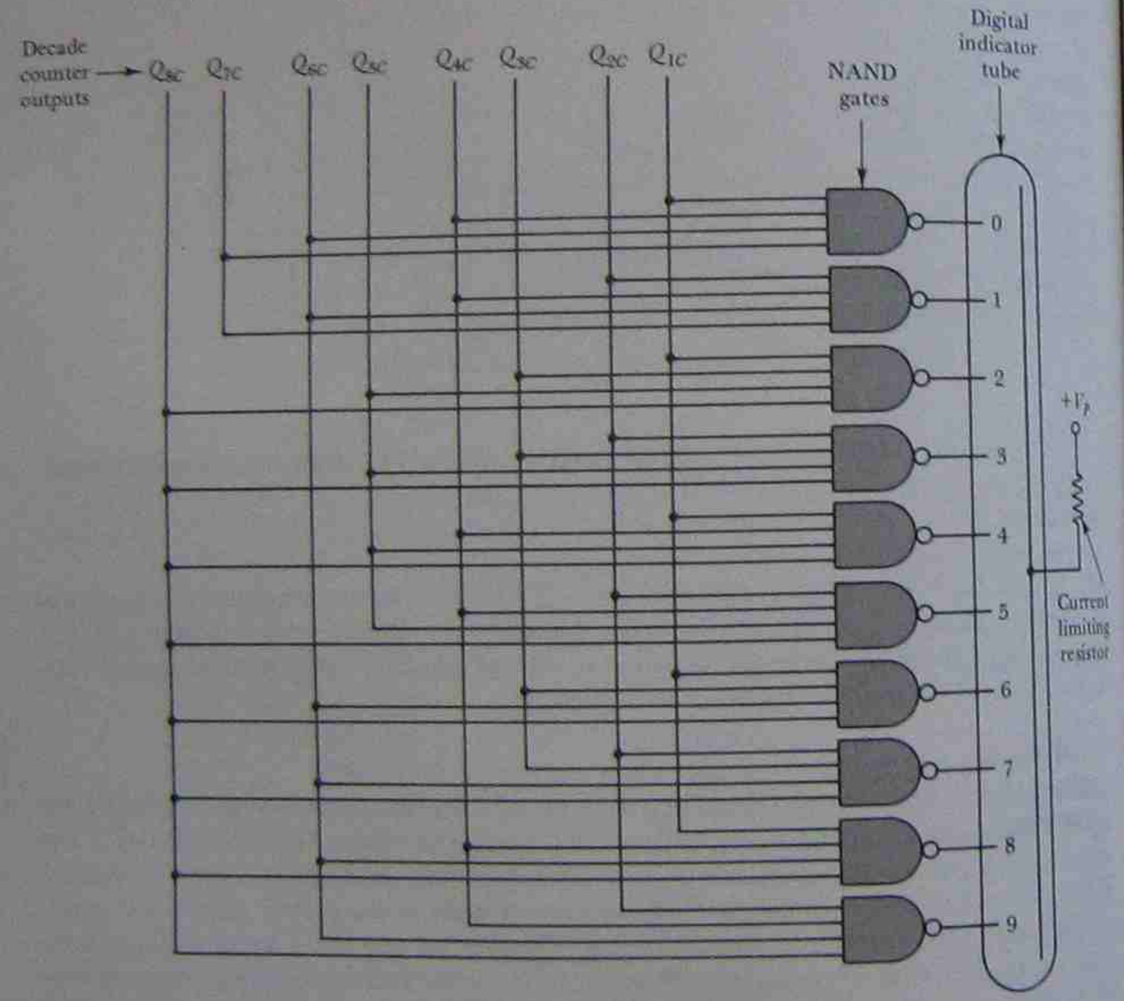


FIGURE 9-15. Logic diagram of display decoder/driver to control digital indicator tube from outputs of decade counter; binary-coded-decimal to decimal conversion.

indicator tube. The four inputs of each NAND gate are connected to the outputs of the decade counter. The input terminal connection arrangement is different for each NAND gate. A positive supply voltage is connected to the anode of the digital indicating tube. When the output of a NAND gate is low (near ground level), current flows through the tube and the grounded cathode glows. As will be seen, only one NAND gate has a low output at any time.

Consider the collector voltage levels in Figure 9-15 for a decimal count of zero. *All* the transistor collector levels, Q_8 to Q_1, are read as: 01 10 10 01. Now look at the inputs to the NAND gate connected to cathode 0 in the digital indicator tube. The inputs of gate 0 are connected to Q_{7C}, Q_{6C}, Q_{4C}, and Q_{1C}. All of these collectors are at high (logic 1) levels. Thus all four inputs to gate 0 are *high*, and consequently the output of this NAND gate is *low*. The 0 cathode in the digital indicator tube is glowing, indicating that the decimal count is zero.

For a correct 0 indication, all other gates (1 through 9) must have high output levels, so that only cathode 0 is energized. To check that this is the case, it is only necessary to identify one low input to each of gates 1 through 9. Gates 1, 3, 5, 7, and 9 each have one input connected to Q_{2C}. Since Q_{2C} is low, all of these gates have a high output. Gates 2 and 6 each have low input from Q_{3C}, gate 4 has a low input from Q_{5C}, and gate 8 has a low input from Q_{8C}. Therefore, only gate 0 has a low output, and only cathode 0 glows.

A careful examination of the gate input conditions for any particular decimal count shows that only the correct cathode is energized. For example, at a decimal count of 5, only gate 5 produces a low output to energize cathode 5. All other gates have *high* outputs at this time.

The NAND gate system illustrated in Figure 9-15 converts the BCD outputs from the decade counter to a decimal output. Thus it can be termed *BCD to decimal* conversion. Conversion of the decade counter outputs to drive a seven-segment display is termed *BCD to seven-segment* conversion, and it is a little more complex than BCD to decimal conversion.

9-7 SCALE-OF-2000 COUNTER

One decade counter together with a digital display and the necessary conversion circuitry can be employed to count from 0 to 9. Each time the tenth input pulse is applied, the display goes from 9 to 0 again. When this occurs, the output of the final transistor in the decade counter goes from 1 to 0 (see Figure 9-11). This is the only time that the final transistor produces a negative-going output, and this output can be used to trigger another decade counter.

Consider the block diagram of the *scale-of-2000* counter shown in Figure 9-16. The system consists of three complete decade counters and

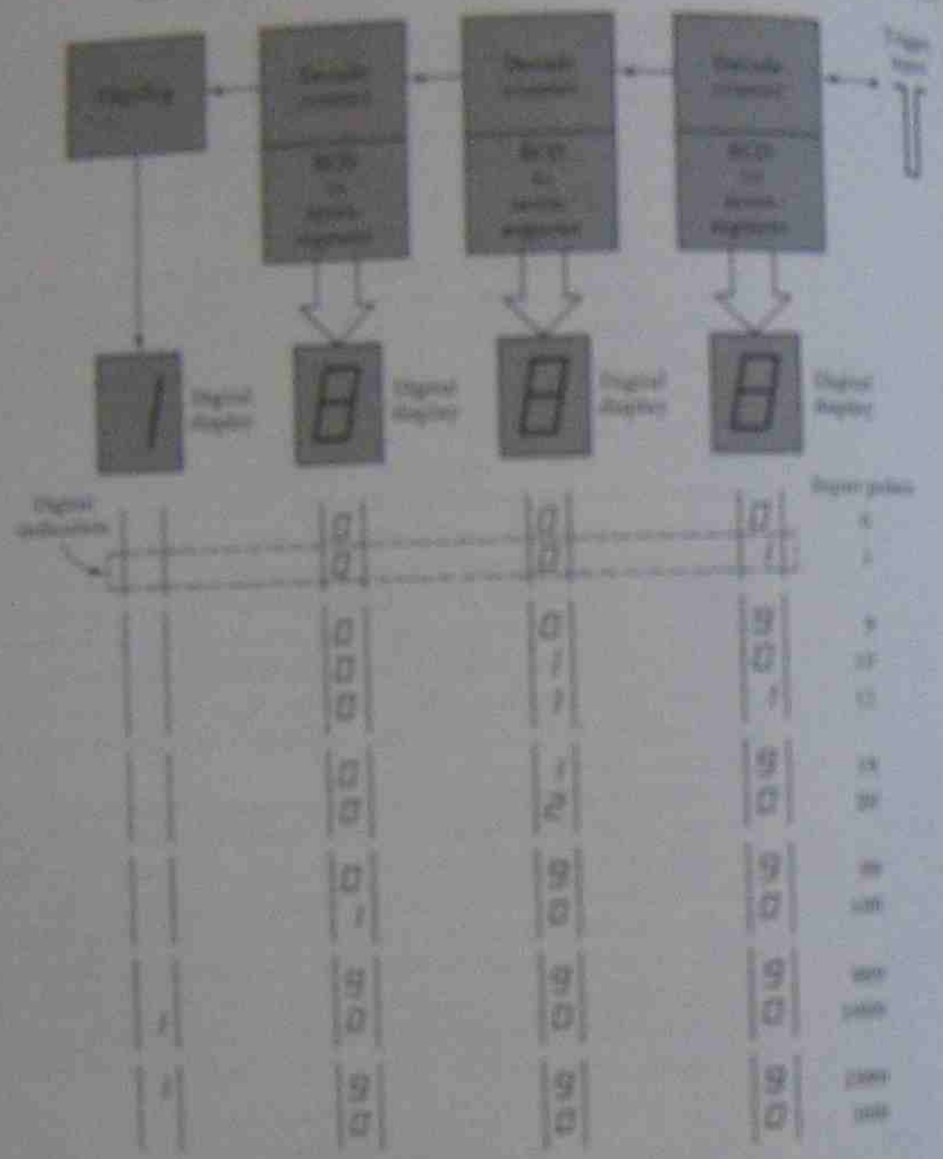


FIGURE 9-16. Scale-of-2000 counter.

displays, and one flip-flop controlling a display which indicates as numeral 1 when on. Starting from 0, all three counters are set at the normal starting conditions, and the numeral 1 indicator is off. This gives an indication of 000. The first 9 input pulses register only on the 1s (right-hand side) display. On the tenth input pulse, the first display goes to 0, and a negative-going pulse output from the first decade counter sets the second decade counter. The display of the second counter now reads

1, so that the complete display reads 010. The counter has counted to 10, and has also registered 10 on the display system.

The next nine input pulses cause the first counter to go from 0 to 9 again so that the display reads 019 on the 19th pulse. The 20th pulse causes the first display to go 0 again. At this time, the final transistor in the first decade counter puts out another negative pulse, which again triggers the second decade counter. The total display now reads 020, which indicates the fact that 20 pulses have been applied to the input of the first decade counter. It is seen that the second decade counter and display is counting tens of input pulses.

Counting continues as described until the display indicates 999 after the 999th input pulse. The 1000th input pulse causes the first two displays (from the right) to go to 0. The second decade counter emits a negative pulse at this time, which triggers the third decade counter. Therefore, the count reads 100. On the 1000th pulse, the first third decade counters go from 999 to 000, and the negative pulse emitted from the third decade counter triggers the flip-flop and turns on the 1 display. The display now reads 1000. It is seen that the system shown in Figure 9-16 can count to a maximum of 1999. One more pulse causes the display to return to its initial 000 condition. The three components of the display which indicate up to 999 are referred to as a *three-digit display*. With the additional 1 component included, the complete numerical display is termed a *3½ digit display*.

REVIEW QUESTIONS AND PROBLEMS

9-1. Sketch a circuit to show an npn transistor employed as a switch. Identify the *on* and *off* voltage polarities and typical voltage levels at the base-emitter and at the collector-emitter terminals. Briefly explain.

9-2. A transistor connected as in Figure 9-1(a) has $V_{CC} = 9$ V, $R_L = 3.3$ kΩ, $h_{FE} = 50$. Calculate the level of V_{CE}: (a) when $I_B = 0$, (b) when $I_B = 25$ μA, and (c) when $I_B = 54.5$ μA.

9-3. Sketch the circuit and logic symbol of a four-input diode AND gate. Explain the operation of the circuit.

9-4. Sketch the circuit and logic symbol of a two-input diode OR gate. Explain the circuit operation.

9-5. Sketch the circuit and logic symbol of a three-input DTL NAND gate. Explain the operation of the circuit.

9-6. Sketch the circuit and logic symbol of a three-input DTL NOR gate. Explain the operation of the circuit.

9-7. Sketch the circuit of a flip-flop using two npn transistors. Carefully explain the conditions that keep one transistor *on* and the other one *off*.

9-8. A transistor flip-flop, as shown in Figure 9-6, has the following components and supply voltages: $R_{C1} = R_{C2} = 4.7$ kΩ, $R_1 = R_2 =$

27 kΩ, $R_2 = R_2' = 40$ kΩ, $h_{FE(min)} = 110$, $V_{CC} = \pm 9$ V. Calculate the transistor base and collector voltages.

9-9. For the circuit described in Question 9-8, calculate the voltage across each of the commutating capacitors. Explain the function of these capacitors.

9-10. Sketch a circuit to show how a flip-flop may be triggered (or toggeled) continuously by input pulses. Explain the triggering circuit operation.

9-11. Sketch a circuit to show how a flip-flop may be set and reset by different inputs. Explain the operation of the circuit.

9-12. Sketch the logic symbols for a toggeled flip-flop and for an RST flip-flop.

9-13. Sketch the logic diagram and truth table for a scale-of-16 counter. Explain the operation of the system.

9-14. Sketch a logic diagram and truth table for a decade counter. Explain the operation of the system. Define *binary-coded decimal*.

9-15. Sketch the cross-section of a light-emitting diode. Explain its operation. Sketch a LED seven-segment display. Explain common-cathode and common-anode type LED displays.

9-16. Sketch the cross-section of a liquid crystal cell, and briefly explain its operation. Sketch a seven-segment liquid crystal display. Discuss the supply requirements for liquid crystal displays, and compare LCD and LED displays.

9-17. Sketch the construction of a digital indicator tube. Explain its operation, and discuss its supply voltage requirements.

9-18. Sketch the logic diagram of a display decoder/driver for controlling a digital indicator tube from a decade counter. Explain the operation of the system.

9-19. Sketch a block diagram for a scale-of-2000 counter. Explain the operation of the system. Show how the system should be modified to count up to: (a) 20 000, (b) 9999. Define $3\frac{1}{2}$ digit display.

10

DIGITAL INSTRUMENTS

INTRODUCTION If a pulse waveform is fed to the input of a digital counter for a time period of exactly one second, the counter indicates the frequency of the waveform. Suppose the counter registers 1000 at the end of a second; then the frequency of the input is 1000 pulses per second. Essentially, a *digital frequency meter* is a digital counter combined with an accurate timing system.

A dc voltage can be converted to a time period which is directly proportional to the voltage. This time period can be measured digitally and the output read as a voltage. Direct current, resistance, and alternating quantities can all be converted into dc voltages for digital measurement. Inductance and capacitance can also be measured digitally.

10-1 TIME BASE

A block diagram and voltage waveforms of a typical time base circuit for a digital frequency meter are shown in Figure 10-1. The source of time interval over which input pulses are counted is a very accurate crystal-controlled oscillator usually referred to as a *clock source*. The crystal is often enclosed in a constant temperature *oven* to maintain a stable oscillation frequency.

The output frequency from the final flip-flop of a decade counter is exactly one-tenth of the input triggering frequency. This means that the time period of the output waveform is exactly ten times the time period of

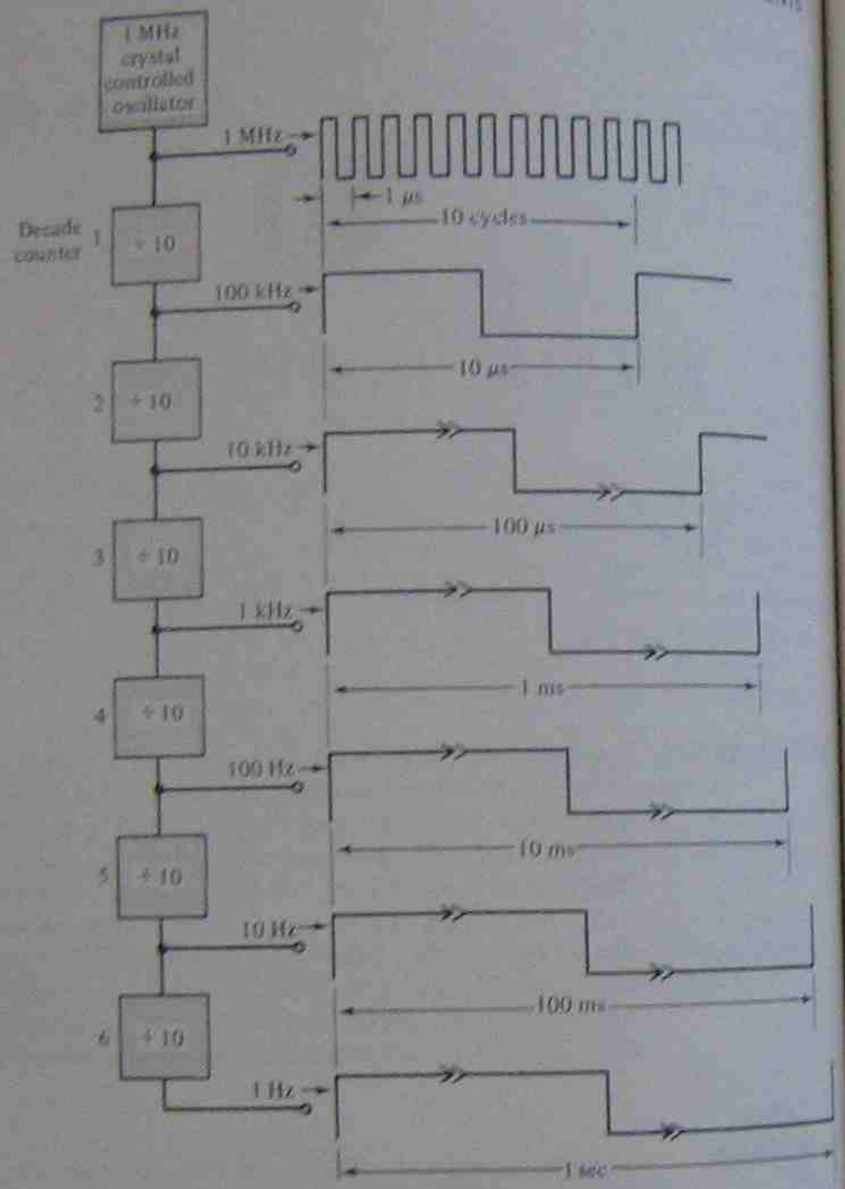


FIGURE 10-1. Time base generation for digital frequency meter.

the input waveform. The 1-MHz output from the crystal oscillator in Figure 10-1 has a time period of 1 μs, and the output waveform from the first decade counter (triggered by the 1-MHz oscillator) has a time period of 10 μs. The time period of the output from the second decade counter (triggered by the output of the first decade counter) is 100 μs, and that from the third decade counter is 1 ms, etc. With all six decade counters, the

available time periods are 1 μs, 10 μs, 100 μs, 1 ms, 10 ms, 100 ms, and 1 sec.

When the counting circuits in a digital frequency meter are triggered for a period of exactly 1 sec, the display registers the input frequency directly. A count of 1000 cycles over the 1-sec period represents a frequency of 1000 Hz or 1 kHz; a 5000 display indicates 5000 Hz, etc. These figures are more easily read when a decimal point is placed after the first numeral and the output is identified in kilohertz. Thus a display of 1.000 is 1 kHz, 5.000 is 5 kHz, and 5.473 is 5.473 kHz. In an LED display, the decimal point is created by use of a single suitably placed light-emitting diode. Also, a *kHz* indication usually is displayed.

Now consider the effect of using the 100-ms time period to control the counting circuits. A display of 1000 now means 1000 cycles per 100 ms. This is 10 000 cycles per sec or 10 kHz. When the time period is switched from 1 sec to 100 ms, the decimal point is also switched from the first numeral to a position after the second numeral. The 10.00 display is now read as 10.00 kHz; 50.00 is read as 50.00 kHz, etc.

When the time period is switched to 10 ms, the decimal point is moved to a new position after the third numeral on the display. A 100.0 display now becomes 100.0 kHz. Since this is the result of 1000 cycles of input counted over a period of 10 ms, the actual input frequency is 1000/10 ms, that is, 100 kHz. With a 1-ms time period, a display of 1000 indicates 1000 cycles during 1 ms, or 1 MHz. The decimal point is now moved back to its original position after the first numeral, and a *MHz* indication is displayed. Therefore, the display of 1.000 with a 1-ms time base is read as 1.000 MHz. If the 100-μs and 10-μs time periods are used, the decimal point is again moved so that the 1000 indication becomes 10.00 MHz and 100.0 MHz, respectively.

EXAMPLE 10-1 A 3.5-kHz sine wave is applied to a digital frequency meter. The time base is derived from a 1-MHz clock generator frequency divided by decade counters. Determine the meter indication when the time base uses (a) six decade counters and (b) four decade counters.

SOLUTION

a. When six decade counters are used:

$$\textit{time base frequency} = f_t = \frac{1\text{ MHz}}{10^6} = 1\text{ Hz},$$

$$\textit{time base} = t_t = \frac{1}{f_t} = \frac{1}{1\text{ Hz}} = 1\text{ sec}$$

$$\left.\begin{matrix}\textit{cycles of input}\\ \textit{counted during } t_t\end{matrix}\right\} = (\textit{input frequency}) \times t_t$$

$$= 3.5\text{ kHz} \times 1\text{ sec}$$

$$= 3500.$$

b. When four decade counters are used:

$$\text{time base frequency} = f_2 = \frac{1\text{ MHz}}{10^4} = 100\text{ Hz},$$

$$\text{time base} = t_2 = \frac{1}{f_2} = \frac{1}{100\text{ Hz}} = 10\text{ ms},$$

$$\left.\begin{matrix}\text{cycles of input} \\ \text{counted during } t_2\end{matrix}\right\} = \text{input frequency} \times t_2$$

$$= 3.5\text{ kHz} \times 10\text{ ms}$$

$$= 35.$$

10-2 LATCH AND DISPLAY ENABLE

If the numerical display devices in a digital frequency meter are controlled directly from the counting circuits, the display changes rapidly as the count progresses from zero. Suppose the input pulses are counted over a period of 1 sec, and then the count is held constant for 1 sec. The display alternates between changing continuously for one second and being constant for the next second. Therefore, the display is quite difficult to read, and the difficulty is increased when shorter time periods are employed for counting. To overcome this problem, *latch circuits* are employed.

A *latch* isolates the display devices from the counting circuits while counting is in progress. At the end of the counting time, a signal to the latch causes the display to change to the decimal equivalent of the final condition of the counting circuits. Latch circuits are essentially additional (special kind) flip-flops connected between the outputs of a decade counter and the display decoder/driver circuitry (e.g., between the transistor collectors and the NAND gate inputs in Figure 9-15). While counting is in progress, the latch flip-flop outputs are held in a constant state. At the end of the counting time, the flip-flops are released to set the displays according to the final states of the decade counter outputs.

A *display enable* control which open-circuits the supply voltage to the display devices is sometimes used instead of a latch. The display is simply switched *off* during the counting time and *on* during the noncounting time. The (normally constant) displayed numerals are thus switched *on* and *off* continuously, with no display occurring during the counting time. When the display time and counting time are brief enough, the *on/off* frequency of the display is so high that the human eye sees only a constant display.

10-3 BASIC DIGITAL FREQUENCY METER SYSTEM

The block diagram of a digital frequency meter with a four-digit display is shown in Figure 10-2, and the voltage waveforms for the system are illustrated in Figure 10-3. The input signal which is to have its frequency measured is first amplified or attenuated, as necessary, and then fed to a

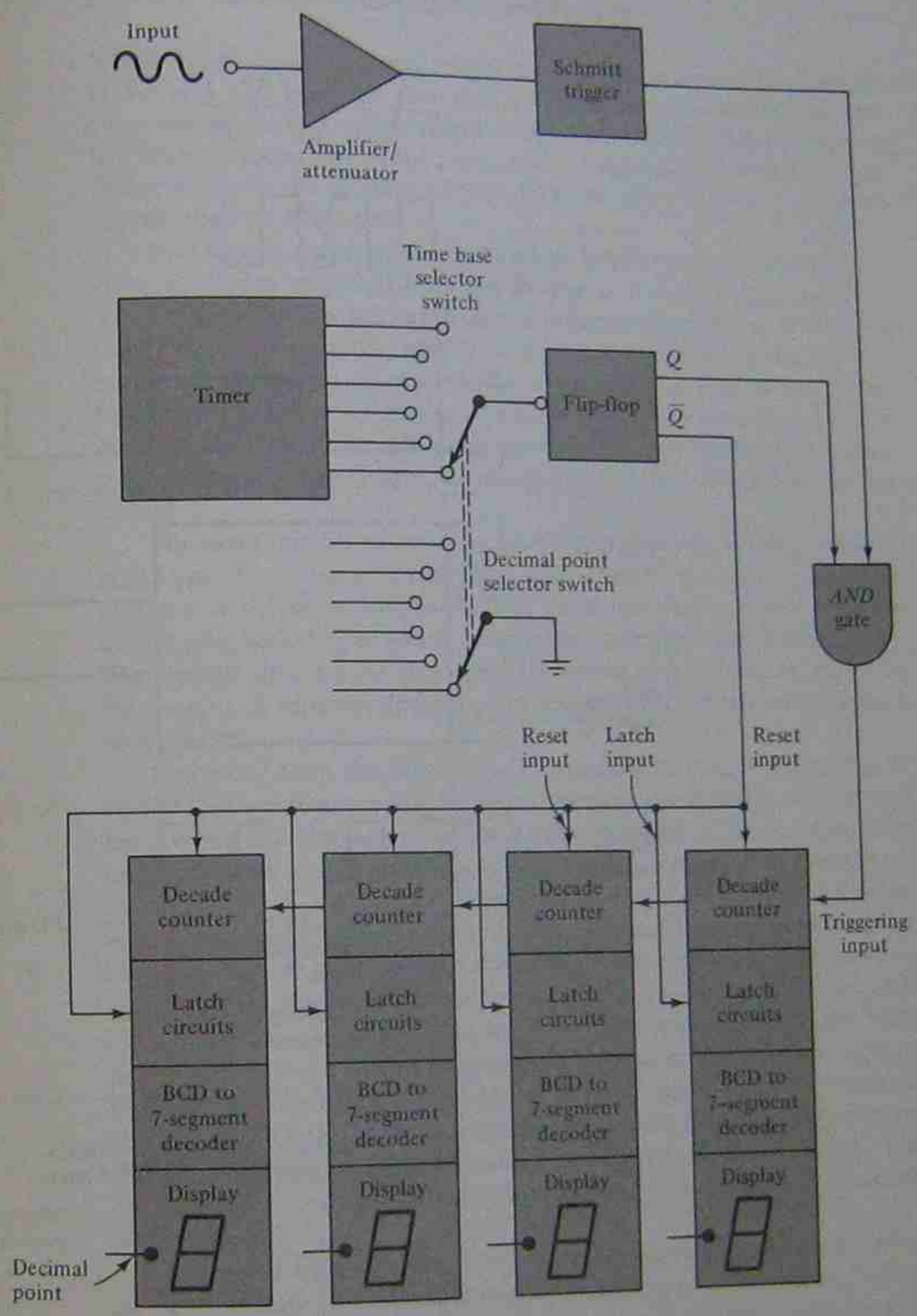


FIGURE 10-2. Block diagram of a digital frequency meter.

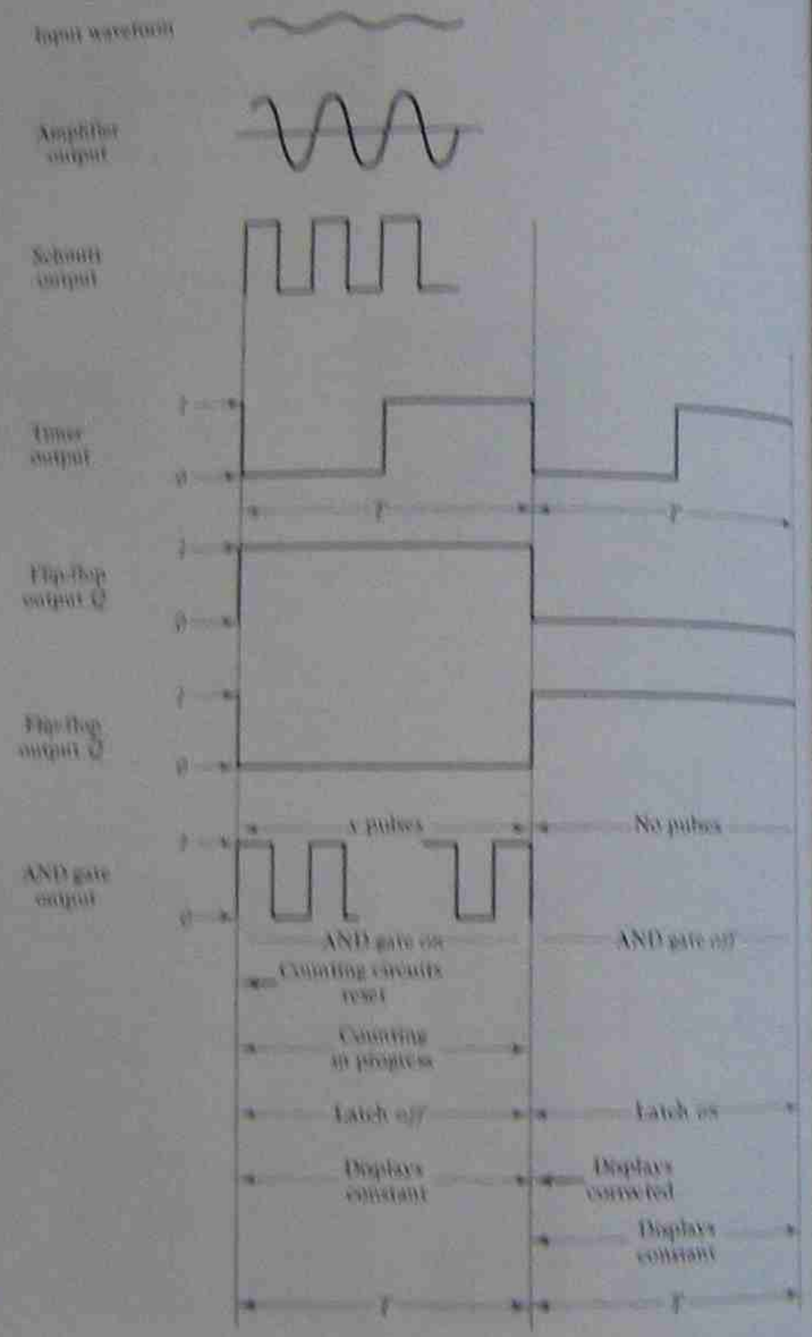


FIGURE 10-3. Waveforms for a digital frequency meter.

Schmitt trigger circuit. (Schmitt trigger circuits are explained in Sections 11-4-1 and 15-2. For now note that a Schmitt circuit converts sine and other waveforms into square waves or pulse waves). The Schmitt output has the same frequency as the input, and it triggers the counting circuits. Before it gets to the counting circuits, however, the pulse waveform must pass through an AND gate.

The square wave from the Schmitt passes to the counting circuits only when output Q from the *flip-flop* is at logic 1 (i.e., positive). The flip-flop changes state each time a negative-going output is received from the timer. Therefore, when $T = 1$ sec (see Figure 10-3), the flip-flop output is alternately at level 1 for 1 sec and at level 0 for 1 sec. Consequently, the AND gate is alternately *on* for one second and *off* for one second. That is, the AND gate alternately passes the Schmitt output pulses to the counting circuits for one second, and then blocks them for one second.

The exact number of input pulses is counted during the time that the AND gate is *on*, and as already discussed, when $T = 1$ sec the count is a measure of the input frequency. The timer has six (or more) available output time periods over which counting can take place (see Section 10-1). The desired time period is selected by means of a switch, as shown in Figure 10-2. A separate decimal point selector switch moves with the time base selector.

Output $\bar{Q}$ from the flip-flop is in antiphase to output Q (see Figure 10-3). This waveform is employed for resetting the counting circuits and for opening and closing the latches. At the beginning of the counting time, output $\bar{Q}$ from the flip-flop is a negative-going voltage. This triggers the reset circuitry in the decade counters to correctly set the initial starting conditions of each counter. Since flip-flop output $\bar{Q}$ is at logic 0 during the counting time, its application to the latch circuits ensures that each latch is *off*. Therefore, during the counting time nothing passes through the latch circuits. At the end of the counting time, the waveform fed to the latch inputs goes to logic 1. This triggers each latch *on* so that the conditions of the displays are corrected, if necessary, to reflect the states of the counting circuits. During the latch *on* time, the AND gate is *off* and no counting occurs. Therefore, once corrected, the displays remain constant. The displays remain constant also during the counting time, since the latch circuits are *off*.

Instead of manually switching to the appropriate timer range, some instruments have an automatic range selection system (*auto ranging*). This usually consists of a circuit which generates a voltage approximately proportional to the input frequency. Depending upon the actual voltage level, one of several transistor switches is turned *on* to select the correct time base and decimal point position.

10-4 FREQUENCY MEASUREMENTS, ERRORS, AND RECIPROCAL COUNTING

In the system described in Section 10-3, the time base could switch the AND gate *on* or *off* while an input pulse (from the Schmitt) is being applied. The partial pulses that get through the AND gate may or may not succeed in triggering the counting circuits. So there is always a possible error of ±1 cycle in the count of input cycles during the timing period. Thus, the accuracy of a digital frequency meter is usually stated as

$$\pm 1 \text{ count} \pm \text{time base error}.$$

Errors in the time base generated by the crystal oscillator (Figure 10-1) are normally the result of variations in temperature, supply voltage changes, and aging of crystals. With reasonable precautions, the total time base error might typically be $< 1 \times 10^{-6}$, or *less than one part in* 10^6 *parts*. (Higher quality time bases have smaller errors.) The total measurement error depends upon the actual frequency being measured. This is demonstrated by Example 10-2.

EXAMPLE 10-2 A frequency counter with an accuracy of ±1 count $\pm(1 \times 10^{-6})$ is employed to measure frequencies of 100 Hz, 1 MHz, and 100 MHz. Calculate the percentage measurement error in each case.

SOLUTION

At $f = 100$ Hz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 100 \text{ Hz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 1 \times 10^{-4} \text{ counts}) \\ &\approx \pm 1 \text{ count}, \\ \% \text{ error} &= \pm \left(\frac{1}{100 \text{ Hz}} \times 100\% \right) \\ &= \pm 1\%. \end{aligned}$$

At $f = 1$ MHz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 1 \text{ MHz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 1 \text{ count}) \\ &\approx \pm 2 \text{ counts}, \\ \% \text{ error} &= \frac{2}{1 \text{ MHz}} \times 100\% \\ &= 2 \times 10^{-4}\%. \end{aligned}$$

At $f = 100$ MHz,

$$\begin{aligned} \text{error} &= \pm (1 \text{ count} + 100 \text{ MHz} \times 10^{-6}) \\ &= \pm (1 \text{ count} + 100 \text{ counts}) \\ &= \pm 101 \text{ counts}, \\ \% \text{ error} &= \pm \left(\frac{101}{100 \text{ MHz}} \times 100\% \right) \\ &= \pm 1.01 \times 10^{-4}\%. \end{aligned}$$

Example 10-2 demonstrates that at a frequency of 100 Hz the error due to ±1 count is ±1%, while that due to the time base is insignificant. At 1 MHz, the error due to one count is equal to that due to the time base. At 100 MHz, the time base is responsible for an error of ±100 counts, although the total error is still a very small percentage of the measured frequency. Therefore, at high frequencies the time base error is larger than the ±1 count error, while at low frequencies the ±1 count error is the larger of the two.

Obviously, the greatest measurement error occurs at low frequencies. At frequencies lower than 100 Hz, the percentage error due to ±1 count is greater than 1%. The low frequency error can be greatly reduced by the *reciprocal counting technique*.

Suppose the time base is disconnected from the system shown in Figure 10-2. Also, assume that the 1-MHz frequency from the crystal-controlled oscillator in the time base (Figure 10-1) is connected directly to the AND gate input in place of the Schmitt. The Schmitt output is now applied as an input to the flip-flop, so that the frequency to be measured is going to the flip-flop instead of to the AND gate input. The new arrangement is shown in Figure 10-4. The result is that the AND gate is switched *on* for the period of the frequency to be measured (see Figure 10-4) and that pulses from the 1-MHz crystal source trigger the counting circuits during this time.

When the frequency to be measured is 100 Hz, the AND gate is *on* for a period of 1/100 Hz = 10 ms. Each cycle from the 1-MHz crystal has a time period of 1 μs. Therefore, the number of pulses counted during 10 ms is

$$\frac{10 \text{ ms}}{1 \mu s} = 10\,000.$$

This is indicated on the display as *100.00 Hz*. (In fact, the four-digit display in Figure 10-2 would not be suitable in this case. A $4\frac{1}{2}$-digit display, or a 5-digit display is required.) The accuracy of measurement of the 100-Hz

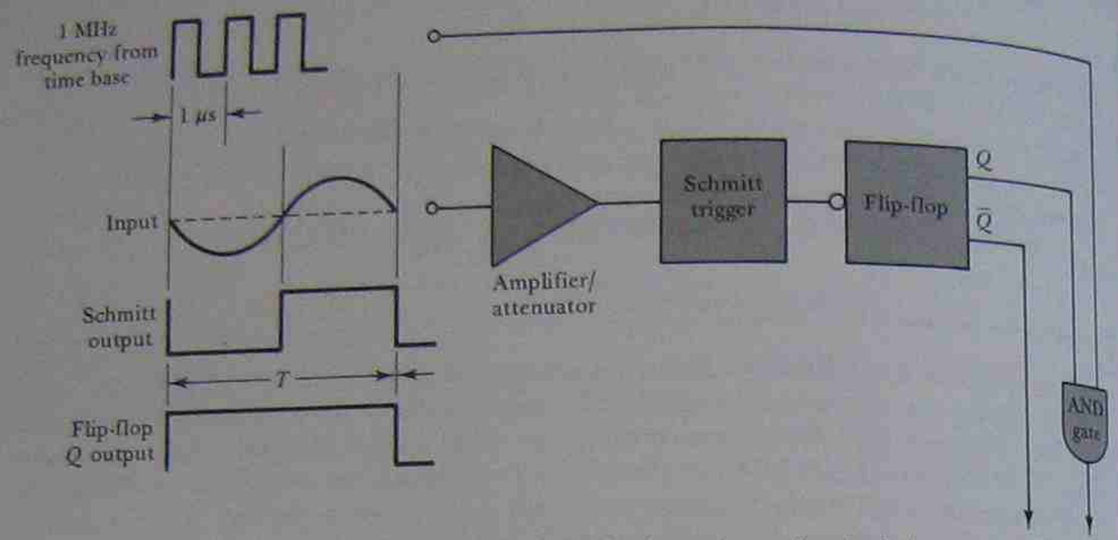


FIGURE 10-4. Reciprocal counting technique.

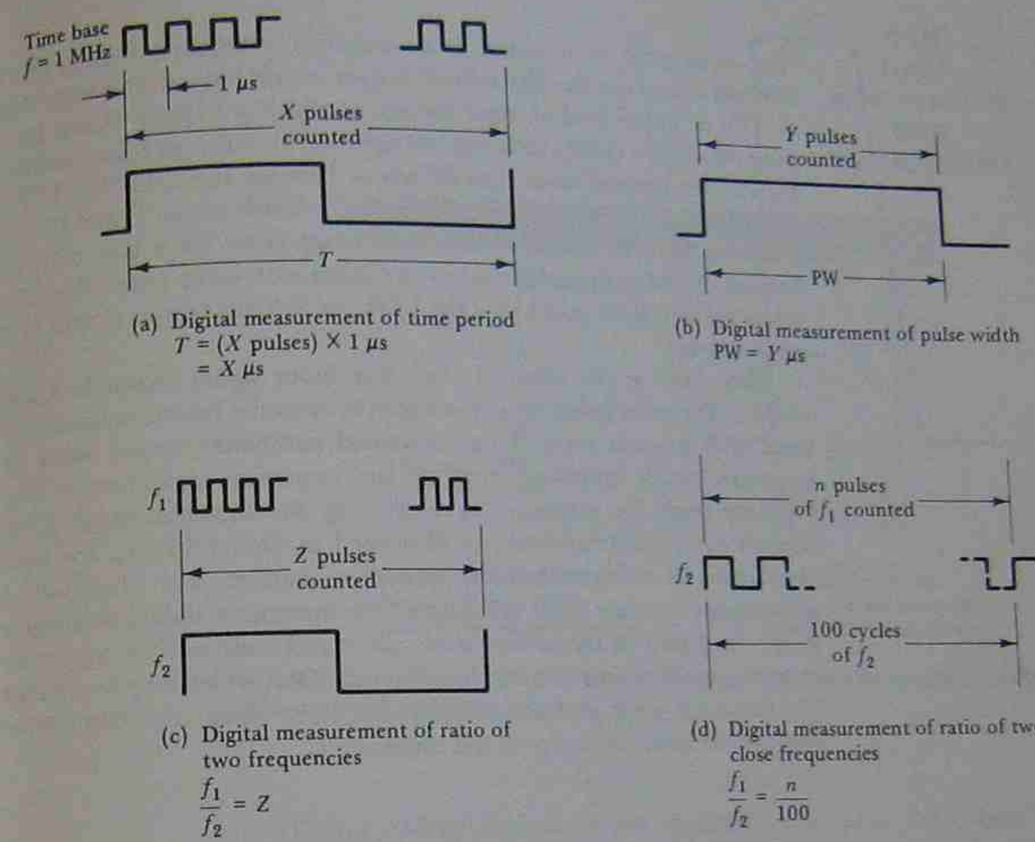
frequency is now ±1 count in 10 000, or 100 Hz/10 000 = 0.01 Hz. As a percentage of the measured frequency the error is

$$\% \text{ error} = \frac{0.01 \text{ Hz}}{100 \text{ Hz}} \times 100\% = \pm 0.01\%.$$

A 0.01% error is a big improvement over the 1% error that occurs with the straight counting technique. At frequencies lower than 100 Hz, the accuracy of measurement is even better (with the reciprocal counting technique). At high frequencies, the straight counting method gives the most accurate results.

10-5 TIME AND RATIO MEASUREMENT

The reciprocal count technique described in Section 10-4 is, in fact, a time measurement method, although the display is expressed as a frequency. The display could be properly expressed as a time period; for example, the 100.00-Hz measurement is made as 10 000 × 1 μs, which is 10.000 ms. The time period of any input waveform can be measured in this way [see Figure 10-5(a)]. If the flip-flop in Figure 10-4 is made to trigger on positive-going inputs as well as on negative-going signals, the width or duration of an input pulse can be measured [Figure 10-5(b)]. Most digital counters have a *start input* and a *stop input*, so that the *time between events* can be measured.



(a) Digital measurement of time period
$T = (X \text{ pulses}) \times 1\ \mu s = X\ \mu s$

(b) Digital measurement of pulse width
$PW = Y\ \mu s$

(c) Digital measurement of ratio of two frequencies
$\frac{f_1}{f_2} = Z$

(d) Digital measurement of ratio of two close frequencies
$\frac{f_1}{f_2} = \frac{n}{100}$

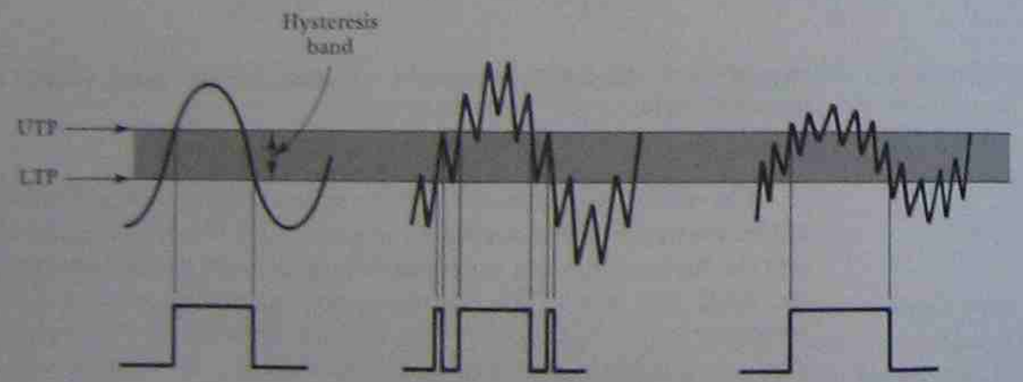
FIGURE 10-5. Digital measurement of time period, pulse width, and frequency ratio.

The ratio of two frequencies can be measured by a counter. The lowest of the two frequencies is applied as an input to the flip-flop in Figure 10-4, and the higher frequency is applied (via appropriate shaping circuitry) to the AND gate input. The instrument now counts the number of high-frequency cycles that occur during the time period of the low frequency. The waveforms are illustrated in Figure 10-5(c). If the high frequency is 100 times the low input frequency, 100 cycles of high frequency are counted. Thus, the displayed number is the ratio of the two input frequencies. The waveform illustrated in Figure 10-5(c) are for the case when one frequency is very much greater than the other. When this is *not* the case (e.g., when $f_1/f_2 = 1.11$), the cycles of f_1 are counted over perhaps 100 cycles of f_2 [Figure 10-5(d)]. With the decimal point selected correctly, the displayed ratio is 1.110.

10-6 INPUT ATTENUATION AND AMPLIFICATION

The input stage to a counter is an amplifier/attenuator feeding into a Schmitt trigger circuit. The Schmitt trigger circuit has an *upper trigger point* (UTP), or upper level of input voltage at which it triggers. It also has a *lower trigger point* (LTP), or lower voltage level at which its output switches back to the original state. The difference between the UTP and LTP is termed *hysteresis*. The effect of the hysteresis is illustrated in Figure 10-6(a). Assuming that the amplifier/attenuator stage is set for a gain of 1, the Schmitt output goes positive when the input sine wave passes the UTP. When the sine wave goes below the LTP, the Schmitt output returns to its previous level.

Now look at the effect of the noisy input signal shown in Figure 10-6(b). The noise spikes cause the signal to cross the hysteresis band more than twice in each cycle. Thus, unwanted additional output pulses are generated which introduce errors in the frequency measurement. This difficulty could be overcome by expanding the hysteresis band of the Schmitt circuit. Alternatively, as illustrated in Figure 10-6(c), the input signal can be attenuated. Most frequency counters are fitted with a continuously variable input attenuator. The attenuator should be adjusted to set the signal at the lowest level which will satisfactorily trigger the counting circuits. Some counters have *low-pass filters* which may be switched into the input stage to attenuate high-frequency noise, and thus further improve the noise immunity of the counter.

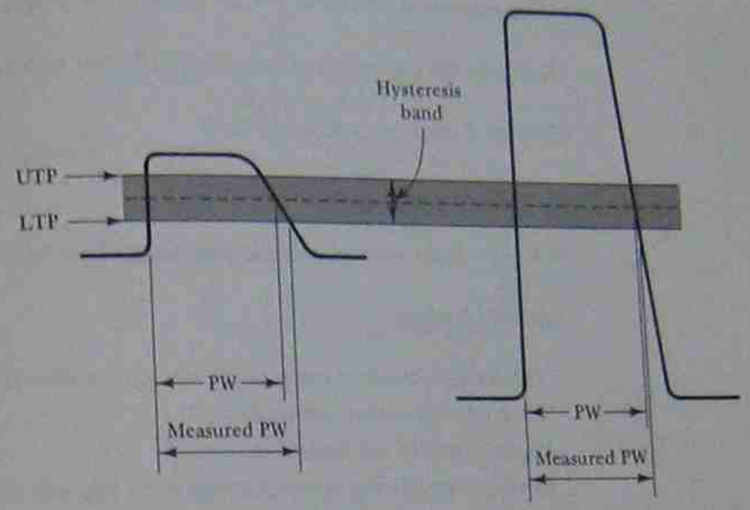


(a) 'Clean' sine wave crosses the hysteresis band twice during each cycle — triggers counting circuits once per cycle

(b) Noisy sine wave crosses hysteresis band more than twice during each cycle — produces counting errors

(c) Attenuated noisy waveform crosses hysteresis band twice in each cycle

FIGURE 10-6. Noisy input signals must be attenuated to avoid frequency counting errors.



(a) A low amplitude input pulse can produce errors in pulse width measurement

(b) Amplification of the input pulse minimizes the pulse width measurement

FIGURE 10-7. Pulses should be amplified to avoid errors in pulse width measurement by digital counter.

Figure 10-7(a) illustrates a problem that occurs when the counter is used as a timer to measure pulse width (PW). The average width of the pulse is the PW illustrated in Figure 10-7(a). However, because of the hysteresis of the Schmitt trigger circuit there is an error in the measured pulse width (see illustration). This error can be minimized either by reducing the hysteresis, or by amplifying the pulse as shown in Figure 10-7(b).

10-7 SPECIFICATIONS FOR DIGITAL COUNTER/TIMERS

The following specification statements are typical of the range of digital counter/timer instruments available today:

Frequency measurement	
Low range	10 Hz to 80 MHz
Wide range, direct measurement	dc to 1.5 GHz
Wide range with added high-frequency converter	dc to 40 GHz

Time measurement: 10 ns to 10^9 sec (approx. 31 years)

Sensitivity: Minimum input voltage 10 mV rms to 50 mV rms

Display: 7 digits to 9 digits

Accuracy: ± 1 digit ± time base error

Gate time: Time over which counting occurs 1 μs to 1 sec

Additional functions

Totalizing—count of input pulses over given time period.
Time interval—time between events.
Ratio—ratio of two input frequencies.
Scaling—producing an output frequency digitally divided from input.

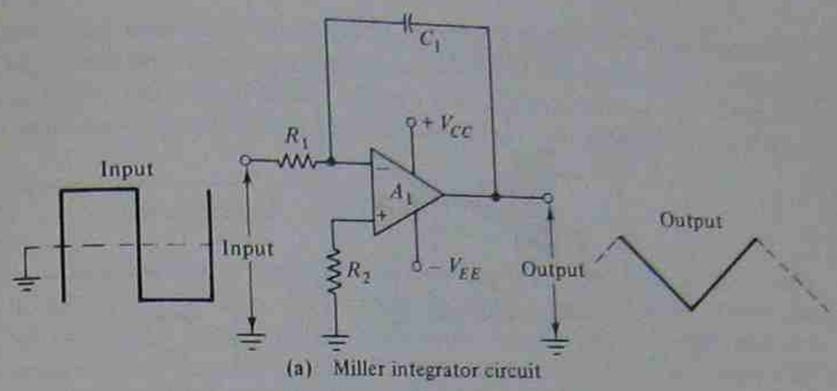
10-8 DIGITAL VOLTMETER SYSTEM

In a *digital voltmeter* (DVM), the voltage to be measured is converted into a time period. This time period is then fed to a digital counter, and the display is read as a voltage. For example, suppose an input of 1 V is converted into a time of exactly 1 sec. If the time base frequency is 1 kHz, then 1000 pulses are counted during the 1-sec time period. This is read as 1.000 V. Now, if the input goes to 1.295 V, it produces a time period of 1.295 sec, during which 1295 pulses are counted. The display is now 1.295 V. One system which accurately converts voltage into time period uses a circuit known as a *Miller integrator*.

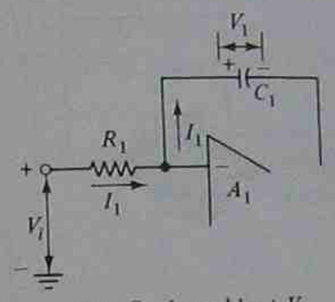
The Miller integrator circuit in Figure 10-8(a) consists of resistor R_1, capacitor C_1, and operational amplifier A_1. With no input voltage and C_1 initially uncharged, the operational amplifier behaves as a voltage follower (see Section 8-6-2) with its noninverting terminal grounded. Thus, the inverting input and the output terminal are also at ground level.

When a positive input voltage V_i is applied [Figure 10-8(b)], the op-amp inverting terminal remains at ground level, and the input current is $I_1 = V_i/R_1$. This is a *constant* current which is very much greater than the op-amp input bias current. Effectively all of I_1 flows to capacitor C_1 to charge it: + on the left-hand side and − on the right. Because the op-amp inverting terminal remains at ground level, the output decreases as C_1 charges. Also, because I_1 is constant, C_1 charges linearly producing a negative-going linear ramp output [see Figure 10-8(d)].

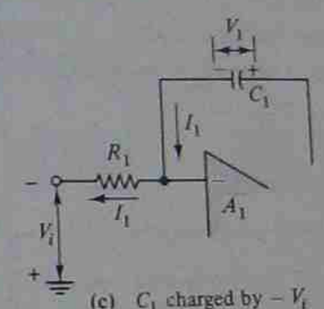
When the input voltage goes negative [Figure 10-8(c)], $I_1 = -V_i/R_1$. Once again, this a constant current which flows through C_1. Again C_1 charges at a constant rate, but now, because of the reversed current



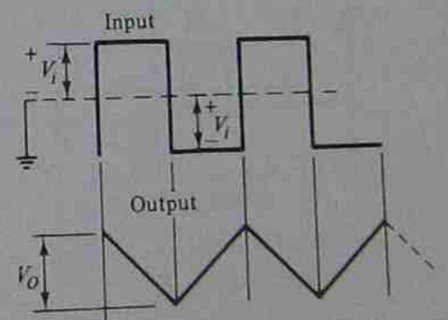
(a) Miller integrator circuit



(b) C_1 charged by $+V_i$



(c) C_1 charged by $-V_i$



(d) Input and output waveforms

FIGURE 10-8. Miller integrator circuit, C_1 charging action, and waveforms.

direction, its polarity is going + on the right and − on the left. At this time the op-amp output voltage is a linear positive-going ramp [Figure 10-8(d)].

A Miller integrator circuit is incorporated in the *dual-slope integrator* illustrated in Figure 10-9. The voltage to be measured (V_i) is applied via a voltage follower which offers a high input impedance. The voltage follower output is switched via FET Q_1 to the input of the Miller integrator. An

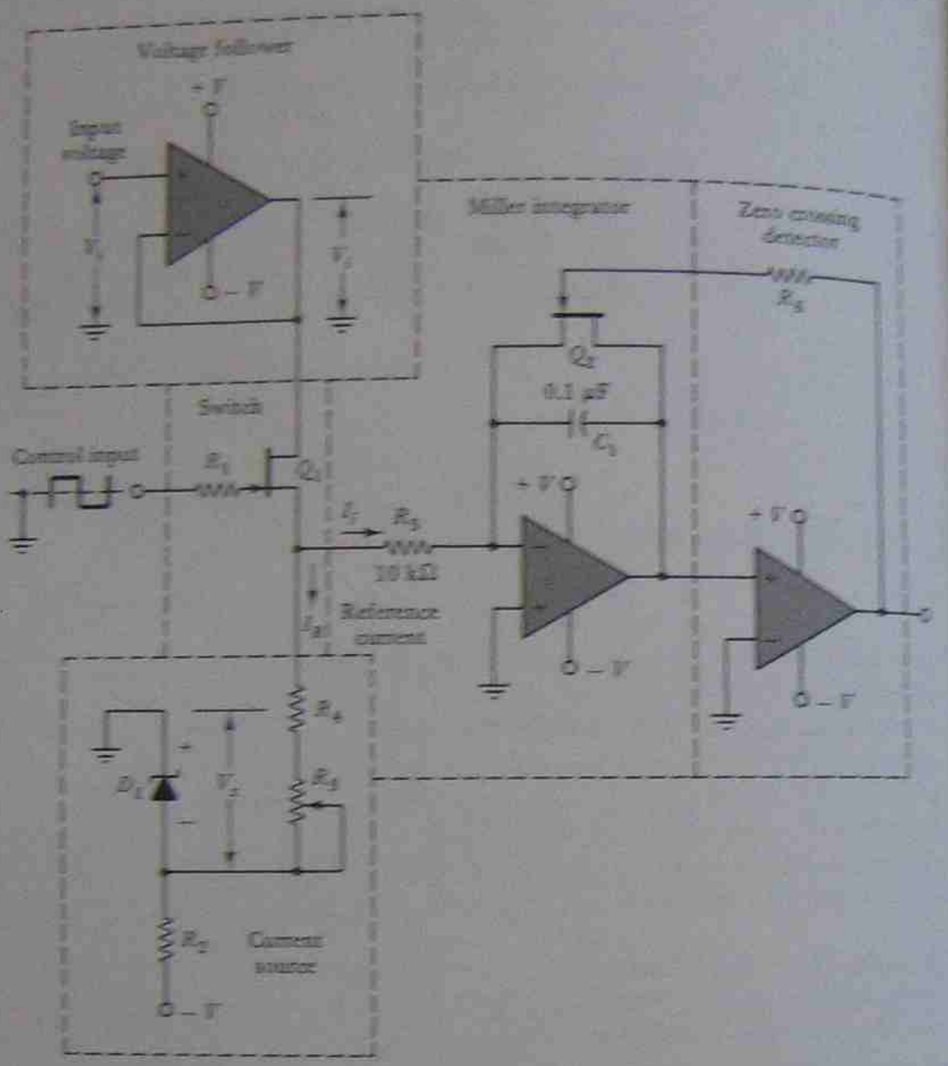


FIGURE 10-9. Dual-slope integrator.

accurate current source is also connected to the Miller integrator input, and the integrator output level is monitored by a *zero-crossing detector*. The zero-crossing detector is basically a high-gain operational amplifier. A large positive output is produced when its input is slightly above ground, and a large negative output occurs when the input is below ground level. The zero-crossing detector controls FET Q_2. When the output of the zero-crossing detector is high, Q_2 is *on* and C_1 is short-circuited. When the zero-crossing detector has a low output, Q_2 is *off* and C_1 can be charged.

The square wave input to Q_1 controls the time interval during which I_1 flows into R_3, and the time during which I_R flows out of R_3. This square

wave is generated by using decade counters to divide the output frequency of a clock source, as explained in Section 10-1. When the control input is negative, FET Q_1 is biased *off* and V_1 is isolated. During this time, the reference current flows through R_3. The level of the reference current is

$$I_R = \frac{-V_r}{R_3 + R_4 + R_5}$$

The direction of the current is such that it flows through C_1 from right to left, and C_1 tends to charge positively on the right-hand side. The output of the Miller integrator now eventually rises to ground level, and the zero-crossing detector generates a large positive output. This biases FET Q_2 *on*, and Q_2 short-circuits C_1. Therefore, at the end of the negative half of the square wave input to Q_1, capacitor C_1 is short-circuited and the Miller circuit output is held close to ground level.

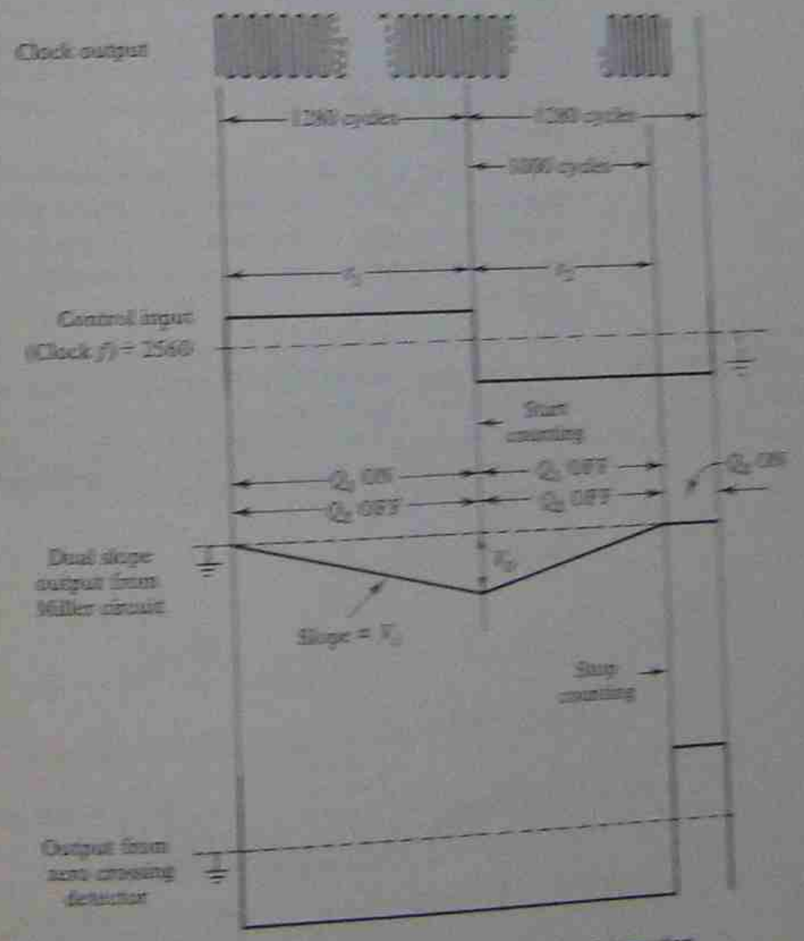


FIGURE 10-10. Waveforms for a dual-slope integrator.

Transistor Q_1 switches *on* when the square wave input becomes positive. This action connects voltage V_i to resistance R_5, and provides the input current $I_i = V_i/R_5$ to the Miller circuit. Capacitor C_1 now charges with negative polarity on the right-hand side and this produces a negative-going output from the Miller circuit (see waveforms in Figure 10-10). Consequently, the zero-crossing detector has a large negative output, which biases transistor Q_2 *off*, thus permitting C_1 to charge. The output from the Miller circuit is a linear negative ramp voltage (Figure 10-10) which continues during the positive portion of the square wave input to Q_1. Since I_i is directly proportional to V_i, the slope of the ramp is also proportional to V_i. Also, the time duration t_1 of the positive input voltage is a constant (Figure 10-10). This means that the ramp amplitude V_s is directly proportional to V_i.

When the square wave input again becomes negative, Q_1 switches *off* and the reference current I_R commences to flow through R_5 and C_1 once more. I_R discharges C_1 so that the Miller circuit output now becomes a positive-going ramp (Figure 10-10). The positive-going ramp continues until it arrives at ground level. Then the zero-crossing detector provides an output which switches Q_2 *on*, discharges C_1, and holds C_1 in short-circuit once again.

The time t_2 for the ramp voltage to climb to zero is directly proportional to V_i. Time t_2 is measured by starting the counting circuits at the negative-going edge of the square wave input to Q_1, and stopping the count at the positive-going edge of the output from the zero-crossing detector.

EXAMPLE 10-3 The dual slope integrator in Figure 10-9 has a square wave input with each half cycle equivalent to 1280 clock pulses (see Figure 10-10). The output frequency from the clock is 200 kHz. If 1000 pulses during time t_2 are to represent an input of $V_i = 1$ V, determine the required level of reference current.

SOLUTION

$$I_i = \frac{V_i}{R_5}.$$

For $V_i = 1$ V,

$$I_i = \frac{1\text{ V}}{10\text{ k}\Omega} = 100\ \mu\text{A},$$

$$\text{Clock frequency} = 200\text{ kHz},$$

$$T = \frac{1}{f} = \frac{1}{200\text{ kHz}} = 5\ \mu\text{s}.$$

If t_1 is the time duration of 1280 clock pulses;

$$t_1 = 5\ \mu\text{s} \times 1280 = 6.4\text{ ms}.$$

I_i is applied to the integrator input for a time period t_1. Since

$$C = \frac{It}{V},$$

ramp voltage

$$V_s = \frac{I_i t_1}{C_1} = \frac{100\ \mu\text{A} \times 6.4\text{ ms}}{0.1\ \mu\text{F}} = 6.4\text{ V}.$$

If t_2 is the time duration of 1000 clock pulses,

$$t_2 = 5\ \mu\text{s} \times 1000 = 5\text{ ms},$$

and I_R must discharge C_1 in time period t_2,

$$I_R = \frac{C_1 V_s}{t_2}$$

$$= \frac{0.1\ \mu\text{F} \times 6.4\text{ V}}{5\text{ ms}}$$

$$= 128\ \mu\text{A}.$$

One of the most important advantages of the dual-slope integration method is that small drifts in the clock frequency have little or no effect on the accuracy of measurements. Consider the following example: Let clock frequency = f; then time period of one cycle of clock frequency = $T = 1/f$. The time duration of 1280 clock pulses (t_1) is $1280 \times T$.

$$V_s = \frac{I_i t_1}{C_1} = \frac{100\ \mu\text{A} \times 1280T}{C_1}$$

$$t_2 = \frac{C_1 V_s}{I_R} = \left(\frac{C_1}{128\ \mu\text{A}}\right)\left(\frac{100\ \mu\text{A} \times 1280T}{C_1}\right) = 1000T.$$

The number of clock pulses during t_2 is given by

$$\frac{t_2}{\text{Time period of clock pulses}} = \frac{1000T}{T} = 1000.$$

It is seen that when the clock frequency drifts, the digital measurement of voltage is unaffected.

Figure 10-11 shows a block diagram of a DVM system employing dual slope integration. In this particular system, the clock generator has a frequency of 200 kHz. The 200 kHz is divided by a decade counter and two divide-by-sixteen counters as shown, giving a frequency of approximately 78 Hz. As already explained, this (78 Hz) is the square wave which controls the integrator. The 200-kHz clock signal, the 78-Hz square wave, and the integrator output are all fed to input terminals of a NAND gate.

The 200-kHz clock output acts as a triggering signal to the counting circuitry when the other two inputs to the NAND gate are high. This occurs during time t_2, as illustrated in Figure 10-10. The integrator output

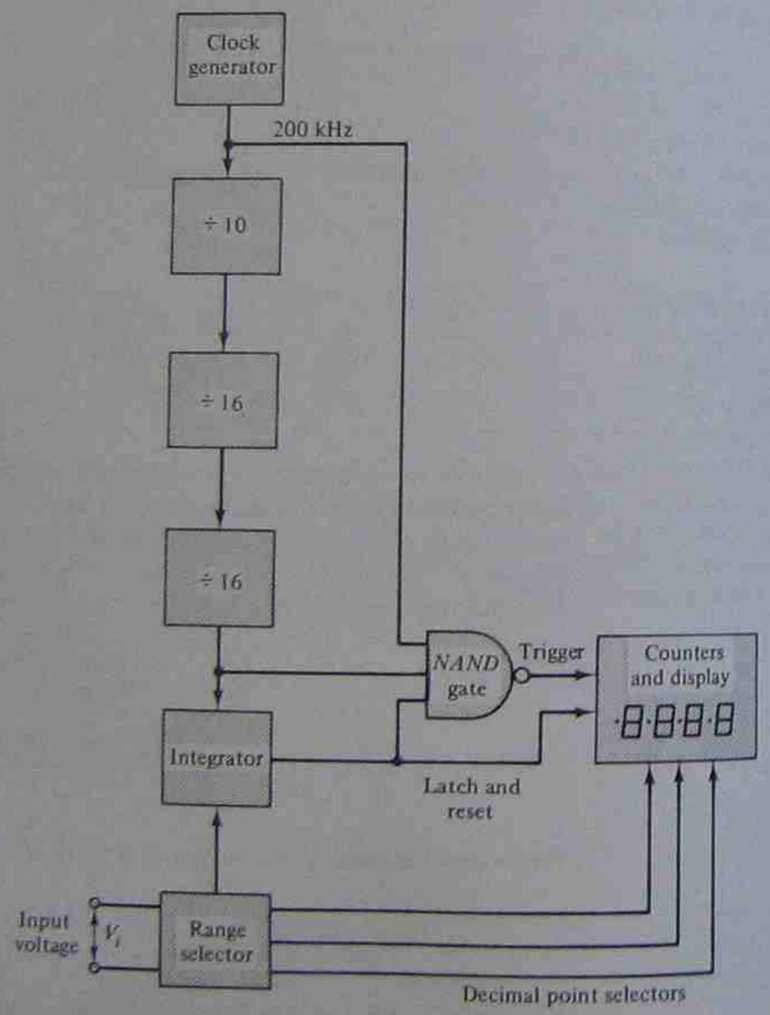


FIGURE 10-11. Digital voltmeter system.

(i.e., zero-crossing detector output) is also used to reset the counting circuits and to control the latch. The counting circuits are reset at the beginning of time period t_1. Counting commences at the start of t_2. The latch is switched *on* at the end of t_2 in order to set the displays according to the counting circuits.

The range selector is adjusted to suit the input voltage. An input of less than 1 V is applied directly to the integrator, and a decimal point is selected so that the display can indicate a maximum of .9999 V. An input voltage between 1 V and 10 .V is first potentially divided by 10 and applied to the integrator again as a voltage less than 1 V. In this case the decimal point is selected so that the display can indicate a maximum of 9.999 V. An input voltage between 10 V and 100 V is reduced by a factor of 100 before passing to the integrator. Decimal point selection now allows the meter to indicate a maximum of 99.99 V.

Some DVMs employ *automatic ranging circuits*. These determine the approximate level of the input voltage, and trigger transistor switches to select the appropriate time base and decimal point position.

10-9 DIGITAL MEASUREMENT OF CURRENT RESISTANCE AND AC QUANTITIES

The method used in digital instruments to convert current and resistance into measurable voltage levels are similar to those employed in analog electronic instruments. As explained in Section 8-10 for analog instruments, shunts are used for digital current measurements. The digital display is identified as mA, μA, etc. For very low current ranges, relatively high shunt resistances are used, and this must be taken into account when connecting the meter into a circuit.

In digital instruments, resistance must be converted into direct voltage by a linear method such as that described in Section 8-8-3. The voltage is then measured digitally and displayed as kΩ or MΩ.

Alternating voltage and current must be converted into dc quantities either by rectification or by a true rms method, as discussed in Section 8-9. Once again as in the case of analog instruments, where rectification is used the digital meter readings are true only for pure sine waves. When true rms conversion techniques are used, the instrument indicates the true rms measurement no matter what the waveform.

10-10 DIGITAL MULTIMETER

Perhaps the most important feature of a *digital multimeter* (DMM) compared to an analog instrument is the direct digital indication of the measurement. With analog instruments the pointer position must be carefully read to avoid parallax, and the range must be noted to avoid misreading. Neither of these are necessary with a digital instrument.

Furthermore, with a deflection instrument the exact pointer position cannot be determined more accurately than to about ±0.3% of full scale. Digital instruments, on the other hand, can give readings with three or more decimal places. Thus, a digital instrument has better *resolution* than an analog instrument.

Many DMMs have automatic ranging circuits which select the most appropriate range. When the range is selected manually, greatest accuracy is achieved by using a range that gives the largest possible numerical display. This is the same as adjusting the range of analog instruments for the greatest on-scale pointer deflection. For example, a display of 1.933 V is obviously more accurate than a display of 001.9 V. When the selected range is too low, the display usually *blanks*, or flashes on and off continuously.

Another very important advantage of digital instruments over analog is that digital instruments are by far the most accurate. Good quality analog voltmeters have ±1% accuracy, while even the least expensive DVMs have a typical accuracy of ±0.5%. Good quality digital instruments have ±0.1% or better accuracy.

Digital instrument accuracy is usually stated as ±(0.1% rdg + 1 d). This means ±(0.1% of reading +1 digit). The 1 digit refers to the right-hand numeral of the display. The maximum error in a 1.500-V reading on a $3\frac{1}{2}$-digit display would be

$$\begin{aligned}\text{error} &= \pm\,[(0.1\%\text{ of }1.5\text{ V}) + 0.001\text{ V}]\\ &= \pm\,(0.0015\text{ V} + 0.001\text{ V})\\ &= \pm 0.0025\text{ V}\\ &\simeq \pm\,(0.17\%\text{ of }1.5\text{ V}).\end{aligned}$$

The following specification statements are typical of currently available digital multimeters:

Display

$3\frac{1}{2}$ and $4\frac{1}{2}$ digit

dc voltage

range 0.1 V to 1000 V
accuracy ±(0.1% rdg + 1 d)
input resistance 10 MΩ

ac Voltage

range 0.1 V to 1000 V rms
accuracy ±(0.6% rdg + 10 d)
frequency range 10 Hz to 10 kHz
input resistance 10 MΩ

dc Current

range 100 mA to 10 A
accuracy ±(1% rdg +10 d)
shunt resistance 0.1 Ω to 1 kΩ

ac Current

range 100 mA to 10A
accuracy ±(2% rdg + 15 d)
shunt resistance 0.1 Ω to 1 kΩ

Resistance

range 1 kΩ to 11 MΩ
accuracy ±(0.6% rdg + 10 d)
open-circuit terminal voltage 5 V

Various probes are available for extending the ranges of digital multimeters. Some of these are:

- *50 A shunt* extends current measurements to 50 A
- *High voltage probe* extends voltage range to 40 kV
- *RF probe* extends frequency range to 100 MHz
- *Clamp-on ac current probe* extends ac current range to 200 A rms.

The controls and terminals of a representative laboratory type DMM are shown in Figure 10-12. The function and range selections are performed by push-button controls. Starting from the left-hand side, the first button is a power *on / off* switch. The next five buttons are for function selection: AC/DC, *LO / HI* (resistance range), Ω, V, and A. The five right-hand buttons are for range selection. To use the instrument, switch *on* the power, select the appropriate function and range, connect the source to be measured, and read the display.



FIGURE 10-12. Front panel of digital multimeter (Courtesy of Keithley Instruments Inc.).

The input terminals are identified as LO (*low*) and HI (*high*). Some DMMs have more than two terminals (for example, there may be an additional resistance or current terminal). On these instruments the *low* terminal is identified as COM (*common*) terminal. In all cases the *low* or *common* terminal should be connected to any ground point in a circuit where measurements are being made. Also, when more than one electronic instrument is connected in a circuit the *low* or *common* terminals should all be connected to one point in the circuit. As explained in Section 8-3-3, this is because the *low* or *common* terminal is usually grounded via a capacitor within the instrument.

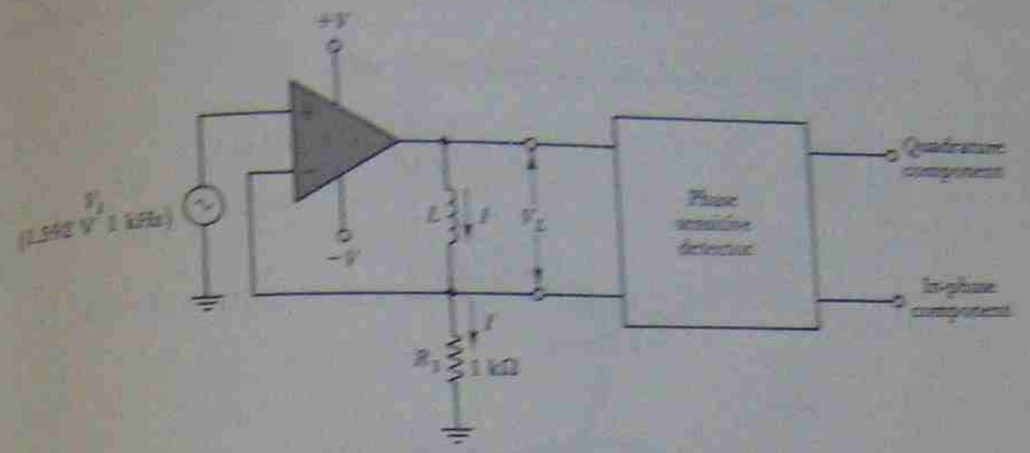
When measuring quantities which have a negative polarity with respect to the *low* terminal, a negative sign is displayed beside the digital indication. For the instrument in Figure 10-12, the absence of a polarity sign indicates a positive polarity. If the selected range is too low for the applied voltage or current, the display flashes 0000.

Analog instruments must be *zeroed* before use, and the same is true of many digital instruments. For the instrument illustrated in Figure 10-12, the zeroing procedure is: select the resistance function, short the terminals together, adjust the slot-headed *zero* control until the display indicates zero.

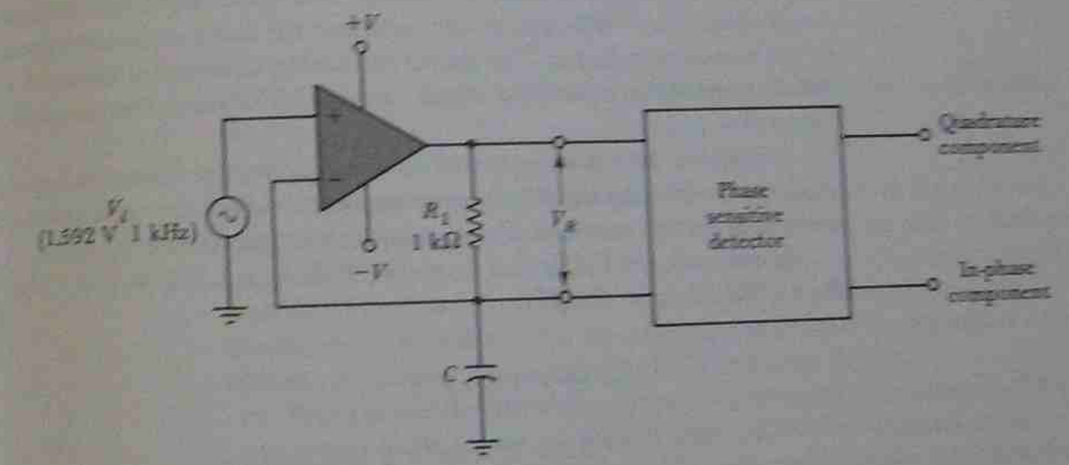
10-11 DIGITAL LCR MEASUREMENTS

As in the case of the resistance measuring techniques described in Section 8-8-3, inductive and capacitive impedances are first converted into voltages before measurement. Figure 10-13 illustrates the basic method.

In Figure 10-13(a) an ac voltage is applied to the noninverting input terminal of the operational amplifier. The input voltage is developed across resistor R_1 to give a current: $I = V_i/R_1$. This current also flow through the inductor giving a voltage drop: $V_L = IX_L$. If $V_i = 1.592$ V,



(a) Linear conversion of inductive impedance into voltage



(b) Linear conversion of capacitive impedance into voltage

FIGURE 10-13. Basic circuits for converting inductive and capacitive impedances into voltage components for digital measurement.

$f = 1$ kHz, $R_1 = 1$ kΩ, and $L = 100$ mH:

$$I = \frac{V_1}{R_1} = \frac{1.592\text{ V}}{1\text{ k}\Omega} = 1.592\text{ mA},$$

and

$$V_L = I(2\pi fL) = 1.592\text{ mA} \times 2\pi \times 1\text{ kHz} \times 100\text{ mH}$$
$$= 1\text{ V(rms)},$$

when

$L = 200$ mH, $V_L = 2$ V; when $L = 300$ mH, $V_L = 3$ V; etc.

It is seen that the voltage developed across L is directly proportional to the inductive impedance. A *phase sensitive detector* [Figure 10-13(a)] is employed to resolve the inductor voltage into quadrature and in-phase components. These two components represent the series equivalent circuit of the measured inductor. The digital measuring circuits are arranged to measure the series equivalent circuit inductance L_s and the dissipation factor $D = 1/Q$.

Capacitive impedance is treated in a similar way to inductive impedance, except that the input voltage is developed across the capacitor and the output voltage is measured across the resistor [see Figure 10-13(b)].

In this case $I = V_1/X_c$, and $V_R = IR$. With $V_1 = 1.592$ V, $f = 1$ kHz, $R_1 = 1$ kΩ, and $C = 0.1$ μF:

$$I = \frac{V_1}{X_c} = V_1(2\pi fC)$$
$$= 1.592\text{ V} \times 2\pi \times 1\text{ kHz} \times 0.1\ \mu\text{F}$$
$$= 1\text{ mA},$$

and

$$V_R = IR = 1\text{ mA} \times 1\text{ k}\Omega$$
$$= 1\text{ V (rms)},$$

when $C = 0.2$ μF, $V_R = 2$ V; when $C = 0.3$ μF, $V_R = 3$ V, etc.

The voltage developed across R is directly proportional to the capacitive impedance. The phase sensitive detector [Figure 10-13(b)] resolves the resistor voltage into quadrature and in-phase components, which in this case are proportional to the capacitor current. The displayed capacitance measurement is that of the parallel equivalent circuit (C_p). The dissipation factor (D) of the capacitor is also displayed.

The digital LCR meter shown in Figure 10-14 can measure *inductance*, *capacitance*, *resistance*, *conductance*, and *dissipation factor*. The desired function is

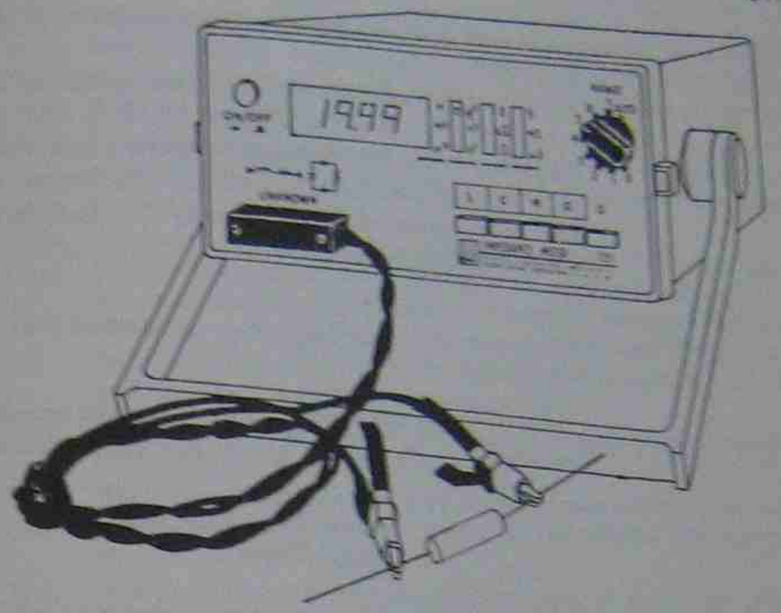


FIGURE 10-14. Digital LCR meter (Courtesy of Electro Scientific Industries, Inc.).

selected by push button. The range switch is normally set to the automatic (AUTO) position for convenience. However, when a number of similar measurements are to be made, it is faster to use the appropriate range instead of the automatic range selection. The numerical value of the measurement is indicated on the 3½-digit display, and the multiplier and measured quantity are identified by LED indicating lamps.

Four (*current* and *potential*) terminals are provided for connection of the component to be measured. (See Section 6-4 for four-terminal measurements.) For general use each pair of current and voltage terminals are joined together at two spring clips which facilitate quick connection of components. A ground terminal for guard-ring type measurements (see Section 6-5) is provided at the rear of the instrument. The ground terminal together with the other four terminals is said to give the instrument *five-terminal measurement* capability. *Bias terminals* are also available at the rear of the instrument, so that a bias current can be passed through an inductor or a bias voltage applied to a capacitor during measurement.

For R, L, C, and G, typical measurement accuracies are $\pm[0.25\% + (1 + 0.002\ R, L, C,$ or $G)$ digits]; for D the measurement accuracy is $\pm(2\% + 0.010)$.

Resistance measurements may be made directly on the digital LCR instrument in Figure 10-14, over a range of 2 Ω to 2 MΩ. Conductance is measured directly over a range of 2 μS to 20 S. Resistances between 2 MΩ and 1000 MΩ can be measured as conductances, and the resistance

calculated: $R = 1/G$. For example, a resistance of 10 MΩ is measured as 0.100 μS.

Inductance and capacitance measurements may be made directly over a range of 200 μH to 200 H, and 200 pF to 2000 μF, respectively. The dissipation factor D is measured by pressing and holding in the D button while the L or C button is still selected. The directly measured inductance is the series equivalent circuit quantity L_s. The Q factor of the inductor is calculated as the reciprocal of D:

$$Q = \frac{\omega L_s}{R_s} = \frac{1}{D} \text{ (see Section 7-4).}$$

Direct capacitance measurements give the parallel equivalent circuit quantity C_p. In this case D (for the parallel equivalent CR circuit) is:

$$D = \frac{1}{\omega C_p R_p} \text{ (see Section 7-4).}$$

When measuring low values of resistance or inductance, the connecting clips should first be shorted together and the residual R or L values noted (as indicated digitally). These values should then be subtracted from the measured value of the component. When measuring low capacitances, the connecting clips should first be placed as close together as the terminals of the component to be measured (i.e., without connecting the component). The indicated residual capacitance is noted and then subtracted from the measured component capacitance.

Return to Figure 10-13(a) and assume that a capacitor is connected in place of the inductor. The measured quantity is displayed as an inductance prefixed by a negative sign on the LCR meter in Figure 10-14. The capacitive impedance is equivalent to the impedance of the indicated inductance:

$$\omega L_s = \frac{1}{\omega C_s},$$

or

$$C_s = \frac{1}{\omega^2 L_s}.$$

For an indicated inductance of 100 mH, and a measuring frequency of 1 kHz,

$$C_s = \frac{1}{(2\pi \times 1 \text{ kHz})^2 \times 100 \text{ mH}} = 0.25 \ \mu\text{F}.$$

Similarly, inductance can be measured as capacitance when it is convenient to do so.

REVIEW QUESTIONS AND PROBLEMS

10-1. Sketch the block diagram of a time base system for a digital frequency meter. Starting with a 1-MHz crystal controlled oscillator, show the time periods of the output waveforms at various points in the system. Briefly explain.

10-2. If the time base system in Question 10-1 has the 1-MHz oscillator replaced with a 3.3-MHz oscillator, calculate the new time periods at each output terminal.

10-3. A square wave is applied to a digital frequency meter that uses a time base consisting of a 1-MHz clock generator which has its output divided by decade counters. Determine the meter indication when: (a) the square wave frequency is 5 kHz and the time base uses six decade counters, (b) the square wave frequency is 2.9 kHz and the time base uses five decade counters.

10-4. Explain the function of a latch and a display-enable control as used with a frequency counter.

10-5. Sketch the block diagram of a digital frequency meter. Also sketch the waveforms at various points in the system, and carefully explain the system operation.

10-6. A frequency meter with a stated accuracy of ±1 count ±(1×10^{-5}) is used to measure frequencies of 30 Hz, 30 MHz, and 300 MHz. Calculate the percentage measurement error in each case.

10-7. Sketch a block diagram of the input stages of a digital frequency meter arranged for reciprocal counting. Explain the system operation.

10-8. The frequency meter in Question 10-6 is rearranged for reciprocal counting. Calculate the percentage error that occurs when a 30-Hz frequency is measured on this system.

10-9. Explain how time period and frequency ratio can be measured on a digital frequency meter. Use illustrations in your explanation.

10-10. Using illustrations, discuss the need for an input amplifier/attenuator stage with a digital frequency meter. Explain the situation where (a) amplification and (b) attenuation is required to avoid errors.

10-11. Sketch the circuit of an IC op-amp Miller integrator. Briefly explain the circuit operation, and sketch input and output waveforms.

10-12. Sketch the circuit of a dual-slope integrator. Sketch the waveforms that occur at the various points throughout the circuit. Identify each part of the circuit, and carefully explain the circuit operation.

10-13. A dual-slope integrator, as shown in Figure 10-9, has a square wave input with each half-cycle equivalent to 1563 clock pulses. The clock output frequency is 1 MHz. During time t_2 (in Figure 10-10), 1000 pulses are to represent $V_i = 1$ V. Calculate the required level of reference current.

10-14. Show that small drifts in clock frequency have little effect on the accuracy of a dual-slope integrator system for use with a digital voltmeter.

10-15. Sketch the block diagram of a digital voltmeter system, and explain its operation.

10-16. Discuss digital measurement of current, resistance, and ac quantities.

10-17. Discuss the typical accuracy specification for a digital voltmeter, and compare it to analog voltmeter specifications.

10-18. Sketch the basic circuits for converting inductive and capacitive impedances into quadrature and in-phase components for digital measurement. Carefully explain the operation of each circuit.

11

CATHODE-RAY OSCILLOSCOPES

INTRODUCTION

The cathode ray oscilloscope consists of a *cathode ray tube* (CRT) and its associated control and input circuitry. The CRT is a vacuum tube in which electrons generated at a heated cathode are shaped into a fine beam and accelerated toward a fluorescent screen. The screen glows at the point at which the electron beam strikes. The electron beam is easily deflected vertically and horizontally across the screen by voltages applied to deflecting plates. Usually, the beam is swept horizontally across the screen by a ramp voltage generated by a *time base* circuit, and a changing input voltage is applied to deflect the beam vertically. This results in a display of the waveform (voltage versus time) of the input voltage. Most oscilloscopes are dual trace instruments, capable of simultaneously displaying two waveforms.

The oscilloscope is the basic instrument for the study of all types of waveforms. It can be employed to measure voltage, frequency and phase difference. Many other quantities such as pulse width, rise time and delay time can all be investigated. The characteristics of electronic devices can also be displayed on an oscilloscope screen.

11-1 THE CATHODE-RAY TUBE

The basic construction and biasing of a cathode-ray tube are shown in Figure 11-1. The system of electrodes is contained in an evacuated glass tube with a viewing screen at one end. A beam of electrons is generated by

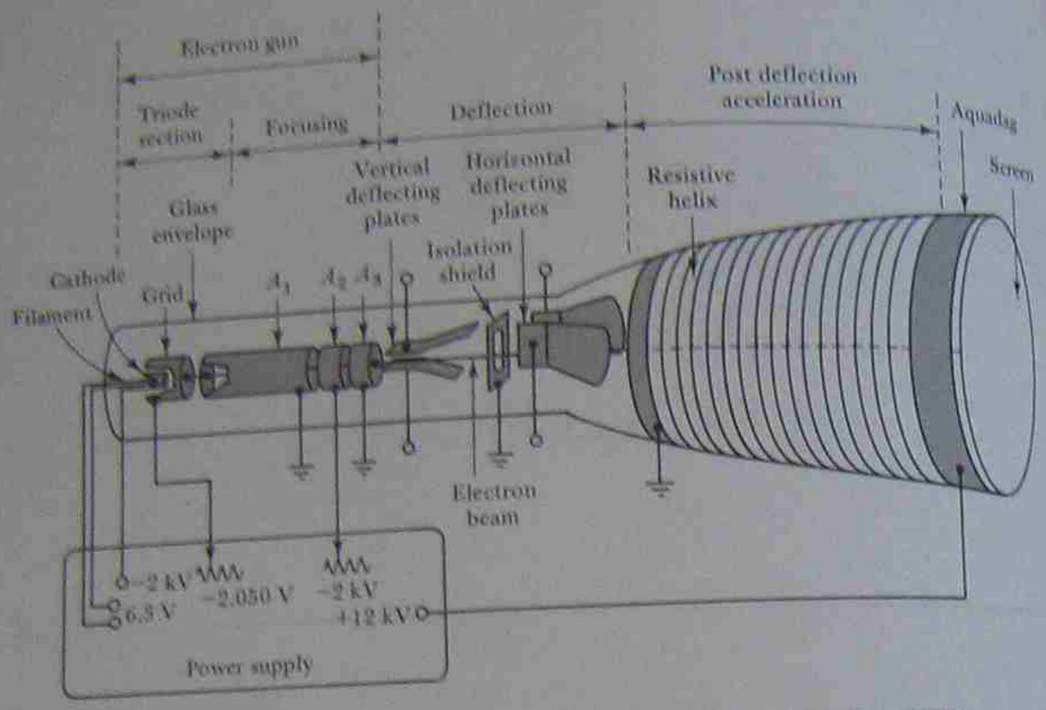


FIGURE 11-1. Basic construction and biasing of CRT.

11-1-1 General

the cathode and directed to the screen, causing the phosphor coating on the screen to glow where the electrons strike. The electron beam is deflected vertically and horizontally by externally applied voltages.

11-1-2 The Triode Section

The triode section of the tube consists of a *cathode*, a *grid*, and an *anode*, which are all substantially different in construction from the usual electrodes in a triode vacuum tube. The grid, which is a nickel cup with a hole in it (see Figure 11-1), almost completely encloses the cathode. The cathode, also made of nickel, is cylinder shaped with a flat, oxide-coated, electron-emitting surface directed toward the hole in the grid. Cathode heating is provided by an inside filament. The cathode is typically held at approximately −2 kV, and the grid potential is adjustable from approximately −2000 V to −2050 V. The grid potential controls the electron flow from the cathode and thus controls the number of electrons directed to the screen. A large number of electrons striking one point will cause the screen to glow brightly; a small number will produce a dim glow. Therefore, the grid potential control is a *brightness control*.

The first anode (A_1) is cylinder shaped, open at one end and closed at the other end, with a hole at the center of the closed end. Since A_1 is grounded and the cathode is at a high negative potential, A_1 is highly

positive with respect to the cathode. Electrons are accelerated from the cathode through the holes in the grid and anode to the focusing section of the tube.

11-1-3 The Focusing System

The focusing electrodes A_1, A_2, and A_3 are sometimes referred to as an *electron lens*. Their function is to focus the electrons to a fine point on the screen of the tube. A_1 provides the accelerating field to draw the electrons from the cathode, and the hole in A_1 limits the initial cross section of the electron beam. A_3 and A_1 are held at ground potential while the A_2 potential is adjustable around −2 kV. The result of the potential difference between anodes is that *equipotential lines* are set up as shown in Figure 11-2. These are lines along which the potential is constant. Line 1, for example, might have a potential of −700 V along its entire length, while the potential of line 2 might be −500 V over its whole length. The electrons enter A_1 as a divergent beam. On crossing the equipotential lines, however, the electrons experience a force which changes their direction of travel toward right angles with respect to the equipotential lines. The shape of the lines within A_1 produces a convergent force on the divergent electron beam, and those within A_3 produce a divergent force on the beam. The convergent and divergent forces can be altered by adjusting the potential on A_2. This adjusts the point at which the beam is focused. A_2 is sometimes referred to as the *focus ring*. Figure 11-2 is a two-dimensional representation of a three-dimensional apparatus, so there are really equipotential *planes* rather than equipotential *lines*.

The negative potential on A_2 tends to slow down the electrons, but they are accelerated again by A_3, so that the beam speed leaving A_3 is the same as when entering A_1. The electrons are travelling at a constant velocity as they pass between the deflecting plates.

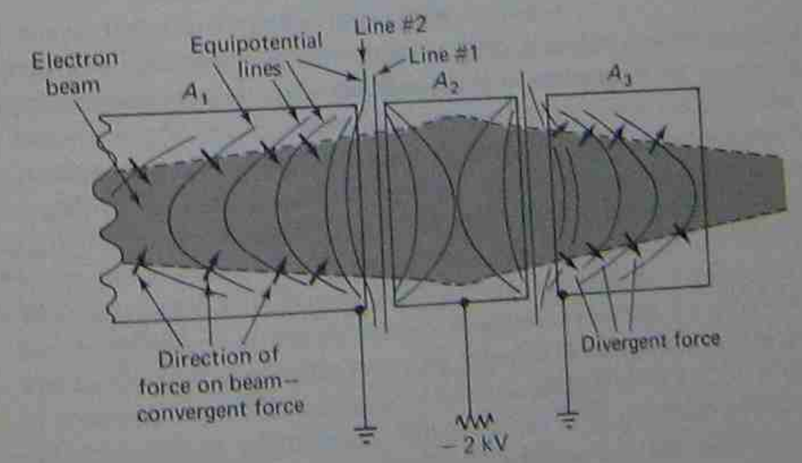


FIGURE 11-2. Electrostatic focusing.

11-1-4 Deflection Section

If the horizontal and vertical deflecting plates were grounded, or left unconnected, the beam of electrons would pass between each pair of plates and strike the center of the oscilloscope screen. There they would produce a bright glowing point. When one plate of a pair of deflecting plates has a positive voltage applied to it, and the other one has a negative potential, the electrons in the beam are attracted towards the positive plate and repelled from the negative plate. The electrons are actually accelerated in the direction of the positive plate. However, since they are travelling axially between the plates, no electrons ever strike a deflecting plate. Instead, the beam is deflected so that the electrons strike the screen at a new position.

Consider the electrostatic deflection illustration in Figure 11-3. When the potential on each plate is zero, the electrons passing between the plates do not experience any deflecting force. When the upper plate potential is $+E/2$ volts and the lower potential is $-E/2$, the potential difference between the plates is E volts. The (negatively charged) electrons are attracted toward the positive plate and repelled from the negative plate. The beam could be deflected by grounding one plate and applying a positive or negative potential to the other plate. In this case, the potential at the center of the space between the plates would be greater or less than zero volts. This would cause horizontal acceleration or deceleration of the electrons, thus altering the beam speed. Equal positive and negative deflecting voltages would then not produce equal deflections. With $+E/2$ volts on one plate and $-E/2$ on the other plate, the center potential in the space between plates is zero volts, and the beam speed is unaffected. The tube sensitivity to deflecting voltages can be expressed in two ways. The voltage required to produce one division of deflection at the screen (V/cm) is referred to as the *deflection factor* of the tube. The deflection produced by 1 V (cm/V) is termed the *deflection sensitivity*.

When an alternating voltage is applied to the deflecting plates, the beam is deflected first in one direction, and then in the other. This produces a horiztonal line when the ac voltage is applied to the horizontal

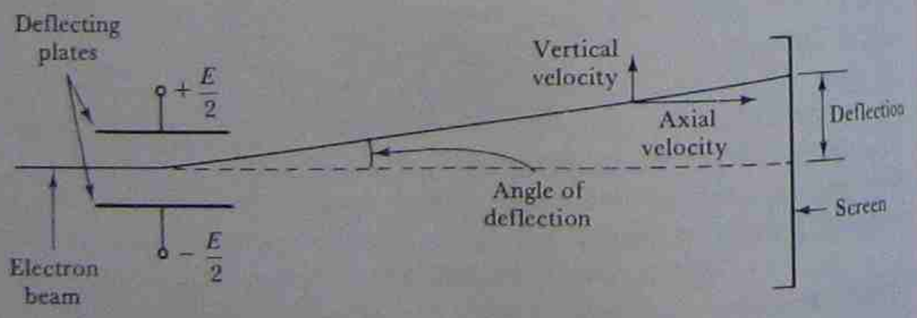


FIGURE 11-3. Electrostatic deflection.

plates, and a vertical line when the vertical deflection plates are involved. In Section 11-3 it is explained that the waveform to be displayed is applied via an amplifier to the vertical deflecting plates, and that the horizontal plates normally have a ramp waveform.

A grounded *isolation shield* is situated between the vertical and horizontal deflecting plates (see Figure 11-1). This prevents the electric fields from one set of plates from influencing the other pair of plates.

11-1-5 The Screen

The screen of a CRT is formed by placing a coating of phosphor materials on the inside of the tube face. When the electron beam strikes the screen, electrons within the screen material are raised to a higher energy level and emit light as they return to their normal levels. The glow may persist for a few milliseconds, for several seconds, or even longer. Depending upon the materials employed, the color of the glow produced at the screen may be blue, red, green, or white.

The phosphors used on the screen are insulators, and, but for secondary emission, the screen would develop a negative potential as the primary electrons accumulate. The negative potential would eventually become so great that it would repel the electron beam. The secondary electrons are collected by a graphite coating termed *aquadag* around the neck of the tube (see Figure 11-1), so that the negative potential does not accumulate on the screen. In another type of tube, the screen has a fine film of aluminum deposited on the surface at which the electrons strike. This permits the electron beam to pass through, but collects the secondary electrons and conducts them to ground. The aluminum film also improves the brightness of the glow by reflecting the emitted light toward the glass. A further advantage of the film is that it acts as a *heat sink*, conducting away heat that might otherwise damage the screen.

11-1-6 Brightness of Display

As has already been explained, the brightness of the glow produced at the screen is dependent upon the number of electrons making up the beam. Since the grid controls the electron emission from the cathode, the grid voltage control is a brightness control. Brightness also depends upon beam speed; so for maximum brightness the electrons should be accelerated to the greatest possible velocity. However, if the electron velocity is very high when passing through the deflection plates, the deflecting voltages will have a reduced influence, and the deflection sensitivity will be poor. It is for this reason that *post deflection acceleration* is provided; i.e., the electrons are accelerated again after they pass between the deflecting plates. A helix of resistive material is deposited on the inside of the tube from the deflecting plates to the screen (Figure 11-1). The potential at the screen end of the helix might be typically +12 kV and at the other end 0 kV.

Thus, the electrons leaving the deflecting plates experience a continuous accelerating force all the way to the screen, where they strike with high energy.

11-2 DEFLECTION AMPLIFIERS

Any voltage that is to produce deflection of the electron beam must be converted into two equal and opposite voltages, $+E/2$ and $-E/2$, as explained in Section 11-1-4. This requires an amplifier which accepts an (ac or dc) input and provides *differential* outputs. The basic circuit of such an amplifier is illustrated in Figure 11-4. Transistors Q_2 and Q_3 form an emitter-coupled amplifier (already discussed in Section 8-5-1). Q_1 and Q_4 are emitter followers to provide high input resistance.

When the input voltage to the attenuator is zero, the base of Q_1 is at ground level. If Q_4 base is also adjusted to ground level, Q_2 and Q_3 bases are both at the same negative potential with respect to ground ($-V_{B2} = -V_{B3}$). Also, $I_{C2} = I_{C3}$, and the voltage drops across R_3 and R_6 set the collectors of Q_2 and Q_3 at ground level. These collectors are the amplifier outputs, and they are connected directly to the deflection plates.

The moving contact of potentiometer R_4 should normally be situated equidistant from each end. When the moving contact is moved left, there is less resistance in the emitter circuit of Q_2 and more resistance in Q_3 emitter circuit. Q_2 now passes more collector current than Q_3, and the dc voltage at the collector of Q_2 falls while that at Q_3 collector rises. When the moving contact of R_4 is moved past center towards Q_3 emitter, the reverse effect occurs. Thus, R_4 functions as a *balance control*, to balance (or equalize) the differential outputs of the amplifier.

An input voltage which is to produce vertical deflection is coupled to the *attenuator* of the amplifier feeding the vertical plates (see Figure 11-4). The attenuated voltage appears at the base of transistor Q_1, where it is further attenuated (via R_1 and R_2) and then applied to Q_2 base. A positive-going input produces a positive-going voltage at Q_2 base, and causes I_{C2} to increase and I_{C3} to decrease. The I_{C2} increase causes output V_{C2} to fall below its normal ground level, and the I_{C3} decrease makes V_{C3} rise above ground. If the change in V_{C2} is $\Delta V_{C2} = -1$ V, then $\Delta V_{C3} = +1$ V. When the input to the attenuator is a negative-going quantity, I_{C2} decreases and I_{C3} increases. Now, ΔV_{C2} is positive and ΔV_{C3} is an equal and opposite negative voltage.

Where the amplifier is used with the vertical deflection plates, the attenuator resistors are selected to produce a wide range of deflection sensitivity. At the most sensitive position of the attenuator switch (least attenuation), a 2-mV input typically produces one division of deflection on the screen. At the greatest attenuation position of the switch, a 10-V input is required to produce one division of deflection. The input to the attenuator may be capacitor coupled (ac) or direct coupled (dc), according to the selected position of switch S_1 in Figure 11-4.

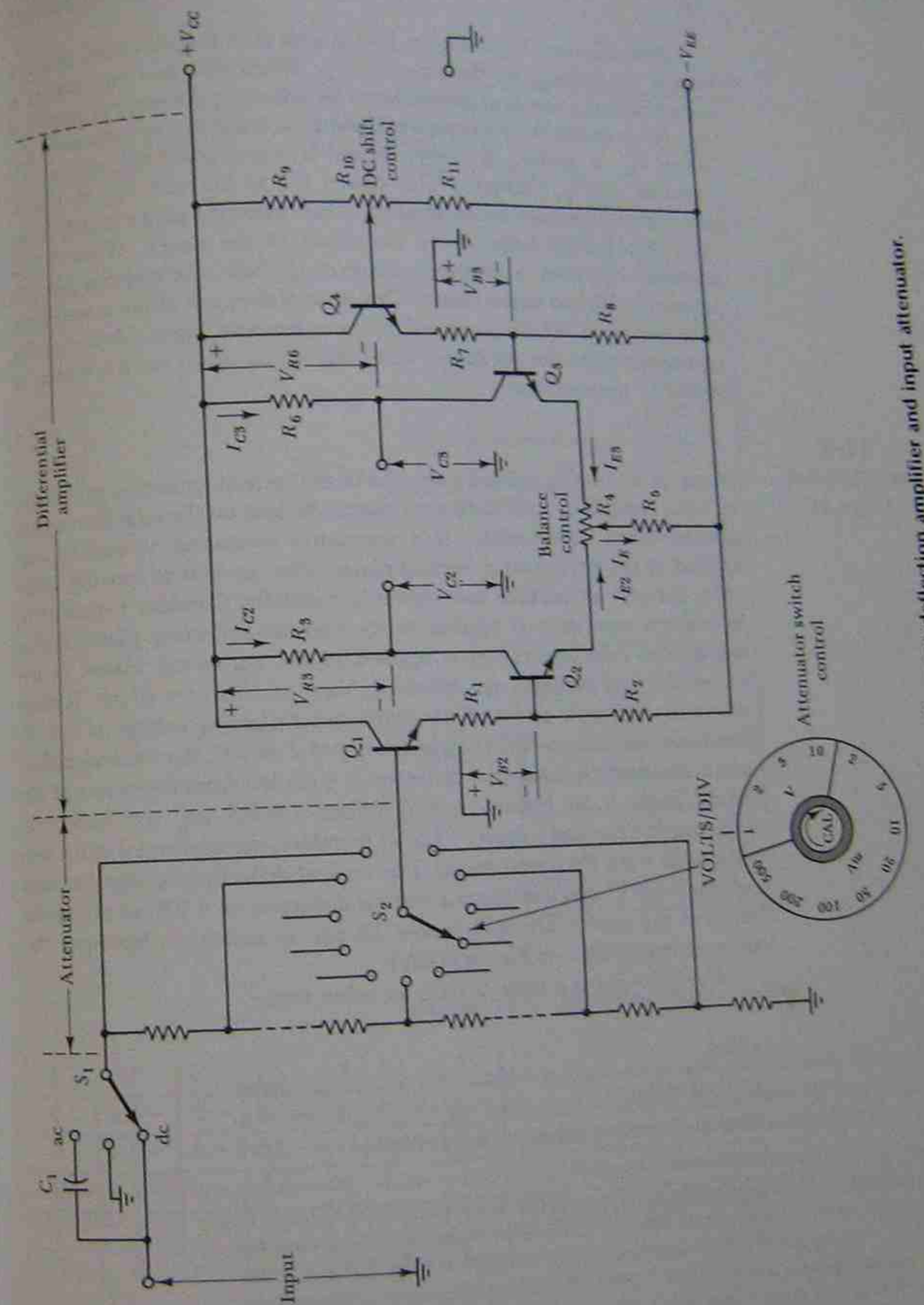


FIGURE 11-4. Basic circuit of oscilloscope deflection amplifier and input attenuator.

Potentiometer R_{10} in Figure 11-4 is a dc shift control which serves to adjust the voltage at the base of Q_4. When the moving contact is centralized, Q_4 base is at ground level. By adjusting the moving contact of R_{10}, either a positive or a negative dc potential is applied to the base of Q_4. When V_{B4} is positive, Q_3 base voltage is raised positively, so that I_{C3} increases and I_{C2} decreases. This causes V_{C3} to fall and V_{C2} to rise. A differential dc voltage is thus applied to the deflecting plates to deflect (or *shift*) the electron beam above the center of the screen. When R_{10} is adjusted to produce a negative voltage at Q_4 base, the electron beam is adjusted below the screen center. This dc shift does not affect a waveform to be displayed, which is applied to the attenuator input. However, R_{10} adjustment shifts the displayed waveform up or down on the screen as desired by the operator.

11-3 WAVEFORM DISPLAY

When an alternating voltage is applied to the vertical deflecting plates and no input is applied to the horizontal plates, the spot on the tube face moves up and down continuously. If a constantly increasing voltage is also applied to the horizontal deflecting plates, then, as well as moving vertically, the spot on the tube face moves horizontally. Consider Figure 11-5, in which a sine wave is applied to the vertical deflecting plates and a *sawtooth* (or repetitive ramp) is applied to the horizontal plates. If the waveforms are perfectly synchronized, then at time $t = 0$ the vertical deflecting voltage is zero and the horizontal deflecting voltage is -2 V. Therefore, assuming a deflecting sensitivity of 2 cm/V, the vertical deflection is zero and the horizontal deflection is 4 cm left from the center of the screen [point 1 on Figure 11-5(c)]. When $t = 0.5$ ms, the horizontal deflecting voltage has become -1.5 V; therefore, the horizontal deflection is 3 cm left from the screen center. The vertical deflecting voltage has now become $+1.4$ V, and this causes a vertical deflection of $+2.8$ cm above the center of the screen. The spot is now 2.8 cm up and 3 cm left from the screen center, point 2 on Figure 11-5(c).

The following is a table of data for other times:

t (ms)	1	1.5	2	2.5	3	3.5	4
vertical voltage (V)	+2	+1.4	0	−1.4	−2	−1.4	0
vertical deflection (cm)	+4	+2.8	0	−2.8	−4	−2.8	0
horizontal voltage (V)	−1	−0.5	0	+0.5	+1	+1.5	+2
horizontal deflection (cm)	−2	−1	0	+1	+2	+3	+4
point	3	4	5	6	7	8	9

At point 9 the horizontal deflecting voltage rapidly goes to -2 V again so the beam returns to the left side of the screen. From here it is ready to repeat the waveform trace over again. It is seen that with a sawtooth applied to the horizontal deflecting plates, any waveform applied to the vertical plates will be displayed on the screen of the CRT.

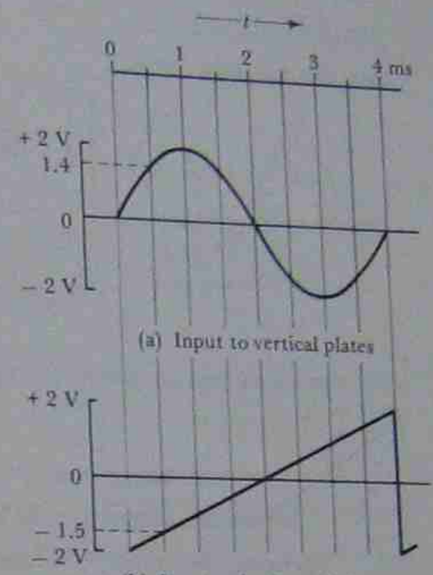


FIGURE 11-5. Waveform display on CRT.

EXAMPLE 11-1 A 500-Hz triangular wave with a peak amplitude of 40 V is applied to the vertical deflecting plates of a CRT. A 250-Hz sawtooth wave with a peak amplitude of 50 V is applied to the horizontal deflecting plates. The CRT has a vertical deflection sensitivity of 0.1 cm/V and a horizontal deflection sensitivity of 0.08 cm/V. Assuming that the two inputs are synchronized, determine the waveform displayed on the screen.

SOLUTION

For the triangular wave,

$$T = \frac{1}{f} = \frac{1}{500\ \text{Hz}} = 2\ \text{ms}.$$

For the sawtooth wave,

$$T = \frac{1}{250\ \text{Hz}} = 4\ \text{ms}.$$

The two waveforms are shown in Figure 11-6(a) and (b).
At t = 0:

$$\begin{aligned} \text{vertical voltage} &= 0 \\ \text{horizontal voltage} &= -50\ \text{V} \\ \text{horizontal deflection} &= \text{voltage} \times (\text{deflection sensitivity}) \\ &= -50 \times 0.08\ \text{cm} \\ &= -4\ \text{cm (i.e., 4 cm left from center)}; \end{aligned}$$

Point 1 on the CRT screen [Figure 11-6(c)] is at

$$\begin{aligned} \text{vertical deflection} &= 0, \\ \text{horizontal deflection} &= 4\ \text{cm left of center}. \end{aligned}$$

At t = 0.5 ms:

$$\begin{aligned} \text{vertical voltage} &= +40\ \text{V}, \\ \text{horizontal voltage} &= -37.5\ \text{V}; \end{aligned}$$

therefore, at *point 2* on the CRT screen,

$$\begin{aligned} \text{vertical deflection} &= +40 \times 0.1\ \text{cm} = +4\ \text{cm}, \\ \text{horizontal deflection} &= -37.5 \times 0.08\ \text{cm} = -3\ \text{cm}. \end{aligned}$$

At t = 1 ms (point 3):

$$\begin{aligned} \text{vertical deflection} &= 0, \\ \text{horizontal deflection} &= -25 \times 0.08\ \text{cm} = -2\ \text{cm}. \end{aligned}$$

At t = 1.5 ms (point 4):

$$\begin{aligned} \text{vertical deflection} &= -40 \times 0.1\ \text{cm} = -4\ \text{cm}, \\ \text{horizontal deflection} &= -12.5 \times 0.08\ \text{cm} = -1\ \text{cm}. \end{aligned}$$

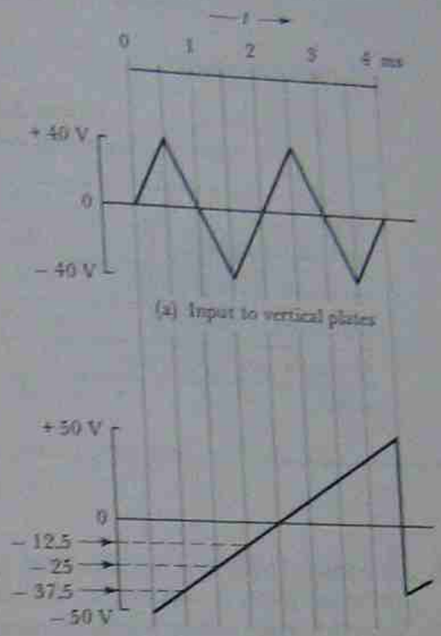


FIGURE 11-6. Waveforms and display for Example 11-1.

At t = 2 ms (point 5):

vertical deflection = 0,
horizontal deflection = 0.

t (ms)	2.5	3	3.5	4
vertical voltage (V)	+ 40	0	− 40	0
vertical deflection (cm)	+ 4	0	− 4	0
horizontal voltage (V)	+ 12.5	+ 25	+ 37.5	+ 50
horizontal deflection (cm)	+ 1	+ 2	+ 3	+ 4
point	6	7	8	9

11-4 OSCILLOSCOPE TIME BASE

11-4-1 Horizontal Sweep Generator

In Section 11-3 it was explained that a waveform applied to the vertical deflecting plates is displayed on the oscilloscope screen if a sawtooth (or repetitive ramp) voltage is simultaneously applied to the horizontal deflecting plates. The sawtooth voltage is produced by a *sweep generator circuit*, which may be of the type illustrated in Figure 11-7.

The sweep generator shown consists of two major components: a ramp generator and a noninverting Schmitt trigger circuit. Note that the inverting terminal of the operational amplifier is grounded via resistor R_7. (Operational amplifiers are discussed in Section 8-6-1.) Ignoring C_2, the input voltage to the Schmitt is the ramp generator output (V_1), applied via resistor R_6. Because the op-amp has a very large voltage gain (typically 200 000), a very small difference between the inverting and noninverting terminals causes the Schmitt output to be *saturated*. This means that the output voltage is very close to either the positive or the negative supply voltages. Typically, the saturated output voltage is

$$V_2 = +(V_{CC} - 1\text{ V}) \quad \text{or} \quad -(V_{EE} - 1\text{ V}).$$

Assume that the Schmitt output is negative, and that the ramp input to the Schmitt is at its minimum level. The voltages at both ends of potential divider $R_5 + R_6$ are negative, so the junction of R_5 and R_6 must also be negative. Thus, the op-amp noninverting terminal voltage is below the level of the (grounded) inverting terminal, and the op-amp output remains saturated in a negative direction.

As the ramp voltage grows, the voltage at the junction of R_5 and R_6 rises towards ground. When the ramp reaches a high enough positive level, the noninverting terminal is eventually raised slightly above ground. This causes the op-amp output to rapidly switch from the negative saturated level to saturation in the positive direction. The positive output voltage

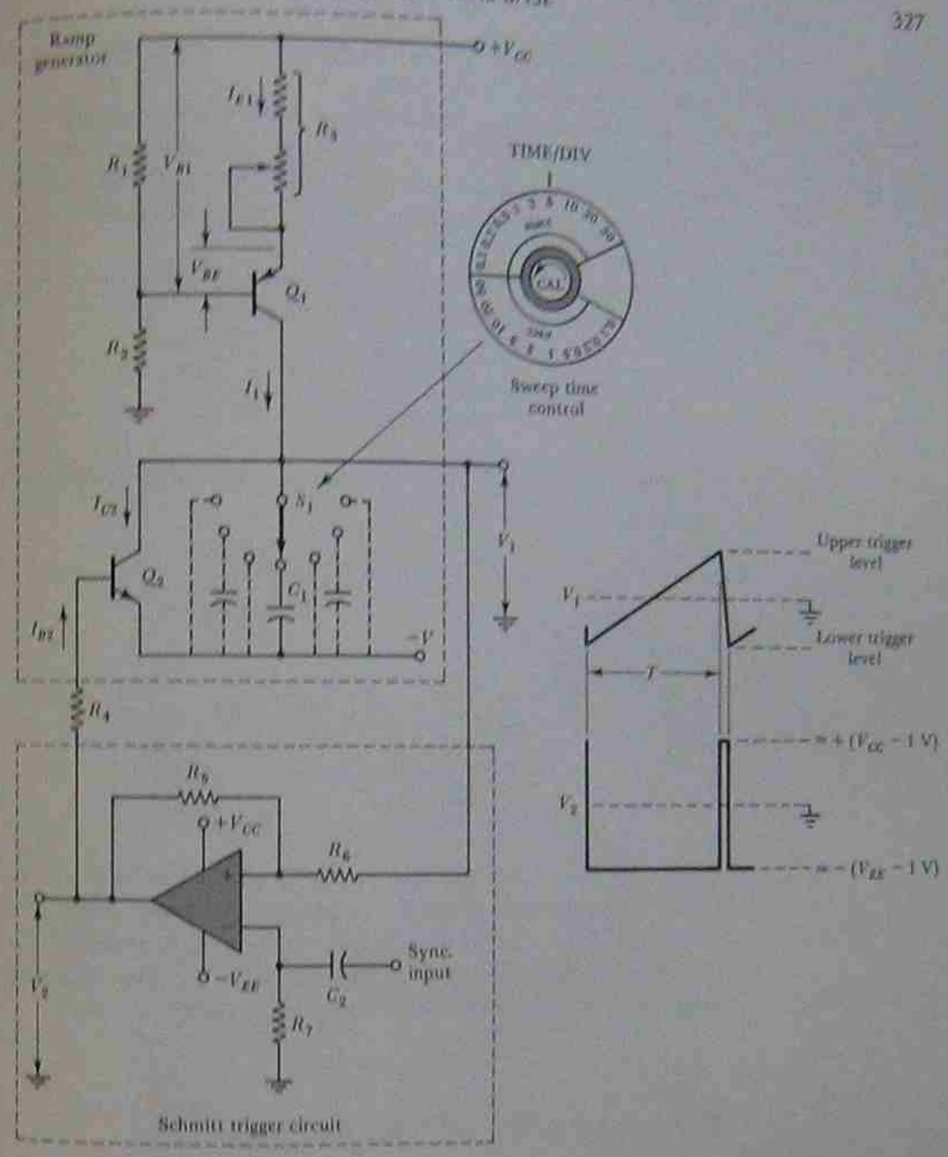


FIGURE 11-7. Basic circuit and waveforms of an oscilloscope sweep generator.

now causes the junction of R_5 and R_6 to become more positive. This positive input at the noninverting terminal tends to keep the op-amp output saturated in the positive direction. The level of the input voltage (to R_6) which causes the output to switch positively is known as the *upper trigger point*. For the output to go negative once more, the input to R_6 must fall to a negative level which will pull the noninverting terminal below ground. The negative input voltage level required to trigger the output to

negative saturation is termed the *lower trigger point*, and it is numerically equal to the upper trigger point.

It is seen that the trigger circuit output remains negative until the input voltage to R_6 rises to the upper trigger point for the circuit. Then the output switches to the positive saturation level. It also remains positive until the input falls to the lower trigger point, when it once again switches to negative saturation.

At the instant that triggering commences, the junction of R_5 and R_6 is at ground level, and the current through R_5 is

$$I = \frac{V_2 - 0}{R_5} \simeq \frac{(V_{CC} - 1\text{ V})}{R_5}.$$

This current also flows through R_6, giving the input (triggering) voltage as

$$I R_6 = \frac{(V_{CC} - 1\text{ V})}{R_5} R_6$$

or,

$$\boxed{\text{trigger voltage} = (V_{CC} - 1\text{ V})\frac{R_6}{R_5}.} \qquad (11\text{-}1)$$

In the ramp generator portion of Figure 11-7 transistor Q_1 and its associated components constitute a *constant current source*. Resistors R_1 and R_2 potentially divide the positive supply voltage (V_{CC}) to provide a constant bias voltage (V_{B1}) to the base of *pnp* transistor Q_1. This makes the voltage drop across emitter resistor R_3 a constant quantity:

$$V_{R3} = V_{B1} - V_{BE}.$$

Therefore, the emitter current I_{E1} is constant:

$$I_{E1} = \frac{V_{B1} - V_{BE}}{R_3}.$$

Since the transistor collector current is approximately equal to its emitter current, I_1 is a constant current:

$$\boxed{I_1 \simeq \frac{V_{B1} - V_{BE}}{R_3}.} \qquad (11\text{-}2)$$

Alteration of I_1 is possible by means of the adjustable portion of resistor R_3.

When the trigger circuit output is positive, a base current (I_{B2}) flows into *npn* transistor Q_2 via R_4. This switches Q_2 into saturation and produces collector current I_{C2}. When Q_2 is *on*, capacitor C_1 is effectively short-circuited, and I_1 flows via Q_2 to the $-V$ supply.

When the trigger circuit output goes negative, the base-emitter junction of Q_2 is reverse biased, I_{B2} ceases, and Q_2 is switched *off*. Constant current I_1 now flows into capacitor C_1, charging it linearly and producing a ramp output. The equation for the ramp voltage is

$$\boxed{\Delta V_1 = \frac{I_1 T}{C_1},} \qquad (11\text{-}3)$$

Where ΔV_1 is the capacitor voltage change during time T and C_1 is the capacitance.

The capacitor voltage continues to grow linearly until it arrives at the upper trigger level for the Schmitt. Then the Schmitt output goes positive once again, turning Q_2 *on* and rapidly discharging C_1. When the voltage across C_1 falls to the lower trigger level of the Schmitt, the trigger circuit output switches to negative again. Q_2 is once again switched *off*, and the voltage across C_1 commences to grow linearly once more.

The process described above is repeated continuously, producing a repetitive ramp wave (V_1 in Figure 11-7). A pulse waveform (V_2) is also generated at the output of the Schmitt trigger circuit. The complete circuit is termed a *free-running ramp generator*.

The amplitude of the ramp waveform is obviously dictated by the upper and lower trigger points of the Schmitt trigger circuit. The time period (T) of the ramp depends upon charging current I_1, and upon the capacitance of C_1. I_1 can be altered by the adjustable component of R_3 [see Figure 11-7]. As illustrated, new values of C_1 can be switched into the circuit, thus altering time period T to any one of a wide range of values. Individual capacitors can be selected to generate ramps which sweep the electron beam across the screen of the CRT at 1 div/10 ms, 1 div/50 ms, or at any one of several other rates. The capacitor selection switch on the oscilloscope front panel is identified as TIME/DIV.

EXAMPLE 11-2 The sweep generator circuit in Figure 11-7 has the following components: $R_1 = 2.2\text{ k}\Omega$, $R_2 = 4.5\text{ k}\Omega$, $R_3 = 4.2\text{ k}\Omega$, $C_1 = 0.25\ \mu\text{F}$, $R_5 = 27\text{ k}\Omega$, and $R_6 = 3.9\text{ k}\Omega$. The supply voltages are ± 15 V, and the transistors are silicon devices. Calculate the peak-to-peak amplitude and time period of the ramp waveform.

SOLUTION

From Equation 11-1,

$$\text{trigger voltage} \simeq (V_{CC} - 1\text{ V})\frac{R_6}{R_5}$$
$$\simeq (15 - 1\text{ V})\frac{3.9\text{ k}\Omega}{27\text{ k}\Omega}$$
$$\simeq 2\text{ V},$$

upper trigger voltage = 2 V = positive peak of ramp, lower trigger voltage = −2 V = negative ramp peak, peak to peak ramp output = 4 V.

$$V_{B1} = V_{CC}\frac{R_1}{R_1 + R_2}\ (\text{assuming } I_{B1} \ll I_{B2})$$
$$= 15\text{ V} \times \frac{2.2\text{ k}\Omega}{2.2\text{ k}\Omega + 4.5\text{ k}\Omega}$$
$$= 4.9\text{ V}.$$

Equation 11-2,

$$I_{C1} = \frac{V_{B1} - V_{BE}}{R_3}$$
$$= \frac{4.9\text{ V} - 0.7\text{ V}}{4.2\text{ k}\Omega}$$
$$= 1\text{ mA},$$
$$\Delta V_1 = 4\text{ V peak to peak.}$$

From Equation 11-3,

$$T = \frac{\Delta V_1 \times C_1}{I_{C1}}$$
$$= \frac{4\text{ V} \times 0.25\ \mu\text{F}}{1\text{ mA}}$$
$$= 1\text{ ms}.$$

11-4-2 Automatic Time Base

For a waveform to be correctly displayed on an oscilloscope, it is important that the ramp voltage producing the horizontal sweep commences at the instant that the displayed waveform goes positive. Alternatively, it may be made to commence as the displayed wave goes negative. The ramp wave must be *synchronized* with the input waveform. If the input and ramp

waveforms are not synchronized, the displayed wave will appear to continuously slide off to one side of the screen. Synchronization is accomplished by means of the *sync input* to the Schmitt in Figure 11-7, and by the other components of the *automatic time base* in Figure 11-8.

The voltage waveform to be displayed is applied to the *vertical amplifier* and to the time base *triggering amplifier* (see Figure 11-8). Like the vertical amplifier, the triggering amplifier has differential outputs (see Section 11-2). These provide two identical but antiphase voltage waveforms (V_{s1} and V_{s2}). In the triggering amplifier the input is amplified so much that its peaks are cut-off by saturation of the amplifier output stage. So the output waveforms are almost square, (Figure 11-8). One of these waveforms is passed via switch S_2 to the input of a Schmitt trigger circuit. The Schmitt is designed to have upper and lower trigger points slightly above and below ground. The Schmitt output rapidly goes positive as the input passes the upper trigger point, and negative as the input passes the lower trigger point (see the waveforms in Figure 11-8).

The output from the Schmitt circuit is a square waveform exactly in synchronism with the input wave to be displayed. This square wave is applied to a *differentiating circuit*. The differentiator produces an output which is proportional to the rate of change of the square wave. During the times that the square wave is at its constant positive level or at its constant negative level, its rate of change is zero. So the differentiator output is zero at these times. At the positive-going edge of the square wave, the rate of change is a large positive quantity. At the negative-going edge, the rate of change is a large negative quantity. Therefore, the differentiated square wave is a series of positive spikes coinciding with the positive-going edges of the square wave, and negative spikes coinciding with the negative-going edges (see Figure 11-8).

The spike waveform is now fed to a *positive clipper circuit*. This is essentially a rectifier circuit which passes the negative spikes but blocks (or *clips off*) the positive spikes. The negative spikes (which coincide with the commencement of each cycle of the original input) are passed via a *hold-off circuit* to the sync input of the sweep generator. For now, ignore the function of the hold-off circuit.

Return once again to the sweep generator circuit in Figure 11-7. Note that the sync input is capacitor coupled to the inverting input terminal of the Schmitt operational amplifier. Now assume that the ramp voltage from the integrator is approaching the upper trigger point of the Schmitt, but that it will not get there before commencement of another cycle of input. The situation is illustrated in Figure 11-9(a). The negative spike arrives at the op-amp inverting terminal via capacitor C_2. The inverting terminal is driven below ground level and below the level of the voltage at the noninverting terminal. The noninverting terminal is now positive with respect to the inverting terminal, and the Schmitt output rapidly switches

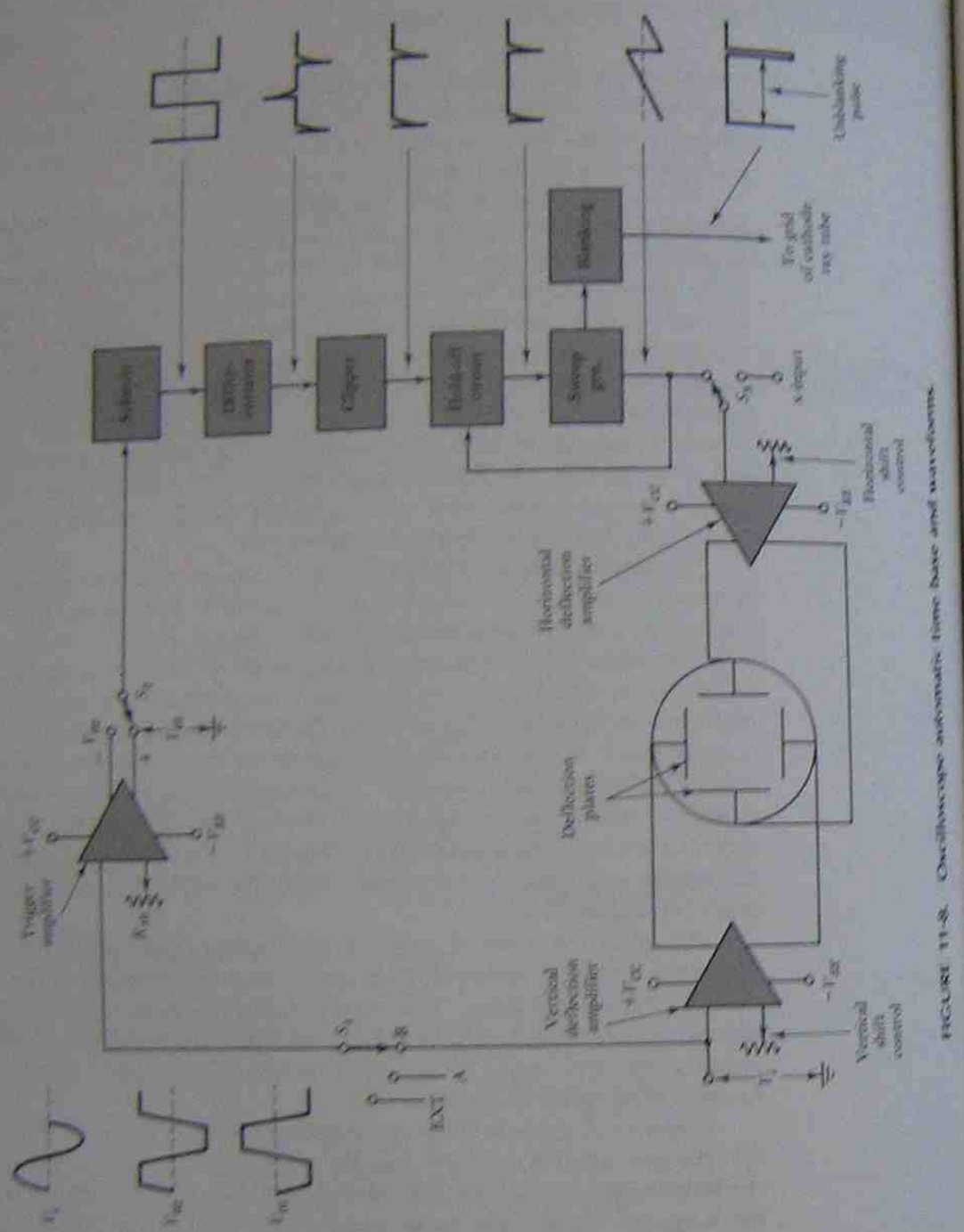


FIGURE 11-8. Oscilloscope automatic time base and waveforms.

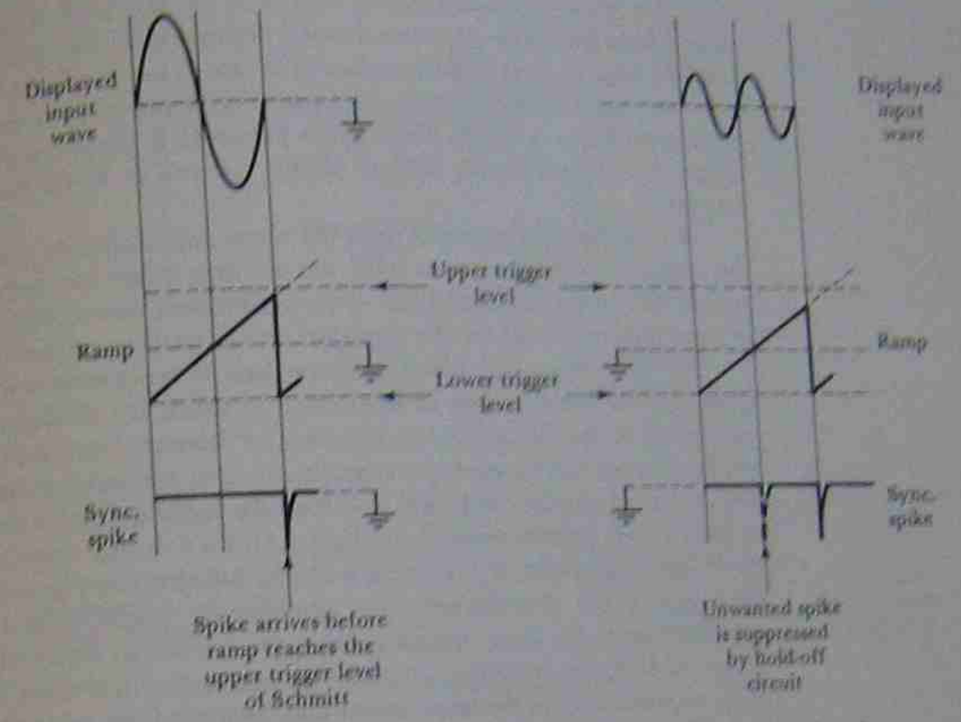


FIGURE 11-9. Synchronization of the ramp applied to the horizontal deflection plates with the input wave applied to the vertical plates.

to positive saturation. Q_2 is switched *on*, the ramp output falls rapidly to the Schmitt lower trigger point and then recommences to grow linearly again.

It is seen that the train of negative spikes causes the ramp output of the sweep generator to be synchronized with the input waveform that is to be displayed. The ramp commences at the beginning of each positive half cycle of the input. The ramp output from the sweep generator is fed to the horizontal amplifier (Figure 11-8). This amplifier provides differential (antiphase) ramp outputs to the horizontal deflecting plates, and causes the electron beam to sweep from left to right on the oscilloscope screen. The input waveform is now displayed exactly as explained in Section 11-3.

It is not desirable that *every* negative spike should trigger the Schmitt and reset the ramp to its starting point. If this occurred, the displayed wave would always consist of only one cycle, instead of two or more cycles which are frequently required [see Figure 11-9(b)]. The hold-off circuit in Figure

11-8 is a spike-suppressing circuit controlled by the level of the ramp output from the sweep generator. Once a negative spike has synchronized the time base, no more spikes are allowed to pass to the sync input terminal until the ramp output of the sweep generator approaches its maximum amplitude [Figure 11-9(b)]. Note that in Figure 11-8, the sweep generator output is fed back to the hold-off circuit, as well as to the horizontal amplifier.

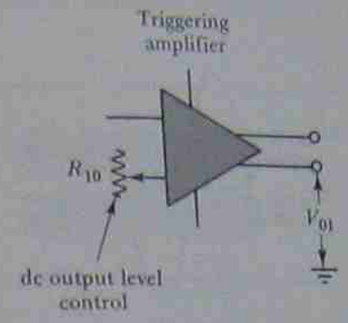
With all spikes suppressed until the ramp approaches its peak level, the ramp is *not* reset to zero until the electron beam has been swept horizontally to the right-hand side of the oscilloscope screen. Any number of waveform cycles can now be displayed on the oscilloscope screen.

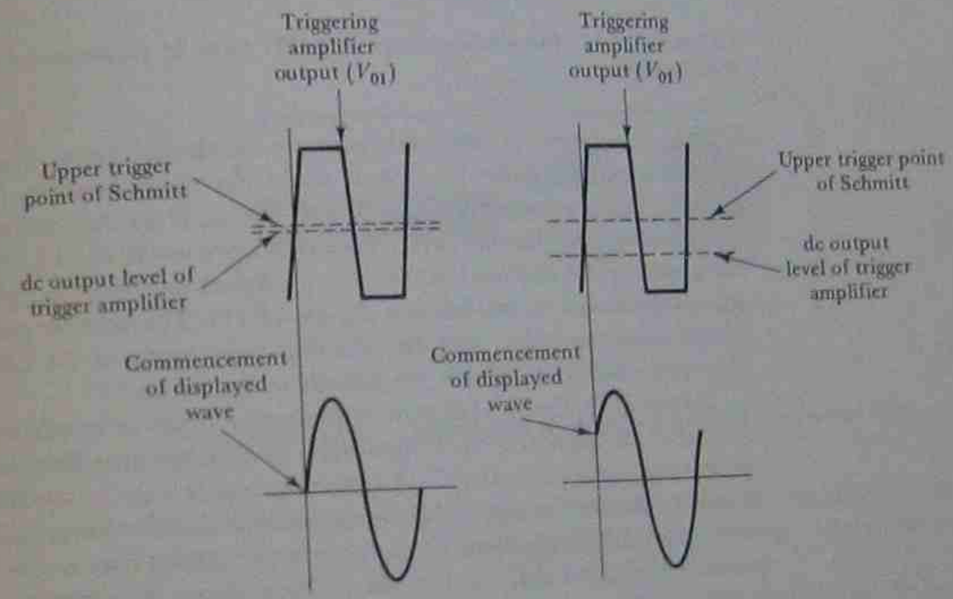
The exact instant at which the time base is synchronized with the input wave is usually taken as the instant at which the displayed wave commences its positive half cycle. However, as illustrated in Figure 11-10, synchronization can be made to occur shortly after the wave crosses zero. The triggering amplifier in Figure 11-8 is similar to the deflection amplifier in Figure 11-4. Potentiometer R_{10} in Figure 11-4 is a dc *shift control*, and in the triggering amplifier R_{10} performs a similar function (see Figure 11-10). By means of this potentiometer, the amplifier dc output levels can be adjusted close to the upper trigger point of the Schmitt in Figure 11-8. In Figure 11-10(a) the triggering amplifier output reaches the upper trigger point approximately at the same instant that the input wave commences its cycle. Therefore, the displayed wave commences at this instant. In Figure 11-10(b) the output of the triggering amplifier does not reach the trigger point until some time after the input wave has commenced its cycle. The displayed wave now commences at this point.

It is seen that potentiometer R_{10} functions as a *trigger level control*, to adjust the instant in time at which the displayed wave commences on the oscilloscope screen.

The displayed wave may be made to commence at the beginning of its negative half cycle, instead of its positive half cycle. This is accomplished simply by switching S_2 in Figure 11-8 to the in-phase output of the triggering amplifier (V_{o2}). The input to the Schmitt is now in phase with the input wave, and the negative spikes are generated at the instant that the input crosses zero from positive to negative. The horizontal sweep now commences at this instant, and the negative half cycle of the displayed wave occurs first.

In Figure 11-8 an output from the sweep generator is fed to a *blanking circuit*. This is the pulse waveform output (V_2) from the Schmitt in Figure 11-7. The pulse wave is inverted and capacitor coupled to convert it to a train of positive pulses during the sweep time, and negative pulses which occur each time the ramp wave falls from its maximum positive level to its maximum negative level. These pulses are fed to the grid of the CRT (Figure 11-1). The negative pulses (known as *blanking pulses*) drive the grid





(a) Displayed wave commences at the beginning of its cycle when the dc output level of the triggering amplifier is close to the Schmitt trigger point

(b) Displayed wave commences later in its cycle when the dc output level of the triggering amplifier is much lower than the Schmitt trigger point

FIGURE 11-10. The instant at which the displayed waveform commences is determined by the dc level control of the triggering amplifier.

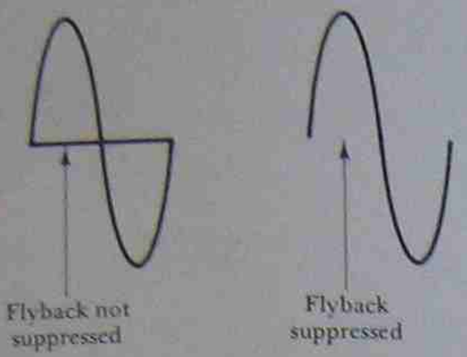


FIGURE 11-11. The electron beam in a CRT must be suppressed during the flyback time.

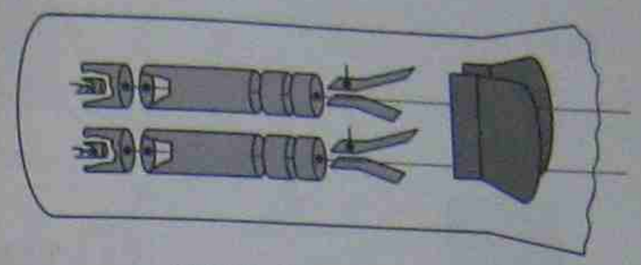
sufficiently negative to completely suppress the electron beam. This means that no electrons strike the screen while the ramp is going from its maximum positive to its maximum negative level. If the electrons were not suppressed during this time, every displayed wave would have a horizontal line traced by the electron beam during the *flyback time* from the right-hand side of the screen to the left (see Figure 11-11). The positive pulses are termed *unblanking pulses*, and the bias that these apply to the CRT grid cause electrons to travel from the cathode to the screen.

Switch S_1 in Figure 11-8 permits triggering inputs to be selected from channel A or channel B in a dual-trace oscilloscope (see Section 11-5). Alternatively, an external (EXT) triggering source can be selected. The time base can be disconnected from the horizontal deflection amplifier by means of switch S_3 in Figure 11-8. An external x-input may be applied to produce horizontal deflection of the electron beam. Applications of this facility are discussed in Section 11-10.

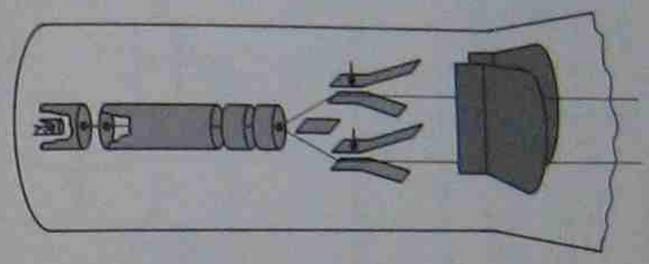
11-5 DUAL-TRACE OSCILLOSCOPES

Most oscilloscopes can display two waveforms rather than just one. This allows waveforms to be compared in terms of amplitude and phase or time. Two input terminals and two sets of controls are provided, identified as channel A and channel B.

The construction of a dual-trace CRT could be exactly as illustrated in Figure 11-1, with the exception that two complete electron guns are contained in a single tube [see Figure 11-12(a)]. In this case the instrument can be termed a *dual-beam oscilloscope* because there are two separate electron beams, one for each waveform trace. In another type of dual-trace CRT [Figure 11-12(b)], a single electron gun is involved, but the beam is split into two separate beams before it passes to the deflection plates. This is referred to as a *split-beam* CRT. The dual-beam and split-beam instruments each have only one set of horizontal deflection plates. The sawtooth



(a) CRT with two electron guns



(b) Split-beam CRT

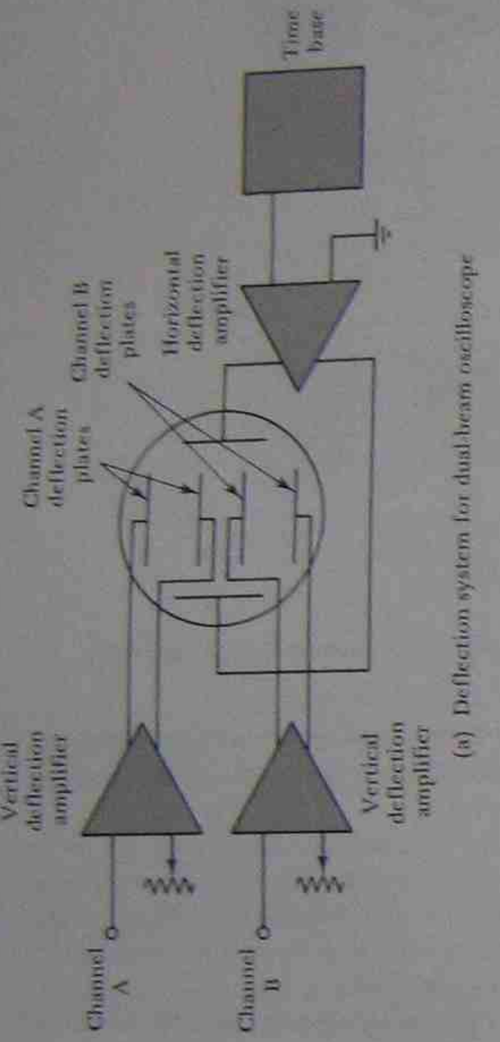
FIGURE 11-12. Construction of double-beam and split-beam CRTs.

wave from the time base is applied to the single set of horizontal deflection plates, and both beams are made to sweep across the screen simultaneously.

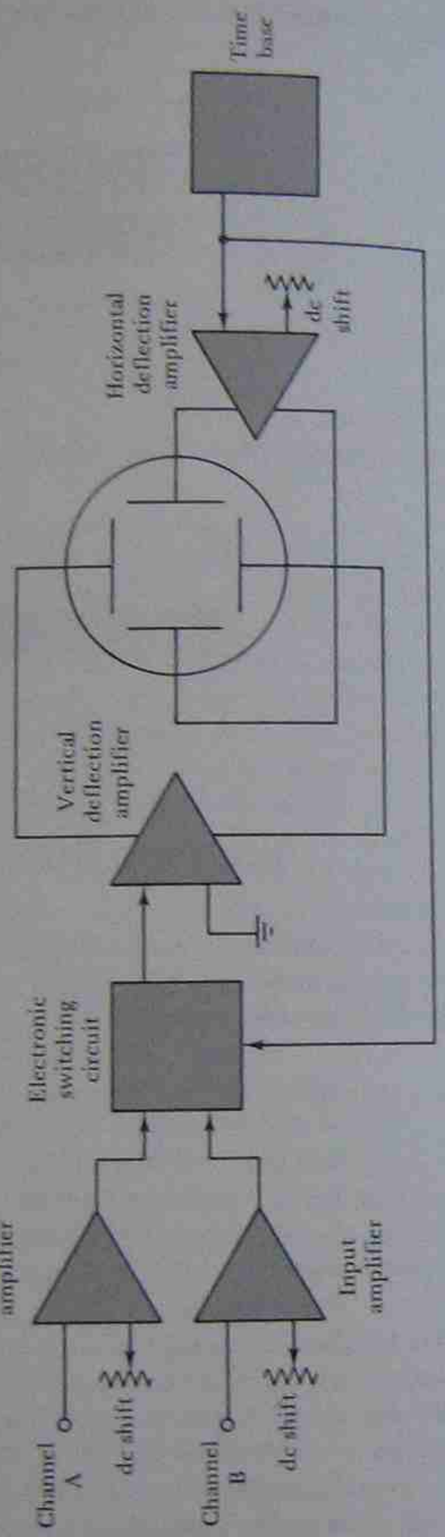
Figure 11-13(a) shows that in a dual-beam oscilloscope (or in a split-beam type) there are two completely separate vertical inputs: channel A and channel B. Each channel has its own deflection amplifier feeding one pair of vertical deflection plates. A time base controls the single set of horizontal deflection plates, as already explained.

Another more common type of dual-trace oscilloscope is illustrated in Figure 11-13(b). A single-beam CRT is shown, with only one set of vertical deflection plates. Two separate (channel A and channel B) input amplifiers are employed, with a single amplifier feeding the vertical deflection plates. The input to this amplifier is alternately switched between channels A and B, and the switching frequency is controlled by the time base circuit.

Consider Figure 11-14, which illustrates the process of alternately displaying first one input wave and then the other. The input to channel A is a sine wave with time period T, and that to channel B is a triangular wave also having a time period T [Figure 11-14(a)]. The two waveforms are in synchronism. Note that channel A input has a dc offset which puts it above ground level, while channel B is offset below ground. Channel A



(a) Deflection system for dual-beam oscilloscope



(b) Deflection system for single-beam dual-trace oscilloscope

FIGURE 11-13. Deflection systems for a dual-beam oscilloscope and for a single-beam, dual-trace oscilloscope.

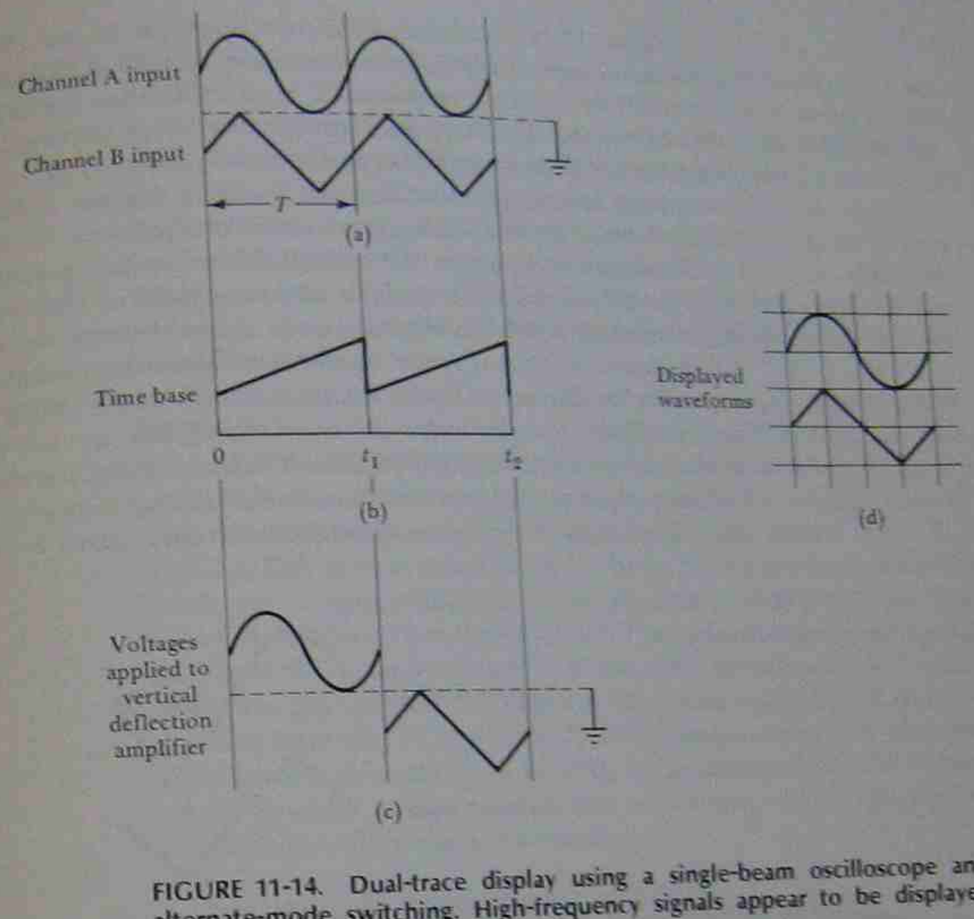


FIGURE 11-14. Dual-trace display using a single-beam oscilloscope and alternate-mode switching. High-frequency signals appear to be displayed simultaneously.

input is switched to the vertical deflection amplifier, and traced on the oscilloscope screen during time 0 to t_1. Channel *B* input is next applied to the vertical deflection amplifier and traced on the oscilloscope screen during time t_1 to t_2 [Figure 11-14(b),(c)]. The dc offsets on the inputs cause the waveform on channel *A* to be traced on the top half of the oscilloscope screen and that on channel *B* to be traced on the bottom half of the screen. During the next cycle of the time base channel *A* input is again traced on the screen, followed by channel *B* input once again. Thus, the two inputs are alternately and repeatedly traced on the screen. The repetition frequency is usually so high that the waveforms appear to be displayed simultaneously [Figure 11-14(d)].

When the method described above is employed to display two waveforms, the oscilloscope is said to be operating in *alternate mode*. A similar method which uses a much higher switching frequency is termed *chop mode*.

Figure 11-15 illustrates oscilloscope operation in the chop mode. Channel A input is traced for a short time, t_1, then channel B input is traced for time t_2. Back to channel A input for t_3, then channel B for t_4, and so on, as illustrated. High-frequency waveforms would be displayed as broken lines, exactly as shown in Figure 11-15. However, the breaks in the trace waveforms are of such short duration that they become invisible when medium-frequency and low-frequency waves are displayed.

Dual-trace oscilloscopes that employ channel switching normally permit selection of operation in either alternate mode or chop mode. For high-frequency inputs the alternate mode is best, because the waveform traces appear continuous rather than broken. When the alternate mode is used with low-frequency inputs, the beam is seen slowly tracing out first one wave and then the other. The two waveforms are not displayed continuously, and this makes comparison difficult. Using the chop mode with low-frequency inputs results in both waves being displayed continuously. The breaks in each trace are so short that they cannot be seen.

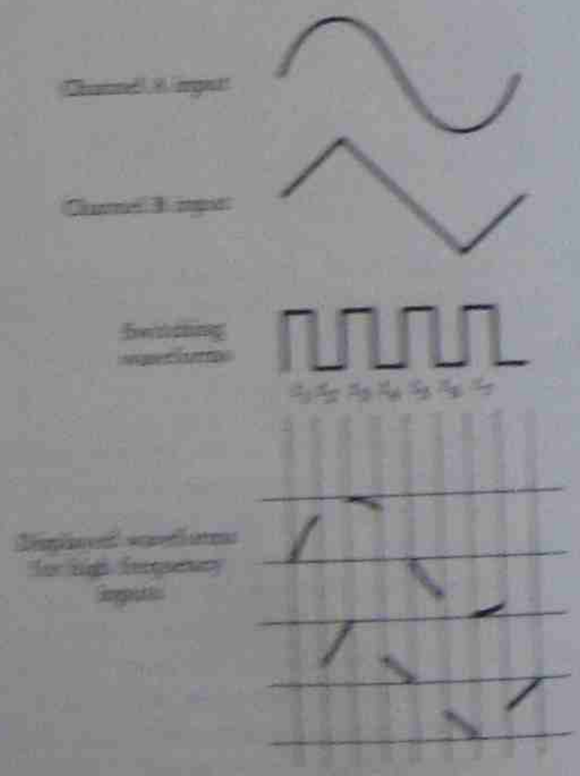


FIGURE 11-15. Dual-trace display using a single-beam oscilloscope in chop mode switching. For low-frequency inputs, the gaps in each trace are too short to be visible.

11-6 OSCILLOSCOPE CONTROLS

The front panel and controls of a representative single-beam dual-trace oscilloscope are illustrated in Figure 11-16. The waveforms under investigation are displayed on the screen, which is protected with a calibrated flat piece of hard plastic called a *graticule*. The graticule is used for measuring the amplitude (in vertical divisions) and the time period (in horizontal divisions) of any displayed waveform. Immediately below the screen is a power LINE ON/OFF switch, an INTENSITY control to adjust the brightness of the display, a FOCUS control to focus the display to a fine line, and a push-button BEAM FINDER to locate a display that has been shifted off the screen.

To facilitate display of two waveforms, there are two separate sets of VERTICAL controls identified as CHANNEL A and CHANNEL B. The purpose of the POSITION controls is to move each waveform vertically up or down the screen to set it in the best position for viewing. Each of these is a deflection amplifier dc shift control (see Figure 11-4). The VOLTS/DIV selector switch for each channel determines the sensitivity of the display to input voltages. These are attenuator selection switches, S_1 in Figure 11-4. When this control is set to 1 V, a signal having a peak-to-peak amplitude of 1 V would occupy 1 division of the screen graticule. A signal which occupies four screen divisions at this setting would have a peak-to-peak amplitude of 4 V. The VOLTS/DIV setting is correct only when the vernier knob at its center is in the CAL (calibrated) position. The vernier control provides continuous volts/div adjustment, so that the display amplitude may be increased as desired.



FIGURE 11-16. Single-beam, dual-trace oscilloscope (Courtesy of Hewlett-Packard).

Below the channel *A* and channel *B* VOLTS/DIV switches is a horizontal row of push-button switches, and below these are channel *A* and channel *B* input (coaxial cable) terminals. The two push buttons immediately above each input terminal facilitate ac or dc connection of the input voltage. Sometimes it is necessary to display an alternating voltage and block a dc level that it may be superimposed upon. This is achieved by setting the AC-DC button to AC, where a coupling capacitor passes the ac quantity and blocks the dc. The GND (ground) buttons alongside each AC-DC button disconnects the input signal and grounds the input terminal. This allows each trace to be set to a convenient *zero* position on the screen. When an input voltage is displayed, its dc level may be measured with respect to the zero position. The AC-DC and GND switches perform the same function as switch S_1 in Figure 11-4.

The VERTICAL DISPLAY *A* and *B* push buttons allow channel *A* input, channel *B* input, or both to be displayed on the screen. The B INV button is included to invert the channel *B* input, and the *A* + *B* button permits the channel *A* and channel *B* waveforms to be added together and displayed. With the A + B and B INV buttons pressed, the displayed waveform is the *difference* of channel *A* and channel *B* input voltages.

The horizontal TIME/DIV selector switch determines the number of horizontal divisions occupied by each cycle of displayed waveform. This control applies to both waveforms, and it is in fact the time base capacitor selection switch S_1 illustrated in Figure 11-7. With the TIME/DIV switch at 1 ms, a cycle of displayed waveform which occupies exactly 1 horizontal division on the screen has a time period of exactly 1 ms. Similarly, when one cycle of waveform occupies exactly 3.5 division at 1 ms/division its time period is 3.5 ms. The TIME/DIV setting is correct only when the vernier knob at its center is in the CAL position. The vernier control or *expander* provides continuous time/division adjustment, so that cycles of displayed waveforms may be widened as desired up to ten times the horizontal time/div setting. The HORIZONTAL POSITION knob performs a similar function to the VERTICAL POSITION controls. The displayed waveforms may be moved horizontally about the screen as desired. Once again, this control functions similarly to the dc shift control on the deflection amplifier in Figure 11-4.

The TRIGGER LEVEL knob continuously adjusts the triggering point of the input wave, as explained in Section 11-4-2. When set to AUTO OFF, the time base circuit no longer operates automatically. Each horizontal sweep of the electron beam must be triggered by an input waveform.

Immediately below the TRIGGER LEVEL control a PROBE ADJ (probe adjust) terminal is situated. A 2-kHz, 0.5-V square wave output may be taken from this terminal for use in calibrating attenuator probes. The calibration process is explained in Section 11-9-2.

The first three push-button switches in the vertical row below the PROBE ADJ terminal are for trigger source selection. They perform the same function as switch S_1 in Figure 11-8. The INT button selects an *internal* trigger source, which means that the time base is triggered from one of the input waveforms. When both channel *A* and channel *B* inputs are displayed, the internal trigger source is channel *A*. When the EXT (external) button is depressed, the time base is triggered from an external source connected to the EXT TRIGGER terminal. When LINE is selected as a trigger source, the time base is triggered from the line or ac power frequency. The TV-NORM push button is kept in its NORMAL position for most purposes. For studying TV video signals, the button is placed in the TV position. By means of the − + button, displayed waveform may be made to commence at the beginning of the *positive* half cycle (+) or at the beginning of the *negative* half cycle (−). This − + button performs the same function as S_2 in Figure 11-8.

The A-B SWP button is usually set in the SWP (sweep) position, where it allows the internal time base to sweep the electron beam horizontally across the tube face for waveform display. When the button is in the A-B position, signals applied to channel *B* input terminal produce vertical deflection, while channel *A* inputs produce horizontal deflection. One application for this facility is the display of electronic device characteristics (see Section 11-10).

11-7 MEASUREMENT OF VOLTAGE, FREQUENCY, AND PHASE

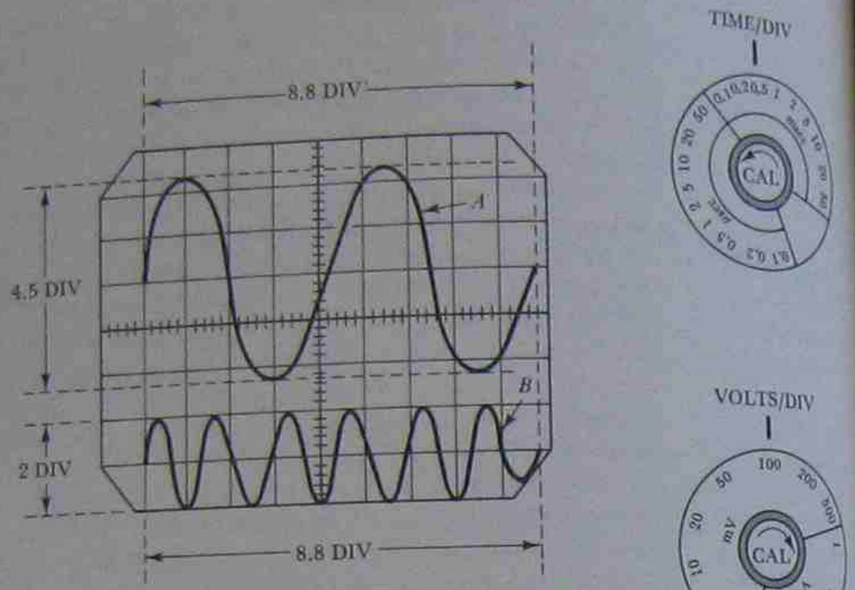
The peak-to-peak amplitude of a displayed waveform is very easily measured on an oscilloscope. Figure 11-17 shows two sine waves with different amplitudes and time periods. Waveform *A* has a peak-to-peak amplitude of 4.6 vertical divisions on the graticule, while wave *B* is measured as 2 vertical divisions peak-to-peak. *It is very important to check that the central vernier knob on the VOLTS / DIV control is in its calibrated (CAL) position before measuring the waveform amplitudes.* With the *VOLTS / DIV* control at 100 mV as illustrated, the peak-to-peak voltages of each wave are

$$\textit{Wave A: } V = (4.6\ \textit{divisions}) \times 100\ \text{mV} = 460\ \text{mV}.$$

$$\textit{Wave B: } V = (2\ \textit{divisions}) \times 100\ \text{mV} = 200\ \text{mV}.$$

If the waveforms shown in Figure 11-17 were outputs from an amplifier, for example, they might have dc components as well as the ac components illustrated. Suppose, the dc level of wave *A* were 10 V. The dc level would produce a deflection of

$$10\ \text{V}/100\ \text{mV} = 100\ \text{divisions}.$$



V_A = (4.5 DIV) × 100 mV/DIV
V_B = (2 DIV) × 100 mV/DIV
$2T_A$ = (8.8 DIV) × 0.5 ms/DIV
$6T_B$ = (8.8 DIV) × 0.5 ms/DIV

FIGURE 11-17. Measurement of peak-to-peak voltage and time period of sine waves.

Clearly, the wave would be deflected right off the screen if the oscilloscope is dc coupled. With ac coupling the wave is on screen.

The time period of a sine wave is determined by measuring the time for one cycle in horizontal divisions and multiplying by the setting of the TIME/DIV control:

$$T = (\text{Horizontal divisions/cycle}) \times (\text{TIME/DIV}) \qquad (11\text{-}4)$$

The frequency is then calculated as the inverse of the time period. Here again, before measuring the time period of the wave, *it is necessary to check that the central vernier knob on the TIME / DIV control is set in its calibrated (CAL) position*. The time period and frequency of each wave in Figure

11-17 are:

$$\text{Wave } A\text{: } T = \frac{(8.8 \text{ divisions}) \times 0.5 \text{ ms}}{2 \text{ cycles}} = 2.2 \text{ ms},$$

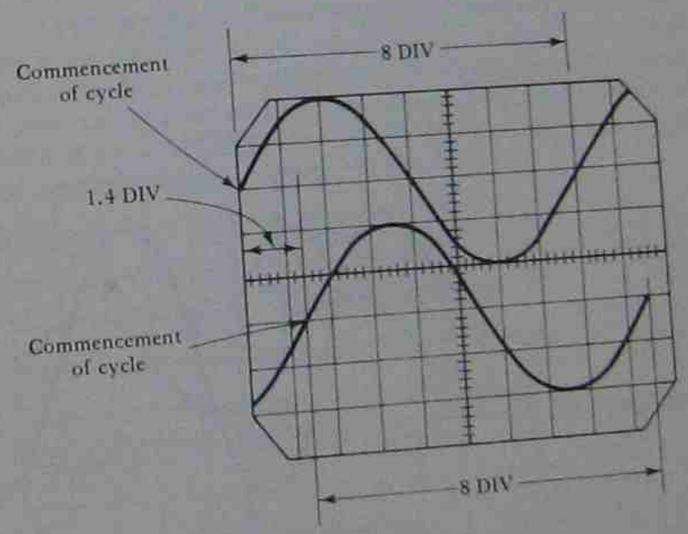
$$f = 1/(2.2 \text{ ms}) \approx 455 \text{ Hz}.$$

$$\text{Wave } B\text{: } T = \frac{(8.8 \text{ divisions}) \times 0.5 \text{ ms}}{6 \text{ cycles}} = 0.73 \text{ ms},$$

$$f = 1/(0.73 \text{ ms}) \approx 1.36 \text{ kHz}.$$

The phase difference between two waveforms is measured by the method illustrated in Figure 11-18. Each wave has a time period of 8 horizontal divisions, and the time between commencement of each cycle is 1.4 divisions. One cycle = 360°. Therefore, 8 div = 360° and,

$$1 \text{ div} = \frac{360}{8} = 45°$$



8 DIV = 360°

$$1.4 \text{ DIV} = \frac{360°}{8 \text{ DIV}} \times 1.4 \text{ DIV}$$

FIGURE 11-18. Measurement of phase difference between two sine waves.

Thus, the phase difference is

$$\phi = 1.4 \text{ div} \times (45^\circ/\text{div})$$
$$= 63^\circ.$$

EXAMPLE 11-3 Determine the amplitude frequency and phase difference between the two waveforms illustrated in Figure 11-19.

SOLUTION

$$V_A \text{ peak-to-peak} = (6 \text{ vertical div}) \times (200 \text{ mV/div})$$
$$= 1.2 \text{ V},$$
$$T_A = (6 \text{ horizontal div}) \times (0.1 \text{ ms/div})$$
$$= 0.6 \text{ ms},$$
$$f_A = 1/T = 1/0.6 \text{ ms}$$
$$= 1670 \text{ Hz},$$

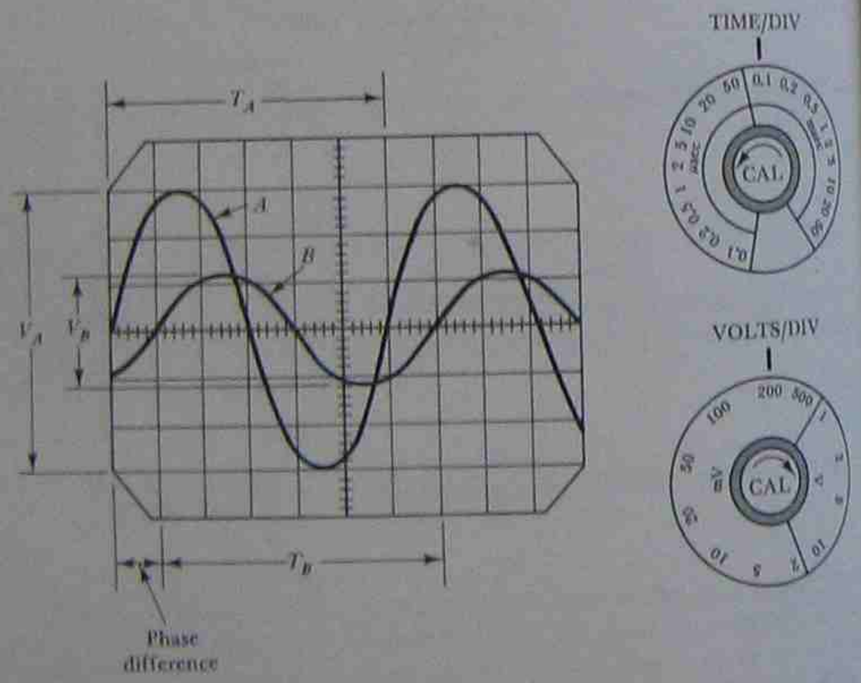


FIGURE 11-19. Waveforms for Example 11-3.

$$V_B \text{ peak-to-peak} = (2.4 \text{ vertical div}) \times (200 \text{ mV/div})$$
$$= 480 \text{ mV},$$
$$T_B = 0.6 \text{ ms},$$
$$f_B = 1670 \text{ Hz}.$$

$$\text{one cycle} = (6 \text{ horizontal div}) = 360^\circ,$$
$$\text{phase difference} = 1 \text{ div}$$
$$= \frac{360^\circ}{6} = 60^\circ.$$

11-8 PULSE MEASUREMENTS

Two pulse waveforms are displayed in Figure 11-20. The upper wave of the two has steep leading and lagging edges, while the lower has measurable *rise time* (t_r) and *fall time* (t_f). If the upper wave is the input to a circuit, the lower might be an output. In this case there could be a *delay time* (t_d). The rise time of the pulse is the time for the pulse to go from 10% to 90% of the pulse amplitude. This is shown in the illustration. Similarly, the fall time is the time required for the pulse to go from 90% to 10% of its amplitude. The delay time is the time elapsed from commencement of the input pulse to the point at which the output pulse reaches 10% of its amplitude. If the TIME/DIV control is at 1 μs, the delay time, rise time, and fall time from Figure 11-20 are:

$$t_d = 1 \text{ div} \times 1 \ \mu\text{s} = 1 \ \mu\text{s},$$
$$t_r = 0.7 \text{ div} \times 1 \ \mu\text{s} = 0.7 \ \mu\text{s},$$
$$t_f = 0.9 \text{ div} \times 1 \ \mu\text{s} = 0.9 \ \mu\text{s}.$$

The pulse width (PW) and the time period (T) of the upper wave in Figure 11-20 are

$$\text{PW} = 4.5 \ \mu\text{s},$$
$$T = 8 \ \mu\text{s},$$

giving

$$f = 1/8 \ \mu\text{s} = 125 \text{ kHz}.$$

Another important measurement that can be made from the kind of pulse wave displayed in Figure 11-20 is termed the *slew rate*. This is

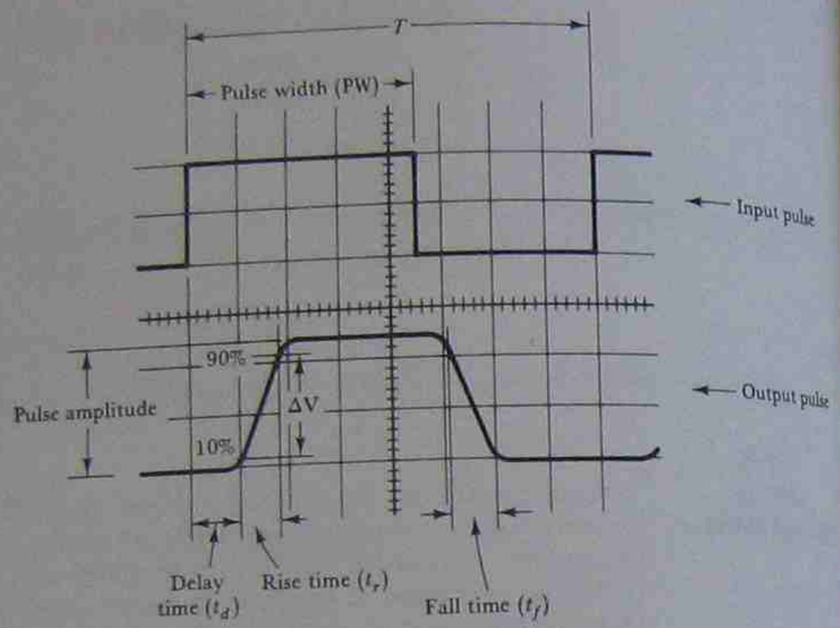


FIGURE 11-20. Measurement of pulse amplitude, pulse width, rise time, and fall time.

particularly applicable to operational amplifiers, and it is related to the frequency response of the amplifier. The slew rate defines how fast the output of an amplifier may be made to change when a pulse type signal is applied to the amplifier input. The rate of change (i.e., the slew rate) is measured as (voltage change)/time, usually in units of volts/μs. Referring to the lower wave in Figure 11-20, the voltage change during the rise time is ΔV = (2 vertical divisions). With the TIME/DIV control at 1 μs, the rise time is $t_r = 0.7\ \mu$s, as already determined. If the VOLTS/DIV control is at 1 V, $\Delta V = 2$ V. These quantities give:

$$\text{slew rate} = \frac{\Delta V}{t_r} = \frac{2\text{ V}}{0.7\ \mu\text{s}} \simeq 2.9\text{ V}/\mu\text{s}.$$

EXAMPLE 11-4 Determine the rise time, fall time, and frequency of the pulse wave illustrated in Figure 11-21. Also, calculate the slew rate of the amplifier which produces this wave as an output.

SOLUTION

$$\begin{aligned}
\text{pulse amplitude} &= (4\text{ vertical div}) \times (2\text{ V/div}) \\
&= 8\text{ V}, \\
T &\simeq (5.6\text{ horizontal div}) \times (5\ \mu\text{s/div}) \\
&= 28\ \mu\text{s}, \\
f &= 1/28\ \mu\text{s} \\
&\simeq 35.7\text{ kHz}, \\
t_r &\simeq (0.5\text{ div}) \times (5\ \mu\text{s/div}) \\
&= 2.5\ \mu\text{s}, \\
t_f &\simeq (0.6\text{ div}) \times (5\ \mu\text{s/div}) \\
&= 3\ \mu\text{s};
\end{aligned}$$

$$\begin{aligned}
\text{slew rate} &= \frac{\Delta V}{t_r} \\
&= \frac{(3.6\text{ div}) \times (2\text{ V/div})}{2.5\ \mu\text{s}} \\
&\simeq 2.9\text{ V}/\mu\text{s}.
\end{aligned}$$

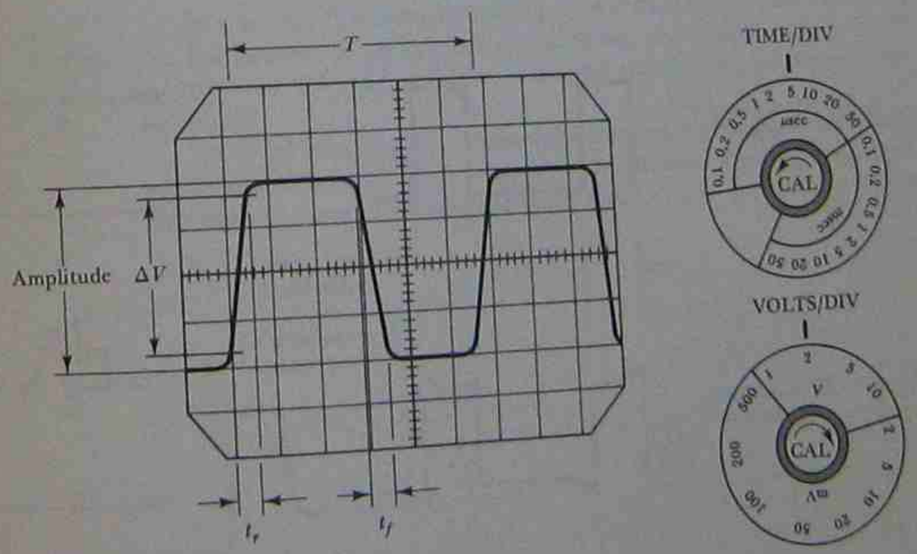


FIGURE 11-21. Waveform for Example 11-4.

Some more pulse measurements are illustrated in Figure 11-22. A pulse wave with $PW = 50$ ms is shown in Figure 11-22(a). This is how the wave is displayed when the signal is direct coupled to the oscilloscope. If this same wave is ac coupled, distortion may be introduced by the oscilloscope as shown in Figure 11-22(b). When the oscilloscope input is switched from dc to ac, a 0.1-μF coupling capacitor is introduced in series with the input terminal. This capacitor is charging and discharging (via the 1-MΩ input resistance) during the pulse width, and during the space time between pulses. Thus the input voltage is not faithfully passsed to the deflection amplifier. The type of distortion shown in Figure 11-22(b) is classified as *low-frequency distortion*. The product of the 0.1-μF coupling capacitor and the 1-MΩ input resistance gives a quantity known as the oscilloscope input time constant (τ):

$$\boxed{\tau = CR} \tag{11-5}$$

$$\begin{aligned}\tau &= C_c R_i \\ &= 0.1\ \mu\text{F} \times 1\ \text{M}\Omega \\ &= 0.1\ \text{sec.}\end{aligned}$$

In Figure 11-22(a) and (b), the pulse width is 50 ms, which is exactly half of τ. When the pulse width (and the space between pulses) is very

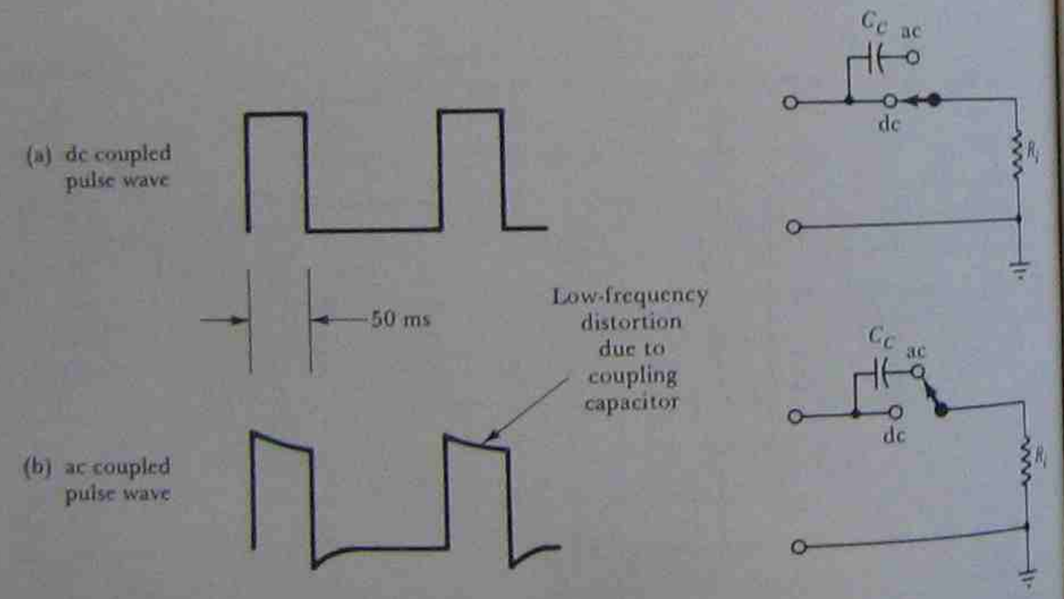


FIGURE 11-22. A dc-coupled pulse wave that is faithfully reproduced on an oscilloscope may have low-frequency distortion when ac coupled. This is introduced by the oscilloscope coupling capacitor.

much less than the time constant, the capacitor charges by such a small amount that there is no noticeable distortion introduced.

Sometimes a pulse wave with a large dc component has to be displayed, and it is necessary to use ac coupling to get an on-screen display. To avoid noticeable low-frequency pulse distortion introduced by the oscilloscope, the pulse width and space width should typically be less than 1/20 of the input time constant of the oscilloscope.

Figure 11-23 shows high-frequency distortion of a pulse wave. Again this is introduced by the oscilloscope, and it is present whether the input is ac or dc coupled. In this case very short duration pulses are involved. In Figure 11-23 the pulse width is = 0.2 μs.

The broken line shows that the pulse should have very steep sides and a flat top. The distortion has introduced noticeable rise and fall times and has rounded some of the corners of the waveform. This is high-frequency distortion, and it is the result of the combination of pulse-wave source resistance and oscilloscope input capacitance (*not* coupling capacitance). The oscilloscope input capacitance is typically $C_i = 30$ pF. Now suppose the source resistance is $R_s = 1$ kΩ. The circuit time constant is

$$\begin{aligned}\tau &= C_i R_s = 30\ \text{pF} \times 1\ \text{k}\Omega \\ &= 0.03\ \mu\text{s.}\end{aligned}$$

In this case, C_i is charging and thus introducing rise and fall times that are not present in the original pulses. If the pulse width is very much greater than $C_i R_s$, the distortion caused by the rise and fall times is not noticeable.

To avoid (oscilloscope introduced) *low-frequency* pulse distortion, pulse widths should be very much *shorter* than the product of *coupling capacitance* and *input resistance*. Typically the pulse width should be equal to or less

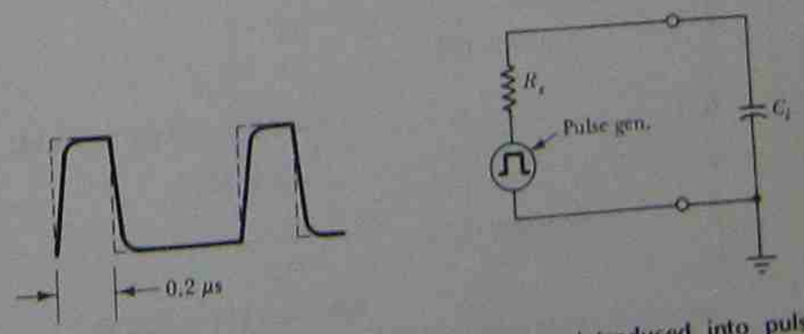


FIGURE 11-23. High-frequency distortion can be introduced into pulse waveforms by the input capacitance of an oscilloscope.

than $1/20$ of C_iR_s:

$$\boxed{PW \leq \frac{C_iR_s}{20}.} \tag{11-6}$$

To avoid *high-frequency* pulse distortion pulse widths should be very much *longer* than the product of *input capacitance* and *source resistance*. Typically pulse widths should be equal to or greater than 20 times C_iR_s:

$$\boxed{PW \geq 20C_iR_s.} \tag{11-7}$$

EXAMPLE 11-5 (*a*) An oscilloscope with $R_i = 10\ M\Omega$, and $C_i = 0.1\ \mu F$ is to be used to display an ac coupled pulse wave. Determine the longest pulse width that may be displayed without low-frequency distortion introduced by the oscilloscope.

(*b*) A pulse waveform with a 3.3-kΩ source resistance is to be displayed on an oscilloscope with an input capacitance of 15 pF. Determine the shortest pulse width that may be displayed without high-frequency distortion being introduced.

SOLUTION (*a*)

$$\tau = C_iR_i = 0.1\ \mu F \times 10\ M\Omega$$
$$= 1\ s,$$

Equation 11-6,

$$\text{maximum PW} = 1/20 \times C_iR_i$$
$$= 1/20 \times 1\ s$$
$$= 50\ ms.$$

SOLUTION (*b*)

$$\tau = C_iR_s = 15\ pF \times 3.3\ k\Omega$$
$$\simeq 5 \times 10^{-8},$$

Equation 11-7,

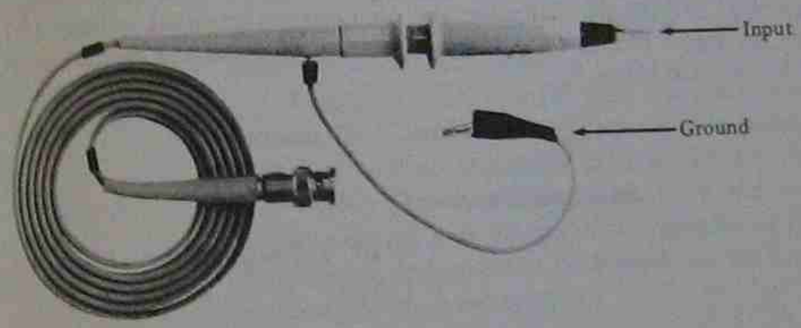
$$\text{minimum PW} = 20C_iR_s$$
$$= 20 \times 5 \times 10^{-8}$$
$$= 1\ \mu s.$$

11-9 OSCILLOSCOPE PROBES

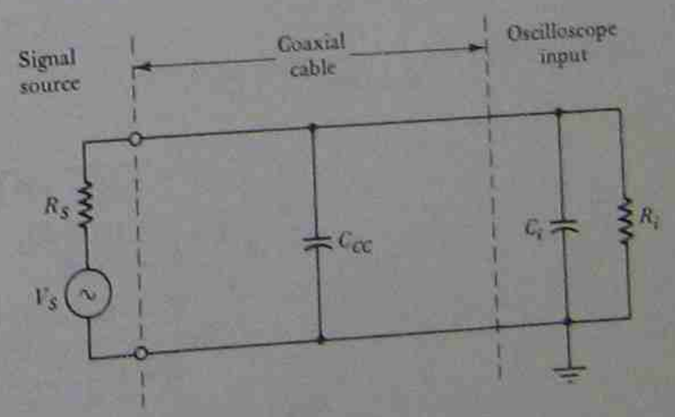
11-9-1 1:1 Probes

The input signals to an oscilloscope are usually connected via coaxial cables with *probes* on one end [see Figure 11-24(a)]. These are normally just convenient-to-use insulated connecting clips. As illustrated, each probe has two connections, an *input* and a *ground*. The coaxial cable consists of an insulated central conductor surrounded by a braided circular conductor which is covered by an outer layer of insulation. The central conductor carries the input signal, and the circular conductor is grounded so that it acts as a screen to help prevent unwanted signals being *picked up* by the oscilloscope input. This type of probe is usually referred to as a *1:1 (one-to-one) probe*, because it does not contain resistors to attenuate the input signal.

The coaxial cable connecting the probe to the oscilloscope has a capacitance which can effectively overload a high-frequency signal source. The input impedance of the oscilloscope *at the front panel* is typically 1 MΩ in parallel with 30 pF. The coaxial cable can add another 100 pF to the total input capacitance. The circuit of a signal source, probe, and oscilloscope input is illustrated in Figure 11-24(b). The total impedance offered



(a) Typical 1:1 probe (Courtesy of Hewlett-Packard)



(b) Equivalent circuit of signal source, probe, and oscilloscope input

FIGURE 11-24. Oscilloscope 1:1 probe and equivalent circuit.

by the coaxial cable and the oscilloscope input should always be much larger than the signal source impedance. Where this is not the case, the signal is attenuated and phase shifted when connected to the oscilloscope.

At frequencies where the reactance of $(C_{cc} + C_i)$ is very much larger than R_s and R_i, the capacitances have a negligible effect and the oscilloscope terminal voltage is

$$V_i = V_s \frac{R_i}{R_s + R_i}$$

As the signal frequency increases, the capacitive reactance gets smaller and smaller, and the signal is noticeably attenuated when it arrives at the oscilloscope terminals. The signal is attenuated by 3 dB at the frequency at which the capacitive reactance equals R_s. There is also a 45° phase shift introduced at this frequency.

EXAMPLE 11-6 A signal with an amplitude of $V_s = 1$ V and a source resistance of $R_s = 600\ \Omega$ is connected to an oscilloscope with an input impedance of $R_i = 1\ \text{M}\Omega$ in parallel with $C_i = 30$ pF. The coaxial cable has a capacitance of $C_{cc} = 100$ pF. Calculate the oscilloscope terminal voltage (V_i) when the signal frequency is 100 Hz. Also determine the frequency at which V_i is 3 dB below V_s.

SOLUTION

$$\begin{aligned}\text{total capacitance} &= C_i + C_{cc}\\ &= 30\ \text{pF} + 100\ \text{pF}\\ &= 130\ \text{pF},\end{aligned}$$

$$X_c = \frac{1}{2\pi fC};$$

at 1 kHz,

$$\begin{aligned}X_c &= \frac{1}{2\pi \times 100\ \text{Hz} \times 130\ \text{pF}}\\ &= 12.2\ \text{M}\Omega,\\ R_s &= 600\ \Omega,\\ X_c &\gg R_s \quad \text{and} \quad R_i,\\ V_i &= V_s \frac{R_i}{R_s + R_i}\\ &= 1\ \text{V} \times \frac{1\ \text{M}\Omega}{600\ \Omega + 1\ \text{M}\Omega}\\ &= 0.9994\ \text{V}.\end{aligned}$$

When $V_i = (V_s - 3\ \text{dB})$:

$$\begin{aligned}X_c &= R_s = 600\ \Omega,\\ \frac{1}{2\pi fC} &= 600\Omega,\\ f &= \frac{1}{2\pi C \times 600\ \Omega}\\ &= \frac{1}{2\pi \times 130\ \text{pF} \times 600\ \Omega}\\ &= 2.04\ \text{MHz}.\end{aligned}$$

11-9-2 Attenuator Probes

Attenuator probes attenuate the input signal, usually by a factor of 10. They also normally offer a much larger input impedance than a 1 : 1 probe, thereby minimizing loading effects on the circuit under test. Compensation is included for oscilloscope input capacitance and coaxial cable capacitance. Because of the ten-times attenuation, these probes are usually referred to as *10 : 1 probes*; however, other probes are available with different attenuation factors.

Figure 11-25(a) and (b) show the circuit and equivalent circuit of a typical 10 : 1 probe. A 9-MΩ resistor is included in series with the input terminal, and an adjustable capacitor (C_1) is connected in parallel with the 9-MΩ resistor, as illustrated. C_2 is the sum of oscilloscope input capacitance C_i and coaxial cable capacitance C_{cc}. At low and medium frequencies, the capacitive impedances are too large to be effective, and the oscilloscope input voltage is

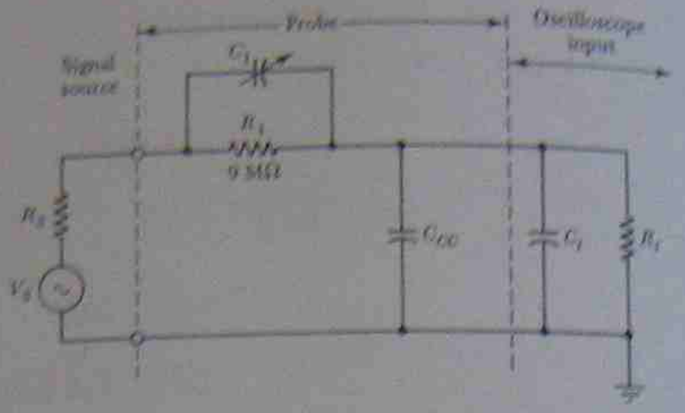
$$V_i = V_s \frac{R_i}{R_1 + R_s + R_i} \qquad \text{[see Figure 11-25(b)]}$$

when $R_s \ll R_1$,

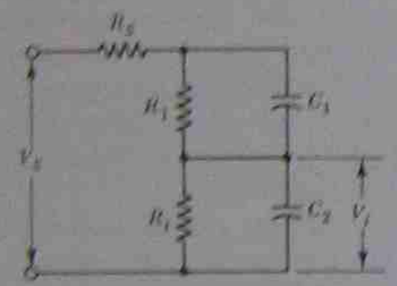
$$V_i = V_s \frac{R_i}{R_1 + R_i};$$

with $R_1 = 9\ \text{M}\Omega$ and $R_i = 1\ \text{M}\Omega$,

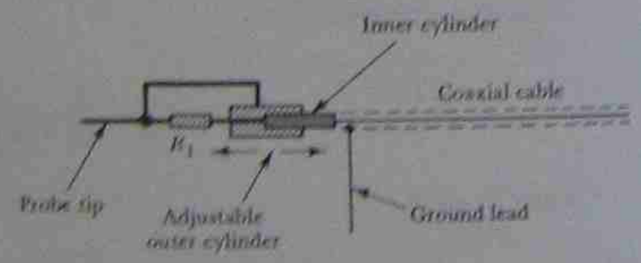
$$\begin{aligned}V_i &= V_s \frac{1\ \text{M}\Omega}{9\ \text{M}\Omega + 1\ \text{M}\Omega}\\ &= V_s/10.\end{aligned}$$



(a) Circuit of 10:1 probe



(b) Equivalent circuit



(c) Inner construction of 10:1 probe

FIGURE 11-25. Circuit and construction of a 10:1 oscilloscope probe.

The attenuation of the signal due to the capacitors acting alone can be calculated from:

$$V_i = V_s \frac{X_{C2}}{X_{C1} + X_{C2}}$$

$$= V_s \frac{1/\omega C_2}{1/\omega C_1 + 1/\omega C_2}$$

$$= V_s \frac{1}{(C_2/C_1) + 1},$$

$$V_i = V_s \frac{C_1}{C_2 + C_1}.$$

When the capacitive network attenuates the signal in the same proportion as the resistive network attenuation, V_s across R_i equals V_i across C_2 and

$$\boxed{\frac{R_i}{R_1 + R_i} = \frac{C_1}{C_2 + C_1}.} \tag{11-8}$$

A phasor diagram can be drawn to show that the voltages across C_2 and R_i are in phase, as well as being equal in amplitude. Therefore, C_1 completely compensates for the presences of C_2. The additional attenuation and phase shift at high frequencies due to the presences of C_2 (without C_1) is now eliminated, and the probe-oscilloscope combination is compensated for *all* frequencies.

The value of C_1 required to compensate for C_2 is determined from Equation 11-8 as

$$\boxed{C_1 = C_2 \frac{R_i}{R_1}.} \tag{11-9}$$

EXAMPLE 11-7 Calculate the value of C_1 required to compensate a 10:1 probe, when the oscilloscope input capacitance is 30 pF and the coaxial cable capacitance is 100 pF. Also calculate the probe input capacitance *seen* from the load.

SOLUTION

$$C_2 = C_{cc} + C_i$$
$$= 130 \text{ pF}$$

Equation 11-9,

$$C_1 = C_2 \frac{R_i}{R_1}$$
$$= 130 \text{ pF} \times \frac{1 \text{ M}\Omega}{9 \text{ M}\Omega}$$
$$= 14.4 \text{ pF}$$

The probe input capacitance C_T is C_1 in series with C_2:

$$1/C_T = 1/C_1 + 1/C_2$$
$$= 1/14.4 \text{ pF} + 1/130 \text{ pF},$$
$$C_T \simeq 13 \text{ pF}.$$

EXAMPLE 11-8 Determine the signal frequency at which the probe in Example 11-7 causes a 3-dB reduction in the signal from a 600-Ω source.

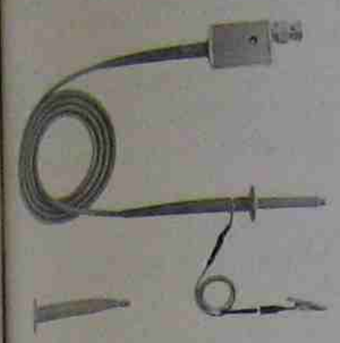
SOLUTION

$$X_c = R_s,$$
$$\frac{1}{2\pi fC} = 600\ \Omega,$$
$$f = \frac{1}{2\pi \times 13 \text{ pF} \times 600\ \Omega}$$
$$= 20.4 \text{ MHz}.$$

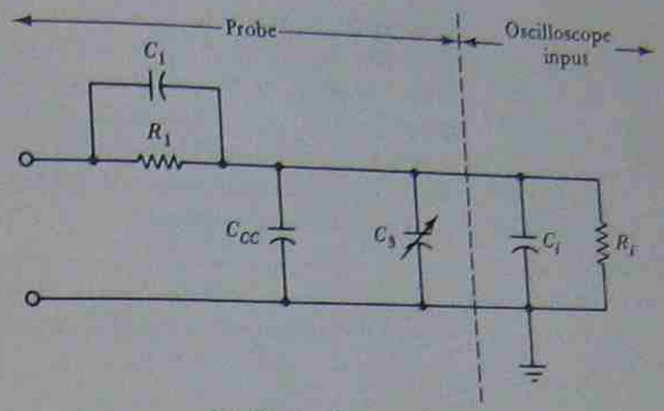
Figure 11-25(c) shows the typical construction of an attenuator probe. C_1 is the capacitance between concentric metal cylinders which are connected to opposite ends of the 9-MΩ resistor (R_1). Screw threads facilitate adjustment of the cylinders for variation of capacitance C_1.

Another 10 : 1 probe and its equivalent circuit are shown in Figure 11-26. In this case capacitor C_1 is a fixed quantity, and an additional variable capacitor (C_3) is included in parallel with C_i and C_{cc}. C_2 is now the total capacitance of C_i, C_{cc}, and C_3 in parallel. C_2 can be calculated from Equation 11-9.

The input capacitance and input resistance vary from one oscilloscope to another, even for otherwise identical instruments. *It is important that every probe be correctly adjusted when it is first connected for use with a particular oscilloscope.*



(a) 10:1 probe with connection box (Courtesy of Hewlett-Packard)



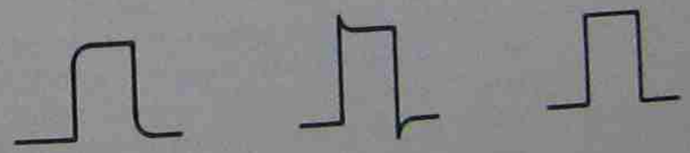
(b) Circuit of probe and oscilloscope input

FIGURE 11-26. Construction and circuit of a 10:1 oscilloscope probe using a correction box.

As already mentioned in Section 11-6, a square-wave calibration voltage is generated within the oscilloscope and connected to a terminal on the front panel. The probe is connected to this terminal to display the square wave on the screen. The variable capacitor is now adjusted until the displayed wave is perfectly square. The shape of waveform with a correctly compensated, under-compensated, and over-compensated probe is illustrated in Figure 11-27.

11-9-3 Active Probes

Active probes contain electronic amplifiers which increase the probe input resistance and minimize its input capacitance. Modern active probes use FET input stages, or FET input operational amplifiers. The circuit is



(a) Excessive attenuation of high frequencies – under compensated

(b) Overemphasis of high frequencies – over compensated

(c) Correctly compensated

FIGURE 11-27. Waveform of calibration voltage displayed when adjusting attenuator probes.

connected to function as a voltage follower (see Section 8-6-2). The amplifier has a gain of 1, and a typical input impedance of 1 MΩ||3.5 pF. Input impedances of 10 MΩ or greater are also possible with FET input stages, and the input capacitance effect can be further reduced by resistive attenuation. Power must be supplied to operate the amplifier. This may be derived from the oscilloscope, or the probe may contain its own regulated power supply with a line cord.

EXAMPLE 11-9 Determine the signal frequency at which a probe with $Z_i = 10\ \text{M}\Omega||3.5\ \text{pF}$ reduces the signal from a 600-Ω source by 3 dB.

SOLUTION

$$X_c = R_s,$$

$$1/(2\pi f \times 3.5\ \text{pF}) = 600\ \Omega$$

$$f = \frac{1}{2\pi \times 3.5\ \text{pF} \times 600\ \Omega}$$

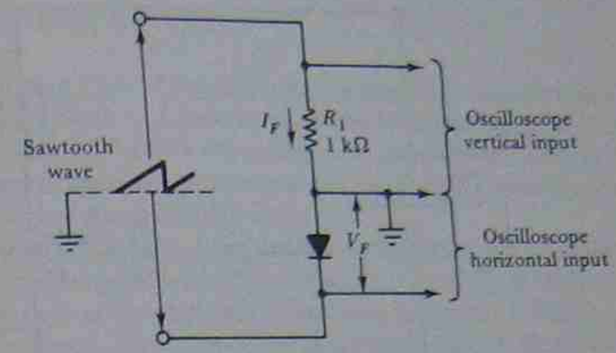
$$= 75.8\ \text{MHz}.$$

11-10 DISPLAY OF DEVICE CHARACTERISTICS

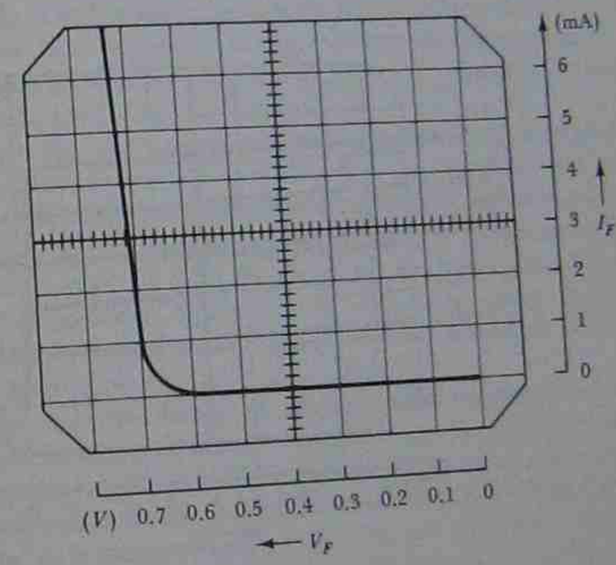
The characteristics of electronic devices can be displayed on an oscilloscope screen when the time base is disconnected from the horizontal input. On the HP 1222A oscilloscope (Figure 11-16), pushing the A-B SWP button disconnects the time base and connects channel *A* inputs to the horizontal deflection amplifier. Channel *A* input should now be made proportional to the horizontal component of the device characteristics, and channel *B* input should be proportional to the vertical component. Figure 11-28 illustrates the method of displaying the characteristics of a semiconductor diode.

In Figure 11-28(a). A 1-kΩ resistor (R_1) is connected in series with the device, and a sawtooth voltage wave is applied, as illustrated. The frequency of the sawtooth waveform could be anywhere between about 100 Hz and 1 kHz. The amplitude of the sawtooth should be equal to the maximum voltage drop that is going to occur across R_1 plus the voltage drop across the device. For a maximum forward current of 7 mA, as shown in Figure 11-28(b), the sawtooth waveform amplitude should exceed 7.7 V. The voltage across R_1 is applied to the oscilloscope vertical input channel, and that across the diode is applied to the horizontal input. Note that the common terminal is the grounded terminal for both channels.

With $R_1 = 1\ \text{k}\Omega$, the resistor voltage for each 1 mA of diode current is $1\ \text{mA} \times 1\ \text{k}\Omega = 1\ \text{V}$. Therefore, with the oscilloscope vertical deflection control set to 1 V/DIV, each 1 V of vertical deflection represents 1 mA of diode forward current. For the display shown in Figure 11-28(b), the horizontal deflection control is set to 0.1 V/DIV. Thus, each screen division represents 0.1 V of diode forward voltage.

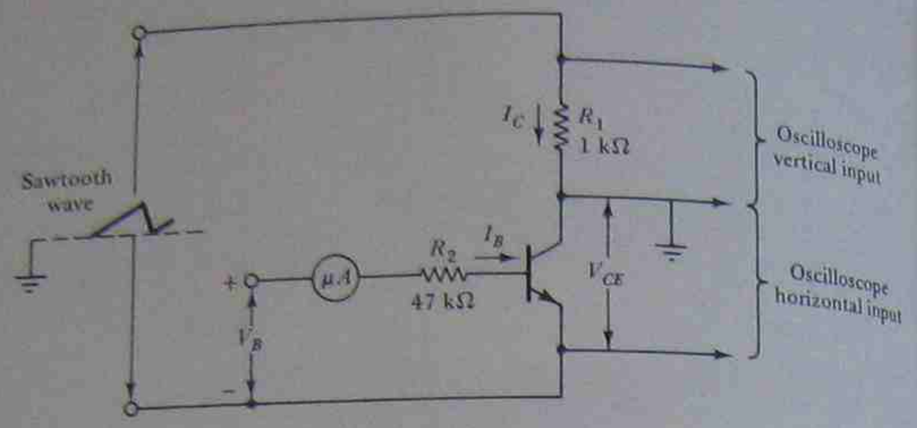


(a) Circuit for displaying diode forward characteristics

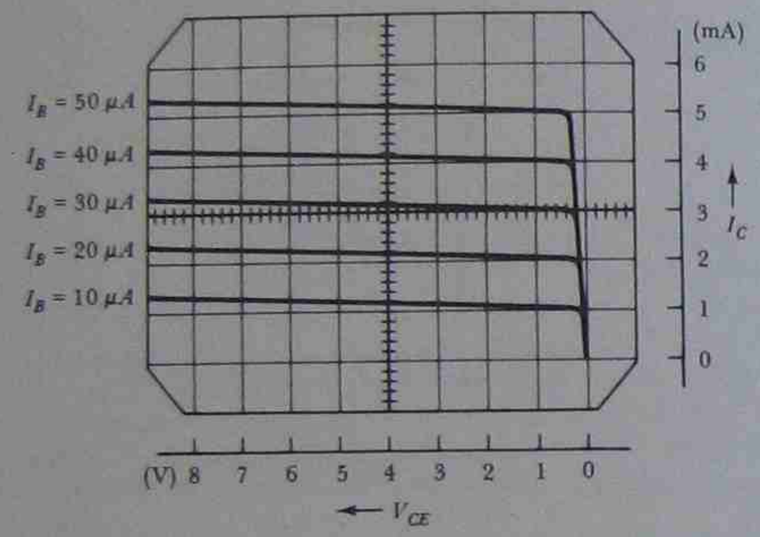


(b) Oscilloscope display of diode forward characteristics

FIGURE 11-28. Method of displaying diode forward characteristics on an oscilloscope.



(a) Circuit for displaying transistor collector characteristics



(b) Oscilloscope display of transistor collector characteristics

FIGURE 11-29. Method of displaying transistor collector characteristics on an oscilloscope.

During each cycle of the sawtooth, the applied voltage increases from zero, causing I_F and V_F to grow from zero and trace the device characteristics on the screen. When the sawtooth goes to ground level again, I_F and V_F are returned to zero. The characteristic of the diode is repeatedly traced at the frequency of the sawtooth waveform.

A permanent record of the device characteristics can be obtained by using an oscilloscope camera. The scales for I_F and V_F should be drawn along the edges of the photograph, as shown in Figure 11-28(b).

The collector characteristics of a transistor can be displayed on an oscilloscope by the method shown in Figure 11-29. As in the case of a diode, a sawtooth waveform is applied to the device via a 1-kΩ resistor (R_1). Once again the voltage across R_1 is applied to the oscilloscope vertical input. This makes the vertical deflection proportional to collector current I_C. The horizontal input is the device collector-emitter voltage V_{CE}. Transistor base current I_B is supplied from dc voltage source V_B via a 47-kΩ current-limiting resistor (R_2). A microammeter is included to monitor the level of I_B.

When the base current is set to 10 μA, the sawtooth input causes the I_C/V_{CE} characteristic for $I_B = 10$ μA to be traced on the oscilloscope screen. Only this single characteristic is displayed, and, as in the case of the diode, it is repeatedly traced at the frequency of the sawtooth. To display the characteristic for $I_B = 20$ μA, or for any other level of I_B, the base current is increased to the desired level. Once again, only this single characteristic is displayed on the screen. The amplitude of the sawtooth should be at least $V_{CE(max)} + (I_{C(max)}R_1)$.

The complete family of transistor collector characteristics can be captured on one photograph. The base current is first set to the required minimum level [10 μA in Figure 11-29(b)]. The camera is now placed over the oscilloscope screen, and a photograph is taken. Without removing the camera, I_B is increased to the next level, and the camera shutter is again triggered. The process is repeated until the characteristics for every desired I_B level are recorded on the same photograph. The scales for I_C and V_{CE} should be drawn at the edges of the photograph, and each I_B level should be identified [see Figure 11-29(b)].

11-11 LISSAJOU FIGURES

When the oscilloscope time base is disconnected and sine waves are applied to both horizontal and vertical inputs, the resulting display depends upon the relationship between the two sine waves. Very simple displays occur when the waveforms are equal in frequency. Quite complex figures may be produced with sine waves having different frequencies. In all cases these are known as *Lissajou figures*.

When only one input is applied, either a vertical line or a horizontal line results [Figure 11-30(a) and (b)]. Perfectly in-phase sine waves with

equal amplitudes produce a straight line at an angle of 45° from the horizontal, as shown in Figure 11-30(c). This is explained as follows. Both waveforms are at zero at the same instant. Therefore, there is neither vertical nor horizontal deflection, and the electron beam strikes the center of the screen [points 1 and 3 in Figure 11-30(c)]. When both waveforms are at maximum positive amplitude, maximum vertical and horizontal deflection is produced. The positive peak vertical input produces maximum positive (up-going) vertical deflection, and the positive peak horizontal input produces maximum right-hand side deflection. At this instant the electron beam is at point 2 in Figure 11-30(c). When the sine waves are at their negative peaks, maximum negative (down-going) vertical deflection and maximum left-hand side horizontal deflection occur. These conditions cause the electron beam to strike the screen at point 4 in Figure 11-30(c). The simultaneously changing voltage levels cause the beam to trace out the straight line between points 2 and 4.

Figure 11-30(d) shows that when the waveforms are in antiphase a line is traced at an angle of 135° with respect to horizontal. In this case, maximum positive vertical deflection occurs at the positive peak of the vertical input. However, at this instant the horizontal input is at its negative peak, and this produces maximum left-hand side deflection. Similarly, when the vertical input is at its negative peak and the horizontal input is at its positive peak, maximum negative vertical deflection and maximum right-hand side horizontal deflection results.

A circular display is produced when a 90° phase difference exists between vertical and horizontal inputs [Figure 11-30(e)]. When the vertical input is zero and the horizontal is at its negative peak, zero vertical deflection and maximum left-hand horizontal deflection occurs (point 1). When the horizontal input is zero and the vertical is at its positive peak, maximum positive vertical deflection and zero horizontal deflection results (point 2). At the instant of zero vertical input and maximum positive horizontal input, the beam experiences maximum right-hand side horizontal deflection and zero vertical deflection (point 3). Point 4 on the display is the result of zero horizontal input and maximum negative vertical input. The point at which the beam strikes, the screen rotates continuously, tracing the circular display.

When the phase difference between vertical and horizontal inputs is greater than zero but less than 90°, an elliptical display is traced, as illustrated in Figure 11-30(f). This is a thick (almost circular) ellipse when the phase difference is close to 90°. A near-zero phase difference produces a narrow ellipse. An ellipse tilted in the opposite direction is shown in Figure 11-30(g). This is the product of vertical and horizontal inputs with a phase difference greater than 90° but less than 180°. Once again, the ellipse may be thin or thick depending upon whether the phase difference is close to 180° or close to 90°. The actual phase difference between the

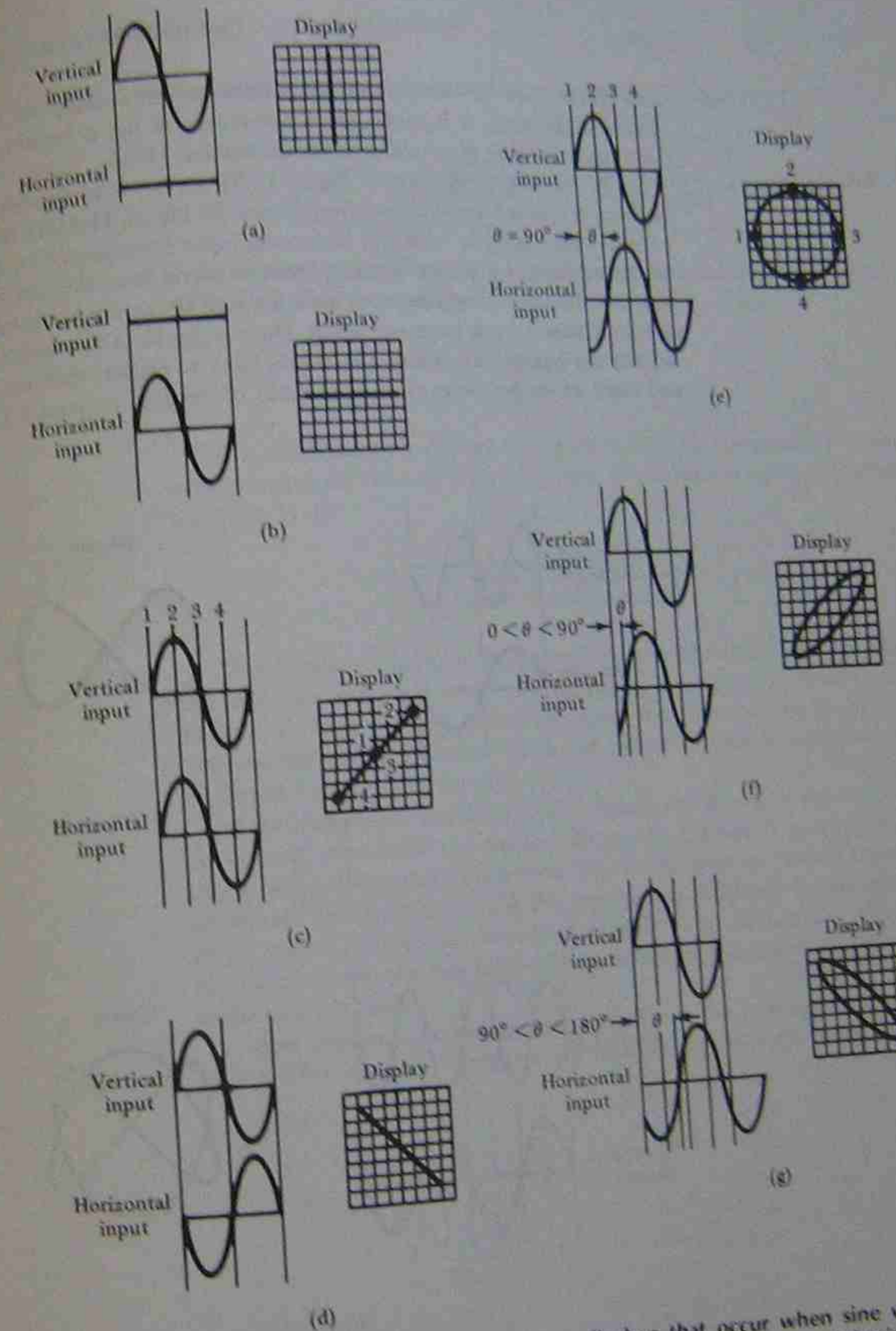
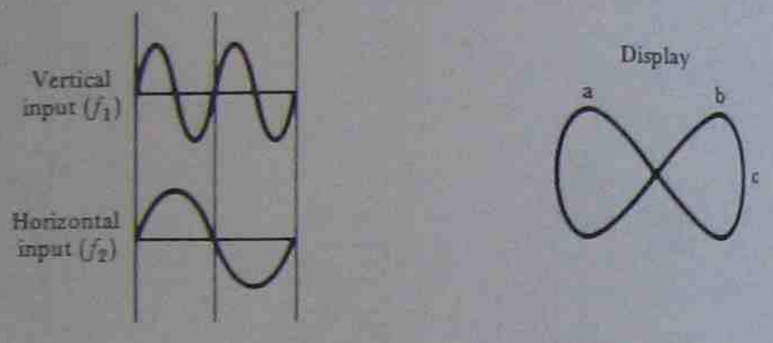


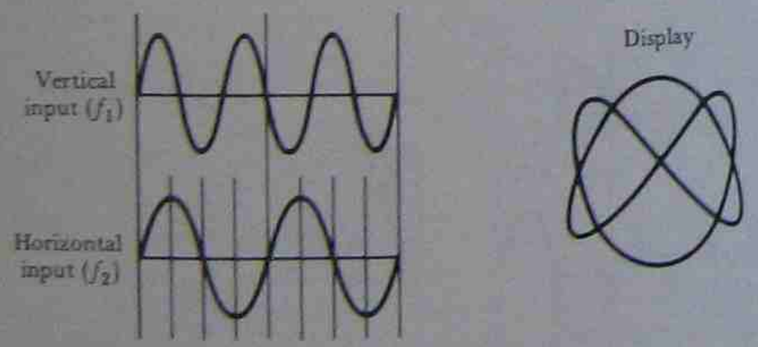
FIGURE 11-30. Various oscilloscope displays that occur when sine waves equal in frequency and amplitude are applied as vertical and horizontal inputs.

two waves may be determined from measurements made on elliptical displays. However, it is much more convenient to use a horizontal time base for measuring phase differences (see Section 11-7).

The oscilloscope displays in Figure 11-31 occur when the vertical and horizontal inputs have different frequencies. In Figure 11-31(a), the vertical input frequency is twice the horizontal input frequency. One cycle of horizontal input causes the electron beam to travel from the center of the screen to the right-hand side, then back through the center to the left-hand side, and finally back to center again. During this time the vertical input deflects the beam from center, up, down, back to center; then up, down, and back to center once more. The ratio of vertical frequency (f_1) to



(a) $\frac{f_1}{f_2} = 2$



(b) $\frac{f_1}{f_2} = \frac{3}{2}$

FIGURE 11-31. Complex oscilloscope displays occur when the vertical and horizontal inputs have different frequencies.

horizontal frequency (f_2) can be determined from the display:

$$\boxed{\frac{f_1}{f_2} = \frac{\text{(number of positive peaks)}}{\text{(number of right-hand side peaks)}}} \qquad (11\text{-}10)$$

In Figure 11-31(a) there are two positive peaks on the display: points *a* and *b*. There is only one right-hand side peak: point *c*. Thus,

$$\frac{f_1}{f_2} = \frac{2}{1}.$$

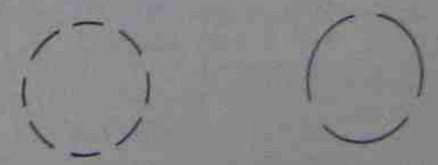
The more complex display in Figure 11-31(b) is the result of inputs with a frequency ratio of 3 : 2. The ratio is determined, as before, from Equation 11-10:

$$\frac{f_1}{f_2} = \frac{\text{(3 positive peaks)}}{\text{(2 right-hand side peaks)}} = \frac{3}{2}.$$

The displayed Lissajou figures can become extremely complex when the frequency ratios are other than the simple 2 : 1 and 3 : 2 ratios used in Figure 11-31. Also, for a stationary figure there must be an exact ratio between the two frequencies. When the frequency ratio is not exact, the displayed figure changes continuously.

Two broken-line circular Lissajou figures are shown in Figure 11-32. As already explained, the circular display is a result of two sinusoidal inputs with a 90° phase difference. The waves must be exactly equal in amplitude and frequency, and this can be best achieved by applying a single sine wave to two *phase shift networks*. The broken line effect is achieved by using another higher frequency wave to modulate the intensity of the electron beam.

Most oscilloscopes have a (rear) connector for intensity modulation inputs. This is usually termed *Z axis modulation*. The input wave actually



(a) $f_m = 8\,f_P$ (b) $f_m = 5\,f_P$

FIGURE 11-32. A broken-line circle is displayed when a circular trace is intensity modulated.

modulates the voltage on the grid of the oscilloscope (see Figure 11-1). Thus, the grid voltage is driven more negative during each negative half cycle of the modulating wave. This either dims the intensity of the trace or causes it to be completely blanked. Each short line and gap in the circular figure represents one cycle of modulating frequency. Each trace of circular figure is completed by one cycle of the vertical and horizontal inputs. Therefore, the ratio of modulating frequency to deflecting plate frequency is

$$\frac{f_m}{f_p} = \frac{\text{number of gaps in circle}}{1}. \qquad (11\text{-}11)$$

Where the ratio of $f_m : f_p$ is not an exact quantity, the gaps in the circle rotate.

Another type of Lissajou figure may be generated by displaying a circle, and modulating the final anode of the oscilloscope. Modulation of the (circle-generating) deflecting plate input voltages produces still another family of figures.

REVIEW QUESTIONS AND PROBLEMS

11-1. Sketch the basic construction of a cathode ray tube. Identify each section of the tube, and show typical supply voltages at each appropriate point. Carefully explain the operation of the CRT.

11-2. Sketch the focusing section of a CRT. Show the equipotential lines and their effect on electrons traveling from the cathode to the screen. Explain.

11-3. Draw a sketch to illustrate electrostatic deflection. Explain. Define *deflection factor* and *deflection sensitivity* for a CRT.

11-4. Discuss the screen of a CRT and the factors affecting the brightness of the display.

11-5. Sketch the basic circuit of an oscilloscope deflection amplifier together with an input attenuator. Carefully explain the operation of the circuit.

11-6. A 1-kHz triangular wave with a peak amplitude of 10 V is applied to the vertical deflecting plates of a CRT. A 1-kHz sawtooth wave with a peak amplitude of 20 V is applied to the horizontal deflecting plates. The CRT has a vertical deflection sensitivity of 0.4 cm/V, and a horizontal deflection sensitivity of 0.25 cm/V. Assuming that the two inputs are synchronized, determine the waveform displayed on the screen.

11-7. Repeat Question 11-6 with the triangular wave frequency changed to 2 kHz.

11-8. Sketch the basic circuit and output waveforms of an oscilloscope sweep generator. Carefully explain the circuit operation.

11-9. A sweep generator, as shown in Figure 11-7, has the following components: $R_1 = 4.7$ kΩ, $R_2 = 8.2$ kΩ, $R_3 = 3.3$ kΩ, $C_1 = 0.5$ μF, $R_5 = 12$ kΩ, $R_6 = 4.7$ kΩ. The supply voltages are ±12 V, and the transistors are silicon. Calculate the peak-to-peak amplitude and the time period of the ramp waveform.

11-10. The ramp output from the circuit described in Question 11-9 is to have its time period doubled. How should C_1 be modified? If the time period is to be adjustable by ±10%, what modifications should be made?

11-11. Sketch the block diagram of an automatic time base for an oscilloscope. Show the waveforms at various points in the system, and carefully explain the operation of the time base.

11-12. Using illustrations, explain the function of a hold-off circuit in an oscilloscope time base.

11-13. Using illustrations, show how a dc output level control on a triggering amplifier can be used to adjust the instant at which a displayed waveform commences on an oscilloscope.

11-14. Explain blanking and unblanking in an oscilloscope, and discuss the need for blanking.

11-15. Sketch the construction of dual-beam and split-beam oscilloscopes. Briefly explain.

11-16. Sketch the deflection system for: (a) a dual-beam oscilloscope, (b) a single-beam dual-trace oscilloscope. Explain the operation of the single-beam dual-trace system. Also explain the use of this system in chop mode and in alternate mode. Sketch waveforms to illustrate the two modes of operation.

11-17. Briefly discuss each of the following oscilloscope controls: intensity, focus, position, dc shift, volts/div, time/div, trigger level.

11-18. Briefly discuss the procedure for making amplitude and time measurements on an oscilloscope.

11-19. If the waveforms illustrated in Figure 11-17 occur when the time/div control is set to 0.1 ms, and the volts/div control is at 500 mV, determine the peak amplitude and frequency of each waveform.

11-20. For the waveforms illustrated in Figure 11-18, the time/div control is at 50 ms, and the volts/div control is set to 20 mV. Determine the peak amplitude and frequency of each waveform, and calculate the phase difference.

11-21. In Figure 11-18, how many horizontal divisions would there be between the beginning of each waveform cycle for a phase difference of 25°?

11-22. If the waveforms shown in Figure 11-19 occur when the time/div control is set to 10 ms and the volts/div control is at 5 V, determine the peak amplitude and frequency of each waveform.

11-23. Two waveforms (A and B), each occupying five horizontal divi-

sions for one cycle, are displayed on an oscilloscope. Wave B commences 1.6 divisions after commencement of wave A. Calculate the phase difference between the two.

11-24. If the waveforms shown in Figure 11-20 occur when the volts/div control is set to 0.1 V and the time/div control is at 20 μs, determine: each pulse amplitude, the pulse frequency, the delay time, the rise time, and the fall time.

11-25. Using illustrations, explain the kind of pulse wave distortion that can occur with: (a) a coupling capacitor, (b) oscilloscope input capacitance. Define the circuit time constant in each case.

11-26. A pulse wave from a signal generator with a source resistance of 600 Ω is to be displayed on an oscilloscope with $R_i = 1$ MΩ, $C_i = 30$ pF and $C_c = 0.1$ μF.

(a) Determine the width of the longest pulse that can be displayed without distortion when the oscilloscope input is set to ac.

(b) Calculate the width of the shortest pulse that may be displayed without distortion when the input is set to dc.

11-27. Describe a 1 : 1 probe for use with an oscilloscope. Sketch the circuit diagram for the probe together with the signal source and the oscilloscope input. Briefly explain.

11-28. A signal with an amplitude of $V_s = 500$ mV and a source resistance of 1 kΩ is connected to an oscilloscope with $R_i = 1$ MΩ in parallel with $C_i = 40$ pF. The coaxial cable of the 1 : 1 probe used has a capacitance of $C_{cc} = 80$ pF. Calculate the signal voltage level (V_i) at the oscilloscope terminals when the signal frequency is 120 Hz. Also calculate the signal frequency at which V_i is 3 dB below V_s.

11-29. Sketch the construction of a 10 : 1 attenuator probe for use with an oscilloscope. Sketch the circuit diagram of the probe together with the signal source and the oscilloscope input. Briefly explain.

11-30. A 10 : 1 oscilloscope probe, as shown in Figure 11-25, is used with an oscilloscope with $R_i = 1$ MΩ and $C_i = 40$ pF. If the probe uses a 9-MΩ series resistor, and the coaxial cable has a capacitance of 80 pF, determine the value of capacitor C_1 that should be connected in parallel with the 9-MΩ resistor. Also calculate the signal frequency at which this probe will produce a 3-dB reduction in signal from a 1-kΩ source.

11-31. Describe a 10 : 1 oscilloscope probe that uses a correction box. Sketch its equivalent circuit.

11-32. Discuss the adjustment of oscilloscope probes, and show the various waveforms that can occur when adjusting a probe.

11-33. Briefly discuss active probes for use with oscilloscopes.

11-34. Sketch a circuit diagram for displaying the characteristics of a diode on an oscilloscope. Explain the operation of the circuit, and sketch the type of display that is created.

11-35. Sketch a circuit diagram for displaying the collector characteristics of a transistor on an oscilloscope. Explain the operation of the circuit, and sketch the type of display that occurs. Explain how a complete family of transistor characteristics can be captured on one photograph.

11-36. Sketch the oscilloscope display that occurs with sine wave vertical and horizontal inputs that: (a) are in phase, (b) are in antiphase, (c) have a phase difference of 90°, and (d) have a phase difference greater than zero but less than 90°.

11-37. Sketch the oscilloscope display that occurs with two synchronized sine waves when: (a) the horizontal input has a frequency twice that of the vertical input and (b) the ratio of vertical input frequency f_1 to horizontal input f_2 is $f_1/f_2 = 3/2$.

11-38. Describe how a broken line circular display may be produced on an oscilloscope. Explain the frequency ratio involved.

12

SPECIAL OSCILLOSCOPES

INTRODUCTION

An oscilloscope with a *delayed time base* has two time base generators: a normal time base, and an additional delayed time base, which is superimposed upon the normal time base output. This facility allows any portion of a displayed waveform to be brightened when the oscilloscope is operating on a normal time base. Switching to delayed time base causes the brightened portion to completely fill the screen for detailed investigation.

Many special oscilloscopes use a normal type of cathode ray tube (CRT) together with special control and input circuitry. An exception to this is the *analog storage oscilloscope*, which employs a special type of CRT. Signal waveforms are stored on electrodes within the CRT. This instrument is particularly useful for investigation of nonrepetitive, single-event signals.

A signal with a frequency too high for displaying on a normal oscilloscope can be sampled to create a dot waveform display. A *sampling oscilloscope* samples a repetitive signal once per cycle at different points during the repeating cycle. The samples are used to construct a low-frequency representation of the high-frequency waveform. Single-event signals cannot be investigated in this way.

A *digital storage oscilloscope* might be thought of as a combination of the sampling and storage oscilloscopes. Input signal are sampled, and the samples are stored in a digital memory. No special CRT is involved. The stored samples are recalled from the memory to reconstruct the original

input waveform for display. The digital oscilloscope can be used for both single-event and repetitive signals.

12-1 DELAYED TIME BASE OSCILLOSCOPE

12-1-1 Need for a Time Delay

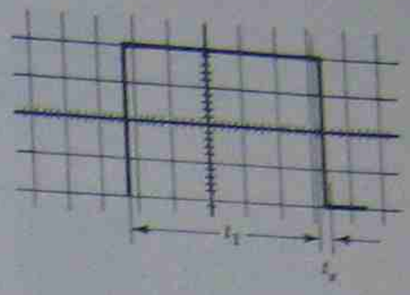
The need for a time delay system in an oscilloscope is illustrated by Figure 12-1. For the square wave shown in Figure 12-1(a), the portion identified as t_x is to be studied. This includes the trailing edge of the waveform and part of the wave immediately preceding the trailing edge. When the oscilloscope is triggered on the leading edge of the wave, the time base sensitivity can be adjusted to make the waveform fill the screen. For $(t_1 + t_x) = 100\ \mu s$, the maximum time base sensitivity that can be used is 10 μs/div. A more sensitive setting eliminates the trailing edge of the wave from the display. In the resultant trace [Figure 12-1(b)], time t_x occupies a fraction of a horizontal division on the oscilloscope screen. Using the 10 times magnifier on the time base together with the horizontal shift control, t_x may be made to fill more than one horizontal division of the oscilloscope screen. This is illustrated in Figure 12-1(c). If the oscilloscope time base is triggered by the trailing edge of the wave (and adjusted for greatest sensitivity), only part of the portion to be investigated is displayed [Figure 12-1(d)].

The display shown in Figure 12-1(c) is the best that can be obtained with an ordinary oscilloscope. No further horizontal expansion of t_x is possible. Instead of triggering the oscilloscope time base from the leading edge of the waveform in Figure 12-1(a), suppose a *time delay circuit* is triggered to give a delay of approximately 90 μs. At the end of this 90 μs, the oscilloscope time base is triggered so that the display commences at the start of t_x [Figure 12-2(a)]. Such an arrangement would allow a time base sensitivity to be used that causes t_x to completely fill the oscilloscope screen horizontally [Figure 12-2(b)]. This is essentially what occurs in an oscilloscope with a delayed time base. The portion of the waveform to be studied is selected, and a time delay is introduced as required. The delayed time base circuits allow the desired portion of the displayed waveform to be brightened for identification. Then the necessary time delay is introduced simply by throwing a switch.

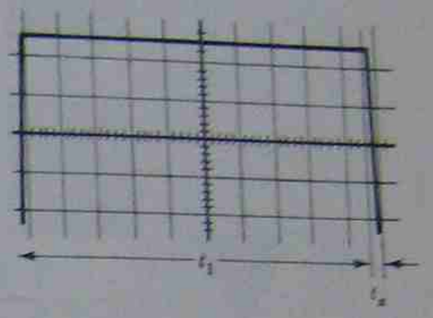
12-1-2 Delayed Time Base System

The block diagram and waveforms for a delayed time base system are illustrated in Figure 12-3. The main time base (MTB) is triggered as explained in Section 11-4-2. Also, as already explained, the MTB blanking circuit generates an unblanking pulse to turn on the electron beam in the CRT during the display sweep time. The MTB ramp output is fed via switch S (in Figure 12-3) to the horizontal deflection amplifier. The MTB ramp also goes to one input of a *voltage comparator*. The voltage comparator *compares* the levels of two input voltages and produces a negative (or

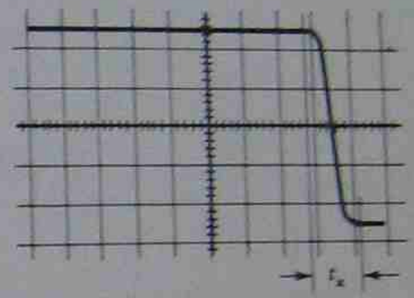
(a) Square waveform in which trailing edge (during t_x) is to be studied.



(b) With the time base triggered on the leading edge and best sensitivity, the wave fills the screen. t_x still occupies only a small portion of the screen.



(c) Conditions as in (b) above, but using the 10 X control on the time base.



(d) Triggering on the trailing edge of the waveform, much of t_x is lost.

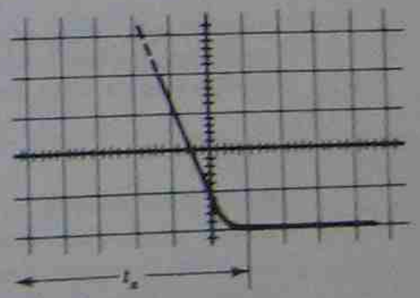
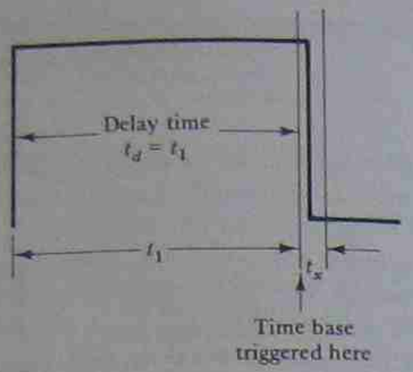
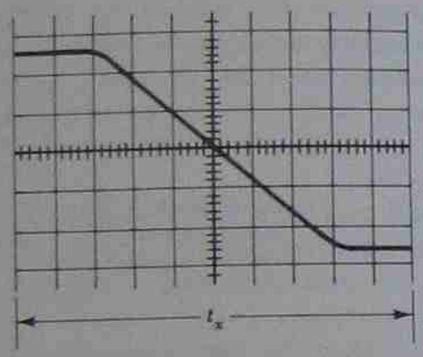


FIGURE 12-1. On an oscilloscope without a delayed time base, the detail in which a portion of the waveform can be studied is limited by the time (t_1) from the triggering point to the portion to be investigated.



(a) Time base triggering is delayed by time $t_d = t_1$



(b) With delayed triggering, t_x can be made to fill the screen.

FIGURE 12-2. When a time delay circuit is triggered at the leading edge of a pulse, and the oscilloscope time base is triggered after delay time t_d, the portion t_x of the wave can be studied in detail.

positive) output spike at the instant that the two voltage levels become exactly equal. The voltage level at the other input of the comparator is controlled by a potentiometer, as illustrated. When the instantaneous level of the MTB ramp becomes equal to the potentiometer voltage, the comparator generates an output spike to trigger the delayed time base (DTB). The delay time t_d for the MTB ramp to become equal to the potentiometer voltage can obviously be altered by adjusting the potentiometer.

Like the MTB, the DTB also has a blanking circuit that generates an unblanking pulse during the DTB ramp time. The two unblanking pulses are added together in a *summing circuit* before being applied to the grid of

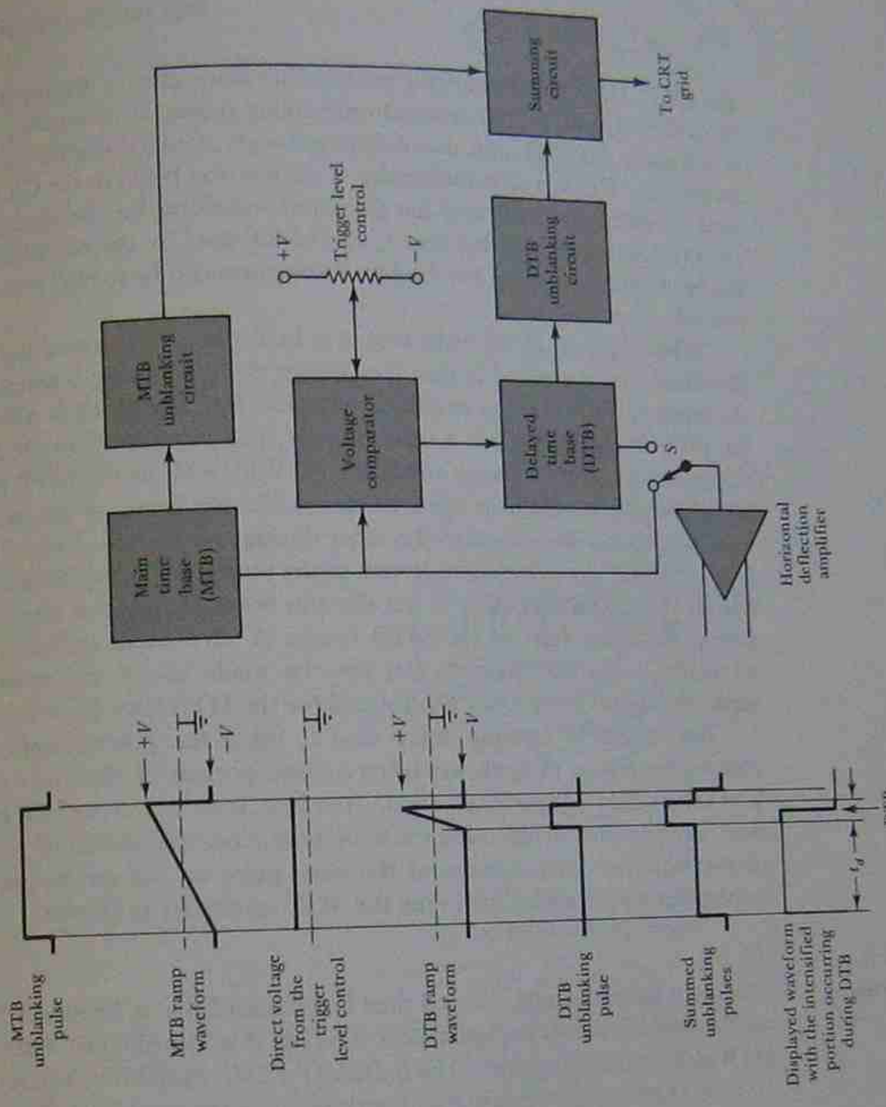


FIGURE 12-3. Delayed time base system and waveforms.

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the CRT. The MTB unblanking pulse acting alone gives a displayed trace of uniform intensity. The summed unblanking pulses, as illustrated, apply a voltage to the CRT grid that is approximately doubled during the DTB ramp time. This increases the density of the electron beam in the CRT and thus intensifies (or brightens) the displayed waveform for the duration of the DTB ramp. Since delay time t_d can be adjusted by the potentiometer, the brightened portion of the displayed waveform can be moved around as desired.

When the part of the wave that is to be further investigated has been identified and brightened as described above, the DTB ramp is switched to the input of the horizontal amplifier via switch S in Figure 12-3. Although the DTB ramp usually has a much shorter time duration than the MTB ramp, it does have the same amplitude ($-$V to $+$V) as the MTB ramp. Consequently, it can cause the oscilloscope electron beam to be deflected from one side of the screen to the other during the shortened ramp time. Now, only the formerly bright portion of the waveform is displayed on the screen. Horizontal deflection of the electron beam commences after delay time t_d from the start of the MTB sweep. A very small section of the waveform under investigation can now be made to fill the screen by adjusting the DTB time/div control and/or the DTB *times 10* switch.

The system of creating delay time t_d using the potentiometer and comparator results in t_d always being a fixed portion of the main sweep time rather than a fixed time period. That is, t_d is set in terms of the MTB time/div selection. When using the main time base, the intensified portion of the displayed wave remains at the same point on the screen (not the same point on the wave) each time the MTB sensitivity is altered.

12-1-3 Controls

The main time base and delayed time base controls for a Tektronix 2215 oscilloscope are shown in Figure 12-4. The MTB is identified as *A* and the DTB as *B* on this instrument. The *B DELAY TIME POSITION* control is a 10-turn potentiometer, which sets the delay time (as explained above) in terms of the (MTB) *A SEC/DIV* selection.

The *A* and *B SEC/DIV* controls are combined, as illustrated. A clear plastic disc is rotated over the time/div scale by means of a knob to the desired *A SEC/DIV* range. The selected range shows between two black lines on the plastic disc. The *B SEC/DIV* range is set by pulling out the knob and rotating it. A white line on the knob identifies the selected (DTB) range. A vernier control incorporated in the knob provides continuous (uncalibrated) adjustment of the *A SEC/DIV* setting. A 10 times magnifier switch is operated by pulling out the *A* and *B SEC/DIV* knob. This increases the displayed time/div sensitivity by a factor of 10.

The *HORIZONTAL MODE* switch (in Figure 12-4) facilitates selection of time base *A* or *B* (MTB or DTB respectively). Alternate mode (*ALT*)

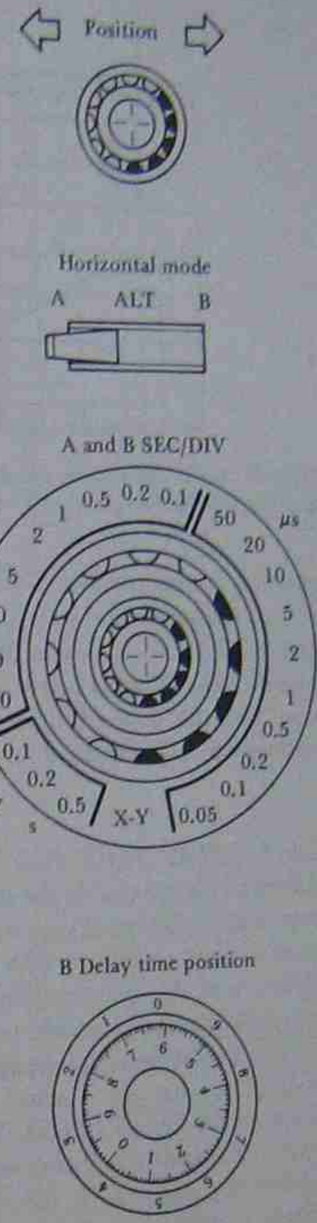


FIGURE 12-4. Main and delayed time base controls for a Tektronix 2215 oscilloscope (Courtesy of Tektronix Inc.).

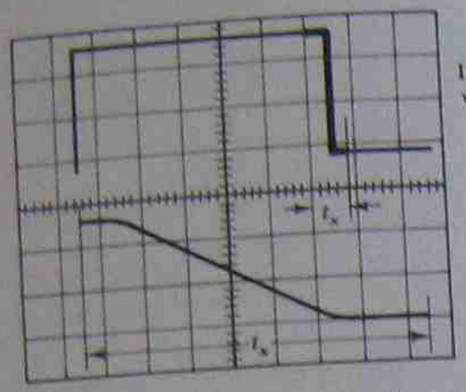


FIGURE 12-5. By means of alternate time base mode, the whole waveform and the intensified portion can be displayed simultaneously.

selection is also possible. This allows the entire waveform and the magnified portion to be simultaneously displayed as two separate traces (see Figure 12-5). In alternate mode, the input terminal of the horizontal amplifier (in Figure 12-3) is alternately switched between the main time base and the delayed time base. The two displays can be separated vertically by adjustment of an *A/B SWP SEP* control (not shown).

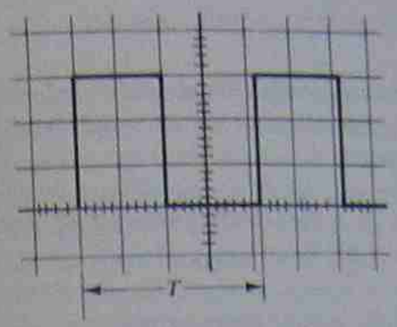
12-1-4 Applications

The *B DELAY TIME POSITION* control (Figure 12-4) has a 10-turn calibrated dial to enable the delay time to be set precisely. This affords a very accurate means of time measurement. Consider Figure 12-6(a), which shows a pulse waveform with a time period T. With the MTB set at 1 μs/div, and the distance between leading pulse edges estimated as 4.2 horizontal divisions, the time period is: $T = 4.2\ \mu s$.

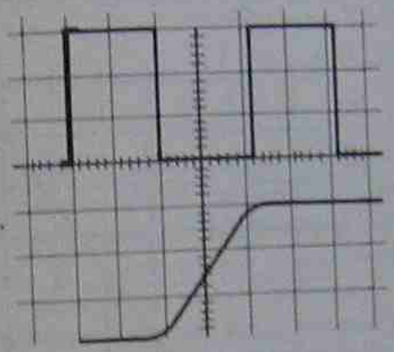
For a more accurate measurement of T, the time delay control is first adjusted so that the leading edge of the first pulse is intensified, as illustrated in Figure 12-6(b). With *alternate mode* display, the delay time control is carefully adjusted to set the half-amplitude point of the (DTB displayed) pulse edge at the central vertical line on the screen graticule [Figure 12-6(b)]. The dial setting (D_1) of the delay time control is noted. Now the delay time is adjusted to move the intensified zone from the leading edge of the first pulse to the leading edge of the second pulse [Figure 12-6(c)]. Further fine adjustment of the delay time is made to once again set the (DTB displayed) pulse edge so that its half-amplitude point coincides with the central vertical graticule line. The new dial setting (D_2) of the delay time control is noted. The time between the two leading edges of the pulse wave is determined as:

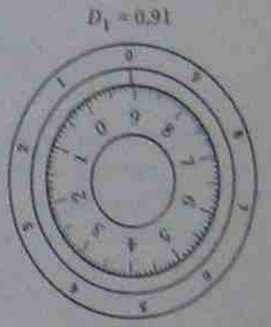
$$T = (D_2 - D_1) \times (\text{MTB time/div})$$

(a) Display using main time base.

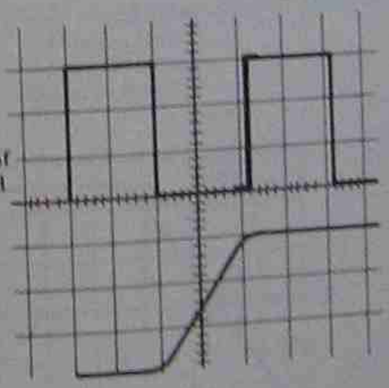


(b) Alternate display of main time base and delayed time base at leading edge of first pulse.





(c) Alternate display of main time base and delayed time base at leading edge of second pulse.



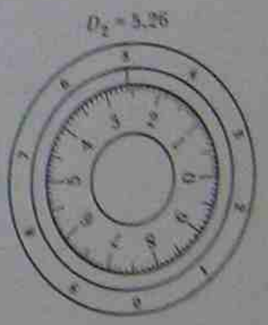
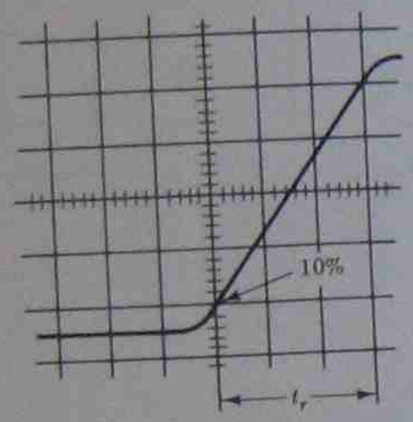


FIGURE 12-6. Use of delayed time base for accurate measurement of time period of a waveform.

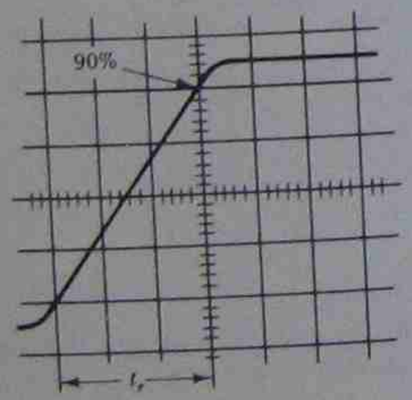
For the time period previously estimated as 4.2 μs, the dial settings of the time delay control might be: $D_1 = 0.91$ and $D_2 = 5.26$. Then with the MTB at 1 μs/div:

$$T = (5.26 - 0.91) \times (1\ \mu\text{s/div})$$
$$= 4.35\ \mu\text{s}$$

The rise time (or fall time) of a pulse can also be measured accurately by means of the calibrated DTB control. Figure 12-7 illustrates the process. After the desired portion of the displayed waveform has been identified by



(a) Delay time control adjusted to set 10% point at center of screen



(b) Delay time control adjusted to set 90% point at center of screen

FIGURE 12-7. Measurement of rise time by use of delayed time base.

brightening it, the oscilloscope is switched to DTB. The type of display shown in Figure 12-7(a) is now obtained. The rise time (t_r) is defined as the time for the leading edge of the wave to go from 10% to 90% of its amplitude (see Section 11-8). By carefully adjusting the delay time control, the 10% point on the pulse wave is set at the center of the screen graticule [Figure 12-7(a)]. Suppose the DTB control dial is $D_1 = 0.51$ at this point. The DTB control is now readjusted to set the 90% point on the pulse edge to the center of the screen [Figure 12-7(b)], and the dial reading is again noted. If the dial now reads $D_2 = 3.93$, the rise time is calculated as:

$$t_r = (D_2 - D_1) \times (\text{MTB time/div})$$
$$= (3.93 - 0.51) \times (1\ \mu\text{s/div})$$
$$= 3.42\ \mu\text{s}$$

One more application of the delayed time base is illustrated in Figure 12-8. Sometimes the time period (T) between leading edges in a repetitive pulse wave varies slightly from one pair of pulses to the next. This effect occurs, for example, when a pulse wave is played back from a magnetic tape recorder. Because of tape speed variations during the record and playback process, there is a continuous fluctuation in time period T. This is known as *flutter*, when a tape recorder is involved, or as *pulse jitter*, when the waveform is derived from some other source.

To measure pulse jitter, the leading edge of the second pulse is intensified, as shown in Figure 12-8(a). With alternate mode display, the

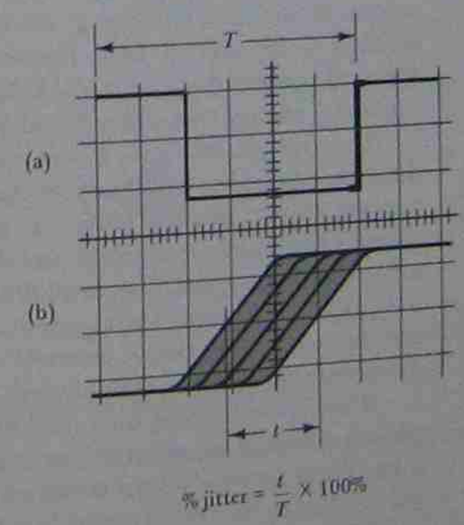


FIGURE 12-8. Pulse jitter (or flutter) can be measured by use of delayed time base.

DTB display in Figure 12-8(b) is produced. The display is a thick blur of pulse edges varying in horizontal position due to pulse jitter. The thickness (t) of the display is measured by means of the DTB control and dial, as already explained. The percentage of flutter or jitter is calculated simply by expressing t as a percentage of the waveform time period T.

12-2 ANALOG STORAGE OSCILLOSCOPE

12-2-1 Operation of Storage Oscilloscope

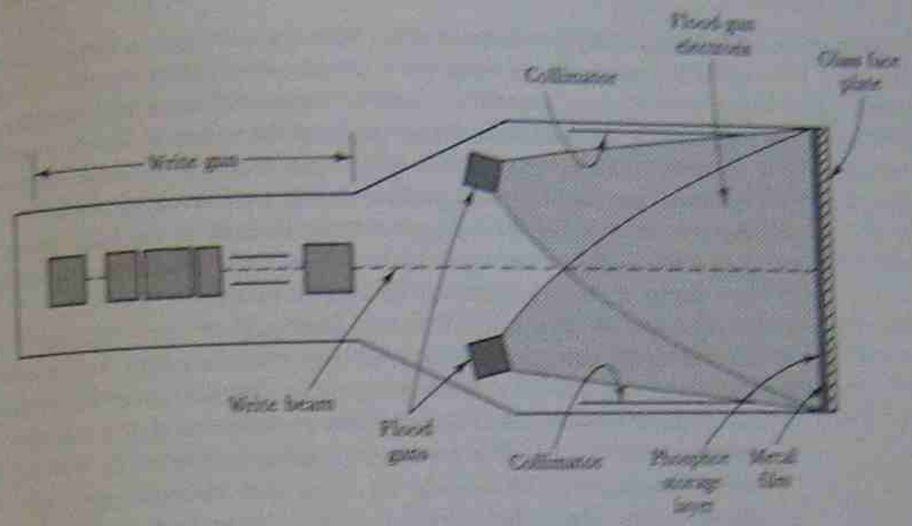
The phosphor materials used on the screen of an oscilloscope normally glow for a period of only milliseconds. This is referred to as *persistence*. A short persistence display is satisfactory for most waveforms studied. However, when very low frequency signals are displayed, a short persistence screen shows a dot tracing out the wave, rather than the actual waveform. If the screen can be made to continue glowing along the path of the traced-out wave (long persistence), then the actual waveform of the signal can be viewed more easily. Another situation in which ordinary oscilloscopes are unsatisfactory is the case of a *transient*. This is a nonrepetitive waveform that appears only once (for example, when a power supply is switched on). In a *storage oscilloscope*, the waveform is retained and can be displayed continuously for an hour or more. A special type of CRT is required to achieve this effect.

Figure 12-9(a) shows the basic construction of a *bistable* storage CRT. The term *bistable* is applied to a CRT that can display a stored waveform at only one level of brightness. The waveform is either displayed or not displayed. No variation in display intensity is possible. The screen has a storage layer of phosphor material that is capable of *secondary emission* and which has a very high insulation resistance between particles. (Secondary emission occurs when high-energy electrons strike a surface and cause other electrons to be emitted from the surface.) A transparent *metal film* is deposited between the glass of the CRT screen and the storage layer. The *collimator* is another metal film deposited around the neck of the tube.

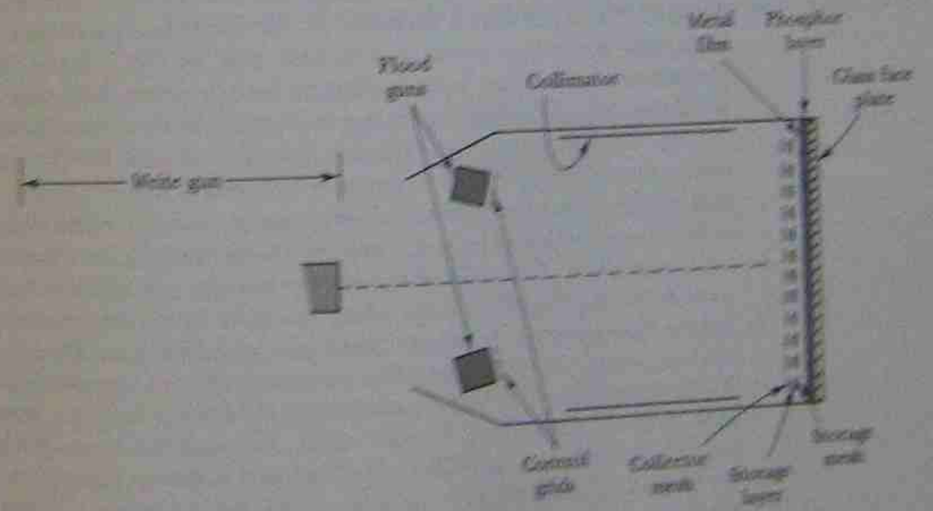
The *write gun* in Figure 12-9(a) is made up of the accelerating and deflecting electrodes, as already discussed in Section 11-1. The *two flood guns* are simply cathodes heated to generate low-energy electrons. The cathodes are at ground potential, and the collimator may also be at ground level or slightly positive. The metal film is at a potential of +1 V to +5 V with respect to ground. The clouds of electrons emitted by the flood guns are attracted by the positive potential on the metal film so that they flood the screen with electrons, as illustrated.

If the electron beam from the write gun has not been activated, the phosphor layer is not affected by the low-energy electrons from the flood guns. These electrons do not penetrate the phosphor and are collected by the collimator. No display occurs in this circumstance.

Now consider what happens when the write gun is energized and a waveform is applied to the oscilloscope input for a very brief time period.



(a) Bistable type storage CRT



(b) Variable persistence storage CRT

FIGURE 12-9. Bistable and variable persistence type storage cathode ray tubes.

The beam of high-velocity electrons from the write gun is deflected across the CRT screen. These electrons strike the phosphur layer with sufficient energy to produce secondary emission. The emitted secondary electrons are collected by the collimator. Every point on the screen at which secondary emission occurs becomes positively charged because electrons have been lost from that point. Thus, a positive charge path is traced on the storage layer in the shape of the input waveform. Because of the high insulation properties of the storage layer, there is very little charge carrier leakage, and the positive charge path can remain for hours.

The low-energy electrons from the flood guns are now attracted to the positive charge path, and they pass through it to the (more positive) metal film. In passing through the storage layer, the electrons cause the phosphor to continue glowing. In this way, the one-time-occurring transient is displayed continuously. Erasure of the display is effected by making the metal film negative. This repels the flood gun electrons back into the storage layer, where they accumulate and return the written area to the same potential as the surrounding material.

A storage CRT capable of *variable persistence* operation is shown in Figure 12-9(b). The major difference between this tube and the CRT in Figure 12-9(a) is that a fine wire *storage mesh* and a *collector mesh* are now included. The *storage layer* is deposited on the inside surface of the storage mesh, and the screen is just the normal type of CRT screen with a low-persistence phosphor layer backed by an aluminum film. One additional change is that control grids are included in front of each flood gun.

The collector mesh has a positive potential around 100 V, and the voltage on the storage mesh is typically between 0 V and −10 V. The high-energy electron beam from the write gun produces secondary emission at the storage layer and creates a positive charge path in the shape of the input waveform. Flood gun electrons (low energy) are repelled from all parts of the storage layer except where the write beam has produced the positive charge path. Here, the flood gun electrons pass through and produce a trace on the screen. The secondary emitted electrons and the flood gun electrons that do not pass through the storage layer are attracted back to the highly positive collector mesh. Although the screen phosphor has low persistence in this CRT, the flood gun electrons passing through the positive trace on the storage layer continue to maintain a display on the screen.

Erasure of the stored waveform is effected by connecting the storage mesh to the same high positive voltage as the collector mesh for a brief time period. In this case, the flood gun electrons produce secondary emission all over the storage layer so that the written waveform is wiped out. The storage mesh is then returned to its normal voltage level. Erasure can also be performed by adjusting the display persistence control.

Variation of the display persistence is obtained by slowly erasing the stored waveform. A repetitive negative pulse (−4 V to −11 V) is applied to the storage mesh to discharge the positively charged areas. The pulse has a constant frequency of 1200 Hz typically, and the pulse width is continuously variable. The narrowest pulses give the longest display persistence, and the wider pulses shorten the persistence by discharging the storage layer more rapidly. Alternatively, the pulse width might be maintained constant and the frequency increased or decreased to shorten or lengthen the persistence.

The brightness of the displayed waveform depends upon the number and energy of the flood gun electrons that strike the screen. The voltage applied to the grids of the flood guns controls these electrons. A high negative voltage completely cuts off the flood gun electrons. A zero voltage level on the grids permits maximum electron flow.

12-2-2 Storage Oscilloscope Controls

The storage controls on the front panel of an HP1741A variable persistence/storage oscilloscope are shown in Figure 12-10. The *BRIGHTNESS* control knob adjusts a potentiometer, which controls the voltage level on the flood gun grids. The *PERSISTENCE* control sets the width of the negative discharge pulse waveform that is continuously applied to the



FIGURE 12-10. Storage controls on the HP1741A variable persistence storage oscilloscope (Courtesy of Hewlett-Packard).

storage mesh. A pushbutton at the center of the persistence control facilitates rapid erasure of the stored waveform by connecting the storage mesh to the collector mesh.

Three functions are available: *WRITE*, *STORE*, and *DISPLAY*. To store a repetitive waveform, the *WRITE* function is selected, and the persistence and brightness are adjusted for a satisfactory display. Then the *STORE* function is selected. This cuts off the write beam so that the waveform already written on the storage layer is retained at maximum persistence. The stored waveform is displayed by selecting the *DISPLAY* function, which switches on the flood gun electrons. More than one event may be successively stored on different parts of the storage mesh by using the oscilloscope vertical control to set each waveform to a convenient position on the screen. All stored waves may then be displayed simultaneously for comparison.

In general, for displaying a very low frequency signal, the persistence control should initially be set to *NORMAL* and the write beam *INTENSITY* control should be adjusted until the moving spot intensity is acceptable. Then the *PERSISTENCE* and *BRIGHTNESS* controls should be alternately adjusted by small amounts until a satisfactory display is obtained. To capture a transient, the brightness should be set to minimum, the persistence to maximum, and the *WRITE* function selected. When the transient has been applied to the oscilloscope, the *DISPLAY* function can be selected and the brightness adjusted as necessary. If the write beam intensity is too great, a *blooming* effect (or bright out-of-focus condition) of the displayed waveform may be created. The intensity of the write beam should be experimented with to obtain a nonblooming display. If the transient cannot be continuously repeated, then it might be simulated by means of a waveform (from a signal generator) having approximately the same sweep time as the transient.

An oscilloscope with the *AUTO STORE* function (see Figure 12-10) stores a received transient and then switches on a light-emitting diode (LED) to indicate that the transient is stored. The waveform may then be displayed and studied. The *AUTO ERASE* function is used when a series of high-speed signals are to be scanned. The persistence is automatically adjusted so that one signal fades out before the next one appears.

12-3 SAMPLING OSCILLOSCOPES

Most ordinary oscilloscopes have an upper frequency limit in the range of 20 MHz to 50 MHz. Higher input frequencies cause the electron beam to move so fast across the screen that only a very faint trace is produced. The *sampling oscilloscope* (*sampling scope*) overcomes this difficulty by producing a low-frequency dot representation of the signal. Each dot represents an amplitude sample of the input signal, and each sample is taken in a different cycle. The sampling circuits must be capable of operating at very

high frequencies, but the CRT and its associated circuitry may be relatively low-frequency equipment.

Figure 12-11 shows 10 cycles of a high-frequency waveform that is to be displayed. One amplitude sample is taken at successively later times in each cycle. The resultant series of samples reproduces the original waveform at a lower frequency. Suppose the input signal has a time period of $T = 0.01\ \mu s$. Its frequency is $f_1 = 1/0.01\ \mu s = 100$ MHz. The dot display has a time period of $10 \times 0.01\ \mu s$ or a frequency of $f_2 = 100\ \text{MHz}/10 = 10$ MHz. Thus, a 100-MHz signal is converted into a 10-MHz waveform for display. If one cycle of dot display is created by sampling 100 cycles of signal, the frequency of the displayed wave is 1/100 of the signal frequency. One disadvantage of this system is that only purely repetitive signal waveforms can be investigated. If the waveform changes over several cycles, the dot display will be in error. A transient waveform cannot be investigated by means of this type of sampling scope.

A basic block diagram and waveforms for a sampling scope are shown in Figure 12-12. Instead of the ramp generator employed in a regular oscilloscope, a *staircase generator* is used for horizontally deflecting the electron beam in the CRT. As the waveform shows, the output of the

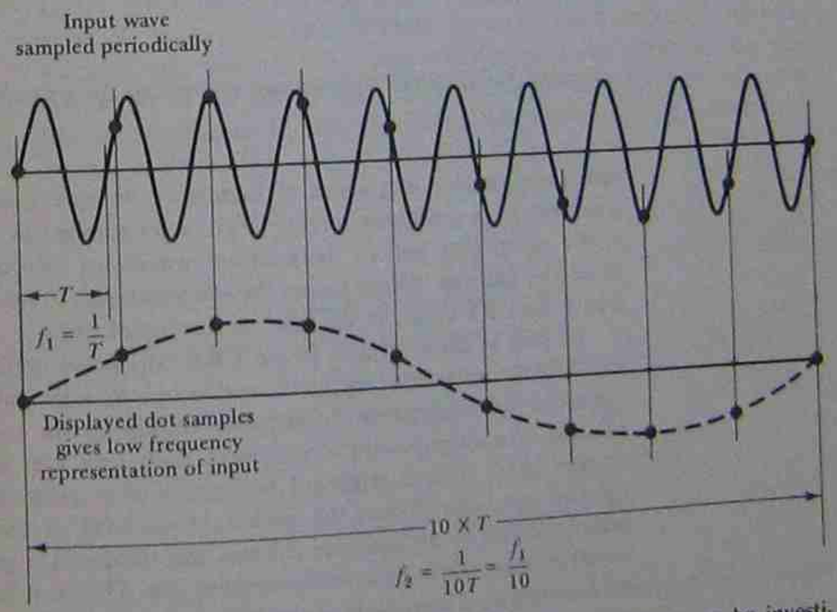


FIGURE 12-11. A very high frequency repetitive waveform can be investigated by sampling successive cycles to create a low frequency dot display on an oscilloscope.

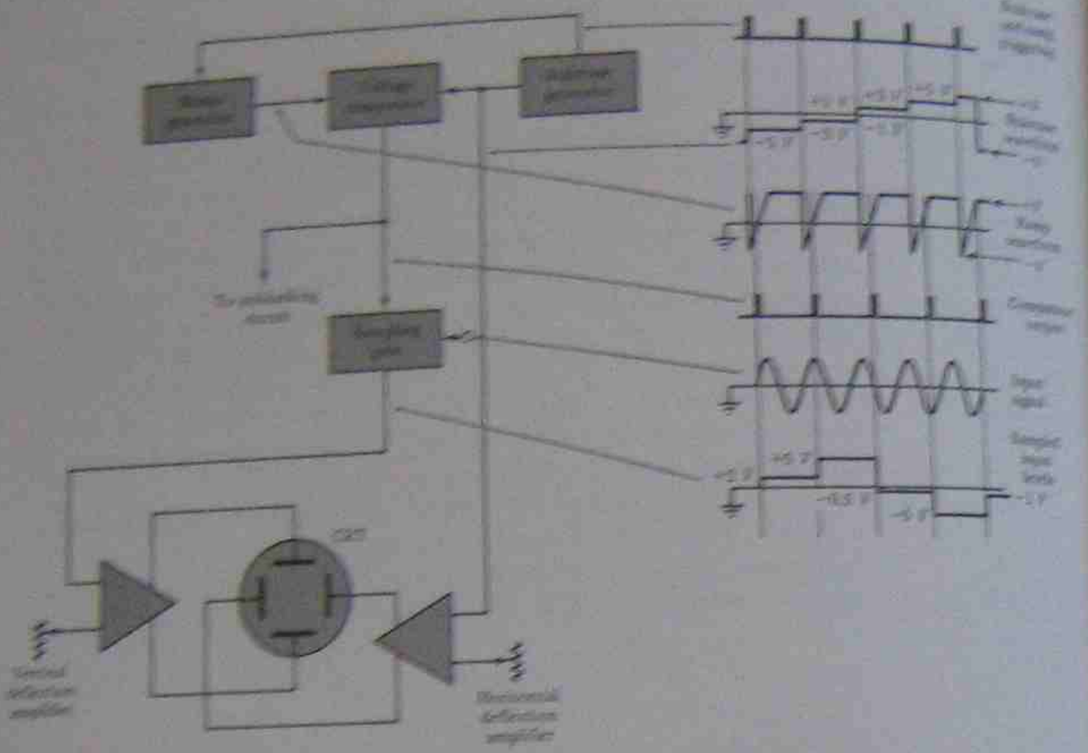


FIGURE 12-12. Block diagram and waveforms for a sampling oscilloscope.

staircase generator is a series of increasing voltage steps (or staircase), which rise from a negative level (−V) to a positive level (+V). At the end of the sweep time period, the staircase waveform returns to its starting level. The staircase voltage causes the electron beam to be moved from one side of the CRT screen to the other in a series of steps.

As well as being applied to the CRT horizontal deflection amplifier, the staircase generator output is connected to one input of a *voltage comparator*. This compares the staircase voltage to the output of a *ramp generator*. The ramp output commences each time the staircase voltage changes level. This is triggered by means of a pulse signal from the staircase generator. When the instantaneous level of the ramp voltage becomes equal to the staircase voltage, the comparator produces a short duration pulse, which turns on the *sampling gate*. The sampling gate samples the instantaneous amplitude of the high-frequency input waveform. After switching on for only a brief instant, the sampling gate holds its output

level constant until the next sample is taken. The pulse output from the comparator is also applied as an *unblanking pulse* to the CRT grid. This turns on the electron beam for a short time to create a dot on the screen.

The waveforms in Figure 12-12 illustrate the process of creating the dot display. The input wave is sampled, as already explained, to create a low-frequency step representation of the original. This step wave is applied to the CRT vertical deflection amplifier, while the staircase wave from the staircase generator is applied to the horizontal deflection amplifier. No waveform display occurs while the CRT grid is biased negatively. Each time an unblanking pulse occurs, a bright dot is created on the screen. The position of each dot depends upon the voltages that appear at the horizontal and vertical deflection plates and upon the deflection sensitivity of the CRT.

Consider the deflecting voltages when the first (left-hand) unblanking pulse (from the comparator) occurs in Figure 12-12. The vertical deflecting voltage (sampled level) is +2 V, and the horizontal deflecting voltage (staircase wave) is −3 V. Assume that the vertical deflection sensitivity is 0.5 cm/V and the horizontal deflection sensitivity is 1 cm/V. The electron beam is deflected vertically up from the center line on the screen by: 2 V × 0.5 cm/V = 1 cm. The beam is also deflected horizontally to the left of center by: 3 V × 1 cm/V = 3 cm. This gives point 1 in Figure 12-13. When the unblanking pulse occurs, a bright dot is created at this point. At the next unblanking pulse, the vertical and horizontal deflecting voltages have become +3 V and −1 V respectively. Therefore, the next dot occurs at 2.5 cm up from the screen center and 1 cm left of center (point 2 in Figure 12-13). Continuing this process, the dot waveform is created as illustrated.

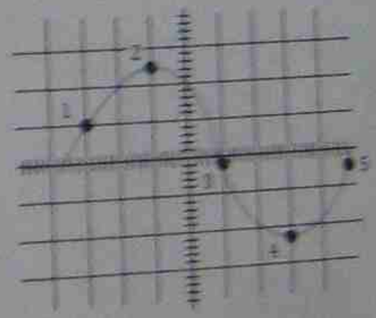


FIGURE 12-13. Dot display derived from staircase waveform and sampled input levels in Figure 12-12.

Figures 12-14, 12-15, and 12-16 respectively show the basic circuits of a staircase generator, a voltage comparator, and a sampling gate. The staircase generator circuit is similar to the sweep generator in Figure 11-7, except that the constant current transistor (Q_1) is controlled by a pulse generator. Each negative-going pulse from the pulse generator turns Q_1 *on* for a brief time period. Each time Q_1 is switched *on*, it provides a current pulse to capacitor C_1. Every current pulse charges C_1 to a new voltage level, which remains constant until the next current pulse arrives. When the capacitor voltage exceeds the intended upper level, the Schmitt trigger circuit is activated to turn Q_2 *on* and discharge C_1 to its starting level (as in the linear sweep generator circuit of Figure 11-7).

In the voltage comparator in Figure 12-15, transistors Q_1 and Q_2 constitute a *differential amplifier* (see Section 8-5-1). Another amplifier stage takes the collector output voltages from Q_1 and Q_2 and amplifies their difference up to the supply voltage saturation levels. With the instantaneous level of the ramp input to Q_1 lower than the staircase voltage, Q_1 is biased *off* and Q_2 is *on*. The collector voltage of Q_1 is high (close to $+V_{CC}$), and the collector of Q_2 is low. With the amplifier input polarity illustrated, the output voltage is low at this time. When Q_1 input becomes equal to the input level of Q_2, its collector voltage falls while the collector of Q_2 rises. This produces a positive-going output from the amplifier stage. Therefore,

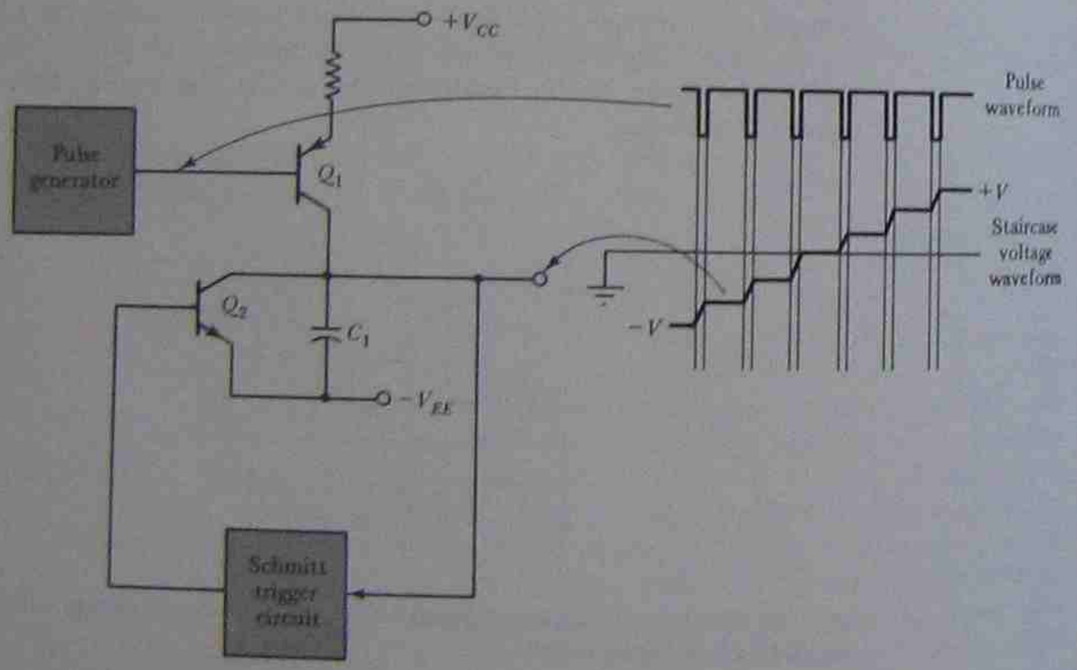


FIGURE 12-14. Basic circuit and waveforms for a staircase generator.

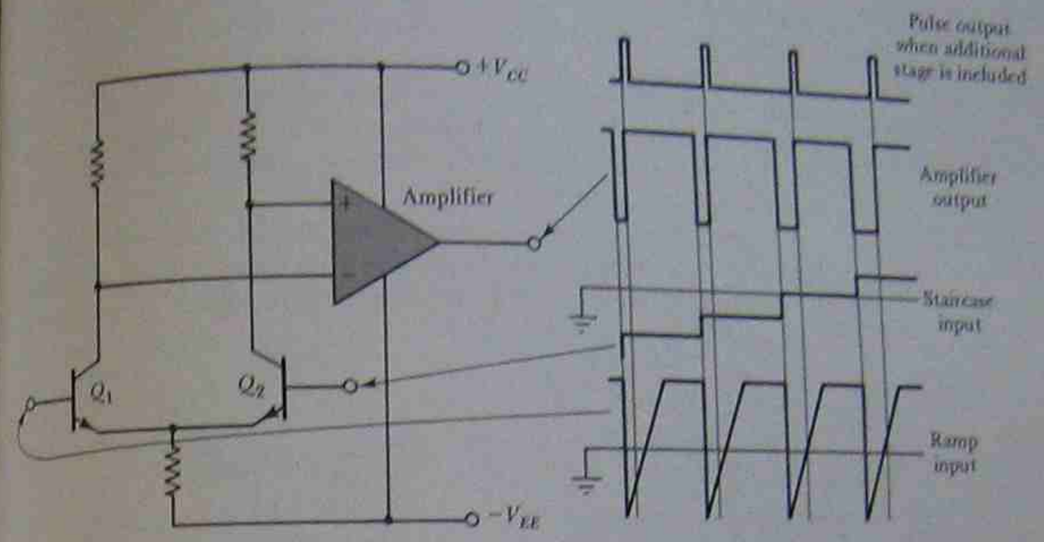


FIGURE 12-15. Voltage comparator circuit and waveforms.

the comparator output is normally low while the ramp voltage is below the staircase level, and it rapidly switches to a high level when the two inputs become equal. A further stage can be added to the circuit in Figure 12-15 to give a spike or short pulse output at the instant that the inputs reach equality.

The sampling gate in Figure 12-16 consists of FET Q_1 and capacitor C_1. A voltage follower (see Section 8-6-2) is included to provide a low-

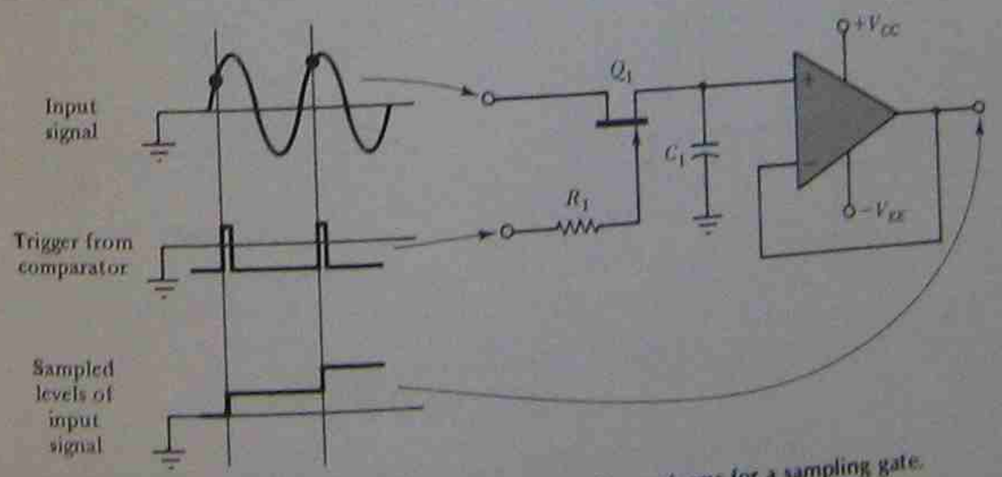
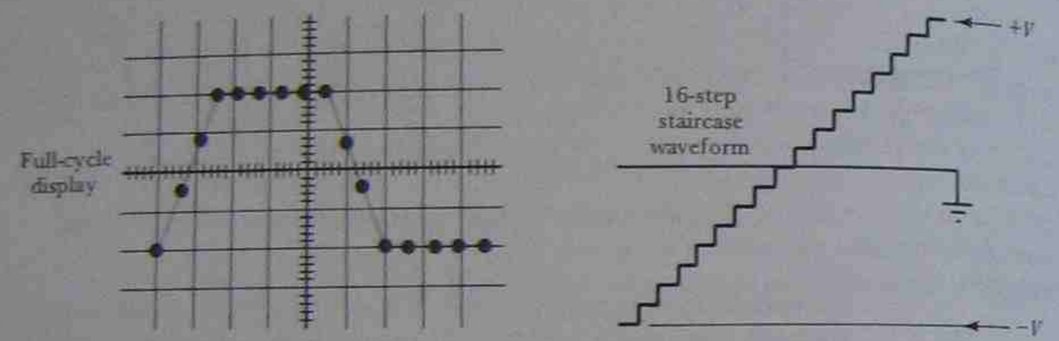


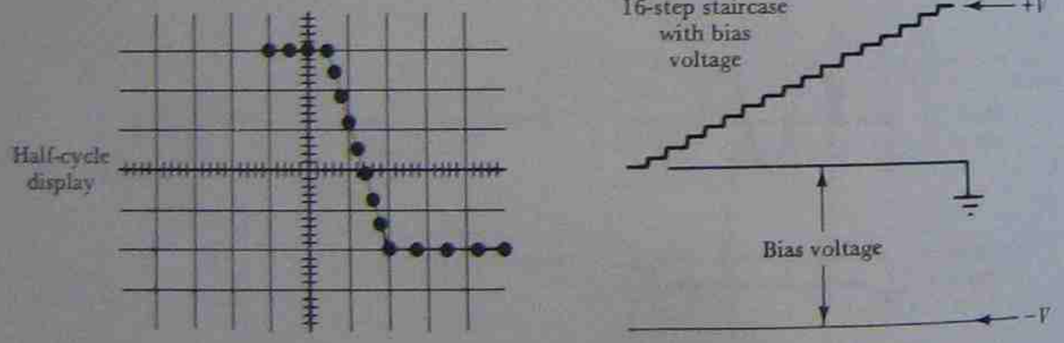
FIGURE 12-16. Circuit and waveforms for a sampling gate.

output impedance. With the input to the gate of Q_1 normally biased negatively, Q_1 is *off*. In this condition, it is like an open switch. When a positive pulse occurs at the gate, Q_1 switches *on* into saturation. The voltage drop from the drain to source terminals of the FET is extremely small when the device is biased *on*, so in the *on* condition it is like a closed switch. Capacitor C_1 is charged to the level of the input voltage each time the FET is biased *on*. When the FET goes *off*, C_1 retains its voltage constant at the level of the last sample.

When a sampling scope is operated in *expanded mode*, the results are similar to those obtained with the delayed time base discussed in Section 12-1. Figure 12-17(a) shows a dot representation of an approximately



(a) A complete cycle of input signal is sampled and displayed using a normal staircase waveform.



(b) Combining a bias voltage with a more dense staircase allows a portion of the input signal to be sampled and displayed.

FIGURE 12-17. A sampling scope can be operated in *expanded mode* to investigate any portion of the cycle of an input signal.

square wave input signal. Since there are 16 (amplitude sample) dots shown, the signal was sampled 16 times. To do this, the staircase time base had to have 16 steps, as illustrated. Now, suppose the time base is adjusted to consist of 16 smaller steps and that this is superimposed upon a dc bias voltage, as illustrated in Figure 12-17(b). This causes all 16 amplitude samples to be taken during the latter half-cycle of the input signal. Thus, only this half of the signal is displayed on the oscilloscope screen. However, this portion is displayed in much greater detail than before when the horizontal deflection sensitivity of the oscilloscope is expanded to give a full-screen display of the sampled portion of the input waveform.

By adjusting the bias voltage and the density of the staircase waveform, any portion (including very small portions) of the input signal can be investigated. The section of the waveform to be investigated is usually identified by moving a very bright dot to the desired part of the signal when it is displayed in the normal (full-cycle) mode. This, again, is similar to the method used with a delayed time base oscilloscope.

12-4 DIGITAL STORAGE OSCILLOSCOPE

Unlike analog storage scopes, which store the input waveform in the CRT, *digital storage oscilloscopes* digitize the waveform and store it in a memory. The input signal is first sampled, and then each analog sample is converted into a digital sample by means of an *analog-to-digital converter* (ADC). The digitized samples are stored in a memory and converted back to analog form for display purposes using a *digital-to-analog converter* (DAC). The recreated samples are employed in conjunction with a staircase waveform time base to create a dot display on the oscilloscope screen in the same way as in a sampling scope (see Section 12-3).

12-4-1 Operation of the Digital Oscilloscope

A basic sampling and storage system used in a digital scope is illustrated in Figure 12-18. The *time base* generates a pulse waveform at the desired sampling frequency. Each pulse turns the *sampling gate on* (see Section 12-3) for a brief time period. In this way, a series of amplitude samples is generated, as illustrated. Each sample is converted by the ADC into a short train of pulses. The number of pulses in each case is directly proportional to the sampled amplitude. The groups of pulses are counted into a semiconductor (or other type) memory, where they are stored for later recovery.

Figure 12-19 shows a system for recovering the stored information from memory to recreate a dot representation of the original signal. The digital samples from the memory are converted to analog form to create a step representation of the signal. The time base generates a staircase voltage waveform and controls the DAC so that each analog sample is reproduced at the appropriate point during the time base. The analog samples are applied to the input of the vertical deflection amplifier of the oscilloscope, while the staircase wave time base is fed to the horizontal

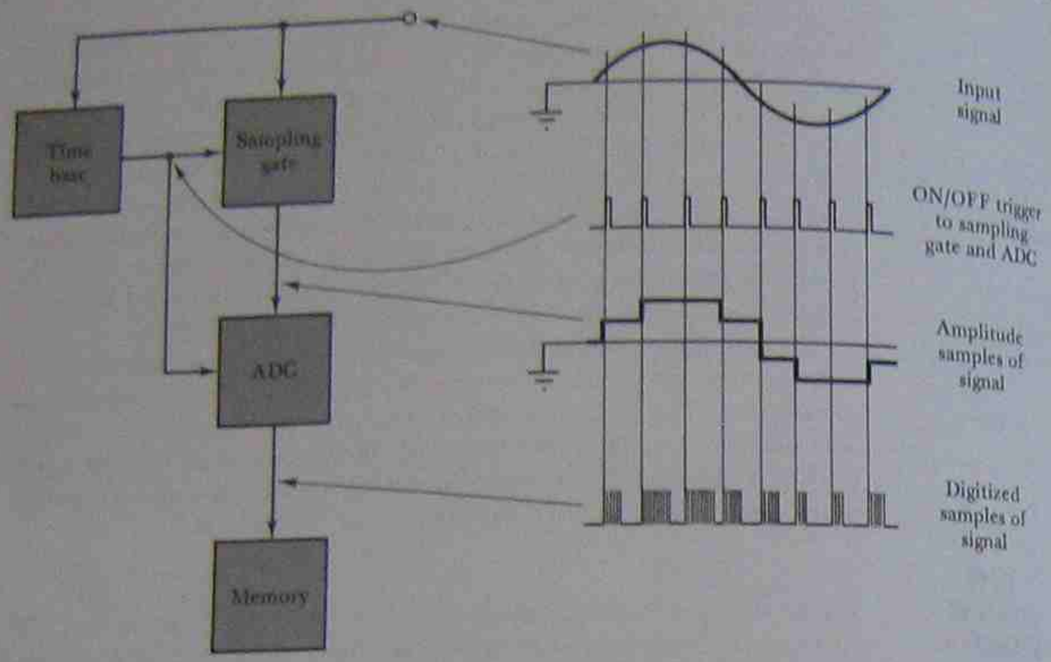


FIGURE 12-18. Basic sampling and storing system for a digital oscilloscope.

deflection amplifier. The combination of these two inputs together with unblanking pulses produces a dot waveform on the CRT screen, representing the original input signal. The dot display is created exactly as explained for the sampling scope in Section 12-3.

12-4-2 Analog-to-Digital Conversion and Storage

A detailed system of digitizing amplitude samples and storing them in flip-flop memories is illustrated in Figure 12-20. The ADC consists of: a *voltage comparator*, a *ramp generator*, a *clock generator*, and an *AND* gate. The ramp generator is triggered by a pulse train from the time base. This pulse train is synchronized with the amplitude samples, as illustrated. The amplitude sample waveform is applied to one input of the voltage comparator (see Section 12-3), while the ramp generator output is applied to the other input terminal. The comparator output voltage is high while the instantaneous level of the ramp is below the voltage of the amplitude sample. When the ramp voltage becomes equal to the sample, the comparator output rapidly falls to a low level. The resultant output from the comparator is a pulse that has a *width* (or *pulse duration*) directly proportional to the amplitude sample. The comparator output waveform in Figure 12-20 has a wide pulse when the amplitude samples are high and progressively narrower pulses for lower-level amplitude samples.

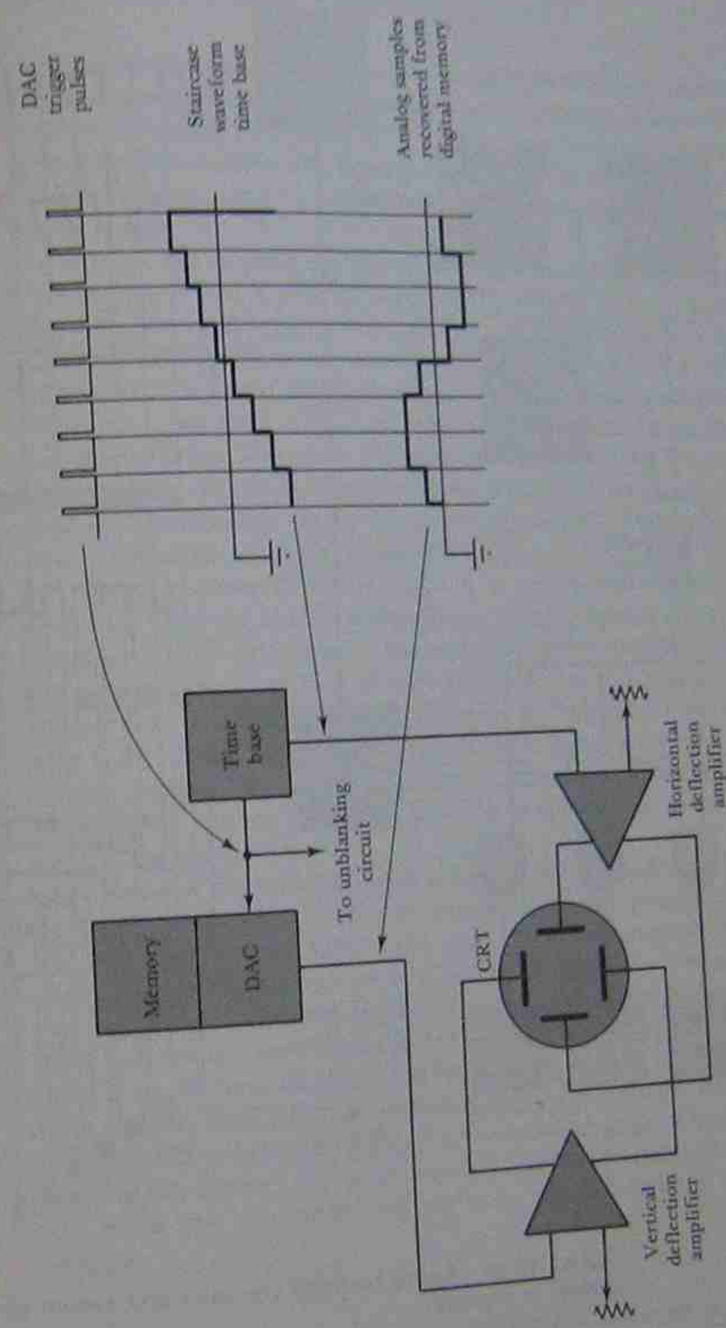


FIGURE 12-19. System for converting digital representation of samples from memory into analog voltage levels for display purposes.

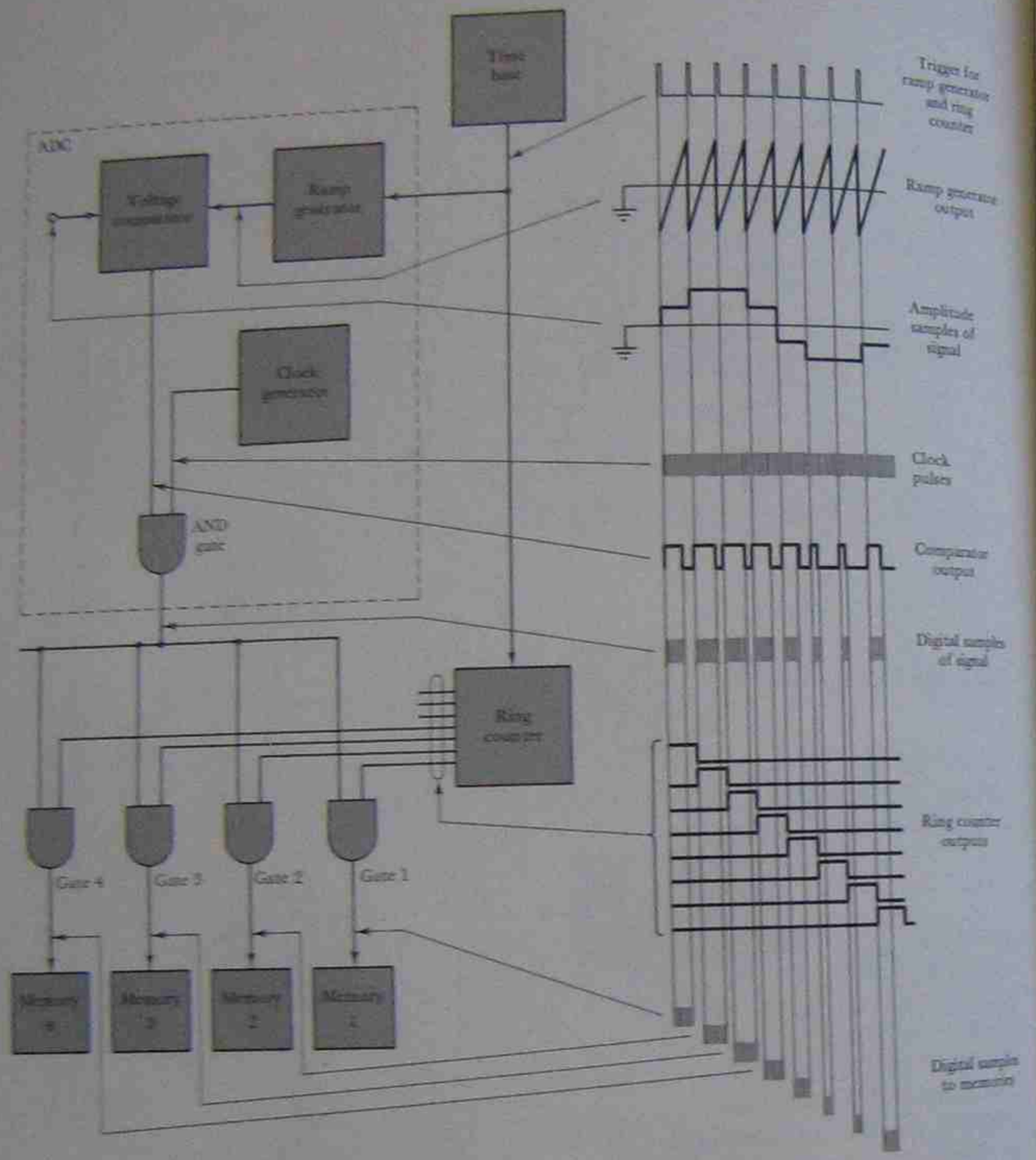


FIGURE 12-20. Analog-to-digital converter and system of storing digitized samples in memory.

The clock generator is an accurate, crystal-controlled pulse generator. The comparator output and the clock output are applied as inputs to an *AND* gate. Outputs occur from the *AND* gate only when both inputs are present (see the waveforms in Figure 12-20). Thus, the *AND* gate output is a train of clock pulses that is present for the duration of each comparator output pulse.

Suppose one amplitude sample of the original input signal is exactly 1 V. Also assume that a 1-ms output pulse is produced by the comparator when the 1-V input level is present. If the clock generator frequency is 1 MHz, then 1000 clock pulses pass through the *AND* gate during the 1-ms time period. Therefore, 1000 pulses represent the 1-V signal sample level. When the signal level is 0.842 V, the pulse width from the comparator becomes 0.842 ms. This allows 842 pulses of the 1-MHz clock frequency to pass through the *AND* gate. Similarly, a 1.375-V amplitude sample produces a comparator output pulse width of 1.375 ms, and consequently, 1375 clock pulses are passed by the *AND* gate.

The *ring counter* in Figure 12-20 is a circuit with several output terminals. Only one of these terminals has a high output at any time (see the ring counter waveforms in Figure 12-20). Pulses from the time base (occurring at the beginning of each amplitude sample) trigger the ring counter from one state to another. The gates in Figure 12-20, identified as gate 1, gate 2, etc., are all *AND* gates leading to memory circuits. The ring counter outputs are connected as inputs to each of these gates. As illustrated, the output of the ADC *AND* gate is applied as a common input to all of the memory gates.

When the ring counter output is high at gate 1, all of the other gates have low-level inputs from the ring counter. Thus, only gate 1 can pass the output pulses from the ADC at this time. The pulses representing the first digitized amplitude sample are now counted into memory 1 via gate 1. At the beginning of the next amplitude sample, the trigger pulse from the time base changes the state of the ring counter to give a high input level to gate 2. At this time, all other gates have low input levels applied from the ring counter. Now, only gate 2 passes output pulses from the ADC. So the group of pulses representing the second amplitude sample of the signal are counted into memory 2. It is seen that any number of amplitude samples of the signal can be digitized and routed to separate memory circuits for storage.

12-4-3 Digital Memory

One type of memory for storing digital samples is simply a cascade of transistor flip-flops, as illustrated in Figures 9-9 and 9-10 and explained in Section 9-4. The truth table in Figure 9-10 shows that a cascade of four flip-flops can count up to 16. Also, the state of the flip-flop outputs can be read as a binary number representing the number of pulses counted into

the circuit. By extending the truth table in Figure 9-10, it can be demonstrated that five flip-flops can count to 32 and six can count to 64. To count to 1000 (or store numbers up to 1000) in binary form, 10 flip-flops are required. (Ten flip-flops can actually count to 1024.) A cascade of 11 flip-flops can count (and store) to over 2000.

If a maximum of 100 pulses is employed to represent the signal sample levels, the presence or absence of one pulse represents a resolution of 1 in 100, or 1%. Where 1000 pulses are used to represent the signal amplitude, the *resolution* is 0.1%. As explained in Section 4-3, resolution is related to measurement precision. Resolution does not represent accuracy of measurement, but accuracy can never be better than resolution. Each of the memory blocks in Figure 12-20 consists of cascaded flip-flops, the number of flip-flops depending upon the required resolution for the signal samples.

12-4-4 Digital-to-Analog Conversion

It has been explained that a signal may be sampled and that the digitized samples can be stored in binary form in flip-flop memories. Now consider how the digital samples can be converted back to analog voltage levels to create a display on the screen of the oscilloscope. The DAC circuit shown in Figure 12-21(a) uses an IC op-amp *inverting amplifier* and *weighted resistors*. The term *weighted resistors* simply means that the resistors connected to the flip-flop memory are chosen according to the digital value represented by each flip-flop. With the noninverting input terminal of the op-amp grounded, the inverting input terminal is always close to ground level (see Section 8-6). Thus, when flip-flop 4 produces an output to resistor R_4, the other end of R_4 remains at ground level, and all of the output voltage from flip-flop 4 (ff4) appears across resistor R_4. Also, recall from Section 8-6 that the current flowing into the op-amp input terminals is virtually zero. So all of current I flows through the feedback resistor R_f. Because one end of R_f is at the (ground level) inverting input terminal and the other end is connected to the op-amp output terminal, the output voltage is:

$$V_o = IR_f$$

Assume that the output voltage from each flip-flop in Figure 12-21(a) is either zero or 1 V. If ff4 has a high output and all others have zero output voltage, the stored binary number is 1000. This is equivalent to decimal 8, as illustrated in Figure 12-21(b). Current I is calculated as:

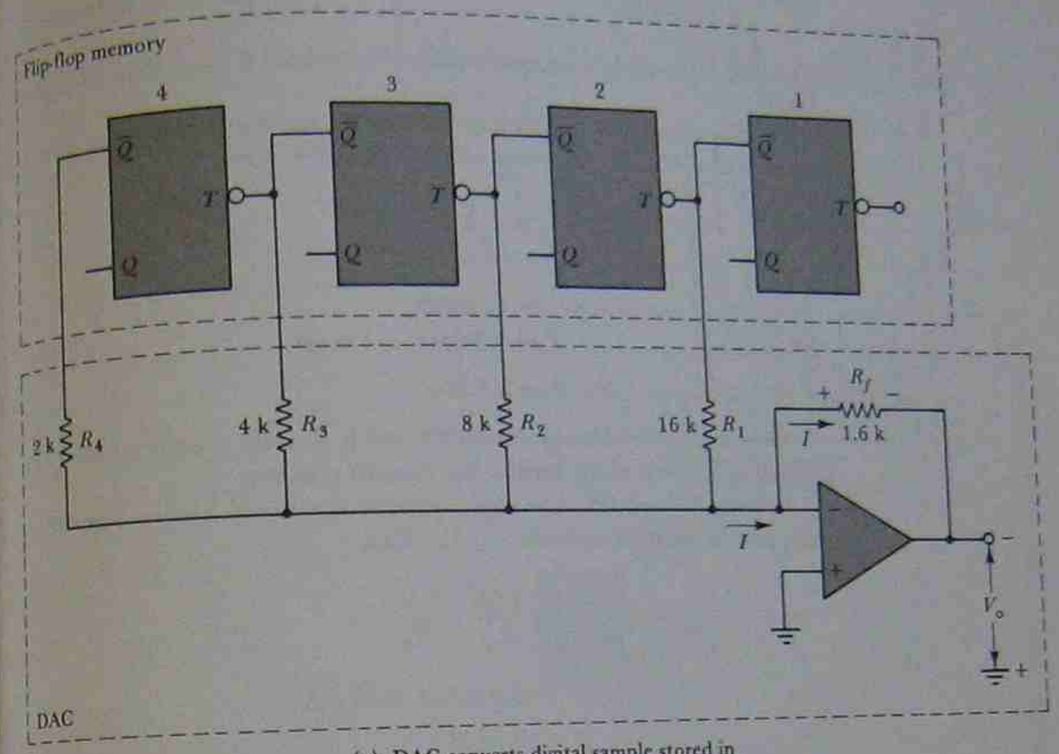
$$I = \frac{1\text{ V}}{R_4} = \frac{1\text{ V}}{2\text{ k}\Omega}$$

$$= 0.5\text{ mA}$$

and,

$$V_o = IR_f = 0.5\text{ mA} \times 1.6\text{ k}\Omega$$

$$= 0.8\text{ V}$$



(a) DAC converts digital sample stored in flip-flop memory into analog voltage level.

Binary number stored in memory	Decimal equivalent
1 0 0 0	8
0 1 0 0	4
0 0 1 0	2
0 0 0 1	1

(b) Binary (digital) numbers and decimal (analog) equivalents

FIGURE 12-21. Digital-to-analog conversion system, and digital and analog equivalent numbers.

This (0.8 V) is directly proportional to the decimal 8 equivalent of binary 1000.

When only ff3 has a high output level, the memory has a stored binary number of 0100, which corresponds to decimal 4. Now:

$$I = \frac{1\text{ V}}{R_3} = \frac{1\text{ V}}{4\text{ k}\Omega}$$

$$= 0.25\text{ mA}$$

and,

$$V_o = 0.25\text{ mA} \times 1.6\text{ k}\Omega$$

$$= 0.4\text{ V}$$

Once again, the analog output voltage is directly proportional to the decimal equivalent of the binary (i.e. digital) number.

If both ff3 and ff4 have high outputs, the stored binary number is 1100, and its decimal equivalent is 12. Also:

$$I = \frac{1\text{ V}}{R_4} + \frac{1\text{ V}}{R_3}$$

$$= 0.5\text{ mA} + 0.25\text{ mA}$$

$$= 0.75\text{ mA}$$

Now,

$$V_o = 0.75\text{ mA} \times 1.6\text{ k}\Omega$$

$$= 1.2\text{ V}$$

It is seen that the DAC output voltage is always directly proportional to the analog equivalent of the digital number stored in memory.

12-4-5 Recovery from Memory

Now refer to Figure 12-22, which shows three channels of a multichannel system for recreating all of the analog amplitude samples from the stored digital information. A time base circuit once again generates a staircase waveform for horizontally deflecting the electron beam in the CRT. The time base also produces a train of pulses to trigger a ring counter at the commencement of each step in the staircase voltage. The ring counter controls the gates to ensure that only one gate produces an output during each step of the staircase time base. These gates are sampling gates (not logic gates), and each one samples the DAC output from the individual memories.

During the first (i.e., lowest) step of the staircase time base voltage, the ring counter holds gate 1 *on* and all other gates *off*. The analog voltage representing the first signal sample is passed via gate 1 to the common output terminal. When the next time base step occurs, only gate 2 is *on*, and the analog output voltage now represents the second sample of the input signal. Other sample levels are recovered in the correct order as the

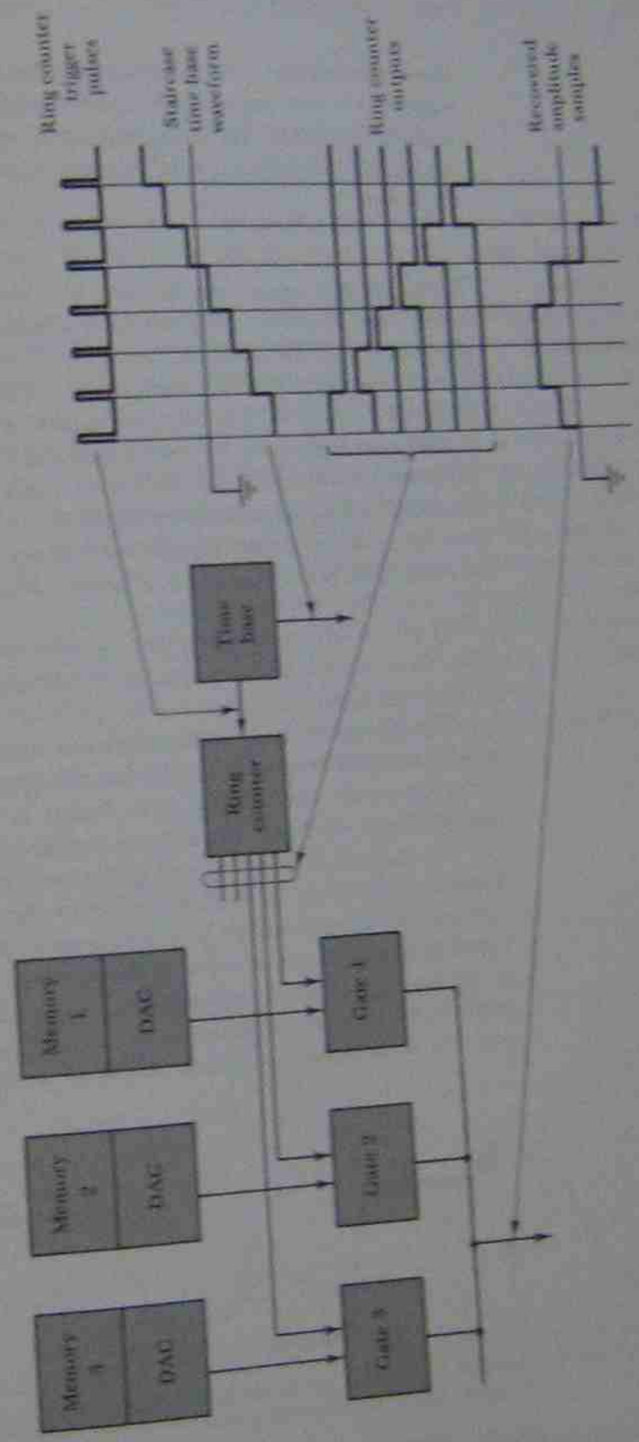


FIGURE 12-22. System for recovering analog samples from digital memory.

gates are switched on in sequence. The recreated (step form) signal waveform is now applied to produce vertical deflection, and the time base is used to produce horizontal deflection at the oscilloscope screen. With appropriate unblanking, a dot representation of the original input signal is displayed.

12-4-6 Digital Oscilloscope Performance

Digital storage scopes can be used to display sine, pulse, and transient waveforms. As with analog sampling scopes, the quality of the displayed waveform depends upon the number of dots (i.e., samples) per cycle. Where a high dot density is used, the waveform is displayed in great detail [Figure 12-23(a)]. With fewer samples during each cycle, important details of the waveform may be lost [Figure 12-23(b)]. The type of detailed waveform shown in Figure 12-23(a) is easily obtained when a relatively low-frequency signal is being investigated. For example, suppose a 500-kHz sine wave is to be displayed on an oscilloscope that can sample at a rate of 50 MHz. The number of samples taken during one cycle is:

$$\frac{\text{sampling rate}}{\text{signal frequency}} = \frac{50\text{ MHz}}{500\text{ kHz}} = 100$$

Therefore, one cycle of the displayed signal is made up of 100 dots. When the signal frequency is 10 MHz, only five dots are displayed in each cycle. Obviously, the 100 dot/cycle display is very satisfactory, while the five dot/cycle waveform does not give a clear picture of the signal.

The maximum sampling rate of the oscilloscope determines the maximum frequency that can be satisfactorily displayed. Sampling theory states that samples must be taken at a rate greater than two times the highest signal frequency to reproduce a repetitive signal. (This rule does not apply to the sampling method used with analog sampling scopes.) In practice, a good display requires a minimum of about 25 samples per cycle. Therefore, the *useful storage bandwidth* (USB) of a digital oscilloscope can be



(a) High dot (sample) density gives good quality waveform display.



(b) With low dot density, important details of a waveform may be lost.

FIGURE 12-23. With dot displays, many samples are required in each cycle for a complete (detailed) trace of the signal.

calculated as:

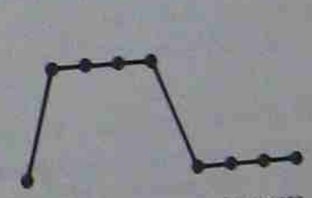
$$\text{USB} = \frac{\text{maximum sampling rate}}{25}$$

This is the upper limit of the signal frequency that can be investigated by the scope. However, as will be explained, the upper limit can be extended.

In order to obtain a more recognizable display, digital scopes normally have a facility for drawing lines between the dots in the display. This is referred to as *interpolation*. Interpolators that draw straight lines from dot to dot are termed *linear* or *pulse interpolators*. These are most suitable for pulse waveform displays. *Sine wave interpolators* introduce a sinusoidal function between the dots. Figure 12-24 illustrates the application of both types. The linear interpolator can give good results with sine waves if sufficient samples are available during each cycle. With fewer samples, straight lines between the dots give a distorted display. A sine wave interpolator can introduce distortions such as overshoots when used with pulse waveforms.

When a linear interpolator is available, the USB of the oscilloscope is increased because a good sinusoidal display is obtained with 10 samples per cycle. Therefore, USB = (maximum sampling rate)/10.

With a sine interpolator, only 2.5 samples per cycle are required for a satisfactory display. So, USB = (maximum sampling rate)/2.5.



(a) Linear or pulse interpolators are suitable for use with pulse waveforms.



(b) Linear interpolators are satisfactory for sine wave signals when there are 10 or more samples per cycle.



(c) Sine interpolators can give a good display with only 2.5 samples per cycle

FIGURE 12-24. The use of interpolators to draw lines between dots makes a big improvement in dot waveform displays.

One of the most important quantities involved in the investigation of pulse waveforms is rise time (t_r) (see Figure 11-20). For a satisfactory display of the edge of the pulse, approximately 10 samples should be taken during t_r. Since the time period of the sampling rate is 1/(sampling rate), the minimum rise time that can be investigated is:

$$t_{r(\min)} = 10/(\text{sampling rate})$$

For a sampling rate of 50 MHz,

$$t_{r(\min)} = 10/(50\ \text{MHz}) = 200\ \text{ns}$$

Pulse waveforms with shorter rise times than this can be investigated, but the edge of the pulse cannot be studied in detail.

Consider Figure 12-25, which shows a pulse display with insufficient detail for investigation of t_r. Measuring from 10% to 90% of pulse amplitude, the maximum possible rise time of the signal is:

$$t_{r(\max)} = 0.8 \times 2(\text{sampling interval})$$

or,

$$t_{(\max)} = 1.6(\text{sampling interval})$$
$$= 1.6/(\text{sampling rate})$$

This defines the useful rise time (Ut_r) of the oscilloscope as:

$$Ut_r = 1.6/(\text{sampling rate})$$

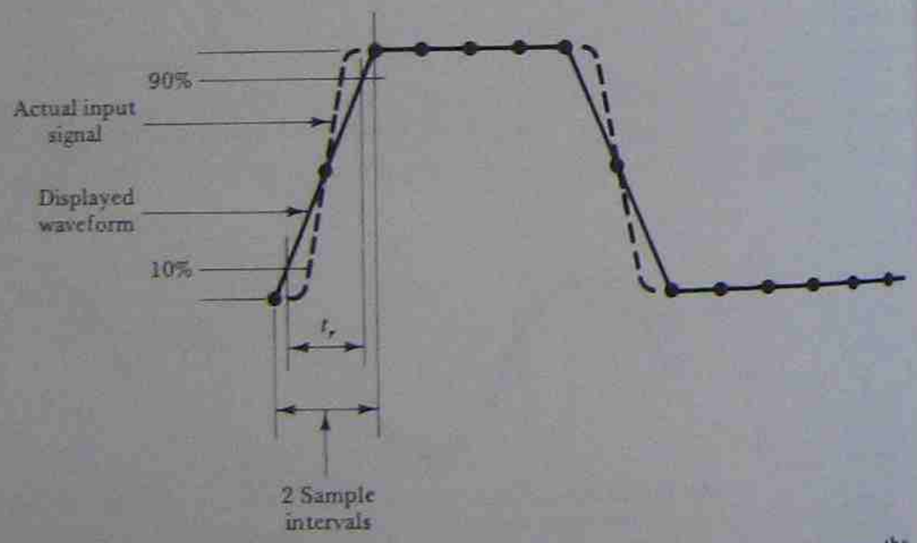


FIGURE 12-25. For a pulse waveform displayed on a digital oscilloscope, the maximum possible rise time of the input signal is measured between the 10% and 90% amplitude levels.

For a sampling rate of 50 MHz,

$$Ut_r = 1.6/(50\ \text{MHz}) = 32\ \text{ns}$$

It is important to note that this equation cannot be applied to calculate the actual rise time of the displayed pulse. However, like USB, Ut_r is a measure of the upper limits of the performance of a digital oscilloscope.

One clear advantage of the digital scope over the analog storage scope is that waveforms can be stored permanently in a digital instrument. The stored information does not fade away with time. When compared to the analog sampling scope, the digital scope has an advantage in its ability to store and display transients as well as repetitive waveforms. Analog sampling scopes can display only repetitive waves, not transients. A disadvantage of most digital instruments is that they cannot be used at signal frequencies as high as those at which analog sampling instruments can operate.

Additional features available with some digital oscilloscopes are:

1. *Pre-trigger Viewing.* The instrument can be set in a *baby-sitting* mode so that it is continuously storing all inputs rather than waiting to be triggered by an event. This gives a view of the complete waveform of the event (or transient), which might otherwise be only partially recorded.
2. *Signal Processing.* Some digital oscilloscopes have internal circuitry to determine average value, rms value, frequency, etc., of the stored waveform. These quantities are then displayed in print form on the oscilloscope screen.
3. *Roll Mode.* This involves continuous scanning of the stored waveforms, with the display moving from right to left on the screen. It is similar to watching a waveform being traced on a strip chart recorder (see Chapter 13). The total memory is capable of giving a playback of many hours of stored information.

REVIEW QUESTIONS AND PROBLEMS

12-1. Discuss the need for a time delay system in an oscilloscope, and explain how it can improve waveform investigations.

12-2. Sketch the waveforms generated by a main time base and a delayed time base. Explain how the MTB and DTB combine to intensify a section of the waveform displayed on the oscilloscope.

12-3. Sketch the block diagram of a delayed time base system. Explain the operation of the system in relation to the waveforms drawn for Question 12-2.

12-4. List the major controls of a delayed time base system. Discuss the use of these in conjunction with the main time base controls.

12-5. Discuss the use of a delayed time base for measurement of: time period, rise time, pulse jitter. Illustrate your discussion with appropriate sketches.

12-6. Sketch the construction of a bistable type storage CRT. Explain its operation.

12-7. Sketch the construction of a variable persistence type storage CRT. Explain its operation.

12-8. List the major controls of a storage oscilloscope, and discuss the use of each control.

12-9. Show by sketches how a high-frequency waveform may be sampled to create a low-frequency dot representation of the high-frequency wave. Explain the relationship between the frequency of the signal, the frequency of the dot waveform, and the number of samples per cycle of dot waveform.

12-10. Sketch the system block diagram and waveforms for a sampling oscilloscope. Briefly explain the system operation.

12-11. Explain how a staircase time base waveform combines with a ramp representation of a sampled signal and unblanking pulses to create a dot representation of a sampled signal.

12-12. The two waveforms illustrated in Figure 12-26 are applied to a oscilloscope with a deflection sensitivity of 1 cm/V. Sketch the resultant waveform that will be displayed on the oscilloscope screen.

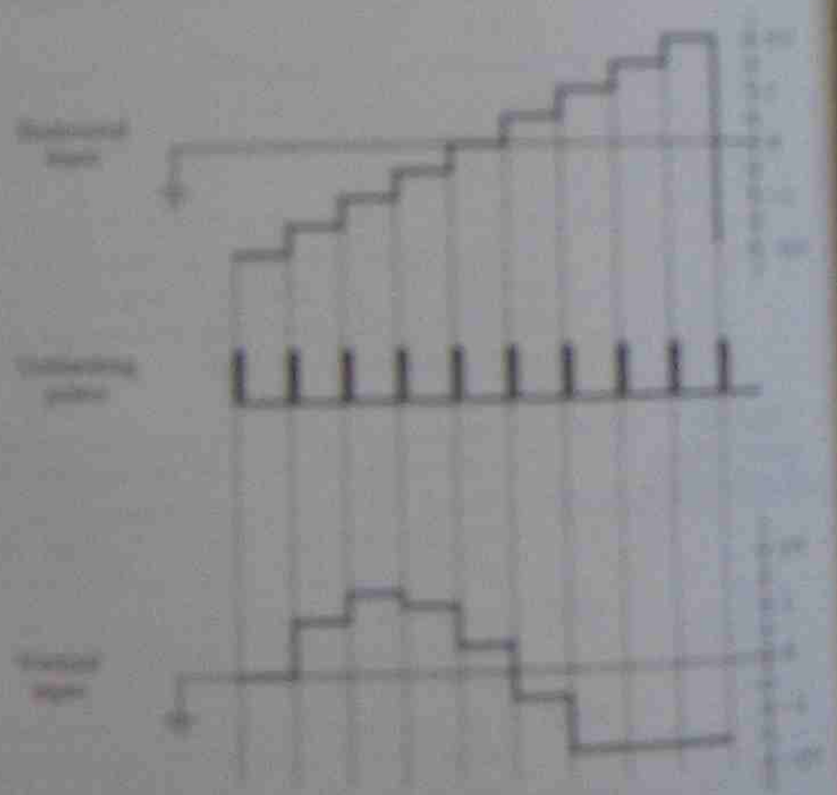


FIGURE 12-26. Waveforms for Question 12-12.

12-13. Sketch the basic circuit of a staircase generator and the circuit waveforms. Briefly explain the circuit operation.

12-14. Sketch the basic circuit of a voltage comparator and the circuit waveforms. Briefly explain the circuit operation.

12-15. Sketch the circuit and waveforms of a sampling gate. Briefly explain.

12-16. Discuss expanded mode operation of a sampling oscilloscope.

12-17. Sketch the basic block diagram and associated waveforms for the sampling and storing system in a digital oscilloscope. Briefly explain the system operation.

12-18. Sketch the basic system block diagram and associated waveforms for converting samples from the memory of a digital oscilloscope into analog levels for display purposes. Briefly explain.

12-19. Sketch the block diagram of an analog-to-digital converter and storage system for a digital oscilloscope. Show the waveforms throughout the system, and carefully explain the system operation.

12-20. Explain how a cascade of flip-flops may be employed as a digital memory. What is the maximum sampling resolution possible when seven cascaded flip-flops are employed to store each sample?

12-21. Sketch the circuit of a digital-to-analog converter using weighted resistors. Show the relationship of the resistor values to each stage of the flip-flop memory, and explain the operation of the circuit.

12-22. For the DAC in Figure 12-21, calculate the output voltage level when the stored binary number is (a) 1111, (b) 1011. Assume that the flip-flop outputs are a high of +5 V and a low of 0 V.

12-23. Sketch the block diagram and waveforms of a system for recovering analog samples from a digital memory. Explain the operation of the system.

12-24. Explain linear or pulse interpolation as used in a digital oscilloscope. Explain useful storage bandwidth (USB), and discuss the USB of a digital oscilloscope (a) without any interpolation, (b) with a linear interpolator, (c) with a sine wave interpolator.

12-25. Discuss the application of a digital oscilloscope to investigation of pulse rise time. Define the terms rise time of a digital oscilloscope

13

GRAPHIC RECORDING INSTRUMENTS

INTRODUCTION

Permanent (hard copy) records of waveforms displayed on an oscilloscope can be made by use of a camera (see Section 11-10). However, for some applications, more satisfactory results can be obtained by the use of a *graphic recorder*, or *chart recorder*. The two basic laboratory type chart recorders are the *strip chart recorder* and the *XY recorder*. In the strip chart recorder, a continuously moving strip of paper is passed under a pen or other recording mechanism. The pen is deflected back and forward across the paper in proportion to an input voltage. The resulting trace is a record of input voltage variations over a given period of time. The XY recorder uses a single sheet of paper and has two inputs; one input deflects the pen horizontally and the other produces vertical deflection. In this case, the resulting trace might represent the characteristics of an electronic device or the frequency response of a circuit. The major disadvantage of chart recorders compared to oscilloscopes is that chart recorders can operate only at very low frequencies while oscilloscopes can display very high frequency waveforms.

13-1 GALVANOMETRIC STRIP CHART RECORDER

In a *galvanometric* (or *oscillographic*) strip chart recorder a strip of paper is unrolled and passed under a pen, as illustrated in Figure 13-1. The pen is at the end of a lightweight pointer connected to the coil of a PMMC type meter movement (or galvanometer). The pen deflection (or pointer position) is directly proportional to the voltage applied to the moving-coil

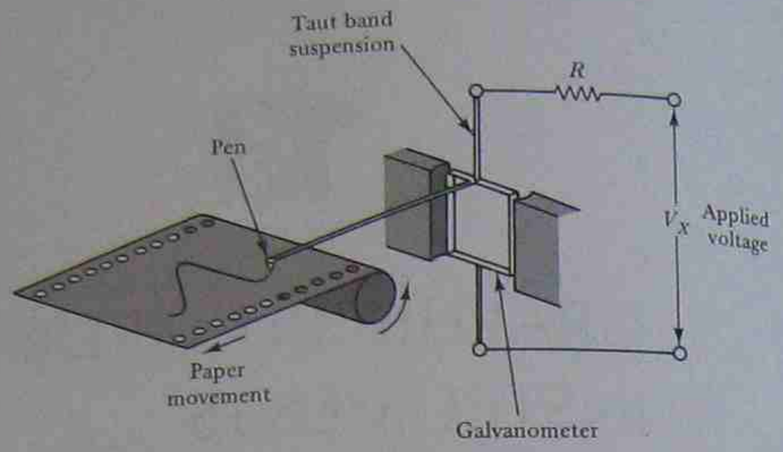


FIGURE 13-1. Galvanometric strip chart recorder using a pen to trace the waveform of an input voltage.

circuit. When a slowly changing voltage is applied to the coil, the pen is deflected back and forward across the paper. With the paper passing under the pen at a constant velocity, the waveform of the input voltage is traced out on the paper. Because the movement of the paper is proportional to time, a strip chart recorder is sometimes termed an *xt recorder*.

The pens used in this type of recorder are usually the fiber tipped type, which are disposable. Instead of a pen, *thermal* writing tips are sometimes employed. These are either tungsten or ceramic tips which are heated by an electric current. The heated tip burns a fine line on the surface of the paper.

Another method of writing on the strip chart is illustrated in Figure 13-2. In this case, the deflection system is a small galvanometer with a mirror instead of a pointer and pen. A finely focused beam of ultraviolet light is reflected from the mirror on to photographically treated paper, producing an instant trace. The one disadvantage of the *light beam* system is that specially treated paper is required. A major advantage is that this type of instrument can record waveforms with frequencies up to 5 kHz, while the galvanometric pen type recorder is usually limited to a maximum frequency of 200 Hz.

Apart from the paper-moving mechanism, a galvanometric type pen recorder is simply an analog voltmeter. Instead of using a calibrated scale, the pointer (with the pen at its end) is deflected across the recording paper. As illustrated in Figure 13-3, the circuitry is similar to the analog electronic voltmeters discussed in Section 8-6. An operational amplifier is used to give a high input resistance and to amplify small voltage levels before applying them to the galvanometer circuit. The attenuator divides high level input voltages down before they are applied to the amplifier. Thus, the galvanometer current can be set to give (for example) a deflection of 1 cm

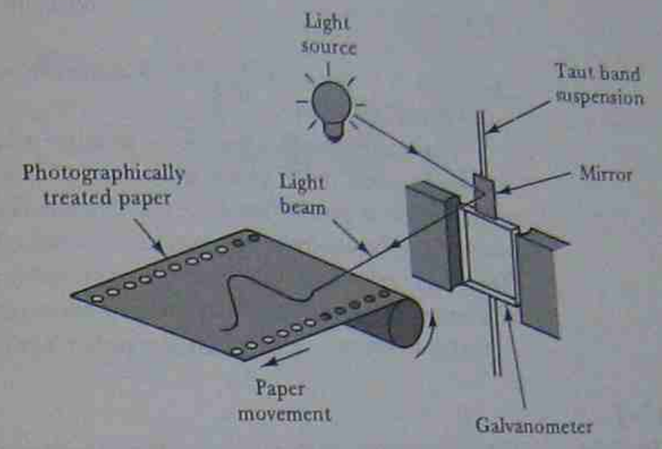


FIGURE 13-2. Strip chart recorder using a light source and a mirror mounted on a lightweight galvanometer. Photographically treated paper must be used.

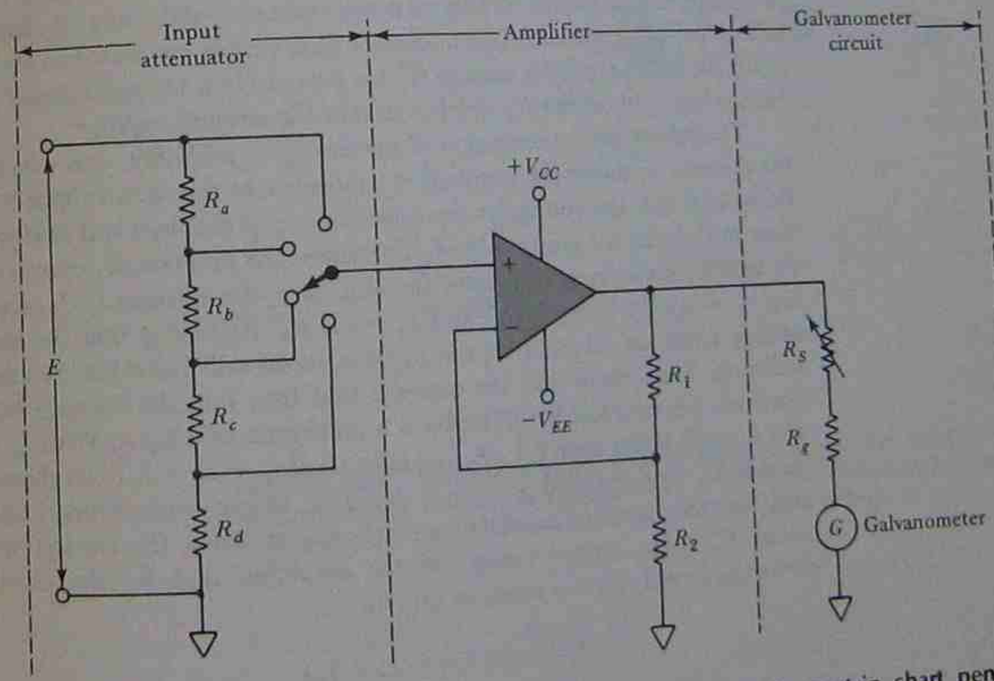


FIGURE 13-3. The galvanometer control circuit for a strip chart pen recorder is similar to an electronic voltmeter circuit.

for each 1-V input (1 cm/V). Alternatively, it might be set to give 2 cm/V, 0.1 cm/V, etc.

The paper-moving system is usually *traction feed*, in which rotating sprocket wheels drive paper with hole-punched edges. The speed of the drive motor is proportional to the current flowing in its windings. This current can be controlled by means of switched or variable series resistors. The paper velocity might be set (for example) to a high speed of 5 cm/s, or a low of perhaps 5 cm/h. A pen *up/down control* is also usually included, so that the pen can be lifted off the paper while adjustments are made.

13-2 POTENTIOMETRIC STRIP CHART RECORDER

The *potentiometric* strip chart recorder mechanism is essentially that of a self-balancing dc potentiometer (see Section 5-10). The basic arrangement for controlling the pen position is illustrated in Figure 13-4. The pen holder slides along a pen carriage shaft under the control of a *drive cord*. The drive cord passes over an *idler pulley* and a *drive pulley* which is mechanically coupled to a *servo motor*. The pen holder makes electrical contact to a *potentiometer slide wire* which has a dc supply voltage ($\pm E$) applied to its terminals. It also makes contact to a low resistance slide wire, so that the voltage *picked-off* from the potentiometer slide wire is connected to the low resistance slide wire. This voltage (V_F) is passed via a voltage follower (see Section 8-6-2) to resistor R_4 which is part of the *summing amplifier*.

To understand the operation of the summing amplifier, first note that the op-amp noninverting terminal is connected to the zero voltage level. Because of this, the voltage at the inverting input terminal will always be close to the zero (or ground) level. Therefore, the junction of resistors R_2, R_3, and R_4 is always at zero volts. Consequently, the currents I_2, I_3, and I_4 are: $I_2 = V_2/R_2$, $I_3 = V_i/R_3$, and $I_4 = V_F/R_4$. Assuming that the input voltage levels are all positive, the input currents will have the directions indicated. Now recall that the currents that flow into the op-amp input terminals are very low levels, perhaps a maximum of 0.5 μA. With I_2, I_3, and I_4 much larger than 0.5 μA, virtually all of $I_2 + I_3 + I_4$ flows through resistor R_5. One terminal of R_5 is at zero (i.e., at the noninverting input), and the other terminal is at the op-amp output. Thus, the voltage drop across R_5 is the output voltage of the amplifier, and for the current directions shown this is a negative quantity:

$$V_o = -R_5(I_2 + I_3 + I_4)$$

$$= -R_5\left(\frac{V_2}{R_2} + \frac{V_i}{R_3} + \frac{V_F}{R_4}\right);$$

if $R_2 = R_3 = R_4 = R_5$,

$$\boxed{V_o = -(V_2 + V_i + V_F).} \qquad (13\text{-}1)$$

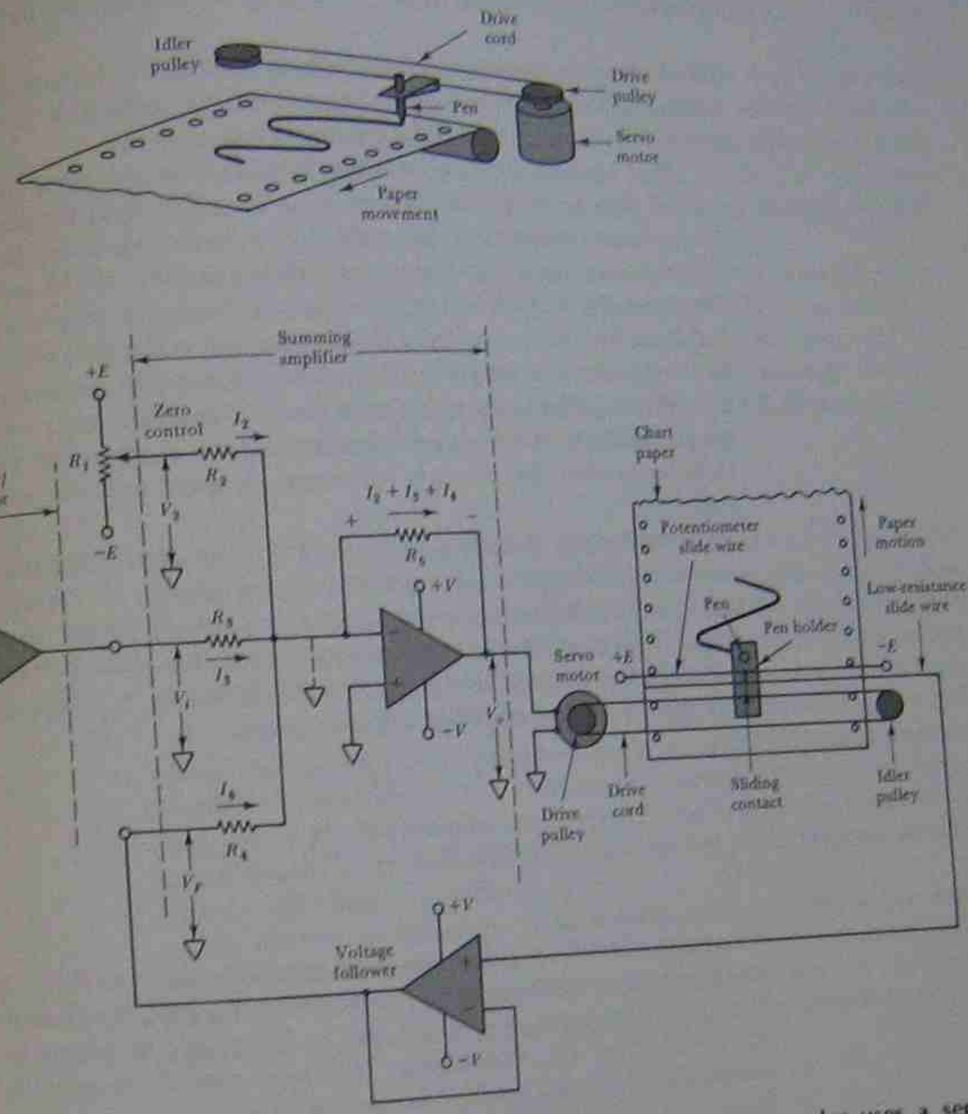


FIGURE 13-4. The potentiometric strip chart pen recorder uses a servo motor to move the pen across the chart. A feedback voltage (V_i) is derived from a potentiometer slide wire to balance the input voltage.

Thus, the output voltage of the summing amplifier is the sum of the input voltages. The negative sign indicates that the output is inverted, i.e., positive inputs give a negative output, and vice versa.

Now consider what occurs when input voltage V_i is zero, and the zero control is set to the center point on R_1 to give $V_2 = 0$. If the pen holder is at the center point on the slide wire, $V_F = 0$. In this situation, the amplifier output is also zero, and there is no voltage applied to the servo motor. Consequently, the pen remains stationary at the center point on the chart. If the pen had been away from the center point on the slide wire, V_F would be some positive or negative voltage level. This would produce an output from the amplifier to drive the servo motor. The servo motor would move the pen holder in the direction necessary to make V_F approach zero. When V_F becomes zero, the motor is no longer energized and the pen remains stationary.

With the pen stationary at the center of the chart, suppose the zero control potentiometer (R_1) is now adjusted to give $V_2 = +E/2$. With V_F and V_i both zero, input current I_2 flows through R_5 giving output $V_o = -E/2$. This energizes the servo motor, causing it to drive the pen holder towards the $-E$ terminal of the slide wire. When $V_F = -E/2$, Equation 13-1 applies and the amplifier output becomes:

$$\begin{aligned} V_o &= -(V_2 + V_i + V_F) \\ &= -\left(\frac{E}{2} + 0 - \frac{E}{2}\right) \\ &= 0. \end{aligned}$$

Therefore, when $V_F = -V_2$, there is no amplifier output to drive the servo motor, and once again the pen remains stationary. If R_1 is adjusted to give $V_2 = -E/2$ or to $V_2 = -E$, the pen is driven to the points at which $V_F = +E/2$ or $+E$, respectively. It is seen that R_1 is actually a *pen zero-position-control* that enables the pen to be set to any point across the chart.

Finally, consider the input voltage V_i, which is applied via an *amplifier/attenuator* input stage. As in the case of oscilloscopes, this input stage allows small voltages to be amplified and large voltage levels to be attenuated, to obtain convenient input levels for operating the circuitry. When V_i is a positive quantity, the amplifier output causes the servo motor to drive the pen holder in the direction of the $-E$ slide wire terminal. When V_F becomes equal to $-V_i$, the amplifier output is zero, and the pen is stationary. When V_i is a slowly changing quantity, the pen moves continuously, keeping $V_F = -V_i$ and tracing the waveform of V_i on the moving chart paper. By adjusting the zero control, the waveform of V_i can be traced symmetrically about the center line on the chart paper, or at any other point across the chart.

The accuracy of the potentiometric type strip chart recorder depends upon supply voltages $\pm E$. The instrument should be calibrated periodically to check the accuracy. This normally involves application of accurately measured positive and negative dc input levels. The deflection produced by each input level is checked, and the supply voltages adjusted as necessary to produce the appropriate deflection.

A major disadvantage of the potentiometric type strip chart recorder is that its frequency response is very low. Typically, 10 Hz is the maximum input frequency that may be traced. An important advantage of the potentiometric instrument is that it can be much more accurate than the galvanometric type. Typical specified accuracies are $\pm 0.2\%$ for potentiometric type, and $\pm 2\%$ for galvanometric instruments.

13-3 SOLID STATE ELECTRODE STRIP CHART RECORDER

The strip chart recording method illustrated in Figure 13-5 uses a stationary bank of individual recording electrodes covering the entire width of the chart. One such instrument (the HI0KI 810) has 200 electrodes which record by means of an electrical discharge on specially prepared paper. Waveforms are traced in the form of broken lines. Because no mechanically moving parts are involved in the recording process (the paper is still moved mechanically), this instrument has a very good frequency response. Typically, frequencies up to 1 kHz can be recorded, which is much better than the 10 Hz for potentiometric type and the 200 Hz for the galvanometric pen recorder. It is still not as good as the 5-kHz response possible with the light beam type recorder.

A method of using the instantaneous voltage levels of an input waveform to energize the appropriate recording electrodes is illustrated in Figure 13-6. The input is amplified or attenuated as necessary, and then applied to the commoned input terminals of 200 *voltage comparators* (one for

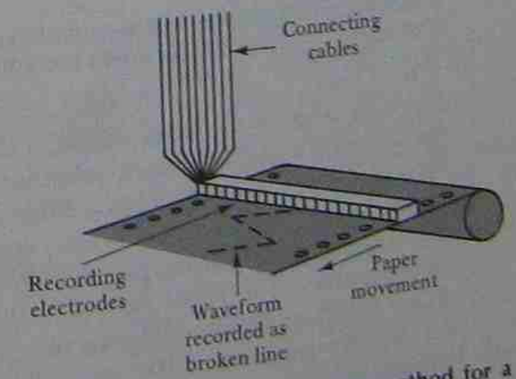


FIGURE 13-5. Solid-state electrode recording method for a strip chart recorder.

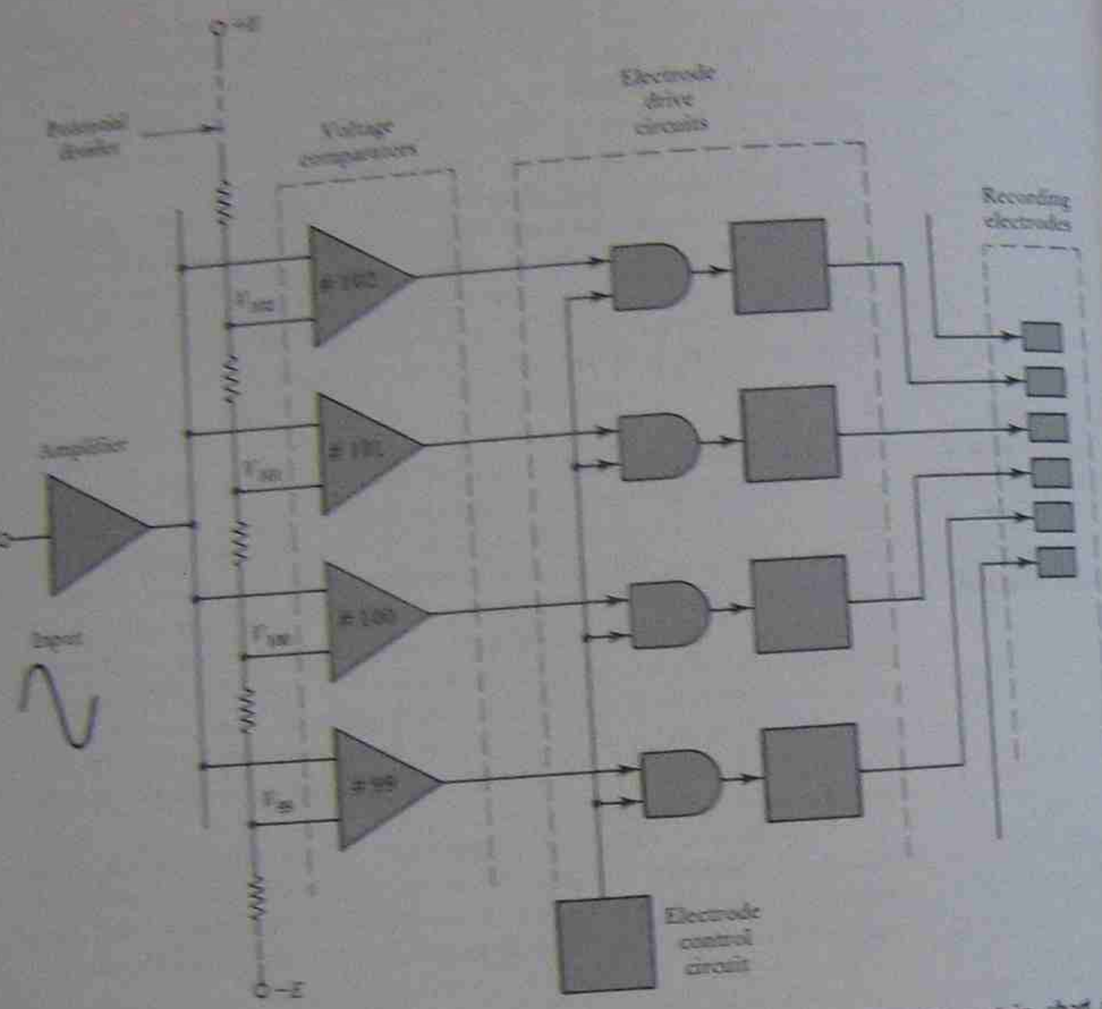


FIGURE 13-6. Electrode selection and control system for a strip chart recorder using a solid-state electrode recording method.

each electrode). As the name implies, a voltage comparator compares the instantaneous input level to a reference voltage (see Section 12-3). In Figure 13-6 each comparator has a different reference voltage level derived by the potential divider resistors from supply voltages $\pm E$. For example, the reference voltage for comparator 100 might be $V_{100} = 0$ V, while that for comparator 101 might be $V_{101} = 0.1$ V, and for comparator 102 $V_{102} = 0.2$ V, etc. When the instantaneous input voltage is between 0 and 0.1 V, only comparator 100 produces an output. When the input is between 0.1 V and 0.2 V, comparator 101 is the only one with an output. The output voltage from each comparator goes to the *drive circuit* for its

associated electrode. An *electrode control circuit* switches the electrodes on periodically. The input stage of each drive circuit has an AND gate (see Section 9-2) which causes the electrode to be energized only when inputs are present from the comparator and from the control circuit. If the input waveform is a constant dc level, one comparator has a continuous output to its electrode drive circuit. The electrode records a broken line as it is energized periodically by the control circuit. When the input is continuously changing, comparators trigger on one after another as the input voltage goes through each reference level. The appropriate electrode drive circuits are energized one after another, and a broken-line waveform is traced on the chart.

13-4 XY RECORDER

An *XY recorder* uses a single stationary sheet of chart paper, and records by moving the pen simultaneously in both the X and Y directions. The recorder mechanism is the same as that of the potentiometric strip chart recorder illustrated in Figure 13-4, except that two complete self-balancing potentiometers are involved. Figure 13-7 shows that the pen holder slides

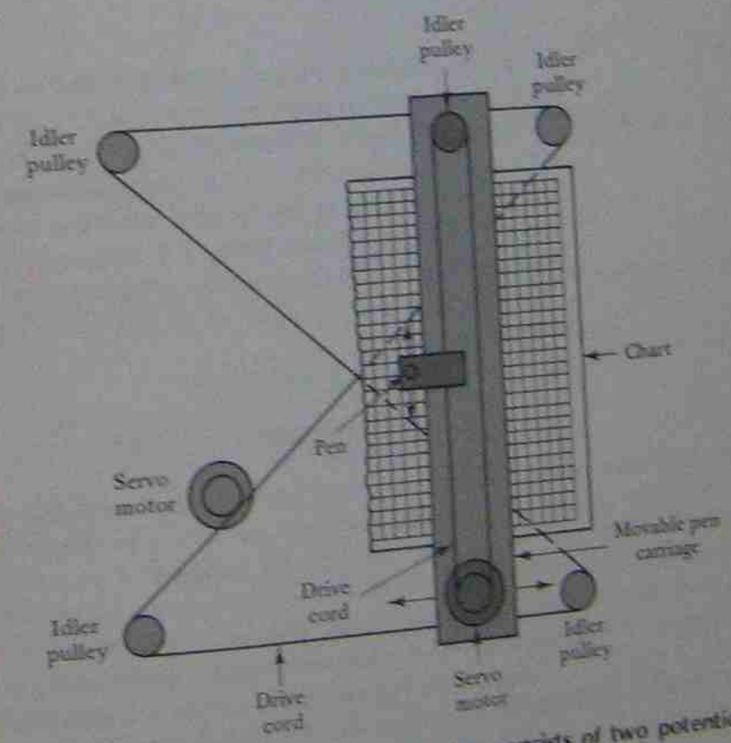


FIGURE 13-7. The XY recorder mechanism consists of two potentiometric pen recorder movements operating at 90° to each other.

along a movable *pen carriage*. A servo motor, idler pulley, and drive cord control the pen position. The entire pen carriage and drive system can be made to slide across the chart paper under the control of another servo motor. Note that the servo motor controlling the position of the pen carriage uses a crossed drive cord which is mounted on four idler pulleys. Two potentiometer slide wires, two low resistance slide wires, and the associated control circuitry are required. These are not illustrated in Figure 13-7.

The control circuits for the X input and Y input are each essentially the same as shown in Figure 13-4. Each has a zero control, a summing amplifier, and a voltage follower for feedback from the slide wire. A typical input amplifier stage is illustrated in Figure 13-8. The circuit is a *noninverting amplifier* (see Section 8-6-3). With switches S_1 and S_2 in the positions shown, the amplifier gain is

$$0.1\text{ V/cm gain} = \frac{R_2 + R_3 + R_4}{R_3 + R_4}$$
$$= \frac{900\text{ k}\Omega + 90\text{ k}\Omega + 10\text{ k}\Omega}{90\text{ k}\Omega + 10\text{ k}\Omega}$$
$$= 10.$$

The S_2 position in Figure 13-8 is identified as 0.1 V/cm. Therefore, a 0.1-V input would produce an output of $10 \times 0.1\text{ V} = 1\text{ V}$. When this 1-V input is applied to the summing amplifier, it produces a pen deflection of 1 cm. When S_2 is in the 1-V/cm position, the amplifier output terminal is connected directly to the op-amp inverting input terminal. Thus the circuit is a voltage follower, giving 1 V output for 1 V input. This gives a deflection of 1 cm. So the amplifier produces 1 cm of deflection for each 1-V input. Now suppose S_2 is set to the 0.01-V/cm position. The gain becomes

$$0.01\text{ V/cm gain} = \frac{R_2 + R_3 + R_4}{R_4}$$
$$= \frac{900\text{ k}\Omega + 90\text{ k}\Omega + 10\text{ k}\Omega}{10\text{ k}\Omega}$$
$$= 100.$$

Thus, each 0.01-V input gives an output of $100 \times 0.01\text{ V} = 1\text{ V}$. Once again, this 1-V output gives 1 cm of pen deflection.

When S_1 in Figure 13-8 is moved from the RANGE position to the VERNIER position, R_2, R_3, and R_4 are disconnected from the op-amp inverting input. Variable resistor R_5 together with resistor R_6 allows the

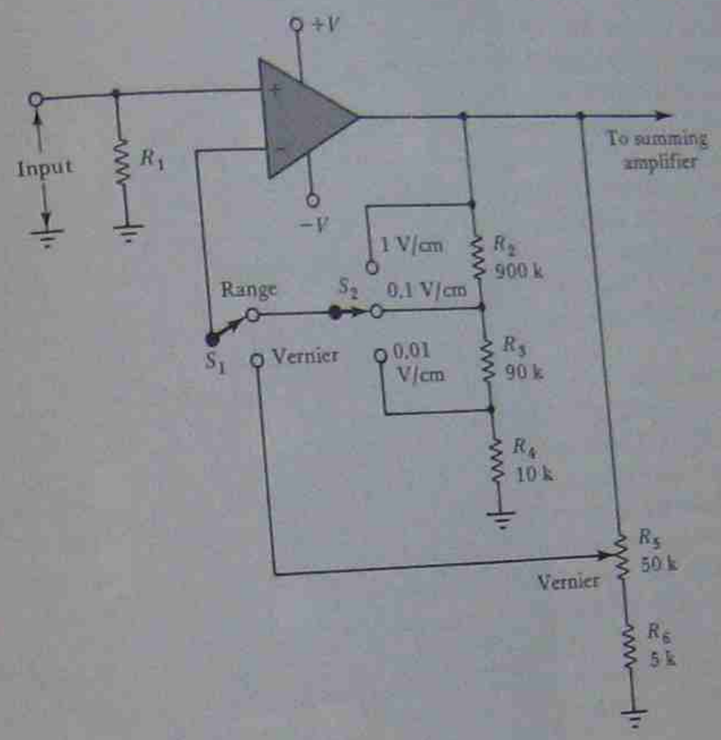


FIGURE 13-8. Input amplifier for XY recorder. With S_1 and S_2 as shown: Gain $= \frac{R_2 + R_3 + R_4}{R_3 + R_4}$.

amplifier gain to be adjusted from a minimum of 1 to a maximum of:

$$\text{vernier gain} = \frac{R_5 + R_6}{R_6} = \frac{50\text{ k}\Omega + 5\text{ k}\Omega}{5\text{ k}\Omega}$$
$$= 11.$$

A typical XY recorder control panel is shown in Figure 13-9. Each (Y and X) input has two terminals identified as + and −, and a *common* terminal is included between the two inputs. The inputs are actually *floating*, i.e., none are grounded. However, the two negative input terminals may be connected together internally, and if an input source has a ground or low voltage terminal it should be connected to a negative input terminal.

The Y and X input controls in Figure 13-9 consist of: a function switch with RANGE, VERNIER, and CHECK-ZERO positions; a RANGE

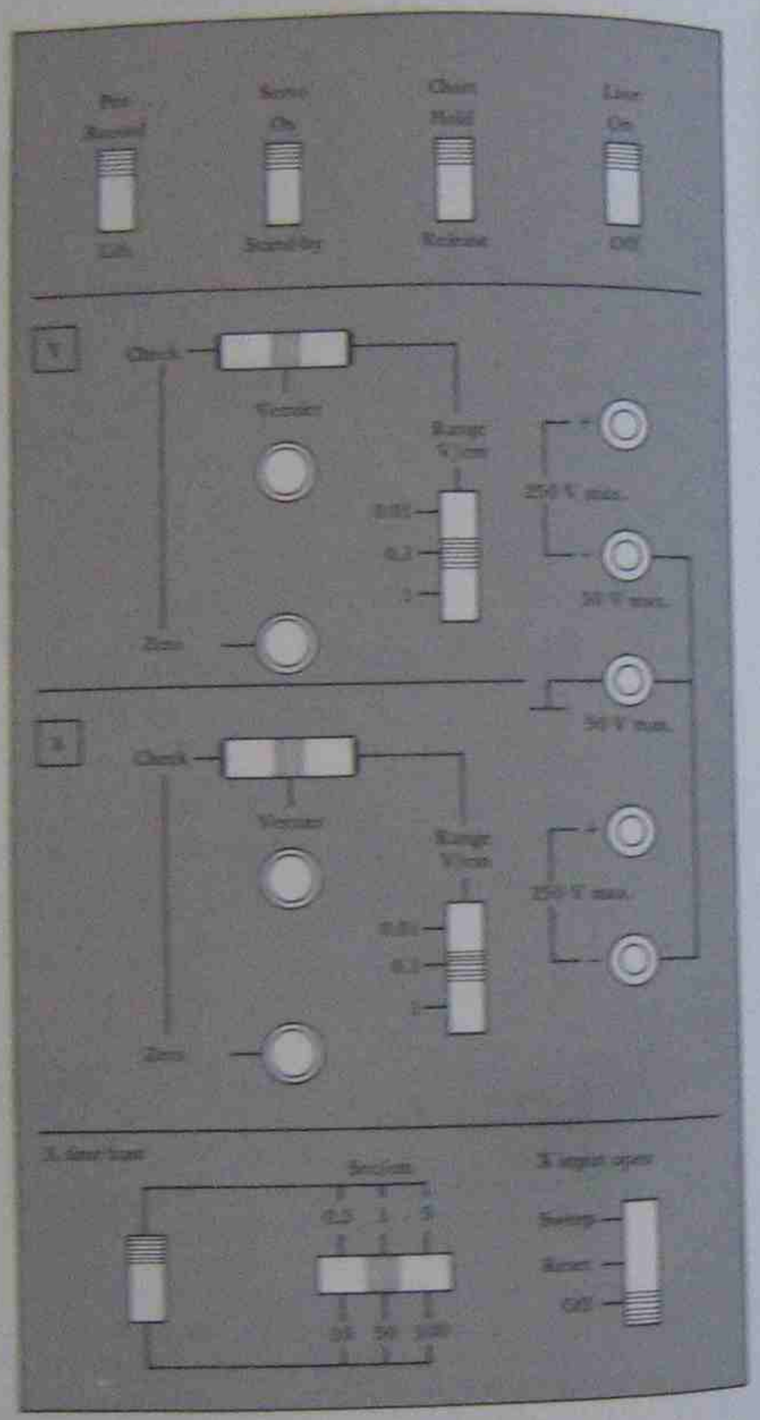


FIGURE 13-9. Control panel of the Hewlett-Packard 7035A XY Recorder (Courtesy of Hewlett-Packard).

switch with 0.01, 0.1, and 1 V/cm positions; a VERNIER control knob; and a ZERO control knob. The positions on the range selector switch correspond to those on S_1 in Figure 13-8. Also, the VERNIER and RANGE positions of the function switch correspond to positions of S_1 in Figure 13-8. The VERNIER control knob has the same effect as R_2 in Figure 13-8, as explained above. When the function switch is in its CHECK-ZERO position, the input voltage is disconnected, so that only the ZERO control knob affects the pen position. The zero control operates like potentiometer R_1 in Figure 13-4, so the CHECK-ZERO position is simply a means of disconnecting the input and checking just where the pen zero position is on the chart.

Above the *Y* and *X* controls in Figure 13-9 is a row of switches identified as PEN, SERVO, CHART, and LINE. The LINE switch is simply an *on / off* switch for the ac supply. The chart HOLD/RELEASE switch controls a high voltage source which electrostatically holds the chart in position. This prevents the chart from sliding when the pen is tracing the input signals. When in the HOLD position a dc voltage (around 500 V) is applied to interlined comb-shaped metal films located just below the surface of the plastic table top (see Figure 13-10). A similar pattern of high voltages are induced (by the applied voltage) in the chart paper on the table top, and these cause the paper to be attracted towards the opposite polarity metal film lines. In this way the paper is held down firmly on the surface of the chart table.

The SERVO ON/STAND-BY switch (in Figure 13-9) disconnects all inputs when in the STAND-BY position. At this time the pen position is not affected by any control or input voltage adjustment. In the SERVO ON position, the inputs are connected and pen deflection proportional to the input voltage occurs. The PEN RECORD/LIFT control activates a solenoid which pulls the pen down onto the chart paper when in the RECORD position. In the LIFT position the solenoid is not energized, and the pen is lifted off the paper by the action of a spring.

At the bottom of the control panel shown in Figure 13-9 is a set of switches identified as *X* TIME BASE. The time base circuitry is similar to the time base in a cathode-ray oscilloscope, except that in an *XY* recorder the time base is normally not repetitive. By means of the time base, the pen can be made to sweep from left to right at one of several rates. Once the rate (in sec/cm) is selected, the time base is either triggered manually, or by means of an external signal. When the trace is complete, the pen can be reset back to its initial zero position, ready for triggering again. Some *XY* recorders do not have a time base.

The typical input resistance of an *XY* recorder is 1 MΩ, with a 10-MΩ resistance to ground. Accuracy is usually around ±0.3% of full scale. In an *XY* recorder specification the term *deadband* defines the minimum input

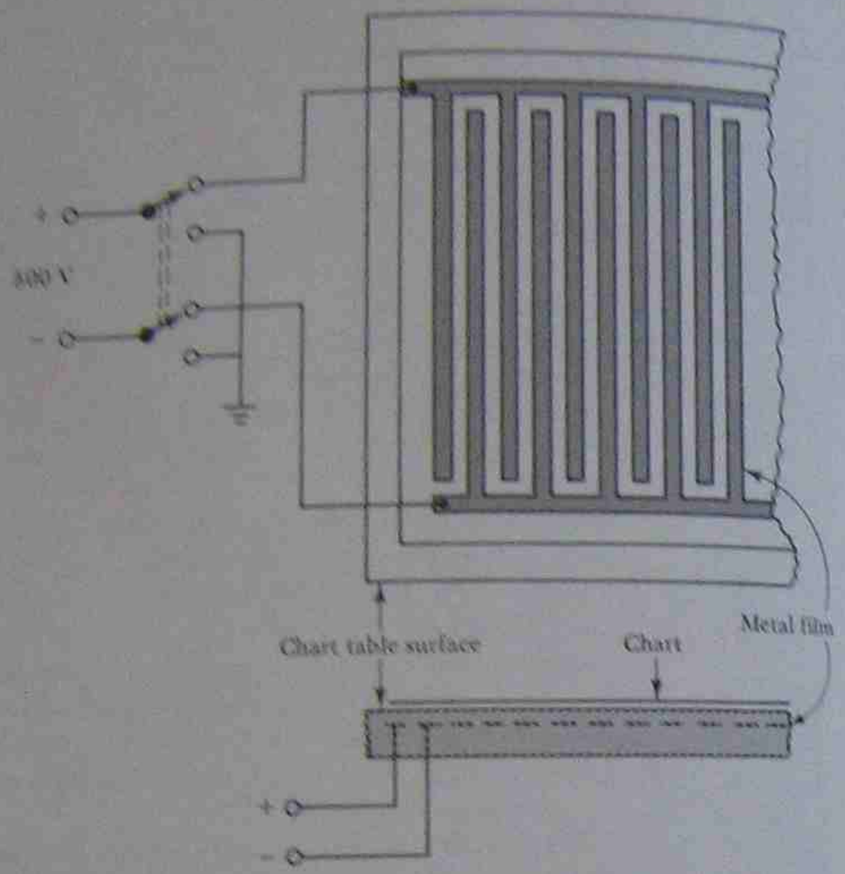


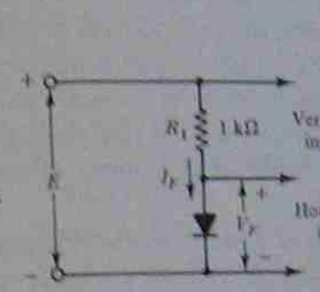
FIGURE 13-10. Electrostatic system for holding down the chart paper on an XY recorder.

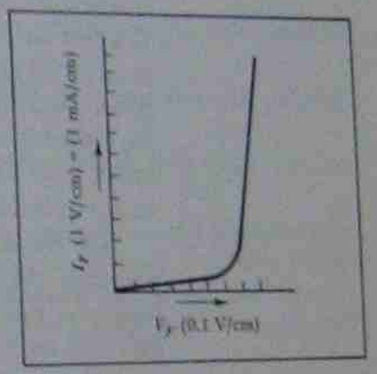
voltage necessary to produce pen movement. Typical deadband might be 0.2% of full scale. *Common mode* inputs are input voltages that appear at both X input terminals at once, or at both Y input terminals. For example, if an input voltage which is to produce deflection is superimposed upon a 10-V bias level, this 10-V level is a common mode input. It is important that such input voltages do not produce any pen deflection. A *common mode rejection ratio* of 90 dB implies that common mode inputs are effectively attenuated by 90 dB. Attenuating by 90 dB is approximately the same as dividing by 32 000. Therefore, a 10-V common mode input would produce the same deflection as a normal input of 10 V/32 000, i.e., approximately 0.3 mV. One other item always listed on an XY recorder specification is the *slewing speed*. This defines the fastest rate at which the pen can be deflected, and might typically be stated as 50 cm/s. The slewing speed limits the maximum signal frequency that may be recorded. Like the potentiometric strip chart recorder, the highest signal frequency that can be recorded by most XY recorders is around 10 Hz.

13-5 PLOTTING DEVICE CHARACTERISTICS ON AN XY RECORDER

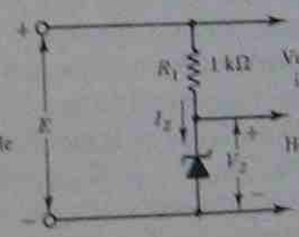
Large-scale characteristics for many types of electronic devices can be traced on an XY recorder. The method is much faster and more convenient than point-by-point plotting, and gives more satisfactory results than a photograph of a CRT display. Figure 13-11(a) shows the circuit for obtaining the forward characteristic of a semiconductor diode. The typical resultant characteristic is also shown. R_1 is a 1-kΩ resistor connected to the

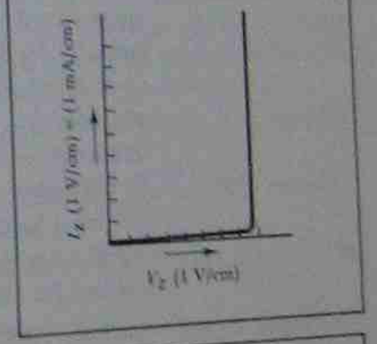
(a) Tracing the forward characteristics of a diode



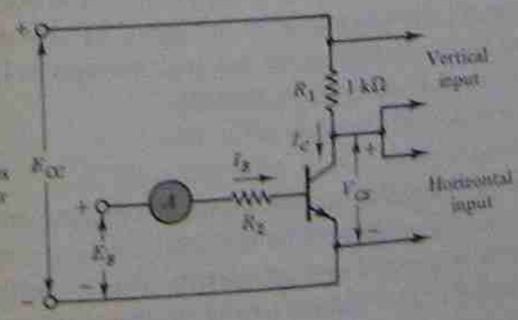


(b) Tracing the characteristics of a zener diode





(c) Tracing the collector characteristics of a transistor



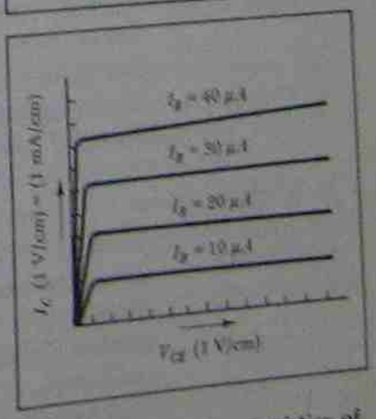


FIGURE 13-11. The XY recorder can be used to trace the characteristics of many electronic devices.

vertical input of the *XY* recorder. When the diode forward current is 1 mA, a 1-V drop is produced across R_1. With the vertical deflection sensitivity at 1 V/cm, the 1-V input produces a 1-cm vertical deflection on the chart. So the vertical scale on the characteristic can be identified as 1 mA/cm. The diode terminals are connected to the horizontal input, and the horizontal input range is set to 0.1 V/cm. For a silicon diode V_F is approximately 0.7 V, thus the maximum horizontal deflection is around 7 cm. The vertical and horizontal ordinates of the graph can be drawn by adjusting the *X* and *Y* zero controls to move the pen. To trace the characteristic, supply voltage *E* is first set to zero, and the pen position is adjusted to the desired zero point on the graph. The supply voltage is then manually adjusted (using a power supply) from zero to the level necessary to trace the characteristic to the desired forward current level. At this point the pen RECORD/LIFT switch is set to LIFT before *E* is reduced to zero. If this is not done a double trace may result.

The characteristics of a zener diode [Figure 13-11(b)] are traced in essentially the same way as for an ordinary diode. In this case, the horizontal scale should be set to 1 V/cm in order to give a convenient deflection for breakdown voltages ranging from 3 V to 12 V.

To trace the collector characteristics of a transistor, two power supplies are required, as illustrated in Figure 13-11(c). With the pen lifted and E_{CC} around 5 V, E_B is adjusted to give a convenient level of bias current, e.g., $I_B = 10\ \mu A$. E_{CC} is next reduced to zero, the pen is lowered onto the chart, and then E_{CC} is gradually increased to produce the transistor collector characteristic for $I_B = 10\ \mu A$. The pen is now lifted off the chart again and E_B is adjusted to increase I_B to 20 μA. E_{CC} is reduced to zero once again, the pen is lowered, and E_{CC} is again gradually increased. This causes the pen to trace the characteristic for $I_B = 20\ \mu A$. The process described is repeated for other levels of I_B to give any number of characteristics.

The characteristics of field effect transistors and vacuum tubes may also be traced on an *XY* recorder. The characteristics of negative resistance devices such as tunnel diodes cannot be produced by this method because the slewing speed of the recorder is just not high enough to follow the rapid change of state in device voltage and current.

13-6 MEMORY RECORDER

A *memory recorder* periodically samples input waveforms and converts the analog samples into digital form. The digitized levels are stored and then reproduced at a slow enough rate to operate a potentiometric type pen recorder mechanism. This is similar to the operation of a digital storage oscilloscope, as described in Section 12-4. One such instrument (the YEW 3069 memory recorder) has a specified input frequency response of dc to 50 kHz. To give a smooth trace, an interpolation process is used to add up to 32 additional samples between each pair of actual waveform samples.

This particular instrument can be used as a strip chart recorder, or as an *XY* recorder. Among additional features it has the ability to print on the chart a list of measured sample levels, the instrument range settings when the samples were taken, and the date and time at which the data was recorded.

REVIEW QUESTIONS AND PROBLEMS

13-1. Sketch the basic construction of a pen-type galvanometric strip chart recorder. Explain.

13-2. Sketch the basic construction of a light-beam type galvanometric strip chart recorder. Explain.

13-3. Compare the performance of light-beam and pen-type galvanometric strip chart recorders.

13-4. Sketch a control circuit for a galvanometric strip chart recorder. Briefly explain.

13-5. Draw a sketch to show the basic construction of a potentiometric strip chart recorder. Also sketch a summing amplifier control circuit for the moving system. Explain the operation of the complete system. State the typical upper frequency limit and accuracy for this type of pen recorder.

13-6. Draw a sketch to show the operation of a solid-state electrode strip chart recorder. Also sketch the block diagram of the electrode selection and control system for this recording method. Explain the operation of the recorder, and discuss its frequency response.

13-7. Sketch the mechanical system of a potentiometric XY recorder. Explain its operation.

13-8. Sketch the circuit of an input amplifier for an XY recorder. Explain the operation of the circuit.

13-9. List the controls normally found on an XY recorder. Explain the function of each control.

13-10. Briefly explain the electrostatic chart-holding system employed on XY recorders.

13-11. Sketch the circuits used when plotting diode and zener diode characteristics on an XY recorder. Explain the operation of each circuit and the recording procedure. Also explain why the traced characteristics may be marked in mA/cm and V/cm.

13-12. Sketch the circuit used for plotting the collector characteristics of a transistor on an XY recorder. Explain the circuit operation and the recording procedure.

13-13. Briefly explain a memory recorder, and compare its performance to other strip chart and XY recorders.

14

dc POWER SUPPLIES

INTRODUCTION

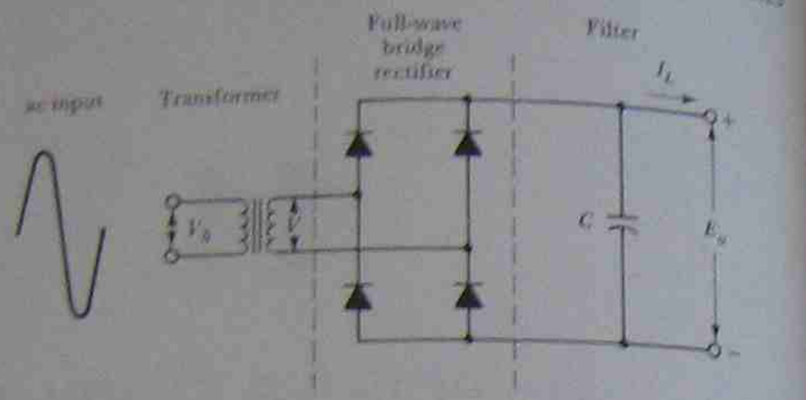
The basic types of dc power supplies used in an electronics laboratory are: unregulated transformer rectifier circuits with filters; single output voltage units using series regulators; multioutput units; and power supplies employing switching regulators. The first and last type listed are essentially for use where high levels of load current must be supplied. The transformer, rectifier, and filter circuit are suitable where the stability of the output voltage is not critical and the ripple voltage content in the output is unimportant. Where a high current supply is required with reasonably good voltage stability, a switching regulator may be most suitable.

The single voltage output unit with a series regulator is probably the most commonly used laboratory power supply. This has good control of output voltage level, and excellent voltage stability. Current limiting or short-circuit protection is also normally included.

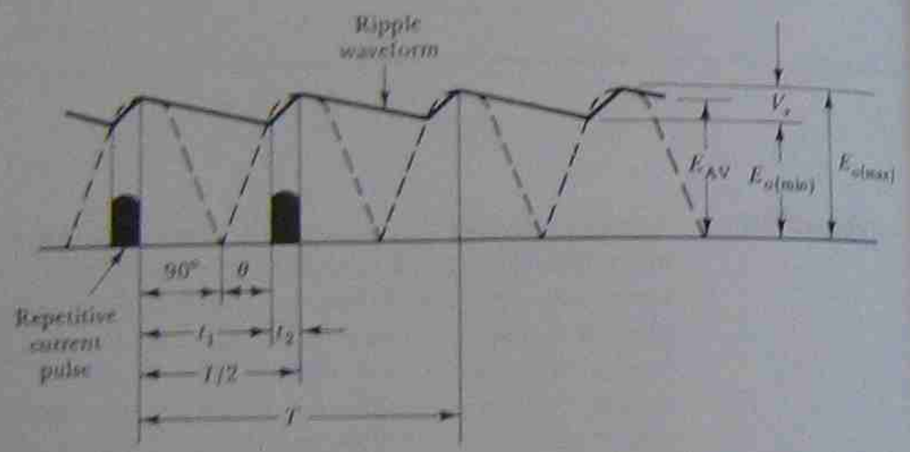
Line regulation and *load regulation* are important parameters which describe the performance of a power supply. Null methods are normally required to measure these parameters.

14-1 UNREGULATED dc POWER SUPPLIES

Laboratory type dc power supplies normally consist of a transformer, a full wave bridge rectifier, and a filter circuit. Such a circuit is shown in Figure 14-1(a).



(a) dc power supply consisting of: transformer, bridge rectifier, and reservoir capacitor



(b) Output from full-wave rectifier with capacitor smoothing circuit

FIGURE 14-1. Basic dc power supply circuit and waveforms.

The transformer converts the normal 120-V supply to an rms voltage which is related to the required dc output voltage. By means of the full-wave bridge rectifier (discussed in Section 2-3-2), the transformer secondary voltage is converted to repetitive positive half cycles of sinusoidal voltage. The filter smoothes the rectified half cycles to make it more closely approximate a dc voltage.

Consider the power supply output waveforms from the circuit as illustrated in Figure 14-1(b). The rectified positive half cycles are shown in broken-line form. The filter circuit consists essentially of the *reservoir capacitor*. The capacitor is charged up to the peak of the output voltage,

and if no output load current flows the capacitor remains charged to the peak voltage. In this case the output voltage is a constant level equal to the peak voltage. When a load current (I_L) is drawn from the supply, the capacitor partially discharges between voltage peaks [see Figure 14-1(b)]. Each time the rectified output approaches the peak voltage, current flows to recharge the capacitor. The capacitor acts as a *reservoir* to supply load current as required. The current from the bridge rectifier and transformer is a series of pulses occurring at the voltage peaks.

The output voltage from the power supply is an average dc level (E_{av}), with a ripple voltage (V_r) superimposed. The amplitude of the ripple depends upon the load current and upon the size of the reservoir capacitor. The minimum level of the output voltage is $E_{o(min)}$, the maximum level is $E_{o(max)}$, and the ripple amplitude is V_r [see Figure 14-1(b)]. The time during which the capacitor is discharging is t_1, which is the sum of the times for 90° and θ°. The time t_2 is the capacitor charging time.

$$t_1 = (\text{time for } 90°) + (\text{time for } \theta°), \tag{14-1}$$

$$t_2 = (\text{time for } 90°) - (\text{time for } \theta°), \tag{14-2}$$

$$E_{o(min)} = E_{o(max)} \sin \theta,$$

$$\text{or} \quad \theta = \arcsin \frac{E_{o(min)}}{E_{o(max)}}. \tag{14-3}$$

Assuming that load current I_L is constant, the equation $C = It/V$ can be employed to determine the required capacitor size:

$$C = \frac{I_L \times t_1}{V_r}. \tag{14-4}$$

EXAMPLE 14-1 A dc power supply with the circuit shown in Figure 14-1(a) is to provide an average output of 20 V with a 10% maximum ripple voltage. The supply frequency is 60 Hz, and the load current is 100 mA. Determine the size of the reservoir capacitor.

SOLUTION

$$V_r = 10\% \text{ of } 20 \text{ V} = 2 \text{ V}$$
$$E_{o(min)} = 20 \text{ V} - 1 \text{ V} = 19 \text{ V}$$
$$E_{o(max)} = 20 \text{ V} + 1 \text{ V} = 21 \text{ V}$$

From Equation 14-3,

$$\theta = \arcsin\frac{19\text{ V}}{21\text{ V}}$$
$$= 65°,$$
$$T = 1/60\text{ Hz} = 16.6\text{ ms}$$
$$= \text{time for } 360°.$$

Equation 14-1,

$$t_1 = (\text{time for } 90°) + (\text{time for } \theta°)$$
$$= \frac{16.6\text{ ms}}{360°}(90° + 65°)$$
$$= 7.16\text{ ms}.$$

Equation 14-4,

$$C = \frac{I_L t_1}{V_r}$$
$$= \frac{100\text{ mA} \times 7.16\text{ ms}}{2\text{ V}}$$
$$= 358\ \mu\text{F}.$$

The forward voltage drop across each rectifier is a minimum of $V_F = 0.7$ V for silicon rectifiers, and may exceed 1 V when the current is greater than 1 A. Because each pair of rectifiers conduct in series in a bridge rectifier the total rectifier voltage drop is $2V_F$. The peak output voltage [from Figure 14-1(b)] is $E_{s(\max)}$. So the peak input voltage to the bridge rectifier circuit is

$$\boxed{V_P = E_{s(\max)} + 2V_F} \qquad (14\text{-}5)$$

and the transformer rms secondary voltage is $V = 0.707V_P$.

In a bridge rectifier, when two of the rectifiers are conducting, the other two are reverse biased, and the *peak reverse voltage* (or *peak inverse voltage*) V_R is equal to the transformer peak output voltage (V_P). In a half-wave rectifier circuit (see Section 2-3-4), $V_R = 2V_P$.

The rms current that must be supplied by the transformer is related to the average output current drawn from the power supply. However, as already explained, the current supplied by the transformer to the capacitor via the rectifiers is actually in the form of repeating pulses. This current is termed the *peak repetitive current* (I_{rep}), and it can be calculated from I_L, T,

and t_2. Since I_L flows continuously during time $T/2$, the capacitor is discharged by $I_L T/2$ coulombs. During time t_2 when I_{rep} flows, the capacitor is recharged by $I_{rep}t_2$ coulombs. For the capacitor to be completely recharged during t_2:

$$I_{rep}t_2 = I_L T/2$$

or

$$\boxed{I_{rep} = \frac{I_L T}{2t_2}.} \qquad (14\text{-}6)$$

The transformer secondary must be able to supply this current (I_{rep}), and the rectifiers must be able to pass the current.

EXAMPLE 14-2 Specify the transformer output and the rectifiers for the power supply in Example 14-1.

SOLUTION

Transformer:
Equation 14-5,

$$V_P = E_{s(\max)} + 2V_F$$
$$= 21\text{ V} + (2 \times 0.7\text{ V})$$
$$= 22.4\text{ V}.$$

rms *output voltage:*

$$V = 0.707V_P = 0.707 \times 22.4\text{ V}$$
$$= 15.8\text{ V}.$$

rms *output current:*

$$I = 1.11\, I_{AV} = 111\text{ mA}.$$

Peak repetitive current:
Equation 14-2,

$$t_2 = (\text{time for } 90°) - (\text{time for } \theta°)$$
$$= \frac{16.6\text{ ms}}{360°}(90° - 65°)$$
$$= 1.15\text{ ms};$$

Equation 14-6,

$$I_{rep} = \frac{I_L T}{2t_2}$$
$$= \frac{100\text{ mA} \times 16.6\text{ ms}}{2 \times 1.15\text{ ms}}$$
$$= 0.722\text{ A}.$$

Rectifiers:

peak reverse voltage $V_p = 22.4$ V,

peak repetitive current $I_{rep} = 0.722$ A.

In Example 14-2, note that the peak repetitive current is very much greater than the output load current.

The use of a choke together with the reservoir capacitor further reduces the amplitude of the output ripple voltage (Figure 14-2). A *bleeder resistor* (R) is sometimes included in the circuit to maintain a minimum current flow in the choke when there is no output load current. This keeps the choke operating and thus helps to minimize the change in voltage drop across the choke when load current is demanded. When no *voltage regulator* (see Section 14-2) is employed, choke-capacitor filtering gives the most constant dc output voltage with the lowest ripple content.

Figure 14-3 shows the circuit of a high current unregulated dc power supply. The transformer has two secondary windings which can be switched (by S_1) to operate either in series or in parallel. When the windings are connected in series the dc output voltage is 12 V. Parallel operation gives an output of only 6 V. However, the 12-V output might be capable of supplying 10 A, while with parallel secondary windings the 6-V output may supply 20 A.

Ideally a dc power supply should produce a constant dc output voltage which does not change. However, dc voltages derived from rectified ac usually have some ripple voltage content. So the ripple output

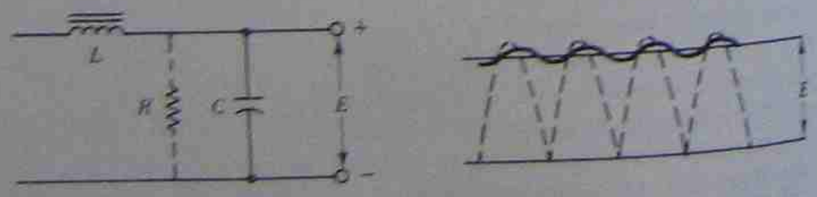


FIGURE 14-2. Choke-capacitor filtering.

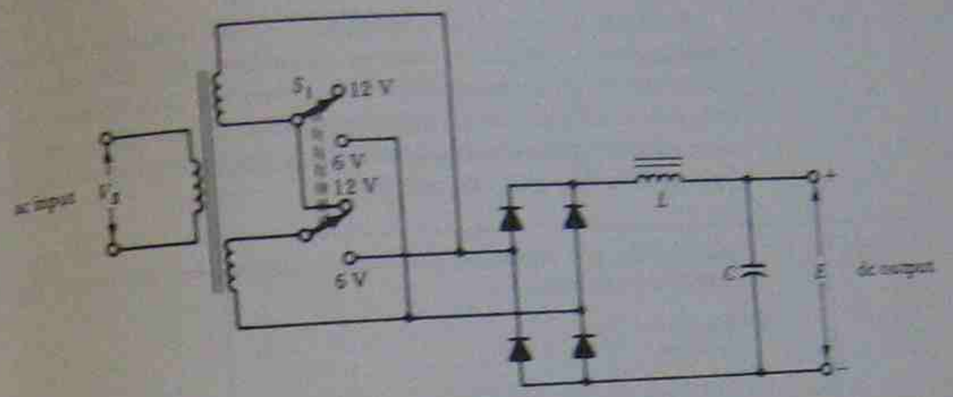


FIGURE 14-3. Circuit of a 12 V/6 V high-current, unregulated dc power supply.

voltage is one parameter used to define the performance of a power supply. Also, the ac input voltage (or line voltage) does not always remain constant. A ±10% variation in line voltage is not unusual. This variation in input is likely to produce some change in output. The *line regulation* of the power supply defines how the dc output voltage is affected by variations in ac input voltage (V_s):

$$\text{Line regulation} = \frac{(\Delta E_s \text{ for 10\% change in } V_s) \times 100\%}{E_s} \quad (14\text{-}7)$$

Another term used to define the effect of input voltage variations upon the power supply output is *source effect*. Once again a specified variation of ac supply voltage is involved (usually ±10%). The actual dc output voltage change that results is then stated as the source effect. Still another term used is *stabilization ratio*, the ratio of percentage variations in dc output voltage and ac input voltage.

The dc output voltage is also affected by load current changes. When the load current increases, the output voltage falls, and when the load current decreases, the output voltage rises. As already explained, the output of a rectifier circuit with capacitor filtering is the peak voltage $E_{s(max)}$ when no load current is flowing [see Figure 14-1(b)]. When load current flows, the output drops to $E_s = E_{av}$. The *load regulation* defines how the dc output voltage is affected by variations in load current:

$$\text{Load regulation} = \frac{(\Delta E_s \text{ for } \Delta I_L = I_{L(max)}) \times 100\%}{E_s} \quad (14\text{-}8)$$

Similar to the case of line regulation, the load regulation of a voltage regulator may be defined in terms of a *load effect*. The load effect is the actual output voltage change that results when the load current changes from zero to full load. Instead of load regulation or load effect, a regulator *output resistance* may be stated: (output voltage change from zero to full load current) divided by (full load current).

EXAMPLE 14-3 Calculate the line regulation and load regulation for the power supply referred to in Example 14-1.

SOLUTION

The circuit in Figure 14-1(a) has no means of reducing the effect of input voltage changes. When V_S changes by 10%, E_o changes by 10%. Therefore,

Line regulation = 10%

When $I_L = 0$,

$$E_o = E_{(max)} = 21 \text{ V}.$$

When $I_L = 100$ mA,

$$E_o = E_{av} = 20 \text{ V},$$

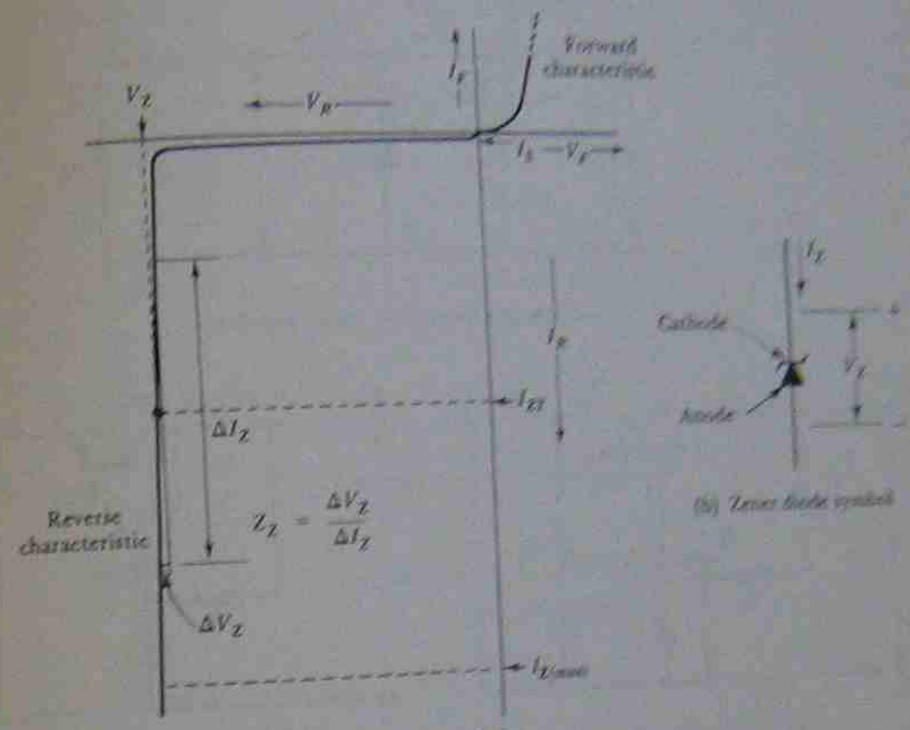
$$\textit{From Equation 14-8, Load regulation} = \frac{(21 \text{ V} - 20 \text{ V}) \times 100\%}{20 \text{ V}}$$

$$= 5\%.$$

14-2 BASIC dc VOLTAGE REGULATORS

Direct current voltage regulators are based upon the use of the *zener diode* (or *breakdown diode*). The zener diode is essentially just a *pn* junction operated in reverse. The characteristics and circuit symbol are illustrated in Figure 14-4. When the diode is reverse biased by a few volts, only a very small reverse current flows. With increased reverse bias a breakdown voltage is eventually reached. As illustrated by the characteristics, the breakdown voltage is a very constant quantity. It is also important to note that when the junction is operating in reverse breakdown its current must be limited by means of a series resistor. Where this is not done, the resultant large current flow may destroy the device.

The most important parameters of the zener diode are: V_z (*breakdown voltage*); I_{zT} (*reverse current* at V_z); and Z_z (*dynamic impedance* of the diode). On the characteristics in Figure 14-4, it is seen that any change in diode



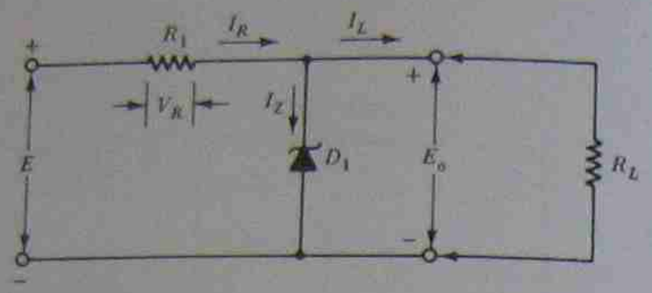
(a) Zener diode characteristics (b) Zener diode symbol

FIGURE 14-4. Characteristics and symbol of Zener diode.

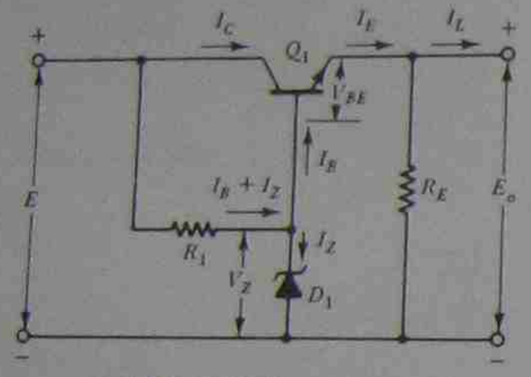
current (ΔI_z) causes a change in diode voltage (ΔV_z). Thus, the diode dynamic impedance represents the relationship between changes in zener diode reverse current and voltage. Z_z can be used to calculate changes that occur in V_z when I_z is altered. The usual zener diode current is $I_{ZT} = 20$ mA, for the type of zener diodes used in voltage regulators. Typical zener voltages available range from a minimum of 2.7 V to a maximum of 12 V, with the most commonly used devices having $V_z = 6$ V to 8 V.

A simple zener diode voltage regulator is illustrated in Figure 14-5(a). The output voltage is $E_o = V_z$, and the maximum load current that can be supplied must allow a minimum zener current $I_{z(min)}$ to flow. A typical maximum zener current is 60 mA for low current devices. (High-current zener diodes are available.) The typical minimum current required to keep the device operational is around 10 mA. Thus the maximum output current that might be taken from such a circuit is

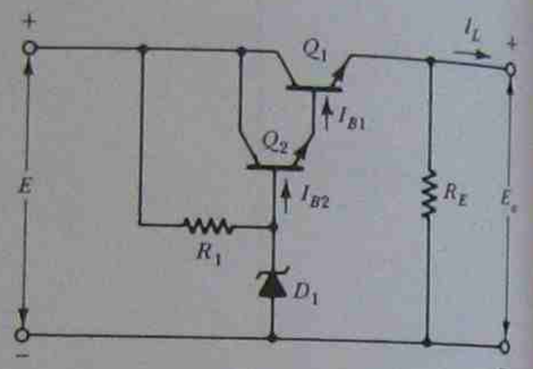
$$I_L = 60 \text{ mA} - 10 \text{ mA} = 50 \text{ mA}.$$



(a) Simple Zener diode voltage regulator



(b) Emitter follower voltage regulator or series regulator



(c) Series regulator with 'Darlington connected' transistors

FIGURE 14-5. Zener diode voltage regulator circuits.

EXAMPLE 14-4 A 12-V zener diode with a dynamic impedance of $Z_z = 7\ \Omega$ is employed in the circuit of Figure 14-5(a). The load resistance is 240 Ω, and the supply voltage is $E = 20$ V. Calculate the value of R_1 and determine the line and load regulation of the circuit. Also calculate the line effect and load effect.

SOLUTION

$$I_L = \frac{E_o}{R_L} = \frac{V_z}{R_L}$$
$$= \frac{12\text{ V}}{240\ \Omega} = 50\text{ mA},$$
$$I_{z(\min)} = 10\text{ mA},$$
$$R_1 = \frac{V_R}{I_R} = \frac{E - V_z}{I_L + I_z}$$
$$= \frac{20\text{ V} - 12\text{ V}}{50\text{ mA} + 10\text{ mA}}$$
$$= 133\ \Omega,$$

$$\Delta E = 10\%\text{ of } E$$
$$= 10\%\text{ of } 20\text{ V}$$
$$= 2\text{ V},$$
$$\Delta I_R = \frac{\Delta E}{R_1} = \frac{2\text{ V}}{133\ \Omega}$$
$$= 15\text{ mA},$$
$$\Delta E_o = \Delta V_z = \Delta I_R Z_z$$
$$= 15\text{ mA} \times 7\ \Omega$$
$$= 105\text{ mV}.$$

From Equation 14-7,

$$\textit{Line regulation} = \frac{105\text{ mV} \times 100\%}{12\text{ V}}$$
$$= 0.9\%,$$
$$\textit{Line effect} = \Delta V_z \quad \text{for } \Delta E \text{ of } 10\%$$
$$= 105\text{ mV}.$$

When $\Delta I_L = 50$ mA,

$$\Delta I_z = 50\text{ mA},$$
$$\Delta E_o = \Delta V_z = \Delta I_z Z_z$$
$$= 50\text{ mA} \times 7\ \Omega$$
$$= 350\text{ mV}.$$

and

From Equation 14-8,

$$\textit{Load regulation} = \frac{350\text{ mV} \times 100\%}{12\text{ V}}$$
$$= 2.9\%,$$
$$\textit{Load effect} = \Delta V_z \quad \text{for } \Delta I_L \text{ of } 50\text{ mA}$$
$$= 350\text{ mV}.$$

The input ripple voltage to the regulator in Figure 14-5(a) is potentially divided by Z_z and R_1 in series. This gives an output ripple V_{ro} which is an attenuated version of the input ripple V_r:

$$V_{ro} = V_r \frac{Z_z}{R_1 + Z_z}. \qquad (14\text{-}9)$$

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For an input ripple of 2 V peak-to-peak, and the R_1 and Z_z values in Example 14-4:

$$V_{r_o} = 2\text{ V} \times \frac{7\ \Omega}{133\ \Omega + 7\ \Omega}$$
$$= 100\text{ mV } \textit{peak-to-peak}.$$

The simple zener diode regulator in Figure 14-5(a) is very wasteful of power, because even when the load current is zero the total of $I_z + I_L$ is drawn from the input. Therefore, this type of circuit is not normally employed to supply load currents around 50 mA. Instead, the same circuit is combined with transistors or an operational amplifier to give a stable output voltage and almost any desired level of load current. The basic circuit combination is shown in Figure 14-5(b) and (c).

In Figure 14-5(b) the transistor functions as an emitter follower (see Section 8-3). The circuit is usually termed a series regulator, and it may be designed to make $I_C = 1$ mA, for example, and $I_z = 20$ mA when no external load current (I_L) is flowing. When maximum load current is demanded, the transistor base current increases. This causes only a very small change in the current through the zener diode.

EXAMPLE 14-5 The regulator circuit in Figure 14-5(b) has $V_z = 12.7$ V, $R_1 = 390\ \Omega$, $R_E = 12$ kΩ, and $R_L = 240\ \Omega$. The supply voltage is $E = 21$ V when $I_L = 0$, and $E = 20$ V when $I_L = 50$ mA. The transistor is silicon and has a current gain of $h_{FE} = 50$. Calculate the zener diode current and the transistor current when the load is disconnected, and when the load is connected.

SOLUTION

With R_L disconnected:

$$V_{RE} = V_z - V_{BE}$$
$$= 12.7\text{ V} - 0.7\text{ V}$$
$$= 12\text{ V},$$
$$I_E = \frac{E_o}{R_E} = \frac{12\text{ V}}{12\text{ k}\Omega}$$
$$= 1\text{ mA},$$
$$I_B \simeq \frac{I_E}{h_{FE}} = \frac{1\text{ mA}}{50}$$
$$= 20\ \mu\text{A},$$
$$V_{R1} = E - V_z$$
$$= 21\text{ V} - 12.7\text{ V}$$
$$= 8.3\text{ V},$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{8.3\text{ V}}{390\ \Omega}$$
$$= 21.3\text{ mA},$$

or

$$I_{R1} = I_z + I_B,$$
$$I_z = I_{R1} - I_B$$
$$= 21.3\text{ mA} - 20\ \mu\text{A}$$
$$\simeq 21.3\text{ mA}.$$

With R_L connected:

$$I_E = \frac{E_o}{R_E} + \frac{E_o}{R_L}$$
$$= \frac{12\text{ V}}{12\text{ k}\Omega} + \frac{12\text{ V}}{240\ \Omega}$$
$$= 51\text{ mA},$$
$$I_B \simeq \frac{I_E}{h_{FE}} = \frac{51\text{ mA}}{50}$$
$$= 1.02\text{ mA},$$
$$I_{R1} = \frac{20\text{ V} - 12.7\text{ V}}{390\ \Omega}$$
$$= 18.7\text{ mA},$$
$$I_z = I_{R1} - I_B$$
$$= 18.7\text{ mA} - 1.02\text{ mA}$$
$$= 17.7\text{ mA}.$$

EXAMPLE 14-6 Determine the line and load regulation for the regulator circuit in Example 14-5. Assume that $Z_z = 7\ \Omega$.

SOLUTION

$$\Delta E = 10\%\text{ of } E$$
$$= 2\text{ V},$$
$$\Delta I_{R1} = \frac{\Delta E}{R_1} = \frac{2\text{ V}}{390\ \Omega}$$
$$= 5.1\text{ mA},$$
$$\Delta E_o = \Delta V_z = \Delta I_{R1} Z_z$$
$$= 5.1\text{ mA} \times 7\ \Omega$$
$$= 36\text{ mV}.$$

From Equation 14-7,

$$\text{Line regulation} = \frac{36\text{ mV} \times 100\%}{12\text{ V}}$$
$$= 0.3\%.$$

When $I_L = 0$, $I_z = 21.3$ mA. When $I_L = 50$ mA, $I_z = 17.7$ mA, and for ΔI_L of 50 mA,

$$\Delta I_z = 21.3 - 17.7\text{ mA}$$
$$= 3.6\text{ mA},$$
$$\Delta E_o = \Delta V_z = \Delta I_z \times Z_z \quad \text{(ignoring any change in } V_{BE})$$
$$= 3.6\text{ mA} \times 7\ \Omega$$
$$= 25.2\text{ mV}.$$

From Equation 14-8,

$$\text{Load regulation} = \frac{25.2\text{ mV} \times 100\%}{12\text{ V}}$$
$$= 0.21\%.$$

Comparing Examples 14-4 and 14-6, it is seen that the addition of the transistor to the zener diode regulator circuit results in improved line regulation and substantially improved load regulation.

In Figure 14-5(c) an additional transistor (Q_2) is connected into the circuit to supply base current to Q_1. The arrangement is known as a *Darlington pair*, and it is necessary where high load currents are to be supplied. The current relationships are

$$I_{B1} = \frac{I_L}{h_{FE1}} \quad \text{and} \quad I_{B2} = \frac{I_{B1}}{h_{FE2}},$$

or

$$\boxed{I_{B2} = \frac{I_L}{h_{FE1}h_{FE2}}}. \tag{14-10}$$

If, for example, $I_L = 500$ mA and $h_{FE} = 20$, then,

$$I_{B1} = \frac{500\text{ mA}}{20} = 25\text{ mA},$$

and this would have to be supplied from the zener diode circuit in the case of Figure 14-5(b). When two transistors are involved, with $h_{FE1} = 20$ and $h_{FE2} = 50$: From Equation 14-10,

$$I_{B1} = \frac{500\text{ mA}}{20 \times 50} = 0.5\text{ mA}.$$

This can very easily be supplied from the zener diode circuit, and it will have only a slight effect upon V_z when the output current changes from zero to 500 mA.

14-3 OPERATIONAL AMPLIFIER REGULATORS AND IC VOLTAGE REGULATORS

If the emitter follower regulator circuit in Figure 14-5(b) has an operational amplifier introduced into it as a *voltage follower* (see Section 8-6-2), as in Figure 14-6(a), the regulator performance is further improved. Note that in Figure 14-6(a) the noninverting terminal of the op-amp is connected to the zener diode, and the inverting terminal is connected to the regulator output or transistor emitter. Because the op-amp inverting terminal voltage remains closely equal to the noninverting terminal voltage, E_o will always be within a few microvolts of V_z. Thus, so long as V_z remains stable the regulator output voltage remains stable.

The zener diode voltage V_z is, of course, affected by variations in supply voltage E. These variations are due to ac line voltage changes and load current changes. As with other zener diode regulators, the line and load regulations are determined by calculating the effect of ΔI_L and ΔE upon the zener voltage V_z.

EXAMPLE 14-7 The voltage regulator circuit in Figure 14-6(a) has a supply voltage of $E = 21$ V at no load. This falls to $E = 20$ V at full load current of 50 mA. $R_1 = 390\ \Omega$, $V_z = 12$ V, and $Z_z = 7\ \Omega$. Calculate the line and load regulation of the circuit.

SOLUTION

$$\Delta E = 10\%\text{ of } E$$
$$= 2\text{ V},$$
$$\Delta I_z = \Delta I_{R1} = \frac{\Delta E}{R_1} = \frac{2\text{ V}}{390\ \Omega}$$
$$= 5.1\text{ mA},$$
$$\Delta E_o = \Delta V_z = 5.1\text{ mA} \times 7\ \Omega$$
$$= 36\text{ mV}.$$

From Equation 14-7,

$$\textit{Line regulation} = \frac{36\text{ mV} \times 100\%}{12\text{ V}}$$
$$= 0.3\%,$$
$$\textit{Zener current, } I_z = \frac{E - V_z}{R_1},$$

When $I_L = 0$,

$$I_z = \frac{21\text{ V} - 12\text{ V}}{390\ \Omega}$$
$$= 23.1\text{ mA}.$$

When $I_L = 50$ mA,

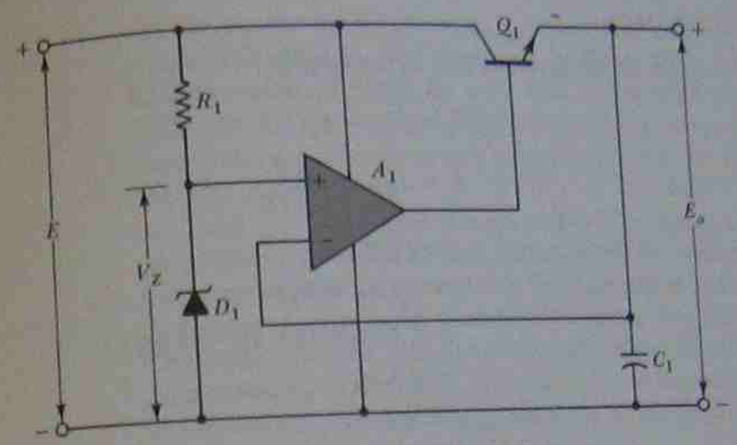
$$I_z = \frac{20\text{ V} - 12\text{ V}}{390\ \Omega}$$
$$= 20.5\text{ mA},$$
$$\Delta I_z = 23.1\text{ mA} - 20.5\text{ mA}$$
$$= 2.6\text{ mA},$$
$$\Delta E_o = \Delta V_z = \Delta I_z \times Z_z$$
$$= 2.6\text{ mA} \times 7\ \Omega$$
$$= 18.2\text{ mV}.$$

From Equation 14-8,

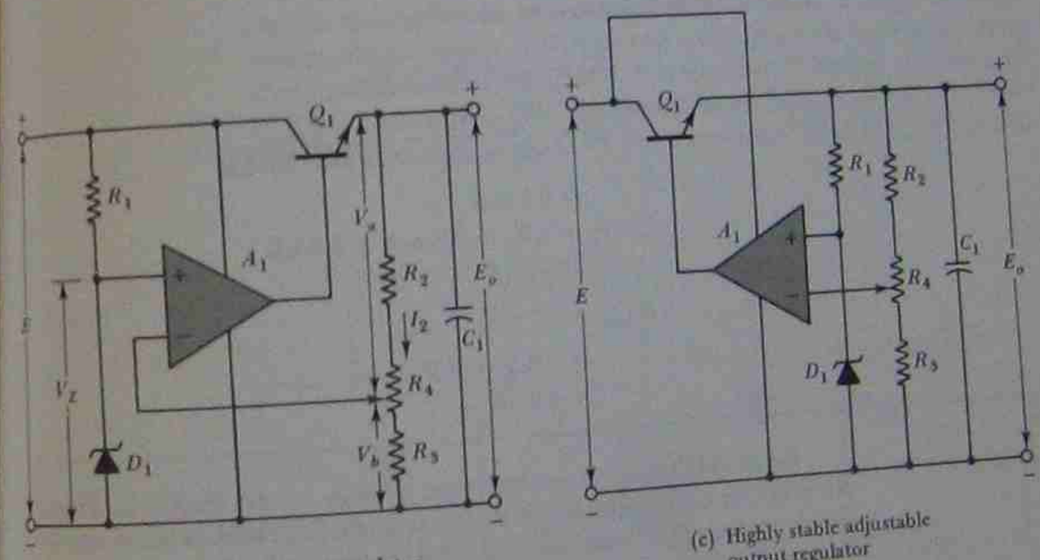
$$\textit{Load regulation} = \frac{18.2\text{ mV} \times 100\%}{12\text{ V}}.$$
$$= 0.15\%.$$

Comparing the results of Example 14-7 to the line and load regulation of the emitter follower regulator (as determined in Example 14-6), it is seen that the voltage follower circuit has no effect upon the line regulation, and that it produces only a slight improvement in the load regulation.

The circuit in Figure 14-6(b) uses the operational amplifier to produce an adjustable output voltage (E_o) which is greater than the zener voltage. This is something that cannot be achieved by an emitter follower regulator operating without an amplifier. Once again, the voltage at the inverting input of the op-amp remains equal to the voltage at the noninverting input



(a) Voltage follower regulator



(b) Adjustable output regulator

(c) Highly stable adjustable output regulator

FIGURE 14-6. dc voltage regulators using IC operational amplifiers.

(i.e., V_z). Thus, $V_b = V_z$ and $E_o = V_a + V_b$. The relationship between V_a and V_b is demonstrated by the following example.

EXAMPLE 14-8 Determine the maximum and minimum output voltage available from the regulator circuit in Figure 14-6(b), when $V_z = 6$ V, $R_2 = 5.6$ kΩ, $R_4 = 3$ kΩ, and $R_3 = 5.6$ kΩ.

SOLUTION

When the moving contact is at the bottom of R_4:

$$V_b = V_{R3} = V_z,$$

and

$$I_2 = \frac{V_{R3}}{R_3} = \frac{6\text{ V}}{5.6\text{ k}\Omega}$$
$$= 1.07\text{ mA},$$
$$V_a = I_2(R_2 + R_4)$$
$$= 1.07\text{ mA}\,(5.6\text{ k}\Omega + 3\text{ k}\Omega)$$
$$= 9.2\text{ V},$$
$$E_{o(\max)} = V_a + V_b$$
$$= 6\text{ V} + 9.2\text{ V}$$
$$= 15.2\text{ V}.$$

When the moving contact is at the top of R_4:

$$V_b = V_{R4} + V_{R3} = V_z,$$

and

$$I_2 = \frac{V_{R4} + V_{R3}}{R_4 + R_3} = \frac{6\text{ V}}{3\text{ k}\Omega + 5.6\text{ k}\Omega}$$
$$= 0.7\text{ mA},$$
$$V_a = I_2R_2 = 0.7\text{ mA} \times 5.6\text{ k}\Omega$$
$$= 3.9\text{ V},$$
$$E_{o(\min)} = V_a + V_b$$
$$= 3.9\text{ V} + 6\text{ V}$$
$$= 9.9\text{ V}.$$

Figure 14-6(c) shows an improved version of the circuit in Figure 14-6(b). The only change is that the zener diode (D_1) and its series resistor (R_1) are supplied from the regulated output voltage instead of the unregulated input. Now input voltage variations (due to changes in supply voltage or changes in load current) have almost no effect upon the zener diode voltage.

Capacitor C_1 shown in all three circuits in Figure 14-6 is usually on the order of 30 μF to 100 μF. C_1 shorts out high-frequency oscillations that can occur in a regulator which uses a high gain amplifier. It also acts as a reservoir capacitor to supply very fast load current demands during the regulator circuit response time.

Power supplies used in laboratories are subject to overloads and short-circuits that can occur in experimental circuitry. Short-circuit protec-

tion, or current-limiting circuits, are absolutely necessary in this circumstance. Transistor Q_2 and resistor R_5 in Figure 14-7 constitute a current-limiting circuit. Resistor R_6 must also be included because, as will be explained, the base voltage of Q_1 must be pulled down, and this cannot be done when Q_1 base is directly connected to the low impedance output terminal of the op-amp.

Load current I_L flows through resistor R_5, causing a voltage drop with the polarity shown. For normal current levels the voltage drop across R_5 is not large enough to forward bias the base-emitter junction of Q_2. However, when I_L reaches its maximum (designed for) level Q_2 is biased on. This causes current I_6 to flow through resistor R_6, producing a voltage drop across R_6 as shown. Q_2 is actually driven into saturation. So the base of transistor Q_1 is *pulled down* to the level of the negative supply terminal, causing the output voltage to go to zero.

The output terminals of the regulator can actually be short-circuited, and the short-circuit current is limited to the maximum level for which the current-limiting circuit is designed. Figure 14-8(a) is a graph of output voltage plotted against load current for a regulator with the type of current limiting illustrated in Figure 14-7. It is seen that E_o remains constant until $I_{L(\max)}$ is approached. Then the output voltage falls rapidly to zero, while the output current remains at the short-circuit level ($I_{L(SC)}$). In this

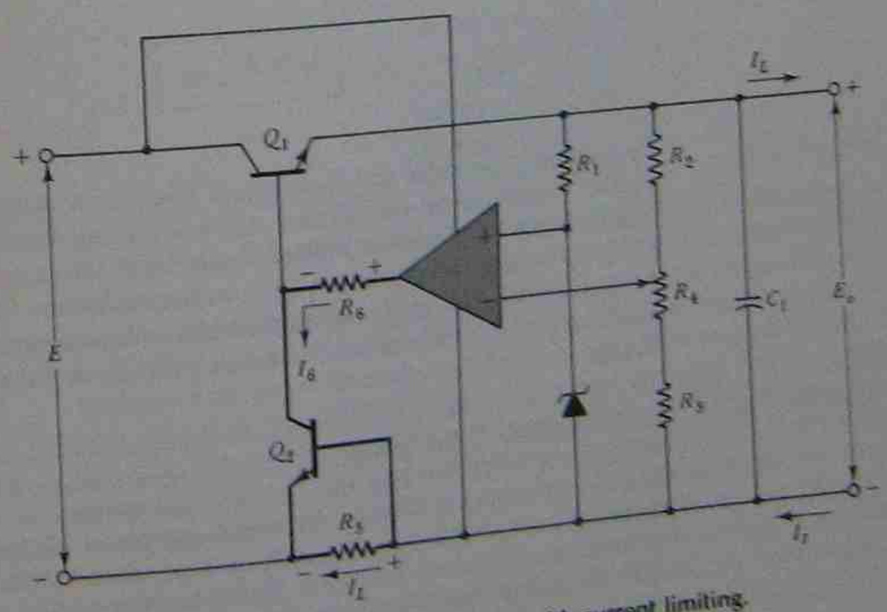
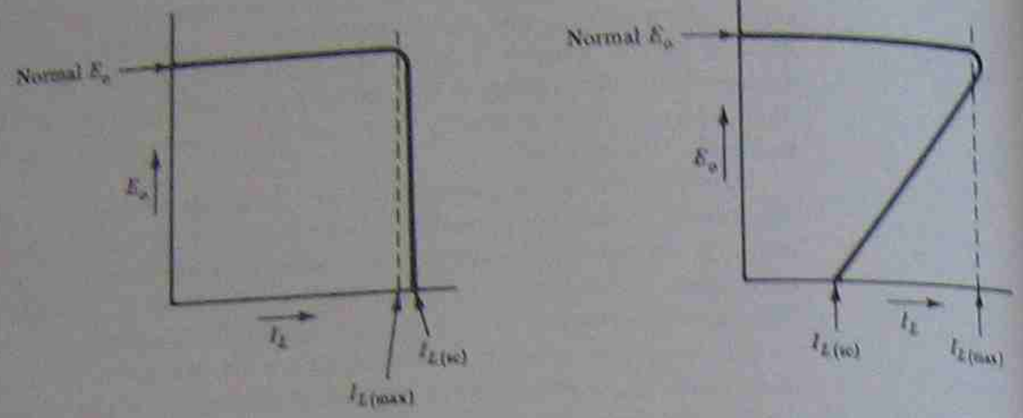


FIGURE 14-7. Regulator with current limiting.



(a) Characteristic of ordinary current-limiting circuit

(b) Characteristic of fold-back current-limiting circuit

FIGURE 14-8. Characteristics of current limiting circuits used with dc voltage regulators.

condition, the power dissipation in the series transistor (Q_1) is

$$P_D = EI_{L(SC)}. \tag{14-11}$$

To minimize the series transistor power dissipation during short-circuit, another slightly more complicated current-limiting circuit is employed. This gives the regulator the *fold-back* short-circuit characteristic illustrated in Figure 14-8(b). In this case $I_{L(SC)}$ is substantially less than $I_{L(max)}$, and the power dissipation in Q_1 during short-circuit is substantially reduced. A regulator with this short-circuit characteristic is said to have *fold-back current limiting*.

EXAMPLE 14-9 In the regulator circuit in Figure 14-7, the input voltage is $E = 20$ V, the output is $E_o = 12$ V, and the normal load current is 250 mA. The short-circuit current is 300 mA. Determine the power dissipated in Q_1: (a) under normal operating conditions, (b) at short-circuit if the current-limiting circuit has the characteristics in Figure 14-8(a), and (c) at short-circuit when the current-limiting circuit characteristics are as in Figure 14-8(b) with $I_{L(SC)} = I_{L(max)}/3$.

SOLUTION

Under normal operating conditions:

$$\begin{aligned} V_{CE1} &= E - E_o \\ &= 20\text{ V} - 12\text{ V} \\ &= 8\text{ V}, \\ P_{D1} &= I_{L(max)} \times V_{CE1} \\ &= 250\text{ mA} \times 8\text{ V} \\ &= 2\text{ W}. \end{aligned}$$

At short-circuit [Figure 14-8(a)]:

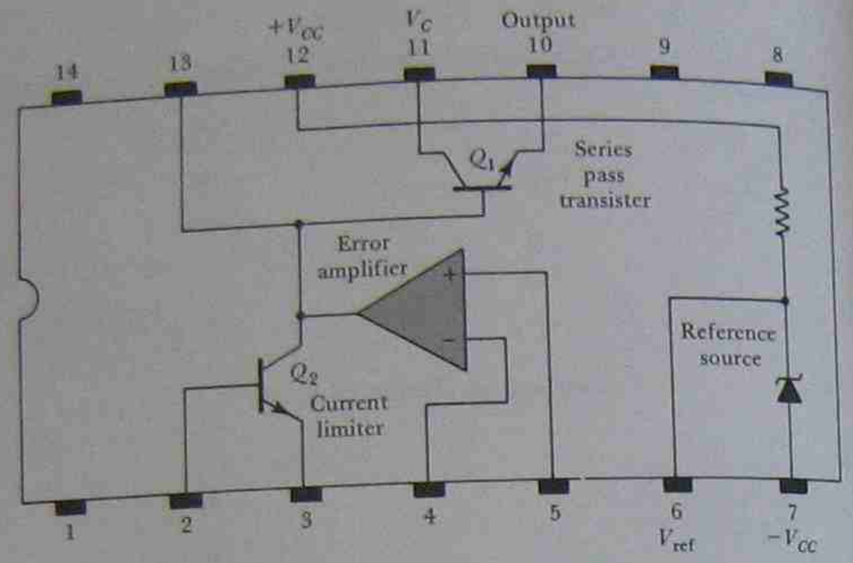
$$\begin{aligned} V_{CE1} &= E - 0 \\ &= 20\text{ V}, \\ P_{D1} &= I_{L(SC)} \times V_{CE1} \\ &= 300\text{ mA} \times 20\text{ V} \\ &= 6\text{ W}. \end{aligned}$$

At short-circuit [Figure 14-8(b)]:

$$\begin{aligned} I_{L(SC)} &= I_{L(max)}/3, \\ &= 300\text{ mA}/3 \\ &= 100\text{ mA}, \\ P_{D1} &= I_{L(SC)} \times V_{CE1} \\ &= 100\text{ mA} \times 20\text{ V} \\ &= 2\text{ W}. \end{aligned}$$

Example 14-9 demonstrates that considerable power is dissipated in series transistor Q_1 under normal operating conditions. When the regulator output terminals are short-circuited, there is much more power dissipated in Q_1 than normal, unless a fold-back current-limiting circuit is employed. Because of the power dissipation, transistor Q_1 must always be fitted with a heat sink. This is usually mounted at the rear of the power supply chassis.

The circuit of a typical *integrated circuit voltage regulator* is illustrated in Figure 14-9. The IC has a reference source, an error amplifier, a series pass transistor, and a current-limiting transistor, all contained in one small package. The series pass transistor is capable of dissipating only relatively small quantities of power, because it is not fitted with a heat sink. Therefore, the IC regulator circuit cannot directly supply high levels of load current. An additional series pass transistor with a heat sink can be



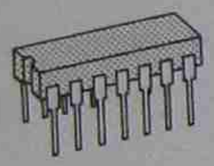


FIGURE 14-9. Basic circuit arrangement of 723 IC voltage regulator and dual-in-line package.

connected in Darlington arrangement with Q_1, to handle any level of load current.

Figure 14-10 shows the circuit of a positive voltage regulator using a 723 IC regulator. The arrangement of components is very similar to the regulator circuit in Figure 14-6(b). One difference between the two circuits is that a 100-pF capacitor C_1 in Figure 14-10 is connected between the error amplifier output and inverting input terminals. This is used instead of the large output capacitor (C_1) in Figure 14-7 to prevent the circuit from oscillating. (Sometimes both capacitors may be required.) The 723 regulator typically operates with input voltages ranging from 9.5 V to 40 V. By suitable selection of R_1 and R_2, the circuit shown in Figure 14-10 can provide a dc output voltage from 7 V to 37 V. Maximum output current is 150 mA, with larger currents handled by an additional transistor. The 723 regulator can also be connected to operate as a negative voltage regulator, or as a *switching regulator* (see Section 14-6).

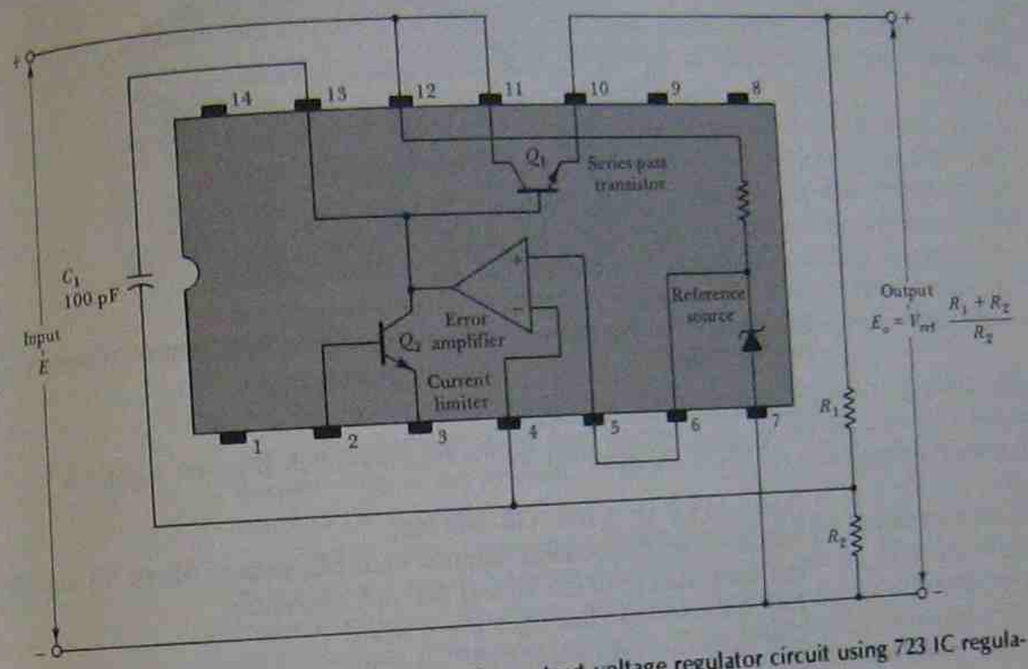


FIGURE 14-10. Positive output voltage regulator circuit using 723 IC regulator.

14-4 dc POWER SUPPLY PERFORMANCE AND USE

Laboratory type dc power supplies for use with solid state circuitry typically have an output voltage range of 0 to 25 V, or 0 to 50 V. Normally, neither terminal of the output is permanently grounded, so the supply is said to be floating. Dual output power supplies are available to provide the commonly required positive and negative ($\pm$V) supply. Multi-output power supplies are also available. For example, one unit provides (0–6 V) and 2.5 A or $\pm$(0–20 V) and 0.5 A. This is convenient for use with combinations of logic and linear circuits.

A typical dual-output power supply (the Harrison 6205 B) is shown in Figure 14-11. The unit has six output terminals: two pairs of $\pm$ terminals and two ground terminals. The two output voltages can be used independently, or they can be connected to operate in series or in parallel. Any terminal of each output pair can be grounded to produce a positive output, a negative output, or $\pm$ outputs. Each of the two outputs has coarse and fine voltage control knobs, a voltmeter/ammeter, and a range selection switch for the meter. Each meter can be set to monitor output voltage or output current on one of several ranges. An ac supply *on / off* switch is also



FIGURE 14-11. Power supply with two independent outputs (Courtesy of Hewlett-Packard).

included on the front panel.

A partial specification for the Harrison 6205 B power supply is:

- *Input*—115 V ac ±10%, (48–440 Hz)
- *Outputs*—Two independent outputs: each can deliver (0–40 V) and 300 mA maximum, or (0–20 V) and 600 mA maximum.
- *Line regulation*—less than (0.01% + 4 mV)
- *Load regulation*—less than (0.01% + 4 mV)
- *Ripple and noise*—less than (200 μV rms, 1 mV peak-to-peak)

Ripple and noise is sometimes listed under the term PARD on a power supply specification. This comes from *periodic and random deviation*, but it simply means ripple and noise voltage.

Other items that occur on a power supply specification are:

- *Voltage resolution*—the smallest change in output voltage then can be produced when adjusting the fine voltage control knob.
- *Current resolution*—applies to a constant current supply, similar to voltage resolution.
- *Transient recovery time*—time for output voltage to return to within 10 mV of its normal level after a specified load current change has suddenly occurred.
- *Internal impedance*—output impedance offered to sinusoidal changes in load current over a specified frequency range.
- *Stability or Drift*—The maximum output voltage change (or current change) during an eight-hour period after a thirty-minute warm-up time.
- *Temperature coefficient*—Output change per degree Celsius change in ambient temperature.

The type of power supply illustrated in Figure 14-11 is normally operated with one positive terminal and one negative terminal grounded, to provide plus-and-minus output voltages. In this condition each voltage is

set to the desired constant output level, and each output has an internally set current limit. Some units have adjustable current limit controls on the front panel, and some have terminals at the rear of the chassis for connecting resistors to alter the current limit.

The two output voltages can also be operated in series to provide higher voltages. Similarly, two or more power supply units can have their output terminals series connected to produce almost any desired voltage level. None of the units involved in a series-connected arrangement should have an internal ground. Also all units must be capable of supplying the required level of load current. *This practice should not be followed where very high voltages are required.* Instead a power supply designed for a high voltage output should be used.

Parallel operation of power supplies is possible, where a single unit cannot supply a required load current. This should be done only where current controls are available to ensure that each unit supplies its correct share of the current.

Two or more power supplies may be connected for *tracking operation*. In this case one supply becomes a *master* and the others are *slaves*. When the output voltage of the master increases or decreases, the other outputs vary in proportion. This kind of operation is achieved by using the output of the master supply (or a portion of it) in place of the internal (zener diode) reference sources in each of the other units.

The normal procedure for using a dc power supply with a single output voltage is listed below. With multioutput units, the procedure is repeated for each output:

1. With the output terminals open-circuited, switch *on* the ac input and adjust the output voltage to the desired level.
2. Where the unit has a front panel current control: (a) Set the control for maximum current if there is no concern about passing too much current through the circuit to be supplied. (b) When the current is to be limited to a particular level, short-circuit the output terminals and adjust the current to the desired level.
3. Open-circuit the output terminals (if previously shorted), and set the meter to indicate output voltage.
4. Switch *off* the ac input, and connect the circuit to be supplied.
5. Switch *on* the ac input and observe (on the meter) that the output voltage remains at the selected level. If the voltage has fallen below the previously set level, the circuit is drawing excessive current.

14-5 POWER SUPPLY TESTING

To measure the line regulation of a power supply, the output voltage must be carefully monitored while the input is varied by ±10%. Similarly, to measure the load regulation, the power supply output must be monitored

while the load is connected and disconnected. The only problem when both of these measurements is that the output changes are very small, in the order of millivolts. A voltmeter connected to measure a 12 V output, for example, might be on a 15 V range. Clearly, a change of 10 or 20 mV cannot be measured on this range. To measure these small voltage changes null methods must be employed.

A means for measuring line and load regulation is shown in Figure 14-13. To facilitate an input adjustment, the power supply to be tested (PS_1) is connected to the ac line via a variable voltage transformer. An ac voltmeter (V_1) monitors the ac supply voltage. A dc voltmeter (V_2) is connected directly across the output terminals of PS_1, so that the dc output can be set to the desired level. An adjustable load resistor (R_L) in series with an ammeter (A_1) can be switched on or off at the output of PS_1 by switch S_1. Null meter V_3 is connected between the positive terminal of PS_1 and the positive terminal of a reference power supply (PS_2). The negative terminal of PS_2 is connected directly to the negative terminal of PS_1. Note that the load current (I_L) does not flow through the null meter, nor through any of the cables connecting PS_1, PS_2, and the null meter.

Any good quality multirange voltmeter can be used as a null meter, as long as it has a range of 100 mV or more. The null meter is connected to indicate the difference between the output voltages of PS_1 and PS_2. It will also measure changes in the output of PS_1, and when on its lowest range it will measure very small changes in PS_1 output. For example, if $E_{PS_1} = 12$ V and PS_2 is adjusted to make $E_{PS_2} = E_{PS_1}$, V_3 indicates zero. V_3 can now be set to its most sensitive range to indicate very small differences in E_{PS_1} and E_{PS_2}. Initially, V_3 should be set to its highest range to avoid damage due to large differences between E_{PS_1} and E_{PS_2}.

The procedure for using the system in Figure 14-13 to measure line and load regulation is:

1. Connect the ac supply to PS_1 and adjust it to 115 V, as indicated on V_1.
2. With S_1 open, switch on PS_1 and adjust E_{PS_1} to the desired level as indicated on V_2.
3. Connect the ac supply to PS_2, switch on and adjust E_{PS_2} until V_3 indicates zero.
4. Progressively set V_3 through lower ranges, adjusting E_{PS_2} for null at each stage until the null meter indicates zero on its most sensitive range.
5. Adjust the ac input to PS_1 by ±10% and note its output voltage change as indicated on V_2.
6. Calculate the percentage change in E_{PS_1} to determine the line regulation of PS_1.



7. Return the ac input to PS_1 to its normal level and adjust E_{o2} as necessary to indicate zero on V_3.
8. Close switch S_1 and adjust R_L to give the desired level of I_L.
9. Open and close S_1 and note the change in E_{o1} as indicated on V_3.
10. Calculate the percentage change in E_{o1} to determine the load regulation of PS_1.

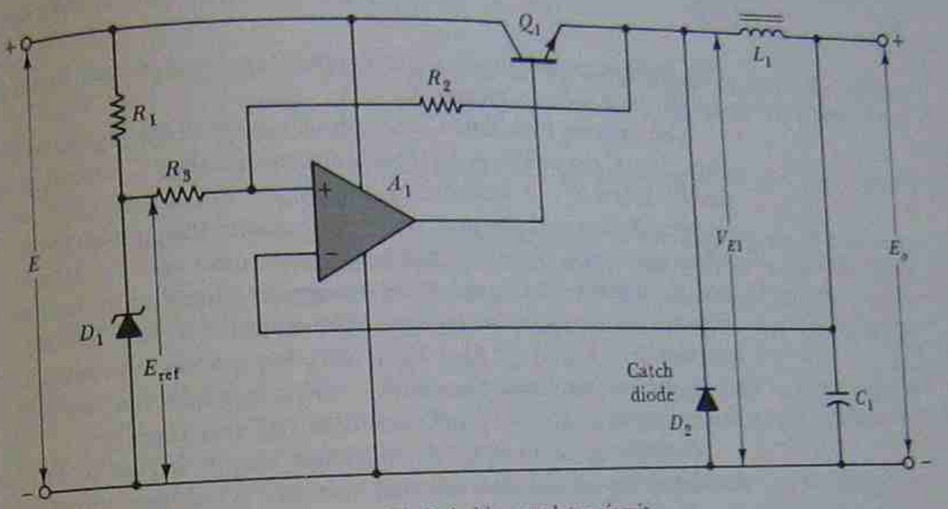
14-6 SWITCHING REGULATORS

The power dissipated in the series pass transistor of a series regulator is wasted power. When a high level of load current is supplied, the wasted power seriously reduces the efficiency of the power supply and can also present a heat dissipation problem. These deficiencies are overcome in switching regulators.

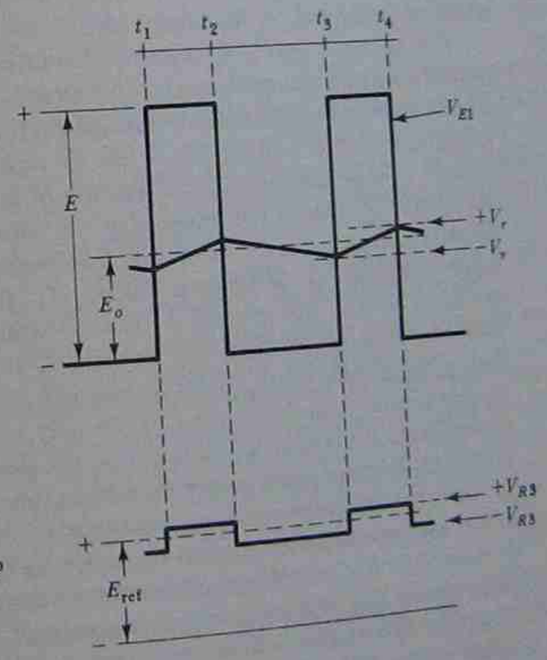
A switching regulator circuit is shown in Figure 14-13(a). As will be explained, the voltage at the emitter of Q_1 has the pulse waveform (V_{E1}), illustrated in Figure 14-13(b). The choke and capacitor smooth out the pulse wave and present the output as its average value. The output (E_o) is not completely smooth, of course, but has a ripple content ($\pm V_r$) with a waveform approximately as illustrated. The most important difference between a series regulator and a switching regulator is that in the switching regulator the series pass transistor is either *on* in saturation or *off*. With Q_1 *on*, its power dissipation is $V_{CE(sat)}I_L$. Since $V_{CE(sat)}$ is very small, the power dissipated in Q_1 is also very small. When Q_1 is *off*, its power dissipation is EI_{Co}, where I_{Co} is the collector leakage current. I_{Co} is very small, and consequently the power dissipated in Q_1 is once again a very small quantity. With Q_1 either *on* or *off*, the efficiency of the regulator is much better than a similar series regulator, and the heat dissipation problem is almost nonexistent.

To understand how the switching regulator in Figure 14-13 operates, first assume that R_2 is removed from the circuit. In this situation, op-amp A_1 behaves as a voltage follower, and the circuit functions as a series regulator. The voltage (E_o) is then equal to the zener diode voltage (E_{ref}).

Now, with R_2 in the circuit assume that Q_1 is in saturation, at time t_1 in Figure 14-13(b). The voltage at the emitter of Q_1 is approximately equal to the input voltage (E). The difference between E and E_{ref} is potentially divided across R_2 and R_3, to put the op-amp noninverting input at a slightly higher voltage than E_{ref}. Referring to the waveforms in Figure 14-13(c), the noninverting input at time t_1 is $E_{ref} + V_{R_3}$. Also note (from the waveforms) that at time t_1 the output voltage, which is applied to the op-amp inverting input, is $E_o - V_r$. E_o is equal to E_{ref} and, therefore, $E_o - V_r$ is less than $E_{ref} + V_{R_3}$. Thus, the input voltage to the op-amp noninverting terminal is higher than the input to the inverting terminal. Consequently, the output of A_1 is saturated in a positive direction. This



(a) Switching regulator circuit



(b) Q_1 emitter voltage and output ripple voltage

(c) Voltage at op-amp noninverting input terminal

FIGURE 14-13. Switching regulator and waveforms.

high positive output drives Q_1 into saturation, and makes V_{E1} approximately equal to input voltage E.

Commencing from time t_1, the output voltage of the regulator is rising from $E_o - V_r$ towards $E_o + V_r$. This is due to capacitor C_1 charging via Q_1 and L_1. When $E_o + V_r$ becomes equal to $E_{ref} + V_{R3}$ at time t_2, the op-amp inverting input equals the noninverting input, and the op-amp output falls. When this occurs, Q_1 is switched out of saturation and V_{E1} falls towards zero. V_{R3} is now reduced, and so the noninverting input to the op-amp falls below the level of the inverting input. The output of A_1 now falls rapidly to zero and Q_1 is biased *off*. Also, V_{E1} is zero, V_{R3} is a negative quantity, and the op-amp noninverting input is $E_{ref} - V_{R3}$. It is seen that when $E_o + V_r$ becomes equal to $E_{ref} + V_{R3}$, Q_1 is switched *off* very rapidly.

With Q_1 *off* at time t_2, the regulator output begins to fall as C_1 discharges due to the flow of load current. When the output falls to $E_o - V_r$, this voltage (at the op-amp inverting terminal) becomes less than $E_{ref} - V_{R3}$ (at the op-amp noninverting terminal). A_1 output now rapidly goes positive once again, switching Q_1 *on* and changing the op-amp inverting input to $E_{ref} + V_{R3}$ once more.

During the *on* time of Q_1, current flows through L_1 to charge C_1. The current flow in L_1 causes energy to be stored in the inductor. When Q_1 attempts to switch *off* the current through L_1, the stored energy generates a voltage across L_1 ($-$ on the left, $+$ on the right), which tends to keep the inductor current flowing. This voltage would be very large, and would in fact destroy Q_1 but for the presence of the *catch diode*. When the inductor terminal voltage at the left-hand side falls below the level of the negative supply terminal, D_2 is forward biased. D_2 now becomes a path for continued current flow through L_1 (to C_1) while Q_1 is *off*. When a high load current is drawn from the output, C_1 tends to discharge quickly during the *off* time of Q_1. In this situation the *on* time of Q_1 tends to become greater than the *off* time. When only a very light load current is demanded at the output, C_1 discharges quite slowly. Consequently, the *off* time of Q_1 becomes much longer than its *on* time.

It is seen that the switching regulator is very efficient, because the series pass transistor is either *on* in saturation or *off*. The dc output voltage E_o is equal to E_{ref}, but the ripple content of the output ($\pm V_r$) is substantially greater than the maximum ripple voltage at the output of a series regulator. The typical output ripple on a 5-V, 10-A switching power supply is 50 to 100 mV peak-to-peak. Where the ripple amplitude does not affect the circuits or equipment supplied, the switching regulator makes a very efficient power supply.

REVIEW QUESTIONS AND PROBLEMS

14-1. Sketch the circuit of an unregulated dc power supply using a bridge rectifier. Sketch the output waveforms, and explain the operation of the circuit.

14-2. Show how a choke should be employed to improve the performance of an unregulated power supply. Explain the effect of the choke.

14-3. Write equations for power supply line regulation and load regulation. Explain.

14-4. An unregulated dc power supply, as shown in Figure 14-1(a), is to provide an average output of 15 V with a 10% maximum ripple voltage. The load current is 150 mA maximum, and the supply frequency is 60 Hz. Determine the required reservior capacitor size.

14-5. Calculate the transformer output voltage and current for the circuit in Question 14-4. Also specify the peak reverse voltage and peak repetitive current for the recifiers.

14-6. Calculate the line and load regulation for the power supply in Question 14-4.

14-7. Sketch the circuit symbol and the characteristics of a zener diode. Identify the most important parameters of the device.

14-8. Sketch the circuit of a simple zener diode voltage regulator. Explain its operation.

14-9. A zener diode regulator circuit as in Figure 14-5(a) uses a 9-V zener diode with a dynamic impedance of 5 Ω. The load resistance on the circuit output is 300 Ω, and the supply voltage is 18 V. Calculate the value of the required series resistor R_1. Also determine line regulation, load regulation, line effect, and load effect for the regulator.

14-10. The regulator in Question 14-9 has an input ripple of 1.5 V peak to peak. Calculate the output ripple voltage.

14-11. Sketch the circuit of an emitter follower voltage regulator or series regulator. Explain the operation of the circuit, and discuss the effect of the transistor on the regulator's performance.

14-12. A series regulator circuit, as shown in Figure 14-5(b), has $V_z = 9$ V, $R_1 = 470$ Ω, $R_E = 8.2$ kΩ, $R_L = 300$ Ω. The supply voltage is $E = 19$ V when $I_L = 0$, and $E = 18$ V when $I_L = 32$ mA, and the transistor has $h_{FE} = 60$. Calculate the transistor emitter current and the zener diode current when the load is connected and when the load is disconnected.

14-13. Calculate the line and load regulation for the regulator in Question 14-12. Also determine the line effect and load effect.

14-14. Sketch the circuit of a series regulator using a Darlington pair. Explain the operation of the circuit, and discuss the effect of the additional transistor.

14-15. Sketch the circuit of an IC op-amp voltage follower regulator. Explain its operation, and discuss the effect of the amplifier upon the performance of the regulator.

14-16. A voltage follower regulator, as shown in Figure 14-6(a), has $R_1 = 470$ Ω, $V_z = 9$ V, ad $Z_z = 5$ Ω. The supply voltage is 19 V

when $I_L = 0$ and 18 V when $I_L = 10$ mA. Calculate the line and load regulation for the circuit. Also determine the line effect and load effect.

14-17. Show how a voltage follower regulator can be modified to produce an adjustable output voltage greater than the zener diode voltage. Show a further modification to improve the performance of the circuit. Explain.

14-18. The circuit in Figure 14-6(b) has $V_z = 7$ V, $R_1 = 2.5$ kΩ, $R_2 = 1.5$ kΩ, and $R_3 = 500$ Ω. Calculate the maximum and minimum output voltages that can be obtained.

14-19. Show how the circuit in Question 14-17 should be modified to include current limiting. Explain the operation of the current limiting circuit.

14-20. Discuss the effect of current limiting on the series transistor of a regulator. Sketch the E_o/I_L characteristics of an ordinary current limiter circuit. Also sketch the characteristics of a fold-back current limiter circuit, and discuss the effects of fold-back current limiting on the series transistor.

14-21. The regulator circuit in Figure 14-7 has an input voltage of $E = 18$ V and an output of $E_o = 10$ V. The normal load current is 200 mA, and the short-circuit current is 180 mA.

(a) Determine the power dissipated in Q_1 under normal and short-circuit conditions.

(b) Determine the power dissipated in Q_1 at short-circuit when fold-back current limiting is used with $I_{L(max)} = I_L/kI_{L(max)}$.

14-22. Sketch the basic circuit of a 723-IC voltage regulator, and show how it should be connected to function as a positive output voltage regulator. Explain. Write the equation for output voltage in terms of reference voltage.

14-23. List the most important terms in a power supply specification. Briefly explain each term. Discuss series operation, parallel operation, and tracking operation of power supplies.

14-24. Sketch the circuit for the null method of testing a power supply. Explain the system, and list the test procedure.

14-25. Sketch the circuit of a switching regulator and the waveform at various points in the circuit. Explain the operation of the regulator. Also discuss switching regulator performance and applications.

15

SIGNAL GENERATORS

INTRODUCTION

The signal generators usually found in electronics laboratories may be classified as low frequency (LF) [illegible] pulse generators, [illegible] frequency (RF) [illegible] tone generators, function generators, pulse generators, and [illegible] frequency of [illegible]

LF signal generators usually have a maximum output frequency of 100 kHz and an output voltage adjustable from 0 to 10 V. Function generators are also usually LF instruments which provide three types of output waveforms: sine, square, and triangular.

The circuit techniques employed for RF signal generators are substantially different from those used in LF instruments. RF [illegible] is necessary. Also, RF generators are normally equipped with an output load meter and a calibrated attenuator. The frequency [illegible] is [illegible] high-frequency instruments, but in this case the output frequency is [illegible] based by a piezoelectric crystal. A phase-locked loop technique is employed to facilitate adjustment of the output frequency.

Pulse generators produce pulse waveforms, and controls are provided for adjustment of pulse amplitude, pulse repetition frequency, and pulse width. Some pulse generators have facilities for adjustment of the time, fall time, delay time, and dc time level.

The output of a sweep frequency generator is a sine wave which gradually increases from a minimum frequency to maximum frequency over a selected time period. A ramp voltage with an amplitude proportional to the instantaneous frequency is also generated. Investigation of circuit frequency response is a major application of the instrument.

15-1 LOW FREQUENCY SINE WAVE GENERATORS

There are several types of sine wave oscillator circuits that can be used for signal generation. The *Wein bridge oscillator* is one circuit that gives an output with good frequency and amplitude stability, and a low distortion waveform. The Wein bridge is an ac bridge in which balance is obtained only at a particular supply frequency dependent upon the values of the bridge components. When used in an oscillator, the Wein bridge forms a feedback network between the output and input terminals of an amplifier.

In the Wein bridge oscillator circuit in Figure 15-1(a), the bridge components are R_1, R_2, R_3, R_4, C_1, and C_2. The operational amplifier together with R_3 and R_4 forms a noninverting amplifier (see Section 8-6-3), and R_1, R_2, C_1, and C_2 constitute the feedback network. Analysis of the bridge shows that balance is obtained when

$$\boxed{\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1},} \tag{15-1}$$

and

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}.} \tag{15-2}$$

If $R_1 = R_2 = R$, and $C_1 = C_2 = C$, then from Equation 15-1,

$$\boxed{R_3 = 2R_4} \tag{15-3}$$

and from Equation 15-2,

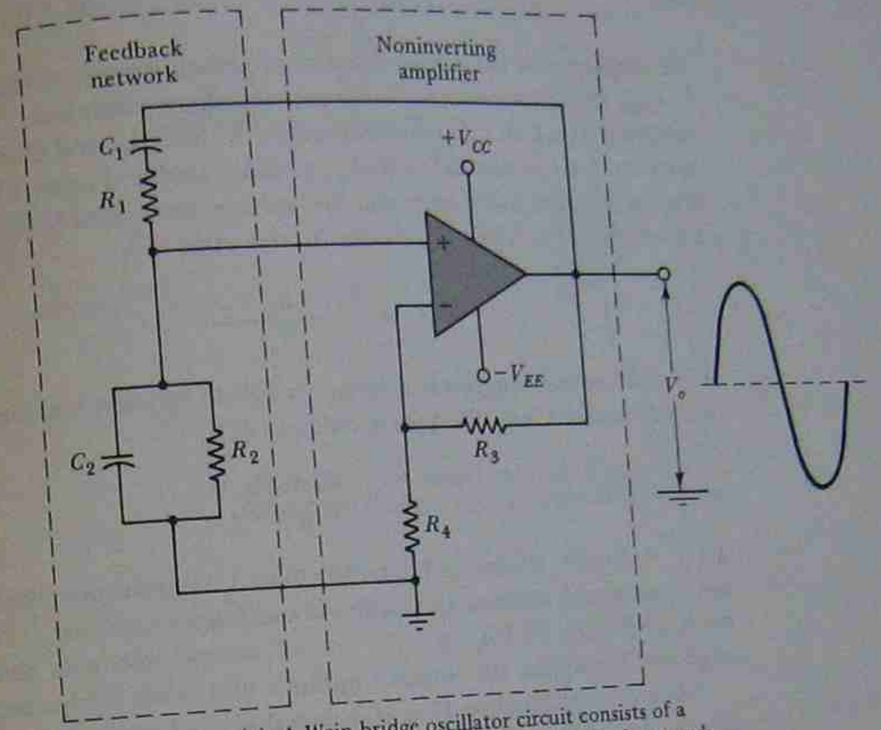
$$\boxed{f = \frac{1}{2\pi CR}.} \tag{15-4}$$

At the balance frequency of the bridge, the amplifier input voltage (developed across R_2 and C_2) is in phase with the output voltage. At all other frequencies the bridge is off balance, and the fed-back voltage does not have the correct phase relationship to the output to sustain oscillations.

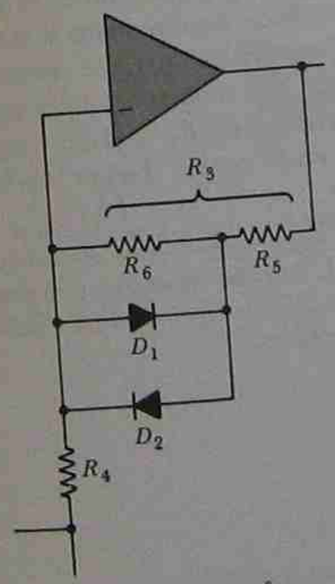
The voltage gain of the noninverting amplifier is

$$A_v = \frac{R_3 + R_4}{R_4}.$$

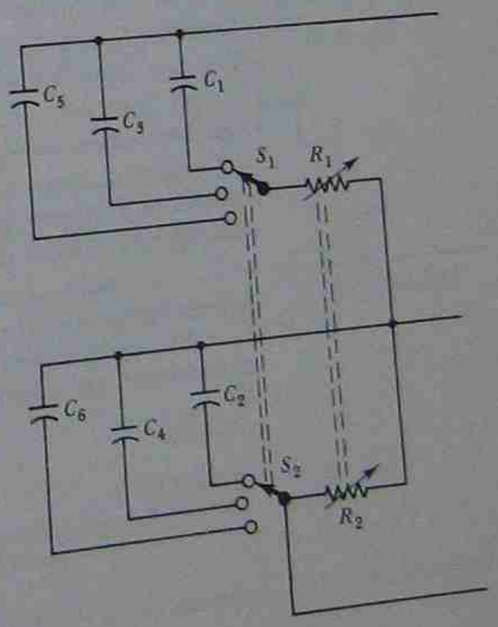
So, with $R_3 = 2R_4$ (from Equation 15-3), $A_v = 3$. In fact, the amplifier gain must be slightly greater than this to sustain oscillations. However,



(a) A Wein bridge oscillator circuit consists of a noninverting amplifier and a feedback network



(b) Modification for output amplitude stabilization



(c) Modification for frequency control

FIGURE 15-1. Basic Wein bridge oscillator circuit and modifications for amplitude stability and frequency control.

the amplitude of the output tends to approach supply voltages $+V_{CC}$ and $-V_{EE}$, and these voltage limits can introduce distortion. To avoid the problem, R_5 is split into two components, R_5 and R_6, and diodes D_1 and D_2 are connected in parallel with R_6, as illustrated in Figure 15-1(b). When the output amplitude is small, the voltage drop across R_6 is not large enough to forward bias the diodes. In this case,

$$A_v = \frac{R_4 + R_5 + R_6}{R_4}.$$

When the output amplitude is large enough to forward bias the diodes, R_6 is short-circuited, and the gain is reduced to

$$A_v = \frac{R_4 + R_5}{R_4}.$$

If $(R_4 + R_5)/R_4$ is arranged to be less than 3, large output oscillations will not be sustained, while small amplitude oscillations continue. The arrangement in Figure 15-1(b) is only one of several methods that can be employed to stabilize the output amplitude of a Wein bridge oscillator.

Referring to Equation 15-4, it is seen that the frequency of oscillations can be altered by adjustment of either R or C. Going back to Equation 15-2, R_1 and R_2 must be adjusted simultaneously to alter the value of R. Similarly, C_1 and C_2 must be simultaneously adjusted in order to alter C. The most convenient way to accommodate these requirements is to change C_1 and C_2 by switching to various standard values, and use continuously variable resistors for R_1 and R_2. Switching the capacitor values provides for frequency range changing, and variation of R_1 and R_2 facilitates continuous frequency adjustment over each range. Figure 15-1(c) illustrates how C and R should be adjusted.

EXAMPLE 15-1 A Wein bridge oscillator, as in Figure 15-1, has the following components: R_1 and R_2 variable from 500 Ω to 5 kΩ and $C_1 = C_2 = 300$ nF. Calculate the maximum and minimum output frequencies.

SOLUTION

Equation 15-4,

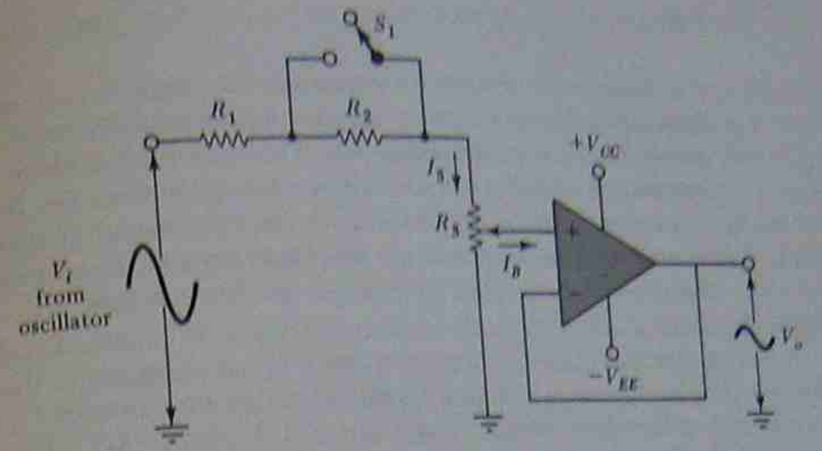
$$f = \frac{1}{2\pi CR},$$

$$f_{(\min)} = \frac{1}{2\pi \times 300\ \text{nF} \times 5\ \text{k}\Omega}$$

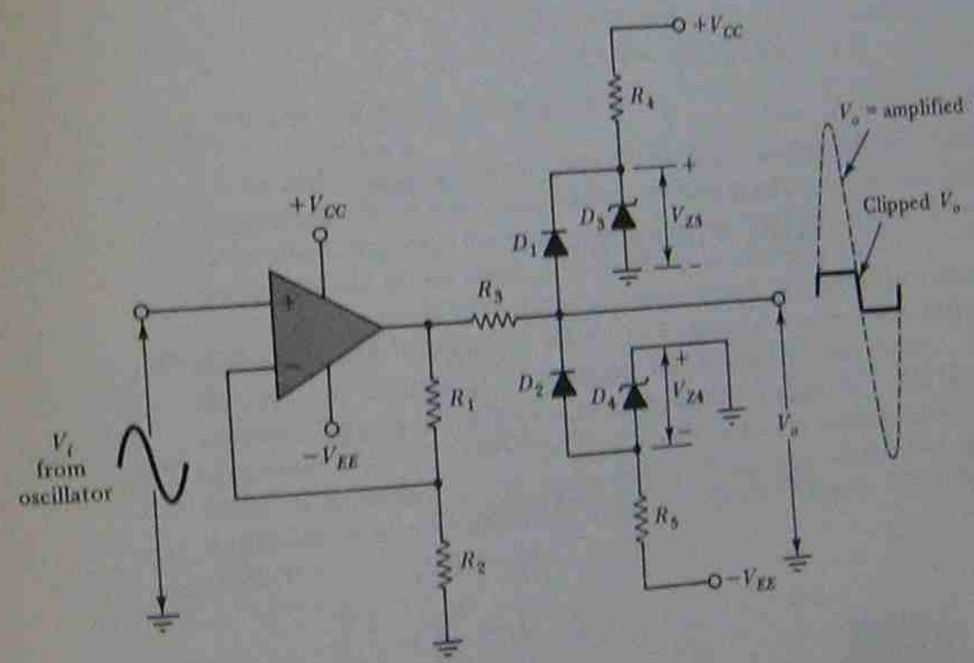
$$= 106\ \text{Hz},$$

$$f_{(\max)} = \frac{1}{2\pi \times 300\ \text{nF} \times 500\ \Omega}$$

$$= 1.06\ \text{kHz}.$$



(a) Attenuator using potentiometer R_S for amplitude control and voltage follower for low output impedance



(b) Amplifier and clipping circuit to convert sine wave into square waveform

FIGURE 15-2. Attenuator and square wave conversion circuits for use with a sinusoidal oscillator.

A sine wave generator for laboratory use must have its output amplitude adjustable, as well as its output frequency. In Figure 15-2(a) R_1, R_2, and R_3 form a potential divider which attenuates the oscillator output. The operational amplifier is connected as a voltage follower (see Section 8-6-2) to provide a low output impedance from the signal generator. R_3 is a potentiometer for adjustment of the output amplitude, and switch S_1 allows the output to be switched between two amplitude ranges.

EXAMPLE 15-2 A 5-V sine wave is fed from a Wein bridge oscillator to the attenuator circuit illustrated in Figure 15-2(a). Calculate the values of R_1, R_2, and R_3 to give output voltage ranges of 0–0.1 V and 0–1 V. The input bias current to the operational amplifier is $I_B = 500$ nA.

SOLUTION

With R_1 and R_2 in the circuit:

$$V_{R3} = 0.1 \text{ V},$$

and

$$\begin{aligned} V_{R1} + V_{R2} &= V_i - V_{R3} \\ &= 5 \text{ V} - 0.1 \text{ V} \\ &= 4.9 \text{ V}, \end{aligned}$$

$$I_3 \gg I_B.$$

Let $I_3 = 100\ \mu$A. Then

$$R_3 = \frac{0.1 \text{ V}}{100\ \mu\text{A}} = 1 \text{ k}\Omega \text{ (potentiometer)},$$

and

$$R_1 + R_2 = \frac{4.9 \text{ V}}{100\ \mu\text{A}} = 49 \text{ k}\Omega.$$

With R_2 switched out of the circuit:

$$V_{R3} = 1 \text{ V},$$

and

$$\begin{aligned} I_3 &= \frac{V_{R3}}{R_3} = \frac{1 \text{ V}}{1 \text{ k}\Omega} \\ &= 1 \text{ mA}, \\ V_{R1} &= 5 \text{ V} - 1 \text{ V} \\ &= 4 \text{ V}, \\ R_1 &= \frac{4 \text{ V}}{1 \text{ mA}} = 4 \text{ k}\Omega, \\ R_2 &= 49 \text{ k}\Omega - 4 \text{ k}\Omega \\ &= 45 \text{ k}\Omega. \end{aligned}$$

Figure 15-2(b) shows a method of converting the sine wave output of an oscillator into a square wave. The operational amplifier is connected to function as a noninverting amplifier (see Section 8-6-3). The amplifier has a very high gain, so that the amplified output tends to be very large [see the waveforms in Figure 15-2(b)]. Diodes D_1 and D_2 together with zener diodes D_3 and D_4 and the associated resistors form a *clipping circuit*. This has the effect of clipping off the positive and negative half cycles of the amplifier output at a certain voltage level. As illustrated, the amplified and clipped sine wave becomes (approximately) a square wave.

Suppose that in Figure 15-2(b) $V_{Z3} = V_{Z4} = 6.3$ V. Also assume that D_1 and D_2 are silicon diodes with a forward voltage drop of 0.7 V. When the amplifier output goes positive, D_1 becomes forward biased and prevents the output from exceeding $(V_{Z3} + V_{D1})$. Similarly, when the output goes negative D_2 is forward biased, and the output cannot fall below $-(V_{Z4} + V_{D2})$. Thus, the square wave output amplitude is

$$\begin{aligned} V_o &= \pm (V_Z + V_D) \\ &= \pm (6.3 \text{ V} + 0.7 \text{ V}) \\ &= \pm 7 \text{ V}. \end{aligned}$$

An audio signal generator normally consists of a sinusoidal oscillator, a sine-to-square wave converter, and an attenuator output stage (see Figure 15-3). When required, the square wave shaping circuit is switched into the system between the oscillator output and the attenuator input.

The front panel of a signal generator which performs the functions discussed above is shown in Figure 15-4. Square or sine wave output is selected by depressing or releasing the left-hand push button. Four frequency ranges are available from a minimum of 10 Hz–100 Hz to a maximum of 10 kHz–100 kHz. Continuous frequency adjustment on each range is provided by the large control knob and scale. The output amplitude is also continuously adjustable on two ranges: 0–0.1 V and 0–10 V.

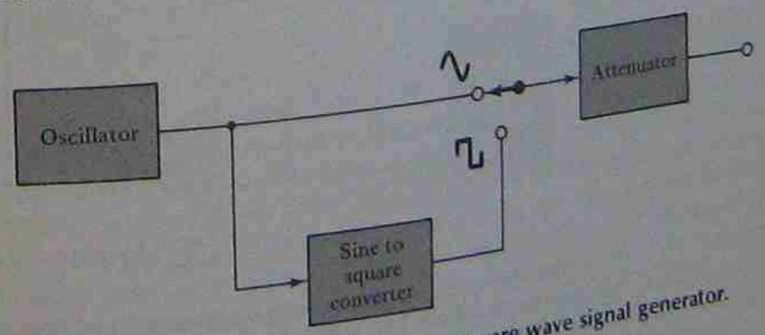


FIGURE 15-3. Block diagram of sine/square wave signal generator.

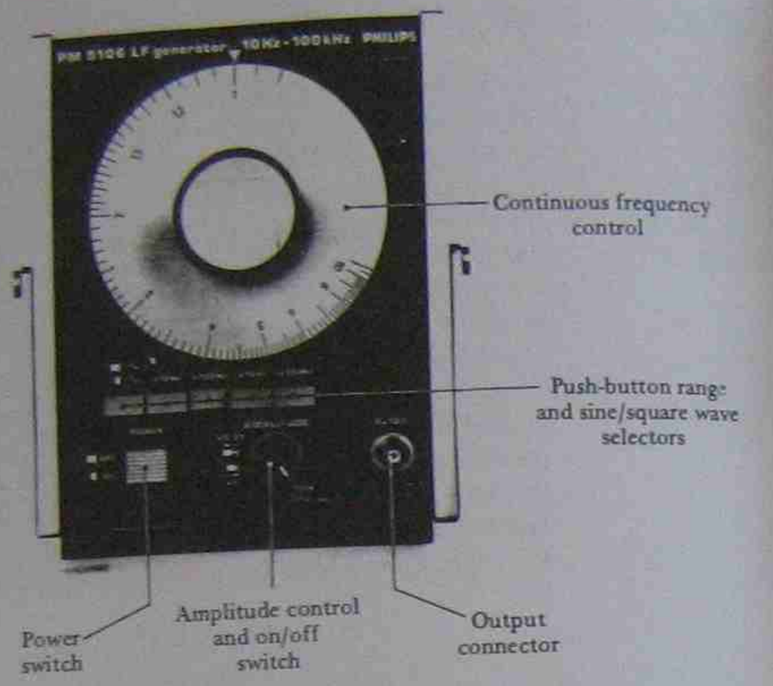


FIGURE 15-4. Low-frequency sine/square wave generator (Courtesy of Philips Electronics).

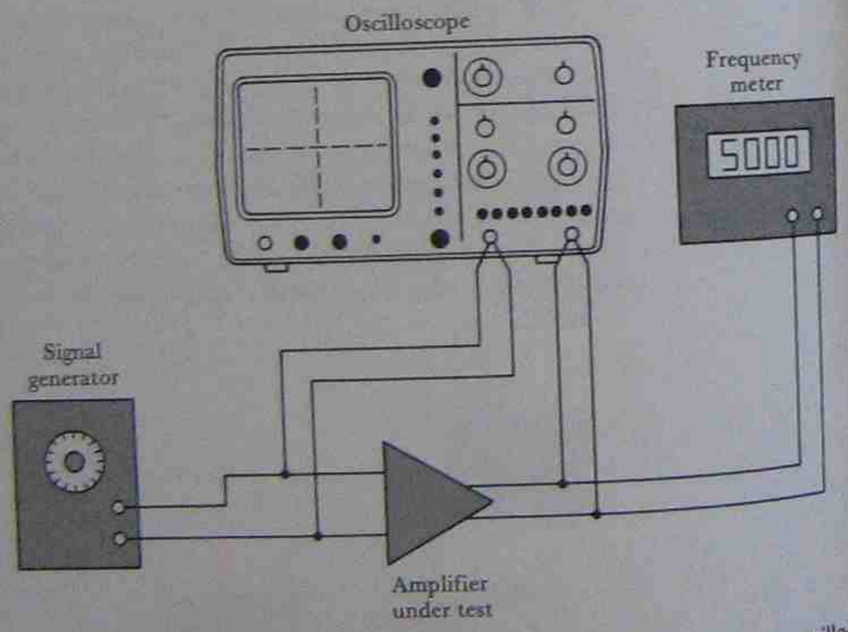


FIGURE 15-5. Audio signal generator used to test an amplifier. An oscilloscope monitors the input and output waveforms of the amplifier, and a frequency meter displays the signal frequency.

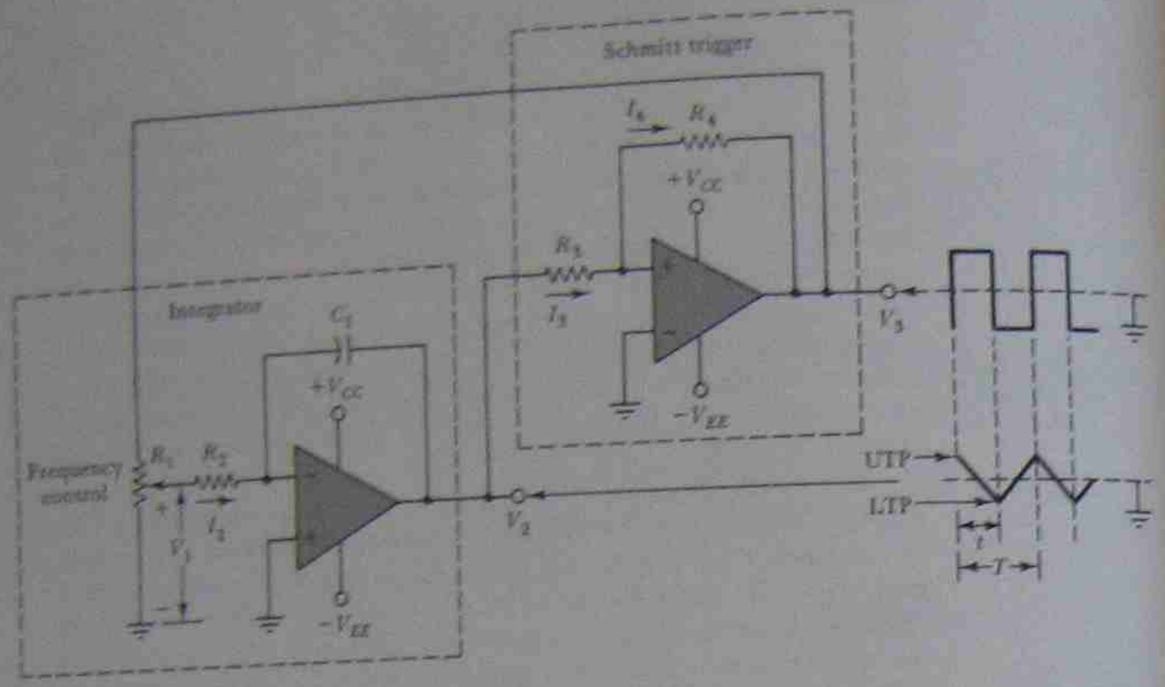
A typical audio signal generator application is illustrated in Figure 15-5. A dual-trace oscilloscope is connected to monitor the input and output waveforms of an amplifier under test, and a frequency meter is included to give an accurate indication of signal frequency. Normally the amplifier is tested for frequency response and phase shift. The phase shift between input and output is easily measured by comparing the two waveforms on the oscilloscope (see Section 11-7). Unless the signal generator is equipped with an output level meter which can be observed, the output voltage cannot be assumed to remain constant. Before each measurement is made of output amplitude, the input level should be checked on the oscilloscope, and the signal generator amplitude control adjusted as necessary.

The signal frequency is first set approximately at the middle of the amplifier frequency response. From this point, the frequency is decreased in convenient steps, and the amplifier gain and phase shift are recorded at each step. The procedure is continued until the amplifier lower 3-dB frequency is found. The generator frequency is then increased in steps from the mid frequency until the upper 3-dB frequency of the amplifier is found. At each step the amplifier gain and phase shift are again noted. Using the recorded data, the gain/frequency and phase/frequency response graphs are plotted for the amplifier. The process described above can be performed very much faster by using a sweep frequency generator (see Section 15-5).

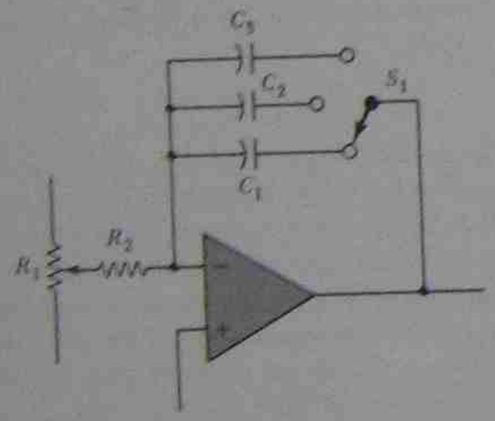
15-2 FUNCTION GENERATORS

A basic *function generator* produces sine, square, and triangular waveform outputs. Sometimes a ramp waveform is also generated. Output frequency and amplitude are variable, and a dc offset adjustment may be included. The sine/square wave generator described in Section 15-1 could be used as a function generator if a circuit for converting the square wave into a triangular wave is employed. However, the usual method of generating a triangular wave is to use an *integrator* and a *Schmitt trigger circuit*. The arrangement is shown in Figure 15-6(a).

The Schmitt trigger circuit is a noninverting type. (Schmitt trigger circuits are also discussed in Section 11-4-1.) When the input voltage increases to the *upper trigger point* (UTP), the output suddenly rises from its most negative level to its most positive level. Similarly, when the input goes to the *lower trigger point* (LTP), the op-amp output voltage rapidly drops to its most negative level. Note that the inverting input terminal of the Schmitt op-amp is grounded. Also recall that the operational amplifier has a voltage gain of about 200 000. Only a very small voltage difference is required between inverting and noninverting terminals to drive the op-amp output to saturation in either a positive or negative direction. If V_{CC} and V_{EE} are ± 15 V, the output is typically ± 14 V. The minimum voltage



(a) Basic circuit and waveforms



(b) Modification for frequency range changing

FIGURE 15-6. A basic function generator circuit consists of an integrator and a Schmitt trigger circuit. Frequency is adjusted continuously by means of R_1 and frequency range is changed by capacitor selection.

difference between the inverting and noninverting input terminals to produce output saturation is

$$V_i = \frac{14\text{ V}}{200\,000} = 70\ \mu\text{V}.$$

When the noninverting input terminal in the Schmitt circuit in Figure 15-6(a) is 70 μV (or more) above or below the grounded inverting input terminal, the output voltage saturates at +14 V or −14 V.

Now assume that the input voltage to R_3 in Figure 15-6(a) is at ground level, and that the output is at −14 V. The output voltage is potentially divided across R_3 and R_4 to give

$$V_{R3} = -14\text{ V} \times \frac{R_3}{R_3 + R_4}.$$

Clearly, the junction of R_3 and R_4 (i.e., the op-amp noninverting input terminal) is at a negative level with respect to ground. With a negative voltage at the noninverting input terminal, the op-amp output is certain to be negative.

Consider the effect of slowly increasing the input voltage (to R_3). With the output voltage still at −14 V, the input may have to be raised several volts above ground before the junction of R_3 and R_4 reaches ground level. When the noninverting terminal is raised just microvolts above ground, the output terminal commences to move positively from its −14-V level. As the output raises, the junction of R_3 and R_4 is driven more positive, and this acts as an input to cause the output to rise further and faster. The result is that just as soon as the noninverting terminal commences to rise above ground, the op-amp output rapidly switches from its negative saturation voltage to its positive saturation level (i.e., from −14 V to +14 V). The input voltage that produces this change is the UTP.

An effect similar to that described above occurs when the output is positive and a negative input voltage is applied. For the Schmitt circuit illustrated in Figure 15-6(a), the LTP is numerically equal to the UTP, although opposite in polarity.

EXAMPLE 15-3 The Schmitt trigger circuit in Figure 15-6(a) has: $V_{CC} = \pm 15$ V, $R_3 = 3.9$ kΩ and $R_4 = 18$ kΩ. Calculate the UTP and LTP.

SOLUTION

$$\textit{output voltage}, V_3 \approx V_{CC} - 1\text{ V}$$
$$= \pm(15\text{ V} - 1\text{ V})$$
$$= \pm 14\text{ V}.$$

The UTP *occurs when* $V_o = -14$ V *and the op-amp noninverting input terminal is at ground, i.e., when* $V_{R4} = 14$ V.

$$I_4 = \frac{V_{R4}}{R_4} = \frac{14\text{ V}}{18\text{ k}\Omega}$$
$$= 0.78\text{ mA},$$
$$I_3 = I_4,$$
$$V_{R3} = I_3 R_3$$
$$= 0.78\text{ mA} \times 3.9\text{ k}\Omega$$
$$\simeq 3\text{ V} = \text{UTP}.$$

and

The LTP *occurs when* $V_o = +14$ V *and the op-amp noninverting terminal is at ground, i.e., when* $V_{R4} = -14$ V.

$$I_3 = I_4 = \frac{V_{R4}}{R_4} = \frac{-14\text{ V}}{18\text{ k}\Omega}$$
$$= -0.78\text{ mA},$$
$$V_{R3} = (-0.78\text{ mA}) \times 3.9\text{ k}\Omega$$
$$= -3\text{ V} = \text{LTP}.$$

Refer to the integrator section of Figure 15-6(a). In this circuit the op-amp noninverting terminal is grounded, and the inverting terminal is connected via capacitor C_1 to the amplifier output. If C_1 were replaced by a short circuit, the op-amp would behave as a voltage follower. Both the output and inverting input terminals would be at ground level because the noninverting input is grounded. With C_1 in circuit and with zero charge on C_1, the circuit again behaves as a voltage follower. All three terminals of the op-amp are at ground level. Now suppose that C_1 becomes charged with a terminal voltage of 1 V, + on the right and − on the left-hand side. The inverting input terminal still remains at ground level, and the output is +1 V with respect to ground. The circuit voltages remain stable at these levels while C_1 terminal voltage remains constant. Similarly, if C_1 is charged to 1 V with the opposite polarity (+ on the left, − on the right), the inverting terminal remains at ground level and the output voltage becomes −1 V with respect to ground.

Now assume that a positive input voltage ($+V_1$) is applied to R_2 as shown in Figure 15-6(a). The left-hand terminal of R_2 is at $+V_1$, while the right-hand terminal is at ground level (because the noninverting input remains at ground). Therefore, all of V_1 appears across R_2, and a *constant current* I_2 flows through R_2:

$$I_2 = \frac{V_1}{R_2}.$$

I_2 is made very much larger than the input bias current to the operational amplifier. Consequently, virtually all of I_2 flows into C_1, charging it with a polarity: + on the left, − on the right. As C_1 charges, its voltage increases linearly, and because its left-hand (+) terminal is at ground level, the op-amp output voltage decreases linearly. When the polarity of V_1 is inverted, I_2 is reversed, and C_1 commences to charge with the opposite polarity. This causes the integrator output voltage to reverse direction.

Returning again to Figure 15-6(a), it is seen that the integrator input voltage is derived from the Schmitt trigger output. Also, the integrator output is applied as an input to the Schmitt circuit. To understand the combined operation of the two circuits, assume that the Schmitt output (V_3) is +14 V, and that the integrator output is at ground level. V_1 is positive because the Schmitt output is +14 V, and consequently I_2 is charging C_1: + on the left, − on the right. Thus, the integrator output voltage (V_2) is decreasing linearly from ground level. When V_2 arrives at the LTP of the Schmitt, the output voltage of the Schmitt rapidly switches to $V_3 = -14$ V. This causes V_1 to reverse polarity and results in I_2 reversing direction. Now C_1 commences to charge in the opposite direction, and V_2 increases linearly from the LTP [see the waveforms in Figure 15-6(a)]. C_1 continues to charge in this direction until the integrator output becomes equal to the Schmitt UTP. When V_2 arrives at the UTP, the Schmitt output immediately reverses polarity once again to $V_3 = +14$ V. V_1 is now positive once more, and I_2 charges C_1 with a polarity that makes V_2 go in a negative direction once again.

The process described above is repetitive, and the integrator output produces a triangular waveform, as illustrated. The Schmitt output is a square wave, which is positive while the integrator output is negative-going, and negative during the time that V_2 is positive-going. The frequency of the output waveforms is determined by the time for C_1 to charge from the UTP to the LTP, and vice versa. The equation for a capacitor charging linearly is

$$C = \frac{It}{\Delta V}$$

or

$$\boxed{t = \frac{C\Delta V}{I}}. \qquad (15\text{-}5)$$

In this case, C is C_1, ΔV = UTP − LTP, I is I_2, and t is the time for V_2 to go between UTP and LTP. Time t is also half the time period of the output waveform. V_1 is adjustable by means of potentiometer R_1, and because $I_2 = V_1/R_2$, I_2 is also controllable by R_1. Adjustment of I_2 results in a change in t; consequently, R_1 is a frequency control. Frequency range changing is effected by switching different capacitor values into the circuit, as illustrated in Figure 15-6(b).

EXAMPLE 15-4 The integrator circuit in Figure 15-6 has $C_1 = 0.1\ \mu\text{F}$, $R_1 = 1\ \text{k}\Omega$, and $R_2 = 10\ \text{k}\Omega$. If the Schmitt trigger circuit has ± 3 V trigger points, calculate the output frequency when the moving contact of R_1 is at the top of the potentiometer, and when it is at 10% of R_1 from the bottom. The supply voltage is $V_{CC} = \pm 15$ V.

SOLUTION

$$\begin{aligned} V_3 &= \pm (V_{CC} - 1\ \text{V}) \\ &= \pm (15\ \text{V} - 1\ \text{V}) \\ &= \pm 14\ \text{V}. \end{aligned}$$

For contact at top of R_1:

$$\begin{aligned} V_1 &= V_3 = 14\ \text{V}, \\ I_2 &= \frac{V_1}{R_2} = \frac{14\ \text{V}}{10\ \text{k}\Omega} \\ &= 1.4\ \text{mA}, \\ \Delta V &= \text{UTP} - \text{LTP} \\ &= 3\ \text{V} - (-3\ \text{V}) \\ &= 6\ \text{V}. \end{aligned}$$

Equation 15-5,

$$\begin{aligned} t &= \frac{C\Delta V}{I_2} \\ &= \frac{0.1\ \mu\text{F} \times 6\ \text{V}}{1.4\ \text{mA}} \\ &\simeq 0.43\ \text{ms}, \\ f &= \frac{1}{2t} = \frac{1}{2 \times 0.43\ \text{ms}} \\ &= 1.17\ \text{kHz}. \end{aligned}$$

For R_1 contact at 10% from bottom:

$$\begin{aligned} V_1 &= 10\%\ \textit{of}\ V_3 \\ &= 10\%\ \textit{of}\ 14\ \text{V} \\ &= 1.4\ \text{V}, \\ I_2 &= \frac{1.4\ \text{V}}{10\ \text{k}\Omega} = 0.14\ \text{mA}, \\ t &= \frac{0.1\ \mu\text{F} \times 6\ \text{V}}{0.14\ \text{mA}} \\ &\simeq 4.3\ \text{ms}, \\ f &= \frac{1}{2 \times 4.3\ \text{ms}} \\ &\simeq 117\ \text{Hz}. \end{aligned}$$

A widely used method for converting a triangular wave into an approximate sinusoidal waveform is illustrated in Figure 15-7. If diodes D_1 and D_2 and resistors R_3 and R_4 were not present in the circuit of Figure 15-7(a), R_1 and R_2 would simply behave as a voltage divider. In this case, the output from the circuit would be an attenuated version of the triangular input wave:

$$V_o = V_i \frac{R_2}{R_1 + R_2}.$$

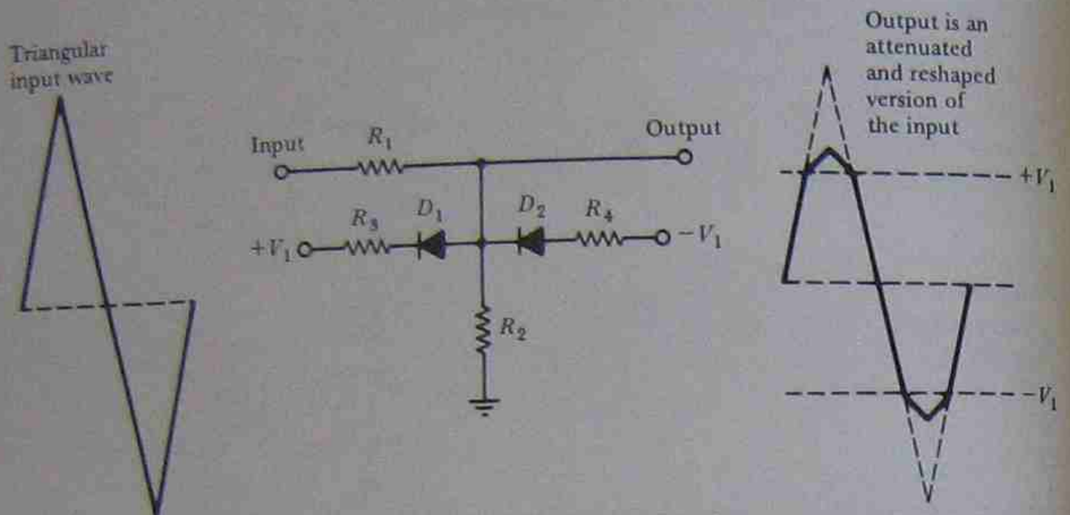
With D_1 and R_3 in the circuit, R_1 and R_2 still behave as a simple voltage divider until V_{R2} exceeds $+V_1$. At this point D_1 becomes forward biased, and R_3 is effectively in parallel with R_2.

Now,

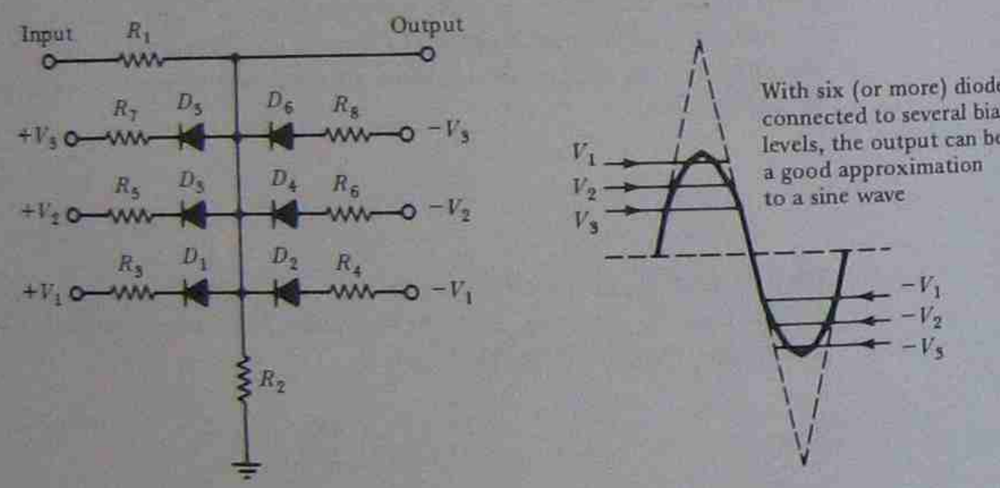
$$V_o = V_i \frac{R_2 \| R_3}{R_1 + R_2 \| R_3}.$$

Output voltage levels above $+V_1$ are attenuated to a greater extent than levels below $+V_1$. Consequently, the output voltage rises less steeply than without D_1 and R_3 in the circuit [see Figure 15-7(a)]. When the output falls below $+V_1$, diode D_1 is reverse biased, R_3 is no longer in parallel with R_2, and the attenuation is once again $R_2/(R_1 + R_2)$. Similarly, during the negative half cycle of the input, the output is $V_o = V_i[R_2/(R_1 + R_2)]$ until V_o goes below $-V_1$. Then, D_2 becomes forward biased, putting R_4 in parallel with R_2 and making

$$V_o = V_i \frac{R_2 \| R_4}{R_1 + R_2 \| R_4}.$$



(a) Two-level diode loading circuit and input and output waveforms



(b) Six-level diode loading circuit and its effect on input waveform

FIGURE 15-7. A triangular waveform can be shaped into a good sine wave approximation by diode loading.

With $R_3 = R_4$, the negative half cycle of the output is similar in shape to the positive half cycle.

When six or more diodes are employed, all connected via resistors to different bias voltage levels [see Figure 15-7(b)], a good sine wave approximation can be achieved. With six diodes, three positive bias voltage levels, and three negative bias levels, the slope of the output wave changes

three times during each quarter cycle. Assuming correctly selected bias voltages and resistor values, the output wave shape is as shown in Figure 15-7(b).

The block diagram of a basic function generator is shown in Figure 15-8. The integrator output is fed into the Schmitt trigger and the sine wave converter. As already explained, the integrator must have the square wave from the Schmitt as an input. A switch is provided for selection of sine, triangular, or square waves. The output stage can be the type of attenuator shown in Figure 15-2(a). This circuit provides low output impedance and output amplitude control. A means of synchronizing the output frequency to an external source is sometimes included in a function generator. In Figure 15-6(a) a sync input can be arranged by connecting a resistor between ground and the Schmitt op-amp inverting input terminal. The sync input pulses are then capacitor coupled to the inverting input terminal. The method is explained in Section 11-4-2.

Commercially available function generators typically have the output frequency in decade ranges from a minimum of 0.2 Hz to a maximum of 2 MHz. Output amplitude is usually 0–20 V *p*-to-*p* and 0–2 V *p*-to-*p*. The amplitude control is often marked as 0–20 V, with a 20-dB attenuation push button which changes the output to 0–2 V. Output impedances of function generators are typically 50 Ω. It should be remembered that the signal voltage is potentially divided across the output impedance and the load impedance. Thus, a 20-V output on open-circuit may become 10 V when a 50-Ω load impedance is connected. The stability of the output amplitude and frequency is commonly specified as ±0.05% for 10 minutes and ±0.25% for 24 hours. Accuracy of frequency selection is usually around ±2% of full scale on any particular range, and distortion content in sinusoidal outputs is normally less than 1%.

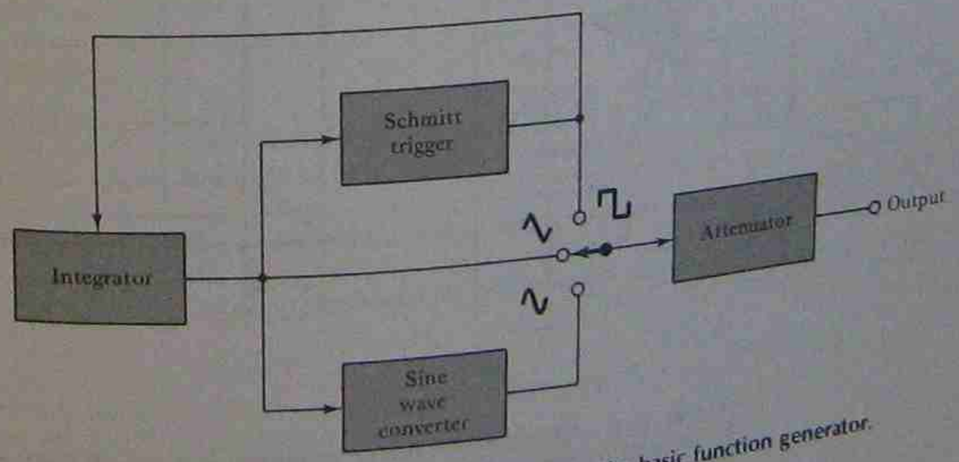


FIGURE 15-8. Block diagram of a basic function generator.

15-3 PULSE GENERATORS

A *pulse generator* normally consists of a square wave generating circuit, a *monostable multivibrator*, and an output stage with attenuation and dc level shifting. The square wave circuit could be one of those already discussed in Sections 15-1 and 15-2. Alternatively, the type of astable multivibrator illustrated in Figure 15-9 could be employed.

The operational amplifier with resistors R_2 and R_3 in Figure 15-9 functions as an inverting Schmitt trigger circuit. Like the noninverting Schmitt described in Section 15-2, it has upper and lower trigger points and a square wave output. The UTP is a positive voltage level, and the LTP is a negative level. Numerically the two are equal to the voltage drop across R_3 when the op-amp output voltage is in its saturated state:

$$|\text{UTP}| = |\text{LTP}| = V_o \frac{R_3}{R_2 + R_3}. \tag{15-6}$$

When the Schmitt output voltage is positive, the voltage at the noninverting input terminal of the op-amp is a positive quantity. Current flows from the output through resistor R_1 to charge capacitor C_1. When the capacitor voltage arrives at the level of the UTP, the op-amp inverting terminal voltage is driven above the level of the noninverting terminal. The op-amp output now commences to fall, and as it does so, V_{R3} falls.

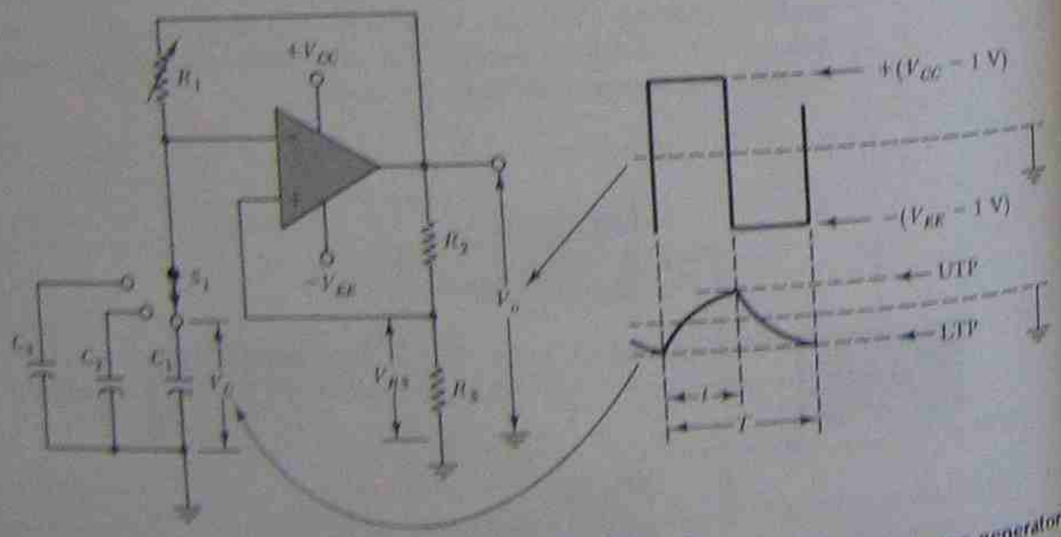


FIGURE 15-9. Astable multivibrator employed as a square wave generator. R_1 provides continuous frequency control, and S_1 is a frequency range selector.

This pulls the noninverting terminal further below the level of the inverting terminal, and thus causes the output to be driven further and faster in a negative direction. In fact, the op-amp output goes very rapidly from approximately $+(V_{CC} - 1\text{ V})$ to $-(V_{EE} - 1\text{ V})$. At this point the capacitor has been charged to the UTP, i.e., $+V_{R3}$. But the charging voltage (V_o) has suddenly switched from $+(V_{CC} - 1\text{ V})$ to $-(V_{EE} - 1\text{ V})$. The capacitor now commences to charge in the opposite direction, eventually arriving at the LTP ($-V_{R3}$). Now the Schmitt output rapidly switches to $+(V_{CC} - 1\text{ V})$ again, and the capacitor commences to recharge in a positive direction.

The process repeats continuously as described, producing a square wave output from the Schmitt circuit, as well as generating an exponential wave across C_1. The frequency of the square wave depends upon the time (t) for the capacitor to charge between LTP and UTP:

$$f = \frac{1}{T} = \frac{1}{2t}.$$

Time t can be adjusted by variable resistor R_1. So R_1 is a continuous frequency control. Frequency range is changed by selecting various capacitor values by means of switch S_1, as illustrated. The time t is calculated from the basic equation for a capacitor charged via a resistor:

$$\epsilon_c = E - (E - E_o)e^{-t/CR}$$

which can be rearranged:

$$t = CR \ln\left[\frac{E - E_o}{E - \epsilon_c}\right]. \tag{15-7}$$

where E is the charging voltage, E_o is the initial charge on the capacitor, and ϵ_c is the final capacitor voltage at time t.

EXAMPLE 15-5 The astable multivibrator circuit in Figure 15-9 has: $R_1 = 20\text{ k}\Omega$, $R_2 = 6.2\text{ k}\Omega$, $R_3 = 5.6\text{ k}\Omega$, and $C_1 = 0.2\ \mu\text{F}$. The supply voltage is ± 12 V. Calculate the frequency of the square wave output.

SOLUTION

$$\begin{aligned} V_o &= \pm (V_{CC} - 1\text{ V}) \\ &= \pm (12\text{ V} - 1\text{ V}) \\ &= \pm 11\text{ V}. \end{aligned}$$

Equation 15-6,

$$|\text{UTP}| = |\text{LTP}| = V_s \frac{R_3}{R_2 + R_3}$$
$$= 11\text{ V} \times \frac{5.6\text{ k}\Omega}{6.2\text{ k}\Omega + 5.6\text{ k}\Omega}$$
$$= 5.22\text{ V},$$
$$E_o = -5.22\text{ V}, e_c = +5.22\text{ V}, E = +11\text{ V}.$$

Equation 15-7,

$$t = C_1 R_1 \ln\left[\frac{E - E_o}{E - e_c}\right]$$
$$= 0.2\,\mu\text{F} \times 20\text{ k}\Omega \times \ln\left[\frac{11\text{ V} - (-5.22\text{ V})}{11\text{ V} - 5.22\text{ V}}\right]$$
$$= 4.13\text{ ms},$$
$$f = \frac{1}{2 \times 4.13\text{ ms}}$$
$$= 121\text{ Hz}.$$

A monostable multivibrator has one stable state. When a triggering input is applied, the output changes state for a fixed period of time, and then reverts back to its initial condition. This produces an output pulse with a constant width each time the monostable multivibrator is triggered.

An operational amplifier connected to function as a monostable multivibrator is shown in Figure 15-10. The inverting input terminal has a positive bias voltage (V_B), where V_B is typically 1 V. The op-amp noninverting terminal is grounded via resistor R_2. Thus, the dc condition of the circuit is (inverting input) = +1 V and (noninverting input) = 0 V. This causes the op-amp output to be saturated in a negative direction, giving $V_o = -(V_{EE} - 1\text{ V})$. Capacitor C_2 is grounded via R_2 on its left-hand side, while its right-hand terminal is at $-(V_{EE} - 1\text{ V})$. Therefore, C_2 is charged (+ on the left, − on the right) to a level of $E_o = (V_{EE} - 1\text{ V})$. These dc voltages are maintained until a triggering input signal arrives via capacitor C_1.

When a square wave input is applied to the monostable circuit, C_1 charges rapidly via R_1 at each positive-going and negative-going edge of the input waveform. The pulses of charging current through R_1 generate spikes at the op-amp inverting input terminal. Positive spikes occur at the positive-going edges of the square wave, and negative-going spikes coincide with the negative-going edges (see Figure 15-10). C_1 and R_1, in fact, behave as a differentiating circuit, and diode D_1 clips off the positive spikes.

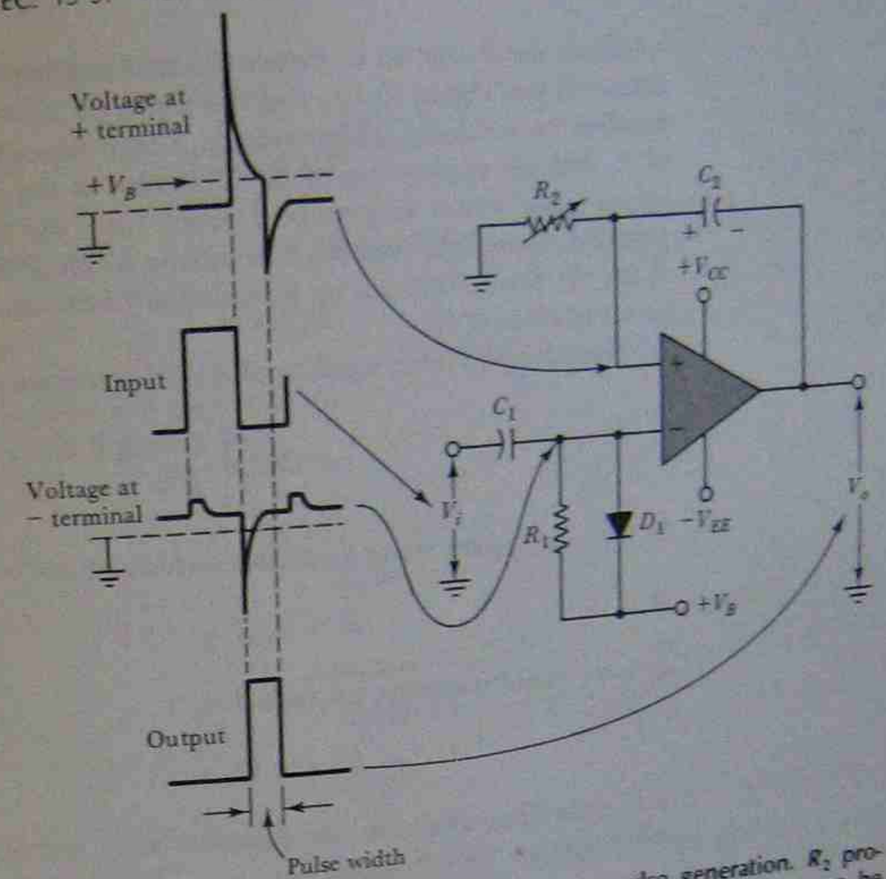


FIGURE 15-10. A monostable multivibrator for pulse generation. R_2 provides continuous pulse width control. Several pulse width ranges can be made available by switching-in different capacitor values for C_2.

Since the positive spikes are clipped off, they have no effect on the monostable circuit. However, the negative-going spikes drive the op-amp inverting input terminal below the level of the noninverting input. When this occurs, the op-amp output rapidly switches to its positive saturation level; $V_o = V_{CC} - 1$ V. When the output goes positive, the voltage at the noninverting input becomes

$$V_o + E_o = (V_{CC} - 1\text{ V}) + (V_{EE} - 1\text{ V})$$
$$= 2V_{CC} - 2\text{ V}.$$

This high positive voltage level at the noninverting terminal holds the op-amp output at its positive saturation level, even when the negative triggering spike has ended.

Capacitor C_2 now begins to discharge via R_2, and to recharge with opposite polarity. As C_2 charges, the noninverting terminal voltage falls towards ground level. As soon as this voltage (at the noninverting input) falls slightly below the bias ($+V_B$) at the inverting input, the op-amp output rapidly switches to $-(V_{EE} - 1\text{ V})$ once again. At the instant of

switching, the charge on C_2 causes the noninverting terminal to be driven negatively (see Figure 15-10), and this assists the switching speed. The time duration for which the output voltage is high depends upon the resistance of R_2 and the capacitance of C_2. This time is the width of the positive output pulse which is generated every time the monostable circuit is triggered. Since R_2 is variable, it is a pulse width (PW) control. The range of the PW can be changed by switching different capacitor values into the circuit in place of C_2.

Equation 15-7 once again applies in determining the output PW:

$$t = CR \ln\left[\frac{E - E_o}{E - \epsilon_c}\right].$$

In this case E is the charging voltage, which equals $+V_o$,

or, $$E = +(V_{CC} - 1\ V);$$

E_o is the initial charge on the capacitor,

$$E_o = -(V_{EE} - 1\ \text{V});$$

and ϵ_c the final charge on the capacitor when the op-amp noninverting input terminal voltage equals V_B,

$$\begin{aligned}\epsilon_c &= V_o - V_B \\ &= +(V_{CC} - 1\ \text{V}) - V_B.\end{aligned}$$

EXAMPLE 15-6 The monostable multivibrator circuit in Figure 15-10 has a supply voltage of ± 10 V, and $V_B = +1$ V. The circuit components are: $R_1 = 22\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $C_1 = 100$ pF, $C_2 = 0.01\ \mu\text{F}$. Calculate the output PW. Also determine the new capacitance of C_2 to give PW = 6 ms.

SOLUTION

$$\begin{aligned}E &= +(V_{CC} - 1\ \text{V}) \\ &= +(10\ \text{V} - 1\ \text{V}) \\ &= +9\ \text{V}, \\ E_o &= -(V_{EE} - 1\ \text{V}) \\ &= -9\ \text{V}, \\ \epsilon_c &= V_o - V_B \\ &= +(10\ \text{V} - 1\ \text{V}) - 1\ \text{V} \\ &= 8\ \text{V},\end{aligned}$$

Equation 15-7,

$$\begin{aligned}t &= C_2 R_2 \ln\left[\frac{E - E_o}{E - \epsilon_c}\right] \\ &= 0.01\ \mu\text{F} \times 10\ \text{k}\Omega \times \ln\left[\frac{9\ \text{V} - (-9\ \text{V})}{9\ \text{V} - 8\ \text{V}}\right] \\ &= 289\ \mu\text{s};\end{aligned}$$

for PW = 6 ms; $t = 6$ ms.
From Equation 15-7,

$$\begin{aligned}C_2 &= \frac{t}{R_2 \ln\left[\frac{E - E_o}{E - \epsilon_c}\right]} \\ &= \frac{6\ \text{ms}}{10\ \text{k}\Omega \times \ln\left[\frac{9\ \text{V} - (-9\ \text{V})}{9\ \text{V} - 8\ \text{V}}\right]} \\ &= 0.2\ \mu\text{F}.\end{aligned}$$

In Figure 15-11, resistors R_1, R_2, and R_3 together with operational amplifier A_1 constitute an output attenuator as already shown in Figure 15-2(a) and discussed in Section 15-1. This allows the output amplitude of the pulse generator to be adjusted and gives a low output impedance. Operational amplifier A_2 and resistors R_4, R_5, and R_6 provide dc level shifting. Capacitor C_1 passes pulses from the pulse generator into the attenuator circuit, while allowing the dc output level of the attenuator to be set to any desired level. A_2 is a voltage follower, and its dc output voltage is set by potentiometer R_5. When the moving contact of R_5 is at ground level, A_2 output is also at ground. This gives an output pulse from A_1 which is symmetrical above and below ground level. When the moving contact of R_5 is +5 V, the output pulse is symmetrical above and below the +5-V level, and when the potentiometer voltage is −5 V, the pulse output is symmetrical above and below the −5-V level.

The output frequency of the pulse generator can be synchronized to an external frequency, by capacitor coupling synchronizing spikes to the junction of R_2 and R_3 in Figure 15-9. The method is essentially as explained in Section 11-4-2.

Some pulse generators are equipped with manual triggering. This is simply a switching arrangement for disconnecting the monostable multivibrator from the square wave generator, and for push-button connection of a step input to C_1 in Figure 15-10. The arrangement is shown in Figure

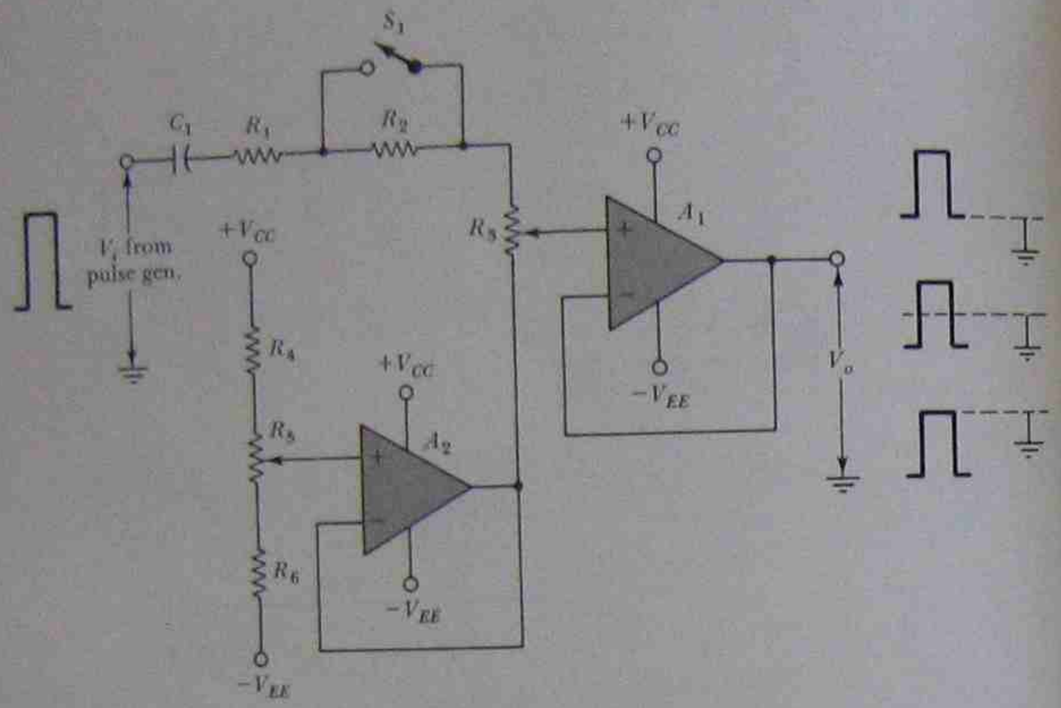


FIGURE 15-11. Attenuator and dc offset control for use with a pulse generator. R_3 provides continuous attenuation adjustment, and S_1 changes the attenuation range. R_5 is the dc offset control.

15-12. S_2 disconnects the square wave input, and R_3 keeps C_1 input grounded until push-button switch S_3 is operated to provide a dc step ($+V_{CC}$) input. Sometimes an external triggering input terminal is also included.

The output pulses from a pulse generator usually have leading and lagging edges which seem to be perfectly vertical when displayed on an oscilloscope. In fact, the leading edges have a finite *rise time*, and the lagging edges have a *fall time* (see Figure 15-13). The rise time (t_r) is defined as the time for the output to go from 10% to 90% of its amplitude, and the fall time (t_f) is the time for the output to go from 90% to 10%. Where t_r and t_f are very much smaller than the PW, the pulse does indeed appear to have perfectly vertical sides. Some pulse generators include facilities for adjusting the rise and fall time of the output pulses. When an external triggering facility is included, an adjustable time delay may also be provided. The *delay time* (t_d in Figure 15-13), is the time between the trigger input and commencement of the output pulse.

The same precautions that are observed when using sine wave signal generators also apply to the use of pulse generators. One additional point is that the selected PW must always be less than the time period of the pulse

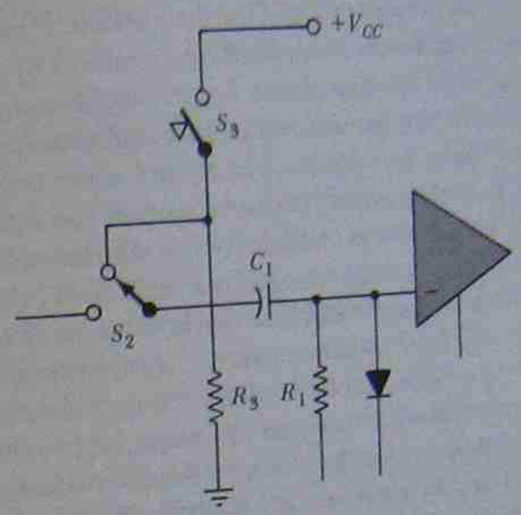


FIGURE 15-12. Modification to Figure 15-10 for manual triggering.

frequency (or pulse repetition rate). Where this is not the case, the frequency is changed by a factor of 2 or more. To correctly set up a desired output frequency and PW, it is best to display the pulse generator output on an oscilloscope. Adjust the PW control as required, and then adjust the frequency control to give the desired output frequency. If the PW is just slightly less than the time period, it is best to start with a PW of

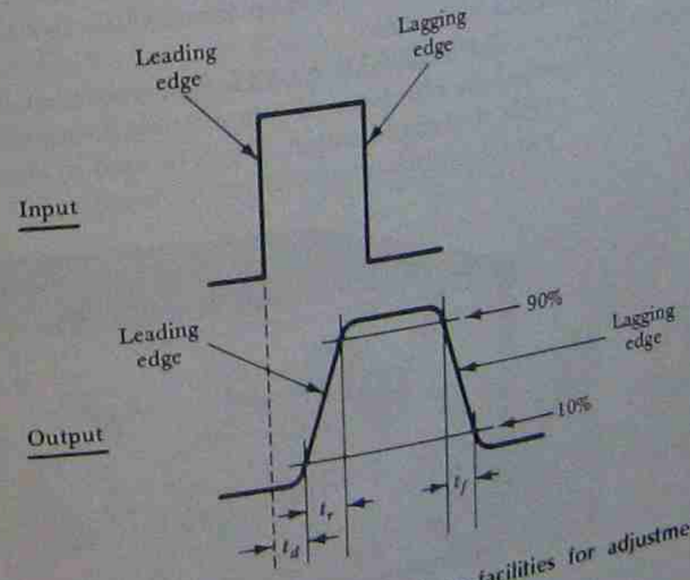


FIGURE 15-13. Many pulse generators have facilities for adjustment of: delay time (t_d), rise time (t_r), and fall time (t_f).

approximately half the time period. Next, adjust for the required frequency, and finally reset the PW.

The commercial function/pulse generator in Figure 15-14 can generate sine, square, and triangular waveforms as well as normal or inverted pulse waveforms. The square wave output is symmetrical about ground level; however, positive and negative square waves are also available, as is a dc voltage level. All of the above are taken from the FUNCTION OUT terminal and selected by the FUNCTION switch. A SYNC OUT terminal is included, and four logic outputs (for ECL—*emitter coupled logic*—and TTL—*transistor transistor logic*) are also provided.

The output frequency ranges from 0.0001 Hz to 20 MHz. This is switched through decade steps, and is continuously variable at each step. The amplitude of output waveforms is a maximum of 30 V peak-to-peak, and by attenuator selection can be reduced in steps to 3 mV. A dc offset up to +15 V can be applied to all outputs from the FUNCTION OUT terminal.

When used as a pulse generator, the output PW can be varied from 25 ns to 1 ms. Here again, the range can be switched in decade steps, and PW is continuously variable for each range. The pulse output can be continuous triggered, manually triggered, or gated by an external triggering source (applied to the TRIG IN terminal). A variable pulse delay can also be introduced, and repetitive double pulses with a variable intervening space can be generated. The frequency and time period of outputs can be varied through a ratio as great as 1000 : 1 by dc or ac inputs applied to the VCG IN terminal.

The TRIGGER START/STOP control is used only with sine and triangular waveforms. This sets the starting and stopping points during the cycle of triggered output. It can be used in conjunction with the dc offset control to produce unusual output waveforms.



FIGURE 15-14. Pulse/function generator (Courtesy of WAVETEK).

15-4 RF SIGNAL GENERATORS

A *radio frequency* (RF) signal generator has a sinusoidal output with a frequency range somewhere in the 100 kHz to 40 GHz region. Basically the instrument consists of an *RF oscillator*, an *amplifier*, a *calibrated attenuator*, and an *output level meter*. Figure 15-15 shows the signal generator block diagram. The RF oscillator has a continuous frequency control and a frequency range switch, to set the output to any desired frequency. The amplifier includes an output amplitude control. This allows the voltage applied to the attenuator to be set to a *calibration point* on the output level meter. The output level must always be reset to this calibration point every time the frequency is changed. This is necessary to ensure that the output voltage levels are correct, as indicated on the calibrated attenuator.

The oscillator circuit used in an RF signal generator is usually either a *Hartley oscillator* or *Colpitts oscillator*. The basic circuits of both types are shown in Figure 15-16. Both circuits consist of an *amplifier* and a phase-shifting *feedback network*. As well as amplifying the input signal the amplifier inverts it, or phase shifts it, through 180°. The amplified output is attenuated and phase shifted through a further 180° by the feedback network. Then it is applied to the amplifier input terminals. The gain of the amplifier equals the reciprocal of the feedback network attenuation. Thus, each oscillator circuit has a *loop gain* of 1 and a *loop phase shift* of 360°, which are the requirements for sustained oscillation.

The essential differences between the Hartley and Colpitts circuits are in the phase shift networks. The Hartley circuit uses two inductors and a capacitor: L_1, L_2, and C in Figure 15-16(a). The Colpitts circuit uses two capacitors and one inductor: C_1, C_2, and L in Figure 15-16(b). Capacitors C_C in both circuits are coupling capacitors. In the Hartley circuit, the base

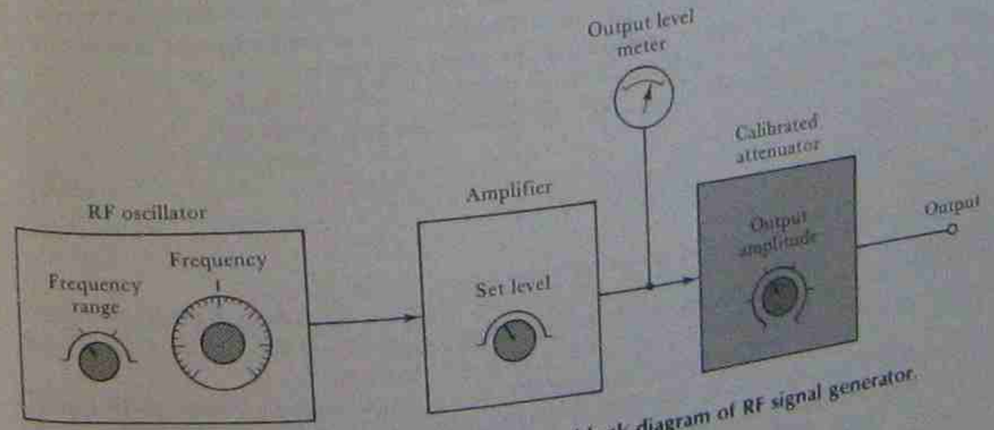
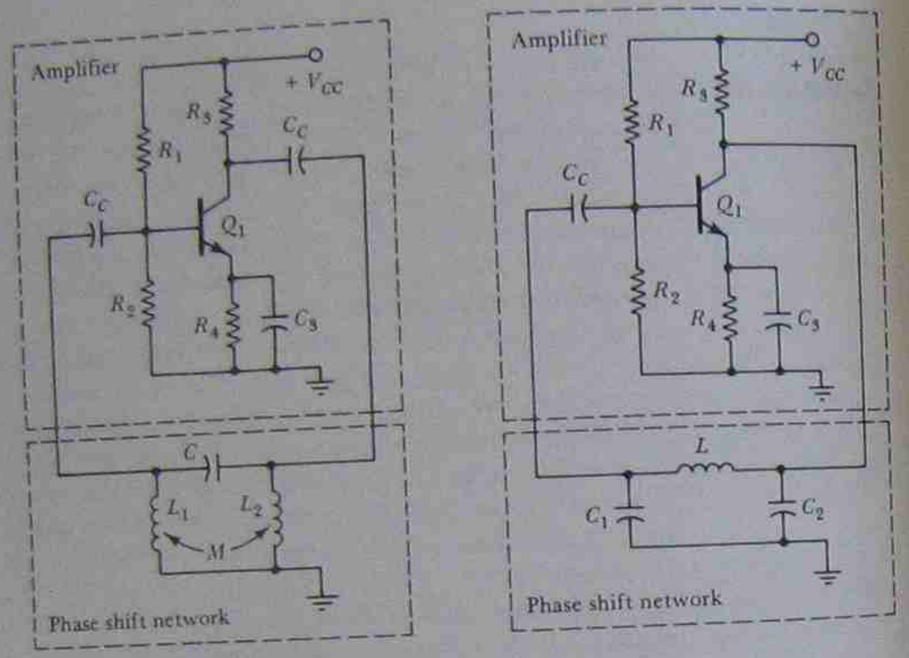


FIGURE 15-15. Basic block diagram of RF signal generator.



(a) Hartley oscillator (b) Colpitts oscillator

FIGURE 15-16. Transistor oscillator circuits suitable for use in RF signal generators.

and collector terminals of transistor Q_1 would be shorted to ground via L_1 and L_2 if the coupling capacitors were not included. In the Colpitts circuit, the transistor collector and base terminals would be shorted together via L, if C_C was not in the circuit. The frequency of oscillations for both circuits is the resonant frequency of the phase shift network:

$$f = \frac{1}{2\pi\sqrt{C_T L_T}}. \tag{15-8}$$

For the Hartley circuit, $C_T = C$, and L_T is the total inductance of L_1 and L_2, including the mutual inductance. For the Colpitts circuit, $L_T = L$, and C_T is the total capacitance of C_1 and C_2 in series.

The oscillating frequency of the two circuits in Figure 15-16 can be altered by changing the component values in the phase shift network. Figure 15-17 shows how this is usually done for a Hartley circuit. Switch S_1 selects various inductor values to change the frequency range, while

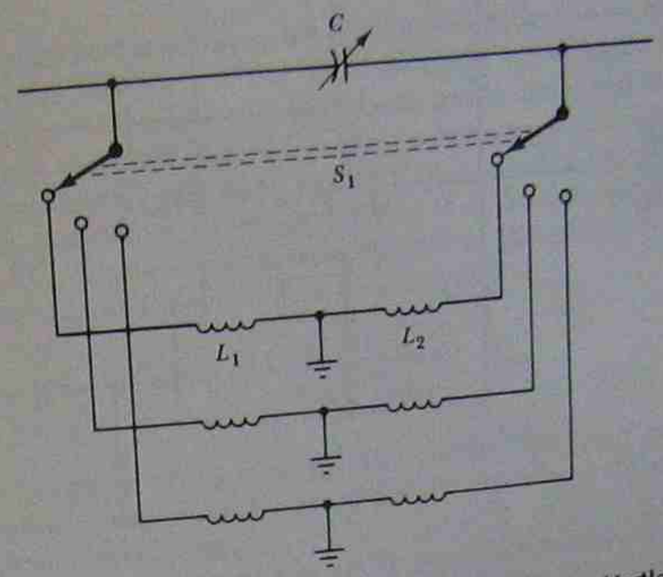


FIGURE 15-17. Arrangement for frequency changing in the Hartley oscillator circuit.

variable capacitor C permits continuous frequency variation over any selected range.

Most RF signal generators include facilities for amplitude modulation and frequency modulation of the output. Amplitude modulation is easily accomplished at the amplification stage. Figure 15-18 shows a basic circuit for this purpose. If field effect transistor Q_2 were not present in the circuit, the amplifier gain would be

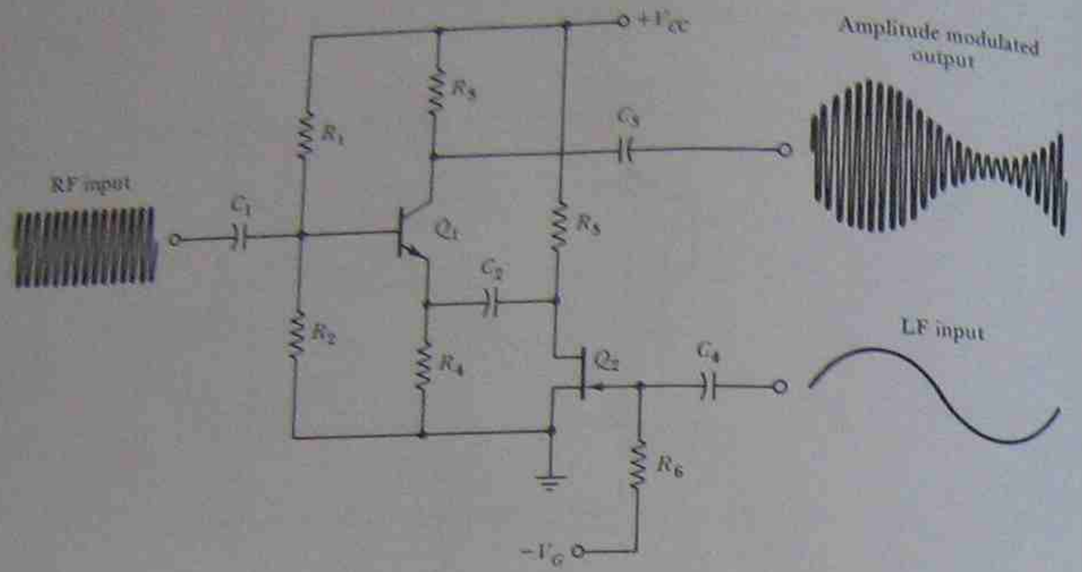
$$A_v = \frac{R_3}{R_4}.$$

Q_2 is capacitor coupled to R_4 via C_2, so that it has no effect on the dc bias condition in the circuit of Q_1. With Q_2 in the circuit the amplifier gain becomes

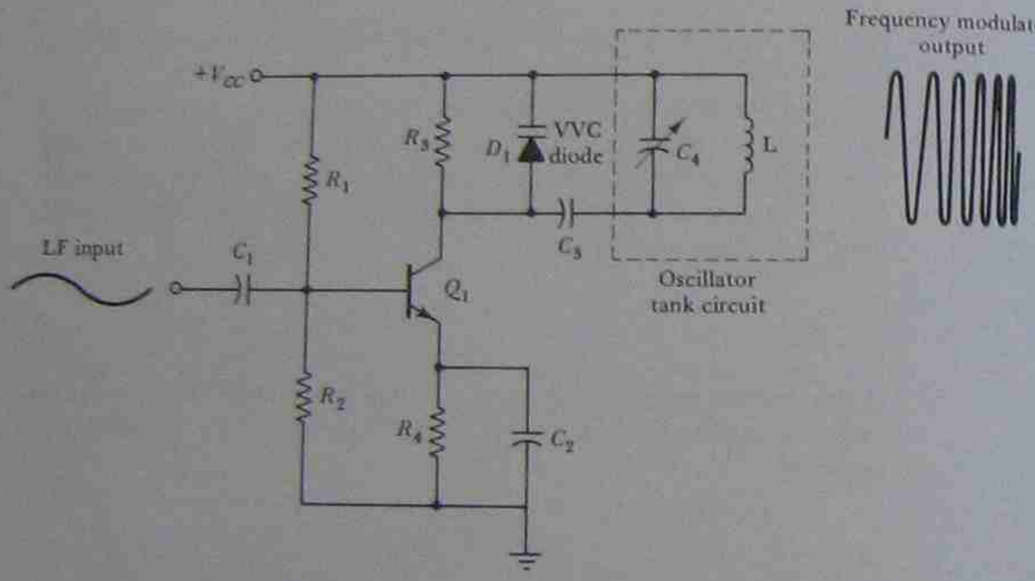
$$A_v = \frac{R_3}{R_4 \| R_D},$$

where R_D is the drain resistance of the FET. The low frequency signal applied to the gate of the FET varies the drain resistance of Q_2, and consequently varies the gain of the amplifier. In this way the amplitude of the RF output is increased and decreased in phase with the low frequency input [see the waveforms in Figure 15-18(a)].

Frequency modulation is usually performed at the oscillator stage of an RF signal generator. One method of frequency modulating the oscillator output uses a *variable voltage capacitor diode* (VVC diode). This is a



(a) Basic circuit for amplitude modulation



(b) Basic frequency modulation circuit

FIGURE 15-18. Basic circuit arrangements for amplitude modulation and frequency modulation in RF signal generator.

specially constructed semiconductor diode operated in reverse bias. Varying the reverse bias on a VVC diode alters its capacitance. In Figure 15-18(b), Q_1 and its associated components can be employed to vary the voltage across the VVC diode (D_1) when a low frequency input signal is applied. Capacitor C_3 couples D_1 to the LC tank circuit of the oscillator. C_3 has a large capacitance, so the capacitance of D_1 is essentially in parallel with L and C_4. The tank circuit capacitance is the diode capacitance C_D in parallel with C_4, and the resonance frequency is

$$f = \frac{1}{2\pi\sqrt{L\,C_D \| C_4}}.$$

As the capacitance of D_1 is varied, the resonant frequency of the tank circuit varies. Thus, the oscillator output frequency is modulated by the low frequency input signal.

A complete block diagram of an RF signal generator is illustrated in Figure 15-19. The basic components from Figure 15-15 (oscillator, amplifier, meter, and attenuator) are reproduced in Figure 15-19, together with FM and AM internal modulating sources. Switches S_1 and S_2 allow selection of *no modulation*, as well as internal or external FM or AM modulation. Note that each section of the system is usually shielded by enclosing it in a metal box. The whole system is then completely shielded. The purpose of this is to prevent RF interference between the components, and to prevent the emission of RF energy from any point except the output terminals. The power line is also decoupled by means of RF chokes and capacitors (see Figure 15-19) to prevent RF emissions on the power line.

Although the RF signal generator in Figure 15-19 has an output level meter, the actual output voltage from the calibrated attenuator is the indicated level only when the instrument is correctly loaded. If a 75-Ω load is specified, then a 75-Ω load must be connected for the attenuator output to be correct [Figure 15-20(a)]. Where the load is other than the specified load for the signal generator, parallel or series resistors must be included to modify the load as necessary [Figure 15-20(b)]. When series-connected resistors are involved, the signal generator output is further attenuated, and the actual signal level applied to the load must be calculated [Figure 15-20(c)].

A typical commercially available RF generator has an output frequency extending from 0.15 MHz to 50 MHz in eight ranges. The frequency error is less than 1%, and the output impedance is 75 Ω. When connected to a 75-Ω load, the output voltage is 50 mV and can be attenuated by up to 80 dB. Amplitude modulation may be performed to a depth of 30% by an internal 1-kHz source, or by an external source with a frequency of 20 Hz to 20 kHz. Internal frequency modulation may be performed by an internal source which is either the power frequency or 1

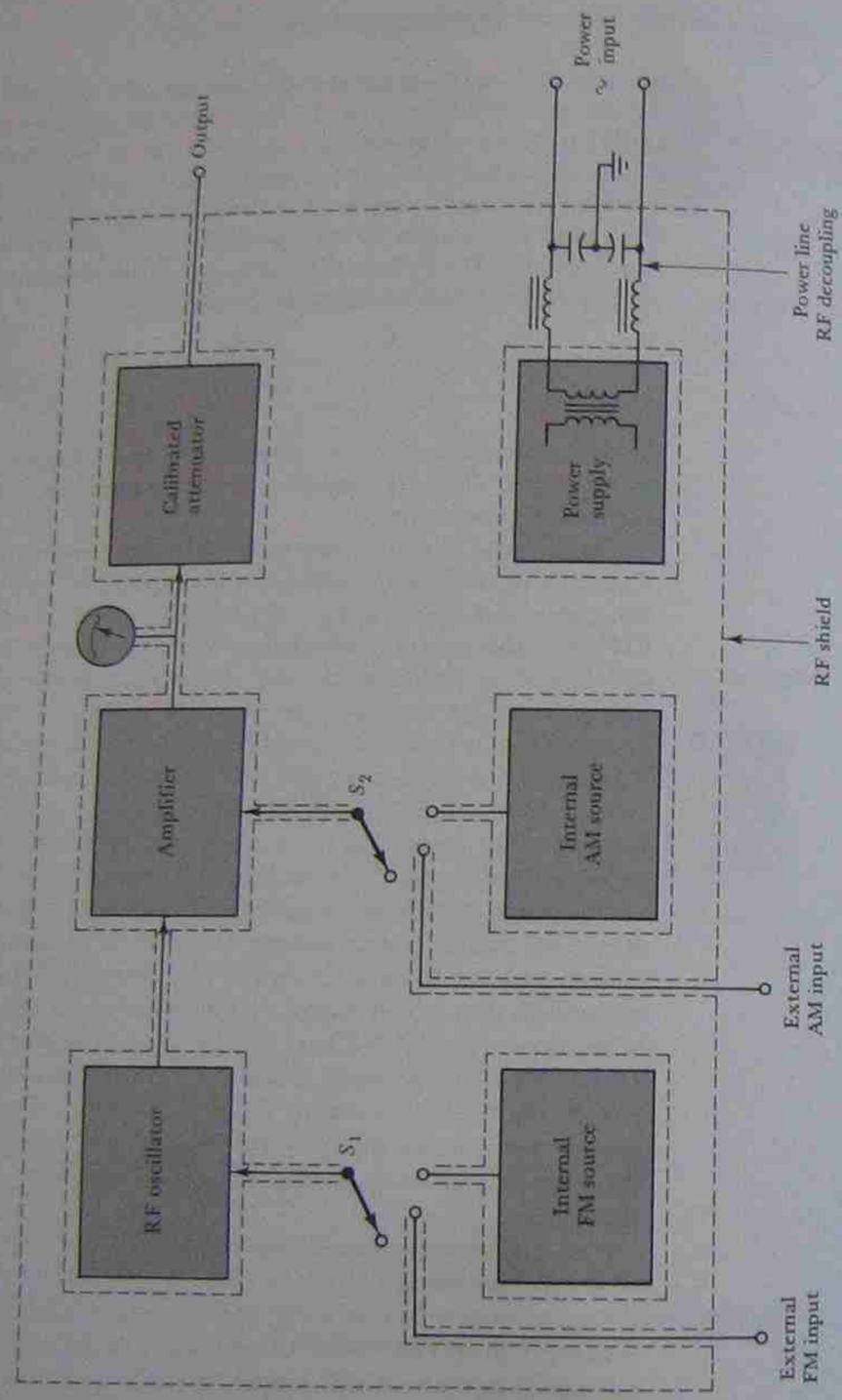
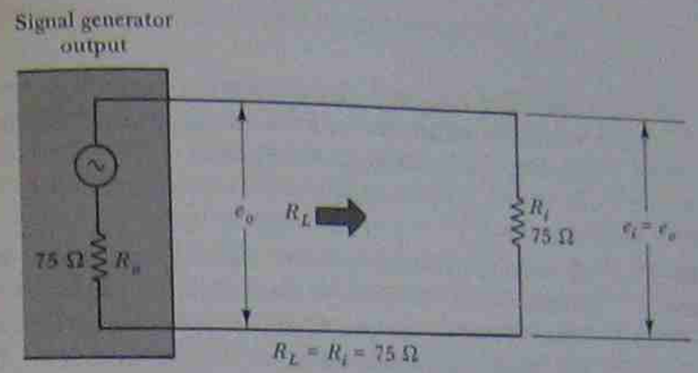
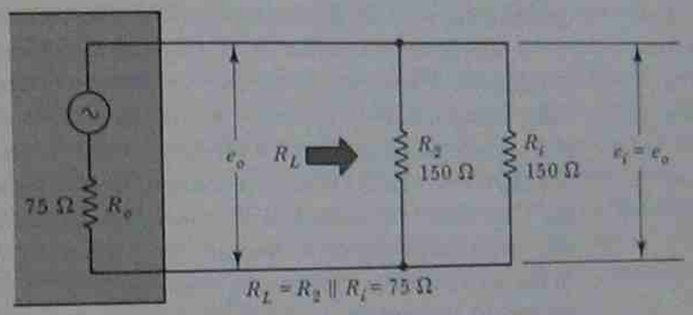


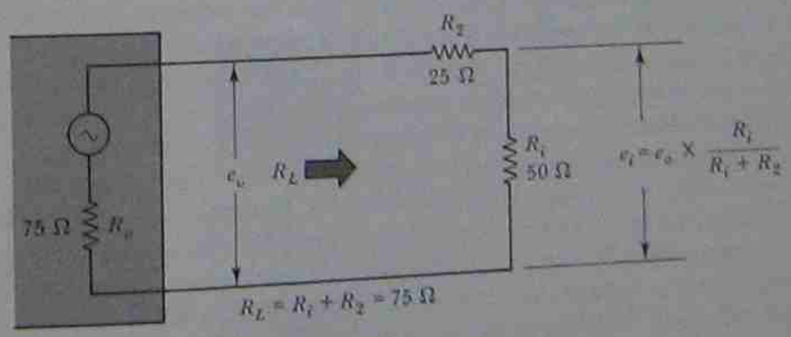
FIGURE 15-19. Complete block diagram of RF signal generator.



(a) When $R_L = R_o$, the output is as specified



(b) When $R_L > R_o$, a parallel resistor must be included to make $R_L = R_o$



(c) When $R_L < R_o$, a series resistor must be connected to make $R_L = R_o$

FIGURE 15-20. An RF signal generator with an output level meter and a calibrated attenuator must be correctly loaded.

kHz. The frequency change effected depends upon the selected output frequency range. An external frequency modulating source can also be used with a frequency of 0 to 5 kHz.

15-5 SWEEP FREQUENCY GENERATORS

A major application of sine wave generators is testing the frequency response of amplifiers and filter circuits. This is performed by setting the signal generator output through a series of frequencies while maintaining the output amplitude constant. The amplitude of the output from the circuit under test is measured at each frequency. These output levels are then plotted versus frequency to give a frequency response graph for the circuit under test. The process can be simplified and speeded up by using a signal generator that automatically varies its frequency over a predetermined range. Such an instrument is known as a *sweep frequency generator*.

A very much simplified block diagram of a sweep frequency generator is shown in Figure 15-21. A *ramp generator* (or *sweep generator*) applies a linear ramp voltage to the input of a *voltage tuned oscillator*. The basic circuit of a voltage tuned oscillator is similar to the frequency modulation circuit in Figure 15-18(b). As the ramp voltage level increases, the reverse bias on the VVC diode increases, and this causes its capacitance to decrease. Thus the resonance frequency of the tank circuit (which is the oscillator output frequency) increases as the ramp voltage grows. When the ramp voltage returns to its zero level, the diode capacitance and oscillator frequency return to their starting levels. The range over which the oscillator frequency is swept is determined by selection of L and C_4 in Figure 15-18(b).

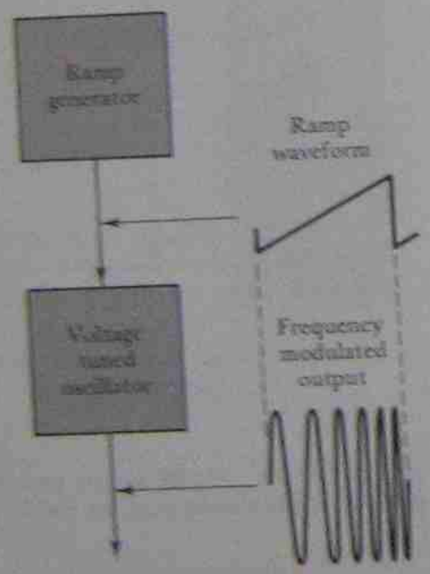


FIGURE 15-21. Basic sweep frequency generator.

A more complete block diagram of a sweep frequency generator is illustrated in Figure 15-22. It should be noted that Figure 15-22 is still to some extent a simplified diagram compared to the block diagrams of commercially available sweep frequency generators. The illustration shows that the ramp waveform output of the sweep generator is amplified and then applied to the voltage tuned oscillator (VTO). As well as going to the next amplifier stage, the VTO output is also applied to a *discriminator*. The discriminator produces an output voltage which is proportional to its input frequency. Because, the discriminator input is the swept frequency from the VTO, its output is a ramp voltage similar to the ramp from the sweep generator. This ramp from the discriminator is applied as an input to the *differential amplifier*. While the VTO output frequency sweeps over the correct range of frequencies, the ramp from the discriminator balances the ramp from the sweep generator. If the VTO output frequency is lower than it should be at any instant, the instantaneous output voltage from the discriminator drops below the instantaneous level of the ramp voltage from the sweep generator. This results in an increased output voltage from the differential amplifier, which causes the VTO output frequency to increase. Similarly, if the VTO output frequency becomes higher than intended, the discriminator output voltage rises above the level of the sweep generator voltage. In this case, the differential amplifier output decreases, and produces a lower VTO output frequency. In this way, the output frequency of the VTO is stabilized.

As well as producing an output frequency that sweeps over a desired band of frequencies, the sweep frequency generator must have a stable output voltage level. It is very important that the output voltage remains constant at whatever level it is set, over the entire range of output frequencies. The output voltage level is stabilized by the action of the *automatic level control* (ALC) circuit and the *variable gain amplifier*. The ALC circuit produces a voltage proportional to the power output of the variable gain amplifier. This voltage is compared to an internal reference voltage in the ALC circuit, and the difference between the two is applied to the variable gain amplifier. Where the power output is lower than required, the amplifier gain is increased. If the power output is too high, the gain is decreased. In this way, the power input to the calibrated attenuator is stabilized. The attenuator offers a constant input resistance, so the constant input power means that the input voltage is constant. Thus, the output voltage from the attenuator remains constant at all frequencies.

The output amplitude from the sweep frequency generator is adjusted by means of the calibrated attenuator. The range of output frequency may be altered by altering the amplitude of the ramp from the sweep generator. Alternatively, the VTO output frequency might be changed by modifying the parameters of the discriminator. For example, if the discriminator output is potentially divided to half its normal level, the VTO output frequency must double in order to make the discriminator output equal to

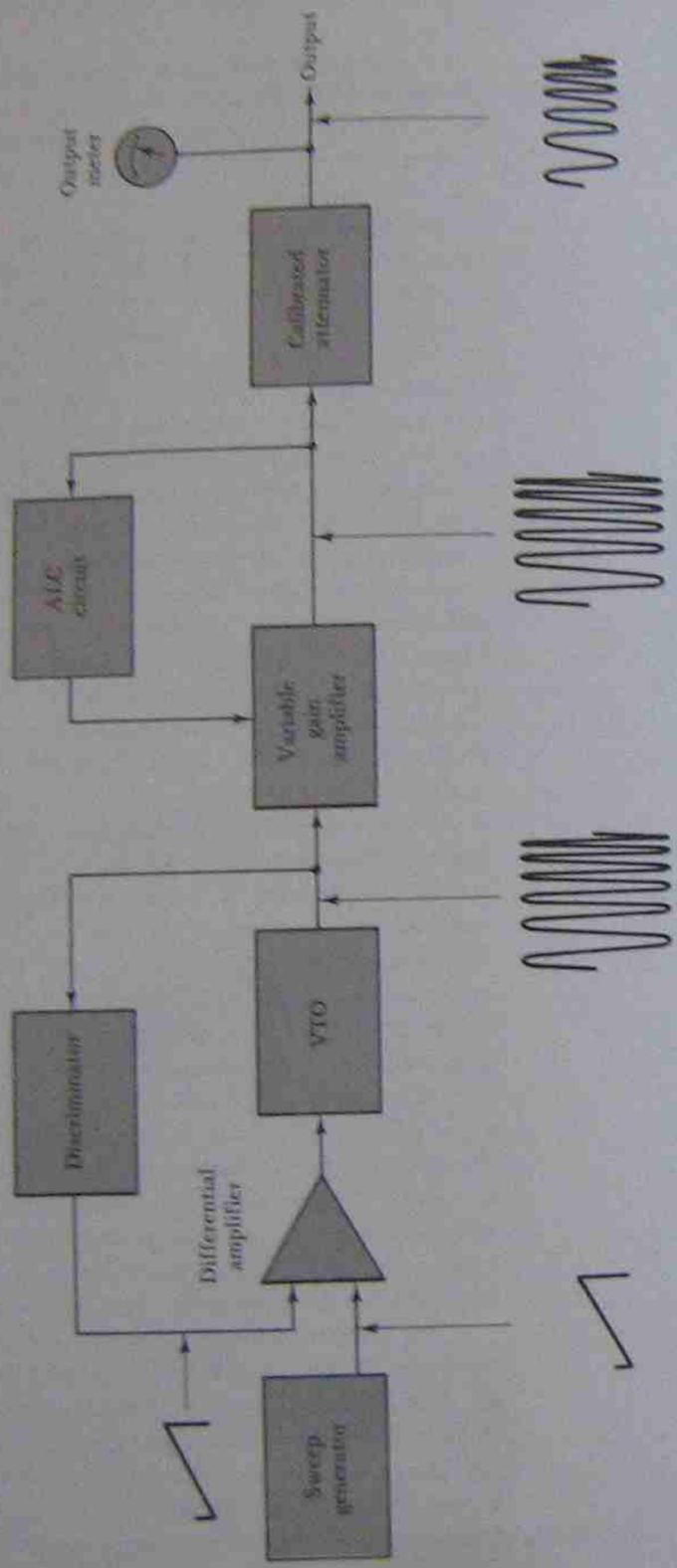


FIGURE 15-22. Block diagram of sweep frequency generator.

the sweep generator ramp voltage. Similarly, if the sweep generator output voltage is doubled, the VTO output frequency must double.

In addition to the controls described above, commercially available sweep frequency generators usually have facilities for adjusting the rate of change of the output frequency, and for triggering the sweep from an external source. The sweep can also be arranged to commence at a particular frequency, or to be symmetrical about a selected center frequency. An output voltage directly proportional to the instantaneous frequency is also usually provided. This can be employed for horizontally deflecting the trace on an oscilloscope used for displaying the characteristics of a circuit under test.

Figures 15-23 and 15-24 show two sweep frequency generators designed for different applications. The HP 8601A in Figure 15-23 is an RF sweep generator with an output frequency ranging from 0.1 MHz to 110 MHz. The output frequency may be constant, or may be swept over part or all of two bands: 0.1 MHz to 11 MHz and 1 MHz to 110 MHz. The selected sweep can be: SYM (symmetrical above and below a selected center frequency), VIDEO (from the lowest frequency in the band to a selected maximum frequency), and FULL (over the entire band of frequencies). In all cases the selected (center or top) frequency is displayed digitally on the instrument's control panel. The symmetrical sweep width is selected by means of the SYM SWEEP WIDTH control. The sweep speed may be set to: FAST (6 to 60 sweeps per second) or SLOW (8 to 80 seconds per sweep). The frequency can also be manually adjusted over the selected range. The sweep can be set to run continuously (FREE), be triggered at the line frequency (LINE), or be triggered manually by push button (TRIG). The meter indicates the actual RF output level in dBm or



FIGURE 15-23. Front panel of RF sweep frequency generator (Courtesy of Hewlett-Packard).



FIGURE 15-24. Low-frequency sweep generator that operates over the range of 0.1 Hz to 1 MHz (Courtesy of Philips Electronics).

in rms volts into a 50-Ω load. Internal and external AM and FM modulation facilities are provided, and an output voltage proportional to instantaneous output frequency is available.

The PM 5165 sweep generator shown in Figure 15-24 operates over a much lower range of frequencies than the HP 8601A. While the HP 8601A is intended for testing RF circuits, the PM 5165 is designed for use with circuits which operate at frequencies less than 1 MHz. The actual range available is 0.1 Hz to 1 MHz, and the frequency can be controlled by an internal sweep generator, or controlled by an external signal. Sine, square, or triangular output waveforms are available, with a maximum output amplitude of 6 V *p*-to-*p* adjustable down to approximately 200 mV *p*-to-*p*.

The output frequency from the PM 5165 can be made to sweep over a wide range of frequencies. Using the internal sweep generator, the ratio of high to low frequencies (f_H/f_L) can be set from 1 : 1 to 10^4: 1. With the digital display and the coarse and fine controls, the high and low frequencies can be set very accurately. Sweep times continuously adjustable between 1 s and 100 s are available, and the sweep may be triggered manually on each cycle or set to continuously repeat. Alternatively, an external sweep may be used. An output voltage proportional to the log of the output frequency is available. This is very useful when displaying a circuit frequency response on an oscilloscope, or when tracing the response on an *XY* recorder.

15-6 THE FREQUENCY SYNTHESIZER

The output frequency of the transistor oscillator circuits shown in Figure 15-16 can be made very stable by substituting a piezoelectric crystal in place of one of the coupling capacitors. The crystal offers a high impedance to all frequencies except its own resonance frequency. Thus, the

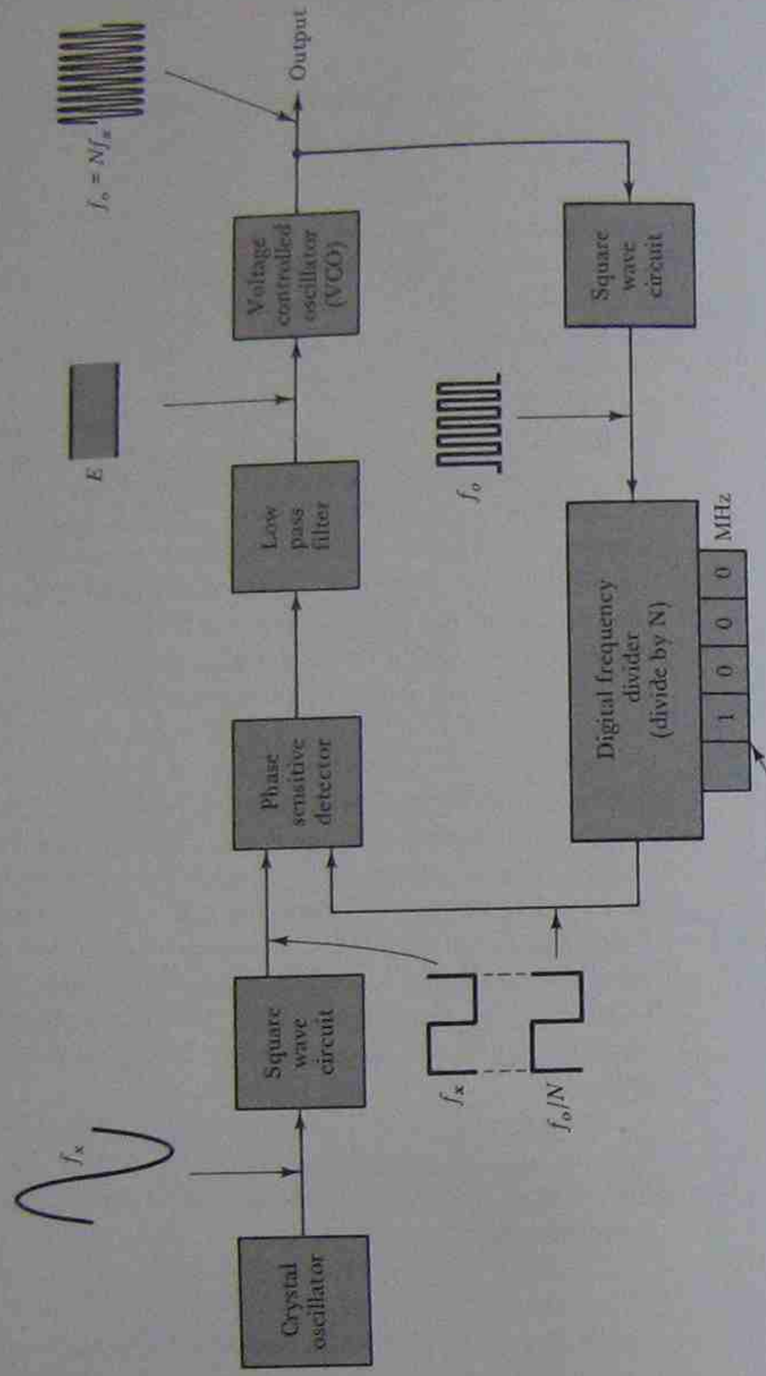
circuit can oscillate only at the resonance frequency of the crystal, which is an extremely stable quantity. The one disadvantage of the crystal oscillator is that its output frequency cannot normally be adjusted. However, the frequency can be altered by using the oscillator as part of a *frequency synthesizer*. In a frequency synthesizer, the output frequency of a crystal oscillator is multiplied by a factor (N) which may be set by a bank of switches. The switches are located on the front panel of the instrument, and are labeled in a way that allows them to be set to indicate the desired output frequency. The system employed to multiply the oscillator frequency is known as a *phase locked loop* (PLL).

The block diagram of a PLL system as used in a frequency synthesizer is illustrated in Figure 15-25. The output of the crystal oscillator is converted into a square wave and is then fed into one input of a *phase sensitive detector*. The other input of the phase sensitive detector has another square wave applied to it, as illustrated. As will be explained, the frequencies of these two square waves are identical, and they are exactly in phase. The output of the phase sensitive detector is a dc voltage which is passed through a *low pass filter* to a *voltage controlled oscillator* (*VCO*). The VCO output frequency is directly proportional to the dc voltage level (E) at its input terminal. The VCO produces the instrument output frequency, and this may be passed through another stage to stabilize its amplitude before applying it to the output attenuator. As illustrated, the output of the VCO is fed to a circuit which converts it into a square wave for triggering a *digital frequency divider*. The frequency divider operates in the manner described in Section 10-1, and the ratio (N) by which it divides the VCO frequency is set by a bank of switches. These switches are usually *thumb wheel type* which numerically indicate their condition. They are connected in such a way that the displayed number is the factor N by which the output frequency is divided before being applied to the phase sensitive detector.

Suppose the crystal oscillator output frequency is $f_x = 1$ MHz, and that the output of the digital frequency divider is also exactly 1 MHz. If the switches are set to divide the VCO output by $N = 1000$, the VCO frequency must be:

$$\begin{aligned} f_v &= Nf_x \\ &= 1000 \times 1 \text{ MHz} \\ &= 1000 \text{ MHz}. \end{aligned}$$

Thus, the dc input voltage to the VCO must have the appropriate level to produce the 1000 MHz output frequency. Now suppose the output frequency increases slightly above 1000 MHz. The frequency divider output is still $f_v/1000$, and this is now greater than $f_x = 1$ MHz. The difference between f_x and f_v/N now causes the phase sensitive detector output voltage to fall to a lower level than before. This lower input voltage



Frequency selection switches

FIGURE 15-25. Phase-locked loop system used in a frequency synthesizer.

to the VCO reduces f_o back toward 1000 MHz. Similarly, if f_o falls below 1000 MHz, the frequency divider output becomes lower than 1 MHz. With f_o/N less than f_x, the detector output voltage increases and returns the VCO frequency toward 1000 MHz once again.

It is seen that the VCO output frequency is stabilized at exactly N times the crystal frequency. With $f_x = 1$ MHz and $N = 1000$, f_o is 1000 MHz. If the frequency ratio is now set to 2345, the output frequency is stabilized at $f_o = 2345 \times f_x$. The output frequency of the synthesizer can be set to any multiple of the crystal oscillator frequency simply by selecting the desired frequency divider ratio.

REVIEW QUESTIONS AND PROBLEMS

15-1. Sketch the circuit of a Wein bridge oscillator. Explain the circuit operation, and write equations for output frequency and amplifier gain.

15-2. Show how modifications should be made to the Wein bridge circuit in Question 15-1 for: (a) output amplitude stabilization, and (b) frequency control. Explain the effect of each modification.

15-3. A Wein bridge oscillator circuit, as shown in Figure 15-1(a), has $C_1 = C_2 = 250$ nF and $R_1 = R_2$ variable from 200 Ω to 3 kΩ. Calculate the maximum and minimum output frequencies. Also determine the new capacitor values required to adjust the output frequency to a maximum of approximately 300 Hz.

15-4. In the Wein bridge circuit modification shown in Figure 15-1(b), $R_4 = 390$ Ω, $R_5 = 470$ Ω and $R_6 = 330$ Ω. Calculate the maximum amplitude of the output voltage.

15-5. Sketch the circuit of a two-range adjustable output attenuator for use with a sinusoidal oscillator. Explain the operation of the circuit.

15-6. Sketch a sine to square wave conversion circuit using an amplifier and clipper. Explain the circuit operation.

15-7. The attenuator circuit in Figure 15-2(a) is to give output voltage ranges of (0–0.3) V and (0–3) V. If the input voltage from the oscillator has an amplitude of 6 V, determine R_1, R_2, and R_3. Assume that the op-amp has an input bias current of 300 mA.

15-8. Sketch the block diagram of a sine/square wave signal generator. Briefly explain.

15-9. Sketch a circuit showing how a low-frequency signal generator is used to test an audio amplifier. Briefly explain.

15-10. Sketch a basic function generator circuit for producing triangular and square waveforms. Explain the circuit operation, and show a modification for frequency range changing.

15-11. The Schmitt trigger circuit in Figure 15-6(a) has $R_3 = 2.7$ kΩ, $R_4 = 15$ kΩ, and $V_{CC} = \pm 12$ V. Calculate the upper and lower trigger points for the circuit.

15-12. If R_3 in Question 15-11 is made adjustable from 2.7 kΩ to 3.2 kΩ, calculate the adjustment range of the trigger points.

15-13. The integrator circuit in Figure 15-6(a) has $R_1 = 500\ \Omega$, $R_2 = 4.7$ kΩ, and $C_1 = 0.3\ \mu$F. If the Schmitt trigger circuit has ±1 V trigger points, calculate the output frequency when the moving contact of R_1 is at its center point. The supply voltages are $V_{CC} = \pm 12$ V.

15-14. The integrator in Question 15-13 is connected together with the Schmitt trigger circuit in Question 15-11 to form a function generator. Calculate the peak-to-peak amplitude and the frequency of the triangular output waveform.

15-15. Sketch a diode loading circuit for converting a triangular waveform into a sine wave. Explain the circuit operation.

15-16. Sketch the block diagram of a basic function generator. Briefly explain.

15-17. List the important items in the specifications for low-frequency sine/square wave generators and function generators. Briefly explain each item.

15-18. Sketch the circuit of an IC op-amp astable multivibrator for use as a square wave generator. Sketch the circuit waveforms, and explain the operation of the circuit.

15-19. The astable multivibrator in Figure 15-9 has $R_1 = 12$ kΩ, $R_2 = 4.7$ kΩ, $R_3 = 3.3$ kΩ, and $C_1 = 0.3\ \mu$F. The supply voltage is $V_{CC} = \pm 9$ V. Calculate the frequency of the square wave output.

15-20. Sketch the circuit of an IC op-amp monostable multivibrator. Show the waveforms at various points in the circuit, and explain the circuit operation.

15-21. Show how the circuit in Question 15-20 should be modified for manual triggering. Briefly explain.

15-22. A monostable multivibrator, as shown in Figure 15-10, has $R_1 = 15$ kΩ, $R_2 = 15$ kΩ, $C_1 = 100$ pF, $C_2 = 0.02\ \mu$F. The supply and bias voltages are $V_{CC} = \pm 12$ V and $V_B = +1.5$ V. Calculate the width of the output pulse.

15-23. Sketch an attenuator and a dc offset control circuit for use with a pulse generator. Explain the operation of the circuit.

15-24. Sketch pulse waveforms showing delay time, rise time, and fall time. Briefly explain. Also discuss any precautions that should be observed in using a pulse generator.

15-25. Sketch the basic block diagram of an RF signal generator. Explain.

15-26. Sketch the circuits of Hartley and Colpitts oscillators, and explain the operation of each. Write the equation for oscillating frequency, and discuss how the frequency can be altered.

15-27. Sketch a basic circuit for amplitude modulation of the output of an RF oscillator. Show the circuit waveforms, and explain the circuit operation.

15-28. Sketch a basic circuit for frequency modulating the output of an RF oscillator. Show the circuit waveforms and explain the operation of the circuit.

15-29. Sketch the complete block diagram of an RF signal generator and explain its operation. Discuss the performance of a typical RF signal generator and the need for correct loading.

15-30. Sketch the basic block diagram of a sweep frequency generator and explain its operation.

15-31. Sketch the complete block diagram of a sweep frequency generator. Show the waveforms at various points in the system. Explain the operation of each section and the overall system operation.

15-32. Define a frequency synthesizer. Sketch the block diagram of a phase locked loop system as used in a frequency synthesizer. Carefully explain the operation of the system.

16

MISCELLANEOUS INSTRUMENTS

INTRODUCTION The three instruments discussed in this chapter are: the distortion analyzer, the *Q* meter, and the spectrum analyzer.

The distortion analyzer measures the total harmonic distortion content in an input signal. Either a percentage scale or a dB scale may be used to indicate the distortion in relation to the complete input signal rms level. Although mainly for audio use, this instrument can handle signal frequencies up to 600 kHz.

In contrast to the distortion analyzer, the *Q* meter is a radio frequency instrument. Its function is to measure the *Q* factor of coils that must operate at radio frequencies. It can also measure inductance, capacitance, and resistance.

A spectrum analyzer uses a CRT type display. However, instead of displaying signal amplitude plotted to a base of time, as is done in an oscilloscope, amplitude is plotted to a base of frequency. Input signals are first separated into their frequency components. Then each component is displayed as a vertical line on the screen. The height of each line represents the amplitude of the particular component, and its horizontal position represents frequency.

16-1 DISTORTION ANALYZER

A sine wave input signal applied to an amplifier or other circuit may produce an output that is not purely sinusoidal. No matter how severe the

16-1-1 Harmonic Distortion

distortion, it can be shown that all repetitive waveforms consist of a *fundamental* frequency component and a number of *harmonics*. The fundamental is a large amplitude sine wave with the same frequency as the distorted repetitive wave. The harmonics are sine waves with frequencies that are multiples of the fundamental frequency (f). A second harmonic has a frequency of $2f$, a third harmonic has a frequency of $3f$, etc.

Distortion in a waveform can be measured in terms of its harmonic content. One method of determining the harmonic content is to suppress the fundamental frequency and measure the rms value of the combined harmonics. This may then be expressed as a percentage of the rms level of the complete waveform, (i.e., fundamental and harmonics). Alternatively, a decibel (dB) scale (see Section 3-7) may be used to indicate the harmonic distortion content.

16-1-2 Rejection Amplifier

The basic component of a *fundamental-suppression harmonic analyzer* is a *rejection amplifier*. The rejection amplifier must heavily attenuate the fundamental frequency of the waveform to be analyzed. It must also pass all harmonics with a constant gain and no alteration in their phase relationship. Some type of *notch filter* must be employed within the circuit to reject the fundamental while passing the harmonics. Facilities must be included to adjust the filter to any one of a wide range of frequencies. To achieve the constant gain and phase relationship for the harmonics, the amplifier must have a high internal (*open-loop*) gain and must use overall *negative feedback* (NFB).

The rejection amplifier circuit in Figure 16-1 has two stages of amplification. These are identified as the *preamplifier* and the *bridge amplifier*. A Wein bridge circuit (see Section 15-1) is also included to operate as a notch filter. Negative feedback is provided from the output of the bridge amplifier to the input stage of the preamplifier. The two stages of amplification provide a high open-loop gain, and the NFB stabilizes the closed-loop gain at approximately 1 dB.

Reference to Section 15-1 shows that the Wein bridge balances at only one frequency. When balance is achieved, the output voltage at the bridge null detector is a minimum. In the rejection amplifier, the bridge output is taken from the null detector terminals, and the input (from the preamplifier) is connected to the bridge supply terminals. When the bridge is balanced, the (balance frequency) output to the bridge amplifier is a minimum. Signals at frequencies other than the bridge balance frequency are only slightly attenuated.

The frequency-dependent components of the bridge may be adjusted to tune to any desired fundamental frequency. Component switching is also normally provided so that the frequency range may be changed. When the bridge is balanced, the fundamental frequency (to which it is adjusted) is

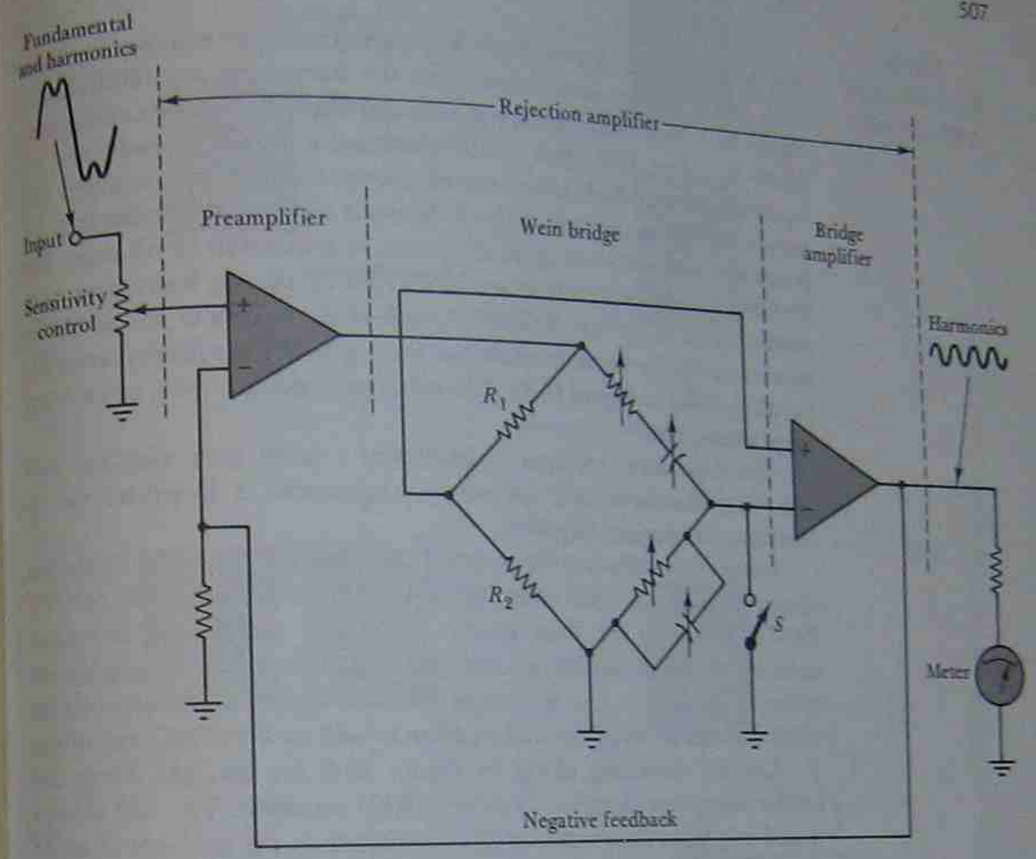


FIGURE 16-1. Basic circuit of a fundamental-suppression harmonic analyzer.

attenuated by approximately 80 dB. Thus, despite the gain of the preamplifier and the bridge amplifier, the fundamental frequency output is negligible. However, as already explained, all harmonics of the fundamental are passed without any added distortion.

When switch S is closed in Figure 16-1, one of the (null detector) output terminals of the bridge is grounded. Now, only the output from the junction of resistors R_1 and R_2 is passed to the bridge amplifier. The frequency-dependent components are grounded (via S), and the signal is only slightly attenuated by R_1 and R_2. Thus, the entire waveform (fundamental and harmonics) is passed to the meter. The input *sensitivity* control can now be adjusted to give a convenient scale reading on the meter. With S open-circuited once again, the fundamental frequency is suppressed by the bridge, and only the harmonics are passed to the meter. The rms value of the harmonics can now be measured and compared to the meter deflection that was obtained with the complete waveform.

16-1-3 Block Diagram and Controls

The block diagram of the HP 331A distortion analyzer is shown in Figure 16-2, and the front panel controls of the instrument are illustrated in Figure 16-3. In addition to the rejection amplifier, there are six component blocks in Figure 16-2. Two of the these are a *1-MΩ attenuator* and an *impedance converter*, which are connected prior to the rejection amplifier. The attenuator reduces the amplitude of the input signal to a suitable level for processing. Attenuation of up to 50 dB can be selected in 10-dB steps. The attenuator switch is identified as *SENSITIVITY* on the instrument front panel (Figure 16-3). The *VERNIER* knob at the center of the sensitivity switch controls the variable resistor at the input of the rejection amplifier (*sensitivity vernier* in Figure 16-2). This provides fine adjustment of the input signal attenuation.

The impedance converter is essentially a unity gain amplifier with high-input impedance and low-output impedance. It interfaces the attenuator and rejection amplifier.

Immediately following the rejection amplifier (in Figure 16-2), the *post attenuator* is simply a meter range selector. It is controlled by the *METER RANGE* switch on the front panel. The range switch and attenuator controls are used in conjunction with each other to set up an appropriate meter indication. The post attenuator feeds the signal to the meter circuit, which includes an amplifier and rectifier as well as a PMMC instrument.

The two remaining blocks in Figure 16-2 are an *AM detector* and another attenuator identified as *1:1 and 1000:1 attenuator*. The AM detector is used only when distortion is to be investigated on the envelope of an RF signal. This circuit recovers the envelope or modulating signal from the RF waveform. The modulating signal is then analyzed for distortion content like any other input signal. On the control panel of the instrument, the AM detector is switched in or out by means of the *NORM/R.F.DET* switch (left-hand side of the panel).

Excluding the rejection amplifier and AM detector, the block diagram in Figure 16-2 constitutes an ac voltmeter. To allow the instrument to be used as a voltmeter, the rejection amplifier can be bypassed by the action of function switch S_1. With S_1 in its upper position in Figure 16-2 (as illustrated), the input signal is fed through the 1:1 and 1000:1 attenuator to the impedance converter and then around the rejection amplifier to the post attenuator and the meter circuit. In Figure 16-3, the S_1 control is identified as *FUNCTION*. Its three positions are: *VOLTMETER*, *SET LEVEL*, and *DISTORTION*. In the *VOLTMETER* position, the rejection amplifier is switched out of the circuit. The 1:1 attenuator is included when the meter range is set from 0.0003 V through 0.3 V, and the 1000:1 attenuator is in circuit for the 1-V to 300-V range. The *SET LEVEL* position corresponds to the center position of S_1 in Figure 16-2. At this setting, one terminal of the Wein bridge is grounded (as explained in

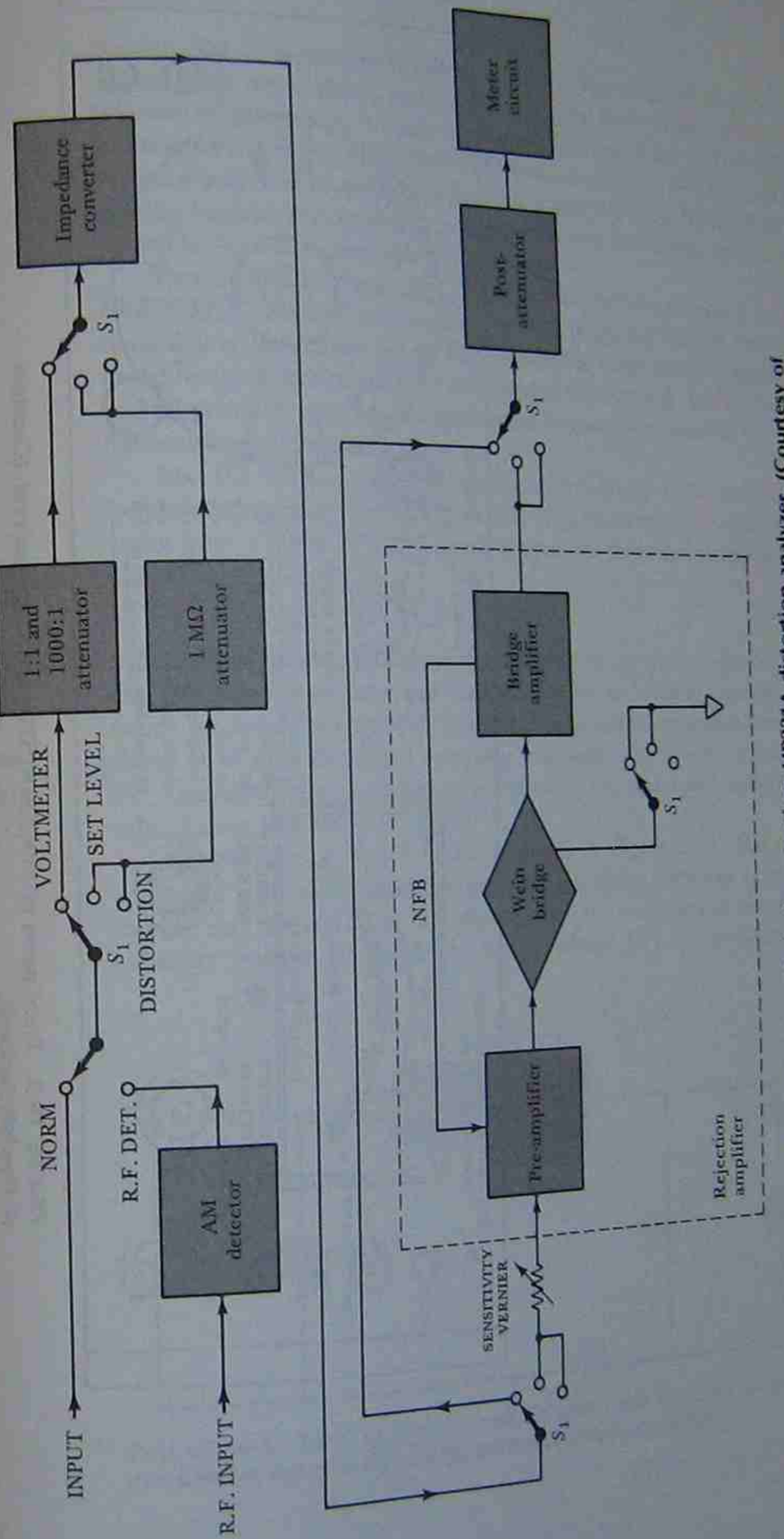


FIGURE 16-2. Block diagram of an HP331A distortion analyzer. (Courtesy of Hewlett-Packard).

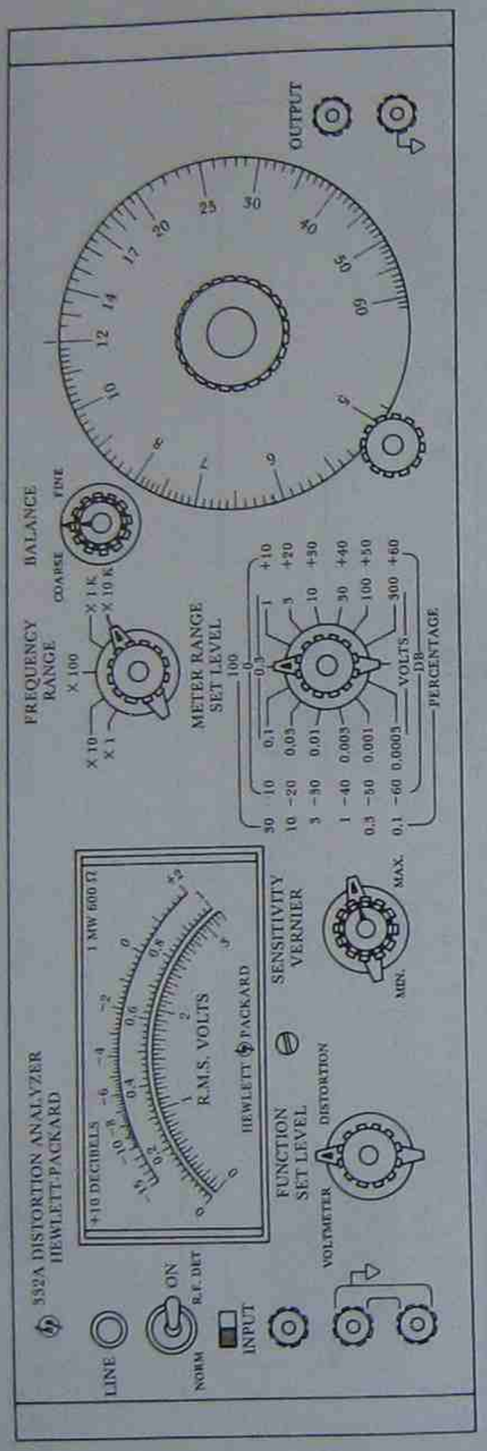


FIGURE 16-3. Front panel of a model HP331A distortion analyzer. (Courtesy of Hewlett-Packard).

Section 16-1-2) to prevent the filtering action. The distorted waveform is passed to the meter circuit, and the sensitivity and meter range controls are adjusted to give a suitable meter indication. Selection of the *DISTORTION* position on the FUNCTION SWITCH (bottom terminal of S_1) brings the rejection amplifier properly into the circuit with the Wein bridge filtering out the fundamental frequency component. Only the harmonics are now passed to the meter circuit for measurement.

Two controls in Figure 16-3 that have not yet been discussed are the *FREQUENCY RANGE* selector and the large frequency dial on the right-hand side of the control panel. These adjust the Wein bridge components to the fundamental frequency of the signal to be analyzed. The *BALANCE* control provides *coarse* and *fine* adjustment of resistors to tune the bridge to the actual signal frequency.

The HP 331A measures distortion on waveforms with fundamental frequencies ranging from 5 Hz to 600 kHz. Accuracy of measurement varies from $\pm 3\%$ to $\pm 12\%$, depending upon the frequency range and the distortion content.

16-2 THE *Q* METER

Inductors, capacitors, and resistors which have to operate at radio frequencies (RF) cannot be measured satisfactorily by ac bridges. Instead, resonance methods are employed in which the unknown component may be tested at or near its normal operating frequency. The *Q meter* is designed for measuring the Q factor of a coil and for measuring inductance, capacitance, and resistance at RF.

16-2-1 *Q* Meter Operation

A basic circuit of a Q meter is shown in Figure 16-4. The circuit consists of a variable calibrated capacitor, a variable frequency ac voltage source, and the coil to be investigated. All are connected in series. The capacitor voltage (V_C) and the source voltage (E) are monitored by

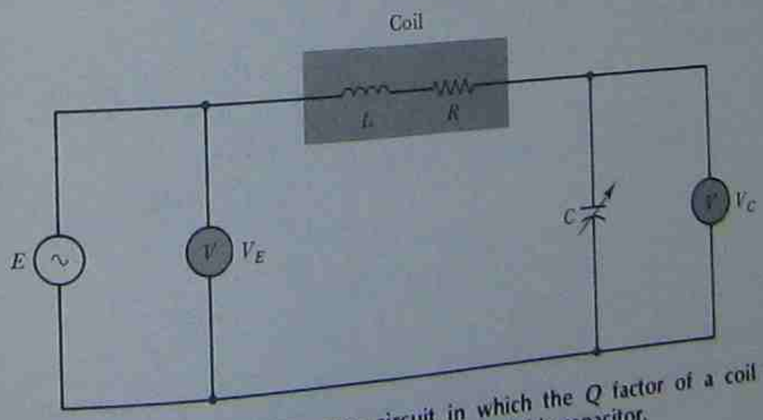


FIGURE 16-4. Basic Q meter circuit in which the Q factor of a coil is measured in terms of the voltage accross a variable capacitor.

voltmeters. The source frequency is set to the desired measuring frequency, and its voltage is adjusted to a convenient level. Capacitor C is adjusted to obtain resonance, as indicated when the voltage across C is a maximum. If necessary, the source is readjusted to the desired output level when resonance is obtained.

At resonance:

$$V_C = V_L, \text{ and } I = E/R$$

also

$$Q = \frac{\omega L}{R} = \frac{1}{\omega CR} \qquad 16\text{-}1$$

and

$$Q = \frac{V_L}{E} = \frac{V_C}{E}$$

EXAMPLE 16-1 When the circuit in Figure 16-4 is in resonance, $E = 100$ mV, $R = 5\ \Omega$, and $X_L = X_C = 100\ \Omega$. Calculate the coil Q and the voltmeter indication. Also determine the Q factor and voltmeter indication for another coil that has $R = 10\ \Omega$ and $X_L = 100\ \Omega$ at resonance.

SOLUTION

$$I = \frac{E}{R} = \frac{100\text{ mV}}{5\ \Omega} = 20\text{ mA}$$

$$V_L = V_C = IX_C$$
$$= 20\text{ mA} \times 100\ \Omega$$
$$= 2\text{ V}$$

$$Q = \frac{V_L}{E} = \frac{2\text{ V}}{100\text{ mV}} = 20$$

For the second coil:

$$I = \frac{E}{R} = \frac{100\text{ mV}}{10\ \Omega} = 10\text{ mA}$$

$$V_L = V_C = IX_L$$
$$= 10\text{ mA} \times 100\ \Omega$$
$$= 1\text{ V}$$

$$Q = \frac{V_L}{E} = \frac{1\text{ V}}{100\text{ mV}} = 10$$

Example 16-1 shows that when $Q = 20$ the capacitor voltmeter indicates 2 V, and when $Q = 10$ the voltmeter indicates 1 V. Clearly, the voltmeter can be calibrated to directly indicate the coil Q.

If the ac supply voltage in Example 16-1 is halved, the circuit current is also halved. This results in V_C and V_L becoming half of the values calculated. Thus, instead of indicating 2 V for a Q of 20, the capacitor voltmeter would indicate only 1 V. The problem can be avoided by always setting the signal generator voltage to the correct level or by having the signal generator output voltage precisely stabilized. However, it can sometimes be convenient to adjust the supply to other voltage levels. If the 100-mV position on the supply voltmeter is marked as *1*, and the 50-mV position is marked as *2*, etc., the supply voltmeter becomes a *multiply-Q-by* meter. When E is set to give a *1* indication, all Q values measured on the capacitor voltmeter are correct. If E is set to the *2* position, measured Q values must be multiplied by *2*. Instruments that have a signal generator with a stabilized output do not use a meter for monitoring the source voltage (i.e., there is no multiply-Q-by meter). In this case, the voltage level of the supply is selected by means of a switch, and this switch becomes a Q meter range control.

If the adjustable capacitor in the Q meter circuit is calibrated and its capacitance indicated on a dial, it can be used to measure the coil inductance. From Equation 16-1:

$$L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi f)^2 C}$$

Suppose $f = 1.592$ MHz, and resonance is obtained with $C = 100$ pF.

$$L = \frac{1}{(2\pi \times 1.592\text{ MHz})^2 \times 100\text{ pF}}$$
$$\simeq 100\ \mu\text{H}$$

When resonance is obtained at the same frequency with $C = 200$ pF, $L \simeq 50\ \mu$H. Also, if $C = 50$ pF at 1.592 MHz, L is calculated as 200 μH. It is seen that the capacitance dial can be calibrated to directly indicate the coil inductance (in addition to capacitance).

If the capacitor dial is calibrated to indicate inductance when $f = 1.592$ MHz, then any change in f changes the inductance scale. For $f = 15.92$ MHz and $C = 100$ pF,

$$L = \frac{1}{(2\pi \times 15.92\text{ MHz})^2 \times 100\text{ pF}}$$
$$= 1\ \mu\text{H}$$

With $C = 200$ pF and 50 pF, L becomes 0.5 μH and 2 μH respectively. Therefore, if the frequency is changed in multiples of 10, the inductance scale can still be used with an appropriate multiplying factor.

As an alternative to using a fixed frequency and adjusting the capacitor, it is sometimes convenient to leave C fixed and adjust f to obtain resonance. In this case, the inductance scale on the capacitor dial is no longer correct. However, Equation 16-1 still applies, so L can be calculated from the C and f values.

Residual resistance and inductance in the Q meter circuit can be an important source of error. If the signal generator has a source resistance R_E, then the circuit current at resonance is:

$$I = \frac{E}{R_E + R} \text{ instead of } I = \frac{E}{R}$$

Also, the indicated Q factor of the coil is:

$$Q = \frac{\omega L}{R_E + R}$$

instead of the actual coil Q, which is:

$$Q = \frac{\omega L}{R}$$

Obviously, R_E must be much smaller than the resistance of any coil to be investigated. Similarly, residual inductance must be held to a minimum to avoid measurement errors. In a practical Q meter, the output resistance of the signal generator is around 0.02 Ω, and the residual inductance may typically be 0.015 μH.

16-2-2 Practical *Q* Meter

The practical Q meter circuit shown in Figure 16-5 is essentially the same as the circuit in Figure 16-4, except that a signal generator with a stabilized output voltage is employed. Inductor and capacitor terminals are shown. Those terminals marked *HI* (high potential) are commoned, and one of the capacitor terminals is grounded. The coil terminal identified as *LO* is connected to ground via the signal generator source resistance.

The Q meter shown in Figure 16-6 has a meter for indicating circuit Q and a *Q LIMIT* (range) switch. A frequency dial with a window is included, and controls are provided for frequency range selection and for continuous adjustment of frequency. The L/C dial indicates the circuit L and C and is adjusted by the series capacitor control identified as L/C. The ΔC control (alongside the L/C control) provides fine adjustment of the series capacitor. Its dial indicates the capacitance as a plus (+) or minus (−) quantity. The total resonating capacitance is the sum or difference of that indicated on the two capacitance dials. To the right of the Q indicating meter, ΔQ ZERO *COARSE* and *FINE* controls are situated.

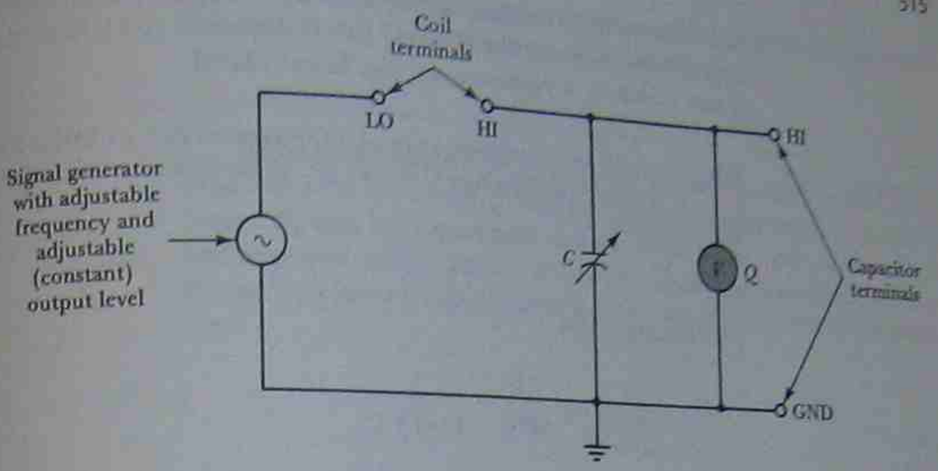


FIGURE 16-5. Practical Q meter circuit.

These are used to measure the difference in Q between two or more coils that have closely equal Q factors.

16-2-3 *Q* Meter Applications

MEDIUM-RANGE INDUCTANCE MEASUREMENT (DIRECT CONNECTION). Coils with inductances of up to about 100 mH can be directly connected to the inductance terminals, as already explained. The signal generator is set to the desired frequency, and its output level is adjusted to give a convenient Q factor range. With the ΔC capacitor dial set to zero, the Q capacitor control is adjusted to give maximum deflection on the Q meter. The Q factor of the coil is now read directly from the meter. The coil inductance may also be read from the C/L dial, if the signal generator



FIGURE 16-6. HP4342A Q meter. (Courtesy of Hewlett-Packard).

is set to a specified frequency. When some other frequency is employed, the inductance can be calculated from f and C (Equation 16-1). With the coil Q and L known, its resistance can also be calculated.

EXAMPLE 16-2 With the signal generator frequency of a Q meter set to 1.25 MHz, the Q of a coil is measured as 98 when $C = 147$ pF. Determine the coil inductance and resistance.

SOLUTION

From Equation 16-1,

$$L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi f)^2 C}$$

$$= \frac{1}{(2\pi \times 1.25 \text{ MHz})^2 \times 147 \text{ pF}}$$

$$= 110\ \mu\text{H}$$

and, $$Q = \frac{\omega L}{R}$$

or, $$R = \frac{2\pi fL}{Q} = \frac{2\pi \times 1.25 \text{ MHz} \times 110\ \mu\text{H}}{98}$$

$$= 8.8\ \Omega$$

HIGH-IMPEDANCE MEASUREMENTS (PARALLEL CONNECTION). Inductances greater than 100 mH, capacitances smaller than 400 pF, and high value resistances are best measured by connecting them in parallel with the capacitor terminals.

For measurement of parallel connected inductance (L_P), the circuit is first resonated using a *reference inductor* (or *work coil*). The values of C and Q are recorded as C_1 and Q_1. L_P is now connected, and the circuit is readjusted for resonance to obtain C_2 and Q_2. The parameters of the unknown inductance are now determined from the following equations:

$$L_P = \frac{1}{\omega^2(C_2 - C_1)} \qquad 16\text{-}2$$

$$Q = \frac{Q_1 Q_2 (C_2 - C_1)}{C_1(Q_2 - Q_1)} \qquad 16\text{-}3$$

To measure a parallel connected capacitance (C_P), the circuit is first resonated using a reference inductor, as before. The values of C_1 and Q_1 are noted. Then the capacitor is connected. Resonance is again found by

adjusting the resonating capacitor to give a value C_2. Normally, the circuit Q is not affected. The unknown capacitance is:

$$C_P = C_1 - C_2 \qquad 16\text{-}4$$

Large value resistors (R_P) connected in parallel with the resonating capacitor alter the circuit Q, but no capacitance adjustment is necessary (unless R_P also has capacitance or inductance). Once again, the circuit is first resonated using a reference inductor. Then R_P is connected, and the change in Q factor (ΔQ) is measured. The unknown resistance is calculated from

$$R_P = \frac{Q_1 Q_2}{\omega C_1 \Delta Q} \qquad 16\text{-}5$$

LOW-IMPEDANCE MEASUREMENTS (SERIES CONNECTION). Small values of resistance, small inductors, and large capacitors can be measured by placing them in series with the reference inductor. The component to be measured is connected between the LO terminal of the Q meter and the low potential terminal of the reference inductor. The other end of the reference inductor is connected to the HI terminal of the Q meter. Initially, a low resistance *shorting strap* is connected to short-out the unknown component. The circuit is now tuned for resonance, and the values of Q_1 and C_1 are noted. The shorting strap is removed, and the circuit is retuned for resonance.

When a pure resistance is involved, circuit resonance should not be affected by removal of the shorting strap. However, the circuit Q should be reduced. The change in Q is measured as ΔQ. The series-connected resistance is now calculated as:

$$R_S = \frac{\Delta Q}{\omega C_1 Q_1 Q_2} \qquad 16\text{-}6$$

A small series-connected inductance (L_s) affects both the Q factor and the circuit resonance. After initially resonating the circuit with L_s shorted, the shorting strap is removed, and the capacitor is readjusted for resonance. The inductance is now calculated as:

$$L_s = \frac{(C_1 - C_2)}{\omega^2 C_1 C_2} \qquad 16\text{-}7$$

With a large series-connected capacitor (C_s), the circuit is first resonated with a shorting strap across the capacitor terminals. The strap is removed, and the circuit capacitor is readjusted for resonance. In this case,

the Q of the circuit should be largely unaffected. The series-connected capacitance is:

$$C_s = \frac{C_1 C_2}{(C_2 - C_1)} \qquad 16\text{-}8$$

16-3 SPECTRUM ANALYZER

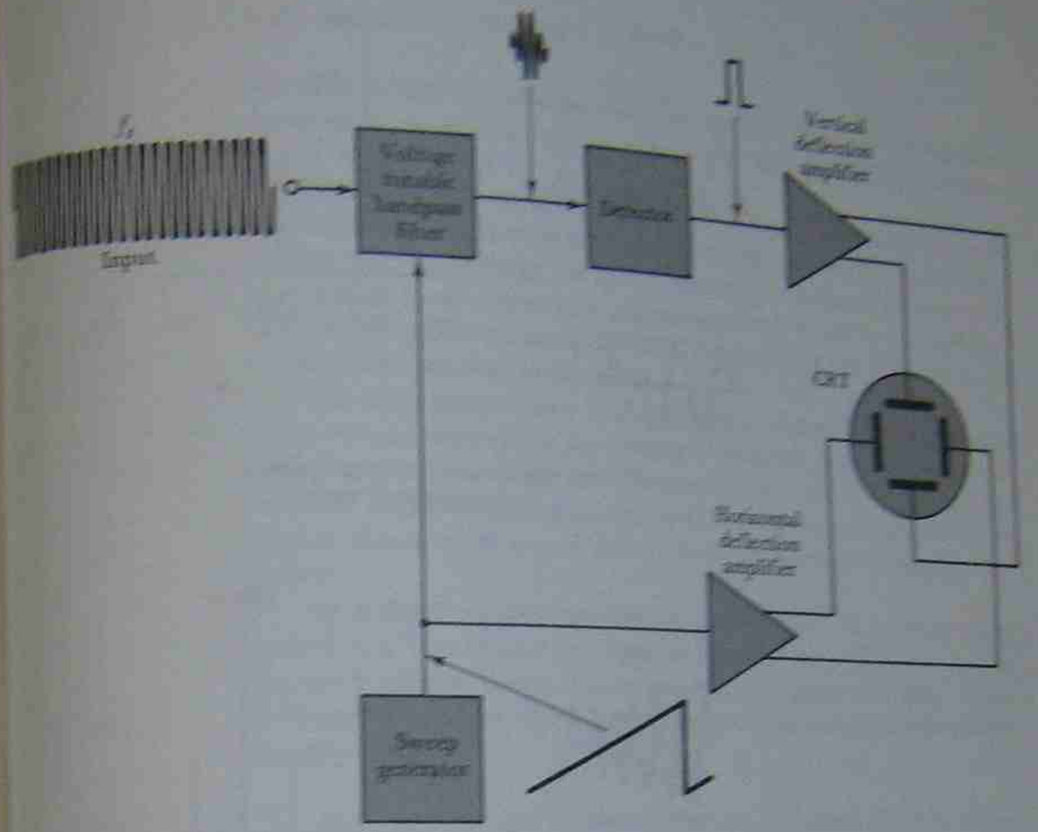
16-3-1 Swept trf Spectrum Analyzer

A *spectrum analyzer* separates an ac signal into its various frequency components and displays each component as a vertical line on a CRT screen. The amplitude of each vertical line in the display represents the amplitude of each frequency component, and the horizontal position of each line defines the frequency.

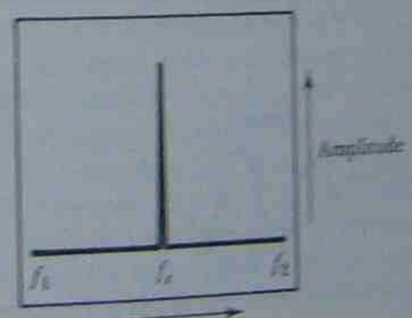
Consider Figure 16-7(a), which shows the block diagram of a *swept trf* (tuned radio frequency) *spectrum analyzer*. A sweep generator produces a linear ramp, which provides horizontal deflection voltage for the CRT. The ramp is also applied to a *voltage tunable bandpass filter*. This is a filter with a very narrow pass-band. The center frequency of the pass-band is swept from a minimum frequency (f_1) to a maximum (f_2) as the ramp voltage sweeps from minimum to maximum amplitude. An input signal with a frequency (f_x) would pass through the bandpass filter only during the brief time that the filter pass-band is tuned to f_x. When the signal (with frequency f_x) emerges from the filter, it is converted to a dc voltage level by the *detector* and applied as an input to the vertical deflection amplifier of the CRT. The detector is basically a rectifier and capacitor circuit that produces a dc output voltage equal to the peak input voltage (see Section 8-9-2). Thus, during the time that the filter pass-band sweeps through f_x, a vertical line representing the signal amplitude is traced on the CRT screen.

The horizontal position of the vertical line is determined by the amplitude of the sweep generator ramp voltage at the instant that f_x is passing through the filter. As already explained, the ramp voltage also dictates the instantaneous filter frequency. The horizontal sweep of the electron beam across the CRT screen represents the changing filter frequency, from f_1 to f_2. Consequently, the horizontal position of each vertical line in the display can be identified as a particular signal frequency. If f_x is exactly halfway between f_1 and f_2, the vertical line representing f_x should be exactly in the center of the screen (see Figure 16-7[b]).

Suppose two different signals are applied simultaneously to the input of the filter. Assume that the signal frequencies are $f_a = 200$ kHz and $f_b = 300$ kHz and that the amplitudes are $V_a = 2$ V and $V_b = 1$ V. If the center frequency of the filter is swept from 100 kHz to 500 kHz, the display shown in Figure 16-8(a) would result. Signal a is displayed at a point one quarter of the way across the screen because its 200-kHz frequency is one quarter of the way between $f_1 = 100$ kHz and $f_2 = 500$ kHz. Similarly, signal b is displayed at the center of the screen because

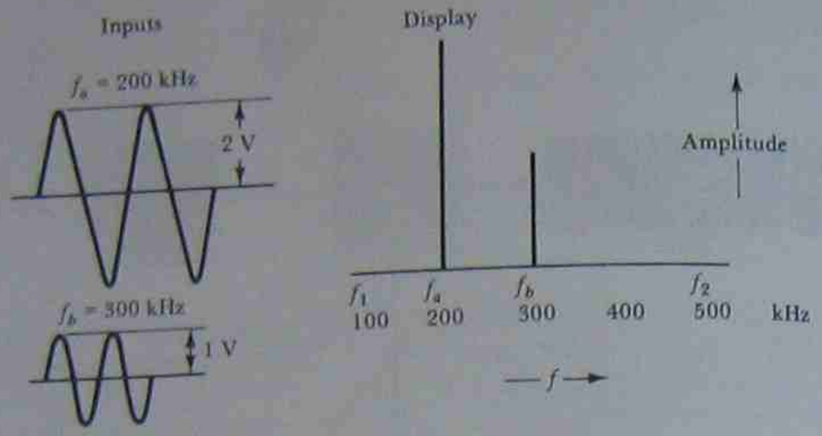


(a) Block diagram of swept *trf* spectrum analyzer

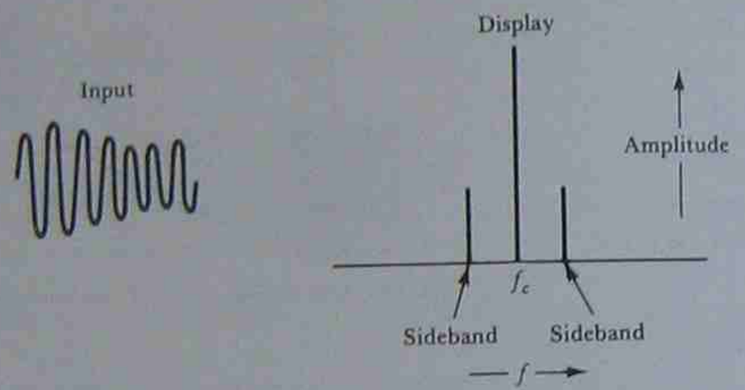


(b) Display produced by a single input frequency

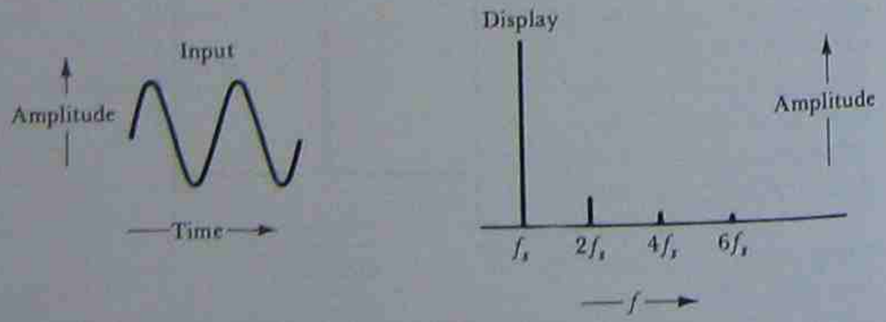
FIGURE 16-7. Swept trf spectrum analyzer, block diagram, and display.



(a) Two different input signals simultaneously applied



(b) Amplitude modulated waveform is separated into its carrier frequency component and two sidebands



(c) An apparently perfect sine wave input might be shown to have harmonic distortion

FIGURE 16-8. Spectrum analyzer displays produced by various input signals.

300 kHz is halfway between 100 kHz and 500 kHz. The vertical line representing signal a is twice as large as the line representing b because $V_a = 2$ V and $V_b = 1$ V.

Figure 16-8(b) illustrates the result of applying an amplitude modulated signal to a spectrum analyzer. The display consists of a single, large, vertical line, representing the carrier frequency amplitude, together with two smaller lines representing the two sideband frequency components. The display allows the amplitudes and frequencies of the sidebands to be investigated in relation to the carrier.

The input signal shown in Figure 16-8(c) appears to be a pure sine wave. When displayed on an ordinary oscilloscope, the signal would not reveal any obvious distortion. However, when applied to a spectrum analyzer, harmonic distortion might well be revealed, as illustrated. In the display shown, small second, fourth, and sixth harmonic components are present.

An ordinary oscilloscope displays the amplitude of the input signal plotted to a base of time (see input in Figure 16-8[c]). Thus, it is said to operate in the *time domain*. A spectrum analyzer displays the signal amplitude plotted to a base of frequency. So a spectrum analyzer operates in the *frequency domain*.

16-3-2 Swept Superheterodyne Spectrum Analyzer

The *swept superheterodyne spectrum analyzer* block diagram shown in Figure 16-9 is basically similar to the swept trf system in Figure 16-7. The difference is that the voltage tunable bandpass filter is now replaced with a *voltage tunable oscillator* (VTO) (see Section 15-5), a *frequency mixer*, and an *intermediate frequency* (IF) *amplifier*. The ramp voltage from the sweep generator is applied, once again, as a horizontal deflecting voltage to the CRT. The ramp is also applied to the VTO to produce a VTO output frequency that sweeps from a minimum (f_1) to a maximum (f_2). The VTO output is applied to one input of the mixer, and the other mixer input terminal receives the signal to be analyzed. If the signal frequency is f_s and the VTO frequency is f_o, the mixer output is the sum and difference of the two frequencies: $f_m = (f_o \pm f_s)$. These are applied to the IF amplifier, which passes and amplifies only one intermediate frequency.

Assume that the IF amplifier passes only a 100-kHz output frequency component from the mixer and that the VTO frequency (f_o) sweeps from 100 kHz to 200 kHz. If the signal frequency is $f_s = 50$ kHz, the mixer output when $f_o = 100$ kHz would be $f_m = 100$ kHz $\pm$ 50 kHz = (150 kHz or 50 kHz). Neither of these two frequencies is passed by the 100-kHz IF amplifier. Similarly, at the maximum VTO frequency of 200 kHz, f_m = 200 kHz $\pm$ 50 kHz = (250 kHz or 150 kHz). Again, neither frequency can pass through the IF amplifier. When the VTO output has a frequency of 150 kHz, and $f_s = 50$ kHz, then $f_m = 150$ kHz $\pm$ 50 kHz = (100 kHz or 200 kHz). The 100-kHz component is passed and amplified by the IF

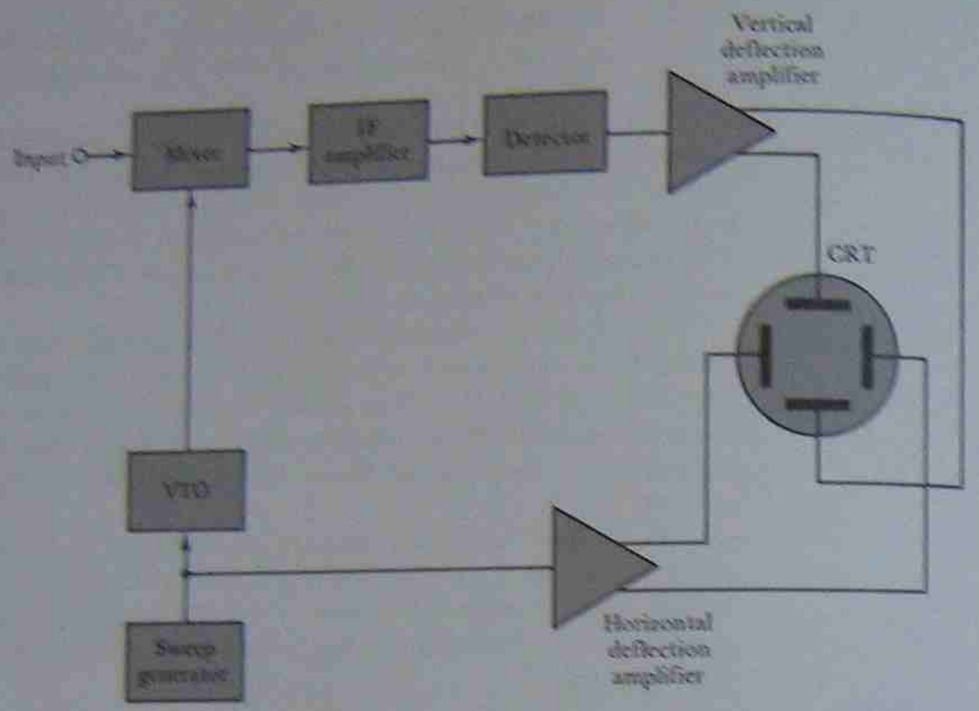


FIGURE 16-9. Block diagram of swept superheterodyne spectrum analyzer.

amplifier, and it produces a vertical line on the CRT. The VTO output at 150 kHz is exactly halfway between its extremes of 100 kHz and 200 kHz. Therefore, the vertical line representing $f_s = 50$ kHz occurs at the center of the CRT screen (see Figure 16-10).

When $f_s = 25$ kHz, a passable IF input of 100 kHz occurs at $f_o = 125$ kHz. This produces a vertical line one quarter of the way across the screen horizontally. Similarly, when $f_s = 75$ kHz, the 100 kHz IF is produced with $f_o = 175$ kHz to display a vertical line three quarters of the way across the screen, as shown in Figure 16-10. When $f_s = 0$, and when $f_s = 100$ kHz, lines are produced at the left-hand side and right-hand side, respectively, of the CRT screen. Thus, as displayed in Figure 16-10, signal frequencies from 0 to 100 kHz can be investigated. A change of IF amplifier or VTO will change the range of signal frequencies that may be displayed.

The major advantage of the superheterodyne spectrum analyzer over the trf type is that the IF amplifier improves the instrument sensitivity. Also, the detector can give a better performance, since it has to operate at only one (IF) frequency.

16-3-3 Spectrum Analyzer Controls

The three major controls on a spectrum analyzer are: *TUNING*, *FREQUENCY SPAN/DIV*, and *REFERENCE LEVEL* (see Figure 16-11). The tuning control selects the display frequency either as starting frequency

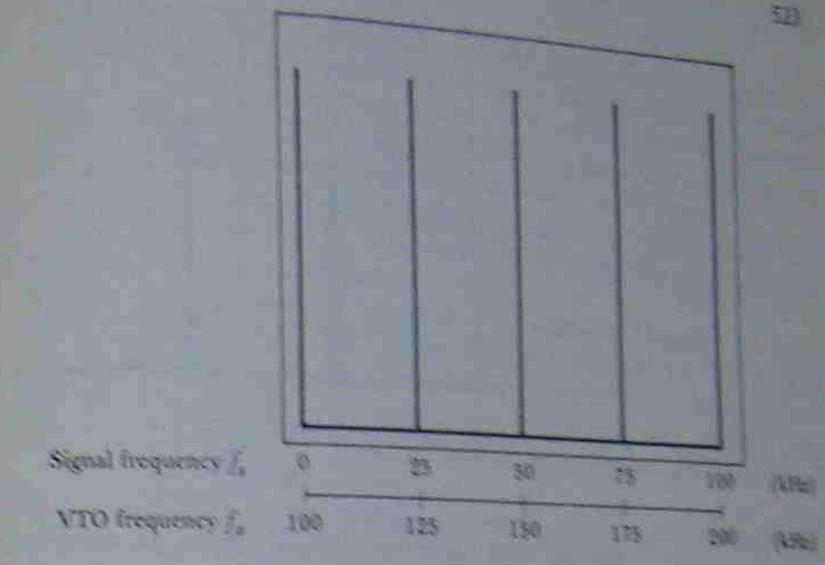


FIGURE 16-10. Relationship of display, signal frequency, and VTO frequency in swept superheterodyne spectrum analyzer with an intermediate frequency of 100 kHz.

or center frequency. This frequency is displayed digitally alongside the tuning dial. The frequency range is set by the frequency span/div control. At the 100-MHz selection, for example, each horizontal division on the screen represents an increase in frequency (from left to right) of 100 MHz. The actual display frequencies depend upon the tuning control. The tuning control can also be used to set an inverted marker spike (see Figure 16-12) anywhere across the screen to identify a particular signal to be investigated. In this case, the digital frequency dial displays the marked

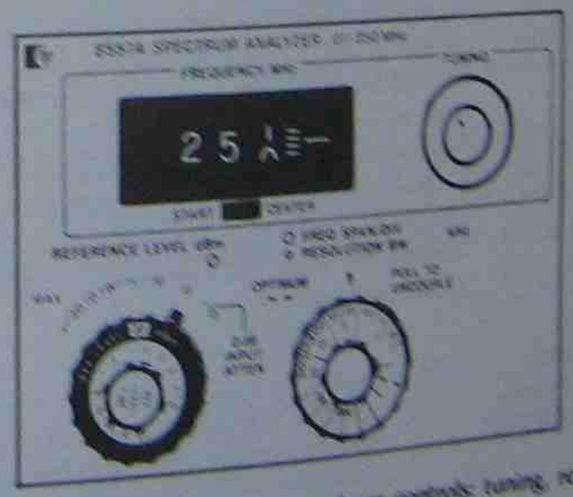


FIGURE 16-11. Three major spectrum analyzer controls: tuning, reference level, and frequency span/div. (Courtesy of Hewlett-Packard).

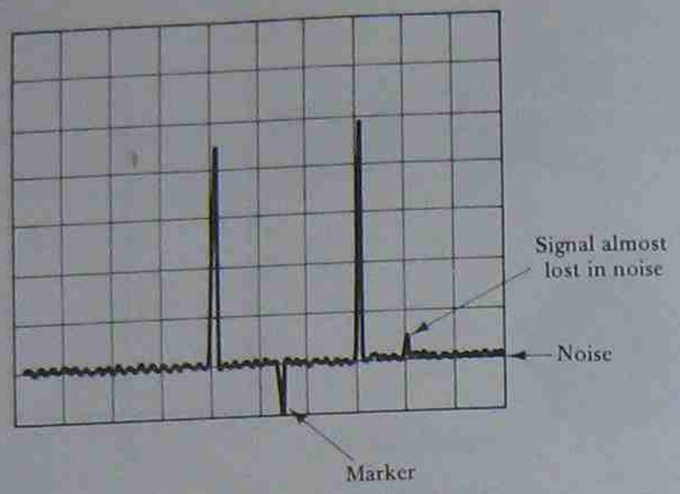


FIGURE 16-12. Spectrum analyzer display showing inverted marker spike and thermal noise.

signal frequency. The signal identified in this manner can be expanded by adjusting the frequency span/div control.

By means of the *reference level* control, a main signal (or reference signal) is adjusted to fill the screen vertically. The position of the reference level control identifies the absolute power of the reference signal in dBm. All other signals can be measured by the relation of their amplitudes to the (full scale) reference level.

Important quantities in the specification of a spectrum analyzer are: *frequency range*, *frequency resolution*, and *sensitivity*. The frequency range obviously specifies the extremes of signal frequency that may be investigated. Frequency resolution defines the smallest signal frequency separation that can be identified. This is dictated by the bandwidth of the IF amplifier. If the IF bandwidth is 100 Hz, then two signals with frequencies differing by 100 Hz can be identified as different signals. Frequencies much closer than this would tend to be displayed as one signal. The sensitivity of the instrument defines the minimum signal amplitude that may be detected. This sensitivity is limited by thermal noise generated within the spectrum analyzer (see Figure 16-12). The thermal noise is directly proportional to bandwidth. Thus, the narrower the selected bandwidth, the better the instrument sensitivity.

REVIEW QUESTIONS AND PROBLEMS

16-1. Sketch the basic circuit of a fundamental suppression harmonic analyzer. Carefully explain the operation of the circuit, including how the fundamental frequency component is suppressed. Also show how the filtering process can be disabled to pass the complete waveform.

16-2. Sketch the complete block diagram of a fundamental suppression distortion analyzer. Carefully explain the operation of the system. Also discuss the controls normally found on a distortion analyzer.

16-3. Sketch the basic circuit diagram of a Q meter. Explain the operation of the circuit, and write the equation for Q factor.

16-4. The circuit in Figure 16-4 is in resonance when $E = 200$ mV, $R = 3\ \Omega$ and $X_L = X_C = 95\ \Omega$. Calculate the coil Q and the voltmeter indication.

16-5. For the circuit in Figure 16-4, the voltmeter indicates 5 V when a coil is in resonance. If the coil has $R = 3.3\ \Omega$ and $X = 66\ \Omega$ at resonance, calculate the coil Q and the level of the supply voltage.

16-6. Write the equation relating L, C, and f for the basic Q meter circuit in Figure 16-4. Show that the capacitor voltmeter can be calibrated to indicate inductance.

16-7. Explain how the supply voltmeter in Figure 16-4 can be calibrated as a multiply-Q-by meter.

16-8. Discuss the effects of residual resistance and inductance in a Q meter circuit.

16-9. Sketch a practical Q meter circuit. Discuss its operation, and discuss the main controls and dials normally found on a Q meter.

16-10. List the various methods of connecting components to a Q meter for measurement. Briefly explain in each case.

16-11. Sketch the block diagram of a swept trf spectrum analyzer. Show the waveforms at various points in the system and explain its operation.

16-12. Sketch the spectrum analyzer displays that are likely to be produced for: (a) a pure sine wave input with a frequency halfway between the extremes of the swept frequency range, (b) two pure sine wave inputs with different frequencies and amplitudes, (c) an amplitude modulated sinusoidal waveform, and (d) an apparently pure sine wave with some harmonic distortion content. Briefly explain in each case. Also discuss the use of a marker spike to identify displayed signals.

16-13. Sketch the block diagram of a swept superheterodyne spectrum analyzer. Carefully explain the operation of the system, and discuss the relationship of display, signal, and VTO frequencies.

16-14. List the major controls on a spectrum analyzer, and discuss their functions.

INDEX

A

Absolute error, 91
ac bridges, 149:
 accuracy, 188
 capacitance bridge, 154, 162, 165
 frequency bridge, 188
 Hay bridge, 175
 impedance bridge, 179
 inductance bridge, 170, 172, 175
 null detectors, 152
 Owen bridge, 186
 phasor diagram, 164, 174
 residuals, 188
 Schering bridge, 187
 sensitivity, 188
 Wein bridge, 188
ac electronic voltmeters, 237
ac instrument, 41, 50
ac voltmeter, 85, 237
Accuracy, 21, 92, 122, 134, 188
Active probes, 359
Adapters, 89
ADC, 395
Air damping, 11
ALC, 495
Alternate mode, 339, 380
Ammeter, 29, 48, 52, 61, 82, 294
Ammeter calibration, 114
Ammeter resistance, 33
Amplification factor, 229
Amplifier/attenuator, 416
Amplifier type voltmeter, 211, 215, 222
Analog electronic instruments, 193
Analog electronic voltmeter, 252
Analog storage scope, 384
Analog to digital converter, 396
AND gate, 261
Anode, 316
Aquadag, 319
Astable multivibrator, 478
Attenuator, 320, 465, 487
Attenuator probes, 355
Audio amplifier testing, 86
Audio signal generator, 468
Auto erase, 388
Auto ranging, 291, 305
Auto store, 388
Automatic level control, 495
Automatic time base, 330
Ayrton shunt, 30, 31

B

Balance control, 320
Balanced bridge, 133
Base, 194
BCD to decimal conversion, 281
BCD to seven segment, 281
Beam finder, 341
Bias terminals, 311
Binary coded decimal, 276
Bistable multivibrator, 265
Bistable storage CRT, 384
BJT, 193
Blanking, 334
Bleeder resistor, 434
Breakdown diode, 436
Bridge rectifier, 42, 239

Brightness, 316, 319, 387
Buffer amplifier, 198

C

Calibrated attenuator, 487
Calibration:
 ac instruments, 120
 accuracy, 122
 chart, 121
 dc ammeter, 114
 dc voltmeter, 117
 potentiometer, 106
 procedures, 121
 transfer instrument, 120
 wattmeter, 119
Calibration control, 70
Capacitance bridge, 154, 162, 165
Capacitor dissipation factor, 161
Capacitor equivalent circuit, 157
Cardinal points, 121
Catch diode, 458
Cathode, 226, 316
Cathode follower, 227
Cathode ray oscilloscope, 315 (See also Oscilloscope)
Cathode ray tube, 315
Center zero scale, 16
Characteristic plotting, 425
Characteristics display
Chart recorders, 411
Choke-capacitor filtering, 434
Circle display, 364
Clamping circuit, 242
Clipping circuit, 467
Clock source, 285
Coil former, 4
Cold junction, 60
Collector mesh, 386
Collector, 194
Collimator, 384
Colpitts oscillator, 487
Common mode rejection ratio, 424
Commutating capacitors, 268
Comparator, 374, 390, 417
Compensated thermocouple, 60
Compensated wattmeter, 55, 56
Concentric vane, 14
Constant current source, 215, 236
Constant current source, 326
Constantan, 32
Controlling force, 2, 3
Core magnet, 8
Core, 7, 8
Counter specification, 297
Counter/timer, 297
Counter weights, 8
Counting circuits, 272
Coupling capacitance, 351
CR equivalent circuit, 157
Critical damping resistance, 17
CRT, 315
Current gain factor, 195
Current limiting, 447
Current probe, 307
Current sensitivity, 17
Current terminals, 26, 27, 139
Current transformer, 48, 63

D

DAC, 395
D'Arsonval instrument, 7
Damping force, 2, 4, 5
Damping resistor, 17
Darington pair, 442
dB, 85, 86, 254
dBm, 254
dc ammeter, 26, 82
dc potentiometer, 103
dc power supplies, 429
dc shift control, 334
dc voltmeter, 34, 84
Deadband, 423
Decade counter, 275
Decade resistance box, 129
Decibel measurement, 85, 254
Decibel-milliwatt, 254
Deflecting force, 2, 3
Deflecting torque, 9, 13
Deflection amplifier, 320
Deflection factor, 318
Deflection instruments, 1
Deflection sensitivity, 318
Delay time, 347, 484
Delayed time base, 374
Device characteristics, 360
Difference amplifier VTVM, 229
Differentiating circuit, 331
Digital displays, 276
Digital frequency meter, 288
Digital indicator tube, 278
Digital instruments, 259, 285
Digital LCR meter, 311
Digital memory, 399, 402
Digital multimeter, 305
Digital storage scope, 395
Digital to analog conversion, 400
Digital voltmeter, 298
Diode, 41
Discriminator, 495
Display drivers, 297
Display enable, 288
Dissipation factor, 161
Distortion analyzer, 505
DMM, 305
Drain, 196
DTB, 376
Dual-beam oscilloscope, 336
Dual-polarity supply, 201
Dual-slope integrator, 299
Dual-trace oscilloscope, 336
DVM, 298
Dynamic impedance, 436
Dynamometer instrument, 11

E

Eddy currents, 4, 5
Electrical zero control, 204, 213
Electrodynamic ammeter, 52
Electrodynamic instrument, 11, 12
Electrodynamic instrument on ac, 50
Electrodynamic voltmeter, 52

Electromechanical system, 2, 7
Electron lens, 317
Electronic ammeter, 249
Electronic galvanometer, 250
Electronic ohmmeters, 231, 234, 236
Electronic voltmeter, 193, 237, 252
Electrostatic deflection, 318
Electrostatic focusing, 317
Electrostatic holding, 423
Emitter, 194
Emitter coupled amplifier, 211
Emitter follower, 196
Emitter follower voltmeter, 196, 198, 200
Equipotential lines, 317
Error:
  difference, 97
  observer, 93
  probable, 100
  product, 98
  quotient, 98
  raised-to-power, 98
  random, 99
  sources, 19
  sum, 96
Expanded mode, 394
Expander, 342

F

Fall time, 484
Feedback amplifier, voltmeter, 215
FET, 196
FET input, 359
FET input stage, 209
FET input voltmeter, 208
Field coils, 11
Field effect transistor, 196
Five-terminal measurement, 311
Flip-flop, 265
Flip-flop triggering, 269
Floating power supplies, 204
Flood guns, 384
Flutter, 383
Flyback time, 336
Focus ring, 317
Focusing system, 317
Fold-back current limiting, 448
Forward volt drop, 41
Four-terminal resistor, 27
Frequency bridge, 188
Frequency domain, 521
Frequency effects, 19
Frequency measurement, 292, 344
Frequency meter, 288
Frequency mixer, 521
Frequency range, 246
Frequency ratio, 294
Frequency response, 59, 61
Frequency synthesizer, 498
Full-wave bridge rectifier, 239
Full-wave rectifier, 43
Function generator, 469
Fundamental suppression, 506

G

Galvanometer, 16
Galvanometric recorder, 411
Gate, 196
Graphic recording, 411
Graticule, 341
Grounds, 204
Guard ring, 144
Guard wire, 142

H

Half-bridge full-wave rectifier, 45, 48, 239
Half-wave rectifier, 45, 238
Harmonic distortions, 506
Hartley oscillator, 487
Hay bridge, 175
High impedance measurement, 516
High resistance measurement, 142
High voltage probe, 89, 307
High-frequency distortion, 351
Hold-off circuit, 331
Horizontal sweep generator, 326
Horseshoe magnet, 7, 8
Hot junction, 60
Hysteresis, 296

I

IC operational amplifiers, 219
IC voltage regulator, 449
IF amplifier, 521
Impedance bridge, 179
Incremental inductance, 183
Inductance bridge, 170
Inductance comparison bridge, 170
Inductance measurements, 515
Inductor equivalent circuit, 159
Inductor Q factor, 161
Infinity, 69, 145
Input amplification, 297
Input attenuation, 296
Input attenuator, 207
Input impedance, 353
Input resistance, 206, 351
Integrator, 298
Interpolation, 405
Inverting amplifier, 400
Inverting input, 219
Iron core, 7, 8
Isolation shield, 319

J

Jewelled bearings, 4, 6

K

Kelvin bridge, 139

L

Latch, 288
LCD, 276
LCR measurement, 308
LED, 176
Light beam recorder, 412
Light emitting diode, 276

Line regulation, 435, 452
Linear interpolator, 405
Linear ohmmeter, 236
Linear scale, 10, 11
Liquid crystal display, 276
Lissajou figures, 363
Load effect, 436
Load regulation, 435, 452
Logic gates, 261
Low impedance measuement, 517
Low-frequency distortion, 350
Low resistance measurement, 139
LR equivalent circuit, 159

M

Main time base, 374
Make-before-break switch, 29, 30
Manganin, 32
Manual triggering, 483
Matched transistors, 217
Maxwell bridge, 172
Maxwell-Wein bridge, 172
Megger, 145
Megohm sensitivity, 17
Megohmmeter, 145
Memory capacitors, 268
Memory recorder, 426
Mercury cadmium cell, 103
Miller integrator, 298
Mirror, 19
Modulated dc amplifier, 251
Modulation, 489
Modulus sixteen counter, 274
Monostable multivibrator, 480
Moving coil instrument, 7, 10
Moving iron instrument, 14
MTB, 376
Multifunction bridge, 179
Multiplier resistance, 34
Multiply-q-by meter, 513
Multirange ammeter, 29
Multirange ohmmeter, 74, 75
Multirange potentiometer, 110
Multirange voltmeter, 36, 37, 252
Multirange wattmeter, 55, 57

N

NAND gate, 263
Negative feedback, 218
Noise, 452
Noninverting amplifier, 222, 420
Noninverting input, 219
Nonlinear circuit, 246
NOR gate, 264
Normal cell, 104
Notch filter, 506
npn transistor, 194
Null detectors, 18, 127, 152
Nulled bridge, 133

O

Ohmmeter:
  accuracy, 78
  electronic, 231, 234, 236
  equivalent circuit, 76
  linear, 236
  multirange, 74, 75
  scale, 68
  series, 67, 231
  shunt, 74, 75, 234
  useful range, 78
  zero control, 70
  zero ohms, 69
One-to-one probe, 353
Op-amp, 219
Operational amplifier voltage regulator, 443
Operational amplifiers, 217, 219
OR gate, 262
Oscillographic recorder, 411
Oscilloscope:
  analog storage, 384
  controls, 341
  digital storage, 395
  flyback time, 336
  graticule, 341
  hold-off circuit, 331
Oscilloscope (*Contd.*)
  horizontal sweep generator, 326
  main time base, 374
  MTB, 376
  persistance, 384, 387
  phase measurement, 345
  post deflection acceleration, 319
  pre-trigger viewing, 407
  probe adjust, 342
  probes, 353
  pulse interpolator, 405
  pulse measurement, 347
  ramp generator, 329
  roll mode, 407
  sampling, 388
  sawtooth, 322
  secondary emission, 384
  sine wave interpolator, 405
  split-beam CRT, 336
  storage, 384, 395
  storage layer, 384, 386
  storage mesh, 386
  sweep generator, 326
  sync input, 331
  time base, 326
  time/div, 329
  time period, 344
  trigger level control, 334
  triggering amplifier, 331
  triode section, 326
  unblanking, 336, 391
  USB, 404
  useful storage bandwidth, 404
  variable persistance, 386
  vernier, 344
  vertical amplifier, 331
  volts/div, 343
  waveform display, 332
  write gun, 384
  Z axis modulation, 367
Output level meter, 487
Owen bridge, 186

P

Parallax error, 19, 20

Parallel resistance capacitance bridge, 165
PARD, 452
Parts-per-million, 92
Peak detector circuit, 242
Peak detector probe, 243
Peak inverse voltage, 432
Peak repetitive current, 432
Peak response voltmeter, 242
Peak reverse voltage, 432
Persistance, 384, 387
Phase locked loop, 4399
Phase measurement, 345
Phase sensitive detector, 310, 499
Phasor diagram, 164
Piezoelectric crystal, 498
Pivots, 4, 6
Plate, 226
Plate resistance, 229
PLL, 499
Plus-and-minus supply, 201, 219
PMMC instrument, 2, 7, 10
PMCC instrument on ac, 41
Polarized instrument, 9, 40
Pole shoes, 7
Positive clipper, 331
Post deflection acceleration, 319
Potential terminals, 139
Potentiometer, 94, 95
Potentiometer calibration, 106
Potentiometric recorder, 414
Power supplies, 429
Precision, 93
Pre-trigger viewing, 407
Probable error, 100
Probe adjust, 342
Probes, 89, 353
Pulse amplitude, 348
Pulse generator, 478
Pulse interpolator, 405
Pulse jitter, 383
Pulse measurement, 347
Pulse width, 347
PW, 347

Q

Q factor, 161
Q meter, 511, 514

R

Radial vane, 14, 15
Radio frequency generator, 487
Radio frequency probe, 89
Ramp generator, 329, 390, 494
Random error, 99
Range changing, 206
Ratio measurement, 295
Reciprocal counting, 293
Rectifier:
  ammeter, 48
  bridge, 42, 49, 239
  full-wave, 43, 48, 239
  half-bridge, full-wave, 45, 48, 239
  half-wave, 45, 238
  voltmeters, 41, 237
Reference inductor, 516
Rejection amplifier, 506
Relative error, 91
Reservoir capacitor, 430
Residuals, 188
Resistance:
  four terminal, 27
  per volt, 39
  plate, 229
  shunt, 18, 29
  surface leakage, 142
  swamping, 32
  volume, 142
Resistance measurement:
  ammeter and voltmeter, 127
  high, 142
  low, 139
  ohmmeter, 67
  potentiometer, 131
  substitution, 129
  VOM, 254
  Wheatstone bridge, 132
Resolution, 94, 400
Reverse leakage current, 41
RF oscillator, 487
RF probe, 307
RF signal generators, 487
Ring counter, 399
Ripple, 452
Rise time, 347, 484
Roll mode, 407
RST flip-flop, 272

S

Sampling scope, 388
Saturated cell, 104
Sawtooth, 322
Scale, 9, 10
Scale-of-sixteen counter, 273
Scale-of-ten counter, 275
Scale of 2000 counter
Scaling, 298
Schering bridge, 187
Schmitt trigger, 296, 469
Secondary emission, 384
Self-balancing potentiometer, 123
Sensitivity, 4, 39, 52, 133, 188
Series ohmmeter, 67, 231
Series-resistance capacitance bridge, 162
Seven-segment display, 276
Short-circuit protection, 446
Shunt box, 115, 116
Shunt, 26, 27
Shunt ohmmeter, 74, 75, 234
Shunt resistance, 18, 29
Signal generators, 461
Sine/square generator, 467
Sine wave generators, 462
Sine wave interpolator, 405
Slew rate, 347
Slewing speed, 424
Slide wire, 106
Sliding contact, 106
Solid-state electrode recorder, 417
Source, 196
Source effect, 435
Source follower, 209
Souce resistance, 352

Specified accuracy, 21
Spectrum analyzer, 518, 521
Spiral springs, 2, 3
Split-beam CRT, 336
Square wave conversion, 465
Stabilization ratio, 435
Staircase generator, 389
Standard cell, 103
Standard instrument, 122
Storage, 396
Storage layer, 384, 386
Storage mesh, 386
Store, 388
Stray capacitance, 188
Strip chart recorder, 407
Substitution, 129
Substitution technique, 189
Summing amplifier, 414
Surface leakage resistance, 142
Swamping resistance, 32
Sweep frequency generator, 494
Sweep generator, 326
Switching regulator, 456
Sync input, 331
Systematic errors, 95

T

Taut-band, 4, 6
Temperature error, 32, 39
Ten-to-one probe, 355
Thermal recorder, 412
Thermocouple, 59:
  ammeter, 61
  bridge, 62
  true rms voltmeter, 244
  voltmeter, 61
  wattmeter, 62, 63
Thevenin, 135
Three-and-a-half digit display, 283
Time base, 285, 326
Time/div, 329
Time domain, 521
Time measurement, 294
Time period, 344
Toggled flip-flop, 271
Tolerance, 92
Torque equation, 9, 13
Totalizing, 298
Tracking, 453
Transfer instrument, 51, 120
Transistor, 193
Transistor amplifier voltmeter, 211
Transistor switching, 259
Triangular wave, 475
Trigger level control, 334
Triggered flip-flop, 271
Triggering amplifier, 331
Triode section, 316
True rms voltmeter, 244
Truth table, 273, 275

U

Unblanking pulses, 336, 391
Unregulated power supplies, 429
Unsaturated cell, 104
USB, 404
Useful storage bandwidth, 404

V

Vacuum triode, 226
Variable gain amplifier, 495
Variable persistance, 386
Variable voltage diode, 489
VCO, 499
Vernier, 344
Vertical amplifier, 331
Video amplifier, 245
Volt box, 117, 118
Volt-ohm-milliammeter, 67, 80
Voltage:
  comparator, 374, 390, 417
  controlled oscillator, 499
  follower, 220
  measurement, 253
  peak inverse, 432
  regulators, 436
  sensitivity, 17
  terminals, 26, 27
Voltage (*Contd.*)
  transformer, 63
  tunable filter, 518
  tunable oscillator, 521
  tuned oscillator, 494
Voltage transformer, 63
Voltmeter:
  ac, 85
  calibration, 117
  dc, 84
  loading, 39
  rectifier, 41, 237
  sensitivity, 39
  thermocouple, 61, 244
  volt-ohm-milliammeter, 67
Volts/div, 343
Volume resistance, 142
VOM, 67, 80
VOM adapters, 89
VOM probes, 89
VTVM, 193, 226
VVC diode, 489

W

Wattmeter, 53, 62, 63
Wattmeter calibration, 119
Waveform display, 322
Weighted resistors, 400
Wein bridge, 188, 506
Weston cadmium cell, 103
Wheatstone bridge, 132
Work coil, 516
Write gun, 384

X

xt recorder, 412
xy recorder, 419

Z

Z axis modulation, 367
Zener diode, 436
Zero control, 70, 204, 213
Zero ohms, 69
Zero position control, 8, 416

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Contents

1 The Basics of Picture Tubes 1

1.1 **Introduction** 1
1.2 **The Television System** 1
1.3 **Aspect Ratio** 2
1.4 **Frame Rate** 2
1.5 **Picture Size** 2
1.6 **Vacuum Tube Operation** 3
- 1.6.1 CRT as a Pentode 5
- 1.6.2 CRT Structure 6
- 1.6.3 Color Cathode Ray Tubes 7
- 1.6.4 Bias Controls 9
- 1.6.5 Color Purity 9

1.7 **Electron Gun Assemblies** 10
1.8 **CRT Numbering Systems** 10

2 Scanning Principles 14

2.1 **Introduction** 14
2.2 **Horizontal Scanning** 14
2.3 **Interlace Scanning** 15
2.4 **Horizontal Timing** 15
2.5 **Vertical Timing** 16
2.6 **The Raster** 16
2.7 **Electrostatic Deflection** 16
2.8 **Electrostatic Advantages** 17
2.9 **Electromagnetic Deflection** 18
2.10 **Advantages and Disadvantages** 19
2.11 **Deflection Yoke Waveforms** 19
2.12 **Mechanical Functions of the Deflection Yoke** 20
2.13 **Pincushion** 21
2.14 **Nonstandard Systems** 22

3 Vertical Deflection Systems 25

3.1 **Introduction** 25
3.2 **Vertical Block Diagram** 25
3.3 **Vertical Oscillators** 26
3.4 **Vertical Output Power Amplifier** 27
3.5 **Schematic Diagrams** 29
3.6 **Vertical Circuit Troubleshooting** 31

4 Horizontal Deflection Systems 34

4.1 Introduction 34
4.2 Partial Horizontal Deflection Block Diagram 34
4.3 Complete Horizontal and High-voltage Block Diagram 34
4.4 Damper Section 36
4.5 Focus Voltage 37
4.6 Boosted *B+* Voltage 37
4.7 Automatic Frequency Control 37
4.7.1 AFC Circuits 38
4.7.2 AFC Circuit Operation 38
4.8 Horizontal Oscillator 40
4.8.1 Multivibrator 40
4.8.2 Electron-coupled Hartley Oscillator 41
4.9 Horizontal Output Power Amplifier 42
4.9.1 Damper Diode 44
4.10 High Voltage 44
4.10.1 Voltage Multipliers 44
4.10.2 X-radiation 45
4.11 Troubleshooting 46
4.11.1 Keystone Raster 46
4.11.2 Narrow Raster 47
4.11.3 Horizontal Frequency 47
4.11.4 No Raster 47
4.12 Pincushion Correction 48
4.13 Convergence Correction 49

5 The Video Signall 54

5.1 Introduction 54
5.2 One Line of Video (Analog) 54
5.3 Horizontal Blanking Pulses 54
5.4 Horizontal Synchronizing Pulse 55
5.5 Composite Video Signal 55
5.5.1 Negative and Positive Picture Phase 56
5.5.2 Horizontal Pulse Timing 56
5.6 Vertical Blanking 57
5.7 Vertical Sync Pulse 57
5.7.1 Equalizing Pulses 57
5.7.2 Vertical Serrations 58
5.8 Line Pairing 59
5.9 IRE Units 59
5.10 Vertical Interval Test Signals (VITS) 60
5.10.1 Multiburst 60
5.10.2 Sine Squared 61
5.10.3 Vertical Interval Reference (VIR) 61
5.10.4 Closed Captioning (Q) 61
5.10.5 Color Bar Pattern 61
5.10.6 Stairstep 61
5.10.7 Closed Caption Framing Code 61
5.11 Closed Caption Reception 62
5.12 Z-axis Modulation 62
5.13 Scoping the Video Wave 63
5.14 Luminance Signal 64
5.15 Lines of Resolution 64

6 Video Amplifiers 68

6.1 Introduction 68
6.2 Basic Block Diagram 68
6.3 Signal Levels 69
6.4 Amplifier Review 69
6.4.1 Common-emitter Amplifier 70
6.4.2 Common-collector Amplifier 70
6.4.3 Common-base Amplifier 70
6.4.4 Op-amps 70
6.5 Gain versus Frequency 70
6.6 Video Amplifier Circuits 71
6.6.1 Video Output Amplifiers 72
6.7 Cascode Amplifiers 74
6.8 DC Restoration 75
6.9 Testing the Video Amplifier 76

7 Synchronization 80

7.1 Introduction 80
7.2 Introductory Circuit 80
7.3 Circuit Requirements 80
7.4 Output Signals 81
7.4.1 Vertical Integrator Output 81
7.4.2 Differentiator Output 82
7.5 Diode Sync Separators 83
7.6 Digital Countdown Circuits 83
7.6.1 Horizontal Section 84
7.6.2 Vertical Section 85
7.6.3 Other Countdown Circuits 85
7.7 Characteristics of Noise 86
7.7.1 Noise Cancelling Systems 87
7.7.2 Noise Gates 87
7.7.3 Noise Inverters 88
7.8 Troubleshooting Sync Circuits 89
7.8.1 Picture Rolls Vertically 89
7.8.2 Picture Tears Horizontally 90
7.8.3 Total Loss of Synchronization 90
7.8.4 Digital Countdown Circuits 90

8 Color 94

8.1 Introduction 94
8.2 Light 94
8.2.1 Chromaticity 95
8.3 Additive and Subtractive Mixing 96
8.4 Standard R–G–B Values 97
8.5 Compatibility 98
8.6 Color Camera 98
8.6.1 Dichroic Mirrors and Camera Tubes 98
8.6.2 Luminance Signal 99
8.6.3 Color Difference Signals 100
8.6.4 *I* and *Q* Signals 102
8.6.5 Color Area Size 103
8.6.6 Quadrature Balanced Modulation 103
8.6.7 Chrominance 105
8.7 Colorplex Frequency Spectrum 106
8.8 Summary of the Color Camera Functions 107

9 Video Monitors 111

9.1 Introduction 111
9.2 Monochrome Monitor Block Diagram 111
9.2.1 Video Amplifier Functions 112
9.2.2 Sync Separator Functions 112
9.2.3 Vertical Deflection 113
9.2.4 Horizontal Deflection 113
9.3 Low-voltage Power Supplies 113
9.4 Monochrome Monitor Schematic Diagram 113
9.4.1 Video Amplifiers 113
9.4.2 Sync Separators 116
9.4.3 Vertical Deflection 117
9.4.4 Horizontal Deflection 117
9.4.5 Regulated dc Supplies 118
9.5 Color Monitor Block Diagram 118
9.5.1 Monochrome Video 119
9.5.2 Color Video 120
9.5.3 Separate R, G, B, and *I* Inputs 122
9.6 Color Monitor Schematics 123
9.6.1 Signal Tracing 123
9.6.2 Discontinuities and Symbols 127
9.7 Troubleshooting 127
9.8 Summary 130

10 RF Transmission 133

10.1 Introduction 133
10.2 Frequency Ranges 133
10.2.1 VHF Band 133
10.2.2 UHF Channels 135

10.3 Carrier Modulation 135
10.4 Modulated Picture Phase 136
10.5 Frequency-modulated Sound 137
10.5.1 Frequency Deviation 137
10.5.2 Percent of Modulation 138
10.5.3 Deviation Sensitivity 138
10.5.4 Modulation Index 138
10.5.5 Deviation Ratio 139
10.5.6 Bandwidth 139

10.6 Direct Frequency Modulation 139
10.7 Indirect Frequency Modulation (Phase Modulation) 140
10.8 Multichannel Television Sound (MTS): Stereo 141

11 Transmission Lines and Antennas 145

11.1 Transmission Lines 145
11.2 Physical Cable Measurements 145
11.3 Standing Wave Ratio 146
11.4 Antennas 147
11.4.1 Reciprocity Theorem 147
11.4.2 Wavelength 147
11.4.3 Half-wave Dipole Antenna 148
11.4.4 Folded Dipole Antenna 148
11.4.5 Antenna Gain 149

11.5 Parasitic Arrays 149
11.5.1 Driven Arrays 150

11.6 Stacked Antennas 150
11.7 Marconi Antennas 151
11.8 Parabolic Reflectors 151
11.9 Wave Propagation 152
11.9.1 Atmosphere Layers 152
11.9.2 Ground Waves 153
11.9.3 Sky Waves 153
11.9.4 Space Waves 153

11.10 Antenna Heights 153

12 Television Receivers 156

12.1 Introduction 156
12.2 Receiver Block Diagram 156
12.2.1 VHF Tuner 156
12.2.2 UHF Tuner 159

12.3 Video IF Amplifier Section 160
12.4 Automatic Fine Tuning 161
12.5 Video Detectors 162
12.6 Automatic Gain Control 163
12.7 Luminance or Video Amplifiers 164
12.8 Color Demodulation 164
12.9 DC Restoration 167
12.10 Chassis Layout 168
12.10.1 Tuner 168
12.10.2 Video IF Amplifiers 168
12.10.3 High-voltage Horizontal Sections 170
12.10.4 Low Voltage Section 170
12.10.5 Sound Section 170
12.10.6 Color Section 170
12.10.7 Vertical Section 170
12.10.8 Video (Luminance) Amplifiers 170
12.10.9 Sync Section 171

12.11 Split Sound Receivers 171
12.12 Summary 172

13 Tuners and Remote Controls 177

13.1 Introduction 177
13.2 Tuner Types 177

13.3 Mechanical Tuners 177
13.3.1 Wafer Switch Tuners 177
13.3.2 Turret Tuners 181

13.4 Mutual Coupling 183
13.5 Neutralization 184
13.6 UHF Tuners 184
13.7 Electronic Tuners 186
13.7.1 Cable Band Frequencies 186
13.7.2 Diode Band Switching 186
13.7.3 Varactor Diode Tuning 187

13.8 Electronic Tuner Schematics 188
13.8.1 Low-band Operation 189
13.8.2 Superband Operation 190
13.8.3 UHF-band Operation 191

13.9 RF Amplifiers 192
13.9.1 Sensitivity 194

13.10 Testing Tuners 195
13.10.1 Mechanical Tuners 195
13.10.2 Electronic Tuners 196

13.11 Tuner Alignment 197
13.12 Remote Control 198
13.12.1 Infrared Transmitters and Receivers 200
13.12.2 Digital Encoding 200

14 Video IF Amplifiers, Video Detectors, and Automatic Gain Control 206

14.1 Introduction 206
14.2 IF Amplifier Circuit 206
14.2.1 Traps 208
14.2.2 Coupling Circuits 209
14.2.3 Crystal and SAW Filters 210

14.3 Video Detectors 212
14.3.1 Synchronous Detection 212

14.4 Keyed (Gated) AGC 213

14.5 Testing the Video IF Amplifiers 215
14.5.1 Testing the AGC 215
14.5.2 Testing the Amplifier and Video Detector 215

14.6 Large-scale Integrated Circuits 216
14.7 Video IF Alignment 218

15 Receiver Troubleshooting 221

15.1 Introduction 221
15.2 Safety 221
15.2.1 Isolation Transformers 221
15.2.2 Leakage Current Hot Tests 222
15.2.3 High-voltage Measurements 222
15.2.4 Handling CRTs 222

15.3 Troubleshooting Outline 222
15.3.1 No Raster 223
15.3.2 No Raster, No Sound, No ON Condition 223
15.3.3 No Raster, Normal Sound 223
15.3.4 Good Raster 223
Raster with no picture, no sound, no snow 225
Heavy snow, no picture, no sound 225
Good picture, no sound 226
Raster with no picture, but good sound 226
Good picture and good sound 226
15.3.5 Loss of Picture Synchronization 226
15.3.6 Color 226
15.3.7 Color Lock 227
15.3.8 All Channels 227

15.4 Quality 228
15.4.1 Raster Size 228
15.4.2 Raster Brightness 229
15.4.3 Picture Synchronization 229
15.4.4 Luminance Amplifiers 230
15.4.5 Color 232

15.4.6 RF Circuits and Other Conditions 235
15.4.7 Comparing Similar Effects 236

15.5 Troubleshooting by Schematic 236

15.5.1 Vertical Deflection 238
15.5.2 Horizontal Deflection and High Voltage 239
15.5.3 Low-voltage Sources 244
Switching power supplies 246
15.5.4 Cathode Ray Tubes 247
Purity adjustments 249
Gray scale adjustments 250
Static convergence 250
Dynamic convergence 250
15.5.5 Servicing Sync Circuits 250
15.5.6 Luminance 252
15.5.7 Color Circuit Troubleshooting 253
Color output amplifiers 256
15.5.8 Video IF Amplifiers, Video Detectors, and AGC 258
15.5.9 RF Section 259
15.5.10 Sound Circuits 260

15.6 LSI Schematic 262
15.7 Conclusions 270

16 Light Exchangers 271

16.1 Introduction 271
16.2 Projection Systems 271
16.3 Light-emitting Diodes 272
16.4 Liquid-crystal Displays 273
16.5 Pickup Devices 273

16.5.1 Image Orthocon 274
16.5.2 Vidicon Family 275
16.5.3 Charged-coupled Devices 275

16.6 Color Filters 278

17 Video Tape Recording 280

17.1 Introduction 280
17.2 Record Heads 280

17.2.1 Gap Size versus Frequency 282
17.2.2 Bias Voltages 284
17.2.3 Tape Transports 284
17.2.4 Head Alignment 285

17.3 Helical Scanning 285

17.3.1 Tape Track 286
17.3.2 VCR Cassette Loading 288

17.4 Block Diagram 290

17.4.1 System Control 292
17.4.2 Record Circuits 292
17.4.3 Head Switching 294
17.4.4 Playback Circuits 296

17.5 Troubleshooting VCRs 297

18 High-definition Television 300

18.1 Introduction 300
18.2 Expected Improvements 300
18.3 HDTV Timetable 300
18.4 Effects on the General Public 301
18.5 Effects on the Service Industry 301

18.5.1 Circuits that Should not Change 301

18.6 New Signal Circuits 302

18.6.1 System Overview 302
18.6.2 System Information 302

18.7 Transmitter Broadcast Mode 304

18.7.1 Data Randomizer 304
18.7.2 Reed–Solomon Encoder 304
18.7.3 Interleaver 305
18.7.4 Trellis Coding Modulation 305
18.7.5 Synchronization Information 305
18.7.6 Pilot Insertion 306
18.7.7 Preequalizer Filter 307
18.7.8 VSB Modulation 307
18.7.9 Upconverter and RF Carrier Frequency Offset 307

18.8 Receiver Broadcast Mode 308

18.8.1 Tuner 308
18.8.2 Channel Filtering and VSB Carrier Recovery 309
18.8.3 Segment Sync and Symbol Clock Recovery 310
18.8.4 Coherent and Noncoherent AGC 311
18.8.5 Data Field Synchronization 311
18.8.6 Interference Rejection Filter 311
18.8.7 Channel Equalizer 313
18.8.8 Phase Tracking Loop 314
18.8.9 Trellis Decoder 314
18.8.10 Data Deinterleaving 316
18.8.11 Reed–Solomon Decoders 316
18.8.12 Data Derandomizing 316
18.8.13 Recovery Loop Acquisition Sequencing 316

18.9 High-speed Cable Mode Conditions 316

Appendix A World Television Systems 319
Appendix B Voltage Amplifiers Versus Power Amplifiers 321
Appendix C Transistor Biasing and Class of Operation 322
Index 324

1 The Basics of Picture Tubes

1.1 INTRODUCTION

Sight and sound are two of the human senses that make up the communication link between people. Sound is related to the vibration of the surrounding air, which activates the ear drum, and sight is dependent on light to stimulate the rods and cones at the back of the eye. In a completely darkened environment (absence of light), we see only the noise impulses generated by the sensors of the eye.

Light is assumed to be daylight and contains all the color wavelengths in the visible light spectrum. The sum of all light wavelengths is seen by the eye as **white light.** We see a particular color, say red, when white light falls on a red object. All the other color wavelengths of light except red are absorbed by the dyes or pigments of the object, and the wavelength of red light is reflected to be seen by the eye.

This example serves only as an introduction to color, which will be covered in great detail at the appropriate time. Meanwhile, our discussion will be limited to a condition where the brightest areas of the picture are declared to be white and the darkest areas are destined to be black. All light intensities between these two extremes are called shades of gray. The difference between the lightest and darkest areas of the picture is called **contrast.**

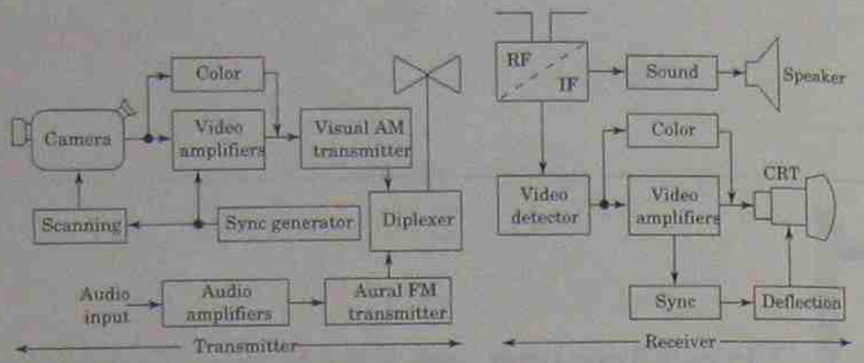
1.2 THE TELEVISION SYSTEM

We will use the theories of sight and sound throughout this entire text. Therefore, a brief exposure to a model system is needed so that when the sections, circuits, and signals are introduced, we will have a feel for where they fit in the overall plan.

In Figure 1.1, the transmit section contains two completely independent transmitters. The visual transmitter includes a camera to convert light images to electrical signals and separate color and video processing sections and a combined *amplitude-modulated* power output section. The scanning and synchronizing sections are the timing circuits for the visual signal. The sound section is a standard *frequency-modulated* transmitter whose output is diplexed with the AM visual signal and fed to a single antenna system. The two transmitters use different forms of modulation so that there is no interference between signals when mixed at the antenna. The two-transmitter system also allows the station to signal the viewer by picture when the sound transmitter is not operating and by sound when the visual transmitter is in trouble.

The receiver part of Figure 1.1 identifies a superheterodyne receiver that selects a station and then separates the FM sound from the AM picture. After removing the picture signal from the carrier, the color part is processed separately from the monochrome part before they are applied to the picture tube. The deflection circuits are the receiver's counterpart to the scanning circuits in the transmitter. The sync circuits keep the receiver in time with the transmitter. You may recognize many familiar sections in the system of Figure 1.1 and realize that the major differences between radio and television are the camera at the transmitter and

FIGURE 1.1
An introductory sketch of a television RF system.



the cathode ray tube at the receiver. We will first study the cathode ray tube.

1.3 ASPECT RATIO

The movie industry was already established when television was introduced to the general public. It was natural that television copied some of the basic features from motion picture technology. Research by the movie pioneers had revealed that it was more comfortable to move the eyes sideways than it was to move them up and down. For this reason, the movie screen and the television screen are 4 units wide for each 3 units of height. This size standard is called the **aspect ratio** and is stated as 4:3. In later years, the movie industry gradually increased to a 7:3 aspect ratio for wide-screen pictures, but television, once set, was locked into the 4:3 aspect ratio. We will see that a larger aspect ratio is planned for high-definition television (HDTV), which is covered in its entirety at the end of this text.

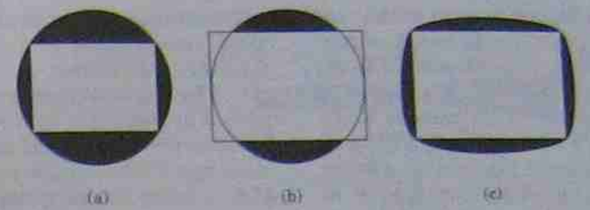
1.4 FRAME RATE

One frame is one complete picture. The process for motion pictures is that a picture is shown on the screen, the shutter is closed to black out the screen, the picture is changed, and the shutter is opened again to show the next frame. Each picture is altered slightly to show motion. At the start, movies were shown at 16 frames per second and if you have seen movies of this era, you were aware of a flickering light pattern (hence the name the flicks) and a very jerky, robotic nature of the movements. As the movie industry matured, the frame rate was changed to 24 frames per second to avoid the flicker and to smooth out the action, making it appear less mechanical. Further advances have each frame shown twice. That is, show one frame, close the shutter, open the shutter, close the shutter, then change the picture, and so on for 24 frames per second, but 48 exposures per second. This works for fast action movies and minimum flicker rate. Television, on the other hand, could not operate at the 48-picture rate because of the interference between the 48 shutter speed and the 60-hertz (Hz) ripple pattern from the power supplies. Therefore, television runs at 30 frames per second (30 complete pictures), or 60 Hz of the ac line divided by 2.

1.5 PICTURE SIZE

The size of the movie screen is limited only by the intensity of the projector lamp, which may be air cooled. A movie screen size of 20 ft by 15 ft might be an average. The size of the television screen is limited to the size of the **cathode ray tube** (CRT) face area. Figure 1.2 shows the progression of **raster** size (the lighted area on the face of the CRT) to the CRT face size. Early television receivers used CRTs that were standard size for oscilloscopes in use at that time. The 3- and 5-in. diameter round tubes were popular sizes. Using the 5-in. round CRT for this example, Figure 1.2a shows that the 4:3 aspect ratio raster will just fit on the screen size (from the 3, 4, 5 triangle of basic trigonometry). With a 4:3 aspect ratio, you will generally know the diagonal (D) size of the CRT. The width then becomes $0.8D$ and the height is $0.6D$. The important idea here is that the diagonal measurement of the raster (hypotenuse) is the same size as the diameter of the CRT. Out of fairness to the general public, this method of measuring picture size from corner to corner became standard and is the same size for a round tube and rectangular tube alike. Notice the wasted tube face area in Figure 1.2a (shaded) and imagine the cabinet size to house the CRT. Picture tubes (CRTs) at

FIGURE 1.2
A 4 : 3 raster ratio and relevant cathode ray tube face size: (a) raster totally enclosed on a round CRT; (b) raster expanded to full tube width; (c) same raster size as in part (b) on a rectangular CRT.



that time had to be made round because we did not have the technology to make them rectangular and safe at the same time until years later.

The next progression is seen in Figure 1.2b. Using the same CRT size as before, 5-in. diameter, but enlarging the raster size to use the full width of the CRT face increased the viewing area by greater than one and one-half times (4 × 3 compared to 5 × 3.75). The corners of the picture were lost, but since the action was generally at the center of the screen, no one objected to the trade-off of corner loss for larger picture size.

The third progression was the development of the rectangular CRT shown in Figure 1.2c, which accounts for both the larger picture size and full efficient use of the CRT face.

1.6 VACUUM TUBE OPERATION

The cathode ray tube is a vacuum tube. Vacuum tube principles can be summarized as follows. These conditions prevail only in a vacuum; they cannot exist in air. Thus, if the glass envelope is defective in any way, air will seep back into the tube and it will not operate.

The cathode (kathode) is established as the current-emitting element. It is coated with a chemical such as boron or cesium oxide that, when heated, boils and emits electrons. The process is similar to a pan of boiling water that gives off steam. This is called *thermionic emission* and is illustrated in Figure 1.3a. Figure 1.3b shows the heater (or filament) as a twisted piece of resistance wire that glows red hot when a voltage (ac or dc) is applied to its terminals. The heater voltage may range from 1 to 50 volts (V) and is the first number of the tube designator. A 6SN7 tube requires 6 V at the heater. A 12SN7 is the same tube but requires 12 V at the heater. Most small vacuum tube heaters draw current that varies in 150-milliampere (mA) steps. Heater currents may be as high as 180 amperes (A) for transmitting power tubes such as the 6166A. The heater is not counted as one of the tube elements.

The **cathode,** often a metallic cylinder around the heater, emits electrons that remain close to the cathode surface in a space charge until acted on by another force.

The **anode** is the second element of the tube. It may be a larger metallic cylinder placed around the outside of the cathode, as seen in Figure 1.3c. When a positive potential is applied to the anode (or **plate**), the negatively charged electrons are attracted through the vacuum to the positively charged anode. The passage of electrons through the vacuum tube from cathode to anode sets up the theory of electron flow as current, which will be used throughout this text. The two-element tube (cathode and anode) make up the vacuum tube diode.

FIGURE 1.3
The structure of a vacuum tube (anode, cathode, and heater): (a) symbolic representation; (b) physical heater and cathode structure; (c) adding the anode (plate).

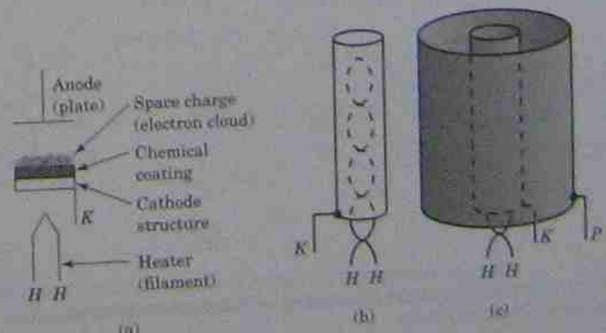


Figure 1.4 shows the progression of the vacuum tube family. Adding a single-ended, widely spaced coil of wire between the cathode and anode makes the tube act like a valve. When a voltage of negative potential compared to the cathode is applied to this coil (called a **control grid**), it opposes the flow of electrons through the tube. A weaker negative voltage difference allows more current to flow. In this manner, the changing voltage on the control grid causes the changing anode current that flows through the external load resistance to develop the output signal voltage. The three-element tube (cathode, control grid, and anode) of Figure 1.4a is called a **triode.**

Further development used the idea that if one positively charged anode would attract electrons then two positively charged elements would attract twice as many electrons and increase anode current. The idea was implemented by placing a second single-ended, widely spaced coil of wire between the control grid and the anode with an applied positive potential. The element was named the **screen grid,** and the tube was called a **tetrode** (four-element tube); it is shown in Figure 1.4b.

The tetrode performed as predicted up to a point. That is, as the plate and screen voltages were increased, the anode current increased linearly. A level was reached where a further increase in voltage caused a decrease in anode current. After another small change in anode voltage, the anode current again increased linearly with voltage. This region of decreasing anode current was called the **negative resistance** region and was due to the increased velocity of the electron striking the anode and bounding back to be drawn out of the tube by the positive potential of the screen grid as screen grid current. This phenomenon, called **secondary emission** is shown graphically in Figure 1.4c and exists only over a small range of applied voltage. This negative resistance region is also found in tunnel diode and pin diode characteristic curves; all three devices make good oscillators, but find very few other applications.

The secondary emission in tubes was controlled by placing a fifth element inside the tube between the screen grid and the anode. This element again was a single-ended, widely spaced coil of wire called the **suppressor grid** that was connected to the cathode or to ground at a very low potential. It opposes the secondary emission electrons and returns them back to the anode to exit the tube as plate current. This five-element tube, having a cathode, control grid, screen grid, suppressor grid, and anode, is called a **pentode** (Figure 1.4d).

Attached to the anode is a flash pot, called a **getter,** that contains a deposit of silver oxide that flashes when power is applied to the tube for the first time. The flash consumes whatever oxygen remains within the tube after the vacuum pumps have reached the limit of their capacity. A silver deposit can be seen on the inside surface of the glass. When any defect allows air to seep back into the tube, this silver deposit turns a chalky white.

To summarize vacuum tube voltage relationships, it is most important to remember that the control grid voltage is always negative compared to the cathode voltage. The range may vary from -0.1 to -25 V depending on circuit design. Second, the screen grid and anode voltages are always positive compared to the cathode voltage. The screen grid and anode may be the same potential. When they are not, the screen grid voltage is lower by about 10% of the anode voltage: for example, anode = +100 V dc, screen grid = +90 V dc. The range of screen grid and anode voltage may be from +40 V dc to several thousands of volts dc. Finally, the suppressor grid is often at the same level as the cathode voltage or at ground potential.

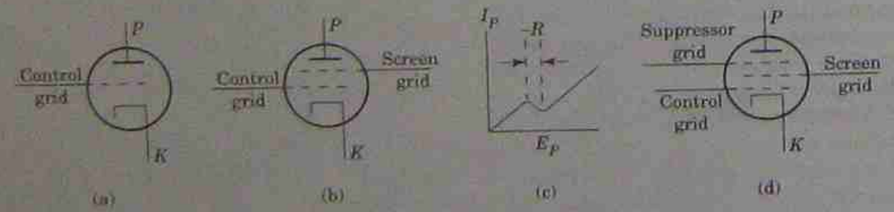


FIGURE 1.4
The vacuum tube progression: (a) triode; (b) tetrode; (c) negative resistance of the tetrode plate current characteristic curve; (d) pentode tube.

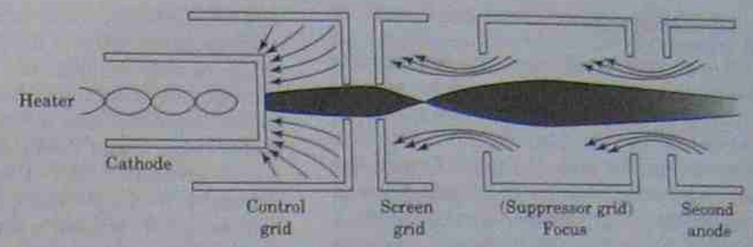


FIGURE 1.5
Electron gun structure. Mounting and support structure not shown. Lines with arrows are electrostatic lines of force between elements. The shaded area is the focused electron beam.

1.6.1 CRT as a Pentode

Although the cathode ray tube is truly a pentode, it differs from the common receiver pentode in two distinct ways. First, the cathode and grids are structured to focus the cathode current into a very narrow electron beam. Second, the anode and cathode are physically far apart so as to require an extremely high anode voltage to draw a small anode current.

The cathode and grid structure is illustrated in Figure 1.5 and is called an **electron gun.** The grids are metallic cylinders with a hole at the center that will confine the flow of electrons to a narrow beam. The electrostatic lines of force formed by the potential difference between electrodes are shown as curved lines with arrowheads. Upon leaving the cathode, the electron beam converges in the area of the screen grid and then diverges again. The lines of force at the screen grid, focus grid, and second anode form the electrons into a narrow beam again by the time that they reach the face of the cathode ray tube. The point of convergence should occur right at the CRT face for best focus. The convergence point is controlled by the voltage placed on the focus electrode. In all future sketches, the electron gun will be shown as in Figure 1.7, rather than redrawing the individual grid structures.

The CRT bias arrangement of Figure 1.6 shows the bias voltage versus cathode current in diagram (a). This curve places the CRT in cutoff when the bias reaches about -80 V dc (control grid negative compared to the cathode). A change in bias voltage causes a change in cathode current, which also changes the brightness on the face of the CRT. The bias and brightness can be changed by adjusting the dc voltage on the cathode or the control grid. Figure 1.6b shows a change in control grid voltage from a negative dc source. Figure 1.6c has the cathode voltage changing from a positive dc source. Either way is correct when you remember to keep the control grid negative compared to the cathode. The screen grid has the same current accelerating function in the CRT as it had in other receiving tubes. Because the anode is so far away from the screen grid, there is no need for a suppressor grid; therefore, the suppressor grid position can be used effectively to control the beam size and functions well as a focus electrode.

The CRT heater normally operates at 6.3 V ac or dc drawing an average of 600-mA heater current.

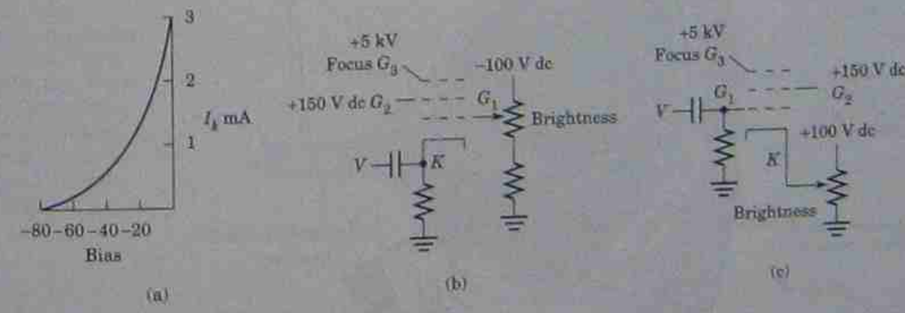


FIGURE 1.6
CRT bias adjustment arrangements: (a) the curve for bias voltage versus cathode current; (b) changing the control grid voltage to change brightness; (c) changing the cathode voltage to change brightness.

1.6.2 CRT Structure

Figure 1.7 is a cutaway side view of a monochrome CRT. *Monochrome* means a single color or, as used here, will imply a black and white picture tube.

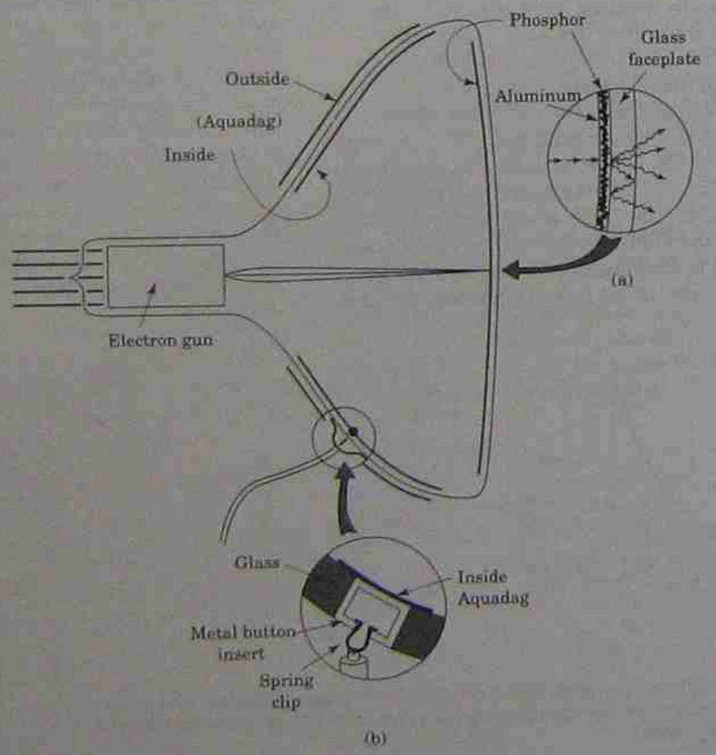
The electron gun is shown in the figure as a single assembly in the neck of the CRT, with the connecting wires extending to the left and through the glass envelope to the outside. The gun emits a narrow beam of electrons to the right and produces a finely focused dot of light on the CRT face at the center.

The inside surface of the CRT face is coated with a *phosphorescent* material such that when it is bombarded by a high-velocity electron beam it gives off light. This action is highlighted in Figure 1.7a. The phosphor material radiates *photons* of light, which vibrate at a wavelength that corresponds to the dominant color represented by the chemical composition of the phosphor.

The electrons strike the phosphor, give up their energy in the form of light, and then fall back as a slower-velocity electron to be collected by the anode. Brightness efficiency can be increased by (1) emitting more electrons in the form of higher cathode current by raising the cathode temperature, or (2) increasing the level of anode voltage. Excessive current will cause the wide-angle photons to reflect at the outside surface of the glass face, back to the inside surface, and then reflect again outwardly as a halo around the dot of light where the electron originally hit the phosphor screen. Try this on your oscilloscope by setting a single dot of light at the center of the screen and adjusting the brightness all the way up.

The bell area of the CRT is painted on the inside (not including the inside face) with a composition of powdered graphite and banana oil called **Aquadag** to form the anode of the CRT. The inside Aquadag makes contact with the metal button embedded in the glass wall for connection to the anode voltage supply. See Figure 1.7b. A coating of Aquadag is also painted on the outside of the CRT, excluding a 5-in. circle around the anode button. The outside coating is grounded by a spring clip at the time of installation. The inside and outside Aquadag coatings are separated by the glass wall of

FIGURE 1.7
A cutaway side view of a monochrome cathode ray tube: (a) detail of the phosphor layer at the faceplate; (b) detail of the anode button on the side of the CRT.



the CRT to form a high-voltage filter capacitor of about 2500 picofarads (pF), with a breakdown voltage rating of 50,000 working volts.

An insulating suction cup is used at the CRT end of the high-voltage wire. It surrounds the wire and tension clip that attaches the high-voltage wire to the metal button in the glass wall. The suction cup is said to be used for protection of the technician against electric shocks. It does this, but its prime function is to keep dust from causing high-voltage arcing. The CRT is an electrostatic dust collector, and dust can provide a high resistive path to ground for high-voltage leakage. The leakage will first appear as a hissing sound that later turns to an arcing sound. When removing the high-voltage lead, first discharge the anode capacity; then peel back the suction cup and pinch the spring clip together to remove the connection from the CRT button.

Referring again to Figure 1.7a, you may have noticed the aluminum coating on the inside surface of the phosphor at the face of the CRT. This aluminum layer is to prevent **ions** from striking and burning the phosphor layer. The electron gun emits ions as well as electrons. The ions are 10 times as heavy as the electron, so when we talk about moving the electron beam around, the ion will move one-tenth the distance of the electron. A heavy concentration of ions at the center of the CRT leaves a brown burn spot on the phosphor. In earlier days, to avoid this condition, the electron gun was bent and an **ion trap** (or beam bender) was used to bring the electron beam back to the center of the CRT face. The heavier ions (not bent as well) are dissipated in the electron gun. Further discussion on this subject seems useless since bent guns and ion traps have not been used for several decades, and you may never see one in your lifetime.

1.6.3 Color Cathode Ray Tubes

All aspects of reproduction are covered at one time in Chapter 8. But when we get there, it would be redundant to discuss the CRT all over again just for color. The basics of color CRTs are explained here, even though there is still much to be studied before a full understanding of color is gained.

The principal idea to be presented here is the concept that the equivalent of three CRTs can be separately operated within one glass envelope. The color phosphor screen is made up of three chemically different deposits that correspond to the primary colors. One phosphor will emit **red** photons of color light when bombarded by electrons, another, **blue** photons of light, and a third, **green** photons of color light. To make this happen, three identical electron gun assemblies are mounted in the neck of the CRT. They take the color name that corresponds to the color phosphor that each will activate. The next arrangement needed is one that will permit each gun to activate only the color phosphor for which it is responsible, without activating the other two phosphors. This comes in the form of a thin, perforated, Mu-metal sheet called a **shadow mask** that is placed close to the CRT screen as seen in Figure 1.8. The holes in the shadow mask are aligned so that each electron beam will pass through each hole and strike only one set of phosphor dots.

FIGURE 1.8
Cutaway view of a color cathode ray tube. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 626, Robert J. Schoenbeck. © 1992.)

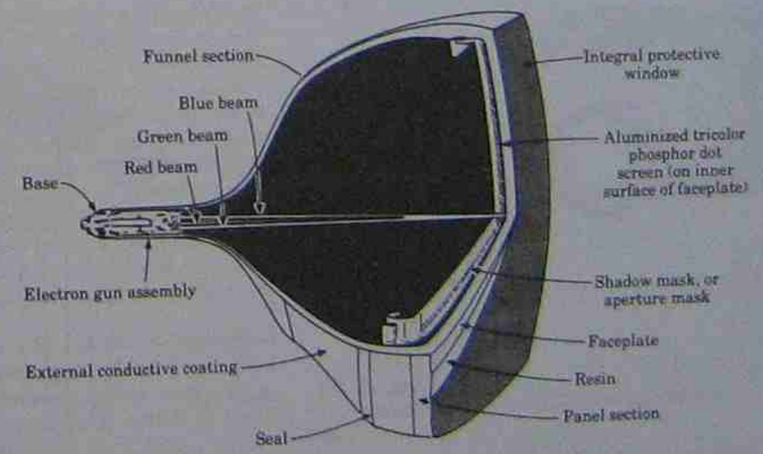


Figure 1.9a illustrates how the three electron beams converge (cross over at one place) as they pass without interference through one hole in the shadow mask to energize the individual phosphor dots. The holes are photoetched into the shadow mask to ensure quality and reproducibility. There are about 350,000 holes in the shadow mask for a 21-in. tube, or 211 square inches (16.8 in. times 12.6 in.).

Figure 1.9b is a side view of the shadow mask to show how the holes are beveled in order to allow most of each electron beam to reach the phosphor screen. More beam current means more brightness.

Figure 1.9c shows how the phosphor dots are arranged so that any three adjacent dots form a triad of dots associated with each hole in the shadow mask. The right side of Figure 1.9c is shaded to illustrate that the area not covered with dots is darkened to improve contrast. Each phosphor dot has a diameter of about $\frac{1}{4}$ in. (0.015625 in.), or about 1650 of each color dot per square inch (4950 total dots per square inch).

Figure 1.9d shows elongated slots in the shadow mask and the association of phosphor stripes that may be used in some cases to increase the light output of the color CRT.

The shadow mask needs some structural support to maintain its shape, which in turn blocks some electrons from reaching the phosphor screen. The efficiency of the shadow mask is 55% to 70%, depending on the mask pattern, when compared to a monochrome CRT. Additionally, the phosphor materials have lower efficiencies. Green tops the list with 70%, and red comes in last at 40% compared to the light output of a monochrome CRT under the same conditions. When all these negative factors are taken into account, coupled with the three-gun assembly, it is easy to see why the high voltage must be 25 to 30 kilovolts (kV) to produce the same light output as the equivalent-sized white CRT, with a high voltage of 12 to 15 kV.

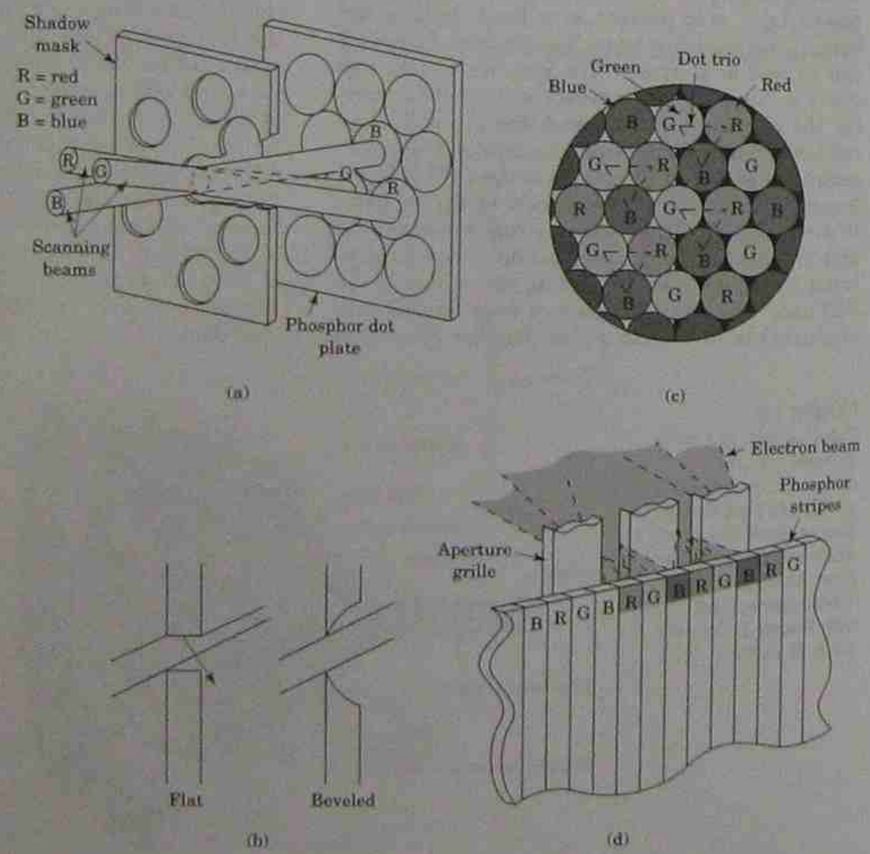


FIGURE 1.9
Relationship between the three electron beams, the shadow mask, and the phosphor screen (see text).

1.6.4 Bias Controls

The dc voltages applied to the base of the color CRT allow the CRT to be operated in two distinct ways. For example, when all three control grids are connected together and the applied dc voltage is varied, the three electron guns increase or decrease conduction equally to change the overall brightness. This control is called the **master brightness** control. At the same time, the three screen grids may be connected to separate controls for different dc voltage settings. These controls change how each electron gun contributes to the overall brightness. Some products identify these controls as the **red, green** and **blue bias** controls and, in effect, they are individual brightness controls for the three primary colors. Ideally, the industry standard for a white raster is obtained when the red phosphor contributes 30% of the overall brightness, the green phosphor, 59% of the overall brightness, and the blue phosphor contributes 11%.

In the majority of the cases, the **"standard white raster"** is set up by eye, using these three controls, to what you will learn to call white. But you will be hard-pressed to find two people who will agree on any specific setting for white. The correct technical procedure for white setup is covered in Chapter 15, where other considerations, not covered yet, are taken into account.

1.6.5 Color Purity

Purity is defined as equal intensity of a single color over the entire face area of the CRT. Each color is examined separately by using the bias controls to display one color at a time. Color contamination creeps into the system when the metal parts around the CRT face become magnetized, including the shadow mask. The renegade magnetic field distorts the path of the electron such that the beam will pass through the shadow mask and strike the wrong set of phosphor dots in some areas but not in other areas. Color purity distortion can occur at any place on the CRT face, in different colors and amounts.

Color purity can only be restored by demagnetizing the metal parts around the face of the CRT. This means exposing the magnetized section to a high-intensity ac magnetic field, which is then slowly reduced to zero.

In practice, a degaussing coil (demagnetizing coil) is plugged into 120 V ac, 60 Hz. Place the coil flat against the CRT face as seen in Figure 1.10, apply power, move the coil around the entire face area of the CRT several times, move the coil away from the CRT to arm's length, turn the coil 90° to the CRT surface, and turn the coil power off.

There is a built-in degaussing coil in every color TV receiver. It electrically connects in the low-voltage power supply circuit and is active every time the power is turned on. The field comes on strong but is made to decrease slowly until it is rendered inactive within 2 to 3 minutes after turn on.

There are commercially available degaussing coils or you can make your own coil. To do so, use 1000 ft of no. 22 enameled wire wound in a 12-in. diameter circle, wrapped with electrical tape and attached to an ac line cord with a series switch.

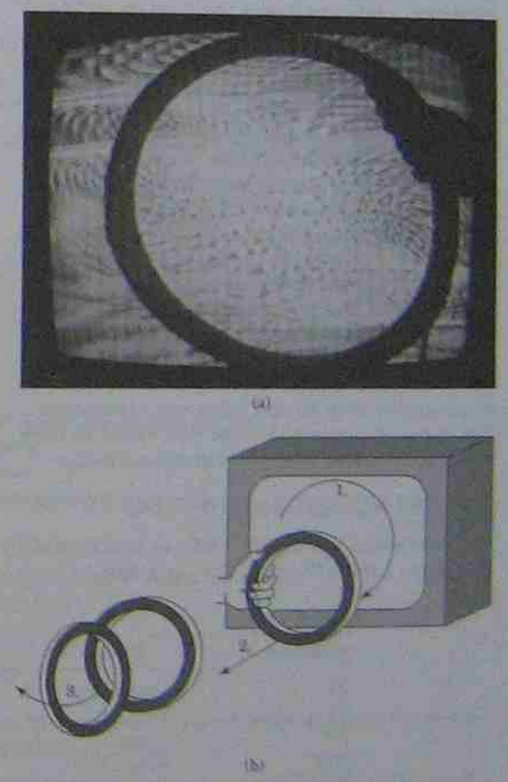


FIGURE 1.10
The three movements to degauss the cathode ray tube.

1.7 ELECTRON GUN ASSEMBLIES

The three electron guns can be arranged in the neck of the CRT in two configurations, the delta gun and the in-line gun arrangement.

The **delta gun** assembles the three guns in a triangle arrangement that allows for the smallest neck size and a smaller yoke. The disadvantage is that none of the three guns are on the same centerline axis. The point of convergence will be different at the top and bottom or from side to side compared to the center of the shadow mask. The picture will be color fringed around the outside edges of the CRT. Convergence correction will be treated later.

The **in-line gun assembly** has all three guns placed side by side by side. The CRT neck is slightly larger, but now there is no vertical convergence problem because all three guns are on the same horizontal center line. There is still a need for horizontal convergence, but the total correction is less than for the delta gun.

The **trinitron** assembly emits three electron beams from three cathodes exactly like the other in-line units. However, there is only one control grid, one screen grid, and one accelerating grid, which are shared by the three electron beams. The assembly is wider than it is high, but still small, and is advertised as a one-gun color tube. The major advantage is how the convergence is arranged. As an in-line gun assembly, no vertical convergence correction is required. In the horizontal direction, the center electron beam is shielded and needs no correction. Only the two outside beams (left and right) need to be corrected to match the pattern of the center beam. The overall convergence correction is much simpler than for any other gun arrangement. The in-line gun assemblies are well suited to work with color phosphors deposited in vertical stripes.

1.8 CRT NUMBERING SYSTEMS

The numbering system for CRTs is broken down into three parts. The first part is a one- or two-digit number to indicate the diagonal size of the tube in inches. In general, the tube industry seems to have settled on the odd-numbered standard for this category, as 5, 7, 9, ..., 19, 21, 23, 25, 27, and 30 in. (the exception), with 13, 19, and 23 in. as the most popular choices. This gives a ±1-in. variation to the actual tube size compared to the number designation.

The second part contains two uppercase letters that are most meaningful to the manufacturers. They identify such characteristics as mechanical mounting and element spacing of the electron gun, as well as neck diameter.

The third part identifies the phosphor screen color and persistency. Persistency is the length of time that the phosphor will remain active after the energy source has been removed. You want a long persistency for radar, for which the screen information may be reinforced only five or six times per second, but a short persistency when high-speed action is required in great detail. Table 1.1 lists the most common phosphors.

In the examples in Table 1.2, the 19EZP4 is a 19-in. (first part) black and white (last part) picture tube and the 23EGP22 is a 23-in. (first part) color picture tube (last part).

A new system seems to be emerging on an international level that calls itself the Worldwide Type Designation System (WTDS) and consists of a five-part designator. The first symbol is a single letter that may be an A to signify a television picture tube or the letter M to identify a tube for a computer monitor. (Test equipment, radar, and other special-purpose tubes are unidentified at this time.) The second part contains two digits that show the CRT size in centimeters. The third part has three uppercase letters to show the country of origin. Letters AAA through DZZ are tubes made in the United States. EAA through HZZ are tubes made in Europe, and JAA through MZZ are tubes made in Japan.

The fourth part has two uppercase letters that mean the same as the two letters in the present system, that is, the phosphor types and persistencies, which are not spelled out at this time. The fifth part has only two symbols; they are an X for color tubes and a WW for black and white tubes.

An example would look like A58BCAEGX. This tells you that it is a television picture tube (A), 58 centimeters in size (about 23 in.), is made in the United States (BCA), with some mechanical specifications (EG), and is a color tube (X). The system is not fully formulated yet, so we need to pay close attention to this system and update it as more information becomes available.

TABLE 1.1

Number	Color	Persistency	Comments
P1	Green	Medium	
P4	White	Short	
P7	Sepia	Short	
P11	Blue	Medium	
P14	Blue-orange	Long	
P15	Green	Long	
P22	R–G–B	Medium	Color TV

TABLE 1.2

Black/White	Color
19EZP4	15VADP22
21FVP4	19VDCP22
23CQP4	23EGP22

QUESTIONS

1.1 White light is the _____ in the visible light spectrum.

1.2 The difference between the lightest and darkest areas of a picture is called _____.

1.3 The different levels of shading between maximum light and darkness are called _____.

1.4 A typical television station uses how many transmitters?

1.5 The form of modulation for the visual signal is
- **(a)** AM,
- **(b)** FM,
- **(c)** DSSC,
- **(d)** SSB.

1.6 The form of modulation for the aural signal is
- **(a)** AM,
- **(b)** FM,
- **(c)** DSSC,
- **(d)** SSB.

1.7 The modulated visual and aural signals are sent to
- **(a)** separate antenna systems,
- **(b)** the same antenna system, or
- **(c)** they do not use antenna systems.

1.8 The aspect ratio for television is _____.

1.9 What are the width and height measurements for a 25-in. CRT?
H = _____, W = _____.

1.10 A frame is defined as _____.

1.11 The frame rate for television is _____.

1.12 To make a fair comparison between round and rectangular tubes, the size of a round tube is a measure of the _____.

1.13 To make a fair comparison between round and rectangular tubes, the size of a rectangular tube is a measure of the _____.

1.14 What is the tube size of a 21ARP4 CRT? _____

1.15 The 21ARP4 tube is a
- **(a)** color tube,
- **(b)** black and white tube.

1.16 The 21ARP4 tube is a
- **(a)** round CRT,
- **(b)** rectangular CRT, or
- **(c)** you cannot tell from the tube number.

1.17 Which of the following statements is true? (1) The control grid must always be negative compared to the cathode; (2) the cathode must always be positive compared to the control grid.
- **(a)** 1,
- **(b)** 2,
- **(c)** neither,
- **(d)** both

1.18 Which of the vacuum tube elements emits electrons?
- **(a)** the heater,
- **(b)** the cathode,
- **(c)** the control grid,
- **(d)** the screen grid,
- **(e)** the anode

1.19 A three-element tube is a
- **(a)** diode,
- **(b)** triode,
- **(c)** tetrode,
- **(d)** pentode,
- **(e)** CRT.

1.20 Secondary emission is a problem in which of the following tube types?
- **(a)** diode,
- **(b)** triode,
- **(c)** tetrode,
- **(d)** pentode,
- **(e)** CRT

1.21 The inside surface of the CRT face plate is coated with _____.

1.22 The inside surface of the CRT bell area is coated with _____.

1.23 The inside coating of the bell area of the CRT is which element of the vacuum tube?

1.24 What causes the CRT to hold a voltage charge?

1.25 P1 phosphor gives off what color light?

1.26 P22 phosphor gives off what color light?

1.27 How many electron guns does a color picture tube have?

1.28 A shadow mask is
- **(a)** a mask worn by the Shadow,
- **(b)** a filter screen near the phosphor layer,
- **(c)** a screen in the neck of the CRT,
- **(d)** used in both monochrome and kodachrome CRTs.

1.29 Convergence means to
- **(a)** align the electron beams to the correct phosphor dots,
- **(b)** line up in series,
- **(c)** line up in parallel,
- **(d)** mix colors.

2 Scanning Principles

2.1 INTRODUCTION

Sometime when you are bored, take a flashlight into a room at night, turn off the lights, and shine the flashlight on the wall. Wiggle the flashlight as fast as you can and you will see a line of light displayed on the wall. You know that there is only one beam of light, yet you see a line of light. This is a major principle in the art of re-creating a television picture. It takes into account the persistency of two pieces of the system.

Persistency was defined in Chapter 1 as a property of the phosphor composition to glow for a period of time after the energy source is removed. That's the first piece. The second piece is the persistency of the human eye, which you demonstrated by wiggling the flashlight. The eye has a persistency of vision of about $\frac{1}{16}$ second(s). That is, if you looked at a $1000.00 bill and then suddenly the money vanished, your eye would hold the vision of the money for $\frac{1}{16}$ second after the bill was gone (however, your mind may hold the vision for a longer period of time). This is why the motion picture industry started out at 16 frames per second. The combination of the persistence of the phosphor and your eye will allow your mind to see a moving image made from a rapidly changing series of still pictures. When you increase the picture rate (frame rate), you dissolve the flicker condition.

2.2 HORIZONTAL SCANNING

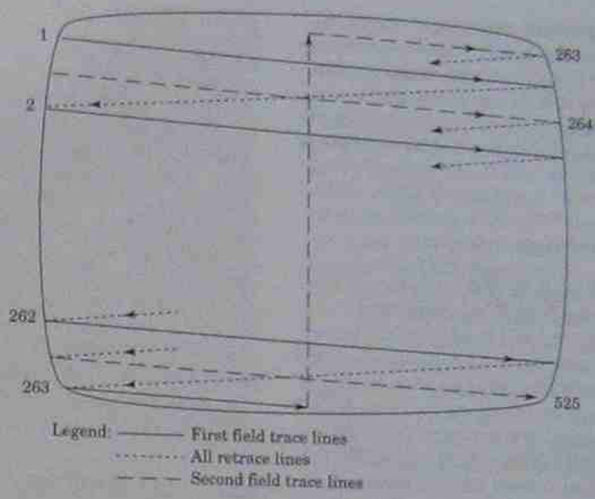
In Chapter 1 it was stated that the beam from the electron gun hits the phosphor screen and causes the phosphor to give off light. The light is in the form of a dot at the center of the CRT face.

To start the scanning process, the dot is first moved to the *top-left* corner of the CRT face. The second action is to move the dot of light sideways across the face of the tube to the right and slightly downward. Upon completion of this step, and to continue the action, the dot must be returned to the left side of the CRT and slightly lower than where the first line started. A second line of light is traced out as the process moves again to the right and slightly downward. Examine Figure 2.1 to see how this looks on the face of the CRT. The progression is much the same as reading in English, moving from left to right on each line and then downward to start at the left again.

The horizontal movement will continue until 262.5 lines have been traced out on the screen. Ending with one-half line tells you that the trace ends at the bottom center of the screen. The beam will then maneuver to the top center of the screen to finish tracing the 263rd line.

But let's stop here for a minute and see what we have before the system gets too far ahead of us. First, we traced out 262.5 lines that go from left to right. Second, we moved from the top-left corner down to the bottom center. So, although this section is titled "horizontal scanning," we have also scanned vertically. It is called horizontal because the lines of light that the eye can see lie in a horizontal position. The sequence of lines advances vertically downward. The total presentation of 262.5 horizontal lines is called **one field** and is completed in $\frac{1}{60}$ second (the reciprocal of 60 Hz).

Figure 2.1
Interlaced horizontal scanning.



OK, back to the system again. The dot of light has been brought up to the top center of the screen and completes tracing line number 263. If this trace starts at the center and moves slightly downward as the very first line did, it cannot occupy the same space as the first line. Furthermore, as we bring the beam back to the left to begin another trace (line 264), it would start midway between lines 1 and 2. This is the start of the **second field,** which continues the second set of 262.5 lines to end at the bottom-right corner of the screen.

Let's recap again. The first field had 262.5 horizontal scan lines and took $\frac{1}{60}$ second to complete. The second horizontal field also had 262.5 scan lines and took the same length of time to be completed. The two fields together total 525 lines and are called a **frame.** The time for one frame is $\frac{1}{60}$ or $\frac{1}{30}$ s, which converts to 30 **frames per second.** Thirty frames per second translates into 30 complete pictures per second in later discussions.

2.3 INTERLACE SCANNING

The technique of laying down one field of lines and then placing the second field of lines in the space between the first set of lines is called **interlace scanning.** It serves three purposes. First, it allows the vertical rate to be the same as the ac line frequency of 60 hertz (Hz). This causes minimum interference between the vertical circuit and the power supply ripple. Second, by the time that the first field is nearing completion, the beginning lines are starting to fade out because of the selected phosphor persistency. The second field reasserts a brightness level from the top to the bottom of the screen and creates the sensation of a continued brightness level for the full frame. Third, it allows the frame rate for television and the frame rate of motion pictures to be nearly compatible. Movies can now be shown on TV without a great deal of conversion in the frame rate sections of either product.

By the time the third field starts (first field of the second frame), the beginning lines of the very first field have completely faded and the second frame can be displayed without interference.

2.4 HORIZONTAL TIMING

Presenting 30 frames per second at 525 lines per frame results in a horizontal scanning frequency of 15,750 Hz (30 × 525 = 15,750). The time for one cycle is the reciprocal of the frequency (1/15,750) or 63.492 microseconds (μs) per cycle. This is generally rounded off to 63.5 μs).

Moving the electron beam from left to right across the face of the CRT is called a **trace.** Returning the electron beam back to the left side of the CRT is called the **retrace.**

It stands to reason that the beam should move at a constant speed all the way across the tube face for good linearity. The retrace back to the left should occur in a much shorter period of time and,

in all likelihood, will also be linear. By NTSC* standards, the horizontal retrace time is limited to 18% ± 0.5% of the horizontal scan time, or about 11.43 μs (rounded to 11.5 μs). This leaves 52 μs for the trace time. A linear trace of 52 μs and a linear retrace of 11.5 μs describes a **sawtooth** waveshape to move the beam.

2.5 VERTICAL TIMING

The reciprocal of 60 Hz is 16.666 milliseconds (ms) and is the time for one field. The action used to describe the horizontal scan will hold true for the vertical scan. That is, moving the beam slowly down the face of the CRT and then rapidly back to the top again also describes a sawtooth action. The NTSC standard for the vertical retrace time is 8% of the time for one cycle, or 0.01666 × 0.08 = 1.33333 ms. Comparing the vertical retrace time in terms of the horizontal cycle time is 1.3333 ms divided by 63.492 μs = 21 horizontal cycle time periods. This means that of the 262.5 horizontal scan lines in one field a maximum of 21 lines per field could be lost to the retrace action. From the total of 525 lines, 483 lines or more per frame remain active for picture information.

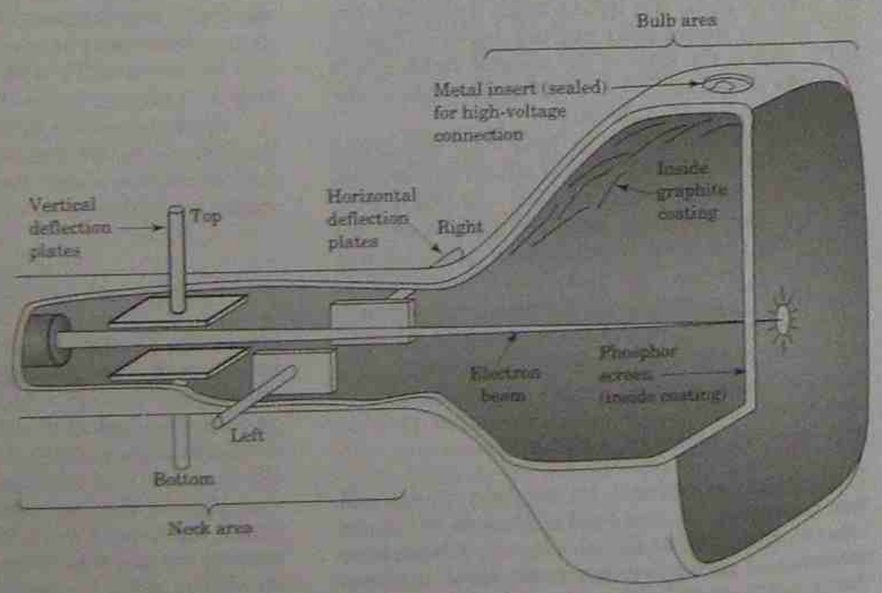
2.6 THE RASTER

As you become more involved with video display systems, you will find that the first question to be asked is, "Do you have a raster?" The raster is the display of light on the face of the CRT that is produced by the scanning lines. You do *not* need a picture to have a raster. The picture will appear on the raster when a video signal (picture signal) from other circuits is added to the input of the CRT. However, you do need a raster in order to be able to see the picture. You *cannot* have a picture without first having a raster. Moving the electron beam around on the face of the CRT to produce a raster in the manner described can be accomplished by one of two methods. These are, the application of electrostatic forces or electromagnetic forces to the CRT from external circuits.

2.7 ELECTROSTATIC DEFLECTION

In this method, four small metallic plates are placed inside the neck of the CRT in the area just forward of the electron gun. They are assembled in two sets of two plates each and positioned such that the electron beam passes between each set of plates. Figure 2.2 shows the horizontal deflection

FIGURE 2.2
Cathode ray tube using electrostatic deflection.



*National Television Systems Committee. See further definitions and Appendix A.

plates in the forward position and placed to the left and right of center where the electron beam will travel. The vertical deflection plates are between the electron gun and the horizontal plates and are placed above and below the center line where the electron beam will travel. Control of the electron beam movement is accomplished by placing a voltage on the plates. Using the vertical plates as an example, you may (1) apply an ac signal directly across the top and bottom plates or (2) ground one plate and apply the ac signal to the other plate. In either case, the beam is controlled by the potential *difference* between the plates whether one plate is grounded or not.

The beam is a flow of electrons that have a negative charge. Therefore, when the top plate is positive and the bottom plate is negative, the beam will be moved *upward*. The positive potential on the top plate attracts the negative electron, and the negative potential on the bottom plate repels the negative electron. The same statement can be made for the horizontal plates. A positive potential on the right plate attracts the electron, while a negative potential on the left plate repels the electron. Remembering our earlier discussion and the action of the beam trace and retrace, it can be concluded that the deflection voltages to both sets of plates will have a sawtooth waveshape: a slow, linear movement in one direction and a rapid, linear movement in the other direction. Figure 2.3 reviews the sawtooth voltages that apply in each case. The shapes are the same, but the frequencies differ.

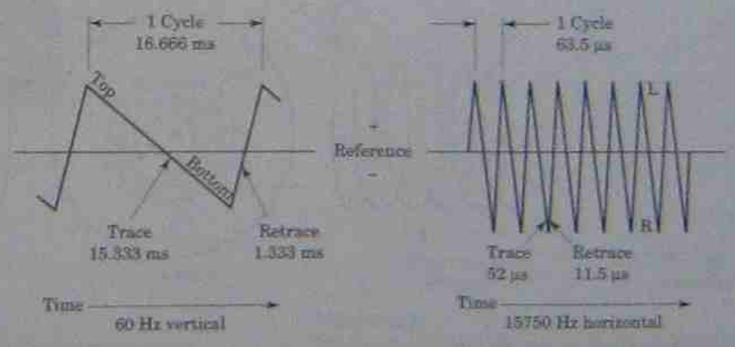
Several observations are noteworthy in Figure 2.3, where the vertical wave is used as the example. Although the wave in part (a) shows a positive excursion and a negative excursion compared to a reference, this does not imply that the positive polarity moves the electron beam to the top of the CRT without first identifying how the wave is connected to the plates. The important notation to be made here is the real time of the wave compared to the beam position on the face of the CRT. By comparing the first event to occur on the face of the CRT to the first event in the wave, we can conclude that the start of the linear trace time places the electron beam at the top of the CRT face. The end of the linear trace time places the electron beam at the bottom of the CRT face, and the retrace time moves the beam back to the top of the CRT again.

For the horizontal wave, we need to understand that the start of the linear trace time marks the left side of the CRT face, and the end of the trace is the right side of the CRT. This method of comparing event time on the oscilloscope to what takes place on the CRT screen will be used again when video signals are covered.

2.8 ELECTROSTATIC ADVANTAGES

Everything in electronics (and in life) has both advantages and disadvantages. The advantages of electrostatic deflection systems are that (1) a linear sawtooth voltage is easy to generate, and (2) the deflection plates perform equally well at all frequencies. The deflection can be as low as 0.01 Hz to several gigahertz. The disadvantage is that only a small angle of deflection can be accomplished with reasonable voltage levels [about ±15° (30°) with about 300-$V_{p\text{-}p}$ signal], and this ratio is not linear. That is, to accomplish twice the deflection angle may require four times the voltage. Electrostatic deflection systems are used for oscilloscopes where these features are an asset. You want to display any signal over a wide range of frequencies, and the

FIGURE 2.3
The sawtooth waveforms for the vertical and horizontal deflection systems: (a) vertical; (b) horizontal.



small deflection angle (which makes the tube longer) is not a real objection.

2.9 ELECTROMAGNETIC DEFLECTION

The explanation of electromagnetic deflection is best broken down into two steps to ensure that none of the parts are missing. A review of how magnetic fields react to each other will be followed by an examination of the waveshapes needed to achieve the desired results.

To do this, we will use basic magnetic field theory and the left-hand rule. You learned in basic electronics that current passing through a wire creates a magnetic field around the wire. You then learned to apply the left-hand rule. That is, placing the palm of your left hand against the wire with the thumb pointed in the direction of current flow allows the fingers to curl around the wire in the direction of travel of the magnetic field. Your instructor at that time used an arrow in the side view presentation to indicate the direction of current flow. The arrow had a tip at the leading end and fletching (feathers) at the trailing end. You may even remember the next trick. When looking at the end view of the wire, a dot in the center of the wire was used to show the tip of the arrow as current is moving toward you. When the current is moving away from you, an X is used to symbolize the feathers of the arrow.

The electron beam inside the neck of the CRT is not current flowing in a wire, but it is electron flow in a very narrow beam and, therefore, acts exactly like current flow in a wire.

The large heavy circle in Figure 2.4 represents the neck of the CRT, and the smaller heavy circle is the electron beam with a dot at the center to indicate current flowing toward you and the CRT face. The magnetic field around the beam is then polarized in a clockwise direction, using the left-hand rule.

A flashback to magnetic field theory tells you that when the wire is shaped to form a coil, the total magnetic field took on the shape of an ellipse around the coil. This is shown in Figure 2.4 as the dashed lines of force around the two halves of the coil L_L on the left and L_R on the right sides of the CRT. The coils are physically on the outside of the neck of the CRT and make up part of a device called a **deflection yoke.** When the applied voltage is polarized as seen in Figure 2.4, the magnetic field between the two halves of the yoke coils passes through the neck of the CRT from left to right.

Inside the neck of the CRT and below the electron beam, the magnetic field around the beam and the magnetic field from the coil *oppose* each other and will cancel. Above the electron beam, the two fields are in the same direction and will aid (add together) to increase the force from this direction. With an increased force above the beam and a decreased force below the beam, the beam will be moved *downward*.

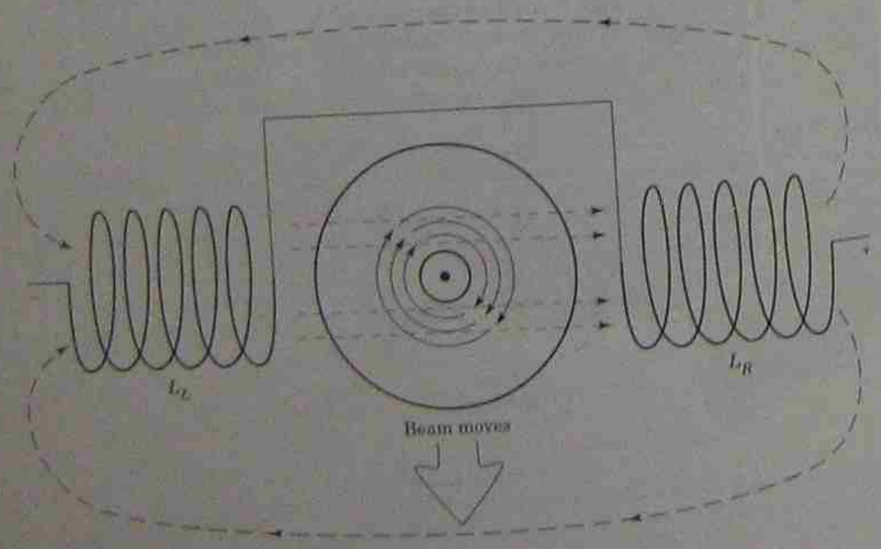


FIGURE 2.4
The effect of the coils' magnetic field on the electron beam.

If the polarity of the applied voltage to the coil is reversed, the magnetic field around the coil changes to the other direction and the beam moves *upward*.

Horizontal beam movement occurs in the same way, differing only by the placement of the two halves of the horizontal coils (top and bottom) and the direction of the beam displacement (left and right).

2.10 ADVANTAGES AND DISADVANTAGES

Deflection angles of ±57° (114°) are achievable in present-day deflection yoke models. The stated angle is implied to be in the horizontal direction since the width is one and one-third times the height. The vertical angle is slightly less than maximum. A wide angle of deflection is the biggest advantage to electromagnetic deflection because it means a shorter tube from front to back, and of course this is a favorable condition for desk-top monitors and home entertainment TV.

All coils have some distributed capacity between the turns of wire plus the lead-in wires and circuit capacity. Independent of the size or shape of the yoke, this capacity forms a resonant circuit with the inductance of the yoke at some frequency. This means that the deflection yoke works best only at one frequency, and this is the disadvantage of electromagnetic deflection. But the vertical circuit is always operated at 60 Hz and the horizontal circuits only at 15,750 Hz. Therefore, by careful selection in the design of the yoke, this disadvantage can be turned around to become a real advantage. Figure 2.5 shows the placement of the coils on the neck of the CRT. The horizontal coils are on the top and bottom, while the vertical coils are on the left and right sides.

2.11 DEFLECTION YOKE WAVEFORMS

Figure 2.3 shows the sawtooth voltages necessary to deflect the electron beam in the electrostatic deflection CRTs. The electromagnetic deflection systems require a sawtooth **current** through the yoke in order for the magnetic field to move the electron beam in a sawtooth pattern.

The coils of the deflection yoke in Figure 2.6 can be broken down into their two electrical component parts, the coil inductance and the wire resistance. The resistance of the wire is distributed throughout the entire length of the wire in the coil, but in a model coil the resistance can be shown in series with the inductance. Each part of the coil can now be treated separately.

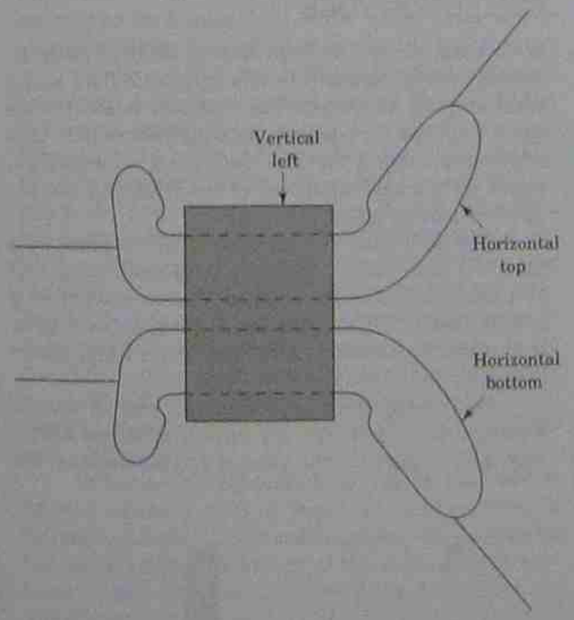


FIGURE 2.5
Skeletal view of the electromagnetic deflection yoke coil positions on the CRT neck.

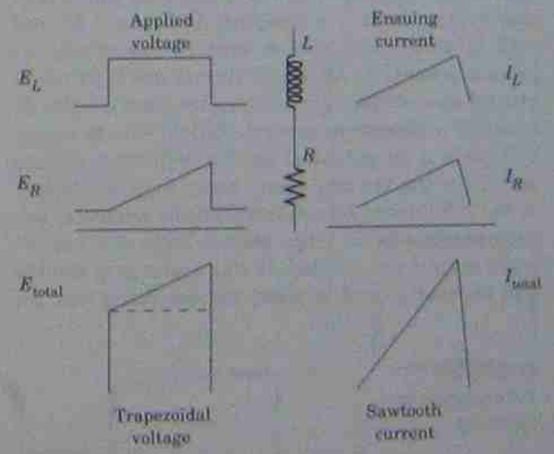


FIGURE 2.6
The trapezoidal voltage applied to the yoke coil to produce a sawtooth magnetic field.

In the resistive part, the applied voltage and the resulting current are linear and in phase. Therefore, a sawtooth current will result in the resistor when a sawtooth voltage is applied across the resistor. The inductance, however, requires that a **square-wave** voltage be applied across the coil for a sawtooth current to flow through the coil. Figure 2.6 shows the relationship of the applied voltage versus current waveforms.

Here the square-wave voltage of the inductive part and the sawtooth voltage of the resistive part add together to form a **trapezoidal** voltage to be applied across the deflection yoke. The resulting total current will be in the form of a sawtooth wave, as will be the magnetic field that surrounds the coils.

Since the resistive component of the yoke can only generate heat and consume power, its value is held as small as possible. The inductive component part of the yoke should be as large as is practical to be consistent with maximum magnetic strength and good linearity. The most efficient deflection yokes will have a large L to R ratio (L/R).

Electrical centering of the raster could be accomplished by adding a dc component of voltage to the applied ac signal. This addition often includes a potentiometer with +dc applied to one end and −dc applied to the other end, with one side of the deflection system attached to the center arm of the control. Assume for a moment that +20 V dc and −20 V dc are applied across the control. With the control arm set at mid-position, the voltage to the deflection system is at 0 V (halfway between +20 and −20 is zero). The center arm is essentially at ground potential. Although this is not a physical ground connection, it has the same effect as one. It is called a **phantom** ground. Either side of center will place a dc potential on the deflection system and move the electron beam away from the center of the CRT face. In electromagnetic systems, the yoke current is so large that a high-wattage (2-watt) control was needed. It was a source of trouble and expensive, and because the centering was set one time at installation only, the centering control was abandoned.

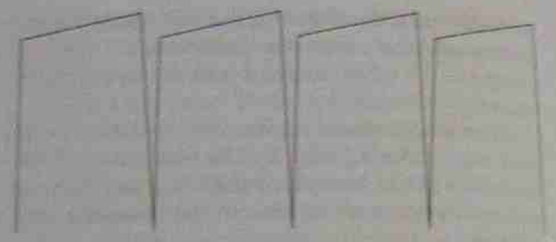


FIGURE 2.7
A train of trapezoidal wave cycles.

A train of trapezoidal cycles of deflection voltage is shown in Figure 2.7, where the slanted top is typical of the sawtooth wave component and the bottom is typical of the square-wave component part of the trapezoidal waveshape. A large L/R ratio will make the sawtooth part of the wave look even less slanted. Care should be taken when viewing this wave to identify it as a positive-going trapezoidal wave and not as negative-going spikes of voltage.

2.12 MECHANICAL FUNCTIONS OF THE DEFLECTION YOKE

With time, it was realized that a smaller neck diameter would require less of a magnetic field and a smaller yoke to deflect the electron beam for an equal angle as for a larger-neck-diameter CRT. One conclusion then is that the deflection yoke size depends on the neck diameter of the CRT and the desired deflection angle.

The deflection yoke is held firmly in place by a modified hose clamp. Either a long-stem wing bolt or a hex nut can be loosened to free the yoke from a locked position. The yoke has a plastic housing so that it can be handled (with care) even when power is applied to the system.

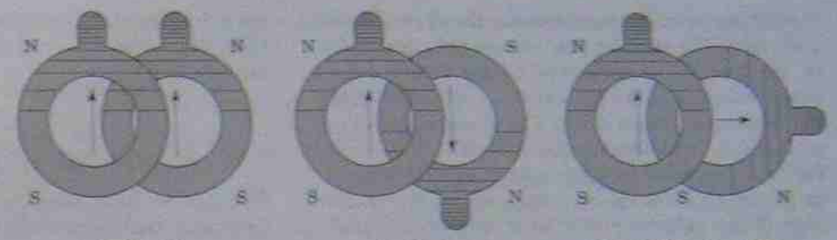
Positioning the yoke incorrectly can be seen in Figure 2.8. In part (a) the raster is tilted either way, and in part (b) the yoke is too far back on the neck of the CRT where the electrons strike the glass envelope at the junction of the neck and bell areas to cast a shadow on the face of the CRT. Refer to Figure 2.5 and imagine moving the deflection yoke to the left so that the beam starts to deflect earlier along its travel through the tube.



FIGURE 2.8
Yoke position and centering.

(a) Tilt (b) Neck shadow (c) Centering

FIGURE 2.9
Magnetic centering rings.



A metallic crimp on the back end of the yoke holds two ring magnets in place that are used for centering the raster on the face of the CRT. Figure 2.9 shows the ring magnets with tabs and how they are polarized north and south. The tabs allow you to position each ring separately in a circular pattern around the center axis. When the tabs are together, as in Figure 2.9a, both north poles are at the top and the magnetic fields will add together.

Assuming that north (N) is positive, the electron beam will be attracted toward the top of the tube with twice the strength of a single magnet. When one tab is up and the other down (either tab), the two magnetic fields will cancel as seen in Figure 2.9b. Two things happen in Figure 2.9c. One tab is straight up while the other tab is turned 90° (a quarter-turn). First, the magnetic field is less than the strength of two full magnets, but not zero. Second, the angle of beam movement is now in a direction that is halfway between the two tabs, 45° to the right rather than straight up or straight sideways. The full assembly (both magnets together) can be rotated around the neck of the CRT to adjust the position.

In the centering procedure, you do not need to know a value of field strength nor do you need to estimate direction. The entire procedure is done by eye while viewing the front of the tube. Simply separate or join the two tabs and then rotate the assembly around the neck of the CRT until, in your opinion, the picture is centered.

In color TV, the centering ring principle is used for a different purpose, called color purity. Keep these basic centering ring ideas in mind when color purity is discussed later.

2.13 PINCUSHION

The location in the neck of the CRT that identifies the apex of the deflection arc will not be the same distance to all points on the face of the CRT at angles away from the center line. Figure 2.10a shows that when the beam is in focus at the center of the CRT, the point of focus follows an arc and is not in best focus at either the top, bottom, left, or right edges. A suggested compromise setting is to make the scan lines as sharp and clear as possible in an area that conforms to the shape of a donut around the dead center of the CRT face.

But the defocusing is not a critical problem. A condition called **pincushioning** also results from

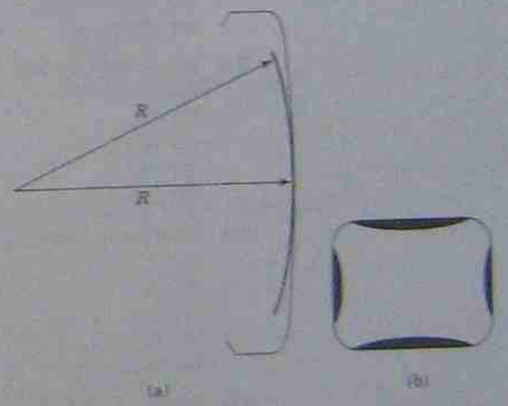


FIGURE 2.10
Pincushioning: (a) the point of focus for length R at the center and at the top or bottom of the CRT; (b) pincushion-shaped raster.

the difference in distance between the apex and the CRT, face. The electron beam is not deflected as far on the vertical or horizontal center lines as it is along the edges of the face, and it creates the raster shape seen in Figure 2.10b. The shape looks like a pincushion, from which it gets its name. This condition was corrected in older models of CRT devices by gluing small permanent magnets on the inside edge of the deflection yoke at strengths and positions that correct the problem.

In color deflection yokes, the same condition causes misalignment of the separate colors and is called **convergence.** In color yokes the problem is overcome by the development of the **precision static toroid** (PST) deflection yoke. More windings are added to the PST yoke for different reasons to be covered in the section on color.

If the problem in black and white and color yokes has been corrected, why should it be mentioned at all? The condition is identified here (1) so that you know of the condition, understand what causes it, and are able to work with other conditions that are similar in nature, and (2) when the subject of convergence is covered at the appropriate time, the same material need not be explained a second time.

2.14 NONSTANDARD SYSTEMS

Thus far, we have used the NTSC standards for all conditions, but suppose that you have a system that will never be a part of any outside network? In all reality, you can select any numbers that best serve your purpose. You can scan vertically instead of horizontally. You can change the vertical rate from 60 Hz to 150 frames per second and the horizontal from 15,750 Hz to 75,000 Hz to scan the CRT with 1000 scan lines. As long as you stay within your own system, there will never be a problem and all things are permissible. But keep in mind that you will not be able to work with any of the software or hardware available in the outside world. You are not compatible. Security systems and military satellite systems may be some of the nonstandard systems.

QUESTIONS

2.1 What would you see on the face of a normally operated CRT, and where would it appear when no deflection voltages are applied?

2.2 The CRT is scanned
(a) vertically,
(b) horizontally,
(c) diagonally.

2.3 How many scanning lines are there to one field?
(a) 1,
(b) 30,
(c) 60,
(d) 262.5,
(e) 525

2.4 How many fields are scanned in one second?
(a) 1,
(b) 2,
(c) 30,
(d) 60,
(e) 262.5

2.5 Which of the following statements is true?
(a) two frames make one field,
(b) two fields make one frame,
(c) 30 fields make one frame,
(d) 262.5 frames make one field, or
(e) none of the answers is true.

2.6 What is the term used to describe the overlay of consecutive fields? _____

2.7 There are _____ fields per second.

2.8 There are _____ frames per second.

2.9 There are _____ horizontal scan lines per field.

2.10 There are _____ horizontal scan lines per frame.

2.11 What is the frequency of the vertical scanning voltage?

2.12 What is the frequency of the horizontal scanning voltage?

2.13 What is the time for one complete cycle of the horizontal scanning voltage?

2.14 What is the trace time for one horizontal scan line?

2.15 What is the retrace time for one horizontal scan line?

2.16 What is the time for one complete cycle of the vertical scanning voltage?

2.17 What is the trace time for one vertical scan?

2.18 What is the retrace time for one vertical scan?

2.19 How many complete horizontal scan cycles occur during one vertical retrace period?

2.20 What is the definition of a raster?

2.21 You can have a picture without a raster.
(a) Yes
(b) No

2.22 You can have a raster without a picture.
(a) Yes
(b) No

2.23 Which deflection system has the widest deflection angle?
(a) electrostatic,
(b) electromagnetic,
(c) both the same

2.24 Which deflection system has the widest frequency response?
(a) electrostatic,
(b) electromagnetic,
(c) both the same

2.25 Which deflection system operates on a sawtooth voltage?
(a) electrostatic,
(b) electromagnetic,
(c) both

2.26 Which deflection system operates on a sawtooth current?
(a) electrostatic,
(b) electromagnetic,
(c) both

2.27 What is the name given to the voltage waveshape that is applied to the deflection yoke?
(a) sawtooth,
(b) sine,
(c) square,
(d) trapezoidal,
(e) ramp

2.28 What is the name of the current waveshape through the deflection yoke?
(a) sawtooth,
(b) sine,
(c) square,
(d) trapezoidal,
(e) ramp

2.29 The two vertical deflection coil halves are placed on the _____ of the neck of the CRT.
(a) top and bottom,
(b) top and right side,
(c) left and right sides,
(d) bottom and left side

2.30 The two horizontal deflection coil halves are placed on the _____ of the neck of the CRT.
(a) top and bottom,
(b) top and right side,
(c) left and right sides,
(d) bottom and left side

2.31 Rotating the deflection yoke around the neck of the CRT causes the raster to _____.

2.32 Moving the deflection yoke back toward the base of the CRT causes the raster to _____.

2.33 What is the function of the two ring magnets that are attached to the back of the deflection yoke?

2.34 How is the centering adjustment measured?

2.35 What international standards are used in this text?
(a) PAL,
(b) NTSC,
(c) SECAM

3 Vertical Deflection Systems

3.1 INTRODUCTION

The purpose of the vertical deflection system is to provide a magnetic field around the neck of the CRT that will move the electron beam down the face of the CRT in a linear fashion and then return the beam rapidly back to the top 60 times every second. It is the first in a series of circuits to be examined and explained because (1) it is the easiest circuit to visualize and understand, (2) it follows the natural sequence in standard curriculum, and (3) some of the concepts set down in the vertical circuits will lay the foundation for other circuits to follow.

3.2 VERTICAL BLOCK DIAGRAM

The first point of agreement to be reached is that the vertical deflection system must be in full operation for 100% of the time that the unit has power applied. Vertical deflection is needed with or without the presence of a picture, on or off channel. This tells you that the first part of the vertical section must be a signal generator, an oscillator.

The oscillator will free run at or about 60 hertz (Hz). A frequency adjustment is provided to set the oscillator to the correct rate during operation. In receiver products, this frequency control is called the **vertical hold** control and is generally available to the end user as a front panel control. See Figure 3.1 for these and other functions to follow.

The dashed input in Figure 3.1 shows that a synchronizing signal is applied to the vertical oscillator. The oscillator is self-sustaining and does not require an input signal to maintain oscillations. The sync signal is generated at the transmitting station to be sent along with the picture information for tracking the receiver and transmitter alike. The vertical hold control is then set by the operator to keep the two systems in a locked mode. Synchronization will be treated as a separate topic at the appropriate time.

The vertical size (or height) control adjusts the dc supply voltage to the vertical oscillator. You may recall from earlier laboratory experiments that the peak-to-peak output voltage changed size when you changed the dc power supply setting. The change in signal strength shows up as a change in the vertical scanning distance. In this case, the height (or vertical size) of the raster can be controlled.

When you recall that the vertical voltage waveshape to be applied to the deflection yoke is a trapezoid, you can rule out sine-wave oscillators for use in vertical deflection circuits. Hartley or Colpitts oscillators (and some others) are rarely used in vertical deflection. Some modified form of square-wave or ramp-wave oscillators are more commonplace as vertical oscillators.

These circuits employ the charge and discharge characteristics of an RC network as the timing element for the period of oscillation. The value of R is adjusted to change the period time constant and the frequency of oscillation. The circuits are under the control of the design engineer, so you will

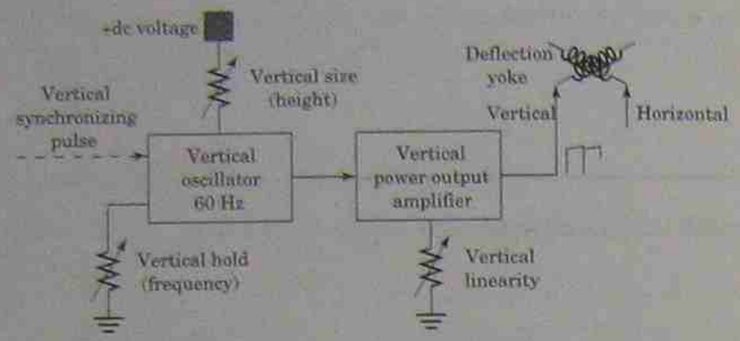


FIGURE 3.1
Block diagram of a typical vertical deflection system.

see many different oscillator circuits, even among different models of the same brand. The only positive fact that you can be assured of is that the vertical deflection circuits start with an oscillator.

There may also be an *RC* filter or waveshaping network between the vertical oscillator and the vertical amplifier (not shown in Figure 3.1), which is used to supply the correct waveshape to the input of the vertical amplifier.

3.3 VERTICAL OSCILLATORS

Many oscillator circuits have evolved over the years. In the beginning, the blocking oscillator ruled as king for a long period of time. However, the blocking oscillator used an iron core transformer that had three windings: one primary, one secondary, and the third was a feedback winding. In an effort to reduce costs and space, a transformerless oscillator was needed. The multivibrator, which had also been around for a long time, became the next circuit of choice. The blocking oscillator will not be discussed here because it has not been used for over a decade.

Two multivibrator circuits find common usage. The collector-coupled multivibrator of Figure 3.2 finds application in vertical circuits, and the emitter-coupled multivibrator is most common in horizontal deflection circuits.

The astable collector-coupled multivibrator of Figure 3.2a is the standard textbook form of circuit presentation. However, we can see that by redrawing the circuit we arrive at the circuit of Figure 3.2b. Here the circuit is composed of two cascade common-emitter, class A amplifiers.

Each amplifier contributes 180° of phase shift so that the output signal at the collector of Q_2 is in phase with the required input signal at the base of Q_1 for positive feedback and sustained oscillation. The component part numbers and values are the same in both diagrams, so you may follow whichever diagram is easiest for you to understand while reading the circuit description.

A quick view of the multivibrator shows that it acts as a seesaw. One amplifier comes on to turn off the second amplifier. A capacitor charges and turns on the second amplifier, which turns off the first amplifier. The capacitor discharges and turns on the first amplifier, which turns off the second amplifier. The *RC* components of the circuit determine the on/off time of each amplifier.

A technical description of Figure 3.2 begins several cycles after power has been applied and the circuit is stabilized in a free-running mode. Since the signal path runs in a loop, it is fitting to identify an arbitrary starting point at which to examine the four waveshapes of interest. The starting point is the dot on each of the four waves in Figure 3.2c. The circuit conditions at the starting point are Q_1 is nonconducting, the collector voltage on Q_1 is high, capacitor C_1 is almost fully charged, Q_2 is conducting heavily, Q_2's collector voltage is low, and capacitor C_2 is almost fully discharged.

An instant later, at time T_1, capacitor C_2 is fully discharged and the base of Q_1 is at a voltage level that sets Q_1 into conduction.

The collector of Q_1 drops quickly low, the base of Q_2 is driven far negative by the voltage drop across Q_1's load resistance plus the full charge on C_1. Q_2 is turned off and its collector voltage goes high, holding Q_1 base high.

Between time T_1 and T_2, capacitor C_1 discharges (and C_2 charges), Q_1 remains on, and Q_2 remains off.

At time T_2, capacitor C_1 has discharged to the point where the voltage on the base of Q_2 turns Q_2 on hard; the collector voltage of Q_2 drops rapidly, placing a negative pulse at the base of Q_1 to turn Q_1 off.

Between time T_2 and T_3, Q_1 is in cutoff, Q_2 conducts heavily, capacitor C_1 charges, and C_2 discharges.

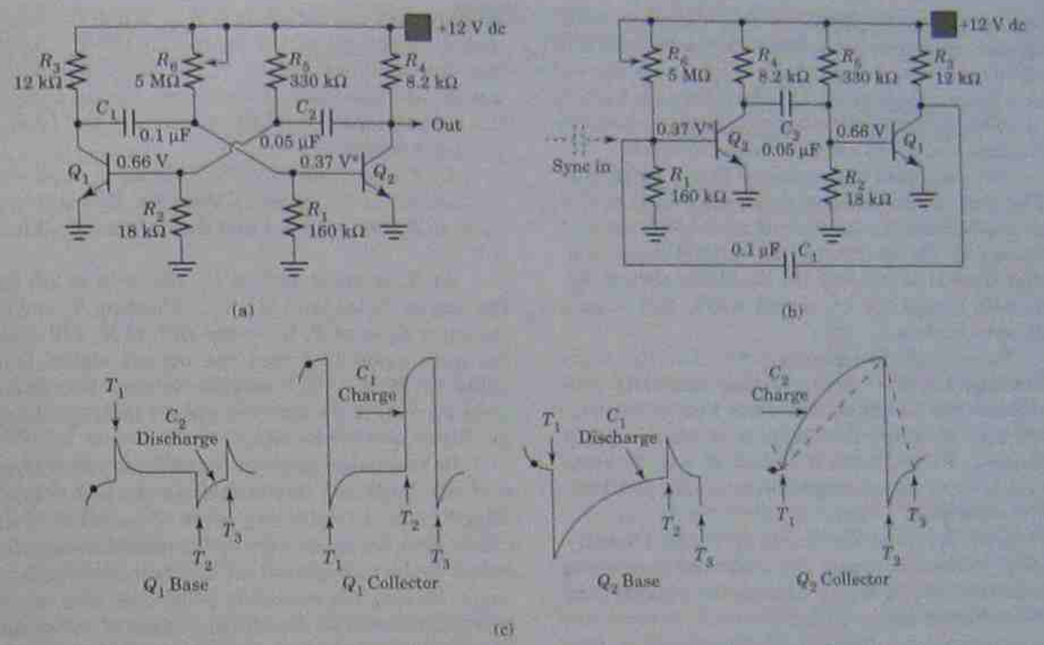


FIGURE 3.2
A collector-coupled multivibrator used in vertical deflection circuits: (a) the textbook configuration and (b) the same circuit arranged as two series amplifiers with overall feedback. (c) Typical waveforms used in testing. (Variables denoted by *.)

At time T_3, the cycle is completed and is the same as it was at time T_1. The pattern repeats for every cycle.

Capacitor C_1 charges during the time that Q_1 is turned off, and Q_1's collector is high. Current flows from ground, through the base-emitter junction of Q_2 to C_1, and then through R_3 to +dc supply.

Capacitor C_1 goes through its discharge cycle when Q_1 is conducting heavily. Current flows from ground through Q_1 (emitter to collector) and to C_1, and then through R_1 back to ground.

Capacitor C_2 charges during the time that Q_2 is turned off, and Q_2's collector is high. C_2's charge path includes the base-emitter junction of Q_1, C_2, and R_4 to the +dc supply. C_2's discharge path is from ground through Q_2 and then through R_2 to ground.

C_1's discharge time represents the scan time, and the discharge time of C_2 is the retrace time. The sum of the two time periods should be greater than the time for one cycle = 16.666 milliseconds (ms). Each charge time should be less than the retrace time of 1.333 ms.

$$C_1\text{'s charge time} = R_3 \times C_1 = 1.2\text{ms} \quad (3.1)$$

$$C_1\text{'s discharge time} = R_1 \times C_1 = 16\text{ ms} \quad (3.2)$$

$$C_2\text{'s charge time} = (R_2 + R_4)C_2 = 1.31\text{ ms} \quad (3.3)$$

$$C_2\text{'s discharge time} = R_2 \times C_2 = 0.9\text{ ms} \quad (3.4)$$

3.4 VERTICAL OUTPUT POWER AMPLIFIER

The name alone should tell you several things about the circuit. First, the word *output* tells you that this is the last circuit in this section. The output of the vertical section goes to the deflection yoke, just as the audio output goes to the speaker or the video output goes to the CRT. Output means last.

Second, the name tells you that this is an amplifier. The circuit has gain. To determine if the circuit is a voltage or power amplifier, you need to examine the circuit values from the schematic

diagram. When the amplifier has a large value of collector resistance (impedance) and a low value of collector current, it is a voltage amplifier. If the collector resistance is small and the current is high, it is a power amplifier. Appendix B gives an example of voltage amplifiers versus power amplifiers.

But you could have guessed that a power amplifier was needed here, since it was stated earlier that the deflection yoke current can be as large as 1 ampere (A). The function of the vertical output amplifier then is to amplify the oscillator output signal, help shape the trapezoid wave, and supply high yoke current.

The only control generally found in the vertical output amplifier is the vertical **linearity** control. Linearity means in a straight line, or of equal change for all equal distances, or straight without distortion. In the vertical circuit, it can be envisioned to be equal spacing between all the 525 horizontal scan lines.

To understand the function of the linearity control, we need to know the difference between a volume control and a gain control. Both controls do the same thing, but in different ways.

A common-emitter amplifier is shown in Figure 3.3a and b that has identical resistor values for R_1, R_2, and R_c. It is further recognized that the amplifier voltage gain is roughly R_c divided by R_e, and in Figure 3.3 we will assign a gain of 5. When 2 $V_{p\text{-}p}$ is applied across R_2 in Figure 3.2a, the position of the movable center arm will determine (by the voltage-divider rule) how much of the 2-$V_{p\text{-}p}$ signal is applied to the amplifier base. With R_2 set at 20% from the bottom, 0.4 $V_{p\text{-}p}$ is applied to the base and, with a gain of 5, the output signal level is 2 $V_{p\text{-}p}$. With the center arm set at its mid-position, 1 $V_{p\text{-}p}$ is input and the output is 5 $V_{p\text{-}p}$. When the center arm is at the top of the control (R_2), 2 $V_{p\text{-}p}$ is put into the amplifier and 10 $V_{p\text{-}p}$ is found at the output. R_2 in Figure 3.3a is a **volume** control and sets the output signal level by controlling the level of the input signal.

In Figure 3.3b, the 2-$V_{p\text{-}p}$ signal is applied to the base of the amplifier all the time. By making R_2 equal to R_c, the gain is 1 and the output signal level is 2 $V_{p\text{-}p}$.

As R_2 is made 40% of R_c, the gain is 2.5 and the output signal level is 5 $V_{p\text{-}p}$. Shorting R_2 and selecting a value of R_2 to be one-fifth of R_c will make the gain equal to 5 and the output signal level equal to 10 $V_{p\text{-}p}$. The emitter control is called a **gain** control. It changes the output level by changing the gain of the amplifier.

In your basic study of amplifiers, you learned that the maximum undistorted output signal is obtained when the operating point (Q point) is at the center or most linear part of the transconductance curve. Refer to Figure 3.3c, the transconductance curve. Moving the operating point to Y or Z on the curve distorts either the top or bottom of the signal. This is exactly what the linearity control does. It changes the amplifier gain by changing the Q-point of the amplifier such as to distort the top or bottom of the trapezoidal wave. Figure 3.4 identifies the top and bottom of the wave. The letter T represents the top of the raster and B represents the bottom of the raster. In Figure 3.4b, the top of the raster is compressed when the operating point is at Z. At Y, the bottom of the raster is compressed. It is common to adjust the vertical size control during the same period as when the linearity control is adjusted and settle on the best compromise setting. In

FIGURE 3.3
Amplifier output controls: (a) volume control; (b) gain control; (c) transconductance curve.

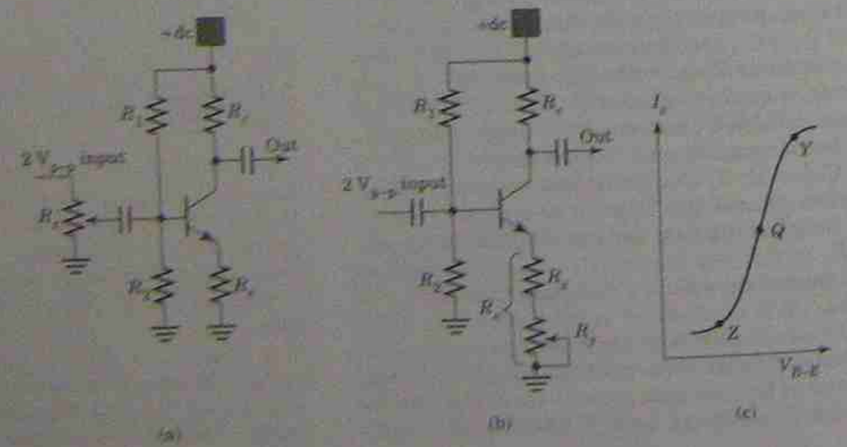
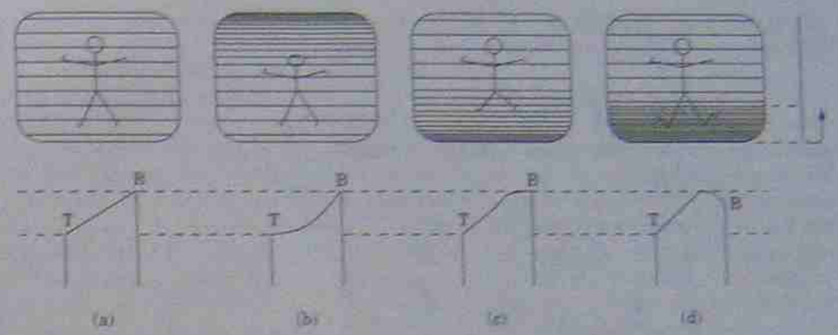


FIGURE 3.4
Forms of vertical linearity distortion: (a) normal raster and picture; (b) top compression; (c) bottom compression; (d) vertical foldover at bottom.



an extreme case, the bottom of the picture may curl up to overlay on itself. This is called vertical **foldover** and looks like a transparent picture with the bottom edge folded up on itself. The raster is shorter than desired, and the bottom section is brighter than the rest of the picture. The vertical size control has a greater effect at the bottom of the raster, while the vertical linearity control has a greater effect at the top of the raster.

Some vertical amplifiers still use an iron core output transformer. High secondary currents require that the transformer have a step-down turns ratio (voltage) that steps up the secondary current. Turns ratios from 20 : 1 to 100 : 1 are typical. Measuring the dc resistance of the windings will give you a reasonable approximation of which is the primary and which is the secondary winding. Because of the transformers large size (approximately 2 $in.^3$), and the weight, cost, and space requirements, such circuits are being replaced with class B push–pull transformerless power output amplifiers.

3.5 SCHEMATIC DIAGRAMS

Figure 3.5 is chosen as a sample vertical deflection section because it is unique and is taken from a 12-in. computer monitor schematic diagram. Recall the Barkhaussen criteria for oscillation, which states that a circuit will sustain oscillation when an in-phase (positive) feedback signal from the output is applied to the input, and the loop has an overall gain of more than 1. Figure 3.5 is unique in that the entire circuit is a power oscillator, that is, an oscillator and power amplifier. It is held in the oscillating state by three feedback loops. The main feedback loop 1 is taken from the output yoke terminal V_1 and applied to the base of Q_{301}. Feedback 2 is the current return loop through the yoke from terminal V_2 to the emitter resistor (R_{304}) of Q_{303} and then to ground. The yoke current through the small resistance (1.2 Ω) develops a feedback voltage at the emitter of Q_{303}. Loop 3 is a negative feedback loop from the emitter of Q_{303} through the linearity control to Q_{301} for waveshaping.

Q_{303} is generally considered to be the oscillator, with Q_{301} and Q_{304} as the class B push–pull power output amplifier. Q_{302} acts as a switch to form the square part of the trapezoidal wave, but it also controls the vertical *blanking* interval (retrace time) of the vertical scan time.

The frequency is controlled by the RC time constant of C_{301} with $R_{301} + R_{302}$ as

$$\text{frequency} = \frac{1}{2\pi RC}\ \text{Hz} \qquad (3.5)$$

Q_{301} is adjustable over a range of 20 to 130 Hz. The size of the raster is changed by adjusting the dc voltage to Q_{301} oscillator, which changes the signal strength to the amplifier and eventually to the deflection yoke.

The linearity is adjusted by modifying the waveshape in feedback loop 3. The linearity is commonly set by observing the raster or picture on the face of the CRT, but greater accuracy can be achieved by observing a waveform on the oscilloscope. A sawtooth current waveshape is desired, but the scope cannot measure current; it can only measure voltage. This condition can be overcome by adding a small 1-ohm resistor (Ω) in series with the deflection yoke and then measuring the voltage across the small resistor. Voltage and current are in phase for a resistor, so the voltage waveshape will be the same as the current waveshape. This is already done for you in Figure 3.5 as the emitter resistor of Q_{303}. The 0.9 $V_{p\text{-}p}$ across 1.2 Ω is 750 mA p-p yoke current.

Adjust the size and linearity controls for the most linear sawtooth wave at the emitter of Q_{303}.

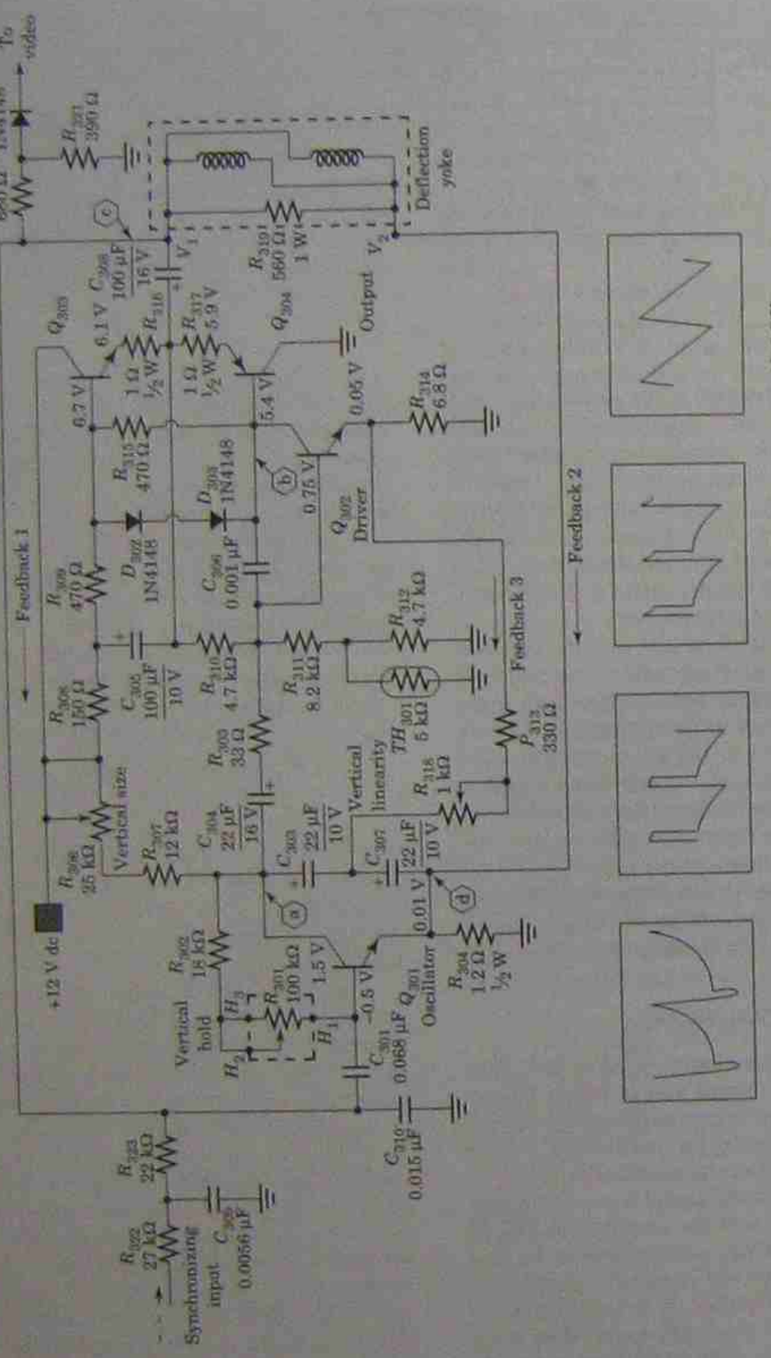


FIGURE 3.5
Vertical deflection circuit.

The synchronizing signal is applied to R_{322} noted by the heavy dashed line.

The thermistor (TH_{301}) decreases resistance as the temperature rises and controls the bias on transistor Q_{302} over the operating temperature range.

Diodes D_{301} and D_{302} establish the bias of 1.4 V dc (2×0.7) between the bases of the output transistors Q_{303} and Q_{304} to minimize crossover distortion.

Resistor R_{319} is a damping resistor to prevent the vertical yoke from oscillating at its natural frequency. Adding a resistor in parallel with a tuned circuit lowers the Q and restricts oscillations.

Resistors R_{320} and R_{321} and diode D_{321} are the retrace blanking network to the video amplifier. This network shuts down the video amplifier during the vertical retrace time. Greater details are given under the section on video amplifiers.

3.6 VERTICAL CIRCUIT TROUBLESHOOTING

All the vertical circuit defects can be observed and analyzed on the face of the CRT. Recall the block diagram of Figure 3.1, which has an oscillator, an amplifier, and a deflection yoke. You do not need a picture on the raster in order to diagnose the faults shown in Figure 3.6 and explained here.

Figure 3.6a has one bright horizontal line across the center of the CRT. This tells you that the vertical circuit has failed completely. The oscillator may have stopped oscillating. The vertical amplifier may be defective and is passing no signal at all, or the vertical half of the yoke may have an open circuit that prevents current from flowing through the yoke. Any of these failures are possible, but since the vertical operates at such a low frequency, it is easy to signal trace with an oscilloscope. You will need to isolate the faulty circuit first and then measure the dc voltages found on the schematic diagram and draw some conclusions as to which component is causing the problem. The voltages marked on the schematic are the dc operating voltages, which may also be accompanied by an ac signal waveform shown at test points a, b, c, and d in Figure 3.5.

In Figure 3.6b, insufficient height is generally caused by low gain in the amplifier circuit. To verify this condition, measure the ac signal waveforms as noted in Figure 3.5. A situation could arise for which all the signal levels are low and the fault could be anywhere in the loop. In this case and the case of Figure 3.6a, open the feedback loop by disconnecting the coupling capacitor C_{301} (the side farthest from the base) and apply a 60-Hz sine wave or triangle wave from a signal generator. Adjust the generator level until you measure 0.6 V_{p-p} at the collector of Q_{301} and then compare all other voltage waveform levels.

If you have a case for which you can fill the raster from top to bottom but the linearity is poor, you are back to low gain in the vertical amplifier. Set the linearity first and then look for some condition that causes low gain.

Figure 3.6c denotes a keystone-shaped raster. This condition can be caused only by an open circuit in one-half of the deflection yoke. The larger size may be on the left or right side. In some cases, the yoke may be examined for a broken wire at the yoke terminals. Turn off the unit, remove the protective cover from the back of the yoke, and give the wiring a good physical examination. Also test for broken wires from the circuit to the yoke.

Review Figure 3.5 and the supporting text for troubleshooting in the vertical linearity circuit.

One other condition may arise when the vertical oscillator strays off frequency. The tests for frequency are best resolved when the synchronizing signals are also included. Therefore, oscillator frequency symptoms are postponed until that time. You can, however, measure oscillator frequency with an oscilloscope any time that the frequency is in question.

The heavy dashed lines around some components indicate that these parts are not on the printed wiring board.

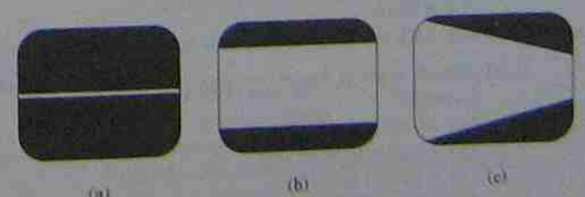


FIGURE 3.6
Common faults in the vertical deflections section: (a) complete loss of vertical deflection; (b) short raster; (c) keystone raster.

QUESTIONS

3.1 The vertical oscillator center frequency is
(a) 30 Hz,
(b) 60 Hz,
(c) 90 Hz,
(d) 120 Hz,
(e) 150 Hz.

3.2 With no station signal selected, the vertical oscillator will
(a) stop oscillating,
(b) assume a selected station frequency,
(c) be free running near 60 Hz,
(d) be free running near 30 Hz.

3.3 The vertical oscillator frequency control is the
(a) height control,
(b) size control,
(c) hold control,
(d) linearity control,
(e) gain control.

3.4 The vertical size control is generally found in the vertical
(a) oscillator circuit,
(b) amplifier circuit,
(c) deflection yoke.

3.5 The vertical frequency control is generally found in the
(a) oscillator circuit,
(b) amplifier circuit,
(c) deflection yoke.

3.6 The vertical linearity control is generally found in the
(a) oscillator circuit,
(b) amplifier circuit,
(c) deflection yoke.

3.7 The vertical synchronizing signal is generally applied to the
(a) oscillator circuit,
(b) amplifier circuit,
(c) deflection yoke.

3.8 The vertical synchronizing signal is *generated* at the
(a) vertical oscillator,
(b) vertical hold control,
(c) transmitting station.

3.9 The vertical oscillator will oscillate
(a) with,
(b) without,
(c) both with and without a synchronizing signal.

3.10 Which type of amplifier has low collector impedance and high collector current?
(a) an oscillator,
(b) a voltage amplifier,
(c) a power amplifier,
(d) all amplifiers

3.11 Nonlinearity shows up in the trapezoidal wave as a change in the
(a) square-wave part of the scope pattern,
(b) sawtooth part of the scope pattern.

3.12 Vertical foldover will generally occur at the
(a) top of the raster,
(b) bottom of the raster.

3.13 Which type of amplifier replaces the class A transformer output amplifier?
(a) class A transformerless,
(b) class B push–pull transformerless,
(c) class C transformerless

3.14 The vertical size control generally has more effect
(a) at the top of the raster,
(b) at the bottom of the raster, or
(c) affects both top and bottom equally.

3.15 The vertical linearity control generally has more effect
(a) at the top of the raster,
(b) at the bottom of the raster, or
(c) affects both top and bottom equally.

3.16 In Figure 3.5, which waveform would best show linearity?
(a) a,
(b) b,
(c) c,
(d) d

3.17 The heavy dashed lines around a component (see Figure 3.5) indicate that the component is
(a) a special device,
(b) not used,
(c) factory-selected value,
(d) mounted off the circuit board.

3.18 One bright horizontal line across the center of the CRT face generally indicates a fault in the
(a) vertical oscillator,
(b) vertical amplifier,
(c) deflection yoke, or
(d) all three circuits are equally suspect.

3.19 A short raster on the CRT face generally indicates a fault in the
(a) vertical oscillator,
(b) vertical amplifier,
(c) deflection yoke, or
(d) all three circuits are equally suspect.

3.20 A keystone-shaped raster (right side shorter) generally indicates a fault in the
(a) vertical oscillator,
(b) vertical amplifier,
(c) deflection yoke, or
(d) all three circuits are equally suspect.

4 Horizontal Deflection Systems

4.1 INTRODUCTION

In Chapter 3 you saw how the vertical deflection system moved the electron beam up and down the face of the CRT. Can you predict how the horizontal deflection system is going to move the electron beam from side to side on the CRT face? It would be safe to say that you have most of it right. Let's see how well you did.

4.2 PARTIAL HORIZONTAL DEFLECTION BLOCK DIAGRAM

As you look at Figure 4.1, you can see that you are right if you said that the horizontal deflection circuit begins with an oscillator. The oscillator must be operational for the full time that power is applied. Figure 4.1 also shows a dashed block to the left of the oscillator, which will be brought into the picture later in this chapter. It is the automatic frequency control (AFC) circuit.

You are also correct if you said that a power output amplifier is required following the oscillator. In the horizontal circuit a transformer is always used with the output amplifier to convert the high signal voltage to a high deflection yoke current. This transformer (T_2) has three names. For now, we will call it the horizontal output transformer (HOT). The other names are identified in the next section.

So far, the horizontal deflection circuit is exactly like the vertical deflection circuit, except for frequency. The vertical is 60 Hz and the horizontal is 15,750 Hz. Both circuits convert a trapezoidal voltage into a sawtooth current to move the electron beam on the face of the CRT in their respective directions.

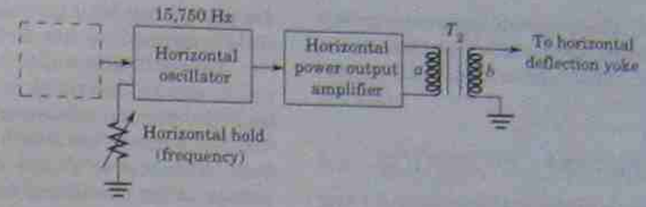
4.3 COMPLETE HORIZONTAL DEFLECTION AND HIGH-VOLTAGE BLOCK DIAGRAM

The differences between the deflection circuits show up in Figure 4.2 to identify more than just the horizontal oscillator and amplifier. The horizontal power output circuit is a class C amplifier that needs a driver amplifier to supply base power through transformer T_1 during the time that the class C conducts and draws base current. The drivers have very low output impedance to match the low input impedance of the class C amplifier during the conduction time. During the nonconducting time, the input impedance of the class C is high and mismatched, but this has no effect on the nonconducting output amplifier.

The output amplifier sends a trapezoidal voltage to winding 1 primary (pins 4 and 6) that is induced into winding 2 secondary (pins 6 and 7) with a step-down turns ratio of about 3:1. The gradually increasing yoke sawtooth current during trace time causes a magnetic field to build around winding 2.

At the peak of the high current wave in winding 2, the output amplifier is driven into cutoff, the output voltage wave drops to zero, the secondary 2 current suddenly drops to zero, and the magnetic

FIGURE 4.1
Partial horizontal deflection block diagram.



field around winding 2 collapses to produce a counter electromotive force (emf) pulse voltage across winding 2 of considerably larger magnitude, but of opposite polarity, than the original applied voltage.

In Figure 4.2, this counter emf is only about 60 $V_{p\text{-}p}$ from a 12-V dc supply. Some products develop several thousands of volts. The time rate of change in current that describes the counter emf uses the expression

$$e = L\frac{\Delta i}{\Delta t} \text{ volts} \qquad (4.1)$$

This says that a large change in current (Δi) that takes place in a short period of time (Δt) will produce a large voltage (e) across inductor L. Greater current changes or shorter time periods produce the largest voltages. Notice that this action takes place during the retrace time.

Also during the retrace time, secondary 2 becomes a primary to transform the large pulse voltage into secondary 3. The turns ratio from windings 2 to 3 is a step-up ratio of about 250:1. Secondary 3 will see a pulsed voltage of about 13,500 $V_{p\text{-}p}$. The large pulsed 3 voltage will be rectified by diode D_1 to a dc voltage for use as the anode voltage for the CRT. Diode D_1, in late-model receivers, is molded into the high-voltage transformer case and is not separately replaceable. This circuit then is the high-voltage section of the CRT circuit.

The most important point to be learned in this entire chapter is that *any* failure in the horizontal oscillator, horizontal driver, or horizontal output amplifier will stop the large pulse voltage needed to generate the high voltage to operate the CRT. There will be *no* high voltage and *no* raster!

Transformer T_2 was identified earlier as the horizontal output transformer, which is still true. However, now you can understand that T_2 is also the *high-voltage* transformer. If you ever wondered how the 12-V dc battery in your car could develop the thousands of volts needed to fire the spark plugs, you can use the same reasoning for the high-voltage section of the CRT. The 12 V dc is applied to a coil where the current will slowly build a magnetic field around the coil. The ignition points are mechanically opened, the current drops to zero, and the magnetic field collapses, inducing a counter emf through a step-up turns ratio of the ignition coil to arc the gap of the spark plug and ignite the fuel mixture. This action is called the **flyback** action and completes the list of names given to transformer T_2. That is, T_2 can be called the horizontal

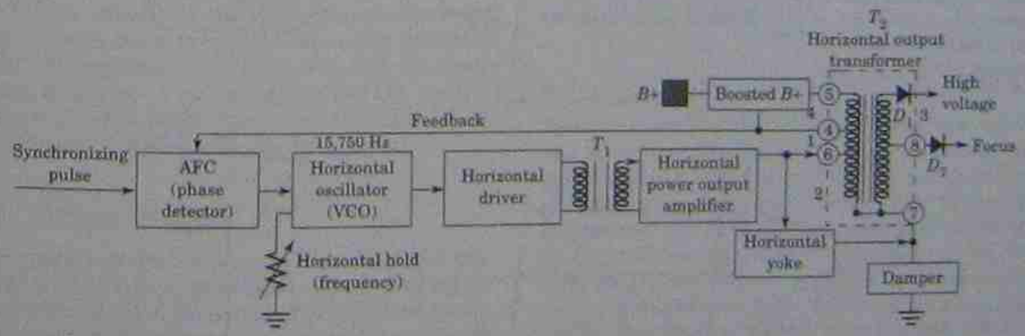


FIGURE 4.2
Complete horizontal deflection and high-voltage block diagram.

output transformer, the high-voltage transformer, or the flyback transformer and all three names are technically correct. The names are used interchangeably in practice.

4.4 DAMPER SECTION

To dampen, besides making moist, means to depress, deaden, or discourage. In the case of the horizontal circuit, it means to depress oscillations in the yoke and high-voltage circuits. The conditions for oscillations are set by the physical construction of the yoke having inductance and distributed capacity to form a resonant circuit at about 70 kilohertz (kHz). The excitation for oscillations stems from the shape of the current wave through the yoke. No problem arises when the current is gradually increased during trace time or when the applied voltage is removed to force the current to drop to zero during retrace time. The problem arises when the counter emf at the end of retrace time wants the yoke current to continue moving in a negative direction as the next cycle of applied voltage wants the current to begin to slowly increase again. Examine Figure 4.3a to see where oscillations are likely to occur in the horizontal yoke sawtooth current wave. Next, examine Figure 4.3b, which compares the action of the yoke sawtooth current with the position of the electron beam (and dot of brightness) on the face of the CRT for one cycle of horizontal trace and retrace.

Using these two sketches as a model, the total action can be described as follows: *First*, assume that no deflection voltage or current is in effect and that the electron beam is in the center of the CRT face, at point *A* in Figure 4.3b. *Second*, the signal voltage to the horizontal amplifier causes the amplifier to conduct, drawing current through the yoke to move the beam from point *A* to the right side of the CRT at point *B*. *Third*, the amplifier is driven into cutoff, amplifier current stops, and the yoke current rapidly drops to zero, moving the beam from point *B* to point *C*, while the counter emf in the output transformer builds. *Fourth*, the counter emf continues to drive the yoke current in a negative direction (now below zero), moving the electron beam past center (at *C*) and on to the left side of the CRT at point *D*. (The damper circuit consists of a diode and a capacitor.) The diode is wired to conduct in the opposite direction from that of the output amplifier, allowing one or the other to conduct, but not both at the same time. *Fifth*, at a predetermined level of voltage charge on the damper capacitor, the damper diode begins to conduct (at point *D* where retrace ends), limiting the level of counter emf and allowing the damper capacitor to gradually discharge through the damper diode and deflection yoke, thus returning the current to zero

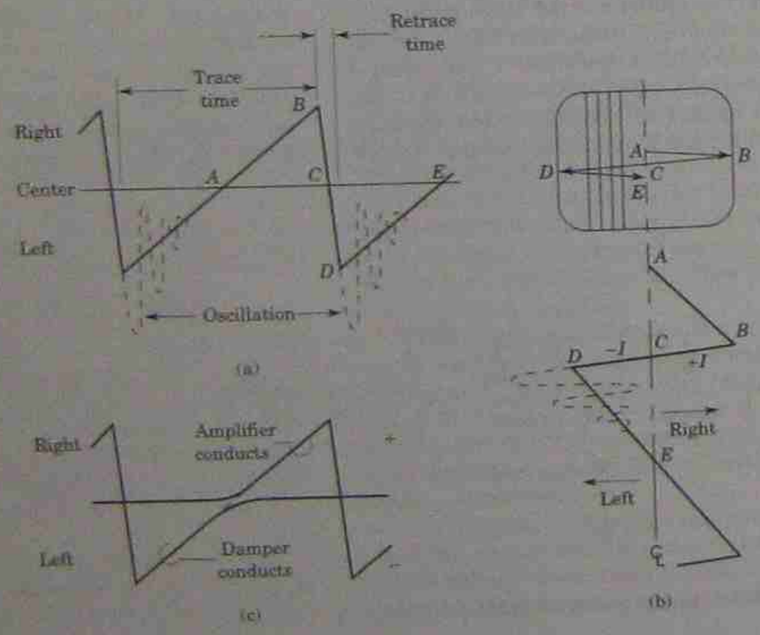


FIGURE 4.3
Barkhausen oscillation in the damper circuit: (a) where oscillations will occur, (b) the appearance of oscillations on the CRT face, and the electron beam movement with oscillations; (c) conducting cycle of the damper and horizontal output.

as the beam moves from left to right back to center on a line between points *D* and *E*. This completes one full horizontal cycle, with steps 2 through 5 repeated for every successive cycle.

Several important items can be noted at this time. The damper diode limits the reverse voltage level (counter emf) and suppresses oscillations called Barkhausen oscillation. The horizontal amplifier conducts to control the beam movement to the right of center (actually about 60% of the total beam travel), while the damper diode conducts to control the beam movement to the left of center (40% of total). This action is more clearly defined in Figure 4.3c. The damper diode begins to conduct at the end of the retrace time (start of trace time). Therefore, any problems relating to horizontal size or distortion (linearity) can be broken down by examining the right and left halves of the CRT face area. Amplifier problems affect the right side, while damper problems affect the left side of the raster. Note also that several bright vertical bars appear on the left side of the raster when the damper fails. These bars correspond to the crest of the oscillating sine wave, where the beam moves slower than during the remainder of the sine-wave cycle.

The vertical deflection yoke can experience the same Barkhausen oscillations, which is treated by simply placing a resistor in parallel with each half of the vertical yoke. The resistor values will range from about 270 ohms (Ω) to about 560 Ω each and have a wattage rating of about 2 watts (W) each. This feature was withheld until now, where a full discussion of damper circuits was warranted.

Your next question is already anticipated. Why are resistors used in the vertical deflection yoke and a diode used in the horizontal deflection yoke circuits? Resistors in the horizontal circuit would need to have about a 10-W power rating each. This would be a waste of considerable power and be much more expensive than using the diode circuit arrangement. In addition to this, the horizontal frequency is much higher than the vertical and results in a larger counter emf voltage, which can best be controlled with the diode circuit.

4.5 FOCUS VOLTAGE

The focus voltage for the cathode ray tube can range from 0 V to 5000 or 6000 volts depending on the design of the CRT circuit. You will need to examine the circuit diagram of the product in question to make this determination. In Figure 4.2, the focus voltage is 550 V dc from a tap on the high-voltage transformer secondary. The tap voltage (at pin 8) is rectified by diode D_2, filtered, and connected to a focus potentiometer (not shown in Figure 4.2).

4.6 BOOSTED *B*+ VOLTAGE

You learned from your early classroom lessons and lab experiments that two or more batteries could be connected in series to supply a total voltage equal to the sum of the individual battery voltages. Later you learned that you could do the same thing with ac to dc power packs, provided that neither dc output terminal was connected to an internal common ground. You further remember from lab that when you increase the dc supply voltage to an amplifier the output signal can be increased proportionately.

Combining these basic ideas provides the foundation for an increased dc supply voltage in the horizontal output circuit called the **boosted *B*+** or **bootstrap** voltage. It is common to use this supply voltage for the horizontal output amplifier only, but on occasion it may also be used for the vertical output circuits. Keep in mind that the boosted *B*+ source is from the horizontal output section. The boosted *B*+ section is seen in Figure 4.2 as a block between the +dc supply and pins 4 and 5 on the horizontal output transformer.

The circuit functions in this manner: The dc supply voltage is applied through the boost circuit to the collector of the horizontal output amplifier. As the amplifier starts to conduct, the output signal is fed to transformer T_2, where a portion of the signal (at winding 4) is rectified, filtered, and added to the supply dc voltage for an increased dc voltage to the collector of the output amplifier. The final result is that the output amplifier receives a dc operating voltage of about two times the *B*+ supply voltage, called boosted *B*+.

4.7 AUTOMATIC FREQUENCY CONTROL

Radar during World War II and consumer television soon thereafter were the first systems to employ the phase-locked loop (PLL) in a practical application on a large-scale basis. The horizontal oscillator is the VCO (voltage-controlled oscillator) that generates the signal frequency to be fed through the horizontal amplifier and horizontal output transformer back to the automatic frequency control (AFC) circuit. Here the feedback signal is compared to an externally applied synchronizing signal and converted to a dc voltage that

controls the frequency of the horizontal oscillator. The AFC circuit then is equivalent to the phase detector in the phase-locked loop circuit.

With *no* synchronizing signal applied, the horizontal oscillator will generate a free-running frequency signal as determined by the circuit components. The applied synchronizing signal will always be at a fixed frequency of 15,750 Hz. Therefore, the horizontal hold control must bring the oscillator frequency within the capture range of the PLL so that the oscillator will lock onto the frequency of the sync signal and be correctly timed.

The vertical and horizontal synchronizing signals are generated at the television station and are transmitted with the picture information. They are used to position the electron beam of the CRT at the receiver to match the location of the electron beam of the camera tube at the transmitting station.

4.7.1 AFC Circuits

There are some variations in the circuits used for automatic frequency control, but the general principles for all the circuits are exactly the same. Therefore, only one circuit will be analyzed in detail, with the understanding that all other similar circuits will achieve the same end results.

The typical AFC circuit of Figure 4.4 is comprised of a pair of opposing germanium diodes having one common terminal. That is, they are wired in series such that both cathodes share a common terminal with separate anodes or have common anodes with separate cathodes. A separate resistor is placed in parallel to each diode in order to develop a differential dc output voltage for the phase detector. The resistors must be of like value, which may range from about 1 kilohm (kΩ) to about 10 kΩ.

The phase detector will always have two input signal terminals and one dc output terminal. The synchronizing pulse signal is generally applied to the common terminal of the diode pair, while the horizontal output feedback signal is applied to the other end of only one of the diodes. The dc output terminal is the uncommon terminal of the second diode that is farthest away from ground potential. Examine Figure 4.4 to identify these features and become familiar with the circuit in general in order to follow the detailed explanation.

4.7.2 AFC Circuit Operation

Case I. In Figure 4.4, when only the positive horizontal output feedback pulse is considered at point *F* (no sync signal), a sawtooth voltage will appear at point *D* due to the integrator R_{416} and C_{418}. The

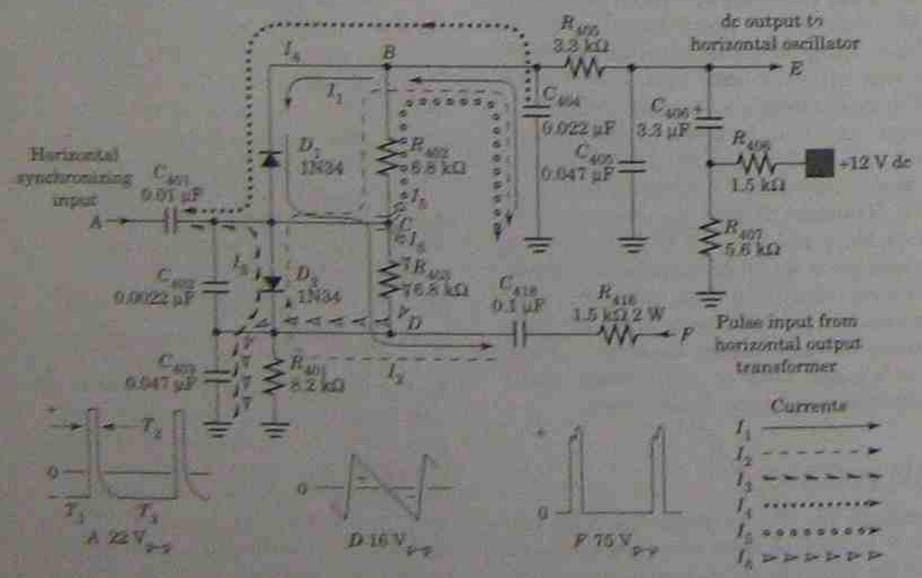


FIGURE 4.4
Automatic frequency control (AFC) circuit showing waveforms and dynamic current paths.

sawtooth voltage will change toward positive during the pulse time (retrace time) and decay gradually to negative during the trace time between pulses. When the sawtooth voltage is positive, diode D_1 conducts and current I_1 results. Current I_1 flows through C_{404} from ground, through diode D_1, down through resistor R_{403} to charge C_{418} negative on the left (positive on the right). The voltage across R_{403} due to current I_1 will make point *D* positive compared to point *C*. On the negative half-cycle of the sawtooth wave at *D*, C_{418} discharges, setting up current I_2, which flows through diode D_2 (D_2 is in cutoff), through R_{402}, through C_{404} to ground which neutralizes the charge on both C_{418} and C_{404}. Current I_2 through R_{402} sets up a voltage drop across R_{402} that is positive at point *B* compared to point *C*.

The net result is that the voltage across R_{403} due to I_1 is equal and opposite to the voltage drop across R_{402} due to I_2, so the sum of the voltages to affect an output of the phase detector will be zero. The voltage drop from point *B* to point *D* = 0.

Case II. This time the circuit will be examined when only the horizontal sync pulses are applied to Figure 4.4 at point *A*. Consider that time T_1 has passed and that the positive horizontal sync pulse at time T_2 is applied. Two currents will cause capacitor C_{401} to charge rapidly, as follows. Both diodes D_1 and D_2 are turned on. Current I_3 flows up from ground through C_{403}, through diode D_2, to the right side of C_{401}. At the same time, current I_4 charges capacitor C_{404} flowing up from ground, through C_{404}, through diode D_1, to the right side of C_{401}.

Between horizontal sync pulses, time T_3, the input voltage is low, capacitor C_{401} discharges, causing a current to flow from the right side of C_{401} to point *C*. At point *C*, the discharge current divides equally through R_{402} and R_{403}. The current labeled I_5 flows through R_{402} and C_{404} to ground, producing a voltage drop across R_{402} that is positive at point *B* compared to point *C*. The other half of the discharge current labeled I_6 flows through R_{403} and C_{403} to ground to develop a voltage drop across R_{403} that is positive at point *D* compared to point *C*. The sums of the voltages across R_{402} and R_{403} are equal and opposite and will cancel. The net error voltage from the detector due to the sync signal will be zero.

Case III. The sawtooth wave and the positive sync pulse are present at the same time. Remember that each wave separately resulted in a zero voltage drop between points *B* and *D*. Collectively, the same conditions will result when the two waves are present and at the same frequency, as seen in Figure 4.5b. The horizontal oscillator is at the same frequency as the input sync pulses, so the average dc voltage caused by the two ac waves is zero. The signals are balanced and locked together. An imbalance occurs only when the oscillator frequency does not match the frequency of the applied sync pulses.

When the horizontal oscillator frequency increases (shorter time per cycle), the positive part of the sawtooth wave causes a greater voltage drop across R_{402} than the voltage across R_{403}. The dc output voltage at point *E* will be more positive than it was when both signals had the same frequency. The positive voltage forces the oscillator to decrease in frequency. Figure 4.5c identifies this voltage condition.

Figure 4.5a shows the conditions for a lower oscillator frequency than desired (longer time per cycle). The negative part of the sawtooth wave is greater than the positive portion. The signal voltage across R_{402} will be larger than the voltage across R_{403}, resulting in a more negative dc voltage

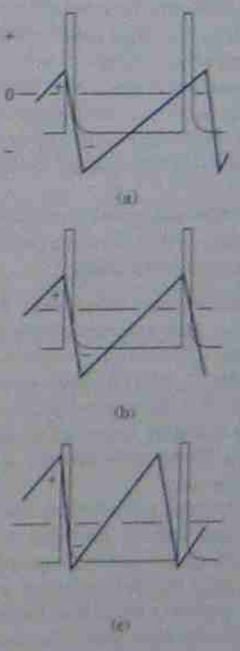


FIGURE 4.5
Horizontal sync pulse relationship to feedback wave frequency and resulting shift in dc output voltage.

at the point E output terminal (less positive dc compared to normal). A negative dc error voltage with respect to the reference voltage level will increase the oscillator frequency.

You have just struggled through a very detailed description of a relatively small circuit that takes into account only one of four possible conditions. The stated conditions are positive sync pulses and a positive horizontal feedback pulse. Both pulses can be negative, or two more cases can be cited where either pulse can be positive while the other pulse is negative. To fully describe three more circuits would be a total waste of time. One full circuit description was necessary to help you to realize that you can analyze a circuit to this depth when you are required to do so but, more importantly, it was done to help you to understand and recognize the relationships between the signals of the circuits.

For instance, in case I where the sawtooth wave was derived from a positive feedback pulse, the sawtooth wave charged in a positive direction during retrace time and in a negative direction during trace time. What differences would result when the feedback pulse is made negative? Answer: the sawtooth wave would be inverted, but the voltage drop across R_{402} and R_{403} would still cancel to end up with a sum error voltage of zero. The difference would manifest itself when the oscillator changed frequency. An oscillator frequency increase would now cause a negative change in dc error voltage, rather than the positive change as described in case III.

With all the suggested possibilities, let's draw some conclusions that will work for all the AFC circuits that you may encounter.

1. Use an oscilloscope to account for the magnitude, shape, and polarity of the sync and feedback pulses.
2. When diodes D_1 and D_2 share a common cathode connection, the input sync pulse must be negative going in order to turn the diodes on. Common anode diode pairs require a positive-going input sync pulse.
3. When both input pulses have the same polarity, the dc output voltage becomes more positive as the horizontal oscillator frequency goes higher than the sync signal frequency and more negative (less positive) when the oscillator frequency drops below the sync pulse frequency.
4. When the two input pulses are of opposite polarity (either pulse positive), the dc output control voltage behaves exactly opposite from the conditions described in item 3.
5. The horizontal oscillator (next section) can be designed by the engineer to increase or decrease in frequency for a +dc change in control voltage.
6. When measured with a dc voltmeter, the voltage from point B to point D should be zero for a correctly working circuit. In practice, the difference may be a few tenths of one volt (no sync signal applied).
7. The dc voltage at point C may be several volts away from ground depending on the design of the oscillator and AFC circuits.

The antihunt circuit shown in Figure 4.4 is basically a low-pass filter to slow down the reaction time of the dc control voltage. Some physical time will pass from the time the oscillator senses a dc voltage change to the time when the feedback pulse is returned to the AFC circuit. Twenty or thirty horizontal cycles may pass from the time of a dc voltage change to the time a correction is made. The oscillator could hunt back and forth before settling on the exact frequency. A slow-reacting control voltage will reduce or eliminate the hunting time.

4.8 HORIZONTAL OSCILLATOR

Two oscillator circuit types stand out as being the most popular from among the many possible oscillator circuit choices. They are the bistable multivibrator and the electron-coupled Hartley oscillators.

4.8.1 Multivibrator

In Chapter 3 you were introduced to the collector-coupled multivibrator as used in the vertical deflection system. That multivibrator is easily synchronized by an external pulse at 60 Hz.

The vertical sync pulses are recovered from the transmitted signal by a low-pass filter (integrator), which also removes all the noise contamination, which can cause false triggering.

The horizontal sync pulses are separated from the transmitted signal by a high-pass filter (differentiator), which also passes all the noise impulses. Second, the horizontal frequency is 262.5 times as high as the vertical frequency and is much more difficult to synchronize with a pulse signal.

It was determined very early in television history that the above two reasons were cause enough to dictate the use of a dc control voltage for frequency stability of the horizontal deflection oscillator. The emitter-coupled multivibrator is best suited for this application, along with the AFC circuit to supply the dc control voltage.

Figure 4.6 shows the circuit for a typical emitter-coupled multivibrator with appropriate waveshapes. The circuit is recognized by the single emitter resistor (R_6) shared by both transistors.

When power is first applied, both transistors will start to conduct. The voltage drop across R_6 will lower the collector voltage of Q_1, which is coupled through C_4 to the base of Q_2. Lowering the base voltage of Q_2 will drive Q_2 into cutoff.

The circuit examination begins (at the dot on the waveshapes) with Q_1 turned on and conducting heavily; Q_2 is off and C_4 is almost completely discharged.

When the charge on capacitor C_4 is completely exhausted, at time T_1, the voltage dividers R_7 and R_{10} supply a base voltage to Q_2 that starts Q_2 into conduction. When Q_2 conducts, the emitter current through R_6 increases the voltage at both emitters. This causes Q_1 to conduct less, reducing the voltage drop across R_6 and allowing C_4 to begin charging. Continued action cuts off Q_1 and turns on Q_2 hard. C_4 now charges between time T_1 and T_2. The charge path is from ground through R_{10}, through the base-emitter junction of Q_2, through C_4, through R_4 to the dc supply. The charge time is $(R_4 + R_{10})$ times C_4 = 10.569 microseconds (μs) and is the retrace time. When C_4 is fully charged, at time T_2, the base current of Q_2 is almost zero, lowering the emitter current of Q_2 and the voltage drop across R_6. This allows Q_1 to begin conduction again. The collector voltage of Q_1 decreases and starts the discharge of C_4 between times T_2 and T_3. T_3 is the same as T_1, and the cycle repeats itself. C_4 discharges through R_{10}, Q_2, C_{10}, and R_7 back to ground. The discharge time is $(R_6 + R_7)$ times C_4 = 72.2 μs to represent the trace time. The dc base voltage of Q_1 can be altered by the voltage-divider setting of the horizontal hold control R_2. Changing the base voltage of Q_1 changes the discharge time of C_4 and the frequency of oscillation. The arrow at the horizontal hold control indicates clockwise rotation.

The automatic frequency control dc voltage is applied to the base of Q_1 to control the frequency by setting the discharge time of C_4.

4.8.2 Electron-coupled Hartley Oscillator

From your early training you will remember that the Hartley oscillator uses the split coil for feedback and is a sine-wave generator. In the Q_1 circuit

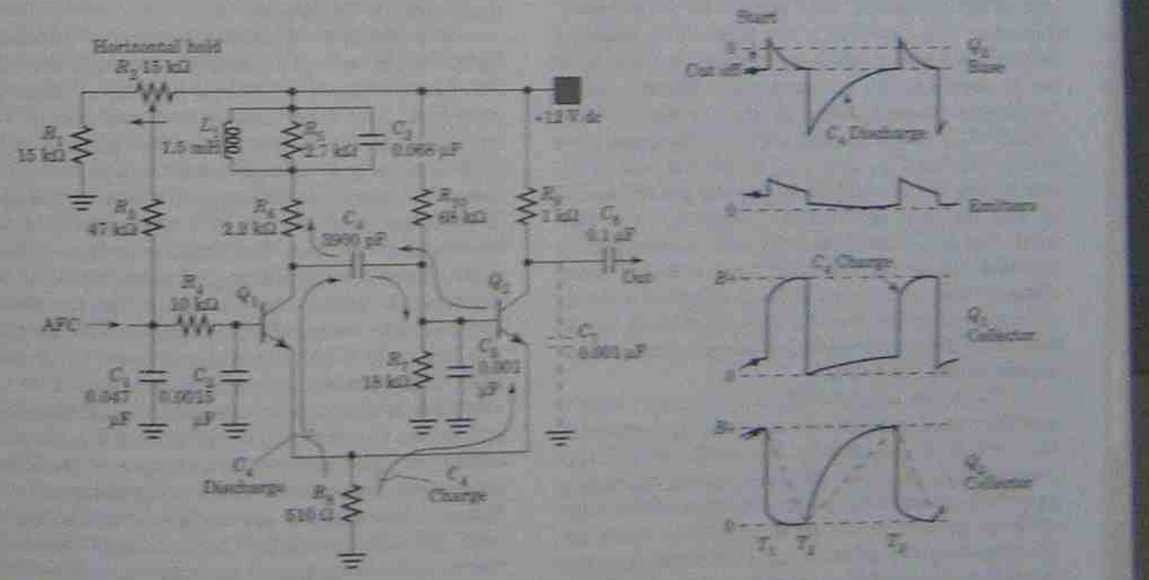


FIGURE 4.6
Emitter-coupled multivibrator as a horizontal voltage-controlled oscillator.

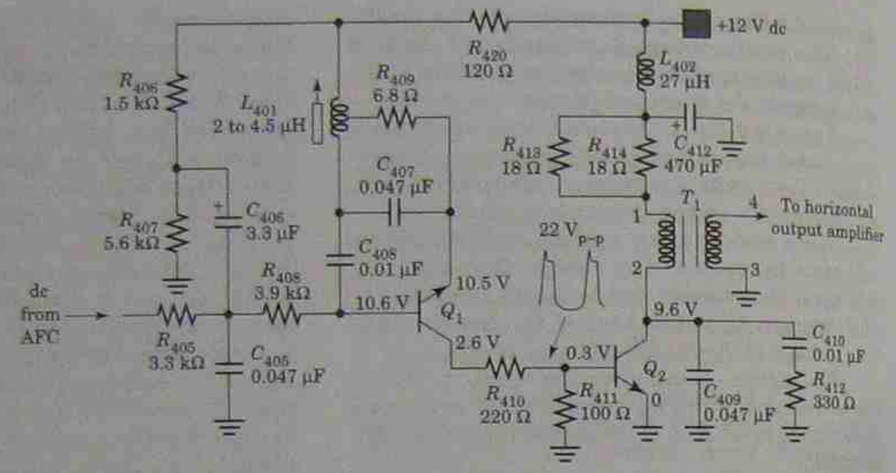


FIGURE 4.7
Electron-coupled Hartley oscillator (Q_1) and horizontal driver amplifier (Q_2).

of Figure 4.7, the transistor is operated in a class C mode with about a 120° conduction angle and sufficient feedback signal to drive the amplifier into full saturation. The output signal at the collector of Q_1 resembles a square wave with about a 33% duty cycle.

The in-phase feedback path is from the emitter of Q_1 through the tuned circuit of L_{401} and C_{407} and back to the base of Q_1 through C_{408}. Coil L_{401} adjusts the free-running frequency of the oscillator and is the horizontal hold control for this circuit. Capacitor C_{408} provides a low impedance path for the feedback signal while separating the base from the dc supply of the emitter circuit. The dc voltage for the base is established by the resistive voltage divider R_{406} and R_{407} and then by the capacitive voltage divider C_{406} and C_{405} to set the bias of Q_1 that affects the conduction angle and the off time of Q_1 and therefore controls the frequency of oscillations. The AFC circuit can now add its dc voltage to the base voltage for frequency change. A PNP transistor is used in this circuit so as to afford a low dc voltage connection for the direct coupling to the base of Q_2 driver transistor, although other configurations would also work.

The driver amplifier Q_2 is a *low-power class C* amplifier used to match the low input impedance of the horizontal output amplifier (to follow). It supplies base power to the amplifier during the output amplifier's conduction period. Because of the large collector current in the driver amplifier, heavy decoupling from the power supply is required, as evidenced by R_{413} and C_{412} along with L_{402}. The driver output is transformer coupled through T_1, with about a 3 : 1 step-down turns ratio, to the base of the horizontal output amplifier.

4.9 HORIZONTAL OUTPUT POWER AMPLIFIER

The horizontal output amplifier circuit in Figure 4.8 starts with transformer T_1. This is the same transformer T_1 seen in Figure 4.7 at the output of the horizontal driver amplifier.

You will also notice that the base of transistor Q_3 has no dc voltage source for biasing. From the four basic forms of transistor biasing (voltage-divider bias, base bias, emitter bias, and self- or signal bias), you can eliminate the first three because of the lack of a dc voltage source to the base. This leaves self-biasing by the applied signal to the base of Q_3 to establish the −0.15 V of dc found on the schematic at the base. The negative dc base voltage is developed during the negative half-cycle of the input signal, which charges C_{411} to that potential and holds the transistor deep into cutoff. The positive half-cycle of the input signal must be of sufficient magnitude to overcome this bias and drive the amplifier to near saturation. Piecing all these observations together tells you that the horizontal output amplifier is operated in a class C mode and conducts for less than 180° of the input signal cycle. These characteristics are typical of power amplifiers. DC current will flow in the class C amplifier when the base is pulsed positive enough to drive the amplifier into conduction. The collector dc current path (electron flow) is from ground, through Q_3

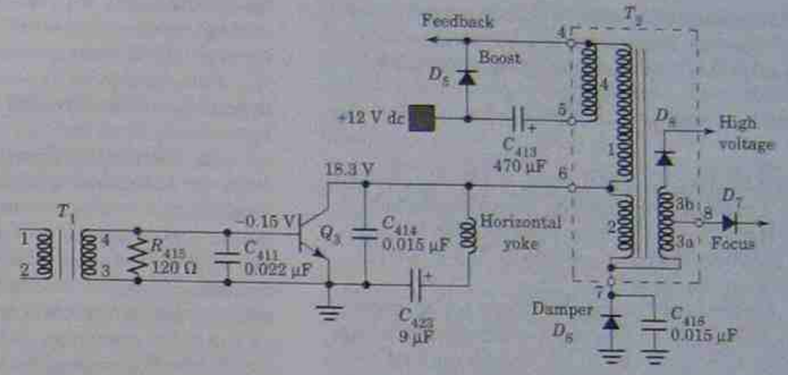


FIGURE 4.8
Horizontal output power amplifier, boosted B+, damper, focus, and high-voltage sections.

emitter to collector to pin 6 of the output transformer T_2, up to and out of pin 4, through the boost diode D_5 to the positive terminal of the dc power source. Failure of the output amplifier to conduct current describes a fault in this dc current path. Insufficient drive signal also holds the amplifier in cutoff where no dc current would flow. The horizontal output transistor is often in a TO-3 or TO-5 case because of the heavy current flow and is heat sinked.

When Q_3 conducts, the ac signal appears across primary winding 1 (pins 4 and 6) of T_2. The portion of the signal that appears across winding 4 (pins 4 and 5) also appears across the boost diode D_5 and filter capacitor C_{413}. Here the signal voltage is rectified, filtered, and added in series with the +12 V dc of the power source.

The schematic diagram in Figure 4.8 has 18.3 V dc at the collector of Q_3 for normal operation resulting from the boost voltage. These levels are small by comparison, because many receivers have boost voltages to 600 or more volts dc. Failure of the filter capacitor C_{413} would result in a reduced dc collector voltage and a linear narrow raster (i.e., horizontal size reduced equally on both sides of center).

A word of caution is warranted here, as well as offering an opportunity to extend a valuable servicing tip. The circuit of Figure 4.8 was chosen because it is straightforward and easy to test. However, you will encounter many horizontal amplifier circuits with a notation at the collector (on the schematic) that states, DO NOT MEASURE. This is because the voltage at the collector may exceed the breakdown voltage for the input of the test equipment, commonly about 600 V. But someone at some time had to measure these voltages in order to warn you of this condition.

EXAMPLE

Assume a horizontal amplifier with 500 V dc and 900 V_{p-p} signal at the collector. Your assignment is to verify the magnitude and shape of the signal for the company service manual. What would you do? Note that your oscilloscope would display only 160 V_{p-p} on the 20-V/cm sensitivity setting (highest setting). If you move the vernier control off the calibrate position, you are guessing at the reading.

Solution

Build a temporary voltage divider to suit your conditions and follow Figure 4.9 to show how it attaches to test point A. Equation 4.2 is for basic voltage dividers:

$$E_o = \frac{(R_1)(E_{in})}{R_1 + R_2} \qquad (4.2)$$

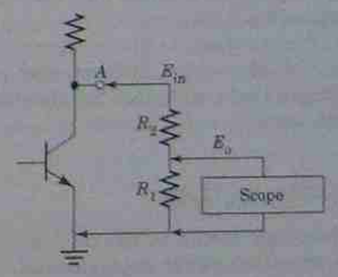


FIGURE 4.9
Voltage divider R_1 and R_2 with oscilloscope set up to measure large waveshape at test point A.

Make the ratio of R_1 to $R_1 + R_2$ any proportion of your choosing. Next, select any large value for R_1 and solve for R_2 by rearranging equation 4.2 as

$$R_2 = \frac{R_1(E_{in} - E_o)}{E_o} \qquad (4.3)$$

With a selected ratio of 6 : 1, E_o = 150 $V_{p\text{-}p}$. Make R_1 = 1 megohm (MΩ) and R_2 will calculate to be 5 MΩ. Here the 6 MΩ across a circuit with 900 $V_{p\text{-}p}$ will result in 150 microamperes (μA) p-p current loading on the circuit.

Or use your low-capacity scope probe, which has a built-in 10 : 1 frequency-compensated voltage divider. E_o will now be 90 $V_{p\text{-}p}$ (assuming that your scope input impedance is 1 MΩ).

4.9.1 Damper Diode

Compare the relative connections in Figure 4.8 between the Q_3 horizontal amplifier, the deflection yoke, and the damper diode, which is in series with winding 2 of T_2. All three branches are in parallel with each other, and the direction of current flow in Q_3 is opposite from the current flow in damper diode D_6. While the amplifier conducts, the damper diode is reverse biased and cannot conduct. The electron beam of the CRT moves from the center to the right edge as the amplifier conducts. When the amplifier is driven into cutoff, the transformer magnetic field decays and the electron beam is returned to the center of the CRT. The collapsing magnetic field induces a counter emf that moves the electron beam to the left edge of the CRT and forward biases the damper diode. The damper diode conducts, pulling current through the deflection yoke that moves the electron beam from the left edge back to the center of the CRT where the amplifier takes over.

The damper diode is like a clipper in parallel with the deflection yoke. It eliminates any overshoot voltages that could cause Barkhausen oscillation in the yoke.

4.10 HIGH VOLTAGE

The high-voltage section of the CRT is treated the same as any other power supply circuit. It has an ac voltage source, a rectifier, and a filter section. The main function is to convert an ac voltage to a dc voltage. This section differs only in that it functions at a much higher voltage level, and the ac voltage source is the horizontal oscillator signal through the flyback transformer. Make sure that the source generator is working, the transformer is operational, and the diode conducts only in one direction.

As you studied Figure 4.8, you may have noticed the absence of a high-voltage filter capacitor. Diode D_6 is a half-wave rectifier that, by itself, will output a pulsating dc voltage. Very early high-voltage circuits included a 2500-picofarad (pF) capacitor, rated at 50,000 working volts, and was very expensive. Modern circuits use the cathode ray tube as the filter capacitor. This works just as well as the 2500-pF capacitor but with a good saving in product cost.

Remember the Aquadag coating on the inside of the CRT that takes the place of the second anode. Then, by adding a coating of the same graphite material on the outside of the CRT, the tube becomes a capacitor (two conducting materials separated by an insulator). The outside coating is grounded by a spring clip riveted to the chassis and held tight against the outside of the CRT.

The electrostatic field around the CRT is a strong dust magnet. Dust on the CRT presents a high-resistance current path that can cause the high voltage to arc through to ground. Dust at the ground clip causes a poor connection that also results in arcing. Preventive maintenance suggests that the CRT be kept reasonably free of dust.

It is important to note that the CRT, as a capacitor, can hold a charge just like any other capacitor. In many cases, the charge remains for longer than 24 hours. Therefore, it is recommended that the anode and high voltage be discharged (set turned off) before any service is attempted in this section (see Section 4.11).

4.10.1 Voltage Multipliers

The horizontal output section is the same for monochrome and color CRTs with the exception of the high-voltage levels. Monochrome CRTs operate in the range from 10 to 15 kilovolts (kV), while color CRTs require 25 to 30 kV. The increase in high-voltage demand for the color CRT is the effect of adding a shadow mask in the path of the electron beam. The shadow mask restricts the number of electrons that strike the phosphor, which in turn lowers the raster brightness. Increasing the high voltage will raise the brightness level. This can be accomplished in several ways. The easiest way is to increase the number of turns on the high-voltage transformer secondary. This will make the transformer physically larger and somewhat more expensive.

Figure 4.10 shows the alternative method of voltage multiplication. Voltage multipliers work equally well at all voltage levels provided that the component parts are correctly rated. The input capacitor C_1 is rated at three times the applied peak voltage. It sees the greatest voltage swing and is therefore the most likely component cause of circuit failure. All other capacitors are rated at the peak ac voltage plus the anticipated dc voltage level at that point.

Figure 4.10a is a voltage doubler. The ac source, in this case, is the high-voltage transformer. When the input ac is on its negative half-cycle, D_1 conducts, charging C_1 to the peak voltage of the applied ac signal, negative on the left, positive on the right. On the positive half-cycle, D_1 is reverse biased, and D_2 conducts to charge C_2 to the peak voltage plus the charge already on C_1, equal to 2 V_{pk} (filtered to a dc value).

A voltage tripler is formed by adding section *b* to section *a* in Figure 4.10. On the next half-cycle of input voltage, diode D_3 conducts to charge C_3 to the peak voltage plus the dc voltage already accumulated on C_2, or to approximately 3 V_{pk}.

The voltage quadrupler uses all three sections of Figure 4.10. On the next half-cycle of applied input, D_4 conducts and charges C_4 to the peak voltage plus the dc already accumulated on C_3, or to approximately 4 V_{pk}.

4.10.2 X-radiation

X-rays are radiated energy in the frequency range above 1 petahertz (10^{15} Hz) that can penetrate human skin tissue. They are produced when electrons experience a rapid change in velocity.

Radiation occurs in and around the cathode ray tube where the high-velocity electron beam strikes the phosphor, gives up its energy in the form of light photons, and then exits the CRT as low-velocity current. When the anode voltage is below about 10,000 V dc, the electron velocity is too slow to produce any measurable x-radiation. Increasing the anode voltage linearly above 10,000 V will result in an exponential increase in x-radiation.

The Federal Department of Health, Education, and Welfare (HEW) has set maximum safe exposure limits based on almost 40 years of exposure records and health effects on people in this environment. The recommended maximum *safe* radiation levels set for consumer products is 0.5 mR/h (milliroentgens per hour) at a distance of 5 centimeters (cm) (2 in.) from the surface of the product. Roentgens is pronounced "runt-gins." Radiation strength is reduced by the **inverse square law** for distance from the source; that is, 0.5 mR at 2 in., 0.125 mR at 4 in., 0.03125 mR at 8 in., 7.8 μR at 16 in., and so on. The health physics program has set maximum safe exposure rates for people who work around nuclear reactors at 300 mR per week accumulated over the life of the employee. These limits are well below those set by HEW for such employees. The conclusion here is that, *yes*, there is x-radiation from consumer products that use cathode ray tubes, but the managed levels are so low that even the level given off by a malfunctioning product is harmless at distances over 2 in. away over your entire lifetime. X-rays are discussed here to dispel any fears or misconceived ideas that there is danger from x-rays emitted from these products.

The importance of this discussion is twofold. (1) Certain components of the receiver control the level of the emitted radiation. They are usually identified by a shaded box around the part on the schematic. They should be replaced by *exact* manufacturer parts if the radiation level is to be maintained low. (2) The horizontal hold-down circuits associated with the x-ray protection may cause misleading symptoms of a straightforward circuit problem.

There are no standard hold-down circuits, so you should look for a circuit on the schematic that senses excessive current or voltage. Both sensors

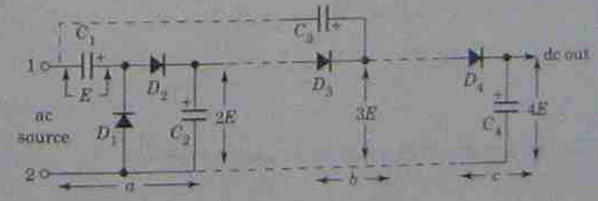


FIGURE 4.10
Voltage multipliers: (a) voltage doubler; (a + b) voltage tripler; (a + b + c) voltage quadrupler.

work in the same way. When the current or voltage exceeds the design value, the sensor activates a latch, which in turn either shuts down the horizontal oscillator or throws the horizontal so far off frequency that a nonviewable picture results. The latch remains engaged until the set is turned off, and the charge on a capacitor is allowed to dissipate. The x-ray protection circuit monitors the CRT beam current. When this current exceeds standard safe leads, the protection circuit shuts down the horizontal oscillator and kills the high voltage. The voltage sensor monitors the horizontal retrace time from the flyback transformer and rectifies the voltage as bias for the latch circuit. The point is that a no-raster condition traced to a failure in the horizontal oscillator may be further traced to the horizontal hold-down circuit.

4.11 TROUBLESHOOTING

A complete horizontal section schematic, shown in Figure 4.11, is the combination of Figures 4.4, 4.7, and 4.8. Included are D_1 and D_2, the AFC phase detector, the electron-coupled Hartley oscillator Q_1, the driver amplifier Q_2, the horizontal output power amplifier Q_3, the horizontal deflection yoke, the boosted $B+$ circuit (D_5), the damper circuit (D_4), the flyback transformer, and the high-voltage and focus-voltage circuits (D_7).

For troubleshooting in the horizontal section, we will use Figure 4.12 to show a common defect and then the text will identify the section and probable cause of that defect. Except as noted, only a raster is needed to observe these conditions.

4.11.1 Keystone Raster

The deflection yoke is the only component that can cause a keystone-shaped raster. The yoke in Figure 4.11 has only one coil for ease of drawing, but remember that the horizontal deflection yoke has two coil sections placed above and below the neck of the CRT. An internal short between turns of coil wire causes a reduction in deflection distance. A defective bottom coil will produce the effect shown in Figure 4.12a, while Figure 4.12b shows a partially shorted top coil section. Generally, the shorted turns cannot be repaired and the yoke must be replaced.

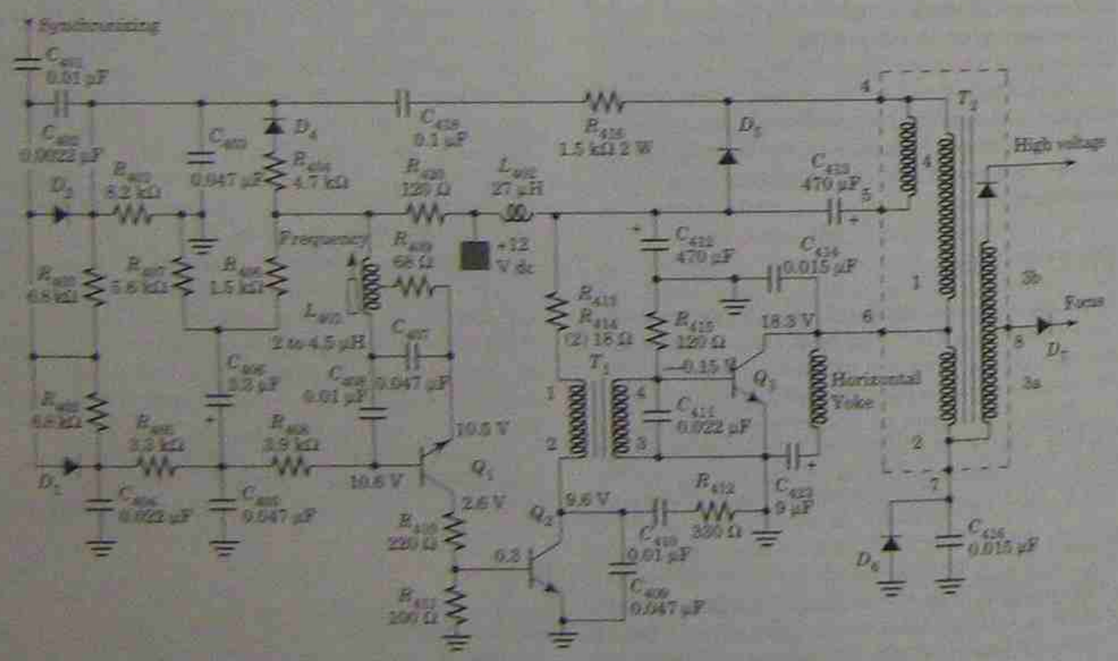


FIGURE 4.11
Complete horizontal deflection and high-voltage schematic (the combined Figures 4.4, 4.7, and 4.8).

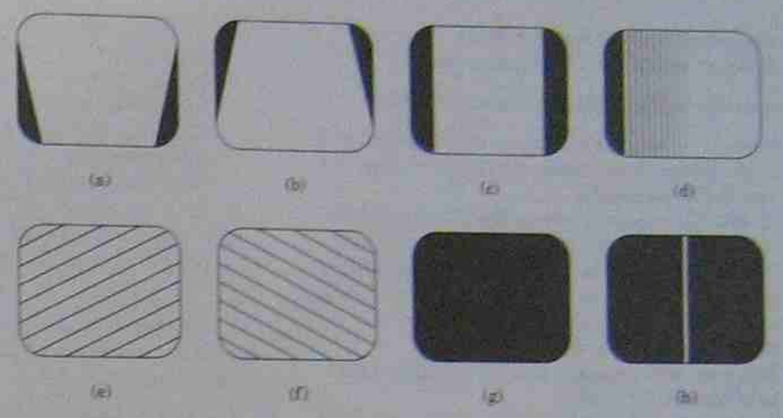


FIGURE 4.12
Visual effects on the face of the CRT for various horizontal and high-voltage section defects (see text).

4.11.2 Narrow Raster

When the raster shrinks in linearly from both sides (see Figure 4.12c), the effect is called a narrow raster. This results from a signal smaller than required to fully deflect the beam sideways. The amplifier gain is suspect, normal operation of the boosted $B+$ circuit is suspect, and a reduced drive signal to the amplifier is suspect. Compare the amplitude of the signal at the base of the horizontal amplifier to the waveform given in the service manual. The measured voltage level should be within 10% of the recommended value. If you cannot find the fault based on ac waveshape measurements, then make a chart of the dc voltages at the emitter, base, and collector of all three transistors. Do not make a decision based on only one or two readings. Measure all nine voltages in this case, and compare the voltages to those marked on the schematic diagram.

A distorted raster only to the left of center (Figure 4.12d) can be traced to a defect in the damper circuit, especially when the distortion is accompanied by several bright vertical lines on the left side. An open damper diode is followed by a shorted damper capacitor in the order of logical things to look for in testing the damper circuit.

4.11.3 Horizontal Frequency

Figures 4.12e and f identify an incorrect oscillator frequency. Figure 4.12e is typical of a frequency higher than 15,750 Hz, and Figure 4.12f, a frequency lower than 15,750 Hz. Note that these conditions can only be observed when picture information is present. We are not ready to treat synchronizing problems at this time, but neither can we ignore incorrect frequency effects while studying the horizontal deflection system. Chapter 7 will cover the subject more completely.

4.11.4 No Raster

In preparation for tackling a problem of this nature, it is essential to clarify some terms. No raster means there is no brightness on the face of the CRT. No picture means that there is brightness on the CRT, but no picture information is present. Learn to distinguish the difference between these two words.

Divide the circuit in half by first checking for a signal at the base of the horizontal output amplifier. If there is no signal here, then work backward with your scope probe to check the signal at the driver amplifier and then at the oscillator.

If you find a signal at the base of the horizontal amplifier, then work toward the high-voltage output section. Look next for a signal at the collector of the output amplifier. If you cannot view this signal directly, then use the voltage-divider method to assist in the viewing. When you find no signal, check the dc current path as described in Section 4.9.

More creative testing is in order when you have a pulsed voltage at the collector of the output amplifier, but still do not have a raster. Some probable causes and tests are as follows:

1a. A number of shorted turns in the yoke can cause a change in impedance that will load down the output transformer and kill the high voltage.

2a. A number of shorted turns in the flyback transformer can have the same effect as in item 1.

3a. Open high-voltage rectifier diode.
4a. A defective CRT or CRT biasing circuit.

The tests for these defects are varied. You may

1b. Measure the dc resistance of the yoke and high-voltage transformer compared to the values on the schematic.
2b. If test 1b is inconclusive, there are commercially available yoke and transformer testers.
3b. You may substitute a known working unit in place of the yoke or transformer. These units are expensive, so this method is used only by facilities that stock replacement parts.
4b. Measure and compare the dc voltages at the base of the CRT socket.
5b. Test the emission of the CRT using a standard tube tester.

There is a final test used by only the most experienced technicians when no other testing devices are readily available. Used carelessly, the individual is in jeopardy of an electric shock. It is not lethal, but it is not pleasant either. If you think about using this test yourself, find and work with an experienced technician on your first attempt. Read the full outline first and then proceed as follows:

1. Turn off the display device (assumed to be out of the cabinet or case and exposed for testing).
2. Discharge the high voltage by connecting a temporary jumper wire from chassis to the high-voltage button on the CRT (under the suction cup). Then remove the shorting wire.
3. Remove the high voltage wire connection at the CRT end. Inspect the wire for cracked or peeling insulation. Continue only if the wire is in good condition.
4. Hold the high-voltage wire in one hand at least 6 in. from the exposed open end. Hold your hand and the exposed open end of the wire well away from any metal parts of the chassis.
5. Use caution from here to the end of the test. Turn the power on and then place your free hand behind your back. Do not touch the chassis with your free hand.
6. *Slowly, slowly* move the exposed end of the wire toward a metal ground point.
   a. As you approach to about 3 in., you will begin to hear a hissing sound and detect a strange odor. This is a corona hiss; the high voltage begins to break down air ions to create ozone.
   b. As you move the wire closer to the chassis, you will see a *purple* or *violet* arc that makes a hissing sound. *Immediately* move the wire away from the chassis.
   c. Move the exposed open end of the high-voltage wire close to the button on the side of the CRT. You will soon hear a snapping arc that is *blue* in color. *Immediately* move the wire away from the CRT button.
   d. Turn the power off, then touch the open end of the high-voltage wire to chassis ground. Discharge the CRT button as outlined in step 2.

You may now safely replace the high-voltage wire connection to the CRT as you draw the following conclusions.

1. A purple or violet hissing arc is indicative of an ac voltage. A strong arc as noted in step 6a indicates that the high-voltage transformer and rectifier are working. The ac in this case is a pulsed voltage.
2. A blue snapping arc as noted in step 6c is normal for a dc voltage. A single snap indicates charging the CRT as a filter capacitor. A continuous snapping arc implies that the CRT will conduct current and is probably normal.

Finally, look at Figure 4.12h. Stop reading for now and see if you can determine under what conditions you would see a single vertical bright line on the face of the CRT. Any condition that you can name except one would not cause this effect. You must be watching the CRT as a failure occurs or you may never see this in your entire lifetime. It is actually a trick question. You already know that when any horizontal circuit fails completely there will be no raster. If you are watching as the fault happens, you will see the raster collapse to the center (Figure 4.12h), and then the high voltage fails and the line disappears.

4.12 PINCUSHION CORRECTION

Vertical and horizontal pincushion effects are treated at the same time for simplicity and continuity. Pincushion effects are seen in Figure 4.13 as a raster that is not truly rectangular in shape. The effects are exaggerated here for purposes of illustration but, nonetheless, they are noticeable even to the casual observer. The raster acquires this shape because the edges of the CRT (top, bottom, right, and left) are closer to the pivot point where the deflection bends than they are from the corners. As a result, the corners appear to be extended, giving the raster this shape.

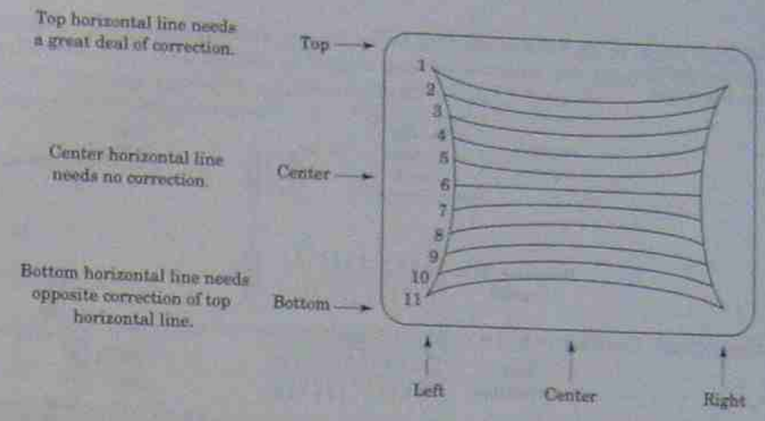


FIGURE 4.13
Pincushion raster.
The center horizontal scan line needs more amplitude than top or bottom horizontal scan lines.

In monochrome systems, the correction is to glue small magnets to the deflection yoke housing at positions and with strengths and polarities that will restore the raster to the desired rectangular shape.

In the case of color deflection systems, small correction magnets attached to the deflection yoke will affect the color purity and convergence more adversely than the problem they are intending to correct. Pincushion deformities and their solutions have been around for so long that some manufacturers take care of the problem as a daily routine and may not include the condition on the schematic. Other manufacturers make a clear point to show the corrections and include an adjustment procedure.

The correction takes the form of simply adding two voltages together in each direction, vertical and horizontal. But, ironically, the horizontal correction comes from the vertical circuits, and the vertical correction comes from the horizontal circuit.

Look again at Figure 4.13 where only 11 horizontal lines are shown for simplicity. Analyze the horizontal notes. You can see that the center horizontal line (6) needs more amplitude for it to cover the same width as the top and bottom lines, and that the correction should come from the vertical section. Note also that the correction waveshape in Figure 4.14 takes the liberty of using a sawtooth wave to identify the scanning action, rather than the true trapezoidal wave.

The vertical rate signal is shaped into a *parabolic* voltage wave and added through a transformer in series with the horizontal yoke coils to yield the sum voltage waveshape. Note that the voltage amplitude at the center of the scan sum voltage in Figure 4.14a is greater than the top and bottom of the scan.

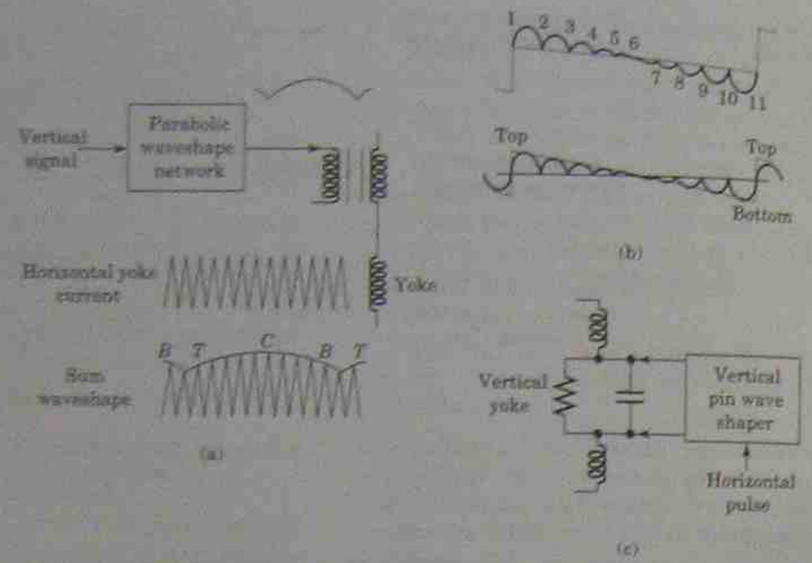
To correct each separate line, read the vertical rate notes in Figure 4.13. The top line needs positive correction, the center needs no correction, and the bottom line needs negative correction. Therefore, a separate correction pulse is added to the vertical deflection sawtooth wave for each horizontal line to be scanned. Figure 4.14b shows the sum waveshape first so that you can see where each horizontal correction pulse is added to the trace of vertical sawtooth wave. Next, the correction wave in Figure 4.14 is exaggerated to show the positive and negative correction. Finally, the pincushion correction transformers are wound into the deflection yoke on many receivers and are not seen separately.

4.13 CONVERGENCE CORRECTION

Convergence correction is similar to pincushion correction. Both modify the position of the electron beam at the edges of the CRT. Convergence differs from pincushion in that convergence will control the position of each electron beam separately. Pincushioning is constant and predictable; convergence is not because of the small size and large number of phosphor dots, plus the critical mechanical alignment between the electron gun, the shadow mask, and phosphor dots. Convergence may also be affected by any surrounding magnetic fields.

Figure 4.15 shows only three horizontal scan

FIGURE 4.14
Vertical and horizontal pincushion correction circuits.



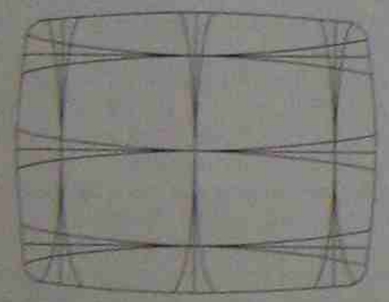


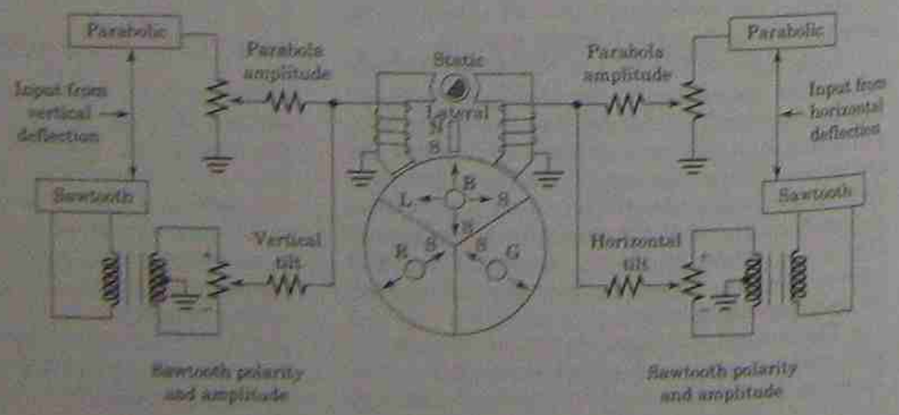
FIGURE 4.15
Convergence pattern showing three horizontal and three vertical lines only. Each of the nine lines is comprised of the three electron beams that converge at the center of their respective traces and diverge away from center.

lines and three vertical scan lines. A true convergence signal applied to the receiver, called a **cross-hatch pattern,** will have 30 horizontal lines and 40 vertical lines. Only the center and edge lines are shown in Figure 4.15.

Review Figure 2.10 as a reminder of how the beam focus and beam crossover at the center are different than at the edges. This difference occurs at the top, bottom, left, and right edges of the tube.

The correction voltages are a combination of a *parabolic* wave and a *sawtooth* wave. The parabola has polarity only in the positive direction, which will move the convergence point closer to the phosphor screen. The adjustment is called the **amplitude** control. The sawtooth wave needs to be either positive or negative, depending on which way the

FIGURE 4.16
Convergence circuit and controls for the blue electron gun only. Equal circuits are needed for the red electron gun and green electron gun.



correction is needed. The sawtooth adjustment control is often called the **tilt** control. The signal sources, waveshaping networks, and application methods are shown in Figure 4.16 for only one electron gun.

The convergence theory is given here, but the correction adjustments are delayed for an in-depth procedural list in Chapter 8.

QUESTIONS

4.1 One part of the horizontal deflection section is a continuous signal generator.
(a) true
(b) false

4.2 What class of amplifier is the horizontal output?
(a) class A,
(b) class B,
(c) class C, or
(d) none of the above

4.3 The frequency of the horizontal oscillator is
(a) 525 Hz,
(b) 15,750 Hz,
(c) 262.5 Hz,
(d) 60 Hz,
(e) 30 Hz.

4.4 The time for one full horizontal cycle is
(a) 11.5 μs,
(b) 15.3 μs,
(c) 52 μs,
(d) 16.6 μs,
(e) 63.5 μs.

4.5 The time of the horizontal trace is
(a) 16.6 ms,
(b) 11.5 μs,
(c) 15.3 ms,
(d) 52 μs,
(e) 63.5μs.

4.6 The time of the horizontal retrace is
(a) 16.6 ms,
(b) 11.5 μs,
(c) 15.3 ms,
(d) 52 μs,
(e) 63.5μs.

4.7 The effect on the face of the CRT when the horizontal oscillator fails completely is
(a) a keystone-shaped raster,
(b) slanted diagonal lines,
(c) a narrow raster,
(d) one bright vertical line,
(e) no raster.

4.8 The effect on the face of the CRT when the horizontal driver fails completely is
(a) a keystone-shaped raster,
(b) slanted diagonal lines,
(c) a narrow raster,
(d) one bright vertical line,
(e) no raster.

4.9 The effect on the face of the CRT when the horizontal amplifier fails completely is
(a) a keystone-shaped raster,
(b) slanted diagonal lines,
(c) a narrow raster,
(d) one bright vertical line,
(e) no raster.

4.10 The effect on the face of the CRT when the horizontal output transformer fails completely is
(a) a keystone-shaped raster,
(b) slanted diagonal lines,
(c) a narrow raster,
(d) one bright vertical line,
(e) no raster.

4.11 The effect on the face of the CRT when the high-voltage rectifier fails completely is
(a) a keystone-shaped raster,
(b) slanted diagonal lines,
(c) a narrow raster,
(d) one bright vertical line,
(e) no raster.

4.12 The horizontal amplifier conducts to move the electron beam over what part of the CRT screen?
(a) top to bottom,
(b) left to center,
(c) center to bottom,
(d) center to right

4.13 The damper diode conducts to move the electron beam over what part of the CRT screen?
(a) top to bottom,
(b) left to center,
(c) center to bottom,
(d) center to right

4.14 In your own words, briefly tell how the boosted $B+$ is developed.

4.15 The signal at the output of the horizontal amplifier cannot be measured.
(a) true
(b) false

4.16 What value of voltage dropping resistor would you use to measure 250 V across a 430-kΩ load from a 3500-V source?
(a) 33 kΩ,
(b) 72 kΩ,
(c) 430 kΩ,
(d) 2.5 MΩ,
(e) 5.6 MΩ

4.17 What polarity of horizontal sync pulse is applied to a horizontal AFC circuit when the diode cathodes share a common terminal?
(a) positive sync,
(b) negative sync,
(c) it depends on the polarity of the horizontal feedback pulse

4.18 Name two common types of horizontal oscillator circuit.

4.19 Which stage in the horizontal deflection block diagram is not used to produce a raster?

4.20 Which of the following circuits conducts during the full horizontal cycle?
(a) horizontal oscillator,
(b) damper diode,
(c) horizontal amplifier,
(d) horizontal driver

4.21 The damper capacitor charges when the damper diode is
(a) conducting,
(b) cut off.

4.22 What are three names given to the horizontal output transformer?

4.23 What two voltages add together to form the boosted $B+$?

4.24 Explain why a trapezoidal voltage waveshape is required to drive the horizontal deflection yoke.

4.25 Identify a method to measure the horizontal yoke sawtooth current waveshape to determine linearity.

4.26 Draw slightly more than one full cycle of the horizontal sawtooth current waveshape and identify the following:
a. The trace and retrace parts of the wave.
b. The left and right sides of the raster.
c. The part of the wave where the horizontal amplifier is conducting.
d. The part of the wave where the damper diode is conducting.

5 The Video Signal

5.1 INTRODUCTION

The video signal is unique in that it contains an analog information signal, six different pulsed signals, a pilot signal, two buried but distinguishable color signals and a specific polarity requirement. No other unmodulated signal is its equal.

5.2 ONE LINE OF VIDEO (ANALOG)

Look at the photo in Figure 5.1 and examine the change in brightness level along the one line highlighted in the photo about one-third of the way down the screen. Assume for the minute that more brightness means a larger positive voltage, and the darker areas resulted from a lesser positive voltage. It would be presumptuous to believe that a hand-drawn sketch could exactly duplicate the changes in voltage necessary to equal the quality of the true waveshape on this line. An approximate reproduction of the voltage wave, however, is shown in Figure 5.2a, with white in the positive direction and black (or dark) in the negative direction.

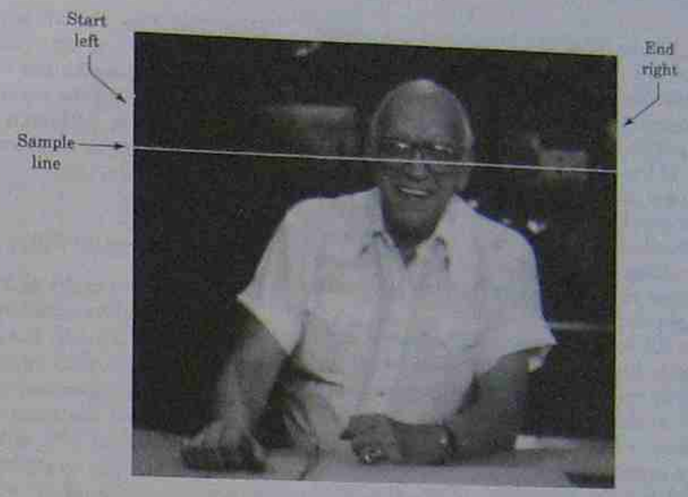
The scan line will start at the left side of the CRT screen and at the left side of the oscilloscope display. The video information line on the television screen *and* the scope display both end on the right side. Compare Figure 5.1 to Figure 5.2a to reinforce this idea. The whiter areas of the picture are toward the top of the wave and the darker areas are toward the bottom of the wave.

Each line of video is different from the line before it and after it. Take another sample line, about two-thirds of the way down the screen, say about the level of the elbows. This line will start at the left in the shadows (dark and low voltage), then alternate lighter and darker as it scans across the grill work, then half white as the scan moves across the right arm, then dark again between the arm and the body. The signal level will go to near maximum voltage (whitest area) as it moves across the white shirt, then lower voltage as it covers the dark area between the arm and body, and half white again across the left arm then dark again across the background and end with an alternating lighter and darker pattern as it scans the grill work at the right hand side of the picture.

5.3 HORIZONTAL BLANKING PULSES

At the end of the line of video, the CRT must be turned off so that the retrace voltage (back to the left) does not appear in the picture. A horizontal blanking pulse is shown in Figure 5.2b going in a negative direction, not just to the black level, but beyond to a level called **blacker than black.** This level does not exist in reality, but only in applied voltage values. It says that if a negative-going pulse of 10 volts (V) will turn the CRT off, then a 12-V pulse will ensure that the CRT is well into a cutoff state. A blanking pulse is shown at the left in Figure 5.2b to represent the line preceding our sample line, and a second blanking pulse is shown to the right for association with our sample line of video. Each line is framed with a blanking pulse of approximately 11.5 microsecond (μs) duration.

FIGURE 5.1
One line of video signal.



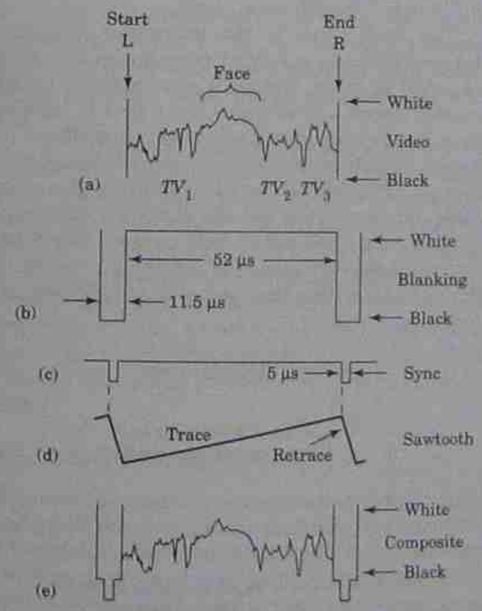


FIGURE 5.2
Voltages for the construction of one line of video: (a) the video signal; (b) the blanking pulses; (c) the sync pulses; (d) comparative horizontal scanning sawtooth; (e) the composite video signal.

5.4 HORIZONTAL SYNCHRONIZING PULSE

Synchronizing the horizontal deflection oscillator at the receiver should take place during the blanking period. The horizontal sync pulse drives the video signal farther into the blacker than black region, holding the CRT farther into cutoff. A positive pulse here could be mistaken for video information, whereas the negative pulse would not. The amplitude of the sync pulse will be about one-third as strong as the blanking pulse, or 25% of the total signal amplitude.

The horizontal sync pulse shown in Figure 5.2c starts 1.5 μs after the leading edge of the blanking pulse and stays on for only 5 μs. The decay of the sync pulse takes place about 5 μs before the end of the blanking interval. The leading 1.5-μs delay is called the **front porch,** and the trailing 5 μs after the sync pulse is called the **back porch.**

A sawtooth wave is shown in Figure 5.2d to identify that the sweep retrace period begins at the leading edge of the sync pulse and must be completed before the end of the blanking pulse time. The leading edge of the sync pulse sets the horizontal oscillator to begin the next cycle. The oscillator is triggered every cycle.

5.5 COMPOSITE VIDEO SIGNAL

Composite means the sum of the parts. In this case, it is the sum of the video information, the horizontal blanking pulse, and the horizontal sync pulse all

added together to form the horizontal composite video signal. Our sample line of video is shown in Figure 5.2e as this composite video signal.

Any signal that is amplified by a common emitter amplifier or inverting op-amp will change the polarity of the signal by 180°. That is, the sync pulses will now be at the top of the wave and the white video signal will be at the bottom of the wave. You should become familiar with the shape of the video wave in both polarities. As you examine the video signal at different locations in the circuit, it will change polarity.

Figure 5.3 is the inverted video signal used here to identify the percent of amplitude for all the signal levels as set forth by the NTSC and adopted by the FCC* in the mid-1940s. The color burst signal (color sync) is included at this time without explanation in order that you know its location, because it will become important later. The color burst is located on the back porch of the horizontal blanking pedestal.

The original levels identified no signal as 0% of the signal. The tip of the sync pulse was set at 100% of the peak signal, which then made the reference white level 12.5% of peak, the black reference level 70% of peak, and the blanking level 75% of peak.

5.5.1 Negative and Positive Picture Phase

When comparing Figure 5.2e to Figure 5.3, the obvious difference is the phase of the voltage wave. It can further be reasoned that the typical television scene will be primarily bright, with flashes of gray or black to show shading or darkness. The blanking and sync pulses are in the blacker than black region. Therefore, the white polarity of the wave, being positive, has the name **positive picture phase.** In Figure 5.3 the white parts of the signal are negative, and the wave is called the **negative picture phase.** Although the picture phase may have little meaning to you now, it has great significance later in the text.

5.5.2 Horizontal Pulse Timing

There may be as many as 1 million TV receivers for every television transmitting station. They must all be compatible. That is, the control signals that they send and receive must be identical.

Comparing the time reference only in Figure 5.4, we see that the maximum time for the entire blanking pulse (at 10% of rise time) is $0.18H$ (H is the time for one complete horizontal cycle, or 63.492 μs). 18% of H = 11.4285 μs, which is rounded off to 11.5 μs in this text. After allowing for the rise time of the blanking pulse, the front porch is set at $0.02H$ minimum, or 1.27 μs. The width of the horizontal sync pulse may range from 0.07 to $0.08H$, or 4.44 to 5.08 μs. This leaves 5.078 to 5.718 μs for the full back porch.

The back porch to the horizontal blanking pulse now takes on a special meaning as the color sync signal is added. The color sync signal is called the **color burst** and is a sine wave that is used to control the frequency and phase of an oscillator in the color circuits of the receiver. The oscillator generates a carrier signal for demodulating the color signals, but since it is not the station's main carrier, it is called the **color subcarrier.** The color subcarrier has a frequency of 3.579545 megahertz (MHz) ±10 Hz with a time per cycle of 0.279365 μs

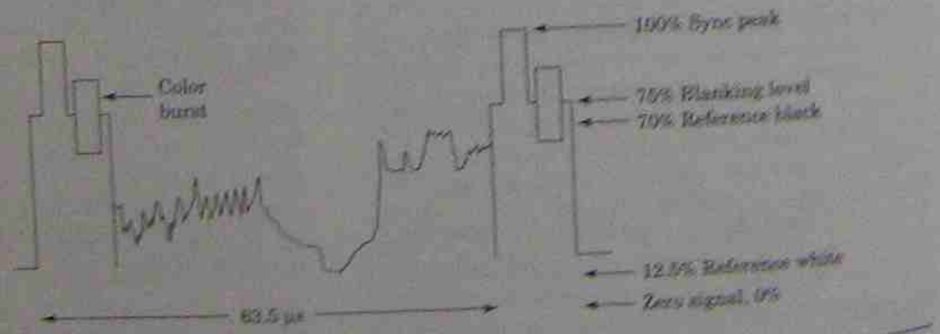


FIGURE 5.3
The horizontal composite video signal showing the relative amplitudes (in percent of peak) for the identifiable levels of signal.

*The Federal Communications Commission. The federal regulating body that sets standards for all electronic signals and controls the airways for RF transmissions in the United States.

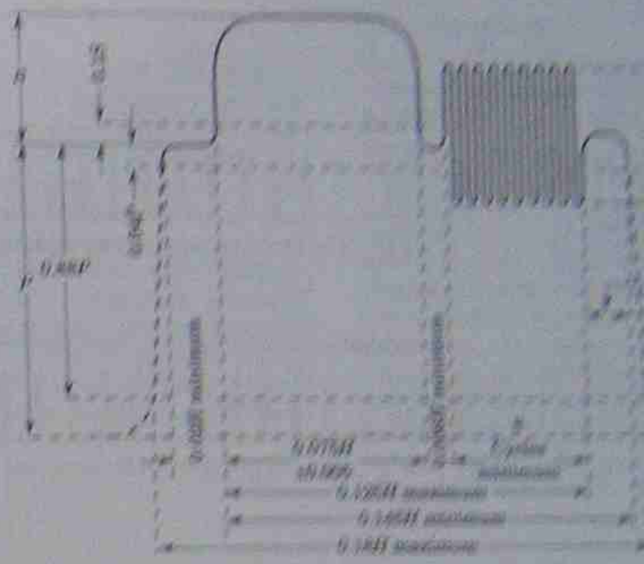


FIGURE 5.4
Timing for the horizontal blanking and synchronizing pulses, including 9 cycles of the color sync (burst) signal.

The color burst will contain 8 to 10 cycles of the color subcarrier signal, making the time for the burst signal between 2.225 and 2.795 μs. The space between the decay of the horizontal sync pulse and the start of the burst signal is called the **breezeway** and is held to $0.008H$, or 0.38 μs. The remaining length of the back porch, after the color burst is called the **back back porch** for finite identification.

Generally we identify the front porch as 1.5 μs in time and the horizontal sync pulse as lasting 5 μs. The remaining period of time is referred to simply as the back porch, which contains 8 to 10 cycles of the color subcarrier at 3.58 MHz. The generators at the transmitter end of the system maintain these standards with rigor, while at the receiving end of the system, where we have no control of the signal, we simply check to see that the signal contains all the correct parts in about the right proportions.

5.6 VERTICAL BLANKING

The vertical scanning sequence requires blanking and synchronizing pulses just like the horizontal rate signal. After a series of 241.5 horizontal lines has been scanned, a vertical blanking pulse is initiated. The vertical blanking time was originally set at 6% to 8% of the vertical cycle. That is the time for 13 to 21 horizontal cycles. But because of recent developments, the vertical blanking pulse is now held to exactly 8% of the vertical cycle time and

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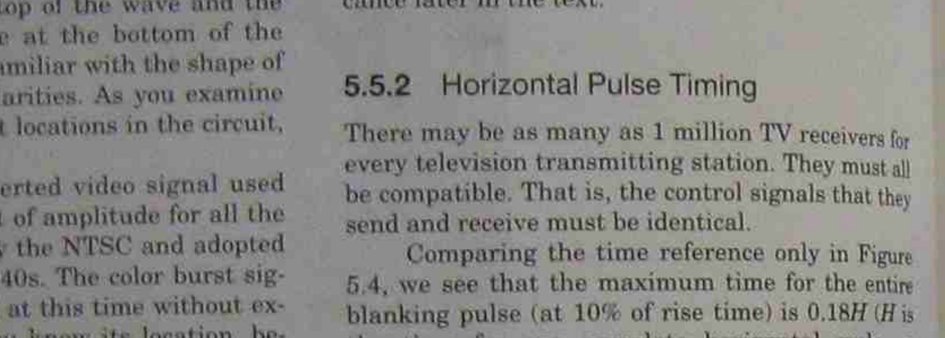

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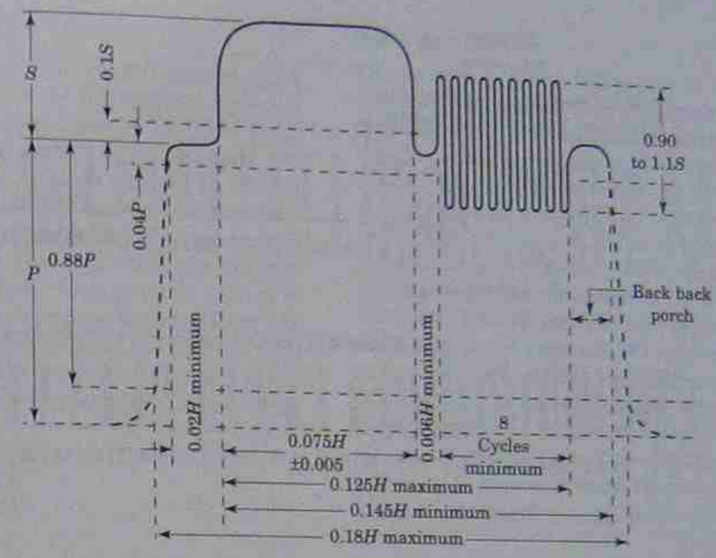

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The amplitude of the vertical blanking pulse is the same as the horizontal pulse at 75% of peak signal. Refer to Figure 5.5 as you read the next sec- tion.

5.7 VERTICAL SYNC PULSE

The vertical sync pulse begins at three horizontal cycle times after the start of the vertical blanking pulse. This sets the vertical front porch at 190.5 μs in length. The vertical sync pulse itself also spans three horizontal cycle time periods for another 190.5 μs. The back porch of the vertical blanking pulse takes up the remaining 952.3 μs of the verti- cal blanking period.

5.7.1 Equalizing Pulses

It was observed that when the horizontal deflection oscillator at the receiver was not synchronized for 21 cycles (during vertical blanking), the top of the picture display wiggles until the horizontal oscilla- tor locked onto the sync pulses after the vertical blanking time. More importantly, the second field of 262.5 lines had to fall midway between the lines of the first field if interlace scanning was to be maintained. The horizontal frequency cannot

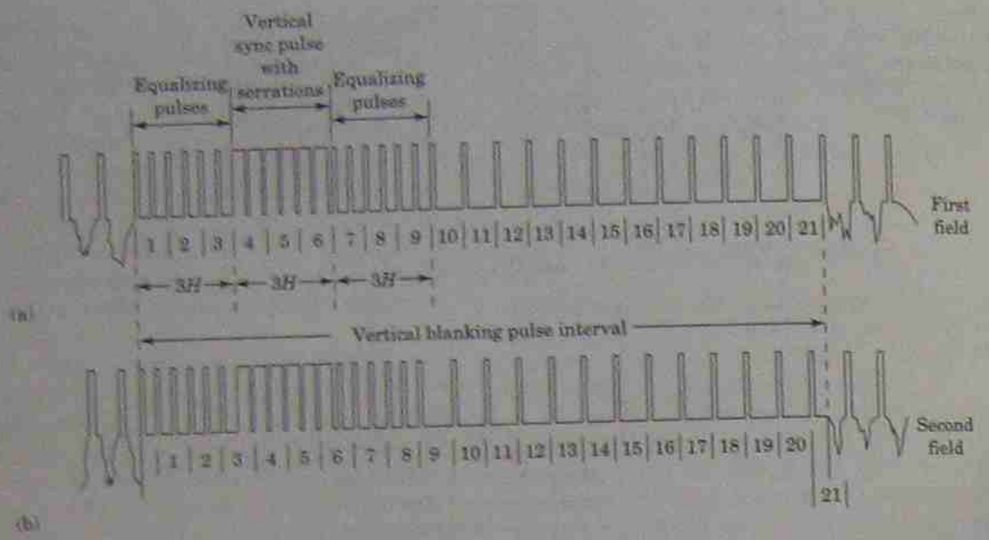


FIGURE 5.5
The vertical blanking and sync interval signal: (a) the first field; (b) second field. See text.

change, but the starting position of the sync pulse needed to be shifted by a half-cycle as compared to the previous field. The starting time change is achieved by running the horizontal time generator at double speed (31,500 Hz) for 18 cycles. These pulses are called **equalizing** pulses and occupy the first 18 positions along the vertical blanking level as horizontal sync pulses. After the equalizing pulses, the remaining 12 horizontal sync pulses on the vertical blanking back porch are standard-rate horizontal pulses, but shifted in time by ½H.

Note that the first six equalizing pulses in Figure 5.5a and b are identical for both fields. The vertical sync pulses with serrations (Section 5.7.2) are the same for both fields. However, there are seven equalizing pulses following the sync pulse in the first field, whereas there are only six equalizing pulses following the sync pulse in the second field. It is this alternating 6, 7, 6, 7 exchange of equalizing pulses that starts one field on a full-line trace and the next field on a midway half-line trace.

The first field is defined in the FCC regulations as having a full field of video between the first equalizing pulse and the preceding horizontal sync pulse. The line numbers start at the first equalizing pulse in the field and go to a full count of 21 lines.

The second field has a half-line of video between the first equalizing pulse and the preceding horizontal sync pulse. The line numbers in the second field start at the second equalizing pulse. Line 21 of the second field is then only one-half horizontal time under vertical blanking interval, which makes very interesting reading when closed captions are discussed.

5.7.2 Vertical Serrations

Figure 5.5 has six equalizing pulses that appear during the vertical sync time. Extending these pulses further in a positive direction would be meaningless and confusing. To avoid this condition, the horizontal sync pulses during the vertical sync time are inverted and appear as saw cuts into the vertical sync signal, called vertical **serrations.** The horizontal deflection oscillator at the receiver will trigger on the leading edge of the positive-going horizontal sync pulse. To maintain this timing integrity, the positive-going trailing edge of the serrated pulses is positioned to match the horizontal rate.

The color burst signal is not transmitted during the equalizing pulse period, but is present for all the regular horizontal sync pulses at the trailing end of the vertical blanking back porch. The color burst signals are not shown in Figure 5.5 in order to keep an already busy waveshape as clean as possible.

The first and second fields can be viewed on a dual-trace scope, set on alternate scan and triggered externally.

5.8 LINE PAIRING

In the preceding section, the second field of 262.5 horizontal scan lines should fall midway between the 262.5 horizontal scan lines of the first field. When the vertical hold control is not properly set, the horizontal equalizing pulses may not do all that they were intended to do. The second field may trigger at only 10% of the time between lines, instead of the 50% as desired. This will cause the horizontal lines to pair together. Line pairing, shown in Figure 5.6, causes a wider space between lines and in general degrades the quality of the picture. Only four line sets are shown paired in Figure 5.6 and the slope is exaggerated to emphasize the condition.

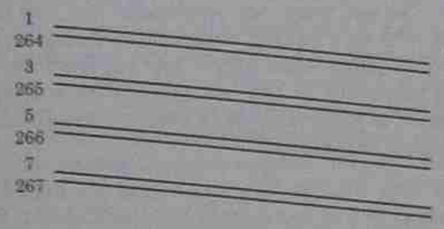


FIGURE 5.6
Horizontal scan lines showing line pairing. Only eight lines shown for simplicity.

5.9 IRE UNITS

The percent of peak video signal scale in Figure 5.3 was adopted as the NTSC industry standard for defining signal levels since the introduction of television. In many aspects of television transmission, they are the only reference levels in use today.

A second useful scale is measured in IRE units. The Institute of Radio Engineers (IRE), now known as the Institute of Electronic and Electrical Engineers (IEEE), has developed a scale using the inverted video signal (positive picture phase). This scale is seen in Figure 5.7, along with the percent scale, using the NTSC color bar pattern as a sample signal. This color bar pattern is not intended to have meaning at this time, although you will see it several times before it is explained in detail in Chapter 8. It is used here only to show a wide variety of standard signal levels in a single waveshape.

Your attention at this time is focused on the comparison between the NTSC percent scale and the corresponding IRE unit scale. You will see both scales used in technical literature, as in this text, but not necessarily together.

The prime levels in the IRE unit scale are as follows: (1) The zero reference level is the blanking pedestal, (2) the white reference level is assigned at +100 IRE units, and (3) the peak sync pulse is at −40 IRE units.

In a step-by-step evaluation, you should be able to identify, on either scale (1) the NTSC zero signal level at 0%. The IRE unit scale does not

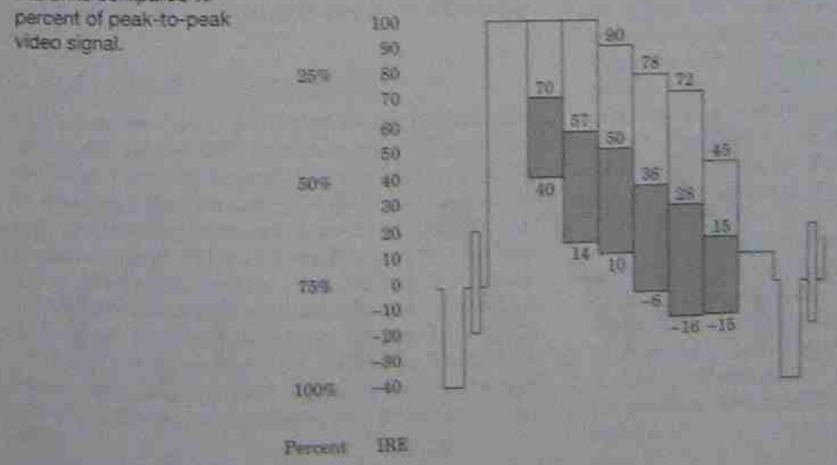


FIGURE 5.7
IRE units compared to percent of peak-to-peak video signal.

specify a zero signal level, but if it did, zero signal would be at +120 IRE units. (2) The NTSC white reference level is at 12.5% or +100 IRE units. (3) The NTSC black reference level is at 70% and is called the **set up** level on the IRE unit scale at +8 IRE units. (4) The blanking pedestal at 75% on the NTSC scale corresponds to the reference level on the IRE scale at 0 IRE units. (5) The sync pulse peaks at 100% on the NTSC scale are at −40 IRE units. (6) The color burst signal on the back porch of the horizontal blanking pulse ranges from 62.5% to 87.5% on the NTSC scale and from +20 to −20 IRE units on the IRE scale. The transition from one scale to the other is easy when you remember that a 1% change in the NTSC signal is equal to 1.6 IRE units.

5.10 VERTICAL INTERVAL TEST SIGNALS (VITS)

The back porch of the vertical blanking signal is put to more efficient use by adding a family of signals on lines 17 through 21 and may be slightly different on the first or second field. Figure 5.8 shows the individual test signals, which are explained in the following paragraphs. The test signals require special test equipment and are primarily used by the engineering staff. However, the better technicians should know *what* these signals are, *where* they are found, and *how* they are used.

5.10.1 Multiburst

The multiburst signal is transmitted on line 17 of the first field as a frequency response test of the signal after many stages of amplification, several modulation steps, and through demodulation at the receiver. It starts with an 8-μs level set at 100 IRE and then drops to the 40-unit level where 6 bursts of sine-wave signals are added. Each sine-wave signal is on for 6 μs, separated by 1-μs spaces (except the trailing space of 2 μs), for a total of 52 μs. The test frequencies are 0.5, 1.5, 2.0, 3.0, 3.58, and 4.2 MHz. The test frequency amplitudes are ±30 units (from +10 to +70 IRE units). Good frequency response is noted when all six test signals have the same amplitude at the test point. Poor frequency response is recognized by a reduced amplitude at the higher frequencies.

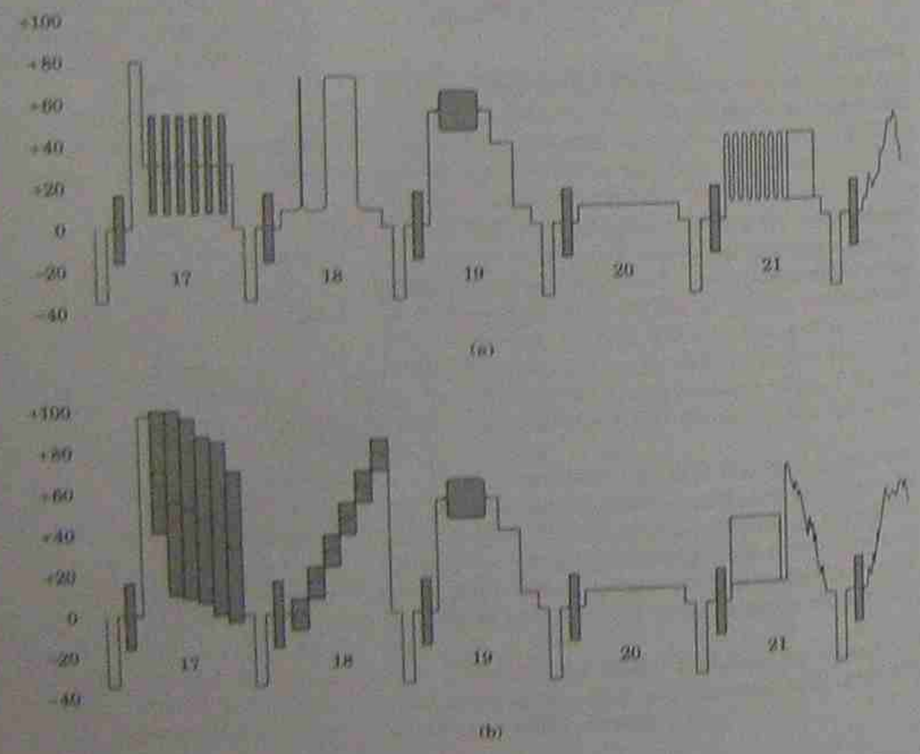


FIGURE 5.8
Vertical interval test signal (VITS): (a) first field, (b) second field. See text.

5.10.2 Sine Squared

Line 18 of the first field is sent only once in every eight fields. A sine wave with positive and negative peaks will have only positive values when the sines of the angles are squared (negative times a negative is positive). It will also double in frequency. This is the spike of signal seen in Figure 5.8a, line 18. It is used to measure phase distortion. The second pulse on line 18 of the first field is a window signal used to measure overshoot and ringing in amplifier circuits. Line 18 is separated from all other signals, put into memory, and repeated for the full screen display. The screen is dark for the first half of the trace, then white for one-fourth of the display, and then black again. Amplifiers that ring show several cycles of damped oscillation, which appear as darkened lines in the window.

5.10.3 Vertical Interval Reference (VIR)

This line is used at the receiver when automatic color alignment and automatic brightness circuits are part of the design of the receiver. The signal rises to +70 units, where a 24-μs run of 3.58-MHz subcarrier at zero phase reference signal can be used for automatic color control. The subcarrier amplitude changes from +50 to +90 IRE units (±20 units). The level then drops to +50 units for 12 μs and then to the black reference level for another 12 μs. The difference between these last two levels is used to automatically compensate the brightness level for the most effective viewing.

Line 20 of the first field is reserved for station use when the channel number, time of day, or other data may be transmitted. It is set up for 48 bits on line 20 for about 1440 bits per second (bps). The end user can use this signal only *if* it is transmitted.

5.10.4 Closed Captioning (Q)

The program dialog, converted to the printed word for display on the CRT screen, is called **closed captioning.** Program listings use the letters Q or CC to designate this feature. It is intended for persons who are hearing impaired. Line 21 of the first field contains seven cycles of a clock signal at 503 kilohertz (kHz) to be used for synchronizing the demodulator carrier oscillator in the receiver. The second half of line 21 allows for a start bit, two 7-bit ASCII characters with parity, and a stop bit. This is the clock signal and the data signal. More will be said about closed captioning under line 21 of the second field.

5.10.5 Color Bar Pattern

Line 17 of the second field is the same color bar pattern as seen in Figure 5.7, where more detail can be noted. Also see Chapter 8.

5.10.6 Stairstep

The stairstep pattern on line 18 of the second field can have any number of steps up to 10. Figure 5.8 shows six levels with a rise per step of 20 IRE units. On each of the steps is a burst of 3.58-MHz color subcarrier signal at zero phase that extends ±10 IRE units above and below the step level. This signal is used for amplitude distortion evaluation over the range from full white to full black at two frequencies, 115 kilohertz (kHz) of the step voltage and at 3.58 MHz of the subcarrier voltage.

The stairstep signal is gated out and fed through a low-pass filter to remove the 3.58-MHz modulation. Each step can then be checked to see if it has a rise of 20 units at maximum white and again at the zero signal level. The low-pass filter is replaced with a high-pass filter so that the steps are removed from the signal, but the six segments of 3.58-MHz carrier signal are passed. When all six segments are the same amplitude, the linearities at full white and at full black are equal.

Line 19 of the second field is exactly like line 19 of the first field and needs no further explanation. Line 20 of the second field is unassigned at this time.

5.10.7 Closed Caption Framing Code

The first half of line 21 of the second field provides for 9 bits of a framing code. The framing code controls the closed caption decoder as to which lines of video are to be blanked out and the captioning inserted, when to open or close the caption circuits, and how long each message set is to remain on the screen. The 9-bit framing code on line 21 of the second field provides for 512 different commands that process the message data on line 21 of the first field.

The second half of line 21 in the second field is beyond the vertical blanking interval and contains video signal information. You can see that when the vertical blanking interval has less than the full 21 lines the closed caption data will be lost. It is the station's responsibility to ensure that line 21 is transmitted. The receiving end of the system has no control.

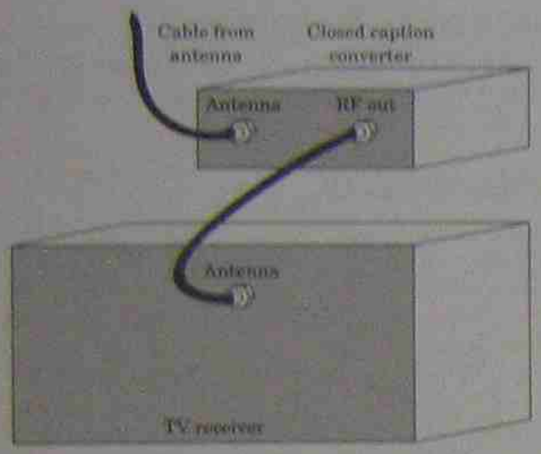


FIGURE 5.9
A closed caption converter as an external unit.

5.11 CLOSED CAPTION RECEPTION

Closed caption is not for all viewers; therefore, there must be a way to turn the captioning on or off at will. By todays methods* a converter similar to a cable television converter is used. You connect your antenna to the converter and feed the output from the converter to the antenna terminals of your television receiver, set to channel 3 or 4, and make all the station selections using the converter channel selector. See Figure 5.9.

The converter receives whatever channel you have selected and demodulates the video signal. The closed caption signal is gated out of line 21 of the vertical interval signal through a decoder and added into the picture information (in alphanumeric characters) on the lines designated by the instructions included in the framing code. The video is then modulated onto a channel 3 or 4 picture carrier signal and fed to the antenna terminals of your television receiver.

The FCC has ruled that all television receivers 13 inches and larger and manufactured or sold in the United States after June 1993 must include a built-in closed caption decoder system.

5.12 *Z*-AXIS MODULATION

The CRT works in exactly the same way as a bipolar transistor circuit. That is (for the bipolar), an input signal may be applied to the base terminal or to the emitter terminal for an output at the collector terminal. The base input signal gives you a 180° signal phase change at the output of the collector, a positive pulse base signal to a negative pulse collector signal. The emitter input signal results in a collector signal with no phase change, a positive pulse emitter input signal to a positive pulse collector output signal. To achieve a positive output pulse at the collector from either input requires a positive pulse input to the emitter or a negative pulse input into the base. The CRT has the same action with the control grid equivalent to the transistor base and the CRT cathode equivalent to the transistor emitter. Figure 5.10 shows the required input signals to the cathode and control grid of the CRT.

The voltage on the cathode must *always* be positive compared to the voltage on the control grid.

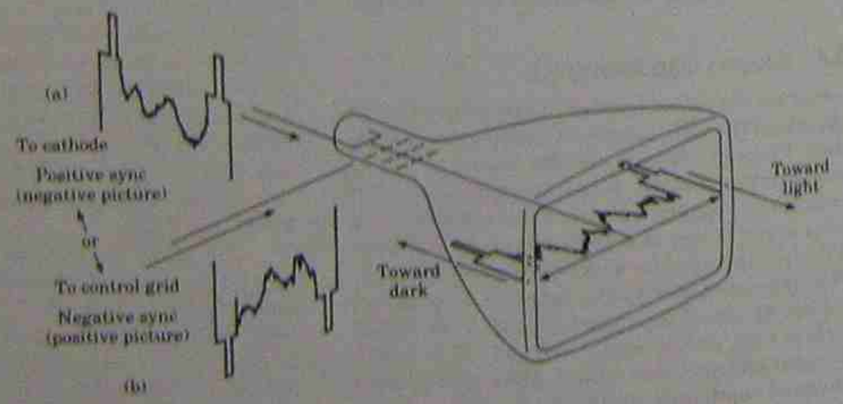


FIGURE 5.10
Effects of applying (a) a negative picture phase signal to the cathode and (b) a positive picture phase signal to the control grid of the CRT. (Reprinted by permission of Prentice-Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, p. 617, 2 ed., Robert J. Schoenbeck, © 1992.)

*Today's methods mean television receivers manufactured before June 1993.

A small difference in potential (cathode at +1 V dc, control grid at 0 V dc) will cause high cathode current and a very bright raster or picture display. A large difference in potential (cathode at +1 V dc, control grid at −60 V dc) will cause a low cathode current and a very dark or black raster or picture display.

Examine Figure 5.10 as you read these two paragraphs. Since we know that the blanking and sync pulses represent dark or black, then, from the previous statement, we can say that with the cathode at +1 V dc the blanking pulse of −60 V will turn the CRT off. A white reference level of 0 V and a blanking signal of −60 V describes a video input signal to the control grid. The control grid requires a positive picture phase input signal.

When the control grid is at 0 V dc and the cathode voltage is at +1 V dc, a +60-V blanking pulse applied to the cathode will also turn the CRT off. The cathode requires a negative picture phase input signal.

In the final analysis, the horizontal deflection moves the electron beam along the *X* axis (abscissa) and the vertical deflection moves the electron beam along the *Y* axis (ordinate); then the video signal changes the intensity (amount of current in the electron beam) of the CRT to increase or decrease the brightness in the *Z* direction. We then define *Z*-axis modulation as a change in cathode current in the CRT that is caused by the changing amplitude in the video signal voltage.

5.13 SCOPING THE VIDEO WAVE

When using the oscilloscope to measure, analyze, or troubleshoot the low-frequency circuits in a computer monitor or video product, it is helpful to know ahead of time what you are expected to see. You should be able to recognize a typical waveshape and measure its amplitude. Here are some pointers that will make it easy.

The first step is to realize that you need to be concerned only about two scope sweep settings. The horizontal rate with the scope sweep time at 10 μs/centimeter (cm) and a vertical rate with the scope sweep time set at 2 ms/cm. Occasionally, the third sweep setting at the color subcarrier frequency may also be useful.

The scope horizontal sweep rate at 10 μs/cm on a 10-graticule scope scale will give you 100 μs across the screen. This is 1.6 cycles of any of the horizontal signals, deflection or video. You will recognize the horizontal video signal by a clearly displayed horizontal blanking and sync pulse, with the color burst on the back porch of the blanking pedestal. The video signal may be changing on live program signals, but this will not change the blanking pulse signal. Figure 5.11 shows the horizontal video signal as a sample.

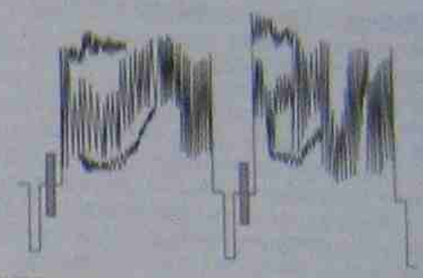


FIGURE 5.11
A live program video signal at the horizontal rate.

When the scope sweep setting is set to 2 ms/cm, the 10-graticule scale covers 20 ms of time and 1.2 full cycles of the vertical signal. You will always want to see at least one full cycle of the signal displayed on the scope in order to examine the start and end of the waveshape.

The vertical video signal in Figure 5.12 is best understood when you remember that there are 241 horizontal pulses between each vertical pulse. With the scope sweep set at 2 milliseconds (ms/cm, you will see one vertical blanking and sync pulse separated by 241 horizontal pulses. The horizontal blanking and sync levels during vertical sweep time look like lines drawn between the vertical blanking and sync pulses, and this gives a different appearance than the horizontal pulse alone. The amplitude change in the horizontal pulses are so fast at this scope setting that the brightness level is too

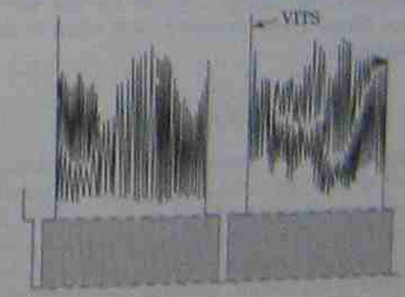


FIGURE 5.12
A live program video signal at the vertical rate.

low to be seen. The horizontal travel of the wave is slower and can be seen.

A special note to remind you that the vertical interval test signals are seen here also. In the VITS, there are several test signals that have a white reference signal. These appear as a single spike of voltage immediately at the trailing edge of the vertical blanking signal. They are only seen at the vertical rate and serve as an accurate measure of the peak-to-peak amplitude of the video signal regardless of the change in picture information.

5.14 LUMINANCE SIGNAL

Before color television, the video signal was just video. It was intended to mean the unmodulated picture information. After color was added, the black and white signal had to be defined more precisely. White is the sum of all colors, and black is the absence of all colors. If white is the only color, then the signal could be labeled the **monochrome** (one color) signal. The white portions of the signal contributed to the brightness of the picture, and the video signal soon became known as the **brightness** signal. The unit of measure for brightness is the **lumen,** so the brightness signal was referred to as the **luminance** signal. The scientific symbol for the lumen is the letter Y, so when the abbreviated form of the signal was needed, it was called the Y-signal.

This entire preceding paragraph is used to inform you that this one signal can be identified by five different names and all are correct.

1. Black and white video signal
2. Monochrome video signal
3. Brightness signal
4. Luminance signal
5. Y-signal

What is worse, all five names may be used in a single descriptive paragraph to mean the one signal. The last three names are used most often in current literature.

5.15 LINES OF RESOLUTION

Although there is a remote association with the number of scan lines, the phrase **lines of resolution** is more directly related to the highest frequency in the video signal. The tie to the scan lines comes from the vertical resolution. If the 482 active scan lines in the vertical direction were made alternately black and white, then you could resolve (or define) 241 black bars separated by 241 spaces from the top to the bottom of the CRT screen. See Figure 5.13a. With a 4 : 3 aspect ratio, we would expect 322 ($\frac{4}{3}$ by 241) alternate black and white vertical stripes when counting sideways across the face of the CRT as horizontal lines of resolution, as in Figure 5.13b.

It is not enough to just calculate 322 on–off (square-wave) cycles occurring in the 52-μs scan time of each line. The transition time from full black to full white will not be instantaneous. Imagine for the moment that the five circles in Figure 5.14 are not five separate electron beams moving across the screen, but rather the same beam in five different positions along the one scan line. At *a*, the beam is fully in the black region and the beam current is zero. At *e*, the beam is fully in the white region and the beam current is 100%. However, at *c*, the beam is half in the black and half in the white regions and the beam current is 50%. Then, from a correction factor of $\sqrt{2}$, we can calculate the number of lines of horizontal resolution compared to the frequency, as follows:

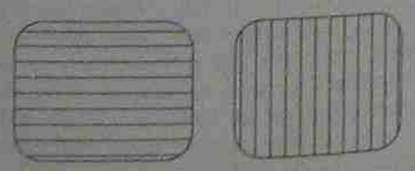
$$\text{lines of resolution} = ft\sqrt{2} \qquad (5.1)$$

where f = the highest video frequency
t = the trace time

But 322 lines of resolution across the CRT screen is not the best we can hope for, nor is it the ideal. It merely states the condition that we would have if the vertical and horizontal resolutions are within the 4 : 3 ratio. The CRT is capable of higher performance than this, and more lines of resolution mean a sharper, crisper picture. It affords faster rise times with cleaner edges.

In consumer electronic television, where the video frequency is limited by law to 4.2 MHz, the number of horizontal lines of resolution is 309 lines.

$$(\sqrt{2})(4.2\text{ MHz})(52\ \mu s) = 308.86 \text{ lines of horizontal resolution}$$



(a) Vertical resolution (b) Horizontal resolution

FIGURE 5.13
Lines of resolution: (a) in the vertical direction and (b) in the horizontal direction.

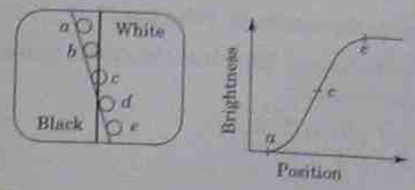


FIGURE 5.14
A single electron beam moving from a black to a white region.

Computer monitors are the only other systems that are compatible with consumer television because they both use the same vertical and horizontal scanning frequencies. However, because computers do not transmit RF signals outside a closed system, the video frequency is raised to 15-MHz bandwidth. This higher frequency is needed to accommodate 80-column word processing formats. The horizontal lines of resolution for monitors are ($\sqrt{2}$)(15 MHz)(52 μs) equals 1103 lines of horizontal resolution.

QUESTIONS

5.1 Into what region is the sync pulse driven?
- **(a)** white,
- **(b)** black,
- **(c)** gray,
- **(d)** blacker than black

5.2 The composite video signal is the
- **(a)** horizontal blanking,
- **(b)** horizontal sync,
- **(c)** vertical blanking,
- **(d)** vertical sync,
- **(e)** video signal, or
- **(f)** all of the above.

5.3 The color burst signal is
- **(a)** a burst of red color,
- **(b)** the color sync signal,
- **(c)** the full color signal,
- **(d)** the composite video signal,
- **(e)** the color subcarrier.

5.4 List the percent of video signal for
- **(a)** the blanking pulse,
- **(b)** no signal,
- **(c)** sync peak,
- **(d)** reference white,
- **(e)** reference black.



(a) (b)

FIGURE 5.15

5.5 Which of the sketches in Figure 5.15 best represents positive picture phase?

5.6 Where is the color burst signal found in the composite video signal?

5.7 Define the term *breezeway* as used in the composite video signal.

5.8 During the front porch time of the horizontal blanking, the scanning beam is at the
(a) left edge of the screen,
(b) center of the screen,
(c) right edge of the screen,
(d) top of the screen,
(e) bottom of the screen.

5.9 How many microseconds long is the horizontal blanking pulse?
(a) 190.5 μs,
(b) 11.5 μs,
(c) 5 μs,
(d) 8 cycles,
(e) 63.5 μs

5.10 The horizontal deflection oscillator at the receiver triggers on which edge of the horizontal sync pulse?
(a) leading edge,
(b) trailing edge,
(c) neither,
(d) both

5.11 Identify the following levels in terms of IRE units.
(a) blanking level,
(b) no signal,
(c) sync peak,
(d) white reference level,
(e) black reference level

5.12 A 57.5% signal level corresponds to what IRE unit level?

5.13 Forty IRE units corresponds to what percent signal change?

5.14 The vertical blanking time is what percent of the total vertical sweep time?

5.15 How many horizontal lines occur during one vertical blanking period?

5.16 How wide is the vertical sync pulse measured in horizontal time periods?

5.17 How many equalizing pulses are there in each field, including the vertical serrations?

5.18 What is the purpose for the equalizing pulses?

5.19 Define the acronym VITS.

5.20 On what line and in which field is the multiburst found?

5.21 What is the multiburst used for?

5.22 On what line and in which field is the vertical interval reference signal found?

5.23 What can the VIR signal be used for?

5.24 On what line and in which field is the stairstep signal found?

5.25 What two conditions is the stairstep signal used to measure?

5.26 Where is the control signal found for the closed caption?

5.27 How many data bits can be placed in the closed caption control signal?

5.28 Where is the data information found that is to be transmitted for closed caption readout?

5.29 Describe how the data for closed caption are formatted in the data information field, including start bits, number of data bits (and the code used), and stop bits.

5.30 Name three differences between the vertical rate video signal and the horizontal rate video signal.

5.31 What video rate signal (vertical or horizontal) is best to use when measuring peak-to-peak video amplitude?

5.32 Explain how you selected your answer to Question 5.31.

6 Video Amplifiers

6.1 INTRODUCTION

Video amplifiers are, in general, wide band amplifiers that process the unmodulated video signal. This could include camera video amplifiers, video cassette recorder (VCR), video amplifiers, monochrome receiver video amplifiers, color receiver video amplifiers or computer monitor video amplifiers. They all have similar, if not identical characteristics. Fortunately, all video amplifiers can be examined with a signal generator and oscilloscope found at every electronic work station.

6.2 BASIC BLOCK DIAGRAM

The layout of Figure 6.1 is the block diagram of a video system in a monochrome television receiver; it will be used as an introduction to this area of study. Many features can be highlighted in this basic system diagram.

The video signal may be applied to the cathode or the control grid of the CRT. A negative picture phase signal is required for the cathode input, while a positive picture phase signal is used when the control grid is the input terminal to the CRT. The choice of cathode or control grid input to the CRT is in the hands of the circuit designer. Either input produces the same results, although the cathode input is most common.

Notice that the brightness control is part of the CRT bias circuit and sets the dc voltage level between the cathode and the control grid for a steady dc current through the CRT and fixed brightness level.

The number of amplifiers in the system varies from two to six and depends on the specified input signal level, the required output signal level, and the gain per stage that can be achieved. There could also be clippers, clampers, and blanking stages that, in this network, would all be considered video amplifiers. The polarity of the input signal could also influence the number and type of amplifiers used in the circuit, although the input signal level and polarity are generally known factors.

In computer monitors, the sound signal is often a separate input terminal from the video input terminal and, therefore, the treatment of the sound signal will be omitted here for monitors.

In television receivers (monochrome), the sound signal and the video signal all arrive at the same input terminal. It is beneficial to separate the sound from the video as early as possible in the amplifier. The sound signal is on a frequency-modulated carrier at this point and is easily separated with a tuned circuit. The signal for the automatic gain control (AGC) is the video signal taken from the input terminal, which will be covered later in the text. The color signal (when used) is also separated from the video signal as soon as possible in this circuit. The video signal is fed in parallel to the video amplifiers, the AGC circuits, the color circuits, and the synchronizing circuits. The separation point for the sync signal depends on the polarity of the signal and the polarity of the synchronizing circuit.

The important point to be emphasized here is that the separation of all the signals that arrive together *must* take place before the contrast control.

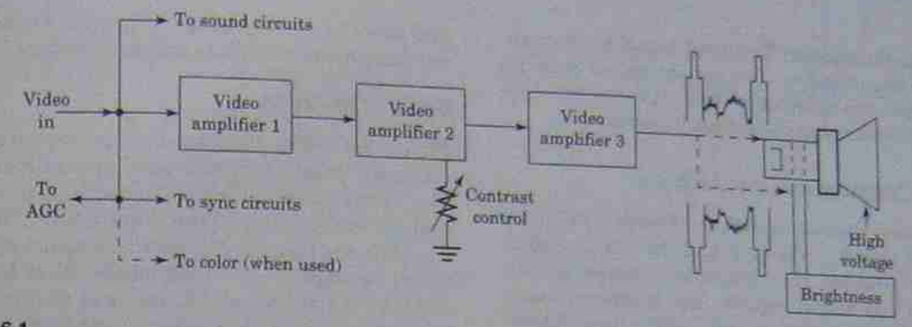


FIGURE 6.1
Introductory block diagram of the video amplifier section in a television receiver.

You do not want the sound or sync signals to change levels when the contrast control is adjusted. The contrast control changes the signal level to the CRT, which affects the black to white ratio.

6.3 SIGNAL LEVELS

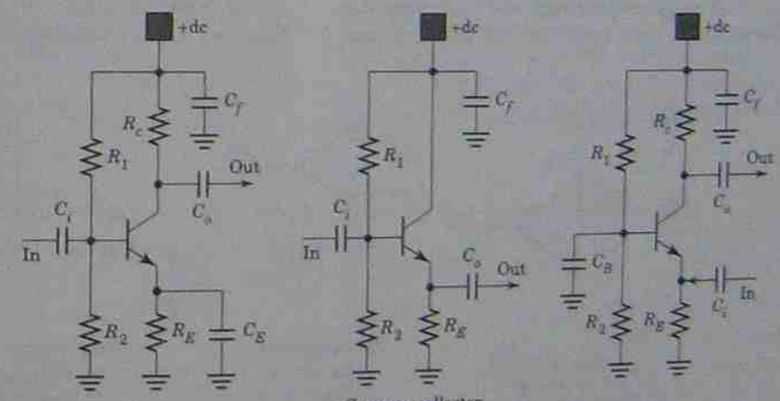
It would be rare to find an input signal of less than 1 volt peak-to-peak ($V_{p\text{-}p}$) and generally not greater than 6 $V_{p\text{-}p}$. The signal required to drive the CRT is at least 40 $V_{p\text{-}p}$ and rarely exceeds 100 $V_{p\text{-}p}$. This means that the overall gain could be 7 for the lowest case or 100 for the worst case. A good typical gain figure for the average video amplifier section is between 15 and 50.

For computer monitors, the input signal level is almost universally 1 $V_{p\text{-}p}$ with negative sync pulses (positive picture phase) polarity. Television receiver video amplifiers generally have a larger input signal level, averaging about 4 $V_{p\text{-}p}$ and most commonly with negative sync pulses (positive picture phase) polarity. The video input signal for television is not a standard value or polarity.

6.4 AMPLIFIER REVIEW

A quick refresher in basic amplifiers here will save considerable time in future discussions. Figure 6.2 shows the three basic configurations for transistor amplifiers. The input signal may be applied to the

FIGURE 6.2
Characteristics of transistor circuits.



base or to the emitter. The input signal is *never* applied to the collector. The output signal may be taken from the collector or from the emitter. The base is never used as the output terminal.

6.4.1 Common-emitter Amplifier

The common-emitter amplifier of Figure 6.2a shows the input signal to the base and the output signal from the collector; the emitter is common to both the input and output signals. The common-emitter amplifier has the highest gain, 180° phase change from input to output, and has medium input impedance and medium output impedance.

6.4.2 Common-collector Amplifier

The common-collector amplifier of Figure 6.2b has a base input signal and an emitter output signal. The collector is common to both the input and output signals (through the ac ground connection of C_f). The gain is less than 1, with no phase change in signal polarity. It has the highest input impedance and the lowest output impedance. The prime function of the emitter follower is as an impedance-matching amplifier.

6.4.3 Common-base Amplifier

The input to the common-base amplifier in Figure 6.2c is the emitter with the output at the collector. The base is common to both the input and output signals, with ac ground through the base capacitor C_b. The common-base amplifier has medium gain and no signal phase change. It has the lowest input impedance and a medium output impedance.

6.4.4 Op-amps

Figure 6.3 shows the common op-amp circuits as compared to the transistor amplifiers of Figure 6.2. The inverting amplifier of Figure 6.3a is like the common-emitter amplifier of Figure 6.2a. The input impedance is equal to R_1 and the output impedance for all op-amps is low at 500 ohms (Ω) or less. Figure 6.3b is the voltage follower and is equal in all respects to the common-collector amplifier of Figure 6.2b. The noninverting amplifier of Figure 6.3c and the common-base amplifier of Figure 6.2c are the same except for the input and output impedances.

Appendix C has information on transistor biasing techniques, amplifier class of operation, and coupling methods if more extensive review would be helpful at this time.

6.5 GAIN VERSUS FREQUENCY

All amplifiers have a characteristic called the **gain–bandwidth product.** The numerical value of the product is only important to each individual device and has no carry-over significance from one device to another. The statement simply says that the gain of a particular device in an uncompensated circuit cannot have a gain change without also affecting the circuit bandwidth. When the gain increases, the bandwidth shrinks.

Figure 6.4 is the curve for an LF356 op-amp that has a gain–bandwidth product of 3 million.

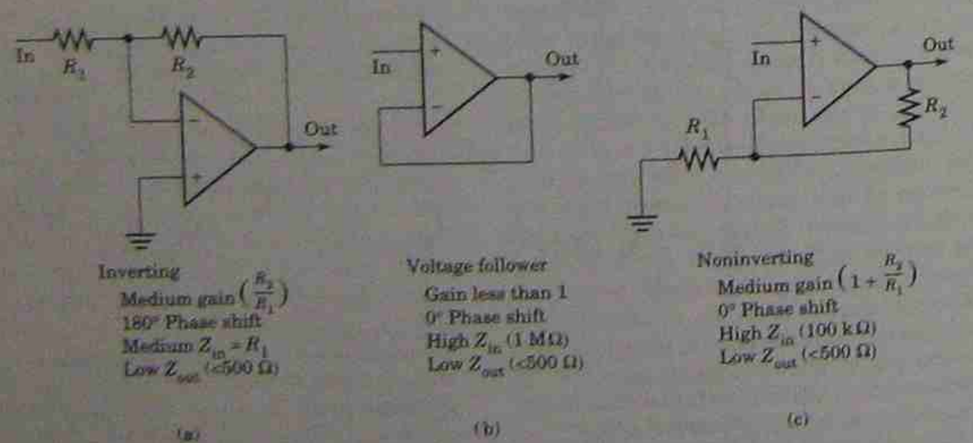
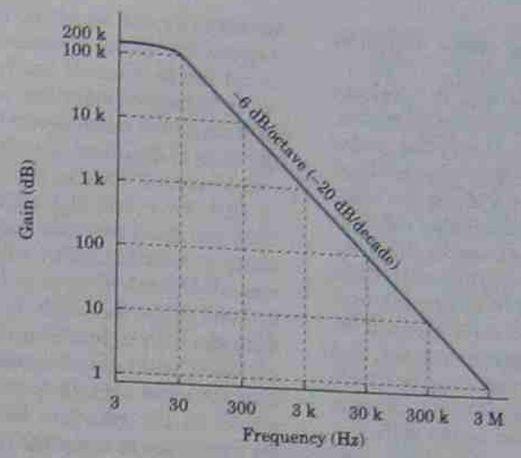


FIGURE 6.3
Characteristics of common op-amp circuits.

FIGURE 6.4
LF356 op-amp gain versus frequency response.



The open-loop gain is 200,000. A gain of 1 has a bandwidth of 3 megahertz (MHz). A gain of 10 will have a bandwidth of 300 kilohertz (kHz), a gain of 100 has a bandwidth of 30 kHz, and so on up the scale. The gain will be 200,000 for frequencies of 15 Hz or less.

The slope of the curve changes at a rate of 6 decibels (dB) per octave. An octave is a frequency change by a factor of 2. One octave up from 100 Hz is 200 Hz. Another octave up is 400 Hz. One octave down from 1200 Hz is 600 Hz. Divide or multiply the frequency by 2 to change one octave.

A decade is a frequency change by a factor of 10. One decade up from 100 Hz is 1000 Hz. One decade down from 5000 Hz is 500 Hz. Another decade down is 50 Hz. There are three and one-third octaves to a decade: $3\frac{1}{3}$ octaves × 6 dB per octave = 20 dB per decade. Therefore, 6 dB per octave is the same as 20 dB per decade. Divide or multiply the frequency by 10 to change one decade.

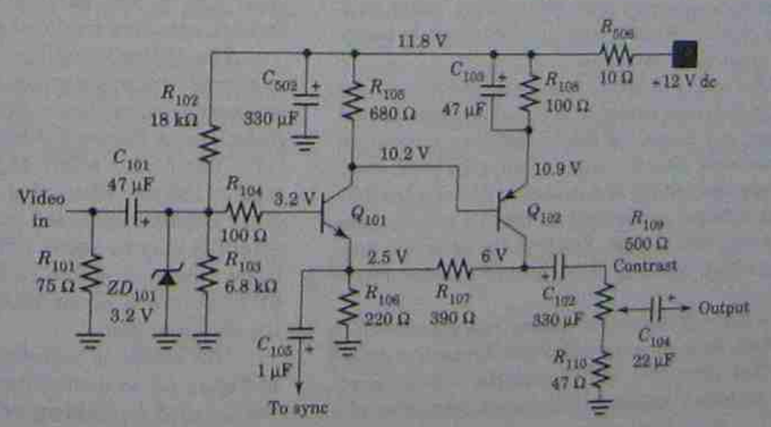
In the video amplifier section, we need a bandwidth of 4.2 MHz, so it is reasonable to say that the gain per stage will be small.

6.6 VIDEO AMPLIFIER CIRCUITS

The low signal half of a monochrome monitor video amplifier is shown in Figure 6.5. The input signal is 1 $V_{p\text{-}p}$ with positive picture phase. The voltages marked on the schematic at the base, emitter, and collector of the transistors are dc operating voltages measured from ground with no input signal.

All video amplifiers are linear (nondistorting) class A or class B push–pull amplifiers. The input

FIGURE 6.5
Low-level video amplifier circuit (monitor).



impedance is 75 Ω and therefore uses a coaxial or shielded input cable.

From Figure 6.5, transistor Q_{101} is a voltage divider biased, class A, common-emitter amplifier. This is your first analysis step. Verify the statements as follows: (1) R_{101} and R_{103} are the base voltage divider to provide 3.2354 V dc at the base. The zener diode, ZD_{101} (3.2 V) overrides the bias circuit to clamp the base of Q_{101} at exactly 3.2 V dc. The diode's second function is to clip any part of the input signal that exceeds +3.2 V to protect Q_{101} from being overdriven. (2) The base is forward biased by 0.7 V compared to the emitter voltage, and the dc base voltage exceeds the peak-to-peak anticipated input signal level (class A). (3) The signal is applied to the base and taken out at the collector, leaving the emitter as the common element. A positive picture phase input signal yields a negative picture phase output signal.

The calculated gain of Q_{101} is approximately R_c divided by R_e, or roughly 3. But there is a negative feedback signal from the collector of Q_{102} back through R_{106} and R_{107} to the emitter of Q_{101}. Hold that thought.

Transistor Q_{102} is a voltage divider biased, class A, common-emitter (PNP type) amplifier. R_{105}, transistor Q_{101}, and R_{106} form the voltage divider that provides the bias voltage to the directly coupled base of Q_{102}. The calculated gain of Q_{102} is R_c ($R_{106} + R_{107} \parallel R_{109} + R_{110}$) divided by R_e (R_{108}) equal to about 2.88. The total gain should then be 3 × 2.88 = 8.64, but because of the feedback voltage the gain is reduced to about 3 for the entire circuit. The gain is reduced, the bandwidth is expanded, and the output voltage is about 3 $V_{p\text{-}p}$.

It will be helpful to recall the basics about volume controls versus gain controls at this time. The contrast control would serve the system better as a volume control where minimum distortion is introduced into the video signal.

After using a signal generator and an oscilloscope to isolate a defect to this circuit, you should measure and record all six dc voltages marked on the schematic plus the supply voltage. Never measure only one voltage and expect to find the trouble. The dc voltages are related so that as one changes others may also change. You find the defect by analyzing which voltages changed and in what direction.

A directly coupled amplifier like Figure 6.5 is the most difficult to troubleshoot because a defect in either transistor will change the voltage readings on both transistors. The input transistor of a directly coupled amplifier set is the easiest to test separately. If the transistor tests bad, you have found the problem. If the transistor tests good, the other transistor amplifier must be bad. Testing the first amplifier takes several steps. First, disconnect the base of Q_{102} from the circuit. Next, find out how much current flows in the collector of Q_{101}: (11.8 V − 10.2 V) ÷ 680 Ω = 2.354 milliamperes (mA). Next you must replace emitter resistor (R_{108}) with a value of resistance that will develop 2.5 V across it when 2.354 mA of current flows through it. $E/I = R$ or 1062 Ω. In this case, use 1000 Ω. This may reduce the gain to less than 1, but it will verify if the amplifier will pass a signal to the collector output. You then use straightforward resistance measurements on the resistors and capacitor substitution for capacitors to complete the testing of this circuit.

6.6.1 Video Output Amplifiers

The input network of Figure 6.6 (contrast control) is the output circuit of Figure 6.5 at 3 $V_{p\text{-}p}$ signal level and positive picture phase. The video output amplifier must raise the signal level to 100 $V_{p\text{-}p}$ (in this case) with a frequency response of 4.2 MHz, which is quite a job for a single amplifier. Several obstacles must be overcome.

The shunt capacities in any circuit are the sum of all the individual capacitances added together and placed in parallel from the signal path to ground. In effect, they reduce the gain at the higher frequencies. Separately, these are known as the *Miller effect* capacity, the interelectrode capacities, and the stray wiring capacities. The interelectrode capacities are held low by the selection of the amplifier transistor (or device). The stray capacitances are minimized by keeping the wire lengths short and by best parts placement and lead dress through educated trial and error methods.

The Miller effect capacity appears from base to ground and has a value of the *gain times the interelectrode capacitance from base to collector*. The transistor of Figure 6.6 has a C_{b-c} of 3 picofarads (pF). The Miller effect capacitance is then 33 × 3 pF = 100 pF. When this value is added to all the other capacitances, the input capacitance of the amplifier may be about 120 pF. At 4.2 MHz, 120 pF has a reactance of 315 Ω. Below 500 kHz, the 120-pF reactance is about 2500 Ω and does not reduce the amplifier gain.

The effects of high-frequency rolloff are shown in Figure 6.7 as a solid line. The compensation network, called a **peaking coil,** appears in Figure 6.6

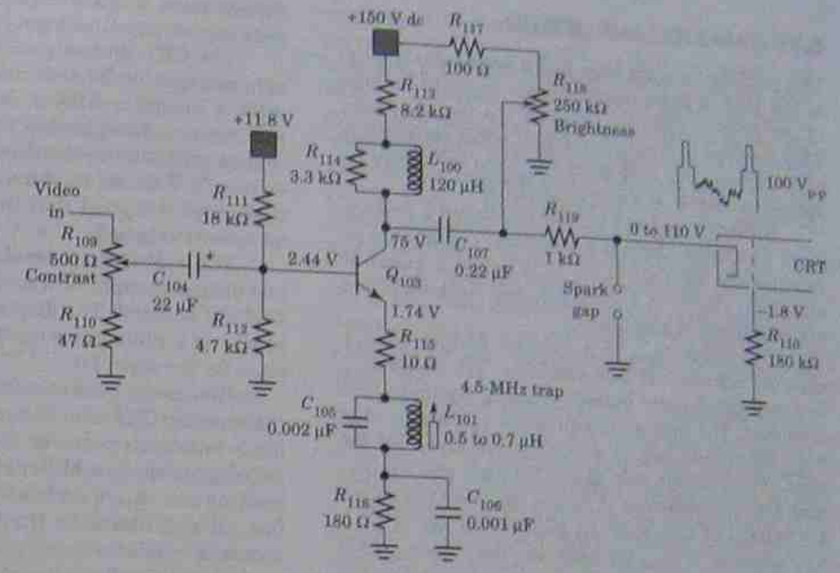


FIGURE 6.6
Monochrome television video output amplifier.

as L_{100} in parallel with R_{114} (3.3 kΩ). At a low frequency of 500 kHz, X_L = 375 Ω. The parallel impedance of R_{114} and L_{100} = 336 Ω. The gain of Q_{103} at 500 kHz is R_c (8.2 kΩ + 336) ÷ ($R_{115} \times R_{110}$) = 45. At high frequencies (4.2 MHz), X_L = 3165 Ω. The parallel combination of R_{114} and L_{100} is now 1620 Ω. The gain at 4.2 MHz is R_c (8.2 kΩ + 1620) ÷ 190 = about 51. The increase in amplifier gain at high frequencies is identified in Figure 6.7 by the dotted line. The net result of the compensation is shown in Figure 6.7 as a dashed line or flat frequency response. The peaking coil uses the resister (3.3 kΩ) as a coil form and is easy to test. Measure the dc resistance of the combination to be about 10 to 20 Ω as the resistance of the coil. If the coil opens, you will measure the resistor value.

The low frequency end of the response curve is affected by any reactance in series with the signal, coupling capacitors in most cases. At a frequency where X_c of the coupling capacitor is equal to the input impedance of the base, the low-frequency response will be down by 3 dB (−3 dB).

Coupling capacitors used with the low input impedance of transistor amplifiers need to be very large in value. In Figure 6.6, C_{104} is 22 microfarads (µF). The output coupling capacitor is smaller because it works with about 250-kΩ input impedance of the CRT. C = 250 kΩ at 30 Hz is about 0.02 µF.

Emitter bypass capacitors also affect the low-frequency response of the amplifier and should have a reactance of 0.1R_e at the lowest frequency to be amplified.

The 4.5-MHz trap (L_{101}) is a high Q notch filter to remove any sound carrier that may have arrived at this point. The impedance of the parallel tuned circuit at resonance is L/RC (R of the coil) and is (0.6 microhenry (µH)/0.5 × 0.002 µF), or about 600 Ω. Raising the emitter resistance lowers the gain, and the 4.5-MHz sound carrier is trapped out.

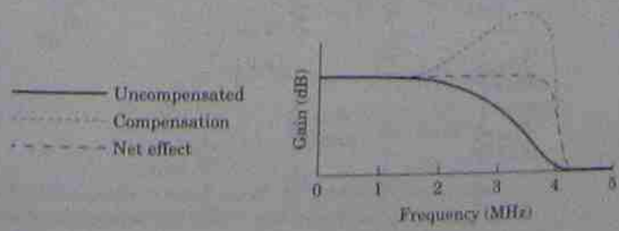


FIGURE 6.7
Effects of peaking coil compensation on frequency reference.

6.7 CASCODE AMPLIFIERS

The pentode vacuum tube had a particular quality of low grid to plate interelectrode capacity because of the greater distance between the two elements. This resulted in a very low Miller effect capacitance and allowed both high gain and wide frequency response to coexist in a single amplifier.

Although we have not yet developed a five-element transistor, there is a transistor circuit that resembles the pentode tube. It is called a **cascode** amplifier, shown in Figure 6.8, and consists of two series-connected amplifiers.

Transistor Q_{103} is a voltage divider biased, class A, common-emitter amplifier. Transistor Q_{104} is a voltage divider biased, class A, common-base amplifier. The bias arrangement is selected so that both amplifiers are in a conductive state all the time. The current that flows through the transistors, like two resistors in series, develops the collector voltage of Q_{103} and the emitter voltage of Q_{104}. The collector of Q_{103} behaves like the screen grid of the pentode, and the base of Q_{103} behaves like the control grid of the pentode, and the base of Q_{104} (at ac ground through C_{109}) acts like the suppressor grid of the pentode. The collector of Q_{104}, then, is the anode connection with a much larger dc voltage supply requirement. Remember that the peak-to-peak output signal voltage of a class A amplifier cannot exceed the dc supply voltage. So the supply voltage must be greater than the required peak-to-peak output signal voltage.

The CRT control grid is connected to a variable voltage-divider network connected between a +100 V dc and a −100 V dc supply. Depending on where the subbrightness control is set, the CRT control grid can be varied over the range of +37 V dc to −70 V dc. As a computer monitor, the brightness is set at a point that turns the raster off when no data are applied.

The video signal level of 40 $V_{p\text{-}p}$ needs to be just strong enough for the white peaks to bring the CRT out of cutoff. The display for monitors is represented as a white pulse for the digital 1 and a cutoff state for the digital 0.

Because of the low video signal requirement of the monitor CRT, the gain need not be as large as for a television receiver video amplifier. The reduced gain, the low Miller effect input capacity, the peaking coil (L_{102}), and the use of a cascode amplifier all contribute to the 15-MHz frequency response of monitors.

The horizontal lines of resolution for monitors are about 1100 lines as compared to the 320 lines for consumer television.

SP_{101} in both Figures 6.6 and 6.8 is a spark gap device that protects the CRT from large static electricity buildup and discharge. It is two wires placed close together, end to end, and encased in a glass bead. The separation between the wires determines the voltage buildup needed to arc across the gap and discharge the static electricity.

The only precaution needed to troubleshoot a cascoded amplifier is to remember that if either amplifier fails both amplifiers will stop conducting. Either amplifier can be tested separately by replacing the other amplifier with its equivalent resistance value. Collector current I_c is about 15 mA; therefore, Q_{104} with 49.7 volts dropped across it looks like a 3300-Ω resistor, and Q_{103} with 2.76 volts dropped across it looks like a 180-Ω resistor.

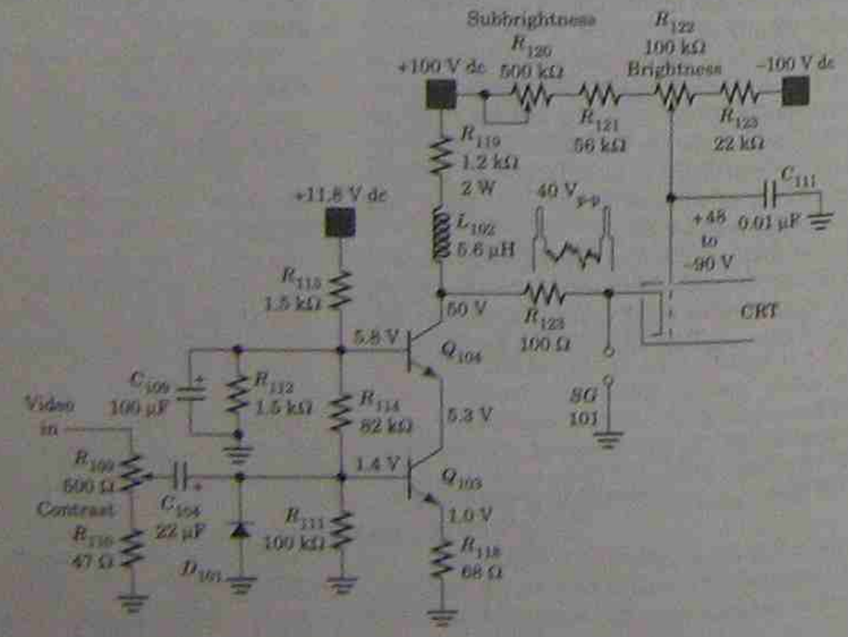


FIGURE 6.8
Cascade video output amplifier for a monochrome computer monitor.

6.8 DC RESTORATION

The video signal at the camera has both an ac component and a dc component. As the signal is assembled, the sync pulse peaks are clamped to a reference voltage, usually zero volts (or ground). This is the condition set up in Figure 6.9a, b, and c. The blanking pulses all reach an established level and the electronic picture image expands in a positive direction from there toward white. The very brightest scene will have the highest positive voltage level. The very same voltage levels are shown again unclamped in Figure 6.9d, e, and f. Drawing 6.9a corresponds to 6.9d at 3 $V_{p\text{-}p}$, 6.9b corresponds to 6.9e at 4.5 $V_{p\text{-}p}$ and drawing 6.9c and 6.9f are both at 6 $V_{p\text{-}p}$. However, an unclamped signal (ac only in d, e, f) will center around the average voltage in the wave (assumed to be zero in this example) and will have both a positive and a negative peak voltage swing. This is what happens when the signal is passed through a series coupling capacitor. The ac signal is unchanged, but the dc reference is lost.

It can then be seen that although the signals are of the same amplitude in the three cases, the clamped signals will present a brighter picture when the dc level is restored then the unclamped signal will.

If this condition were not established as the signal reaches the CRT, the white levels would not be as bright as they were originally and the low-level gray parts of the weaker picture would all be in the black region. The scene is dimmer and the contrast is compressed. For the true integrity of the picture to be restored, the dc component needs to be reestablished.

In ac-coupled amplifiers (those with coupling capacitors), the dc restoration takes place at the

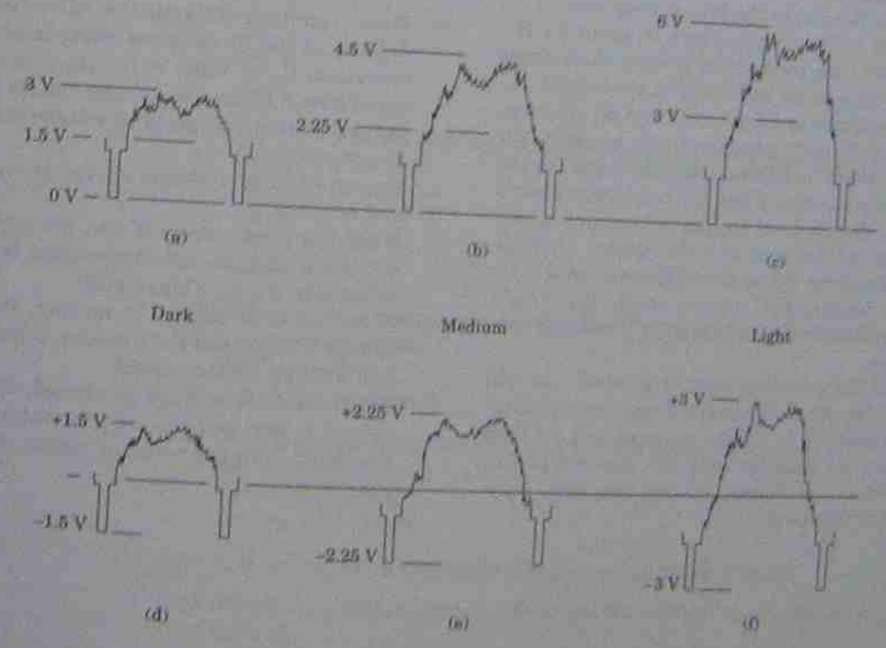


FIGURE 6.9
Dc restoration: a, b, and c identify three levels of video signal clamped to ground (zero volts). Parts d, e, and f are the same signal strength shown with no clamping.

output of the last video amplifier as the signal is applied to the CRT.

In direct-coupled amplifiers, those with no coupling capacitor, the dc restoration may take place at a low signal level and be maintained through each of the direct-coupled amplifiers that follow before the CRT. A dc restorer circuit is usually a diode that clamps the sync pulse peaks to some dc level. The level of dc is not the important issue. What does matter is that, once again, the sync pulse peaks be all aligned on the same dc level.

In Figure 6.8, diode D_{101} is the clamping diode that holds the negative peak input sync pulses to the reference voltage level that will carry through to the CRT. In the base of Q_{103}, the coupling capacitor C_{104} and the input impedance of the base form the RC time constant that charges C_{104}. On the negative input signal peak, diode D_{101} conducts to charge C_{104} to the peak voltage. In the positive direction, C_{104} discharges through the base input impedance of Q_{103}. In Figure 6.8, the input impedance of Q_{103} is about 6 kΩ, therefore, the RC time is 22 μF × 6 kΩ = 0.127 second. This translates to about 8 Hz as the low frequency that the diode circuit will clamp. The only concern is that the clamping action be faithful to the lowest frequency of interest in the video circuit, which is about 30 Hz. So, if the RC time constant is greater than about 0.033 s, the dc restorer will function as planned.

In an attempt to reduce costs, not all video circuits have a dc restoring circuit. As a result, the brightness control is adjusted to compensate for the loss in picture quality. When the brightness control is set high, the low-level signals do not turn off the CRT during retrace time and the retrace lines appear in the picture. When the brightness level is reduced, to remove the retrace lines, the bright scenes lose detail. The net result is a reduced contrast range.

When the restoring diode is shorted, you will lose the video signal. When the diode is an open circuit, you may not be able to pinpoint this problem unless you are familiar with the product performance before the defect or until you start troubleshooting the circuit.

6.9 TESTING THE VIDEO AMPLIFIER

There is no *best* way to test an amplifier. The two most common methods are the signal injection method and the signal tracing method. All gain controls are set for maximum gain.

Signal injection uses a signal generator and starts at the output of the section under test, the CRT in this case. The CRT is the measuring instrument for this test. A signal is applied at a selected test point while observing the face of the CRT. Move backwards through the section until a point is reached where no signal is displayed at the output. You have found the defective circuit.

Signal tracing has a signal applied to the lowest signal level terminal and an oscilloscope is used to observe the signal as it passes through each amplifier in turn. A defect is determined when the signal is lost. Signal tracing is the least complicated and the most often used. The input signal level can be obtained from the schematic diagram. When no level is stated, start at a low level and gradually increase the signal until a detectable signal can be observed on the measuring instrument without distortion. The test frequency may be any convenient signal setting that falls within the amplifier bandpass (1000 Hz is a common test frequency).

- ☐ When you have isolated the defective circuit, determine the dc collector current for normal operation, $V_{cc} - V_c/R_c = I_c$. Use this to understand how a change in voltage causes a change in current and the resulting voltage drop across components.
- ☐ Measure the dc voltages on the base, emitter, and collector.
- ☐ When the base voltage is low, the emitter voltage is low and the collector voltage is high, the defect is in the base bias circuit.
- ☐ When the base voltage is normal, the emitter voltage is high, and the collector is high, the defect is in the emitter circuit.
- ☐ When the base voltage is normal, the emitter voltage is low, and the collector voltage is high, the defect is in the collector circuit or the transistor itself.

QUESTIONS

6.1 From what low frequency to what high frequency is the standard response of a monochrome television video amplifier?

6.2 From what low frequency to what high frequency is the standard response of a monochrome monitor video amplifier?

6.3 What is the practical maximum peak-to-peak output voltage to the CRT from a video amplifier?
(a) 10 $V_{p\text{-}p}$,
(b) 15 $V_{p\text{-}p}$,
(c) 40 $V_{p\text{-}p}$,
(d) 80 $V_{p\text{-}p}$,
(e) 100 $V_{p\text{-}p}$

6.4 What level of dc supply voltage would be appropriate for a video amplifier with 100-$V_{p\text{-}p}$ output signal?
(a) 12 V dc,
(b) 50 V dc,
(c) 100 V dc,
(d) 150 V dc,
(e) 225 V dc

6.5 Elaborate on the polarity and amplitude of the video signal needed to drive the CRT.

6.6 How many times does the signal reverse phase in the circuit in Figure 6.6?
(a) 0,
(b) 1,
(c) 2,
(d) 3,
(e) 4

6.7 How many times does the signal reverse phase in the circuit in Figure 6.8?
(a) 0,
(b) 1,
(c) 2,
(d) 3,
(e) 4

6.8 Which form of transistor amplifier has the greatest gain potential?
(a) common emitter,
(b) common base,
(c) common collector

6.9 Which form of transistor amplifier has the lowest gain potential?
(a) common emitter,
(b) common base,
(c) common collector

6.10 List the type(s) of transistor amplifiers with phase reversal.

6.11 Which form of transistor amplifier has the highest input impedance?
(a) CE,
(b) CB,
(c) CC

6.12 Which form of transistor amplifier has the lowest input impedance?
(a) CE,
(b) CB,
(c) CC

6.13 Which form of transistor amplifier has the highest output impedance?
(a) CE,
(b) CB,
(c) CC

6.14 Which form of transistor amplifier has the lowest output impedance?
(a) CE,
(b) CB,
(c) CC

6.15 What is the highest gain you can expect at 4 MHz from an amplifier with a gain–bandwidth product of 16 million?
(a) 2,
(b) 4,
(c) 6,
(d) 8,
(e) 10

6.16 Which characteristic of an amplifier limits the high-frequency gain?
(a) interelectrode capacity,
(b) stray and wiring capacity,
(c) Miller effect,
(d) series reactance

6.17 What circuit component is used to compensate for high-frequency losses in a video amplifier?
(a) emitter bypass capacitor,
(b) large coupling capacitor,
(c) direct coupling,
(d) peaking coil,
(e) all of the above

6.18 Which circuit component most seriously affects the low-frequency gain of an amplifier?
(a) interelectrode capacity,
(b) stray and wiring capacity,
(c) Miller effect,
(d) series reactances,
(e) series resistances

6.19 What frequency is 3 octaves higher than 800 Hz?
(a) 800 Hz,
(b) 1.6 kHz,
(c) 3.2 kHz,
(d) 250 kHz,
(e) 80 kHz

6.20 What frequency is 3 octaves lower than 320 kHz?
(a) 1.6 kHz,
(b) 3.2 kHz,
(c) 8 kHz,
(d) 80 kHz,
(e) 160 kHz

6.21 What frequency is 3 decades higher than 5 kHz?
(a) 10 kHz,
(b) 20 kHz,
(c) 50 kHz,
(d) 250 kHz,
(e) 0.5 MHz

6.22 What frequency is 3 decades down from 3 MHz?
(a) 30 kHz,
(b) 300 kHz,
(c) 375 kHz,
(d) 750 kHz,
(e) 1.5 MHz

6.23 An amplifier that has a frequency rolloff characteristic of −6 dB per octave will be down by how many decades with a −40-dB rolloff?
(a) 1,
(b) 2,
(c) 3.33,
(d) 6.66,
(e) 10

6.24 What viewing quality is lost when the video amplifier does not include dc reinsertion?
(a) contrast range,
(b) brightness range,
(c) high-frequency detail,
(d) removal of vertical retrace lines, or
(e) all of the above

6.25 What frequency is the dc restoration time constant related to?
(a) the highest frequency of interest,
(b) the full range of frequencies,
(c) the lowest frequency of interest

7 Synchronization

7.1 INTRODUCTION

The synchronizing signal pulses are generated at the television station and transmitted along with the picture and sound information. Their purpose is to control the start and stop of the scanning sequence at the receiver to match the scanning sequence at the camera that generates the picture signal. When the camera is at the top of the picture and scanning down, the receiver should be at the top and scanning down. When the camera is at the left edge of the picture scanning right, the receiver should be at the left of the CRT and scanning right. The first point to be settled then is to establish the function of the sync separator circuit in the receiver. It is intended to slice off all the sync pulses and direct them to their respective deflection oscillators. The video signal, from which the sync pulses are taken, is simply blocked from passing this point in the chain of events. Sync separator circuits are basically clamping circuits followed by a clipping amplifier. The composite string of output sync pulses is applied in parallel to two filters that pass the low-frequency sync to the vertical deflection oscillator and the high-frequency sync to the horizontal deflection oscillator. The sync separator will process only the unmodulated video signal that has been recovered from the station's transmitting picture carrier.

7.2 INTRODUCTORY CIRCUIT

Figure 7.1 is a practical schematic diagram taken from the input section of Figure 6.1 (block diagram) and Figure 6.5 (circuit diagram). The first video amplifier, Q_{101}, has two output signal terminals. The collector signal goes to Q_{102}, the second video amplifier that ends up at the CRT. The emitter output signal goes through C_{501}, to the base of Q_{501}, the sync separator. This special two-output amplifier (Q_{101}) is called a **phase splitter.**

Q_{101} has a positive picture phase signal input to the base and is a voltage divider biased, class A, common-emitter amplifier for the CRT picture signal. The collector signal is reversed in phase with a negative picture phase signal to the base of Q_{102}. However, Q_{101} is also a voltage divider biased, class A, common-collector amplifier for the emitter output signal to the sync separator. As an emitter follower, we know that the phase at the emitter of Q_{101} is the same as the base phase (no change). We also know that the emitter follower has a gain of less than 1. With 1 volt peak-to-peak ($V_{p\text{-}p}$) at the base of Q_{101}, the emitter signal is 0.78 $V_{p\text{-}p}$. The complete composite video signal arrives at the base of Q_{501} with a positive picture phase and an amplitude of .78 $V_{p\text{-}p}$.

7.3 CIRCUIT REQUIREMENTS

The base of Q_{501} in Figure 7.1 shows a dc operating voltage of 11.4 V. Where does this voltage come from? There is no dc source voltage connected to the base circuit. If you have reviewed Appendix C as suggested, you would recognize Q_{501} as a self-biased (or signal biased) class C amplifier. This recognition sets the condition for all sync separator circuits.

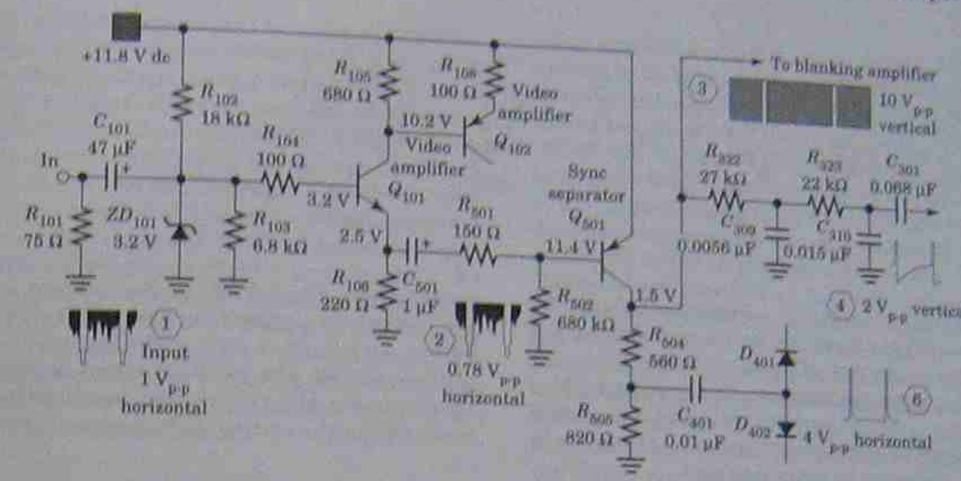


FIGURE 7.1
Part of the video amplifier showing the sync takeoff point, the sync separator, the vertical integrator, and the horizontal differentiator.

Signal bias places a dc voltage on the base by a charge on the base coupling capacitor. In Figure 7.1, the first sync pulse into the left side of C_{501} drives the base negative (turn on for PNP transistors), Q_{501} conducts to charge C_{501} through the base–emitter diode, to the dc supply voltage minus the voltage drop across the base–emitter diode. As the input signal moves in a positive direction, the base–emitter diode of Q_{501} is reverse biased, and the capacitor discharges through R_{502} (680 kΩ) to ground. The *RC* time constant of R_{502} and C_{501} is long (0.68 second), and the voltage charged on C_{501} that is lost due to the discharge time is small compared to the time of the input signal pulses. Each succeeding horizontal sync pulse peak is now clamped to this level. Sync separators are class C amplifiers because the clamped sync pulse peaks must drive the amplifier into conduction for strong or weak input signal levels. The class C amplifier adjusts the dc voltage at the base to correspond to the input signal strength.

A further stipulation for sync separators is that they are almost always silicon switching transistors. Silicon is popular because of the lower base-to-emitter voltage drop (0.3 V dc typical). They are switching transistors because of the small change in input voltage required to shift from the cutoff condition to a saturated (full on) condition. For example, with 0.3-V dc difference between the base and the emitter, the transistor is cut off (nonconducting). With 0.8-V dc difference between the base and the emitter, the transistor is fully saturated (on hard).

7.4 OUTPUT SIGNALS

The emitter voltage of Q_{501} is 1.5 V dc when the transistor is in the ready state and a trickle current is flowing through R_{504} and R_{505}. When the transistor is saturated, about 0.3 V dc is dropped across the transistor, with the remaining voltage from the dc supply (11.8 V − 0.3 V = 11.5 V) appearing at the emitter across R_{504} and R_{505}. Therefore, the peak-to-peak output signal of the composite sync pulses will be 11.5 V − 1.5 V = 10 $V_{p\text{-}p}$. See the waveform at point 3 of Figure 7.1.

7.4.1 Vertical Integrator Output

The full output signal of Q_{501} is fed through an integrating four-pole low-pass filter (two *L* filters in series) to the base of the vertical oscillator Q_{301}, by way of the coupling capacitor C_{301}. The 60-hertz (Hz) vertical sync pulses are attenuated by −14 decibels (dB) to an output level of 2 $V_{p\text{-}p}$ to the vertical oscillator. The horizontal sync pulses pass through the same filter but are attenuated by −55 dB. The horizontal sync pulse signal is −41 dB below the level of the vertical sync pulse going into the vertical circuit.

Waveform 4 in Figure 7.1 is the combination of the feedback wave in the vertical oscillator (see Figure 3.5) and the integrated vertical sync pulse

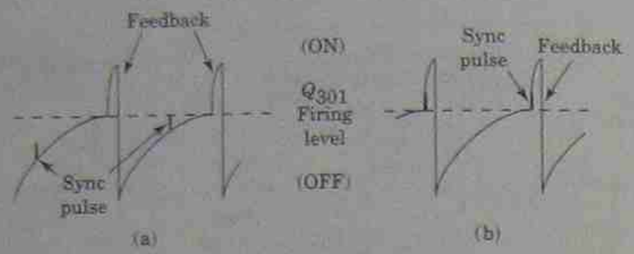


FIGURE 7.2
The relationship between the vertical oscillator wave and the vertical sync pulse: (a) oscillator out of sync; (b) oscillator in sync.

from the sync separator Q_{501}. Figure 7.2a shows the vertical oscillator feedback signal and the vertical sync pulse for an **out of sync** condition. When the sync pulse peak reaches into the conducting bias voltage range of the vertical oscillator, the oscillator triggers and starts a new cycle. This is shown in Figure 7.2b for the **in sync** condition.

Figure 7.3a is a composite string of sync pulses during the vertical blanking interval and represents only the sync pulses, equalizing pulses, and serrations from Figure 5.5 for the first field of the composite video wave.

The vertical integrator in Figure 7.1 has a long *RC* time constant of about 1 millisecond (ms) compared to the time of the vertical sync pulse of 0.2 ms. The vertical integrator output pulse wave is shown in Figure 7.3c and is seen to rise slightly for each horizontal sync pulse, but decays rapidly due to the short pulse time of 5 microseconds (μs) that the horizontal pulse represents.

During the vertical sync pulse time (3*H*), the composite sync pulse voltage is high for a longer period of time, and the integrator output signal rises progressively for each of the six serrated parts of the vertical sync pulse. The decay time during the narrow serrations is short and the drop in output voltage is small. The resulting output buildup from the integrator, although shabby, is adequate to correctly trigger the vertical deflection oscillator.

7.4.2 Differentiator Output

The tapped down output of Q_{501} in Figure 7.1 between R_{504} and R_{505} reduces the horizontal sync signal by −4.6 dB, and it loses another −3.4 dB through the coupling capacitor C_{401} to the horizontal AFC diode circuit. The horizontal sync signal at test point 6 is 4 $V_{p\text{-}p}$. The vertical sync signal through the same differentiator (high-pass filter) is −48 dB below the 4-$V_{p\text{-}p}$ horizontal sync signal level. The two synchronizing signals are now separated from each other through this dual-filter system.

The horizontal differentiator action is seen in Figure 7.3b during the same vertical blanking pulse interval as in Figure 5.5 to illustrate the difference in timing between the two filters. The leading edge of the horizontal sync pulse is a rising voltage that results in a rapid rise at the output of the differentiator. However, because of the short *RC* time constant (1 μs) compared to the time of the 5-μs horizontal sync pulse, the voltage decays to zero again. At the trailing edge of the horizontal sync pulse, the fall of the pulse voltage causes a negative spike to appear at the differentiator output, which also decays rapidly to zero. Only the positive spikes of voltage are useful for this polarity of sync signal. Notice that during the equalizing pulse period and the serrated vertical sync pulse time the horizontal sync pulses are at double speed, or 31,500 Hz, to initiate the full line–half line sequence for interlace scanning.

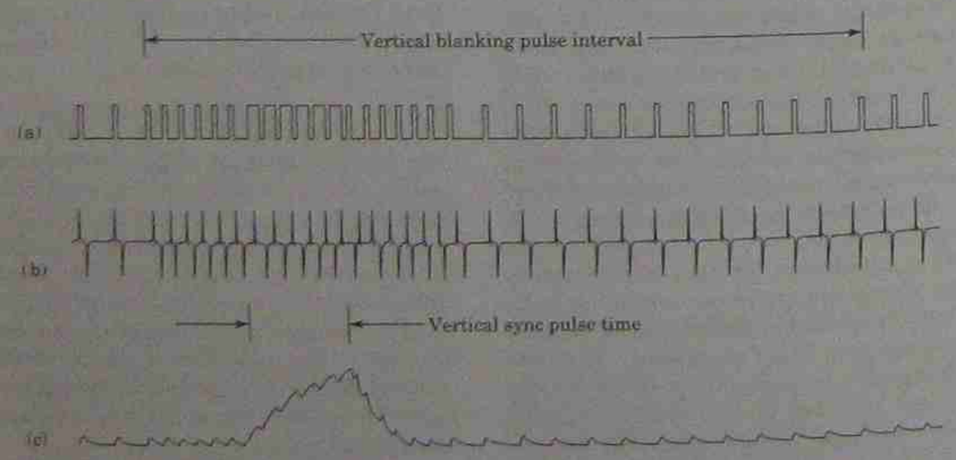


FIGURE 7.3
The timing relationship in the sync separator: (a) the composite string of sync pulses; (b) the differentiator output pulses; (c) the integrator output pulses.

7.5 DIODE SYNC SEPARATORS

A diode used as a clamper could substitute as a separator in the synchronizing circuits. However, it would also require a clipping diode and an amplifier. A combination clipping amplifier is the standard class C amplifier, and the class C amplifier also clamps the input signal to the voltage charge on the input coupling capacitor. Because of the necessary add-on circuits, an individual diode sync separator would *rarely* be encountered in a practical situation, but it will work.

7.6 DIGITAL COUNTDOWN CIRCUITS

The digital countdown system is a monolithic integrated chip that combines the sync circuits, the vertical oscillator circuits, and the horizontal oscillator circuits all in one package. It was deemed practical to present this system as a whole here, rather than break it up into three separate parts in the preceding three chapters.

Note also that, until now, the vertical frequency was given as 60 Hz and the horizontal frequency as 15,750 Hz. These were the true values when television was originally developed and remained so for many years. When color was added to the television signal, for reasons explained in Chapter 8, the horizontal frequency was changed to 15,734.26573 Hz and the vertical frequency then became 59.94006 Hz. These values are within 0.1% of the original frequencies, so no changes had to be made at the receivers because the receivers synchronized easily to the new frequencies. Only the television stations had to readjust their transmitters to reflect these new changes. When discussing the horizontal or vertical frequencies in general terms, it is still common practice to use the 15,750 and 60 Hz as the frequency values. However, when technical accuracy is required, then 15,734.266 Hz and 59.94 Hz are used. The published literature for the digital countdown systems uses the technically correct frequencies.

Figure 7.4 is a simplified block diagram used to show how the overall system works. The horizontal sync input signal to pin 3 and the horizontal feedback signal into pin 14 are compared in frequency by the phase detector block 1 (AFC). The VCO is designed to operate at some multiple of the horizontal frequency. In this example, we use 2*H*, or 31.468532 kilohertz (kHz). The VCO signal is divided by 525 (block 3) to develop the vertical frequency of 59.94 Hz at pin 8 and is divided by 2 (block 4) to develop the horizontal frequency of 15.734266 kHz at pin 10. One oscillator now becomes the master oscillator for the vertical deflection, as well as for the horizontal deflection sections. This principle is called **frequency synthesis,** that is, producing two or more different synthetic frequencies from one oscillator.

Several versions of countdown circuits are currently in use. We will examine the RCA circuit in detail and follow up by examining other systems in the areas where they differ. Only the block diagram presentation is given on the service schematic with external components. You will need to research the specification sheets for the individ-

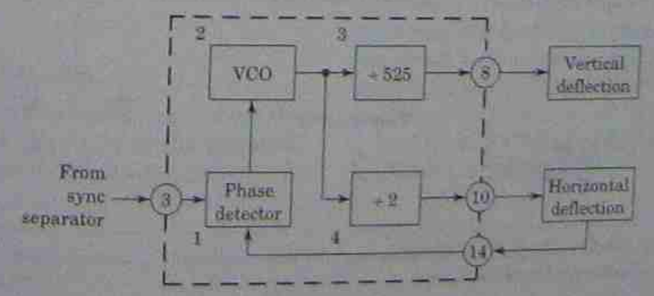


FIGURE 7.4
Simplified digital countdown block diagram.

ual chip in order to determine which circuits are used in each block.

7.6.1 Horizontal Section

In Figure 7.5, a negative picture phase video signal is applied at pin 57 to the sync separator. The separator could be any of the common circuits described earlier, which would include a horizontal differentiator circuit, but is not shown in this schematic drawing. The horizontal sync pulses out of the separator are applied to the phase detector for automatic frequency control (AFC). The second input to the phase detector, at pin 59, comes from the horizontal output transformer in the form of a positive 30-$V_{p\text{-}p}$ feedback pulse. The pulse is integrated by the *RC* filter circuit to deliver a 2-$V_{p\text{-}p}$ sawtooth wave at pin 59. The 20 kilohm (kΩ) potentiometer in this circuit is termed a **phase control,** but in a phase-locked loop circuit, phase is equivalent to frequency, so this control works to adjust the horizontal frequency (horizontal hold control).

The output from the phase detector is the dc error voltage that stabilizes the voltage-controlled oscillator (VCO) at the correct frequency. When the horizontal pulses from the sync separator and the feedback pulse from the output transformer (at pin 59) are the same frequency, the dc error voltage is $\frac{1}{2}V_{cc}$, but cannot be measured on this device. Should either frequency change markedly, the error voltage changes to lock the VCO onto the sync pulse frequency, when the new frequency is within the lock range of the VCO.

The VCO will free run at about 32 times the horizontal frequency when *no* horizontal sync pulses are present. The free-running frequency of the VCO is determined by the crystal (or ceramic resonator) at the oscillator output, pin 63, where a 20-$V_{p\text{-}p}$ sine wave may be observed. The VCO output signal is fed back to pins 61 and 62 to sustain oscillations. Again, no internal circuit is given.

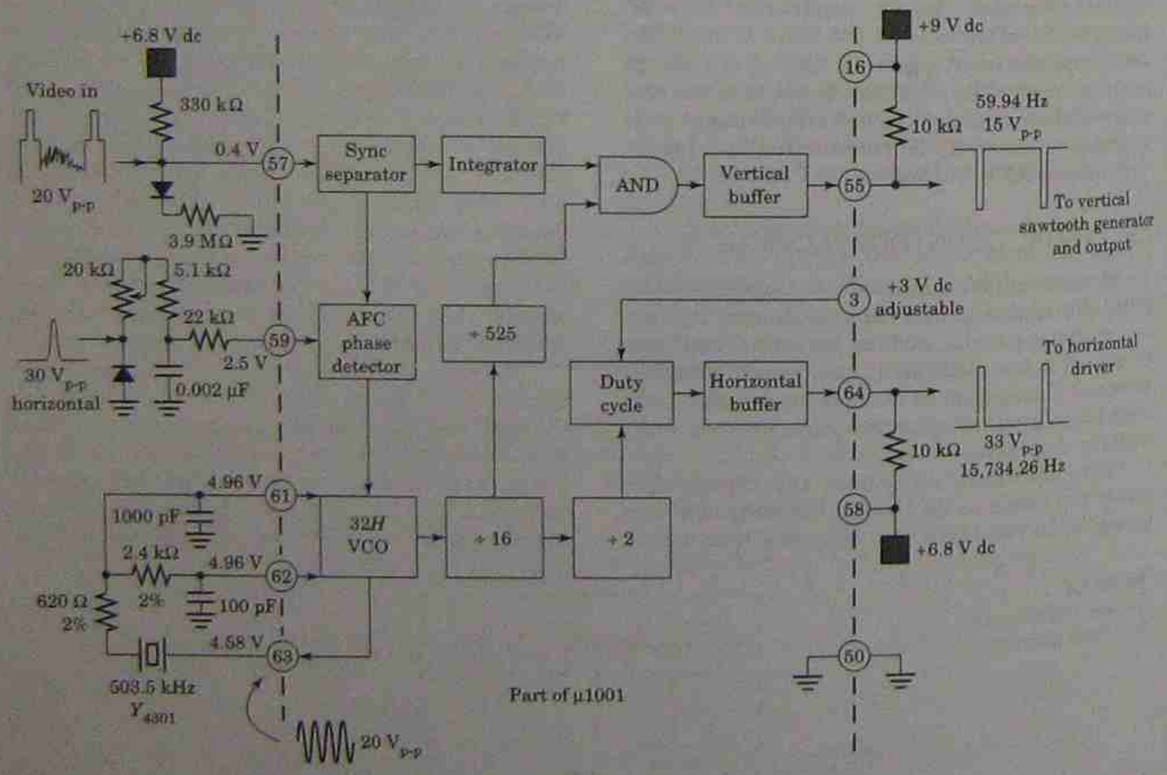


FIGURE 7.5
Digital countdown circuit used in RCA 156/157 chassis. (Courtesy of Thompson Consumer Electronics, Inc.)

In the general description, a VCO frequency of $2H$ was identified because of the dividers needed to derive the vertical frequency. Actually, any frequency related to $2^N H$ will work equally well. Both Zenith and RCA use $2^5 H = 32H = 503.5$ kHz for the free-running frequency of the VCO. One wonders if this is a coincidental choice or forward thinking in light of the new closed caption clock frequency.

The VCO output signal to the divider circuits is an overdriven sine wave that resembles a square wave. The divide by 16 (four divide by 2's) circuit outputs a square wave at 31.46853 kHz. This signal is divided by 2 again to develop the 15.73426-kHz horizontal drive signal frequency to the deflection circuits. Digital dividers output a 50% duty cycle square-wave signal, which must be changed to an 18% duty cycle for the standard horizontal scanning deflection wave. The duty cycle adjust block is most likely a monostable *JK* flip-flop timer that has a variable *on* time determined by the dc voltage on pin 3. Approximately +3 V dc (at pin 3) will set the *on* time to about 11.5 μs and equal to the horizontal retrace time.

During the vertical time period, where the equalizing pulses and serrations are active, the horizontal sync pulse input is doubled in frequency. This will cause the dc error voltage out of the phase detector to rise and change the VCO output frequency. At the end of the equalizing pulse sequence, the horizontal input frequency returns to normal and the dc error voltage drops back to $\frac{1}{2}V_{cc}$, coincidentally timed to start the horizontal oscillator on a half-line scan or full-line scan in accordance with the exact number of equalizing pulses in that field.

The remaining circuit is the buffer amplifier, which is a low-output impedance, noninverting amplifier, and puts out a 33-$V_{p\text{-}p}$, short-duration, positive-pulse output to pin 64 at the horizontal frequency. The action of the buffer amplifier is to isolate the internal circuits and their performance from any external loading effects connected to pin 64 output terminal.

7.6.2 Vertical Section

The vertical section becomes independent from the horizontal circuits (in Figure 7.5) at the output of the divide by 16 counter and at the vertical output of the sync separator. The vertical sync output is integrated and applied to one input of an AND gate. Some literature calls this circuit a *coincident gate.*

The output of the divide by 16 counter is a 31.46853 kHz square wave that must be divided by 525 to develop the 59.94-Hz vertical frequency. The 525 divider is most likely an analog divider that can divide by any whole number, odd or even, whereas digital dividers are efficient only at divide by 2^N. The actual divide circuits are ÷7, ÷5, ÷5, and ÷3, which are identical to the divide by circuits used in the sync generator* at every television station since the inception of broadcast television. The sync generators were originally tube types, then field-effect transistors, and now are monolithic chip circuits. These four dividers may be arranged in any order to extract a submultiple frequency lower than 31.46853 kHz but higher than 59.94 Hz.

The output signal from the 525 dividers is applied to the second input to the AND gate. The truth table for the AND gate shows that the output is high only when both input terminals are high. This condition exists when a positive vertical sync pulse is present on one input and the high half-cycle of the 59.94-Hz square wave from the 525 divider is present on the second input to the AND gate. The vertical sync decays to zero after the 190.5-μs pulse duration, and the AND gate output goes to zero. The AND gate output remains low for the balance of the 59.94-Hz vertical cycle. The gate output goes high again when the next divider cycle goes high, and another vertical sync pulse appears.

One major advantage to countdown circuits is frequency stability. The VCO would need to change by 8400 cycles for the vertical frequency to change by 1 cycle.

7.6.3 Other Countdown Circuits

One version of countdown circuitry uses two separate chips, where the video amplifier and sync separator are in one chip while the divider circuits are in a second chip. There are two sync output terminals from the first chip and two separate sync input terminals to the second chip. The rest of the countdown circuits are as described earlier. No diagram will be given here.

A second version, shown in Figure 7.6, has the unfiltered composite sync chain from the sync sepa-

*See Figure 6.6 in *Electronic Communications, Modulation and Transmission*, 2nd ed., Macmillan Publishing Co., New York, 1992.

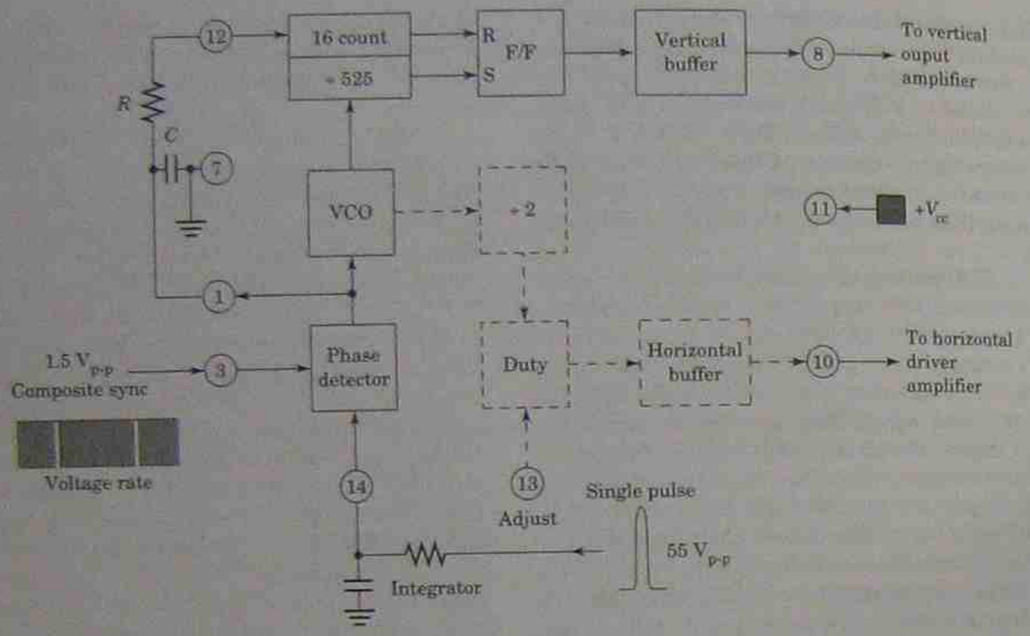


FIGURE 7.6
The vertical section of a countdown circuit in solid blocks. The horizontal section is in dashed blocks.

rator (1.5 $V_{p\text{-}p}$) applied to the phase detector input to control the horizontal section while the vertical section is synchronized by the internal timing circuits.

The phase detector receives the sync pulses at pin 3 and the feedback sawtooth voltage wave at pin 14 (0.9 $V_{p\text{-}p}$) from a positive 55-$V_{p\text{-}p}$ output transformer pulse. The phase detector dc error output voltage is $\frac{1}{2}V_{cc}$ when both input frequencies match. The VCO at this time is locked to the 2*H* output frequency. The horizontal section action is as described in the previous discussion.

The rise in the dc error voltage out of the phase detector during the equalizing pulse sequence sets the 16*H* counter into its timing cycle. The output square wave from the 525 divider is connected to the SET terminal of an *R/S* flip-flop timer. The 16*H* counter will clock off 16 cycles of the 31.46826-kHz VCO signal (equal to eight horizontal time periods) and then shut down. The divide by 525 circuit remains in full operation for as long as power is applied to the circuit. The output of the 16*H* counter is connected to the reset terminal of the *R/S* flip-flop so that the flip-flop output will be high for eight horizontal time periods (0.508 ms) and then go low for the remainder of the 525 divider output count. The next set of equalizing pulses to arrive starts another vertical scanning cycle.

Another variation to countdown circuits is seen at the dc error voltage output terminal. The error voltage exits the chip at pin 1, goes through a filter, and reenters the chip at pin 12 to the 16 counter. The purpose of the filter is to prevent **hook,** or top bending in the picture.

7.7 CHARACTERISTICS OF NOISE

Noise, in general, is identified as any undesirable electrical disturbance that mixes with the signal. All noise appears in the signal as changes in amplitude. Noise may be natural, such as thunderstorms and cosmic disturbances, or it may be man-made, such as arcing in electric motors, automobile spark plugs, or neon signs and lighting, to name a few.

Internal noise in low-level-signal amplifiers is caused by the dc current flow (electron movement) through a resistor. If a consistent number of electrons per second enter a resistor, the number of electrons per second leaving the resistor may not be as consistent for the following reasons. Each individual electron might find a different path through the resistor or might have more collisions with other electrons as they travel through the resistor

and will exit the resistor at an instantaneously varying rate of current flow. This changing rate of current appears as noise called **thermal** or **Johnson noise** and is generally in the frequency range of 1 to about 12 kHz. Cosmic noise extends up to 15 MHz, but decreases rapidly above that frequency.

The point is that, once noise contaminates the signal, it is impossible to remove it. The best we can hope for is to counteract some of the ill effects of noise.

The pulse amplitude sensing circuits used for synchronization cannot tell the difference between a legitimate sync pulse and a maverick noise pulse. In synchronizing circuits, a noise pulse that is greater in amplitude than the blanking level can cause false triggering of the deflection oscillators. The picture will jump vertically or slant diagonally when noise pulses introduce false starts in the oscillators.

The vertical integrator, as a low-pass filter, eliminates all of the higher frequencies where noise is most harmful. The vertical sync voltage is adversely affected by 60- and 120-Hz ripple voltage (hum) from the low-voltage power supply. This is generally not a problem when the power supply and decoupling capacitors are working correctly.

The horizontal differentiator, as a high-pass filter, passes all the noise spikes as well as the differentiated sync pulses. So it is the horizontal deflection system that suffers the most in the presence of noise contamination of the video signal.

7.7.1 Noise Canceling Systems

Noise spikes can occur in rapid succession, maybe eight or more pulses in one horizontal scan time (one line), and be randomly located. Figure 7.7 shows only five noise pulses over two horizontal cycles to identify how each type of noise pulse is treated.

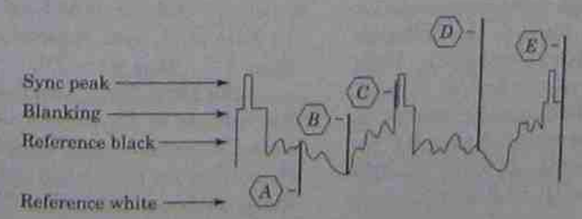
Noise can occur as positive or negative narrow spikes of voltage in the video wave. Pulse *A* in the wave is negative in nature. It will spike toward white and cause a white speck to appear in the picture being viewed. Spike *A* will not affect the synchronizing process and will not be treated as noise. Pulse *B* is a positive spike that, in this instance, causes a black speck to appear in the picture being viewed. However, spike *B*'s amplitude is less than the blanking level. It does not interfere with the synchronizing process and is not treated as noise.

Special note: Spikes *A* and *B* can be removed as noise pulses by very elaborate digital video processing systems, but only when the noise pulse width equates to a half-cycle of voltage for a frequency higher than 4 megahertz (MHz).

Noise pulse *C* is a borderline case that (1) is greater in amplitude than the blanking level but less than the sync pulse peak, and (2) it is within a few percent of one horizontal time period away from the true sync pulse and may or may not interfere with the synchronizing process. Noise pulse *C*, in all likelihood, will not be treated as a threatening noise pulse.

Noise pulses *D* and *E* represent the vast majority of noise spikes that occur in the video signal. This is fortunate because they can be the most damaging to the synchronizing process, and yet are the easiest noise pulses to control. They are the only noise pulses in Figure 7.7 that can be canceled because they have an amplitude greater than the sync pulse peaks.

FIGURE 7.7
Sample noise pulses over two horizontal cycles, explained in the text.

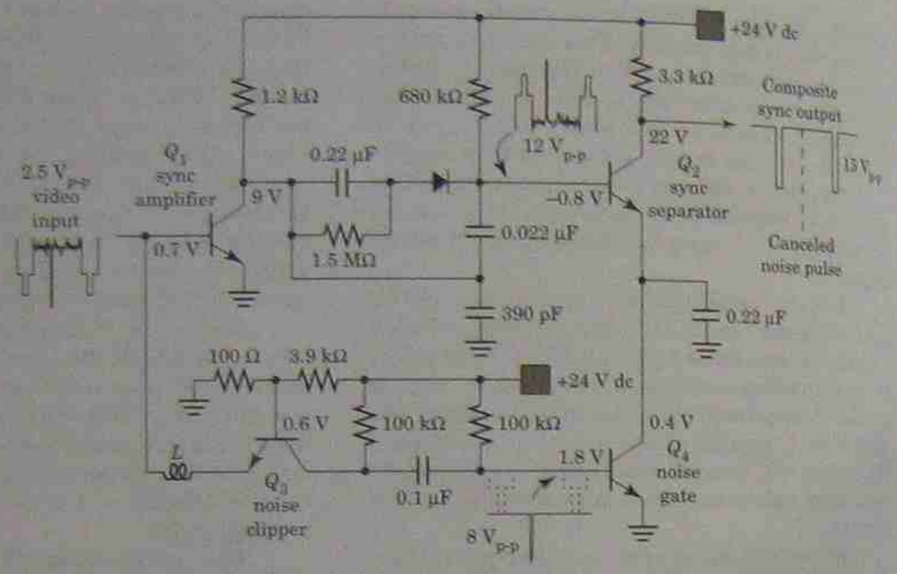


7.7.2 Noise Gates

The two common circuits used to cancel noise are the (1) series noise gate and (2) the noise inverter. The circuits will be described in that order.

The series noise gate, in Figure 7.8, shows an inverting sync amplifier as Q_1 and the sync separator as Q_2. The sync amplifier need not be a class A linear amplifier because video distortion at this circuit location is of little consequence. It should not, however, distort or compress the sync pulses at this time. The sync amplifier is operated between class A and class B, called class AB operation. The 2.5-$V_{p\text{-}p}$ input signal, with a noise pulse, is amplified and inverted, compressing the white level while preserving the linearity of the sync pulse polarity.

FIGURE 7.8
A noise gate form of noise cancellation.



The sync separator Q_2 is operated as a signal biased, class C, common emitter amplifier so that only the positive-going sync pulse (and noise pulse) will turn the amplifier on to produce an output signal.

In parallel with sync amplifier Q_1 and sync separator Q_2 is the noise canceling circuit of Q_3, noise clipper, and Q_4, noise gate. The noise clipper is a voltage divider biased, class C, common-base amplifier. Observe the base resistance ratio of 40:1 to determine class C operation. The same video input signal of 2.5 $V_{p\text{-}p}$ that was applied to Q_1 is also applied to the emitter of Q_3. Q_3 is a clipper that removes (and saves) voltage levels that exceed the sync pulse peaks. These are the noise spikes greater than the sync pulses. The negative noise spikes are applied to the base of Q_4 to turn Q_4 off during the noise spike time. Q_4 is a base biased, class A, common-emitter switching transistor gate. It is called a gate because it does not amplify. It is either saturated (the normal state) or it is totally turned off. Q_4 is also in series with the sync separator Q_2. Two volts dc dropped across the 3.3-kΩ collector resistor of Q_2 means that 0.6 milliamperes (mA) of current flows through Q_2. If you consider that the emitter current is equal to the collector current, then 0.6 mA also flows through Q_4. With 0.4-V dc drop across Q_4 and 0.6 mA of current through it, Q_4 looks like a 660-Ω emitter resister to Q_2. When an amplified noise pulse of negative polarity is present at the base of Q_4, Q_4 turns off. This acts like an open emitter for Q_2, and Q_2 stops amplifying for the period that the noise pulse is active, which takes the noise pulse out of the string of sync pulses passing through Q_2.

7.7.3 Noise Inverters

Several points should be emphasized at this time. (1) The circuits of Figures 7.8 and 7.9 do the same work, but in different ways. (2) Noise canceling circuits remove noise pulses from the sync signal only. The noise pulses remain with the video signal all the way to the CRT and will be present in the picture.

The noise canceling circuit in Figure 7.9 starts with the application of a 2-$V_{p\text{-}p}$ positive picture phase signal into the base of Q_1. Q_1 is a voltage divider biased class A, phase splitting amplifier. The emitter output signal is slightly lower, but in phase with the base input signal. The emitter output signal will continue on through more video amplifiers to the CRT.

The collector output signal has a gain of 9 and is inverted from the input. See waveforms *A* and *B*. The collector output signal will pass through the 330-Ω resistor, up through the 0.02-microfarad (μF) capacitor and the 0.047-μF capacitor to arrive at the base of Q_3 sync separator with an amplitude of about 8 $V_{p\text{-}p}$ (see wave *D*).

The same 2-$V_{p\text{-}p}$ input signal is also applied to the emitter of Q_2, which is an adjustable biased class C, common base, clipping amplifier. The base bias (dc) is set to clip the video signal at the peak of the sync pulse (see wave *C*) for noise amplitudes

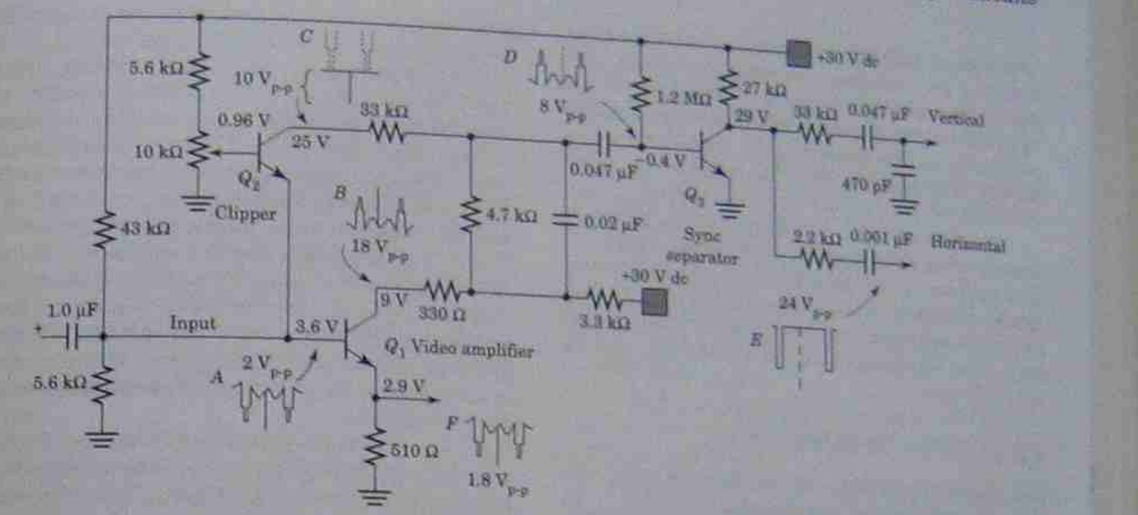


FIGURE 7.9
Noise inversion and cancellation.

greater than the sync pulse peaks. The inverted and amplified noise pulse at the collector of Q_2 is added to the reduced video signal at the base of Q_3 sync separator. The noise pulse is canceled. The base biased, class C, common-emitter sync separator Q_3 passes the composite string of sync pulses to be separated by the vertical integrator and horizontal differentiator for their respective deflection oscillators.

7.8 TROUBLESHOOTING SYNC CIRCUITS

You will isolate problems to the sync circuits by observing the picture on the face of the CRT. The patterns for defects in the sync circuits are (1) the picture rolls up or down slowly, (2) the picture tears (slants) to the left or to the right, (3) the conditions cited in (1) or (2) both occur at the same time, and (4) intermittent behavior. These conditions presume that the picture viewed on the CRT is standard good quality.

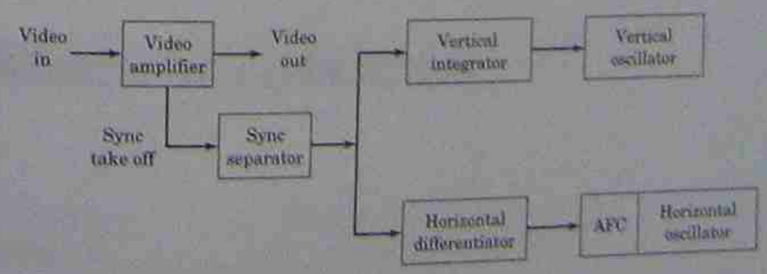
Study the block diagram in Figure 7.10 before diagnosing sync circuit problems.

7.8.1 Picture Rolls Vertically

You observe that the picture appears to be stable horizontally, but is not steady in the vertical direction. The first step is to adjust the vertical hold control. You want to see if the picture can be made to roll up and then roll down. If it can roll in both directions, this tells you that somewhere between rolling up and rolling down the vertical oscillator *will* run at the correct frequency and is OK.

The horizontal holding is OK, which tells you that the sync separator and the horizontal AFC are working. The problem must be in the vertical integrator circuit. There are no dc voltages on the

FIGURE 7.10
Synchronizing circuit block diagram.



schematic to help you to test the integrator. Therefore, use the oscilloscope to tract the vertical sync signal through the integrator. Capacitors are the most likely component to cause this type of defective operation. They may short or open, or they may become leaky (partial short that acts like a high resistance).

Incidentally, if the picture rolls only in one direction when adjusting the vertical hold control, it tells you that the vertical oscillator is too far off frequency for the sync signals to be effective. Rolling up only means that the oscillator frequency is too high. The frequency is too low when the picture only rolls down.

7.8.2 Picture Tears Horizontally

You observe that the picture is not rolling, but has dark diagonal bars slanted in either direction. The troubleshooting procedure here is similar to the outline described for the vertical section. Adjust the horizontal hold control first to determine if the horizontal oscillator will run at the correct frequency. If it will, then use the oscilloscope to test the differentiator and AFC circuits. Be critical when measuring peak-to-peak signal voltages.

7.8.3 Total Loss of Synchronization

Here the picture is rolling and has slanted dark bars at the same time. The chance of a defect in two different circuits at the same time is extremely slim. Look for a circuit that is common to both the vertical and horizontal signals. The sync separator is the most likely cause of this type of problem. Using the oscilloscope to measure the input and output signal levels will help to isolate this defective area. A weak input signal could produce these effects and may lead you back to the video amplifier that supplies the sync takeoff signal.

The sync signals are transmitted as 25% of the peak-to-peak video signal. When a circuit before the sync separator is defective and operating on the nonlinear part of its transconductance curve, the sync pulses could be compressed to 5% or 10% of the peak-to-peak video. You may find it helpful to examine the **hammerhead** pattern in Figure 7.11 to determine sync compression. Reduce the contrast range to emphasize the difference in amplitude from the vertical blanking level (medium gray) to the vertical sync level (darker gray). A reasonable difference in level implies no sync compression. This is a judgment call learned from experience.

The sync input signal is the composite video, and the peak-to-peak level should be measured using the vertical rate scope display. This will establish the white level as well as the sync pulse peak level to confirm your findings.

The sync separator may include a noise cancellation circuit (not shown in Figure 7.10) that could prevent the separator from working as it was intended to work. Measure the dc voltages in the circuit. Comparing your readings to those marked on the schematic will isolate the defect to the component level.

7.8.4 Digital Countdown Circuits

The countdown chip carries with it the same astigmatisms that all chips have. That is, you cannot reach inside the chip and repair or replace any of the parts. When one component in the chip fails, you replace the whole chip. But don't be *too* hasty to replace chips until you have examined all the peripheral components that support the chip in its operation. Examine the input and output signal wave forms and measure the dc operating voltages at each pin before drawing a conclusion.

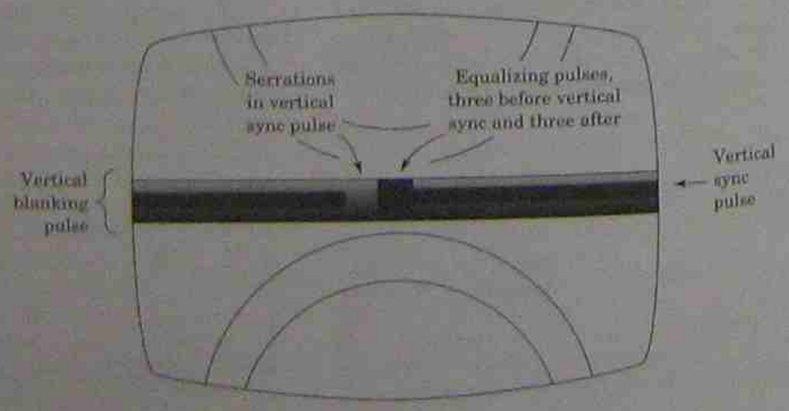


FIGURE 7.11
Hammerhead pattern. Used to examine the vertical blanking and sync pulses.

The troubleshooting procedure here for the countdown circuits takes the reverse approach from the common top-down method. Here we suppose that an internal circuit has failed, one at a time, and try to predict what the effects will be on the CRT display.

If the horizontal phase detector fails, the VCO will go off frequency and the horizontal display will go out of sync. Because the vertical is counted down from the horizontal, the picture will also roll. You will measure normal input signals. The output signals will have normal levels, but will be off frequency.

If the VCO fails, there will be no horizontal drive signal, no horizontal deflection, and, most importantly, no high voltage, so there will be *no raster*. You will not be able to visually determine vertical scan. The input signals will be normal, but you will measure no output at the horizontal or vertical output terminals.

If the divide by 2 circuit, the duty cycle circuit, or the horizontal drive circuit fails, there will be no raster for the same reasons just cited for the VCO. The input signals, the VCO signal, and the vertical output signals will all be normal, but there will be no horizontal drive signal.

If the divide by 525 circuit fails, the horizontal drive output is unaffected and there will be a CRT display. The display will be one bright horizontal line across the center of the CRT because there is no vertical deflection. The same effects result if the vertical buffer fails.

When the sync separator and the 16 count circuits are part of the chip and either fails, you will lose vertical sync only.

Measure all the dc voltages of the chip and check all the waveshapes with the oscilloscope; then compare them to the data supplied on the schematic diagram before making a conclusion.

QUESTIONS

Questions 7.1 through 7.13 apply to discrete component circuits only.

7.1 Sync separators are basically
(a) clampers,
(b) clippers,
(c) amplifiers, or
(d) all of the above.

7.2 The sync separator separates the vertical sync pulses from the horizontal sync pulses.
(a) true
(b) false

7.3 The sync separator separates the composite sync chain from the video signal.
(a) true
(b) false

7.4 What is the nature of the input signal to the sync separator?

7.5 What is the nature of the output signal of the sync separator?

7.6 What class of amplifier is the sync separator?
(a) class A,
(b) class AB,
(c) class B, or
(d) class C

7.7 What is the nature of the signal out of the integrator?

7.8 What is the nature of the signal out of the differentiator?

7.9 In a defective receiver, the picture rolls (up or down) only. The suspect fault is in the
(a) vertical oscillator,
(b) horizontal oscillator,
(c) differentiator,
(d) integrator,
(e) sync separator.

7.10 In a defective receiver, the picture has slanted bars (left or right) only. The suspect fault is in the
(a) vertical oscillator,
(b) horizontal oscillator,
(c) differentiator,
(d) integrator,
(e) sync separator.

7.11 In a defective receiver, the picture rolls and has slanted bars. The suspect fault is in the
(a) vertical oscillator,
(b) horizontal oscillator,
(c) differentiator,
(d) integrator,
(e) sync separator.

7.12 If the vertical integrator fails, there will be no vertical deflection.
(a) true
(b) false

7:13 Noise canceling circuits work
(a) in series,
(b) in parallel with the sync separator.

Questions 7.14 through 7.18 apply to digital countdown circuits only.

7.14 If the phase detector fails completely, the effects on the face of the CRT will be
(a) picture rolling,
(b) picture slanted,
(c) picture rolling and slanted,
(d) one bright horizontal line,
(e) no raster.

7.15 If the VCO fails completely, the effects on the face of the CRT will be
(a) picture rolling,
(b) picture slanted,
(c) picture rolling and slanted,
(d) one bright horizontal line,
(e) no raster.

7.16 If the divide by 2 circuit fails completely, the effects on the face of the CRT will be
(a) picture rolling,
(b) picture slanted,
(c) picture rolling and slanted,
(d) one bright horizontal line,
(e) no raster.

7.17 If the divide by 525 circuit fails completely, the effects on the face of the CRT will be
(a) picture rolling,
(b) picture slanted,
(c) picture rolling and slanted,
(d) one bright horizontal line,
(e) no raster.

7.18 If the sync separator fails completely, the effects on the face of the CRT will be
(a) picture rolling,
(b) picture slanted,
(c) picture rolling and slanted,
(d) one bright horizontal line,
(e) no raster.

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8 Color

8.1 INTRODUCTION

To understand how color is reproduced in video systems, it is first necessary to know some of the science of color and how the eye responds to color. For there to be sight, there must first be light. Light, as used here, means white light and will be treated as direct light and reflected light. Light is radiant energy.

8.2 LIGHT

Sir Isaac Newton (1642–1727) pondered the existence of a rainbow and what caused it. He concluded that sunlight passed through a tear-shaped raindrop at a specific angle and was divided into a range of colors. His experiment, to prove his theory, was to pass a narrow beam of sunlight that came from a pin hole in his window shade through a glass prism and onto a sheet of white paper. As light passed through the boundaries of two materials having different densities, air to glass and glass to air, the light beam was refracted (bent) to display a rainbow pattern on the paper. From this simple experiment, Newton concluded two important basic laws of physics: (1) White light is the sum of all colors of light, and (2) because each color was refracted at a slightly different angle, each color must be radiant energy at a slightly different frequency. Figure 8.1, rendered in half tones, shows

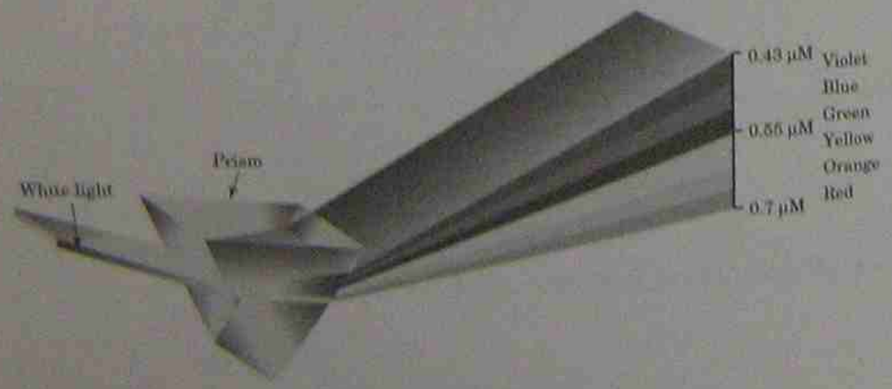


FIGURE 8.1
Newton's experiment to separate white light into the colored light of the rainbow.

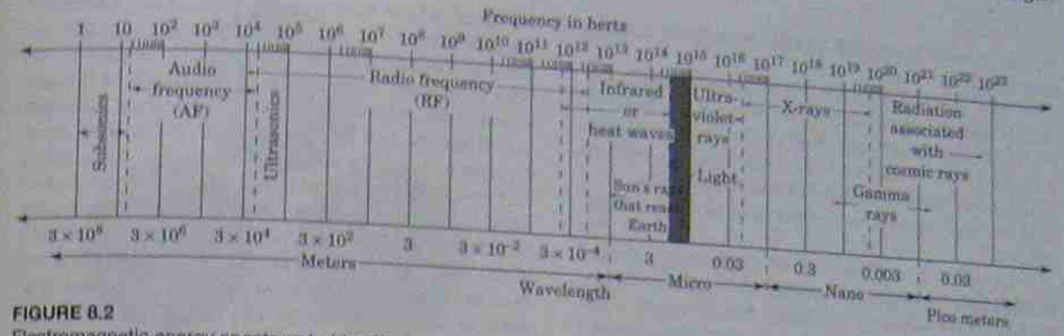


FIGURE 8.2
Electromagnetic energy spectrum to identify the visible light band.

the results of this experiment. It is interesting that the colors in Newton's experiment are in the same order as the resister color code: red, orange, yellow, green, blue, and violet.

Much later, the exact frequency range of visible light was determined by others. The full radiant energy spectrum is found in Figure 8.2, which shows the visible light band in the frequency range from 430 million megahertz (MHz) for the color violet to 700 million MHz for the color red. Frequency is shown along the top edge of the spectrum in Figure 8.2, while wavelength is shown along the bottom edge. The length of one cycle of energy (wavelength) is found by dividing the speed of light in meters (m) (300×10^6m) by the frequency of the wave in hertz (Hz). The wavelength for the color violet at 430×10^{14} Hz is 0.7 micrometers (μm), and the wavelength of red at 700×10^{14} Hz is 0.43 μm. These wavelength notations are also given in Figure 8.1. Some final conclusions formed by this experiment are that, if white light can be divided into a range of color light bands, it also holds true that the full range of color light can be combined to make white light. Furthermore, if the sum of all wavelengths of light is white, then the absence of all light should represent *black*.

8.2.1 Chromaticity

The accomplishments of James C. Maxwell (1831–1879) in the area of light studies resulted in the *chromaticity* diagram of Figure 8.3. The area inside the horseshoe-shaped curve represents all the colors that stimulate the eye, identified in wavelengths. The sum of all colors of light is equal to white, which appears at the center of the diagram as "C" (chromatic).

What appears to be white for one viewer may not be exactly white to another viewer. Therefore, a standard for white had to be established and defined. As a metal is heated, it turns a deep cherry red. Increasing the temperature changes the metal's color to orange, then yellow, then white. A tungsten filament heated to 6500 K will produce the standard white that is identified in Figure 8.3 as C. The kelvin (K) is the unit of a temperature scale starting at absolute zero, which is 273 degrees Celsius below the freezing point of water at sea level. The standard white is measured using a col-

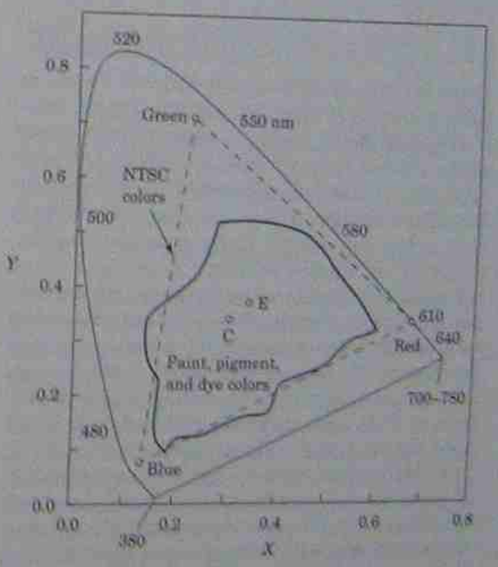


FIGURE 8.3
Maxwell's chromaticity diagram.

orimeter, which may be available only in special testing laboratories.

The periphery of the chromaticity diagram identifies each color at its *dominant* wavelength in the fully *saturated* state. **Saturated color** means vivid, rich, pure, and uncontaminated by any other influence or light. The **hue** of the color is the term used to express the dominant wavelength of the color.

In 1931, the Commission Internationale de L'Estairage, or CIE (International Commission on Illumination), selected the three primary colors for television as red at a wavelength of 0.7 μm, green at 0.546 μm, and blue at 0.436 μm. This selection was based in part on the limitations of the most efficient color phosphors available at that time. These colors, red, green, and blue, at their dominant wavelengths and degree of saturation, are shown in Figure 8.3 at the points of the triangle in the chromaticity diagram. **Primary colors** are defined as a set of colors from which all other colors may be derived and from which any two primary colors will not produce the third primary. The three primary colors found in nature and those that make up printers' ink, clothing dyes, and paint pigments are red, yellow, and blue. In nature, the sum of all colors make a deep shade of gray or black. All pigmented colors together will absorb all light wavelengths and reflect none.

8.3 ADDITIVE AND SUBTRACTIVE MIXING

These two mixing methods also take into account direct and indirect lighting effects. In nature, indirect lighting affects on color support the subtractive mixing process. Here are three examples. (1) A brilliant red rose of 0.7-μm wavelength grows in a garden. White sunlight falls on the rose, and the pigment in the rose absorbs all the color wavelengths except 0.7 μm, which is reflected; we see the 0.7-μm red rose. All the color wavelengths except red are subtracted from white by absorption and only red is reflected. (2) A second rose in the same garden is a desaturated red that appears *pink*. A red rose at 0.7 μm can appear pink by adding white. If 100 units of white light strike the rose and 20 units of green light at 0.52 μm are reflected and 20 units of blue light at 0.43 μm are reflected, the remaining 60 units are red light at 0.7 μm. Twenty units of red added to the 20 units of green and the 20 units of blue will make 60 units of white light. The remaining 40 units of red will combine with the 60 units of white and appear pink. The dominant wavelength of 0.7 μm did not change; only the degree of saturation changed. (3) An orangish-red rose may have a dominant wavelength of 0.6-μm wavelength, which makes this an entirely different hue from the red rose in cases 1 and 2. The same sequence could be repeated about full saturation and desaturation of the 0.6-μm rose, but the points have already been made. The dominant wavelength of light tells the color, and the amount of added white tells the degree of saturation. Color in nature uses the subtractive process of mixing by absorbing some of the wavelengths and reflecting the dominant wavelength. When only one wavelength is reflected, the color is fully saturated. When more than one wavelength is reflected, the color is desaturated without changing its dominant wavelength.

Video systems must create and project light. In a darkened room, a beam of finely focused red projected light appears on a screen as a spot of red color. A displaced green projected light appears as a green spot, and a blue light appears as a blue spot, as seen in Figure 8.4a. When the 3 spots of light are moved closer together, they overlap, as seen in Figure 8.4b and the overlapping areas of light add together. This demonstrates the **additive** light process of color mixing and is effective only with *direct* lighting as used in video systems. Figure 8.4b is rendered in black and white and numbered as follows:

Area 6 is a direct saturated red primary spot, area 4 is a direct saturated green primary spot, and area 7 is a direct saturated blue primary spot of light. All three primary colors combine to make white (in area 1), which supports Newton's theory and Maxwell's triangle from Figures 8.2 and 8.3.

In area 2 in Figure 8.4b, the red and green overlap and add together to form the color yellow. Yellow is opposite in the figure from the color blue. Yellow is then identified as the **complement** (opposite) of blue. Yellow becomes a secondary or complementary color.

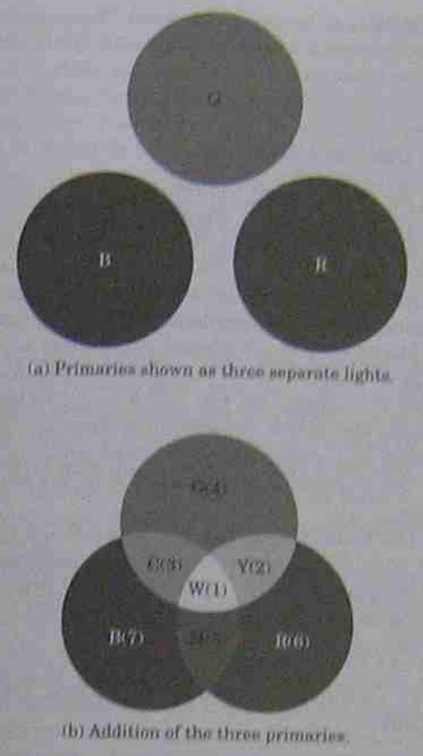
In area 3, the green and blue primaries overlap to create the color cyan, a greenish-blue color. Cyan is the complement of the color red and is also a secondary color.

In area 5, the red and blue primaries overlap to create the color called **magenta,** a purplish color. Magenta is the complement of green and is also a secondary color.

Any of the saturated primaries may be desaturated by the addition of some amount of its complementary color. A small portion of cyan added to pure red will yield a desaturated red without changing the dominant wavelength of the red color. If enough cyan is added, it will cancel the color red and yield the color white. Remember that the color cyan is the sum of green and blue and that the sum of all three primaries is white.

The three primary colors used in video systems are red, green, and blue. The secondary or complementary colors are yellow, cyan, and magenta. These six colors are the standard selection of the NTSC system and for most of the adapted systems throughout the world.

The area in Figure 8.3 chromaticity diagram that would be bounded by the points labeled blue, green, and red identifies the nonspectral colors. That is, the colors that do not have a dominant wavelength of their own, but can be developed by a mixture of the primaries. Magenta is a nonspectral color.



(a) Primaries shown as three separate lights.

(b) Addition of the three primaries.

FIGURE 8.4
Additive mixing of the three primary color lights.

8.4 STANDARD R–G–B VALUES

The letter E in Figure 8.2 is a value of white that will result when equal amounts of red, green and blue are added together. It is easy to see that this is not the standard white at C as selected by the NTSC and other standards committees. It should suggest that to arrive at the standard white, different amounts of the three primaries would be needed, which is described later.

Backtracking momentarily, you will recall that changing the bias on the CRT (difference in voltage between the cathode and control grid) changes the electron flow from the electron gun and the CRT brightness level. In color CRTs, there are three electron guns and three separate bias (brightness) controls. Adjusting the three bias controls for the individual brightness of each phosphor is part of the procedure to set up a white raster. A master brightness control is also available to the user that will change the overall brightness of the raster without affecting the settings of the ratio of the individual R–G–B bias control settings. Check your service schematic, because some systems label these *screen controls*. The bias (or screen) controls are adjusted with no video input signal.

To set the raster for what was determined to be standard white, a series of trial experiments were conducted. The details of the experiments are not essential except to say that it took time and involved many professionals from a number of competing companies. Pooling all the collected data, it was found that a standard white raster could be set when the red phosphor contributed 30% of the total brightness, the green phosphor contributed 59% of the total brightness, and the blue phosphor contributed 11%. The data were then put into the form of an equation:

$$\text{white} = 30\%\ \text{red} + 59\%\ \text{green} + 11\%\ \text{blue} \quad (8.1)$$

This equation became the cornerstone for all the principles and functional circuit blocks for the remainder of the compatible color video systems. It is suggested that you commit equation 8.1 to memory now; it will reappear many times in this chapter and in chapters to follow.

Summing up this section, Figure 8.5 is an engineering interpretation of Maxwell's chromaticity diagram. Although it takes a few liberties, it is factually correct. The center of the visible light spectrum, at 0.565 μm, is rotated counterclockwise and labeled as the 0° reference at the left side of the fig-

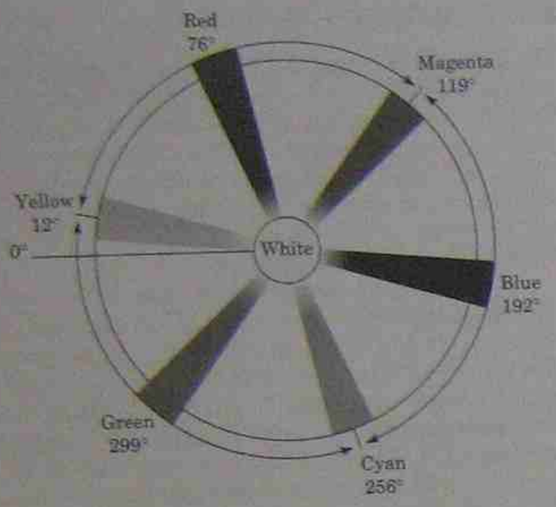


FIGURE 8.5
Engineering interpretation of the primary and secondary colors from Maxwell's chromaticity diagram.

ure. Placing the standard white at the center of Figure 8.5, each of the three primary and three secondary colors is angularly displaced from the zero reference line. The relative color amplitudes are not part of this diagram.

8.5 COMPATIBILITY

Introducing color into an already existing video system was not an easy task and took a considerable amount of time and thought. Why? Because the basic rule of the FCC required that the color system be compatible with the existing black and white system. The black and white unmodulated signal already took the full frequency range from 30 Hz to 4.2 MHz, with the frequency-modulated sound carrier at 4.5 MHz. This was the extent of the full baseband frequencies that were allowed per channel. When transmitting in color, the viewer with a color receiver was to receive the full picture in color along with the associated sound signal without changing the baseband frequency range. At the same time, the viewer with the monochrome receiver was to receive the same picture in black and white with no loss in picture quality along with the associated sound signal. When transmitting in black and white, both viewers would receive the same good quality picture in monochrome along with the associated sound signal without changing any of the control settings. The color transmission was to add three color signals without increasing the 4.2-MHz baseband frequency. This was before digital electronics became practical. Quite a task. Let's see how it was done.

8.6 COLOR CAMERA

If we cover the camera systems first, receiver discussions will be greatly simplified. The camera systems tell us all the what, how, and why in the signal development stage. Separating the signals at the receiver is then easier to understand when you see how they are put together at the transmitter.

The camera is introduced using three separate camera tubes. There are newer and faster ways to develop the signals, as you will see in Chapter 16. However, the newer processes combine several basic steps into groups of operations and therefore loose the continuity that is needed in the learning process.

The camera diagram in Figure 8.6 is broken down into six sections and will be discussed in block diagram form to define functional procedures only. Some unique circuits may be covered as they become essential.

8.6.1 Dichroic Mirrors and Camera Tubes: Section I

Light from the scene being viewed enters the camera through the lens system and is separated into three color spectra by filtered mirrors called **dichroic** mirrors. The light first strikes the blue dichroic mirror, labeled B, and reflects only the blue wavelengths of light onto a standard mirror (2) and then onto the sensing plate of the blue camera tube.

The wavelengths of light that pass through the blue dichroic mirror strike the red dichroic mirror, labeled *R*. The red wavelengths of light are reflected to another standard mirror (4) and then into the red camera tube. The remaining wavelengths of light, after the blue and red have been filtered out, pass through the red dichroic mirror and strike the green camera tube.

The three camera tubes, labeled red, green, and blue are identical tube types and are interchangeable. They get their color names from their positions relative to the dichroic mirror systems.

The NTSC color bar test pattern will be used as the camera target as found on color photo 37 in Chapter 15. This pattern contains eight color bars, the three primary colors, red, green, and blue; the three secondary colors, cyan, yellow, and magenta; plus the sum of all colors, white, and the absence of all colors, black.

In a classroom situation, the luminance signal is developed using the color sequence just described. The student is given a homework assignment to rearrange the colors in a descending order of brightness levels, name the color sequence, and draw the resulting luminance signal waveform. In a textbook situation, this will not work, so here is the color sequence in descending order of brightness:

White–yellow–cyan–green–magenta–red–blue–black

First review photo 37. Then, let's say that regardless of the actual signal voltage level from each of the three camera tubes, we will call it 100% of the output signal. We can examine any one of the 525 horizontal scan lines in the video waveform since they will all be exactly the same. The waveforms of Figure 8.6 are drawn out for you in Figure 8.7A through M.

Waveform A in Figure 8.7, the output of the blue camera tube as one line of the NTSC color bar pattern is scanned, develops as follows. The first bar, white, contains all three primary colors, so the signal level from the blue camera tube is 100% during the white bar. As the yellow bar is scanned, the blue camera tube output drops to zero, since the color yellow is a combination of red and green. Scanning the cyan color bar causes the blue camera tube to again go high (100%), because cyan is a combination of blue and green. There is no blue output as the green color bar is scanned, so the blue camera tube output will drop to zero for this color bar. There is blue in the color bar magenta, because it is a mix of red and blue, so the blue camera tube output is high again (100%). There is no blue in the makeup of the red color bar, so the blue camera output again goes to zero. There is only the color blue as the blue color bar is scanned, so the blue camera tube output goes to 100% again. The last color bar, black, represents the absence of all color, and the blue camera tube output again goes to zero.

The horizontal blanking pulse and sync signals are then added (not shown) before the next line of video is scanned. This is a fixed test pattern, so the next scan line out of the blue camera tube is a repeat of waveform A.

We now look at the output of the red camera tube for the same NTSC color bar pattern to develop waveform B. This is done by using the same logic as applied to the blue camera tube output, but using fewer words. There is output from the red camera tube for the first two color bars (white and yellow), so waveform B is high (100%) for these two colors. There is no red in the makeup of the color bars cyan and green, so waveform B goes to zero for these two bars. There is red in the makeup of the two color bars magenta and red, so the red camera tube output is high (100%) for these two color bars. No red is needed for the last two bars, blue and black, so waveform B will be zero as these two bars are scanned.

Waveform C, the output of the green camera tube, is even simpler. The color green is needed to make up the colors white, yellow, cyan, and green. The output of the green camera tube is high (100%) while scanning the first four color bars. Green is not needed to make up the colors magenta, red, blue, or black, so waveform C out of the green camera tube is zero for the last four color bars in the NTSC color bar test pattern.

Notice that waveforms A, B, and C resemble the output signals of three, divide by 2, flip-flops in a decade down counter.

8.6.2 Luminance Signal

Section II of Figure 8.6 utilizes three resistive voltage-divider sets with the output voltage in all cases appearing across R_1 as waveform D. Resisters R_2 and R_1 supply 11% of the blue camera tube output signal across R_1. Working with resisters R_3 and R_1, an output of 30% of the red camera tube signal is developed across R_1. Resisters R_4 and R_1 supply 59% of the green camera tube output signal across R_1. The sum of the voltages makes up waveform D, the luminance signal.

As the camera scans the white bar of the NTSC color bar pattern, we can see from waveforms A, B, and C in Figure 8.7 that there is an output from all three camera tubes. Eleven percent of the blue camera tube signal plus 30% of the red camera tube signal plus 59% of the green camera tube signal appear simultaneously across R_1. The three voltages add together to yield a 100% signal across R_1 for the color white. Review equation 8.1.

As the second color bar (yellow) is scanned, the blue camera tube output has gone to zero, but the red and green camera tube signals remain high at 100%. Through the resistive voltage dividers, 30% of the red signal is added to 59% of the green signal to supply an 89% signal across R_1 as the second level in the luminance signal waveform D for the color yellow.

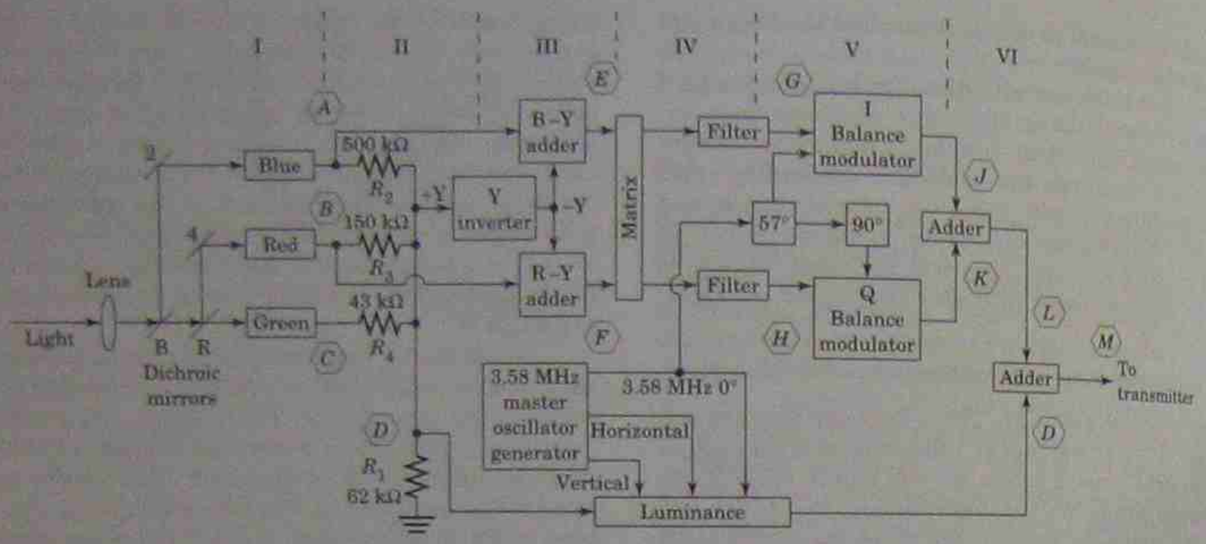


FIGURE 8.6
Block diagrams of a color TV camera.

For the third color bar, cyan, waveform A is high, B is low, and C is high. The voltage dividers reduce the A signal to 11% of maximum and the C signal to 59% of maximum, for a total of 70% signal level for the color cyan in waveform D.

Waveform C is the only camera output that is high as the green color bar is scanned, and it contributes 59% to the voltage in waveform D of the luminance signal.

Scanning the magenta color bar, the blue output (waveform A) is high and contributes 11% to the luminance. The red output (waveform B) is also high, adding another 30% to the luminance, totaling 41% of the luminance signal in waveform D.

Only the red camera tube has output during the scanning of the red color bar, so the luminance signal level is 30% for red.

Only the blue camera tube has output as the blue color bar is scanned, which places 11% in the luminance waveform D.

The color black is the absence of all color light, as shown in waveforms A, B, and C, which makes the voltage of waveform D equal to zero-level luminance for the color black.

It may seem redundant at first to separate the video signal into three color signals and then add them back together again to form the luminance signal. However, it makes sense when you realize that the luminance is the video signal transmitted to viewers with monochrome receivers. This leaves the three color signals to work with for viewers who have color receivers.

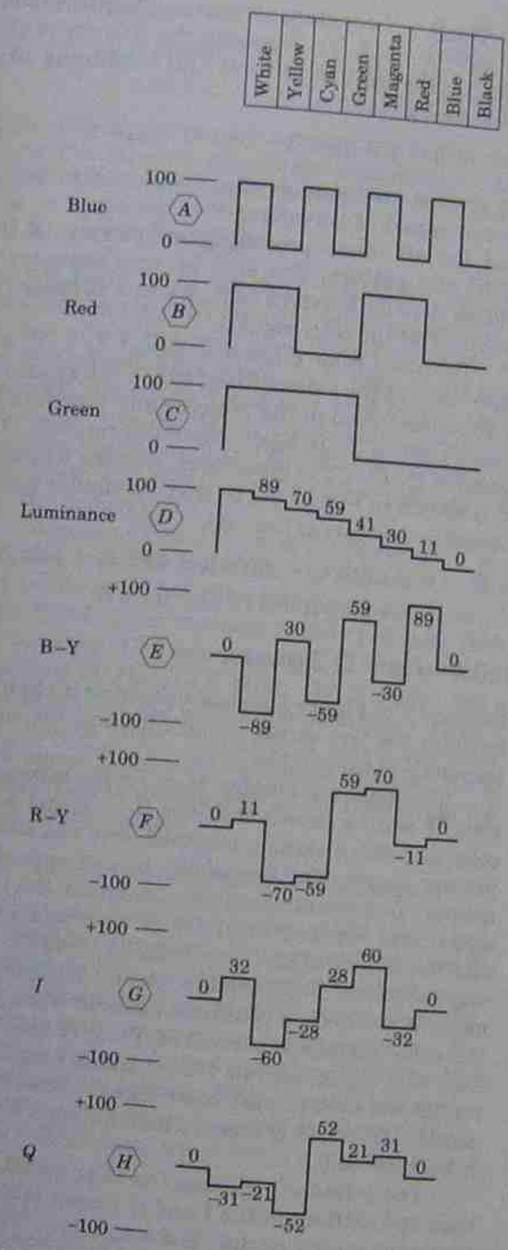
8.6.3 Color Difference Signals

The luminance signal is used in two places. Waveform D is amplified by the luminance video amplifiers to be added to the chroma signals in section VI of Figure 8.6. It is also inverted and added to the camera tube output signals in section III. In this case, we use the letter Y for the luminance signal. The Y inverter can be said to have $+Y$ as an input signal and $-Y$ as an output signal. Any circuit that changes phase by 180° can be used as an inverter, a common-emitter amplifier, an inverting op-amp and a transformer are all examples of inverters.

From equation 8.1, we learned that the luminance signal (or Y signal) is the sum of 30% red, 59% green, and 11% blue. This shows that more than half (59%) of the luminance signal is green. It was reasoned that only two color signals (instead of three) need be transmitted. At the receiver, if the 30% red and the 11% blue signals are inverted to −30% red and −11% blue, they can be subtracted from the luminance signal to recover the 59% green color signal.

In section III of Figure 8.6, 100% of the blue camera signal (waveform A) is added to the inverted Y signal, with an output called the B minus Y (B − Y) shown as waveform E. When 100% of the red signal is added to the inverted Y signal, the R minus Y (R − Y) signal results and is seen in waveform F. The B − Y signal is written in equation form as

$$B - Y = 100\%\ B - (30\%\ R + 59\%\ G + 11\%\ B)$$



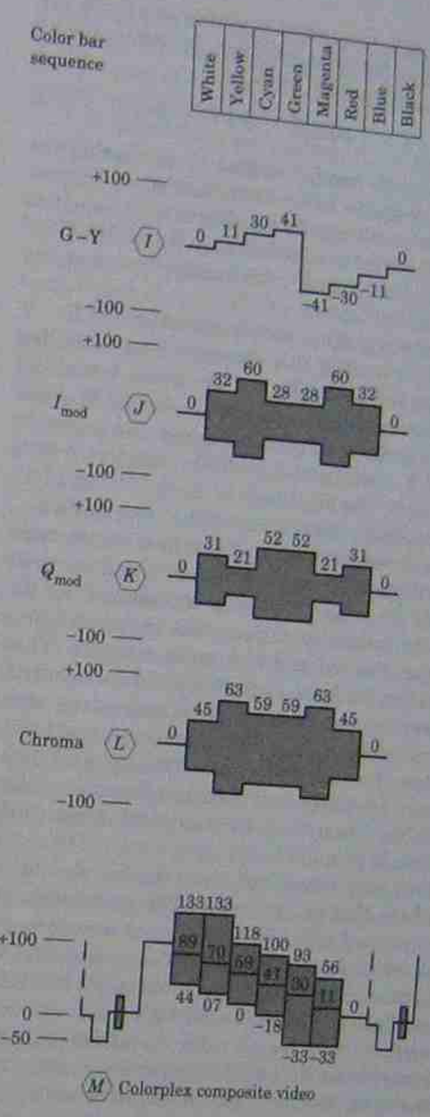


FIGURE 8.7
Waveforms in a color camera chain at designated locations using the NTSC color bar test pattern.

The minus sign changes the polarity of all the values inside the parentheses. Then, by combining all like terms, the equation reads as

$$B - Y = -30\% R - 59\% G + 89\% B \quad (8.2)$$

All color signals can be verified by comparing the sum of the negative terms to the sum of the positive terms. The result should be algebraically equal to zero: −30% added to −59% cancels the +89%. However, individually, each color voltage has meaning and performs a function.

When using equation 8.2 to develop the B − Y waveform E, we find that the color white contains red, green, and blue. The positive terms cancel the negative terms for zero output amplitude. The yellow bar is generated by blending red and green. In the B − Y waveform E, −30% added to −59% makes −89%. The amplitude of the B − Y signal for the color yellow is shown as −89% in waveform E.

The process continues for each of the remaining color bars of the test pattern by the same principle used for yellow. To verify waveform E for the rest of the colors, remember that green and blue make cyan and red and blue make magenta. Then use equation 8.2 for the amplitude of each color bar. Take into account that the amplitude is the algebraic sum of the values. For cyan (green and blue), the value of −59% added to +89% equals +30%. When you get to the last color bar, remember that black is the absence of all color, with a resulting amplitude of zero.

Two very important observations should be noted here that apply for all color waveforms: (1) There is zero amplitude in each color waveform for the colors white and black. White is supplied by the luminance signal D as noted to be 100% for white. Black is the absence of all color and will therefore be zero for all color waveforms. (2) All color waveforms in the NTSC color bar pattern are symmetrical. The right half is the inverted mirror image of the left half. Start at both ends and work toward the center. Waveform E starts and ends with zero amplitude. The second bar is −89% on the left and +89% on the right. The third bar on the left is +30% compared to −30% for the third bar on the right, and the two center bars are −59% and +59%.

The R − Y signal is developed in exactly the same manner as was the B − Y signal. Take 100% of the red camera tube signal and add to it the inverted luminance signal. This becomes the R − Y signal shown as waveform F. The B − Y and R − Y signals are called the color **difference** signals.

The R − Y equation sets up as 100% R − (30% R + 59% G +11% B). Changing the polarity of the terms inside the parentheses and combining like terms, we have

$$R - Y = 70\% R - 59\% G - 11\% B \quad (8.3)$$

The process needed to develop the R − Y color difference signal of waveform F is the same as was used for all other preceding waveforms in the NTSC test pattern. The step by step sequence is omitted here for brevity's sake. Be sure to check the two rules for the color signals.

The third color difference signal, G − Y, was never used at the transmitting end of the system. It is sometimes used in the receiver and therefore becomes part of your basic color information. The equation for G − Y is given here, and the waveform (I) is shown in Figure 8.7 so that all similar data is located in one part of the text.

$$G - Y = 100\% G - (30\% R + 59\% G + 11\% B)$$
$$= -30\% R + 41\% G - 11\% B \quad (8.4)$$

8.6.4 *I* and *Q* Signals

Section IV of Figure 8.6 shows the *matrix* block and includes the two series signal filters at the output terminals of the matrix.

The matrix is another term for the mixing section. It can be shown that the B − Y and R − Y color difference signals overmodulate the station's picture carrier farther along in the camera sequence. To prevent this overmodulation, the R − Y signal was reduced to 87.7% of its original value and the B − Y signal was reduced to 49.3% of its original value. Furthermore, easier manual alignment of the system could be achieved when one of the color signals represented FLESH tones. The flesh tone signal became known as the *I* signal, and the second counterpart color signal became the *Q* signal. The *I* and *Q* signals take on more meaning in Section 8.6.5.

The action of reducing the color signal amplitude and shifting to the *I* and *Q* format takes place inside the matrix circuit. The *I* signal is

$$I = 0.74(R - Y) - 0.41(B - Y)$$

Substituting equation 8.2 for the R − Y and equation 8.3 for the B − Y quantities, multiplying out, and combining like terms, the *I* equation becomes

$$I = 60\% R - 28\% G - 32\% B \quad (8.5)$$

This equation is then used to construct the *I* waveform (G).

The *Q* signal is generated as

$$Q = 0.48(R - Y) + 0.41(B - Y)$$
$$= 21\% R - 52\% G + 31\% B \quad (8.6)$$

The *I* and *Q* signals are constructed in the same manner as all other waveforms. Remember to apply the two basic laws for color waves.

8.6.5 Color Area Size

The eye plays funny tricks on the mind. Large areas of red, green, and blue are easily recognized. If the size of the red color area is made smaller, we can distinguish this down to a very small size. However, the colors green and blue do not share this same property. When the areas of green and blue become smaller, it is difficult to tell green from blue. When the area is made still smaller, green and blue appear gray.

Because of this color size relationship, it was concluded that the bandwidth of the color signals need not be as wide as the luminance signal bandwidth. The *I* signal contains mainly red color (60% from equation 8.5) and is limited to the frequency range from 30 Hz to 1.5 MHz. The *Q* signal has a small amount of red (21% from equation 8.6), so it must contain larger amounts of green and blue. The *Q* signal bandwidth is limited from 30 Hz to 0.5 MHz. This is the function of the filters that follow the matrix section.

8.6.6 Quadrature Balanced Modulation

You may recall from your earlier study that a balanced modulator requires two input signals, as do all modulators. The carrier signal is the higher frequency of the two signals, and the modulation message signal is the lower of the two frequencies. The balanced modulator output signal is a double-sideband suppressed carrier (DSSC) amplitude-modulated wave. An example is shown in Figure 8.8 using a 3.6-MHz sine wave for the carrier signal

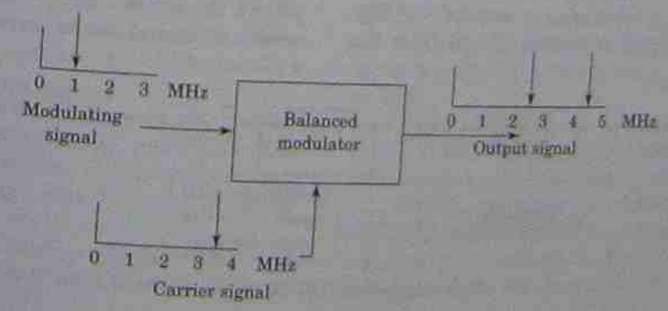


FIGURE 8.8
Balanced modulators produce the upper and lower sidebands only; there is no output at the carrier frequency (DSSC).

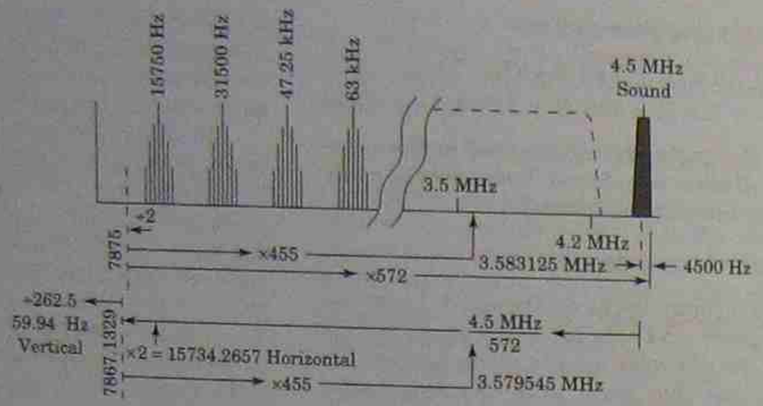
frequency and 1.0 MHz for the modulating signal frequency. The balanced modulator cancels the carrier frequency and outputs only the two side frequencies of 2.6 and 4.6 MHz.

In quadrature modulation, there are two balanced modulators, and both have the same carrier input frequency. In section V of Figure 8.6, the two modulators have an input frequency of 3,579,545.455 Hz. At first sight, this may seem like a strange selection for a carrier, but, as will be seen, it was chosen with a great deal of care.

The frequency response of the luminance signal is known to cover the full frequency range from 30 Hz to 4.2 MHz. It was also known that the sidebands of the modulated color signals should have a suppressed carrier about 600 kilohertz (kHz) lower than the highest video signal frequency. 4.2 MHz − 0.6 MHz = 3.6 MHz.

From very early spectrum analysis, the luminance signal was seen to have clusters of energy at all multiples of the horizontal scanning frequency (15,750 Hz). Figure 8.9 shows that each cluster of energy has diminishing sidebands of energy spaced 30 Hz apart above and below the horizontal rate. Figure 8.9 also shows that there are spaces between each energy cluster where no signal exists. It is in these spaces that the modulated color signals could be placed without interfering with the luminance signal. The spaces are at all *odd* harmonics of one-half the horizontal line frequency of 7875 Hz. A 3.6-MHz color signal would fall near the 457 odd harmonic of 7875 Hz. After several trials, it was found that the 455 odd harmonic of 7875 Hz yielded the minimum interference with the luminance signal. This frequency is then 455 × 7875 Hz = 3.583125 MHz. However, the 572 odd harmonic of 7875 Hz was 4.5045 MHz, which caused a disturbing buzz in the 4.5-MHz sound channel. Two options are open for correction of this buzz problem: (1) change the sound carrier to 4.5045 MHz and realign 50 million television receivers in the cus-

FIGURE 8.9
Clusters of energy at all multiples of the horizontal frequency used to select the color subcarrier frequency.



tomers' homes, or (2) change the horizontal scanning frequency. The latter was the option of choice. Follow this in Figure 8.9. The 572 submultiple of 4.5 MHz is 7867.1328 Hz, as half of the horizontal line frequency, and 2 × 7867.1328 Hz is 15,734.265 Hz, as the new horizontal scanning frequency. Then 15,734.265 Hz divided by 262.5 = 59.94 Hz, as the new vertical scanning frequency. The color subcarrier frequency can then be determined as 455 × 7867.1328 = 3.579545455 MHz. In general discussion, we call this 3.58 MHz.

The horizontal and vertical frequencies are so dependent on this color subcarrier frequency that, at the transmitter, all four signals are often derived from one master oscillator. Figure 8.10 shows one possibility of achieving this condition. The crystal-controlled master oscillator of 28,636,363.64 Hz is divided by 8 for the color subcarrier signal. The master oscillator signal is divided by 910 for the vertical serration pulse signal, which is split to divide by 2 for the horizontal frequency of 15,734.265 Hz and by 525 for the vertical frequency of 59.94 Hz. The four output signals from the oscillator need waveshaping circuits and time-delay circuits, which are not shown in Figure 8.10. The vertical and horizontal signals are also used for scanning the three camera tubes in Figure 8.6.

The *I* balanced modulator in section V of Figure 8.6 gets a 3.58-MHz carrier signal from the master oscillator that is shifted by 57° from the color burst phase to represent the flesh tone carrier. The *I* color signal amplitude modulates the 3.58-MHz, 57° carrier to produce the modulated *I* signal shown in Figure 8.7J. Waveform J is the modulated sidebands of the suppressed carrier signal. This is standard modulation for which the *I* signal amplitude sets the level of the modulated output signal. Note that the green and magenta (for example) have the same amplitude in the modulated wave, but are different in the unmodulated wave. Both colors have the same signal strength, but are 180° out of phase before modulation. After modulation, you see the positive and negative swing of the sidebands that are 180° out of phase between green and magenta.

The *Q* balanced modulator in section V of Figure 8.6 functions in exactly the same manner as the *I* balanced modulator, with two exceptions. The first and obvious difference is that the input signal is the H waveform *Q* signal. The second and most important difference is that the phase of the 3.58-MHz carrier to the *Q* modulator is shifted another 90° beyond the *I* carrier for a total of 147° from the burst phase. The letter *Q* here is used to identify **quadrature** modulation as two carriers at the same frequency and 90° out of phase. Figure 8.11a shows the normal two-dimensional presentation of a sine wave and cosine wave with 90° phase separation. Figure 8.11b shows the *I* and *Q* carrier signals in a three-dimensional plane separated by 90° that allows them to co-exist in the same circuit as individual signals without mixing together. The most valuable feature of Quadrature carriers is that they may be added together at the transmitter and easily separated at the receiver.

FIGURE 8.10
One crystal-controlled master oscillator to develop four frequency-related camera signals

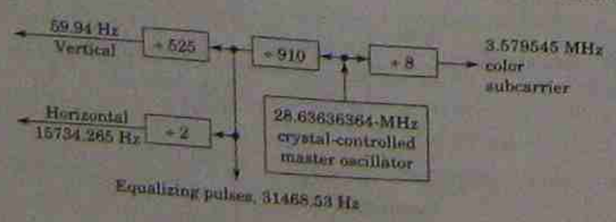
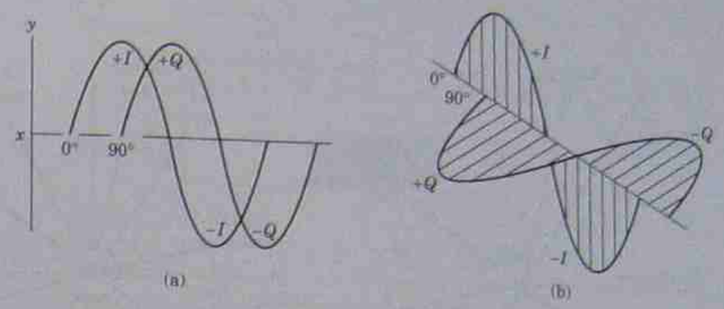


FIGURE 8.11
Quadrature modulation carrier phase relationships.



8.6.7 Chrominance

Section VI of Figure 8.6 has two simple adder circuits. The first adder combines the modulated I signal and the modulated *Q* signal. The output of this adder is the **chrominance signal,** shown as waveform L in Figure 8.7, and it has both amplitude and phase. Chrominance is the name given to the signal when the modulated *I* and modulated *Q* signals are added together. It is often abbreviated as chroma.

The amplitude of the individual color voltages in the chroma signal are the vector sum of the voltages for that color as found in the *I* and *Q* signal, waveforms G and H. These waves are used because they show amplitude and polarity. The amplitude is found by the Pythagorean theorem, which states that the vector length is the square root of the sum of the squares of the voltages for that color in the two applied voltages.

$$\text{length} = \sqrt{I^2 + Q^2} \qquad (8.7)$$

Examine Figure 8.12a to establish that the zero reference is on the *X* axis to the left of center. The $+I$ vector is advanced 57° clockwise from zero, and the $+Q$ vector is advanced another 90° clockwise for a total of 147°.

Hint: a fast way to do color waves and vectors is to work with the three primary colors and then recall from past readings that the three secondary colors are of equal length but 180° out of phase from their complement.

The color red is seen to have $+0.6I$ and $+0.21Q$. The vector length is then found as 0.63, or 63% of peak chroma. The color phase is found by the tangent expression.

$$\theta \text{ red} = \arctan \frac{\text{opposite}}{\text{adjacent}} \qquad (8.8)$$

In this step, you need to decide whether you want to use the *I* signal or the *Q* signal as the reference. The reference will be the side adjacent to the angle in question. In the solution for red, using the a angle in Figure 8.12a, the adjacent side is the *I* reference. The angle becomes

$$\theta \text{ red} = \arctan \frac{0.21}{0.6} = 19.3°$$

Since this angle is measured from the *I* reference, it must be added to the 57° of the *I* signal angle: 57° + 19.3° = 76.3°. We conclude then that the red vector voltage has a magnitude of 63% of the maximum chroma signal at an angle of 76.3°. Cyan is the complement of red and has the same amplitude as red, but is 180° out of phase, or 76.3° + 180° = 256°.

The color blue has voltages of $-0.32I$ and $+0.32Q$. Its vector length is 0.4455 (44.55% of peak chroma signal). Its angle is the arc tan of 0.32 divided by 0.31 = 45.9° from the $+Q$ reference. Add 45.9° to 147° for 192.7°.

Yellow is the complement of blue and therefore has a magnitude of 0.4455 at an angle of 12.7°.

The color green is represented by $-0.28I$ and $-0.52Q$. The vector length of green is 0.59 and its vector angle is 61.7° from the $-I$ reference: 237° + 61.7° = 298.7°.

The complement of green is magenta with the same length but opposite phase. Magenta is 0.59 at 119°.

Figure 8.12b shows the vectors for the three primary and three secondary NTSC colors each at its respective angle and magnitude.

The second adder in section VI of Figure 8.6 adds the chroma signal (waveform L) to the luminance signal (waveform D). Waveform D sets the dc voltage level for the brightness of the color bar at

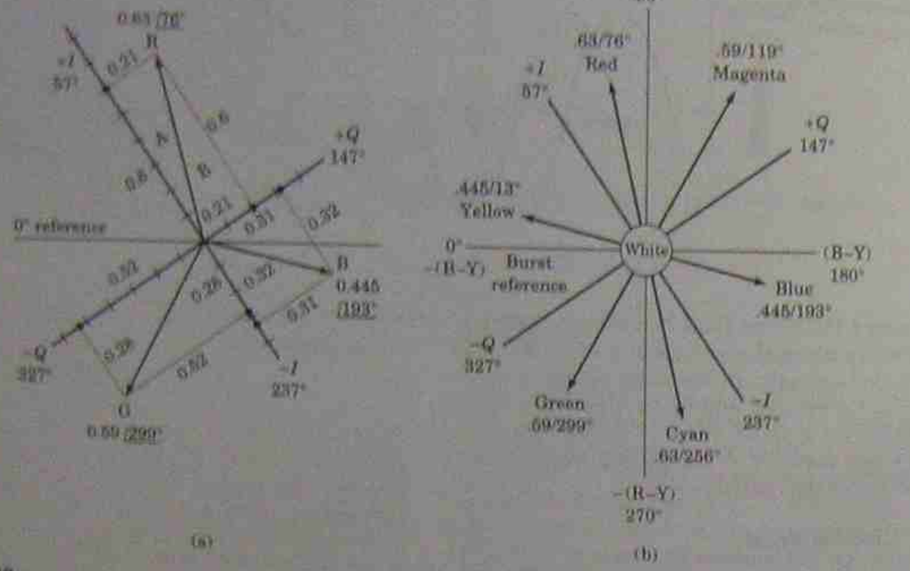


FIGURE 8.12
The vector solution for the phase angles of the NTSC color bars: (a) solution for the primary colors; (b) final placement and magnitude of the NTSC primary and secondary color vector voltages.

that location. In waveform L, yellow has an amplitude change ±0.45 from zero. In waveform M, yellow changes ±0.45 around the dc level of 0.89 of the luminance signal. Each modulated color has a specific dc level in the output of the second added. This total video signal is called the **colorplex composite video** signal. This signal is sent to the station's AM transmitter for modulation of the picture carrier. Figure 8.13 is an oscilloscope photograph of two cycles of the NTSC color bar test pattern.

8.7 COLORPLEX FREQUENCY SPECTRUM

Figure 8.14 sums up the combination of the black and white video signal along with the color signals as they are added to the frequency spectrum of the luminance signal without violating the frequency limitations of required baseband definition. The system is totally compatible.

Figure 8.14a is the response of the *I* signal that is applied to the *I* balanced modulator. It is held to a range from 30 Hz to 1.5 MHz. The output of the *I* balanced modulator contains only the sidebands of modulation with the 3.58-MHz carrier suppressed. The lower sideband extends down to 2.08 MHz (3.58 − 1.5 MHz), and the upper sideband reaches to 5.08 MHz (3.58 + 1.5 MHz). Both

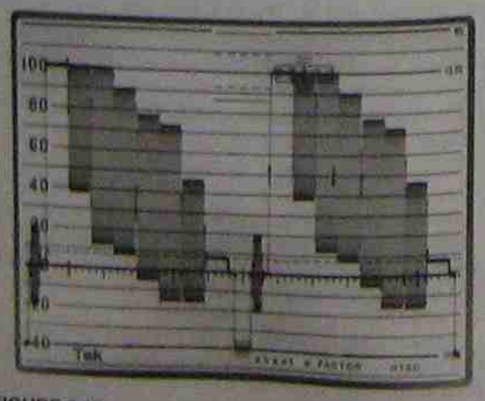
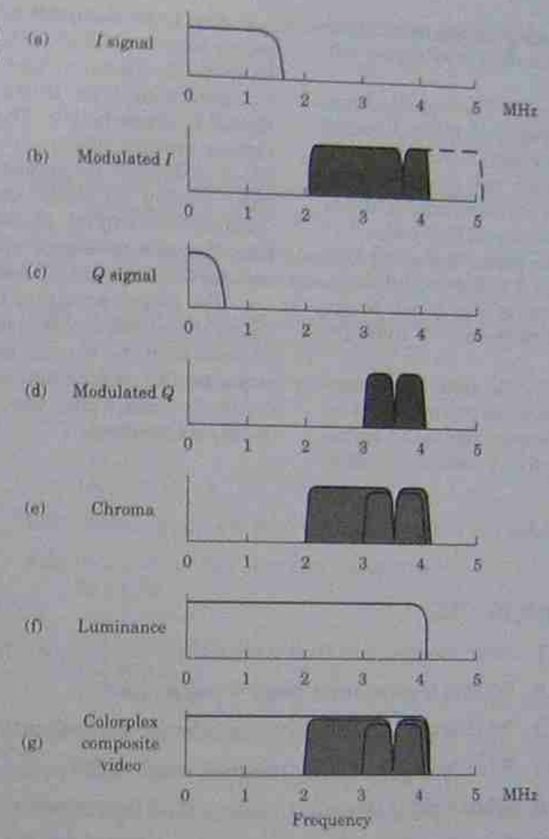


FIGURE 8.13
Oscilloscope pattern for two lines of the NTSC color bar test pattern voltage wave (Courtesy of Tektronix, Inc.)

FIGURE 8.14
The frequency response of the luminance and the two color signals, I and Q.



sidebands contain the same information, but because the video signal cannot exceed 4.2 MHz, the upper sideband is again filtered to hold the high end frequency to 4.2 MHz. This form of sideband control is called **vestigial** sideband transmission and does not change the quality of the sideband information. Vestigial sideband means to send one full sideband and part of another sideband. Either sideband may be restricted.

The *Q* signal into the *Q* balanced modulator is held to the frequency range from 30 Hz to 0.5 MHz by the filters. Because the *Q* signal contains mainly green and blue, its bandwidth need not be as broad as the *I* signal, which contains mainly red.

The output of the *Q* balanced modulator, from Figure 8.14d, has the lower sideband down to 3.08 MHz (3.58 − 0.5 MHz) and the upper sideband to 4.08 MHz (3.58 + 0.5 MHz) with the 3.58-MHz carrier suppressed.

The chroma signal is the modulated *I* signal and the modulated *Q* signal vectorially added together. Figure 8.14e shows the frequency response of the chroma signal in the band from 2.08 to 4.2 MHz.

Figure 8.14f is the frequency band of the luminance signal from 30 Hz to 4.2 MHz, which contains all the fine picture detail in the transmitted signal.

Figure 8.14g is the combined chrominance and luminance signals previously identified as the colorplex composite video signal. Because the modulated chroma signal lies at the odd harmonics of half the line frequency, there is minimum interference between the two signals, even though they occupy the same frequency range.

8.8 SUMMARY OF THE COLOR CAMERA FUNCTIONS

A great deal of information has been presented in this chapter on color. Because of the amount of de-

tail necessary to describe each function, some of the details may be difficult to recall. A brief review will put things in perspective.

Light enters the camera and is separated into three light bands for application to three identical camera tubes. The tubes get their names from the band of light that they receive, red, green, or blue. Appropriate amounts of each camera output signal are used to make up the luminance (Y) signal.

The inverted Y signal is added to the full blue camera signal to develop the B − Y color difference signal. The inverted Y signal is also added to the full red camera signal to form the R − Y color difference signal.

The B − Y and the R − Y signals are converted to the I and Q signals to control overmodulation and set one of the reference phases to represent the flesh tones. The mixing section is called the matrix.

The I and Q signals are amplitude modulated onto a suppressed 3.58-MHz carrier in two separate balanced modulators. The carrier signal to each balanced modulator is the same frequency, but shifted in phase by 90°. The two modulator output signals contain sidebands only at a quarter-cycle phase difference for quadrature modulation. The letter I infers "in phase" carrier and Q represents "quadrature" carrier phase. The I carrier is 57° from the zero reference burst (color sync) signal, and the Q carrier is 147° from zero.

The output signals of the two balanced modulators are added together for the chrominance signal, and then the chroma signal is added to the luminance (Y) signal to make up the colorplex composite video signal that goes to the AM picture carrier transmitter.

QUESTIONS

8.1 State the two basic laws of physics uncovered by Sir Isaac Newton.

8.2 What is the frequency range of visible light?

8.3 What is the unit of measurement for light wavelength?

8.4 What is the wavelength range for visible light?

8.5 White light is the _____ of all light wavelengths.

8.6 The color black is the _____ of all visible light wavelengths.

8.7 Define the term *saturation*.

8.8 Define the term *hue*.

8.9 What are the three primary colors used in television?

8.10 What are the three primary colors used in nature?

8.11 Name the two types of color mixing.

8.12 Which type of color mixing is used in video systems?

8.13 Name the three complementary colors used in television.

8.14 Identify which secondary color is a complement to each television primary color.

8.15 Write the equation for the NTSC standard white in terms of the television primary colors.

8.16 Which controls are adjusted to set up a standard white raster?

8.17 The white raster is set up using
(a) a standard good quality picture, or
(b) no video signal applied.

8.18 How many color signals are transmitted along with the luminance signal?
(a) 1,
(b) 2,
(c) 3,
(d) 4,
(e) 5

8.19 Name the colors in the NTSC color bar test pattern in a descending order of brightness, from left to right.

8.20 When scoping color signal waveforms of the NTSC color bar test pattern, which color bars contain no color information?

8.21 What is the second characteristic to look for when viewing color bar test signal waveforms in the NTSC system?

8.22 What is the algebraic sum of all the colors in the NTSC color bar test signals?
(a) zero,
(b) 50%,
(c) 75%,
(d) 100%

8.23 What signals are used to generate the B − Y color signal?

8.24 What is another name for the matrix?
(a) adder,
(b) inverter,
(c) subtracter,
(d) mixer,
(e) modulator

8.25 What is the bandwidth of the I signal?

8.26 What is the bandwidth of the Q signal?

8.27 What is the bandwidth of the modulated I signal?

8.28 What is the bandwidth of the modulated Q signal?

8.29 What input signal(s) is required for the balanced modulator?

8.30 What is the form of the modulated output from a balanced modulator?

8.31 What single feature identifies the I balanced modulator?

8.32 What single feature identifies the Q balanced modulator?

8.33 What is the name of the modulation system that uses an I balanced modulator and a Q balanced modulator?

8.34 What is the single most valuable reason for using the type of modulation described in the previous Question?

8.35 At what point in the circuit (by name) would you look for the I and Q signals?

8.36 At what point in the circuit (by name) would you look for the modulated I and modulated Q signals?

8.37 How does the chroma signal differ from the I and Q signals?

8.38 What two signals make up the colorplex composite video signal?

8.39 What is the amplitude and phase angle (compared to zero reference) of a color with an I signal of −0.6 and a Q signal of −0.21?

8.40 What color is represented by the vector of the previous Question?

8.41 What is the amplitude and phase angle (compared to zero reference) of a color with an I signal of 0.28 and a Q signal of 0.52?

8.42 What color is represented by the vector of the previous Question?

8.43 What is the amplitude and phase angle (compared to zero reference) for the color gold when the I signal is 0.45 and $Q = -0.23$?

8.44 What is the amplitude and phase angle (compared to zero reference) of the color brown when $I = 0.525$ and $Q = 0.29$?

9 Video Monitors

9.1 INTRODUCTION

To this point, you have been introduced to the structure of a video display. You found out what is needed to produce a raster and how the video intelligence modulates the CRT electron beam to develop a picture. Besides the principal theories, you were shown individual circuits that perform the intended functions, and you learned the composition of the signals that may be found in each case. The term *video* is intended to include analog picture information or computer-generated digital data. Now, let's put these ideas to work in a practical system.

The low-frequency circuits of television receivers (after the demodulator) can and will be the same as the circuits found in a computer monitor. Therefore, although the term *monitor* is used in this chapter, the discussion is equally applicable to the video amplifiers of a television receiver.

9.2 MONOCHROME MONITOR BLOCK DIAGRAM

The block diagram of any system is used to report the functions of the system and the order of events as they relate to each other within the system. The circuits are different from one product to another and will continue to change as long as people develop new ideas and devices. But the *functions* of the circuits will remain the same for as long as the system is in demand.

Figure 9.1 is the block diagram of a monochrome video monitor and the low-frequency section of a typical television receiver (excluding the sound section). Study this diagram with care until you can draw one like it from memory. Although there can be some variations, the basic diagram has all the necessary information for practical use. Remember to include arrowheads on the lines that join the blocks together so that there is no question concerning the direction of signal movement.

The input signal to a monochrome video monitor is about 1 $V_{p\text{-}p}$ with negative sync pulses (positive picture phase). This is a standard signal condition, so any brand of monitor can be used in any system. The video input signal to the same low-frequency circuits of a television receiver ranges from 0.5 to 6.0 $V_{p\text{-}p}$. The difference here is that the television receiver gets its input signal from the front end (high-frequency circuits) of the receiver and does not require interchanging with any other signal source; it is a complete package within itself.

The video amplifier output signal to the CRT of the monitor averages about 40 to 50 $V_{p\text{-}p}$. Almost all monitors have the video information applied to the cathode of the CRT, which means that the signal has positive sync pulses (negative picture phase polarity) at this point. When the product you are working with has the video signal applied to the control grid of the CRT, the polarity of the signal is reversed, but the peak-to-peak level is the same for both cases. In the case of television receivers, the peak-to-peak signal level to the CRT averages around 100 V. The signal polarity to the cathode or control grid is the same as for the monitors, with the cathode connection as the most common.

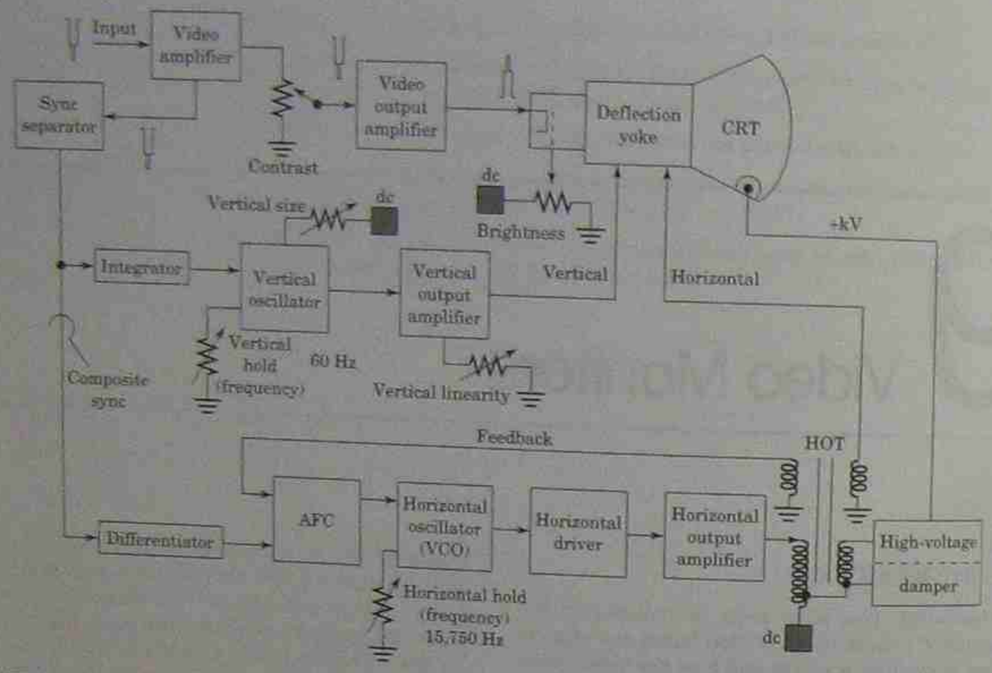


FIGURE 9.1
Typical monochrome video monitor block diagram.

9.2.1 Video Amplifier Functions

The video amplifiers in both applications need an overall gain of about 50. The video monitor may have more amplifying sections because of the wider frequency response of 15 megahertz (MHz) used in 80-column word processors as compared to the 4.2-MHz bandwidth used in consumer television. The gain–bandwidth product predicts a lower gain per stage for wider frequency response amplifiers. The oscilloscope must be used to measure the signal voltage levels that are indicated on the schematic diagram. They are given in peak-to-peak values and you will need to observe polarity. Remember to turn the contrast control to maximum signal when measuring these voltage levels.

The first video amplifier has a typically low gain of about 3 or 4. Its prime function is to supply a strong enough signal to operate the class C sync separator amplifier. The signal polarities are already set by the manufacturer, so you must observe and determine if the measured signals compare favorably with the waveforms given on the schematic diagram. The sync signal takeoff point will *always* be before the contrast control. You do not want the video signal to the sync separator to change amplitude when the contrast control is adjusted.

The contrast control sets the level of video signal to the CRT, while the brightness control adjusts the intensity of the raster by controlling the dc bias on the CRT.

The video output amplifier achieves the gain for a signal that drives the CRT to a rich contrast level. The word *output* is used to indicate the *last* amplifier in that section, such as video output, vertical output, horizontal output, or audio output. The output amplifier is often, but not always, a power amplifier, as compared to a voltage amplifier (see Appendix B).

It is only this chain of amplifiers that you will investigate when a standard good video input signal is applied to the system but does not appear on the face of the CRT or appears in a weak or washed out condition.

9.2.2 Sync Separator Functions

Chapter 7 does a thorough job of explaining the functions of the sync separator, so it would be redundant to repeat that information here. Note, however, that Figure 9.1 shows the location of the sync separator in an overall system. This includes the video input and the composite sync output that is fed in parallel to the two filters that separate the vertical sync from the horizontal sync signals. The integrator (vertical) and the differentiator (horizontal) filters are considered to be part of the sync separator circuit. See Section 9.4.2 for circuit details.

9.2.3 Vertical Deflection

The vertical deflection section of Figure 9.1 is a totally self-contained subsection of any monochrome monitor or television receiver. The vertical hold control brings the oscillator frequency to within range so that the input sync signal may control the exact timing of the oscillator to be in line with the sync pulse source. Refer to Chapter 3 for vertical details and Chapter 7 for sync pulse relationships.

9.2.4 Horizontal Deflection

Several points need to be reinforced while looking at the monitor's horizontal section. This, too, is a self-sustaining subsection and will be similar in many respects to any other horizontal deflection section that you will encounter, regardless of whether the display is a monochrome monitor or television receiver. The input sync signal is needed only to keep the cycle start time of the receivers deflection oscillators in step with the source of the video signal.

The facts that should be recalled at this time are as follows:

1. When the oscillator signal fails to reach the horizontal output transformer (HOT), there will be no high voltage to initiate a raster.
2. The oscillator will work without the AFC circuit or the sync signal input, but will be unstable in frequency.
3. The entire horizontal deflection section is basically a phase-locked loop.
4. The +kV (kilovolt) high voltage level will depend on the size of the CRT in use.
5. The feedback pulse from the HOT to the AFC circuit will later be used for other circuits as well as this one. They are the automatic gain control (AGC) and the color sync signal in television receivers.

Review Chapter 4 as needed to support these statements.

9.3 LOW-VOLTAGE POWER SUPPLIES

All electronic circuits are powered by a dc power source, either a battery or an ac power line converter. No signal circuit will function without a dc power supply. Since power supplies are studied in basic circuit analysis, they will, in general, be omitted from this text.

It is true that the power supply is as much a part of the system as any other functional circuit, but you will not find them in diagrams such as Figure 9.1 or isolated circuits as presented in earlier chapters. We know that they must always be there. The only place that power supply circuits will be found are at the system schematic level, where they will be discussed with reference to the troubleshooting process. Special cases such as voltage doublers and triplers or boosted B+ circuits are the exception. All other diagrams will use the shaded square (■) to indicate a dc voltage connection. There will be no special section on dc power supplies in this text, except this paragraph.

9.4 MONOCHROME MONITOR SCHEMATIC DIAGRAM

Everyone's first exposure to an oversized schematic can be a scary experience. If Figure 9.2 is such a break-in exposure, we can take it one step at a time to ease the agony.

First, all large schematics are laid out on a grid system of sections. Sections 1 through 8 are labeled across the top of the diagram, and sections A through F are indexed vertically along one margin. For example, the video input terminals are located in Figure 9.2 at 3B. Find this point before continuing.

Second, all large schematics separate the individual circuits by group numbers. In Figure 9.2, all video components are in the 100s group, such as R_{101} and R_{102}. All 200 numbers are audio components (not included in Figure 9.2). The vertical section is the 300s group, the horizontal section is the 400s group, the sync circuits are the 500s group, and the low-voltage power supply is the 600s group. Find all five sections before continuing.

9.4.1 Video Amplifiers

In earlier chapters, did you follow and understand each circuit as it was described? If you can answer yes, you are in good shape for this section. If you answer with a question mark, here is a good opportunity to make some major advances.

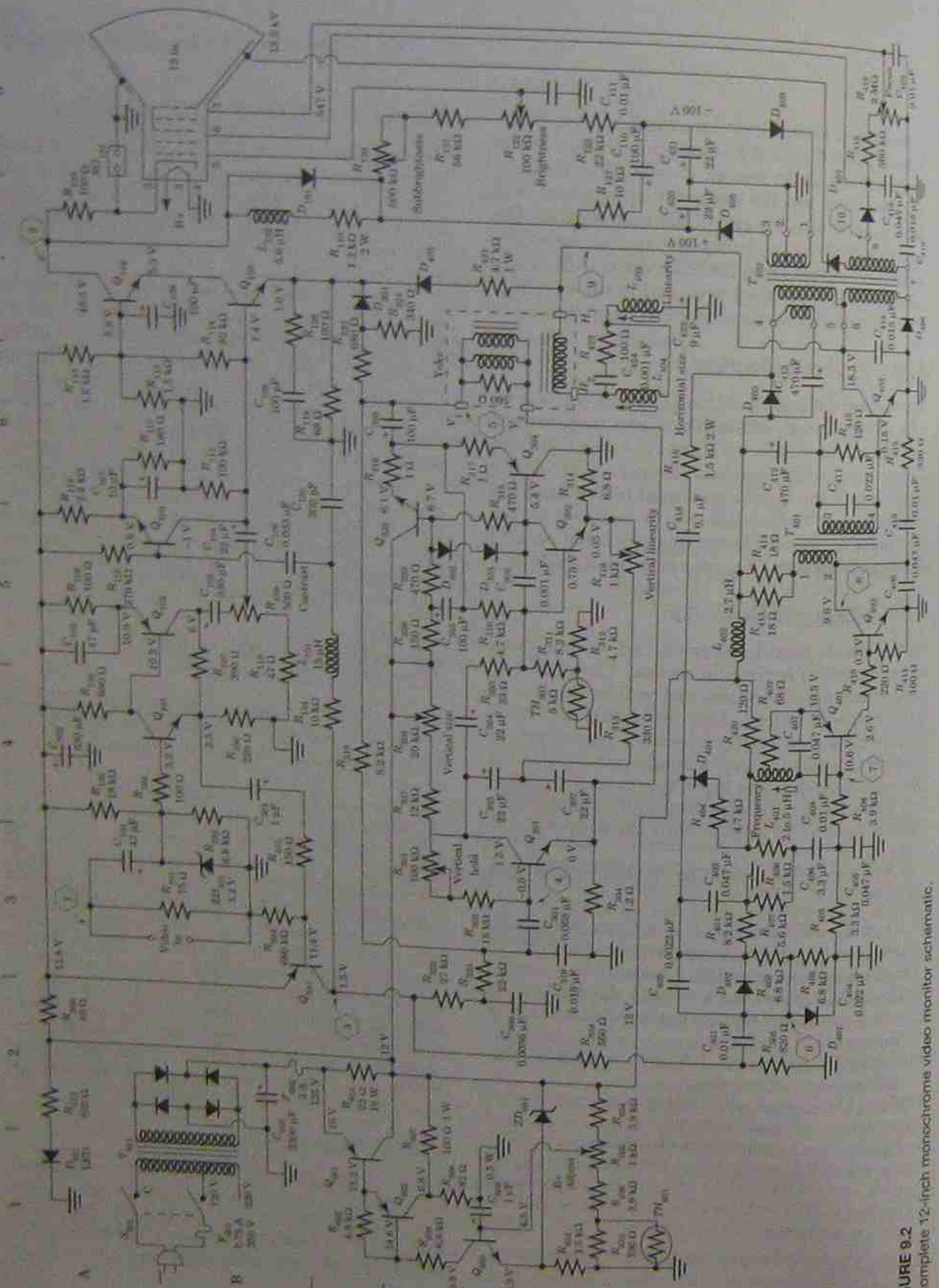


FIGURE 9.2
A complete 12-inch monochrome video monitor schematic.

In Figure 9.2, the video amplifiers are found in sections 3A and B through 8A and B. They include the transistor circuits of Q_{101} through Q_{105} and the CRT. Amplifiers Q_{101} and Q_{102} are the same circuit as seen in Figure 6.5, and the amplifiers Q_{103}, Q_{104}, and Q_{105} are the circuits of Figure 6.8, the video amplifier with a cascode output section. They are drawn in Figure 9.2 slightly differently from the previous figures for sake of space conservation. A good practical exercise at this time would be to compare Figures 6.5 and 6.8 to the video circuit of Figure 9.2 on a part by part basis. Examine each component for part number, value, and point of connection. This will be a valuable experience for learning to read schematic diagrams regardless of how they are drawn.

The monitor schematic of Figure 9.2 was intended for computer use; therefore, the waveshapes of Figure 9.3 show data as video signals. When intended for analog video displays, video waveshapes similar to Figures 5.11 and 5.12 would be shown on the waveshape diagram.

Wave 1 is the video input signal with negative sync. Wave 2 is the video output with positive sync at both the vertical rate and the horizontal rate. Wave 3 is the composite sync signals shown at both the vertical and horizontal rates. Waves 4 and 5 are the vertical deflection waves, and waves 6 through 9 are the horizontal deflection waves. Wave 10 is the ac voltage wave that will be rectified for the CRT focus voltage. Find and highlight all 10 test points on Figure 9.2 before continuing. Highlight all 11 controls found in Figure 9.2 with a different color marker. The controls are B+ adjust, contrast, brightness, subbrightness, vertical hold, vertical size, vertical linearity, horizontal frequency, horizontal size, horizontal linearity, and focus.

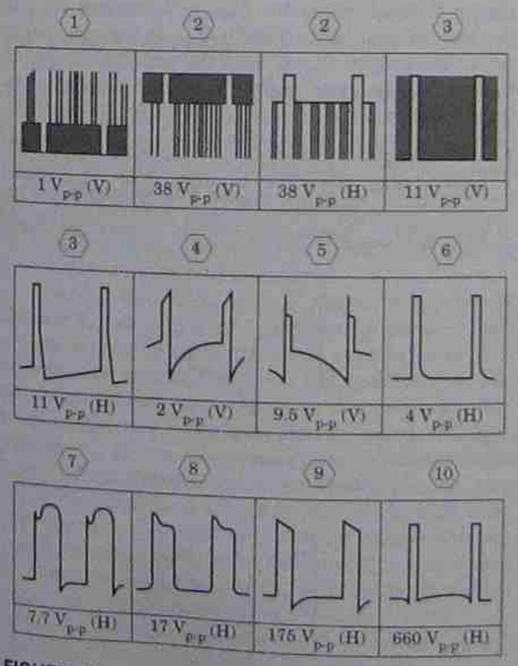


FIGURE 9.3
Waveshapes at designated test points in Figure 9.2.

Using a colored marking pen, draw in the video signal path on Figure 9.2 with arrowheads to show the direction of signal flow, according to the following instructions.

The lower video input terminal is ground, so the top terminal is realistically the video input terminal.

- ☐ From the video input terminal, through capacitor C_{101}, to the right through resistor R_{104} to the base of Q_{101} (arrowhead).
- ☐ Out the collector of Q_{101} to the base of Q_{102} (arrowhead).
- ☐ From the collector of Q_{102} to the top side of the contrast control.
- ☐ From the center arm of the contrast control, to the right, through capacitor C_{104} to the base of Q_{103} (arrowhead).
- ☐ Out the collector of Q_{103}, into the emitter of Q_{104} (arrowhead).
- ☐ Out the collector of Q_{104}, through R_{123}, to the cathode of the CRT (arrowhead).

When tracing the signal through the video amplifier section, this is the sequence of check points that you would examine. Since you can only compare the signal levels at test points 1 and 2, you are somewhat on your own for the points between these two locations. The descriptive paragraphs of Figure 6.5 said that the overall gain of Q_{101} and Q_{102} would be about 3. Figure 6.8, which describes the output circuit of Q_{103} and Q_{104}, claims a gain of about 15. All schematics do not give you these details, so you will need to use some educated judgment. When you find a low output signal (wave 2) for a normal input signal, it will become clear where the fault lies after a few trial cases. This will come with experience.

Although transistor Q_{105} is considered to be part of the video amplifier section, it is out of the loop as far as gain is concerned. Q_{105} will be covered in the next section description.

In some cases, you may be required to predict and verify the signal polarity at an unscheduled test point. In Figure 9.2, the negative sync input signal can be observed at the base of Q_{101}. This is a common-emitter NPN amplifier. There is a 180° signal phase change. Q_{102} is a common-emitter PNP amplifier with another 180° phase change. Q_{103} is a common-emitter NPN amplifier with 180° phase change. Q_{104} is a common-base NPN amplifier with zero phase change. Overall, there are three 180° phase changes so that the signal arriving at the CRT cathode will be opposite in phase from that of the input signal. See Figure 9.3, sketch 1 and 2.

What signal source would you use to test this video amplifier section? You would use the system signal source whenever it is available. A computer monitor should be connected to the computer. A television receiver should be turned to a station program. Or the video output of a camcorder can be used with an analog video monitor. But what would you use if these signal sources are not available? A sine-wave or square-wave signal generator will give you equal or better results than the original signal sources. A sine wave is best for testing gain, frequency response, and clipping distortion, but it will take a highly trained eye to detect phase (linearity) distortion. A square wave can show you gain, frequency response, and phase distortion, but not clipping distortion. Figure 9.4 shows five conditions of square-wave output signals that you can use as a reference when testing video amplifiers.

What should be the frequency of the generated test signal? For a 15-MHz computer monitor, the sine-wave or square-wave test signal should be about 1 MHz. For a 4.2-MHz television video amplifier or a monochrome computer monitor, the sine-wave or square-wave test signal frequency should be about 0.5 MHz. Remember that a square wave is the sum of a fundamental sine wave plus proportionate values of all the odd harmonics of the fundamental frequency. This is practical to about the ninth harmonic. A 1-MHz sine wave with odd multiples to the ninth harmonic is 9 MHz. The amplifier must be capable of passing 9 MHz for a clean square-wave output signal.

At the cathode of the CRT (pin 2) in Figure 9.2, there is a **spark gap** (SG_{101}). Spark gaps are devices intended to discharge static voltages that can build up around cathode ray tubes when extremely high voltages are used. They are two closely spaced wires encased in ceramic or a glass bead. A static discharge will arc across the spark gap so as not to damage the transistors or CRT.

9.4.2 Sync Separators

Using the same color marking pen that was used to trace the video signal path, draw a dashed line to mark the path used by the sync signal according to the following instructions.

From the emitter of Q_{101}, the video signal passes through capacitor C_{501} and resistor R_{501} to the base of Q_{501} (arrowhead). Q_{501} is the sync separator. The output signal from the collector of Q_{501} is the composite sync signal and is distributed to three locations.

1. To the right, through R_{124}, L_{101}, and C_{106} to the base of Q_{105}, the video blanker. The sync signal turns on the normally off Q_{105}. The collector voltage of Q_{105} decreases, which lowers the base voltage of Q_{103} to turn Q_{103} off. This prevents video from arriving at the CRT during retrace time (retrace blanking) and prevents the retrace lines from appearing on the CRT face.
2. From the collector of Q_{105} again, the composite sync signal moves down through R_{322} and R_{323} to the base coupling capacitor C_{301} and the base of Q_{301}, the vertical oscillator. R_{322}, C_{309}, R_{323}, and C_{310} form the integrator (low-pass filter) that passes the vertical sync signal to the oscillator, but blocks the horizontal sync from reaching the oscillator, Q_{301}.
3. From the collector of Q_{501} again, the composite sync signal flows through R_{504} and C_{401} to the anodes of the dual-diode horizontal phase detector. R_{504} and C_{401} form the differentiator (high-pass filter) that allows the horizontal sync signal to reach the phase detector, but not the vertical sync signal.

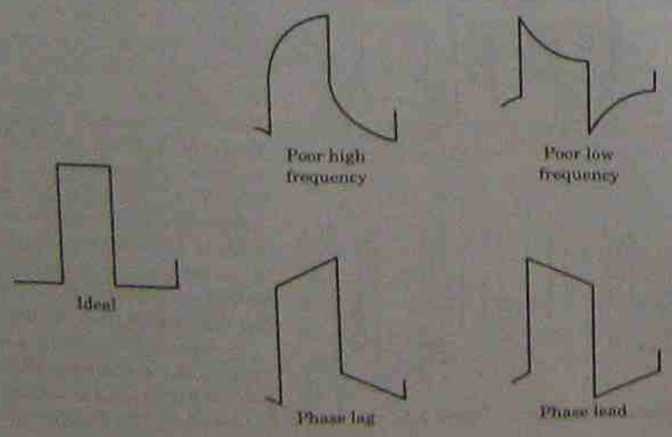


FIGURE 9.4
Reactions to a square-wave input signal as measured at the output of an amplifier.

The sync separator circuit just discussed is identical to Figure 7.1, but is drawn with a different layout to accommodate the connections between the circuits. Compare the diagram of Figure 7.1 to the sync separator circuit of Figure 9.2 on a part by part basis to verify the identities.

9.4.3 Vertical Deflection

The vertical circuit in Figure 9.2 is the full circuit of Figure 3.5 shown in a total system. It is found at the center of Figure 9.2, from 3C and D to 6C and D, and contains the 300s group. The manufacturer's waveforms of Figure 9.3 show only the input (4) and the output as wave 5. Figure 3.5 shows several intermediate waves that were measured to help explain the circuit operation.

When the oscillator is functioning, waveshapes 4 and 5 are the minimum necessary test points. When the oscillator stops working, there are no waves to measure and you will need to revert to dc voltage measurements from the schematic for troubleshooting. When feedback loop 1 is interrupted, the circuit stops oscillating. When feedback loop 2 is incomplete, there is no yoke current, and the CRT displays a single bright horizontal line. The circuit could still oscillate for this condition, which could be verified by measuring waves 4 and 5. The circuit still oscillates, with feedback loop 3 open, but will show very poor linearity.

The only change between the two mentioned figures is the placement of transistor Q_{503} in the push–pull output amplifier. Compare these two circuits for assurance of this change.

The vertical output signal at the yoke terminal V_1, used in feedback loop 1, is also applied through R_{320} and diode D_{301} to the emitter of Q_{102} video amplifier. Diode D_{301} conducts on the positive peak vertical signal and raises the emitter voltage on Q_{103}, turning it off during vertical retrace time. No vertical retrace lines appear on the CRT face during this interval.

Troubleshooting this section is straightforward. When there is no vertical deflection, check the circuit for waveforms first. If the waveforms are present, find out why they are not reaching the deflection yoke, or check the yoke for an open circuit. When there are no waveforms, compare the dc voltages at the emitter, base, and collector of all four transistors to the dc voltages marked on the schematic. When there is deflection with distortion or insufficient size, check the feedback loops.

9.4.4 Horizontal Deflection

The horizontal deflection and high-voltage sections, found in Figure 9.2 between 2E and F to 8E and F, are presented in the same way as in the previous sections. The AFC diodes D_{401} and D_{402} are explained from Figure 4.4. The horizontal oscillator Q_{401} is the electron-coupled Hartley oscillator of Figure 4.7 and includes the driver transistor Q_{402}. The horizontal output amplifier Q_{403} and high-voltage sections are found in Figure 4.8. Examine these sections if extended review is needed, or use Figure 4.11, which summarizes the other three figures, when a minimum review is needed.

Figure 9.5 is a photograph of the high-voltage transformer with a pinout diagram. The pinout is normally found in the service data. The heavy-gauge wire is the high voltage lead to the CRT. The high-voltage rectifier is encased in the molded plastic housing, as noted on the schematic diagram of Figure 9.2 (at 7F) and is not separately replaceable.

The output windings of T_{403}, pins 1, 2, and 3, have been omitted until now. Pin 2 is ground, making the voltage on pin 3 opposite in polarity from pin 1. Pin 3 goes to the anode of diode D_{405} that rectifies the positive peak pulses, which are filtered by capacitor C_{420} to develop a +100-V dc supply voltage. Pin 1 goes to the cathode of diode D_{406} that rectifies the negative peak pulses, which are filtered by capacitor C_{421} to develop a −100-V dc supply voltage. These two voltages are in the brightness circuit and are the dc supply for the cascode video output amplifiers of Figure 6.8 (Q_{102} and Q_{104}).

The horizontal output signal from the yoke terminal H_1 (at 6D) is fed through resistor R_{421} and



FIGURE 9.5
Television flyback transformer.
(Courtesy of Thordarson Meissner, Inc.)

out again, indicating excessive current drain in one of the circuits. Do *not* use a heavier fuse, as this could cause more damage than good. The normal procedure is to measure the dc resistance of each circuit until you find which component causes the high current drain. This can be long and laborious. Instead, change the ac line so that 120 V ac is connected to the 220-V ac tap and common. This will reduce all the voltages to one-half their normal values and may allow you to find the high current drain defect by measuring the voltages in the suspect circuit. All the circuits will still work, but at reduced capacity (i.e., less brightness, weaker video and smaller than needed raster size).

9.5 COLOR MONITOR BLOCK DIAGRAM

Figure 9.6 is the block diagram for a computer color monitor. Compare Figure 9.6 (color) to Figure 9.1 (monochrome) monitors. Look for the similarities and differences between the two diagrams. Both units use cathode ray tubes, but of different types. A deflection yoke is still needed, so there must be a vertical deflection circuit, a horizontal deflection system, and a high-voltage circuit. Without looking at a circuit diagram, you can see that different types of circuitry are used in the two cases, but the functions are the same. That is the important point to remember, that the functions are the same.

A sync circuit is still required for correct timing of the deflection oscillators. For the color monitor, the sync signal may come from either of two sources, the composite video signal or the computer-generated sync input terminals. Therefore, a circuit is needed that recognizes the origin of the sync pulses, and this is the function of the sync gate circuit. The sync separator is internal to the digital countdown chip (*UC402*), as was suggested in Figure 7.5.

Video amplifiers are still needed to drive the CRT, but now there are three electron guns in the CRT requiring three nearly identical video amplifier strings.

The functions of the audio section, when used, are the same for either type of monitor, as is the function of the low-voltage power supply. These will be examined as they appear in the circuit schematics.

The major differences involve the color input circuits and the contents of the composite video input signal, monochrome or color. This monitor sample was selected because it will accept any of three

diode D_{403} to the emitter of Q_{405} to turn the CRT off during horizontal retrace time. Note that diode D_{401} in the vertical and D_{402} in the horizontal circuits do the same work as the blanking transistor Q_{302} in the video amplifier circuit.

9.4.5 Regulated dc Supplies

The low-voltage power supply in Figure 9.2 is located along the left edge in sections 1 and 2. It has an input that accepts 120 or 220 V ac by a solder connection or movable tap on transformer T_{401}. The secondary is connected to a full-wave bridge rectifier and filter capacitor C_{403}. Transistor Q_{404} is the regulator in parallel with a 22-ohm (Ω), 10-watt (W) resistor and maintains a steady voltage drop across R_{404} regardless of how much current is drawn by the monitor. Q_{405} and Q_{406} are the bias setting transistors for Q_{404} and are controlled by the setting of R_{405}, the B+ adjust control.

When all the dc voltages are low or are zero, the problem is in the power supply. The regulator transistor Q_{404} and filter capacitor C_{403} are the most probable suspects. Check these first. If they appear to be in good condition, substitute an external dc voltage (from a separate supply) to the base of Q_{404} to test the circuits of Q_{405} and Q_{406}.

Power supplies of this voltage give you an advantage in cases that involve short circuits. Take the example of when the fuse is burned out. You replace the fuse, turn the unit on, and the fuse burns

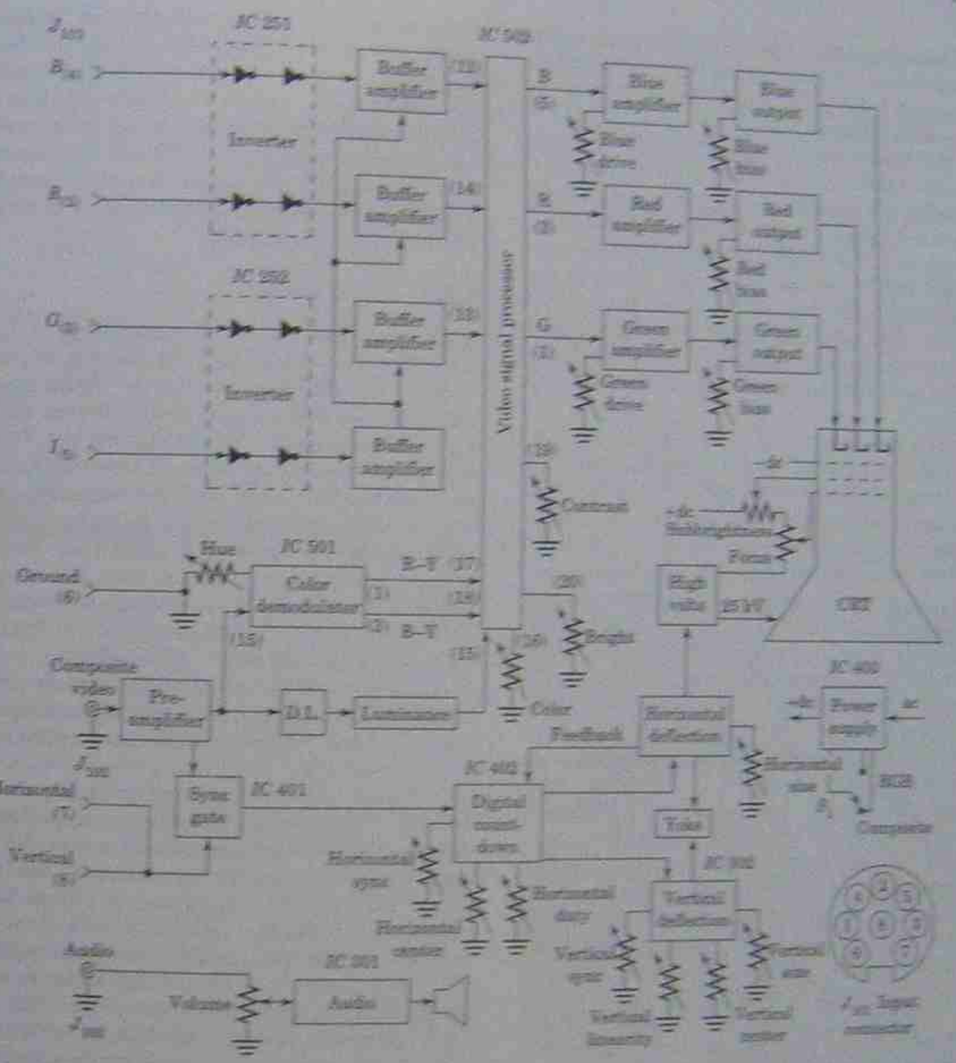


FIGURE 9.6
Block diagram of a computer color monitor. Magnavox model 80.
(Courtesy of Philips Consumer Electronics Co.)

basic signal formats: (1) a monochrome composite video signal for a black and white display, (2) a complex composite video signal for a full color display, and (3) separate red, green, blue, and intensity (*Y* signal) inputs for a full color display. Not all color monitors have this wide a range of input capabilities. You will need to make this observation at the onset of any product examination. This monitor was designed to be sold for use with any computer base unit. When the computer base and monitor are enclosed in the same case, the monitor need only function with that specific computer base.

9.5.1 Monochrome Video

We will start the circuit discussion using a monochrome composite video input signal at terminal J_{101}. Bear in mind that these same circuits main-

the low-frequency (video) circuits of a color television receiver and that you will be referred back to this section for the detailed description when receivers are examined.

The input signal is 1 V_{p-p} with negative sync. It is characterized by no color burst on the back porch of the horizontal blanking pulse. Switch S_1 in the power supply is in the composite position to remove the dc voltage from some of the color circuits. The first circuit encountered by the signal is the preamplifier, which identifies any low-level signal amplifier. The wide bandwidth of the video signal suggests a low gain of about 2 or 3. At this time, you will not know the circuit type, only the circuit function.

From the output of the preamplifier, the signal is fed in parallel to the color demodulator (IC3/1), and to the delay line (DL_1). The color burst signal turns on the color demodulator, and, in its absence, the demodulator is held in the off state. The delay line slows the passage of the video (luminance) signal by approximately 1 microsecond (μs) and then applies the luminance signal to the video signal processor (IC3/2). Inside the video signal processor, the video is fed in parallel to three amplifiers, identified as matrix (mixing) amplifiers. Each matrix amplifier has a separate output for blue (pin 5), red (pin 6), and green (pin 7) for application of the video signal equally through three similar sets of amplifiers to the cathodes of the CRT for a black and white picture display. The contrast control (pin 19) adjusts the gain of all three matrix amplifiers to regulate the signal strength to errors in the three electron guns. The brightness control (master brightness) at pin 20 changes the dc output voltage level of all three matrix amplifiers. It was stated earlier that the brightness control sets the dc bias on the CRT. Therefore, when the brightness control is this far removed from physical contact with the cathodes of the CRT, it must be assumed (with 99.9% accuracy assurance) that the video amplifier chain is all dc coupled (no series coupling capacitors from pin 5 through the blue amplifier and blue output to the cathode of the CRT (blue is used as an example).

The setup of the bias controls to obtain a white raster and the procedure for the drive controls to achieve good gray scale adjustments for this block diagram and the schematic to follow are covered in Chapter 16. Note, however, that the three bias controls set each part of the color output amplifiers. The master brightness control is set to see a raster and then the bias controls (individual brightness controls) are used to balance the red, green, and blue dc voltages on the three cathodes for a clean white raster. There are only two drive controls. The contrast control is set for a predetermined level of video at the CRT and then, using red as a reference, the green and blue video signals are adjusted to maintain a good black to white ratio (individual contrast controls).

9.5.2 Color Video

A colorplex composite video signal input at J_{101} follows the same signal path as the signal just described. The difference is that the signal now contains the modulated *I* and *Q* signals plus the color burst. These signals must be filtered out, demodulated, and then added back as three separate signals into the flow along with the luminance signal. The set of filtering and demodulating causes the color signals to be delayed by about 1 μs. Therefore, a delay line is placed in series with the luminance signal by an equal amount of time so that all signals arrive at the CRT at the same time. This eliminates color fringing of the picture display.

Think back to how the color signals were assembled. The color demodulator block diagram in Figure 9.6 will reverse that process here to recover the color signals.

The detailed block diagram of Figure 9.7 is typical of both discrete and chip circuitry. The modulated color information is contained in the upper frequencies of the video signal range, that is, between 2.1 and 4.1 MHz, as seen in Figure 8.16e. A simple high-pass filter blocks all low frequencies below 2.1 MHz and passes all higher frequencies. The video range is limited to 4.2 MHz, so a high-pass filter passes all frequencies from 2.1 to 4.2 MHz. However, some manufacturers feel that there may be some harmonic content in the upper range and use a true band-pass filter to ensure that only the modulated color signals are used for color recovery. The input to the filter is the colorplex composite video signal as seen in Figure 8.14m, and the chroma signal out of the filter is as seen in Figure 8.14l, at about 300 to 500 millivolts (mV) peak to peak. Inside the demodulator chip IC3/1, the chroma signal is amplified by chroma amplifier 1 and applied in parallel to two keyed amplifiers.

The feedback pulse from the high-voltage transformer to the horizontal phase detector (APC) is also applied to the color demodulator circuit (not shown in Figure 9.6). Some products identify this as the sand castle, and it is so labeled in Figure 9.7.

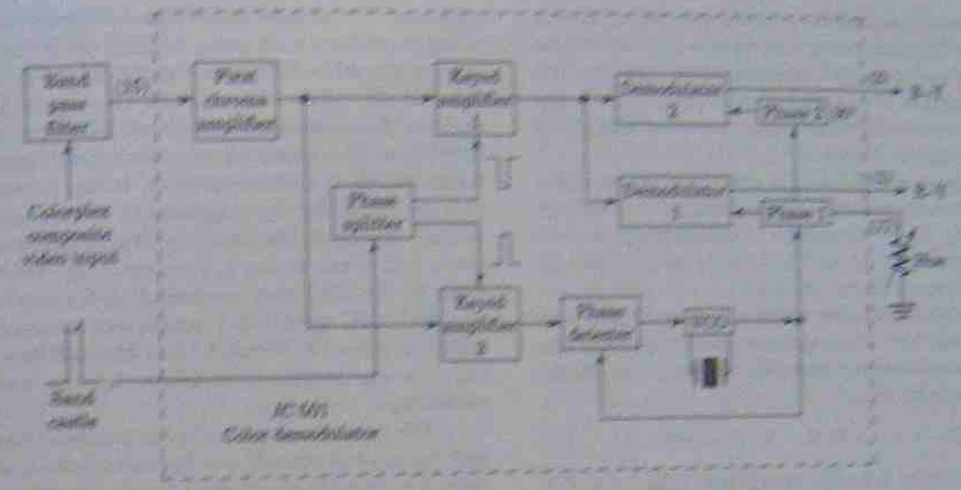


FIGURE 9.7
Block diagram of a typical color demodulator.

The positive horizontal pulse reaches a phase splitter. A common-emitter amplifier with an output from the emitter and another output from the collector is a good example of a phase splitter. A transformer with a grounded secondary center tap is another possibility for phase splitting.

The negative horizontal output pulse is applied to keyed amplifier 1 in Figure 9.7. This will turn off keyed amplifier 1 during the horizontal retrace time and remove the color burst from the chroma signal. The result is a clean chroma signal, which is then fed in parallel to both demodulators.

The positive horizontal pulse from the splitter is fed to keyed amplifier 2 in Figure 9.7. Keyed amplifier 2 is turned on during the horizontal retrace time to pass the color burst signal as a sync signal to the phase-locked-loop, crystal-controlled oscillator (VCO). The VCO must exactly match the color burst in frequency and phase for true color reception. The phase and frequency corrected 3.579545-MHz output from the VCO is now ready for application to the two demodulators.

In the development of the color signals, the *I* or *Q* signal was fed into a balanced modulator along with a specific phase-related carrier signal. The output was the modulated *I* or *Q* signal with a suppressed carrier (sidebands only) format (i.e., DSBSC amplitude modulation).

The demodulators use the same balanced modulator circuit, but the input and output signals are different. When the sidebands only of a DSBSC amplitude-modulated *I* signal are input to the balanced modulator along with the corresponding carrier, the circuit becomes a dc modulator and will output the recovered *I* signal, using *I* as an example.

Second, the transmitters always modulate the *I* and *Q* signals, called wideband color, but the receiver designer may recover (demodulate) the color information by using a phased carrier of his or her choosing. Use Figure 8.12b as a reference. The standard demodulator carrier input signal may be shifted by 57° from the burst to recover the *I* signal. When the carrier is shifted by 90° from the burst, the recovered signal will be the R − Y color signal. A carrier at 147° from the burst will recover the *Q* signal, and when shifted by 180° from the burst, will recover the B − Y color signal.

For the first demodulator, the carrier signal phase is chosen to be phase shifted by 57° or 90° from the burst phase, and the second carrier is always shifted 90° from the first carrier phase to effect quadrature demodulation.

In Figure 9.7, the first phase shift network (θ_1) is at 90° from the VCO carrier output phase to recover the R − Y signal out of demodulator 1. Once this is established, the output of the first phase shift network is shifted another 90° by phase shifter 2 for a total of 180° to recover the B − Y signal out of demodulator 2. The hue or tint control can vary the phase in shifter 1 plus or minus a few degrees to adjust for exact color reproduction. When viewing an unfamiliar color picture there is

no assurance of the colors in the scene being viewed except FLESH tones, and this is the color you should use to make the correct color setting. The demodulated R − Y and B − Y color signals are now passed to the video signal processor along with the luminance (*Y*) signal.

Figure 9.8 shows the operation of the video signal processor and will first be used to conclude handling of the colorplex video and then used to show the conditions for the R, G, B, and *I* input signals in Section 9.5.3.

Inside *IC*502, the video signal processor, the R − Y and B − Y signals are used to develop the third color difference signal G − Y according to the following equation:

$$G - Y = -0.51(R - Y) - 0.19(B - Y) \quad (9.1)$$

Check Chapter 8 for the numerical values of R − Y and B − Y; then multiply the two quantities by their decimal value and combine like terms to arrive at

$$G - Y = -0.3R + 0.41G - 0.11B \quad (9.2)$$

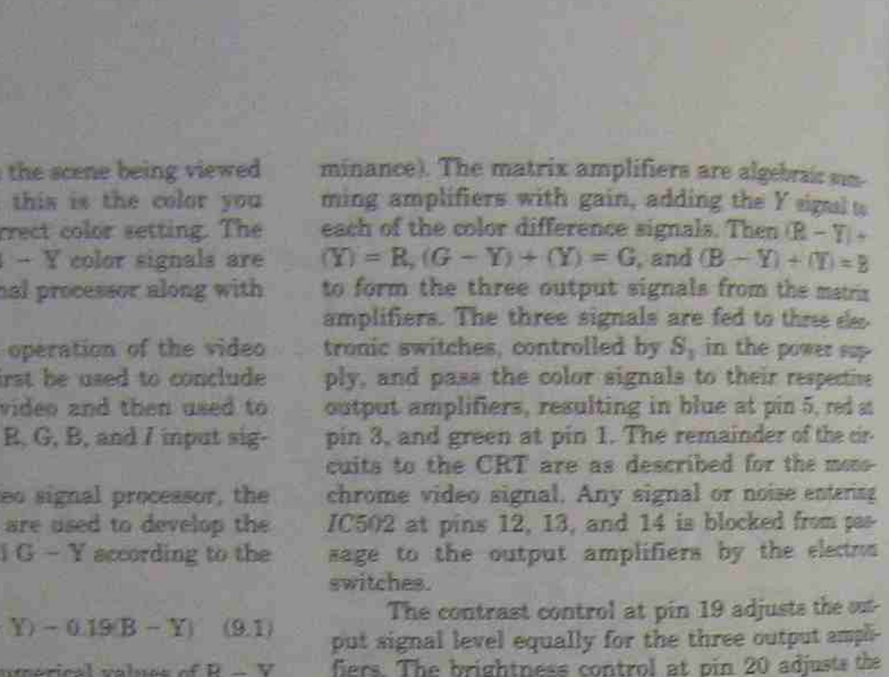
The three quantities R − Y, B − Y, and G − Y are now applied to their respective matrix (mixing) amplifiers along with a positive polarity *Y* signal (luminance). The matrix amplifiers are algebraic summing amplifiers with gain, adding the *Y* signal to each of the color difference signals. Then (R − Y) + (Y) = R, (G − Y) + (Y) = G, and (B − Y) + (Y) = B to form the three output signals from the matrix amplifiers. The three signals are fed to three electronic switches, controlled by S_1 in the power supply, and pass the color signals to their respective output amplifiers, resulting in blue at pin 5, red at pin 3, and green at pin 1. The remainder of the circuits to the CRT are as described for the monochrome video signal. Any signal or noise entering *IC*502 at pins 12, 13, and 14 is blocked from passage to the output amplifiers by the electron switches.

The contrast control at pin 19 adjusts the output signal level equally for the three output amplifiers. The brightness control at pin 20 adjusts the dc at the output of all three amplifiers, and the color contrast control at pin 16 adjusts the gain of all three matrix amplifiers simultaneously.

9.5.3 Separate R, G, B, and *I* Inputs

When a computer supplies individual TTL formatted color signals to the monitor, they arrive through an eight-wire cable at the D8P connector labeled J_{101} in Figures 9.6 and 9.8. The pin-out diagram is given in Figure 9.6.

FIGURE 9.8
Block diagram of a typical video signal processor.



The RGB/composite switch in the power supply is placed in the RGB position before the monitor power is turned on. This sets the sync gate to accept sync pulses from pins 7 and 8 of the input connector and places the three switches in the video signal processor to pass signals from J_{101} to the output amplifiers, rather than from the three matrix amplifiers.

The RGB and *I* input signals are 0.7 V_{p-p} and the positive sync pulses are 1 V_{p-p}. The RGB signals contribute to the background and data information from the computer base, and the *I* signal (intensity) is the dc level required to support the RGB color input signals. Each color input signal has its own set of amplifiers between the cable connector and the entrance to the video signal processor chip, *IC*502. The intensity value (dc level) is supplied in parallel to each color adder. For example, when the waveshapes from Figure 8.7a, b, c, and d are fed into J_{101} pins 4, 2, 3, and 5, respectively, the CRT displays the NTSC color bar pattern. The three switches in *IC*502 are now set to pass the separate color input signals to the processor output amplifiers because of the setting of S_1 in the power supply.

The brightness and contrast controls have the same duties for the separate RGB input signals as they did for the matrix signals, but now the color contrast control has no effect on the color signals. The color gain is controlled by the computer.

The schematic diagram for this color monitor has more amplifier circuits than have been seen here in Figures 9.6, 9.7, and 9.8. They are stages such as inverters, limiters, or automatic control amplifiers, to name a few, and they have been omitted from the block diagrams for simplicity. This does not change the functions of any of the diagrams presented to this point, but simply makes the diagrams less cluttered and easier to understand.

9.6 COLOR MONITOR SCHEMATICS

Figure 9.9 is the full schematic for the block diagram just presented. It is wise to familiarize yourself with each new schematic that you encounter. When the job does not permit this time, take the diagram home with you and invest an evening. The grid system of Figure 9.9 has 1 through 12 across the top and A through E along one edge.

The first step is to locate and highlight all 10 integrated chip circuits on the schematic diagram. Do this before continuing. The second step is to highlight (with a different color) all 22 controls. The controls are sharpness, hue, color, contrast, brightness, blue drive, green drive, blue bias, green bias, red bias, subbrightness, focus, horizontal sync, horizontal duty cycle, horizontal centering, horizontal size, B + adjustment, V sync, V linearity, V size, V centering, and volume. There are three variable resistances on the schematic that are not adjustable; they change value with temperature. Two are at 2E in the degaussing circuit, and the third is at 12B in series with the high-voltage lead. Locate and mark all 22 adjustable controls before continuing.

9.6.1 Signal Tracing

As a final step in familiarization, compare the block diagram of Figure 9.6 to the schematic diagram. Having covered the block diagram in detail over the last few sections, can you now trace any of the three types of signal paths through the schematic diagram? Try these examples. Almost all schematics start in the upper-left corner and advance as you would read text in an English printed book.

EXAMPLE 1

The colorplex composite video signal is applied to J_{101} at 1A. The preamplifier section contains transistors TS_{500}, TS_{502}, and TS_{504}. From the emitter of TS_{504}, the signal splits, following the upper path through a high-pass filter (C_{544}, C_{545}, C_{546}, and coil S_{503}) into the color demodulator *IC* 501 at pin 13. The lower path passes a low-impedance trap at 3.579545 MHz to remove the color subcarrier signal and then goes through the delay line S_{504} (note the schematic symbol) and then to the base of the luminance amplifier TS_{506}, then out from the emitter of TS_{506} and into pin 15 of the video signal processor *IC*502. The two demodulated color signals come from pins 1 and 2 of *IC*501 to join the luminance at pins 17 and 18 of *IC*502. Note the G − Y signal development in *IC*502. The outputs of *IC*502 are the three color signals at pins 5, 3, and 1. Follow the blue signal from pin 5 of *IC*502, past the blue drive control (R_{560}), to the base of TS_{560}, from the collector of TS_{560} to the emitter of TS_{570}, the common-base amplifier; from the collector of TS_{570} to the cathode of the blue electron gun in the CRT. The green and red signals have their own set of amplifiers, just like the blue circuit.

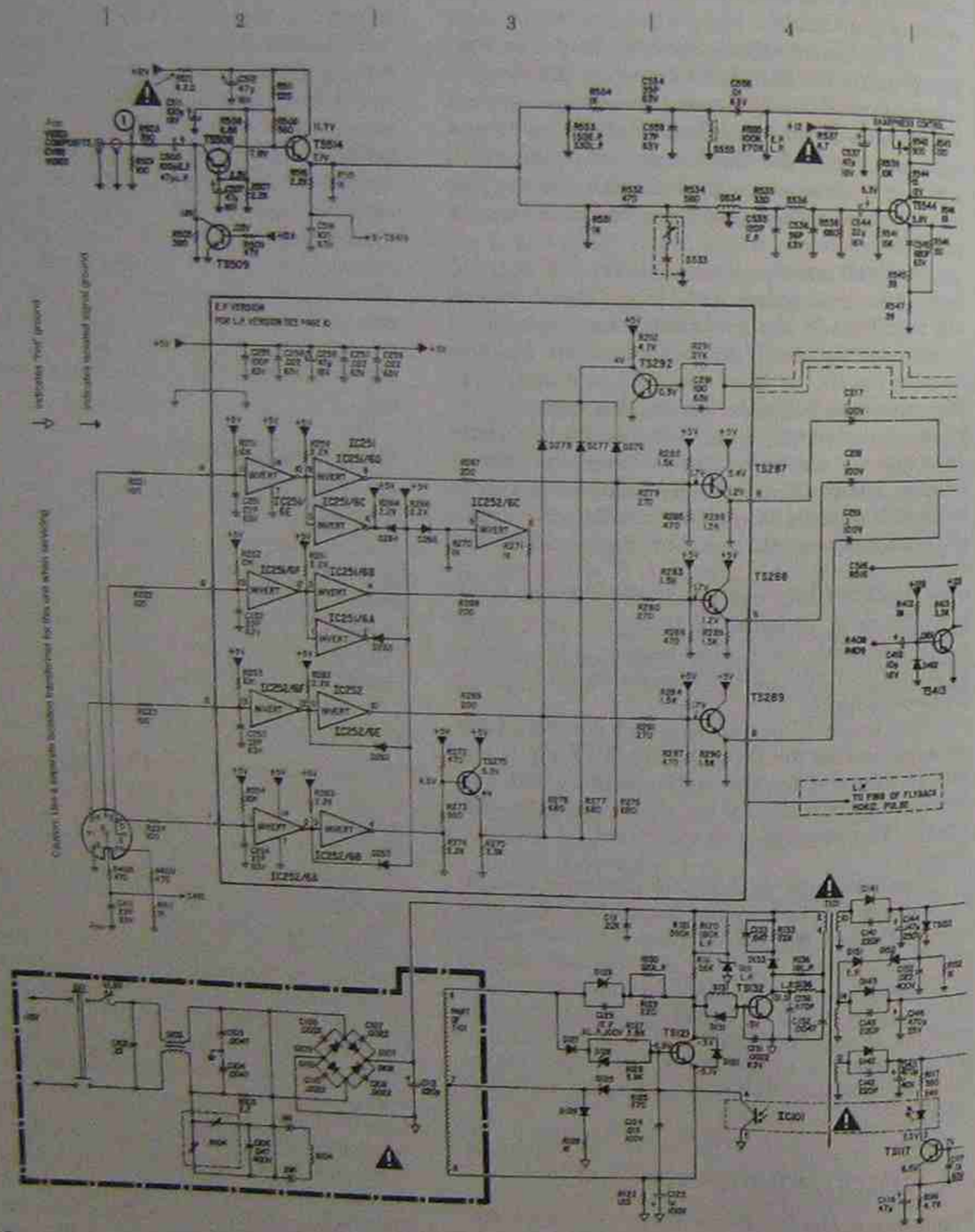


FIGURE 9.9
The circuit schematic for Magnavox model 80 color computer monitor. (Courtesy of Philips Consumer Electronics Company.)

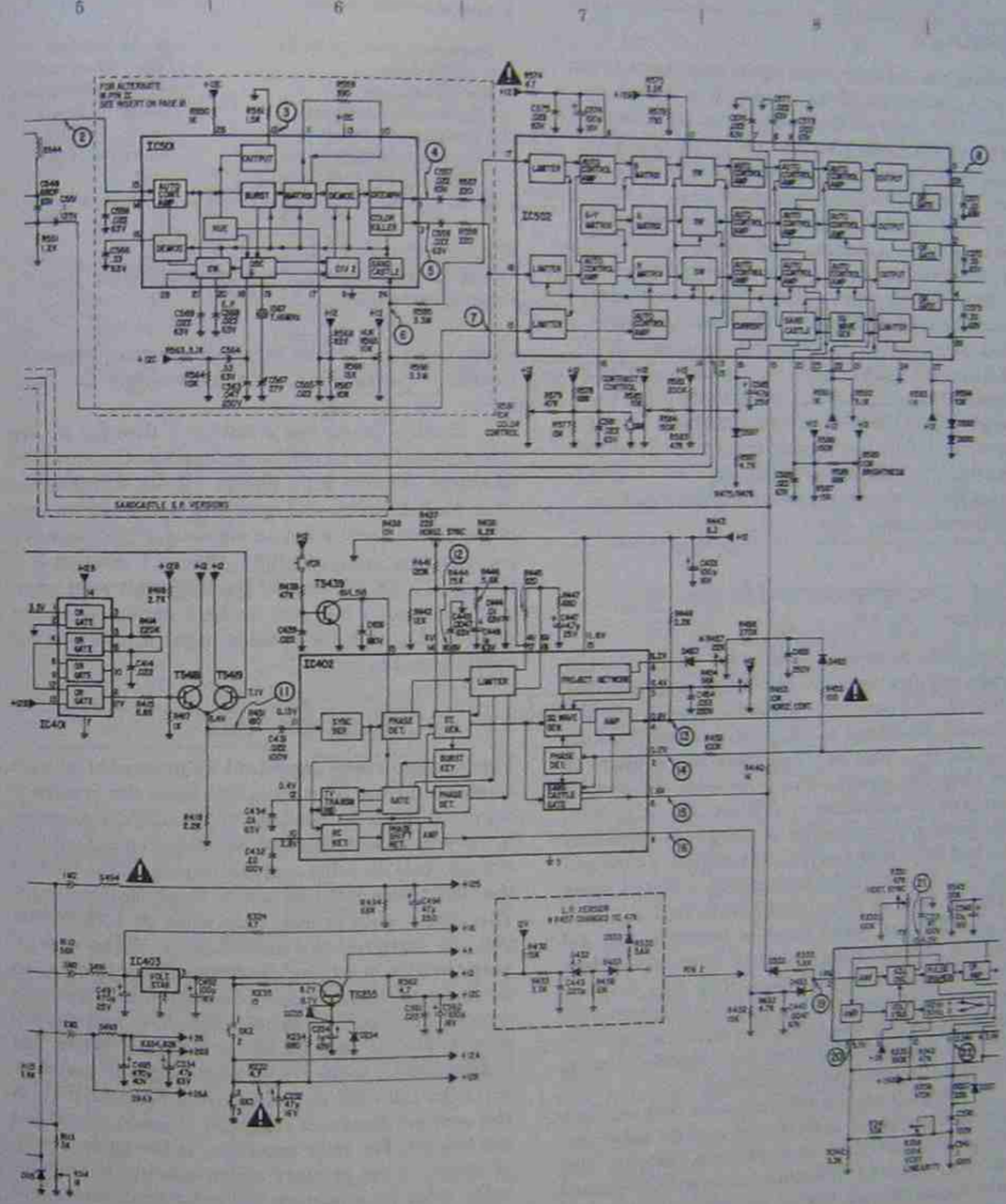


FIGURE 9.9
(*Continued*)

EXAMPLE 2

Tracing the red color input signal only starts at pin 2 of J_{101} in section 1D and goes to R on the interface board. Here we find two inverter sections of *IC* 251. The red signal goes into pin 11, out of pin 10, back in again at pin 9, and out again at pin 8 to the base of the buffer–adder transistor TS_{287}. Notice that the *I* signal (intensity) joins the red signal at the base of TS_{287}, coming from the emitter of TS_{276}. From the emitter of TS_{287}, the red signal enters the *IC* 502 video processor at pin 14. As the red signal goes to the red switch, notice the missing arrowhead. You will find occasional omissions of this kind and will need to make an appraisal of what it means. This is an easy one, because the other two switches have three input signals and one output signal; therefore, the missing arrowhead should be into the switch. From the switch in *IC* 502, the red signal follows the same path as was described for the first example.

9.6.2 Discontinuities and Schematic Symbols

To keep the schematic as clean as possible, many artists will give you a "to" and "from" condition. The sync inputs use this system. At 4C on the schematic, the base of TS_{415} has an arrow noting R_{408} and R_{409}. You then find these two resistors to see where the signal comes from. Some schematics also give you coordinates, such as R_{408}, R_{409} (1D). You then go immediately to the input connector J_{101} and find these two resistors with an arrow noting C_{412}. C_{412} is at the base of TS_{413}. Notice again that the base of TS_{413} sent you to find R_{408} and R_{409}. When you found these at terminal J_{101}, did you also notice another omission? There should be a connecting dot that joins R_{408}, R_{409}, R_{411}, and the arrowhead pointing to C_{412}. With the number of details required on a schematic of this size, some errors are bound to occur, but this should not affect the overall accuracy of the diagram.

Many schematics have a legend that will help you to understand the diagram and its notations. Figure 9.10 identifies some of these features. Particularly note the difference between HOT ground and signal ground. Signal ground is the common connecting foil on the printed circuit (PC) boards and is to be used when measuring dc voltages and oscilloscope waveforms. If you connect your meter or scope to HOT ground, you are in jeopardy of severe electrical shock and/or damage to your equipment. Use a 1 : 1 turns ratio transformer, called an isolation transformer, at the ac input for total safety.

Unless otherwise noted:

Resistors in ohms, 1/8 W, 5%
K = 1000 ohms
M = million ohms
Capacitors in microfarads
except p = picofarads
Voltages are measured with
120 V ac ± 1%, 60-Hz input
Hot ground

+26 dc source
+26 where used
— — — Components not on PC board
- - - - - - - - Possible alternate circuit
Signal ground

FIGURE 9.10
Typical schematic legend. This legend applies to Figure 9.9 schematic.

Finally, the circled numbers 1 through 30 are the ac signal waveforms to be found at the specified locations. Figure 9.11 shows all 30 waveshapes with peak-to-peak voltages and scope sweep settings. These are the key to successful troubleshooting; examine them carefully. Waves 1 through 5, 7 through 10, 28, 29, and 30 are the result seen when a rainbow color bar test pattern generator is applied to J_{102} composite video input and is not the NTSC color bar signal.

9.7 TROUBLESHOOTING

Possibly the most important requirement of successful servicing is to recognize *what* the system is supposed to do. In the case of monitors, determine if it is a color or black and white system. If you are unsure, look for color controls or look at the neck of the CRT to see if it has one or three electron guns. This alone could reduce your work by 50%. While you are verifying the performance of the device, keep the idea of a block diagram in your mind so as to eliminate the working circuits from the nonworking circuits. Look for generalities first and quality second. That is, look for the raster first. When this is established, is the raster bright enough and does it fill the full CRT face? Is there a picture? If so, is the contrast deep and rich or is it faded or washed out (weak)? For color monitors, is the raster white or is one of the primary colors missing? Check for color video by adjusting the color contrast or hue controls. When you know what you should see, you will recognize what is missing. Is the picture locked in vertically and horizontally? When none of these things occurs, check the circuit that is common to all circuits, the power supply. The procedure becomes more natural as you gain experience. You

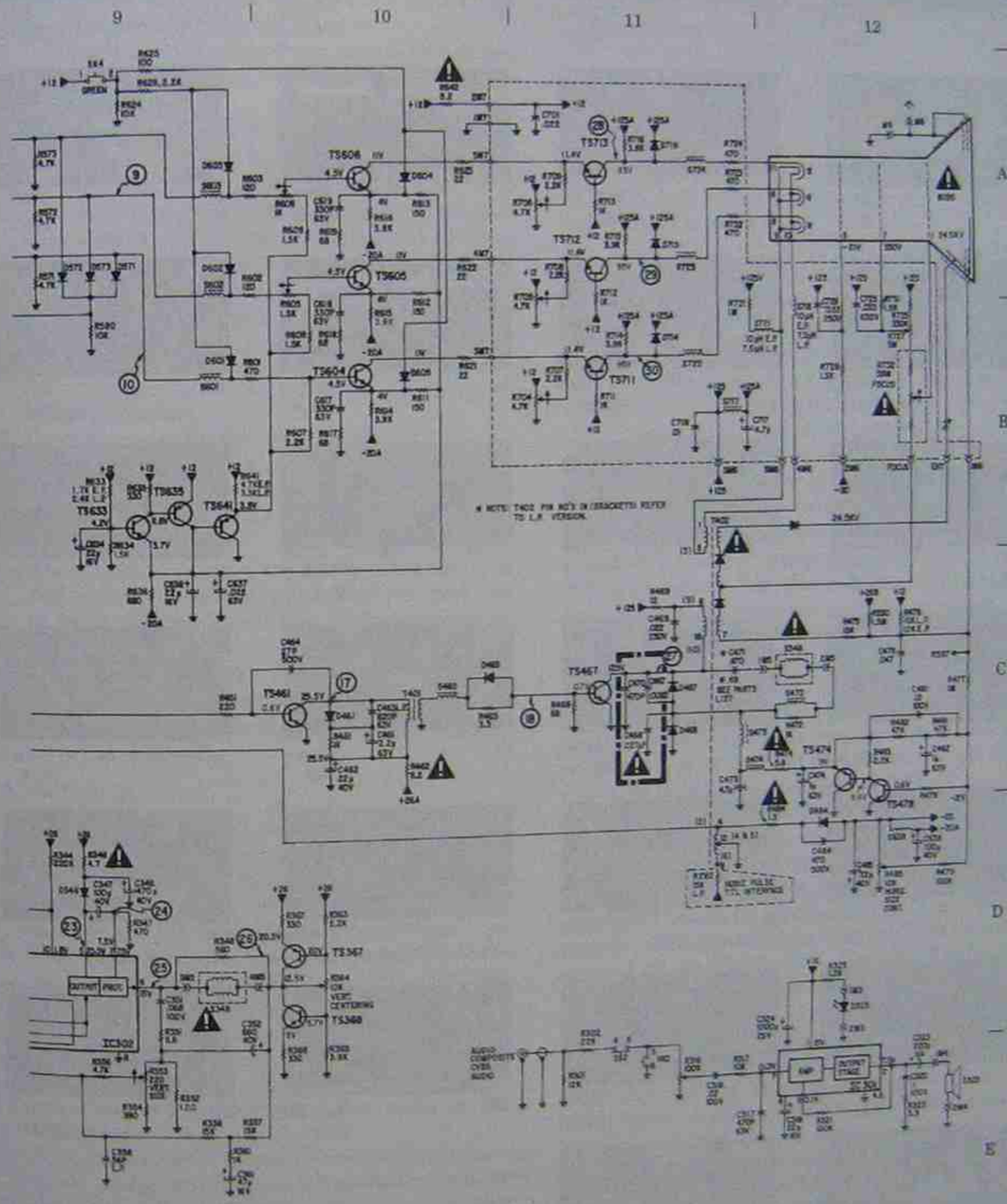
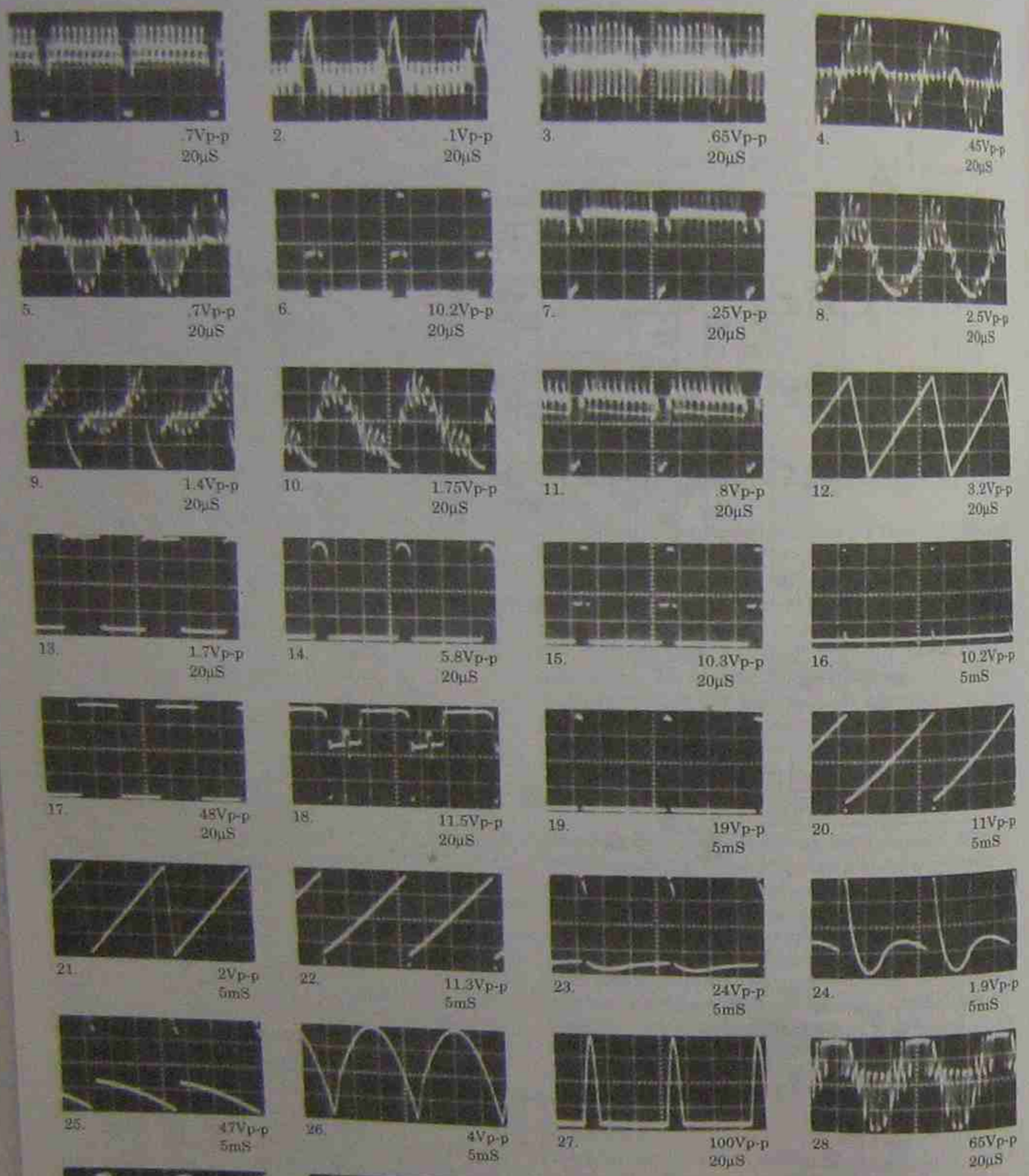


FIGURE 9.9
(*Continued*)



Waveform notes
Unless otherwise specified:

1. Waveforms taken under the conditions specified in the schematic notes
2. Sweep/time cm settings are shown just below photos. All photos were taken with the sweep time controls in the calibrated position. Horizontal positioning of the waveforms was adjusted for maximum clarity.

FIGURE 9.11
The waveforms to be found at the test points (circled numbers) on the schematic of Figure 9.9. (Courtesy of Philips Consumer Electronics Company.)

will soon run this check list through your mind without consciously thinking about it.

We will try two cases of troubleshooting to see if you can follow and understand the logic behind the process.

Case 1. Let's declare a circuit to be faulty and then examine the test results to show how that fault affects performance. Let's say that the red adder–buffer transistor section TS_{287} is incapable of passing a signal, for whatever reason, and no other fault is considered. We will ask questions first and then answer the questions. Try to answer the questions first before looking at the text answers. The set is plugged in and turned on with no input signal.

1. Is there a raster?
2. Does the raster fill the full screen?
3. Is the raster white or some other color? From this point on, an input test signal is required. We have fully tested the static conditions for the monitor.
4. If you elect to apply a composite video signal to J_{102} (color or monochrome), will you find the faulty circuit (mode switch in the composite position)?
5. If you apply the R, G, B, and *I* signals to J_{101} (plus sync), will this identify the faulty circuit?
6. Do you feel that a new plug-in interface card will solve the problem?

Answers to case 1:

1. Yes, there is a raster. This eliminates most of the power supply circuits.
2. Yes, the raster fills the screen. This eliminates the entire horizontal deflection and high-voltage sections and the vertical deflection circuits.
3. The raster is white. This eliminates the three video amplifier strings, TS_{606} and TS_{713} for blue, TS_{605} and TS_{712} for green, and TS_{604} and TS_{711} for red, as well as the output half of *IC*502. These circuits are dc coupled to the CRT. They control the bias on the CRT and hence the brightness of the three colors that make up the white raster.
4. Applying a color or monochrome composite video signal to J_{102} will produce the correct results on the face of the CRT and will not isolate the faulty circuits.
5. This will identify a fault only *if* you change the mode switch to the RGB position.
6. Yes, this will most likely identify the faulty section, but what if changing the interface board does not solve the problem? Notice that an open capacitor C_{217} could cause the same problem. Check them both.

Case 2. This case gives you the operating condition of the monitor that you observe or that has been reported to you. The monitor works well when a TTL logic signal is applied to J_{101}, but will only display in black and white when a colorplex composite video signal is fed into J_{102}.

Look at how much you have learned from this simple defect report. All the deflection and high-voltage circuits have been eliminated. The CRT and the six video output amplifiers have been eliminated. The interface plug-in card and the output half of *IC*502 have been eliminated. There are no reported synchronizing problems, so the sync gate can be eliminated. The input preamplifiers at J_{102} can be eliminated, as well as the luminance amplifier TS_{544}, because they all pass the monochrome video signal. The input half of *IC*502 can be eliminated because it passes the monochrome video signal. *IC*502 switches between the RGB and composite input signals, and the contrast or brightness functions are not reported as malfunctioning. You can eliminate most of the low-voltage power supply and, of course, the audio circuits. This leaves you with less than 10% of the schematic as a possible cause of the problem. The probable circuits are the high-pass filter from the emitter output of TS_{514} and the input to the color demodulator at pin 15 of *IC*501, or the color demodulator of *IC*501.

The next step would be to examine the signals as they pass through the system. Do you know that the input signal contains the color information? Look at waveshape 1 for the color burst and 10 modulated pulses on each horizontal line (rainbow pattern). If it appears to be complete, look for waveshape 2 at pin 15 of *IC*501. The signal here says that the high-pass filter is OK. Look at pins 3 and 1 for the output of *IC*501 at waveshapes 4 and 5, respectively. There is no output at either of these two pins; therefore, the problem must be around *IC*501. But don't be too hasty to change the chip unless it has a plug-in socket and you have a known good chip to spare.

Do check the dc voltages around *IC*501. But there are no voltages marked on the schematic. Do you see that pins 13, 17, and 26 are directly or indirectly connected to a voltage source? When you measure pin 13, the voltage is zero. Pin 17 measures +3 V dc, and pin 26 measures 0 V. You also see that pin 17 gets its voltage from a +12-V source, while pins 13 and 26 get their voltage from

a source marked 12C, a different source. You could take the time to calculate the approximate voltage at pin 17 for both extreme settings of the hue control and find the range to be from +1 to +5 V dc. The +3-V reading then seems normal. The C voltage source is missing. You then go to 6D on the schematic, where this voltage originates, and find that R_{562} (a 4.7-Ω, 1/8-W resistor) is burned or open. Resistors do not normally burn out by themselves. Checking further, you find C_{562} is shorted. This would draw heavy current through R_{562} and cause the burnout. Replacing both components (R_{562} and C_{562}) would have the system up and working again. C_{562} is 100 microfarads (μF) at 16 V. Would 80 μF at 25 V be OK? Any large-value capacitor with an equal or higher voltage rating would probably work, although a direct replacement always works best.

9.8 SUMMARY

This chapter is intended to help you to develop a *thinking* process that will serve you for as long as you are active in problem solving. Although you have gained considerable insight into two specific products, the underlying thought process of block diagram analysis and top-down troubleshooting applies to all electronic devices and is the main thrust of this chapter. Never let the large size or the supposed complexity of a system fool you into thinking that the problem is difficult. Break the system down into functions and then into smaller circuits that perform these functions. Any electronic professional can easily learn to troubleshoot a small circuit. Think through the process.

QUESTIONS

Video Monitors

9.1. What kind of a diagram is used to report the functions and order of events in an electronic system?

9.2. What kind of a diagram shows the exact component connections found in an electronic system?

9.3. Why are arrowheads important on a block diagram?

9.4. List the following events in the order that they would appear in a diagram.
(a) preamplifiers,
(b) contrast control,
(c) output amplifiers,
(d) input signal,
(e) sync takeoff

9.5. How does the grid system help you to read a schematic?

9.6. How are the components grouped on a schematic diagram to help you to find a specific part?

9.7. What is the polarity of the composite video input signal for a computer monitor?

9.8. What polarity of video signal is applied to the cathode of a CRT?

9.9. What polarity of video signal is applied to the control grid of a CRT?

9.10. What is the purpose of the spark gap?

9.11. What input square-wave frequency would you use when testing a color monitor?

9.12. What input square-wave frequency would you use when testing a consumer television video amplifier?

9.13. What signal does the integrator pass?

9.14. What signal does the differentiator pass?

9.15. Physically, where is the high-voltage rectifier to be found?

9.16. What special type of video amplifiers will be found when the brightness control is far removed from the CRT circuit?

9.17. What type of a video monitor, (a) color or (b) monochrome, will have the brightness control far from the CRT circuit?

9.18. Describe direct coupling.

9.19. What is the function of the three bias controls in a color monitor?

9.20. What is another name for the two drive controls in a color monitor?

9.21. What is the approximate delay time used to account for the color demodulator time lapse?

9.22. The delay line will be found in the
(a) color demodulator,
(b) preamplifiers,
(c) luminance amplifiers,
(d) matrix amplifiers, or
(e) RGB amplifiers.

9.23. What is the function of a keyed amplifier?

9.24. What input pulse determines the on–off state of a keyed amplifier?

9.25. Which of the following color signals are paired together?
(a) R − Y,
(b) *Q*,
(c) B − Y,
(d) *I*

9.26. Which of the following subcarrier phase angles are selectable for the first color demodulator?
(a) 57°,
(b) 90°,
(c) 147°,
(d) 180°

9.27. What is the phase relationship between the two color demodulator subcarrier signals?
(a) 57°,
(b) 90°,
(c) 147°,
(d) 180°

Troubleshooting Questions Using Figure 9.2

9.28. When the following are the only observations of choice, select one answer that will result when each of the stated defects occurs (good composite video input signal; power on).

(a) No raster
(b) One bright horizontal line
(c) Raster OK, no picture
(ab) Raster OK, picture rolls
(ac) Raster OK, picture tears
(ad) Raster OK, picture rolls/tears

(d) Raster OK, weak picture
(e) Short raster, picture OK
(ae) Narrow raster, picture OK
(bc) Picture folds over at bottom

1. C_{306} open
2. R_{106} open
3. R_{601} open
4. C_{309} shorted
5. R_{504} open
6. C_{111} shorted
7. C_{103} open

Troubleshooting Questions Using Figure 9.9 (good composite color video signal input; power on)

Select one answer for the stated defects.

9.29. The monitor has a normal raster but no picture.
(a) R_{601} open (9B),
(b) TS_{461} open (9C),
(c) R_{512} open (1A),
(d) R_{346} open and C_{346} shorted (9D),
(e) *IC* 301 defective (11E)

9.30. Normal monochrome picture, no color.
(a) TS_{461} open (9C),
(b) R_{512} open (1A),
(c) R_{544} open (4A),
(d) C_{481} open (5C),
(e) crystal 1567 open (5B)

9.31. One bright horizontal line on CRT.
(a) C_{338} open (8E),
(b) R_{593} open (8B),
(c) TS_{413} open (4C),
(d) C_{555} shorted (3A),
(e) SK_2, 1 and 2 open (5E)

Troubleshooting Questions Using Figure 9.9 (TTL input; power on)

Select one answer for the stated defects.

9.32. Raster OK, no picture.
(a) R_{352} shorted (9D),
(b) R_{236} open (5D),
(c) D_{141} open (4D),
(d) R_{547} open (4B),
(e) TS_{711} open (10B)

9.33. White raster, no red in picture.
(a) C_{638} shorted and S_{638} open (12D),
(b) TS_{711} open (10B),
(c) *IC* 501 defective (5A),
(d) R_{601} open (9B),
(e) R_{638} open (9D)

10 RF Transmission

10.1 INTRODUCTION

When the terms video and radio frequency (RF) transmission are used in the same sentence, the first thing that comes to mind is consumer television. This is good, because it is the tool that will be used here to explain the processes and conditions of modulation. However, data processing is fast moving into the RF transmission area as the link between the workstation and the on-site main frame. RF data transmission relieves the system of the bulk and losses incurred with cables and saves considerable time during installation. However, when the signals are radiated into the air, system security is lost unless scrambling methods are included in the format.

RF transmissions are defined as any message information modulated onto a higher-frequency carrier signal and radiated into the air from an antenna. The range of RF carrier frequencies starts immediately above the highest audible frequency of 20 kilohertz (kHz). There is limited use of the RF frequencies from 20 to 200 kHz, called the *forbidden zone* because of the burden on the antenna size, which is explained in Chapter 11.

Furthermore, the discussion on modulation is limited to the NTSC system in use by the 31 countries of the North American region. See Appendix A for the specifications and locations of the three world systems. The NTSC developed the standards for monochrome television in 1941 and the standards for color television in 1953, which were then adopted by the FCC.

10.2 FREQUENCY RANGES

All frequencies from 200 kHz to 300 gigahertz (GHz) are in use by some group of participants. There are no vacant spaces. The assignments include a carrier center frequency, a specific bandwidth, a maximum radiated power, a maximum antenna height, and a maximum coverage area. This affords minimum RF interference between transmitters and makes the most efficient use of the RF spectrum. Consumer television has been assigned two frequency bands. The very high frequency band (VHF), channels 1 through 13, was assigned in 1941 in the frequency range from 48 to 216 megahertz (MHz). The ultrahigh frequency band (UHF) was assigned in 1956 to include channels 14 through 83 in the frequency band from 470 to 890 MHz.

10.2.1 VHF Band

Each VHF channel is assigned a 6-MHz bandwidth going upward from 48 MHz (Figure 10.1). There are some skips in the sequential range of frequencies (see Table 10.1) where other world services already existed that could not easily be changed. International air navigation, for instance, could not be changed without a multinational agreement. Political reasons suggested that the FM radio band from 88 to 108 MHz, which was moved to this range just a few years earlier, not be changed again.

Channel 1 was reserved as a test channel for the television manufacturers of that time because there were no daytime broadcasts from which they

FIGURE 10.1
Placement of the lower VHF television channels in the frequency spectrum.



TABLE 10.1
Television channel assignments

Channel Number	Band (MHz)	Visual (MHz)	Aural (MHz)	Channel Number	Band (MHz)	Visual (MHz)	Aural (MHz)
2	54–60	55.25	59.75	36	602–608	603.25	607.75
3	60–66	61.25	65.75	37	608–614	609.25	613.75
4	66–72	67.25	71.75	38	614–620	615.25	619.75
5	76–82	77.25	81.75	39	620–626	621.25	625.75
6	82–88	83.25	87.75	40	626–632	627.25	631.75
7	174–180	175.25	179.75	41	632–638	633.25	637.75
8	180–186	181.25	185.75	42	638–644	639.25	643.75
9	186–192	187.25	191.75	43	644–650	645.25	649.75
10	192–198	193.25	197.75	44	650–656	651.25	655.75
11	198–204	199.25	203.75	45	656–662	657.25	661.75
12	204–210	205.25	209.75	46	662–668	663.25	667.75
13	210–216	211.25	215.75	47	668–674	669.25	673.75
14	470–476	471.25	475.75	48	674–680	675.25	679.75
15	476–482	477.25	481.75	49	680–686	681.25	685.75
16	482–488	483.25	487.75	50	686–692	687.25	691.75
17	488–494	489.25	493.75	51	692–698	693.25	697.75
18	494–500	495.25	499.75	52	698–704	699.25	703.75
19	500–506	501.25	505.75	53	704–710	705.25	709.75
20	506–512	507.25	511.75	54	710–716	711.25	715.75
21	512–518	513.25	517.75	55	716–722	717.25	721.75
22	518–524	519.25	523.75	56	722–728	723.25	727.75
23	524–530	525.25	529.75	57	728–734	729.25	733.75
24	530–536	531.25	535.75	58	734–740	735.25	739.75
25	536–542	537.25	541.75	59	740–746	741.25	745.75
26	542–548	543.25	547.75	60	746–752	747.25	751.75
27	548–554	549.25	553.75	61	752–758	753.25	757.75
28	554–560	555.25	559.75	62	758–764	759.25	763.75
29	560–566	561.25	565.75	63	764–770	765.25	769.75
30	566–572	567.25	571.75	64	770–776	771.25	775.75
31	572–578	573.25	577.75	65	776–782	777.25	781.75
32	578–584	579.25	583.75	66	782–788	783.25	787.75
33	584–590	585.25	589.75	67	788–794	789.25	793.75
34	590–596	591.25	595.75	68	794–800	795.25	799.75
35	596–602	597.25	601.75	69	800–806	801.25	805.75

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could test their products using live transmissions. Daily telecasting began with the 5 P.M. news, then went into entertainment programming, and concluded with the 10 P.M. news. One station stayed on the air with a live variety show until midnight before leaving the air. The television manufacturers set up their own transmitters on channel 1 for daytime testing. As daytime programming expanded, the manufacturers used channel 1 less and less. Finally, the FCC recognized an idle channel and stepped in to take channel 1 away from the television industry and reassigned this band of frequencies to other services.

The remaining 12 VHF channels now fall into two frequency groups. Channel 2 through 6 (54 to 88 MHz) are called the low VHF band and channels 7 through 13 (174 to 216 MHz) are called the high VHF band.

10.2.2 UHF Channels

Another 70 channels were opened up to television in 1956 with channels 14 through 83 in the 470- to 890-MHz frequency band. The initial problems with UHF were that (1) an external converter was required to lower the frequency from the UHF band to channel 3 or 4 in the VHF band and often required an additional antenna, (2) the much higher frequency circuits were more unstable than the lower frequency circuits and needed repeated adjustments, (3) the reception was fair to poor compared to the VHF channels, and (4) there were very few programs on UHF and the public was reluctant to invest in a converter and extra antenna until more programs were available. At the same time, the station owners could not justify the large expenditures to erect UHF transmitters until there was a bigger market. The FCC stepped in again and ruled that after 1963 all television receivers in the NTSC system would include a built-in UHF tuner as well as the existing VHF tuner. After 33 years of availability, partly due to cable television, the upper end of the UHF band was still void of public broadcast stations. The FCC stepped in again and in 1989 took channels 70 through 83 away from the television industry and reassigned these 84 MHz to cellular telephone, amateur satellite communications, and other services. The total television broadcast band is as seen in Table 10.1.

10.3 CARRIER MODULATION

Two carrier signals per channel are transmitted. The picture carrier is amplitude modulated and the sound carrier is frequency modulated in the NTSC system. Here's why.

First, in amplitude modulation the voltage and frequency of the carrier are constant, and only one set of sidebands is produced. There is one sideband above and one sideband below the carrier frequency. The amplitude of the sidebands is determined by the amplitude of the modulating signal. The bandwidth of the modulated signal is proportional to the highest modulating signal frequency. For frequency modulation, the voltage and frequency of the carrier change to produce many sets of sideband pairs that are totally dependent on both the modulating signal frequency and voltage.

Second, in earlier lessons you learned that the highest vertical resolution occurred when each scan line was alternately black and white, or about 240 lines of vertical resolution. To make the horizontal lines of resolution proportional to the vertical in a 4 : 3 aspect ratio, the horizontal resolution should yield about 320 lines. Then, from equation 5.1, it can be resolved that a video frequency of 4.27 MHz will net the desired number of horizontal lines of resolution.

The standard was then set to use 4.2-MHz maximum video frequency to amplitude modulate the picture carrier and generate the upper and lower sidebands. This would result in an 8.4-MHz modulated signal bandwidth. It is also known that the same intelligence is contained in each sideband, so to stay within the 6-MHz bandwidth limitations, a large portion of the lower sideband is filtered out. A vestige of the lower sideband remains, as seen in Figure 10.2, and is called **vestigial** sideband transmission.

Under the vestigial sideband specifications, the lower sideband voltage must be maintained at full amplitude (within −3 decibels (db)) for at least 0.75 MHz below the picture carrier frequency and then be attenuated to at least −60 dB below full strength at a frequency of 1.25 MHz lower than the picture carrier frequency.

The upper sideband voltage must be maintained at full amplitude (within −3 dB) over the frequency range of 4.2 MHz above the picture carrier frequency and then be attenuated by at least −40 dB at the sound carrier rest frequency.

The frequency-modulated sound carrier rest frequency must be at 4.5 MHz (±100 Hz) above the picture carrier frequency.

In less legal terms, the amplitude-modulated picture carrier signal is 1.25 MHz above the lowest frequency for the assigned channel, and the fre-

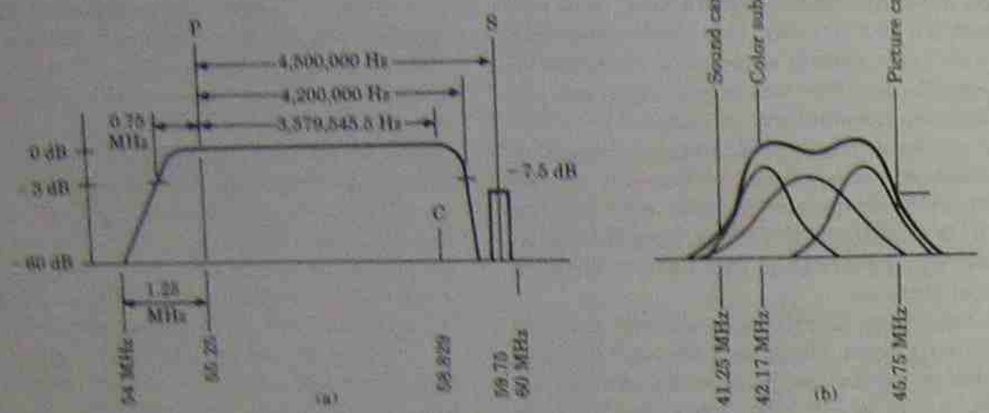


FIGURE 10.2
Vestigial sideband modulation: (a) band-pass response curve of a vestigial sideband transmission; (b) IF amplifier response curve to compensate for the loss of part of one sideband. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 619, Robert J. Schoenbeck, © 1992.)

quency-modulated sound carrier rest frequency is placed 4.5 MHz higher than the picture carrier frequency. All components of the transmitted signal voltage must be reduced by at least −60 dB at the upper and lower frequency limits of the assigned 6-MHz channel bandwidth.

10.4 MODULATED PICTURE PHASE

When amplitude modulating a carrier with an audio signal, the phase of the audio is not important. The recovered audio signal at the receiver causes the speaker cone to move in and out of the magnetic voice coil pole piece; the direction of the cone movement does not change the audio sound. The distance that the cone moves determines the loudness, and the rate of cone movement affects the pitch of the sound.

The video signal used to amplitude modulate the picture carrier has a direction for black and an opposite direction for white. The direction for white identifies the picture phase. Refer to Section 5.4.1 for clarification.

Figure 10.3a shows the amplitude of the sync pulses as the largest peak voltage in the modulated wave. The white portion of the video signal is in the direction of the zero carrier level. This polarity of modulation is called negative picture phase modulation and is used in the majority of nations throughout the world, including the NTSC system.

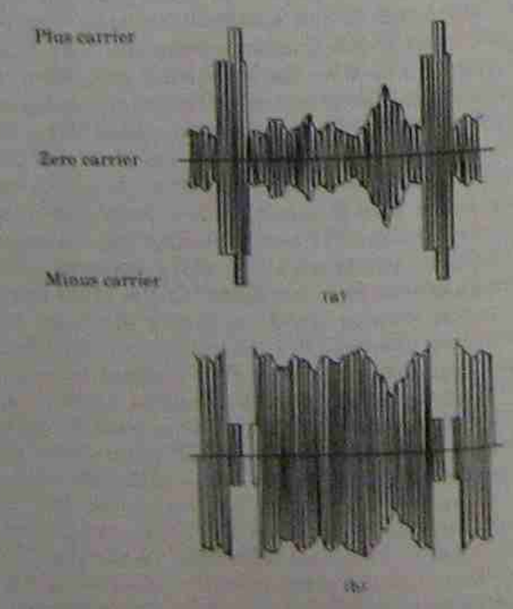


FIGURE 10.3
Video signal amplitude modulating a carrier signal: (a) negative picture phase-modulated carrier; (b) positive picture phase-modulated carrier. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 618, Robert J. Schoenbeck, © 1992.)

Most of the scenes to be televised are bright pictures in daylight or well-lit areas and result in the minimum carrier power for the brightest pictures. This is the major advantage of negative picture phase modulation.

Figure 10.3b represents *positive* picture phase modulation because the white levels of the scene cause the greatest modulated carrier amplitude. Here the sync pulse peaks reach zero carrier voltage. Overmodulation will compress the sync pulses in the positive picture phase mode, causing loss of picture synchronization, which cannot happen in negative picture phase modulation.

Noise pulses in the negative picture phase-modulated carrier appear as black specks and are less objectionable than the noise in the positive picture phase-modulated wave, which appears as white flashes.

10.5 FREQUENCY-MODULATED SOUND

To clarify some terms, video is the low frequencies that modulate the picture carrier. Audio is the low frequencies that modulate the sound carrier. In the same way that amplitude modulation means to change the amplitude of the modulated carrier wave, frequency modulation means to change the frequency of the modulated carrier wave.

There are two ways to frequency modulate the sound carrier. They are called *direct* and *indirect* frequency modulation. In the direct frequency-modulated transmitter, the carrier oscillator frequency changes in direct proportion to the amplitude of the modulating audio signal. The carrier oscillator frequency of the indirectly modulated system does not change; it is stable. The carrier frequency is changed in a circuit at the output of the carrier oscillator by changing the phase of the carrier signal. Indirect frequency modulation is also called *phase* modulation. You cannot change the phase of a signal without also changing the frequency of the signal during the time that the phase is changing. The two modulated waves seen in Figure 10.4 are so similar that the receiver cannot tell if the signal is phase or frequency modulated. It is only when you see the two waves together as in Figure 10.4 that you can see the 90° phase change in the modulated wave. Note also that the amplitude of the FM wave remains constant while the frequency changes with modulation. This constant amplitude produces the two major advantages of frequency modulation over amplitude modulation: (1) All known electrical noise disturbances show up in the transmitted signal as a change in amplitude (spikes of voltage), and since changes in amplitude are not a factor in frequency modulation, the FM wave is virtually noise free. (2) The constant voltage amplitude means constant output power from the FM transmitter that is independent of the percent of modulation.

10.5.1 Frequency Deviation

To deviate means to change. At zero percent modulation, the sound carrier is at its rest frequency, as seen in Figure 10.5a. Assume for the moment that a sine wave is used to frequency modulate this carrier. As the audio sine wave advances along its positive peak half-cycle, the frequency-modulated carrier advances to its highest frequency above the rest frequency. In doing so, the audio and carrier signals heterodyne to generate sidebands, as seen in Figure 10.5b. When the audio half-cycle returns to zero, the carrier returns to its rest frequency. On

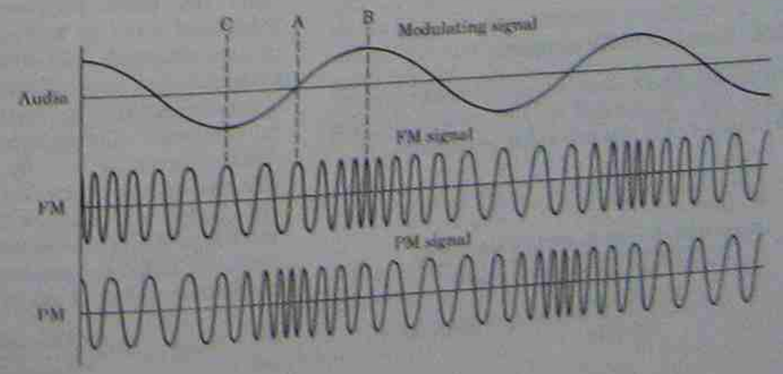


FIGURE 10.4
The relationship between the audio signal, the frequency-modulated carrier signal, and the phase-modulated carrier signal. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 170, Robert J. Schoenbeck, © 1992.)

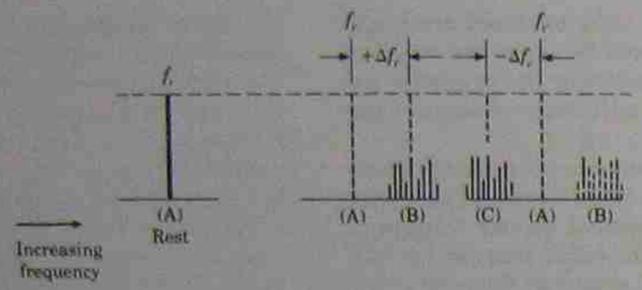


FIGURE 10.5
Frequency-modulated carrier wave shown in the frequency domain. Note the *constant* amplitude and the carrier frequency change at points A, B, and C. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 171, Robert J. Schoenbeck, © 1992.)

the negative half-cycle of audio, the carrier deviates below its rest frequency, as seen in Figure 10.5c, and generates the lower set of sidebands. When the carrier moves away from the rest frequency where the sidebands are developed, note that the voltage in the deviated carrier decreases as the sideband voltage increases. The *sum* of the voltages in the modulated wave at any given instant is equal to the voltage in the unmodulated carrier signal alone. The total voltage in the wave, modulated or unmodulated, remains constant. The carrier may change frequency to any value and not cause distortion in the modulated wave. Therefore, the change in frequency (called **deviation**) is limited by law for each class of FM service. FM radio has a maximum deviation of ±75 kHz from the rest frequency that defines 100% modulation, which for television monaural sound is ±25 kHz and for television stereo sound is ±50 kHz. Deviation identifies how far from the rest frequency the carrier changes; it is symbolized by Δf_c. Television sound has a deviation of 25 kHz and a **frequency swing** of 2 × 25 kHz = 50 kHz.

10.5.2 Percent of Modulation

When the television sound carrier is made to deviate ±10 kHz, controlled by the amplitude of a 4-kHz audio signal, the percent of modulation is

$$m = \frac{\Delta f_c}{\Delta f_{c\,max}} \times 100$$

$$= \frac{\text{measured change in carrier frequency}}{\text{maximum allowable change}} \quad (10.1)$$

$$\frac{10\text{ kHz} \times 100}{25\text{ kHz}} = 40\%\text{ modulation}$$

10.5.3 Deviation Sensitivity

This characteristic is associated with the modulator and establishes the value of peak audio voltage that will affect the peak carrier frequency deviation at the antenna. When 5-V_{pk} audio causes a 25-kHz carrier frequency change, the deviation sensitivity is

$$\frac{V_{pk}\text{ audio}}{\Delta f_{c\,pk}\text{ carrier}} = \frac{5\text{ V}_{pk}}{25\text{ kHz}}, \text{ or } 0.2\text{ V/kHz} \quad (10.2)$$

10.5.4 Modulation Index

Originally, the modulation index was known as the modulation factor, and although the name has changed over the years, the symbol has remained the same, mf. The modulation index ties the modulating audio frequency to the **rate of change** of the carrier frequency. This is the first application of the audio frequency in the frequency-modulation process. Basically, the audio frequency sets the separation space between the sidebands in the modulated wave. The modulation index is used to determine the exact number of sidebands in the modulated wave as well as the voltage and power in each sideband. This exercise is not required for understanding how FM works. However, if desired, a detailed explanation with examples can be found in *Electronic Communications: Modulation and Transmission*, 2 ed., by Robert J. Schoenbeck (Macmillan Inc., New York, 1992). The **modulation index** is a measure of the phase shift for any condition of the modulated FM signal at the antenna, in radians, compared to the phase of the unmodulated carrier alone. It is found by

$$\text{mf} = \frac{\Delta f_c \text{ at the antenna}}{f \text{ audio}} = \text{radians} \quad (10.3)$$

From the earlier example, where a 4-kHz audio signal caused ±10-kHz deviation, the modulation index is

$$\text{mf} = \frac{10\text{ kHz}}{4\text{ kHz}} = 2.5\text{ rad}$$

One radian equals 57.3°.

10.5.5 Deviation Ratio

The **deviation ratio** is the worst-case modulation index and describes the system's capabilities, rather than any actual signal condition. The deviation ratio compares the maximum allowable carrier deviation to the highest permissible audio frequency for each FM service. For television sound, the deviation ratio is

$$\text{deviation ratio} = \frac{\Delta f_{c\,max}}{f_{a\,max}} = \frac{25\text{ kHz}}{15\text{ kHz}}$$

$$= 1.67\text{ rad} \quad (10.4)$$

When the deviation approaches $\pi/2$ rads or less, the system is defined as narrowband FM, and when larger than $\pi/2$, it is wideband FM. Television sound has a deviation ratio of 1.67 rad and is considered to be narrowband FM. Broadcast FM radio has a deviation ratio of 75 kHz divided by 15 kHz = 5 rad and is classified as wideband FM. From this, you can conclude that both systems are minimum-noise, frequency-modulated systems with the highest audio frequency at 15 kHz; but because FM radio is wideband, it will sound better than the narrowband television sound signal.

10.5.6 Bandwidth

The bandwidth (BW) of the FM signal at the output of the transmitter is

$$\text{BW} = 2(\Delta f_c + f_a) \quad (10.5)$$

$$\text{max BW (TV sound)} = 2(25\text{ kHz} + 15\text{ kHz})$$
$$= 80\text{ kHz}$$

$$\text{max BW (FM radio)} = 2(75\text{ kHz} + 15\text{ kHz})$$
$$= 180\text{ kHz}$$

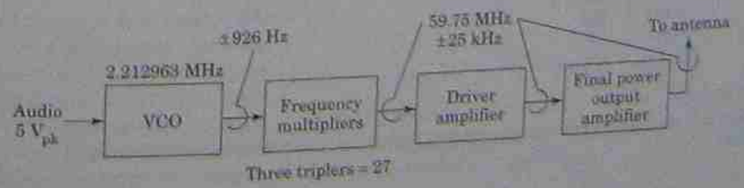


FIGURE 10.6
Block diagram for a *direct* frequency-modulated transmitter.

If you are knowledgeable of frequency-modulation principles, you may argue that there are sidebands beyond this calculation, and you would be right. However, the additional sidebands contribute less than 1% of the total power in the modulated wave and are therefore considered to be insignificant.

10.6 DIRECT FREQUENCY MODULATION

The voltage-controlled oscillator (VCO) in Figure 10.6 is a voltage to frequency converter. It has a free-running frequency of 2.213 MHz with no audio applied. The oscillator has a sensitivity of 185.2 Hz/V, so when 2-V_{pk} audio is applied, the oscillator output will be 2.213 MHz ±370.4 Hz. This signal is applied to the frequency multiplier section containing three frequency triplers for a total multiplication of 27. The carrier output from the oscillator is 27 × 2.213 MHz = 59.751 MHz, and the deviation is 27 × ±370.4 Hz = ±10 kHz. This is the sound carrier frequency for channel 2. It is modulated to (10 kHz divided by 25 kHz) × 100 = 40%. It would take 5-V_{pk} audio signal to change the VCO by ±926 Hz × 27 to equal ±25 kHz for 100% modulation.

Frequency multipliers are tuned input, tuned output RF amplifiers in which the output resonant circuit is tuned to a multiple of the input tuned circuit. When the input circuit is tuned to 2.213 MHz and the output circuit is tuned to 4.426 MHz, the amplifier is a frequency doubler. The output would need to be tuned to 6.639 MHz for the amplifier to be a frequency tripler. Frequency doublers and triplers are the most common of the frequency multipliers. The output signal level drops noticeably when higher multiplying factors are attempted. Push–push tuned RF amplifiers are rich in even harmonics and are used as frequency quadruplers (×4), while push–pull tuned RF amplifiers are rich in odd harmonics and are used as frequency quintuplers (×5) frequency multipliers. These higher-order frequency multipliers are more expensive and are generally avoided in favor of more, but cheaper lower-order frequency multiplier circuits. Frequency multipliers change the carrier frequency and deviation alike. There are no restric-

tions on the rest frequency of the oscillator (VCO) to be modulated or on the number or kinds of frequency multipliers to be used. The only restriction is on the output carrier rest frequency (selected by channel number) and the deviation limits at the output (±25 kHz for television sound).

10.7 INDIRECT FREQUENCY MODULATION (PHASE MODULATION)

Strangely enough, phase modulation starts out as amplitude modulation of a suppressed carrier (balanced modulation). Figure 10.7 shows that the same carrier used for balanced modulation is phase shifted by 90° and then added to the sidebands at the output of the double-sideband suppressed carrier (DSSC) balanced modulator. The net result at the adder output is seen in Figure 10.8 as the carrier voltage that is 90° out of phase from its modulated sideband voltages. The sideband amplitude changes in accordance with the applied audio signal so that the vector sum of the carrier and sideband voltages change the phase angle of the resultant (hypotenuse). The frequency changes only during the interval that the phase is changing. If the phase stops changing, the frequency stops changing. The change in frequency is seen as the change in phase angle (in radians) at the lowest audio frequency:

$$\Delta f_c = (\Delta\theta) f_a \text{ (lowest) Hz} \qquad (10.6)$$

It will reach a deviation of only about ±15 Hz before other conditions render the process unusable. The most damaging of these conditions is the change in amplitude of the FM wave. For safety reasons, the deviation is typically held to about ±10 Hz.

To raise ±10 Hz to 100% modulation of ±25 kHz, a multiplying factor of 2500 is required, but the number of frequency multipliers is not the biggest obstacle to be overcome. The challenge comes when trying to raise the carrier frequency and the deviation by the same amount through a common set of multipliers. The crystal-controlled carrier oscillator for channel 2 sound would need to operate at 23.9 kHz in order to be multiplied by 2500 for transmission at 59.75 MHz. Crystal oscillators work poorly below about 100 kHz. This problem is avoided by multiplying the carrier and deviation to a practical level and then heterodyning the carrier down to a lower frequency before the final multiplication to the station's output frequencies.

From Figure 10.8, a carrier voltage of 10 V_{pk} and a 90° phase shifted sideband voltage of 2.63 V_{pk} would (from the tangent expression) yield a phase angle of about 14.7351°. Divide by 57.3 to change degrees to radians for 0.25716 radian phase change. Equation 10.6 converts this radian change at 50 Hz to a deviation of ±12.86 Hz. This is the condition of the signal out of the linear adder shown in Figure 10.7. The first set of multipliers, one doubler and three triplers, provides a multiplication factor of 54, raising the carrier to 21.6 MHz and the deviation to ±694.44 Hz. The modulated signal is then heterodyned with a crystal-controlled oscillator signal of 23.25972 MHz at the mixer circuit. The by-products of heterodyning are the difference and sum frequencies of the two input signals. Since it is desirable to lower the carrier frequency, the output of the mixer is tuned to the difference

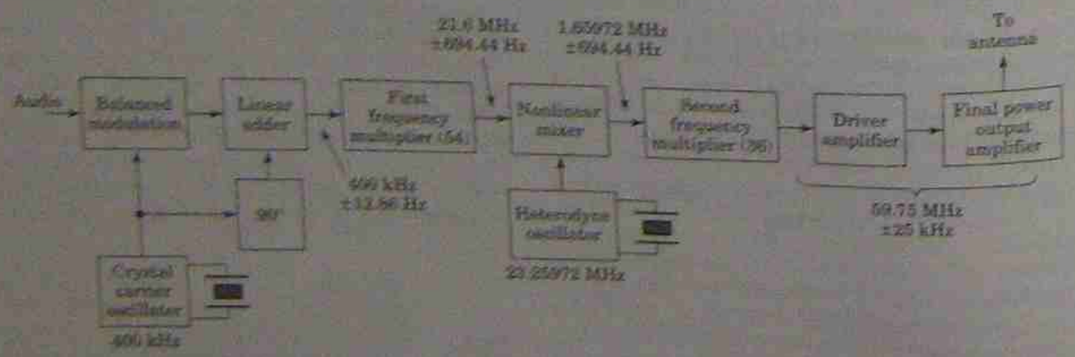
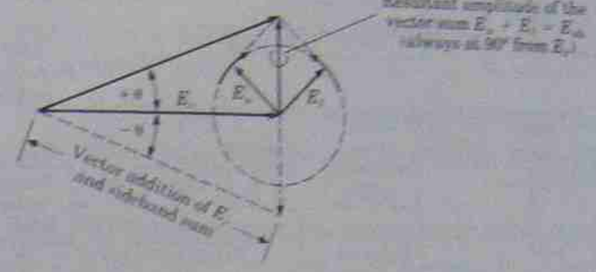


FIGURE 10.7
Block diagram of an indirect frequency-modulated (phase-modulated) television sound transmitter.

FIGURE 10.8
Vector analysis of the Armstrong phase modulator. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 193, Robert J. Schoenbeck, © 1992.)



frequency of 1.65972 MHz (23.25972 − 21.6 MHz). In the heterodyne process, the carrier frequency is changed, but the deviation is unaffected. The second set of multipliers with two doublers and two triplers will multiply the new carrier and deviation by 36. The driver amplifier and final power circuits do not affect the frequency of the signal, so the output to the antenna will be 1.65972 MHz × 36 = 59.75 MHz deviated to ±694.44 Hz × 36 = ±25 kHz for channel 2 sound. Almost all FM transmitters are phase modulated for television sound because of the stability of the crystal-controlled carrier oscillator.

10.8 MULTICHANNEL TELEVISION SOUND (MTS): STEREO

The concepts for FM stereo radio were so successful that it became a simple matter to convert the monaural sound channel to stereo for television. The problem of the subcarrier beat note at the 286th harmonic of the original horizontal frequency (4.5045 MHz) found in color systems was avoided by using multiples of 15,734.266 Hz for the sound channel. These higher-order prime frequencies, set as multiples of 15,734.266 Hz (H), became

$$1H = 15{,}734.266 \text{ Hz}$$
$$2H = 31{,}468.532 \text{ Hz}$$
$$5H = 78{,}671.329 \text{ Hz}$$
$$6.5H = 102{,}272.727 \text{ Hz}$$

Figure 10.9 shows where these signals, along with the associated audio messages, align in the frequency spectrum. The total range of frequencies out to 105 kHz is considered the audio signal that will modulate the FM carrier for television stereo sound. It also shows the level that each signal will deviate the main sound carrier and that several signals are double modulated. Figure 10.10 shows how the signals are combined to form the stereo signal plus the second audio program (SAP) and the voice or data professional channel.

The *left* audio signal, after amplification, is fed to linear adders 1 and 2. The *right* audio signal, after amplification, is fed to linear adder 1, where it and the left audio signal form the left plus right (L + R) monaural audio signal. The L + R signal is treated to reduce the noise (preemphasized). Both left and right audio signals occupy the frequency range of 50 Hz to 15 kHz, so the sum of the two signals is compatible with monaural sound transmission and deviate the station carrier to ±25 kHz.

The right audio signal is inverted and added to the left audio signal to form the left minus right (L − R) stereo channel signal. The L − R audio signal is treated for noise and amplitude compression by a Dolby noise reduction system (dBx). The L − R signal is balance modulated using a $2H$ carrier frequency to generate the double-sideband suppressed carrier (DSSC), amplitude-modulated stereo signal. This signal occupies the frequency band between 16.468 kHz ($2H$ − 15 kHz) and 46.468 kHz ($2H$ +

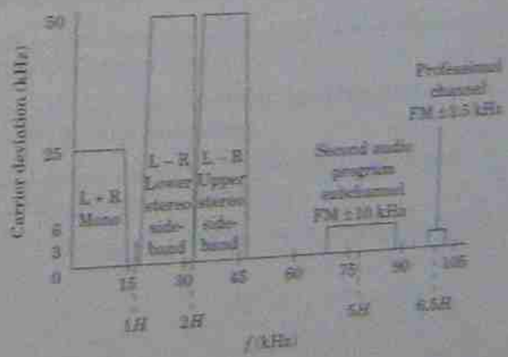


FIGURE 10.9
Frequency to deviation graph for the multichannel television sound (MTS) system.

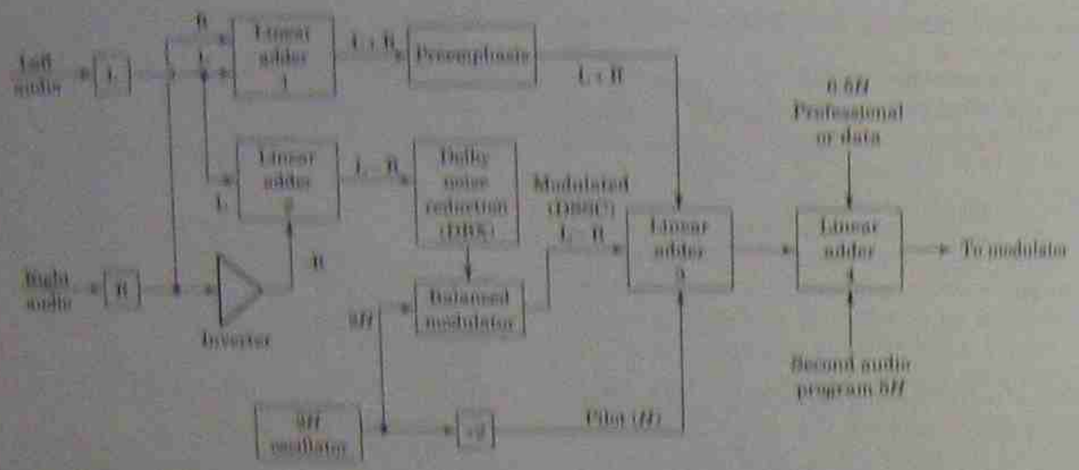


FIGURE 10.10
Multichannel television sound (MTS) transmitter block diagram for television stereo.

15 kHz) and will deviate the station carrier frequency to ±50 kHz. The L + R signal is added in the modulated L − R signal at adder 3. The 2*H* carrier signal is divided by 2 and reinserted into the audio band to serve as the pilot carrier used for recovery of the stereo program at the receiver.

The second audio program (SAP) channel is used for special message transmissions. A typical message would be the translation of a second language telecast or descriptive video services (DVS) to describe the scene and action in a telecast for the weak sighted. The SAP program is frequency modulated onto a 5*H* carrier with a deviation limit of ±10 kHz that can then deviate the station carrier to ±6 kHz. The industry has not taken full advantage of this SAP channel to any great extent, but it is in place for an "as needed" basis.

The professional channel is also a frequency modulated carrier at 0.5*H* with a frequency deviation of ±3.5 kHz, which will frequency modulate the station carrier to ±3 kHz. The professional channel is used for transmissions between station facilities and relay stations. It can be voice modulated to 3 kHz or modulated with data at a 1500-bps data rate.

Your attention is drawn to the extended use of double modulation. The stereo program is first amplitude modulated and then frequency modulated onto the station carrier. The SAP and professional programs are frequency modulated twice. The SAP and professional channels are given here for identification purposes only. They will not be explored in later chapters.

QUESTIONS

10.1 What is the frequency relationship between the carrier and the message signals?

10.2 At what frequency (and above) does the term RF begin to apply?

10.3 What channel numbers are included in the very high frequency television band?

10.4 What channel numbers are currently included in the ultrahigh frequency television band?

10.5 What is the bandwidth of each television channel in the NTSC system?

10.6 Do all world television systems have the same television channel bandwidth?

10.7 What is the highest video signal frequency allowed in the NTSC system?

10.8 Why is the video signal frequency limited to the answer you gave in Question 10.7?

10.9 What form of modulation is used for the picture signal in the NTSC system?

10.10 What form of modulation is used for the sound signal in the NTSC system?

10.11 How is the transmitted form of the picture-modulated signal changed from the typical modulation of the same form?

10.12 What is the name given to this special form of picture modulation?

10.13 What would be the frequency of the picture carrier for a fictitious NTSC television channel assigned to the frequency band of 135 to 141 MHz?

10.14 What would be the rest frequency of the sound carrier signal for a fictitious NTSC television channel assigned to the frequency band of 135 to 141 MHz?

10.15 What picture phase (positive or negative) is used to modulate the picture carrier signal in the NTSC system?

10.16 Is the modulated sound signal in the NTSC system considered to be (a) wideband FM, or (b) narrowband FM?

10.17 Define the carrier deviation that describes 100% modulation of the monaural sound signal in the NTSC television system?

10.18 Define the carrier deviation that describes 100% modulation of the FM stereo sound signal in the NTSC television system.

10.19 What is the percent of modulation when a 5-kHz monaural audio signal deviates the sound carrier at the antenna to ±18 kHz.

10.20 What characteristic of the audio signal would be varied in order to change the percent of modulation?
(a) amplitude,
(b) frequency,
(c) phase,
(d) tone, or
(e) none of the above

10.21 How does the deviation ratio compare to the modulation index?

10.22 How many times and in what form is the stereo program information modulated before being transmitted?

10.23 Including the monaural, the stereo, the SAP program, and the professional sound signals, what is the highest frequency used to modulate the station carrier signal?

11 Transmission Lines and Antennas

11.1 TRANSMISSION LINES

At the low end of the frequency spectrum, all connecting cables are just wires. Even the single conductor wire with an external braided sheath is called shielded wire. It is only when the signal frequency goes above about 200 kilohertz (kHz) that the wires begin to take on their own personality and act like transmission lines. The most important of these features is the impedance of the line, which remains fixed. It is called the **characteristic impedance** and uses the symbol Z_0. Above 200 kHz, the characteristic impedance is independent of frequency and the length of the cable. Z_0 becomes a function of the series inductive reactance and the shunt capacitive reactance:

$$Z_0 = \sqrt{2\pi f_L \times \frac{1}{2\pi f_C}} = \sqrt{\frac{2\pi f_L}{2\pi f_C}} \text{ ohms } (\Omega)$$

but since $2\pi f$ is the same in the numerator and the denominator, they cancel, removing frequency from the equation, and leaving us with

$$Z_0 = \sqrt{\frac{L}{C}}\ \Omega \qquad (11.1)$$

This equation provides us with the means to determine the characteristic impedance of the cable for any length when we can measure, or find from data sheets, the values of line inductance and capacity.

EXAMPLE 1

L=4.5 microhenries (μH)/100 ft and C = 50 picofarads (pF)/100 ft, Z_0 = 300 Ω.

A 750-ft cable has inductance of 33.75 μH and capacity of 375 pF. The impedance is 300 Ω also.

11.2 PHYSICAL CABLE MEASUREMENTS

When the inductance and/or capacity are unknown or cannot be measured, then the physical measurement of the cable can provide the data to determine the characteristic impedance. Here, all cables are divided into two family groups: (1) the flat two-wire parallel conductor cable and (2) the coaxial cable. Figure 11.1 shows these two family groups.

The flat two-wire parallel conductor cable in Figure 11.1a has an impedance equal to

$$Z_0 = 276 \log \frac{2D}{d}\ \Omega \qquad (11.2)$$

where D is the center-to-center distance between the wires and d is the outside diameter of either conductor. An *absolute* minimum impedance of 83 Ω is realized by moving the two wires closer together, just before they touch or short out, regardless of wire diameter. The 2 wires will stop acting like transmission lines and start acting like an antenna when the separation between the two wires be-

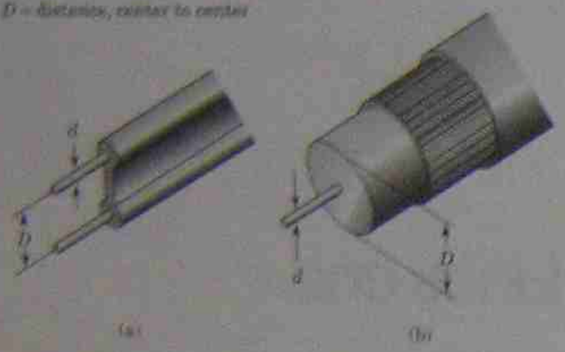


FIGURE 11.1
Transmission line: (a) two-wire parallel cable and (b) coaxial cable. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 275, Robert J. Schoenbeck, © 1992.)

comes greater than 0.2 wavelength (see Chapter 12). The maximum *practical* impedance for two-wire cable is about 600 Ω.

The term coaxial means to share the same center axis. That is, one wire is placed inside the other, as seen in Figure 11.1b. The characteristic impedance of coaxial cable is

$$Z_o = 138 \log \frac{D}{d} \ \Omega \qquad (11.3)$$

where D is the inside diameter of the larger conductor and d is the outside diameter of the smaller conductor. There are no minimum or maximum values of impedance for coaxial cables. As the space between the conductors gets smaller, the impedance decreases, and when the space gets larger, the impedance increases. Extremely small spacing (low impedance) becomes difficult and expensive to manufacture, while high impedances require that the outside diameter conductor be measured in miles. The smallest impedance is about 10 Ω, and the highest impedance for coaxial cables is about 225 Ω, with neither value being absolute. Examine the size ratio of the two conductors. If the ratio is greater than 49 or 50 to 1, chances are that you are going to be in trouble and will either have to find or make a cable to match your requirements.

The insulation that separates the two wires causes a change in the characteristic impedance. All insulating materials have a dielectric constant (ε, epsilon) that is compared to the dielectric constant of air. Air is set as 1 and, by comparison, all other materials range from 1.5 to about 1000. The average is about 2.5. When the cable has an insulation other than air, the fixed values in equations 11.2 (276) and 11.3 (138) are divided by the square root of the dielectric constant. In all cases, the impedance is made slightly smaller than when air is the dielectric.

11.3 STANDING WAVE RATIO

An axiom states that maximum power will be transferred to the load when the load impedance matches the line impedance; this is particularly true for transmission lines. When the load impedance does not match the line impedance, an endless number of possibilities exist. However, only three cases are meaningful: (1) when the load impedance is infinite (open circuit), (2) when the load impedance matches the line impedance ($Z_0 = Z_L$), and (3) when the load impedance is short circuited ($Z_0 = 0$). Case 2 is the ideal, where all the energy sent down the line is absorbed by the load.

In case 1, the source energy sent down the line to the load sees an open circuit. An open circuit cannot absorb energy, so all the energy will be reflected back up the line to the source.

In case 3, the source energy sent down the line to the load sees a short circuit. A short circuit cannot absorb energy, so all the energy will be reflected back up the line to the source.

In cases 1 and 3, the energy returning to the source adds to the energy coming from the source at points where the two energies are in phase. They cancel at points where the two energies are out of phase. As a result, a standing wave of voltage appears along the line that is stationary. It does not move. Figure 11.2 shows that the peak of the voltage standing wave is two times the source peak voltage. Furthermore, where there is voltage and impedance, there will be current. A current standing wave will appear along the line that is 90° out of phase from the voltage standing wave. The null points (and peak points) of voltage are one half-wavelength apart.

Cases 1 and 3 are not exactly the same. In case 1, Figure 11.2a, current cannot flow in an open circuit; therefore, at the load end of the line the voltage is maximum and current is minimum. In case 3, Figure 11.2b, current is maximum in a short circuit and voltage is minimum at the load. The

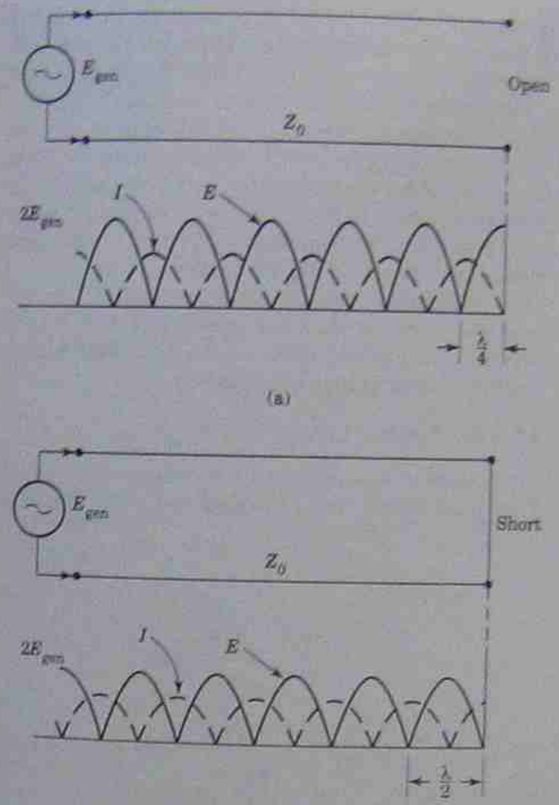


FIGURE 11.2
Voltage standing waves on transmission lines: (a) voltage standing wave for an open load; (b) voltage standing wave for a shorted load. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 288, Robert J. Schoenbeck, © 1992.)

voltage standing wave in the two cases is 90° out of phase.

The ratio of energy sent down the line to the energy absorbed by the load is called the **standing wave ratio;** 100% of the energy sent divided by 100% absorbed = 1, the ideal case. One hundred percent sent divided by 50% absorbed results in a SWR of 2 : 1. A ratio of 1 : 1 is ideal, 2 : 1 is poorer, and 3 : 1 is worse yet. Larger numbers mean greater losses.

When two-wire parallel lines are used outdoors, they absorb moisture and the impedance varies, but they are fairly stable indoors. Coaxial cables have lower impedances and often do not match the impedance of the antennas or the television receiver. Impedance matching transformers are used at the antenna to match the antenna impedance to the cable impedance and again at the receiver to match the cable to the television set input impedance.

11.4 ANTENNAS

Whole books have been written about antennas. The subject appears boundless and indeed it may be. We do not know everything about antennas, but from the vast store of information gathered to date, the one concept that is most obvious is the relationship between antenna size and one half-wavelength at the operating frequency.

There are three basic models that describe how an antenna launches energy into the surrounding atmosphere:

1. The isotropic source
2. The elementary doublet
3. The half-wave dipole

Types 1 and 2 are primarily theoretical tools used to develop antenna principles; therefore, we will concern ourselves only with aspects of the half-wave dipole antenna. All practical antennas are modified forms of the basic half-wave dipole antenna.

11.4.1 Reciprocity Theorem

The behavior of every antenna is reciprocating. That is, the antennas will have identical characteristics for transmitting and receiving, except for power-handling capabilities. A 1-megawatt (MW) transmitting antenna may conduct 60 amperes (A) of current while the receiving antenna in the same system may conduct only about 60 microamperes (μA) of current, so the wire size will be different. All other features will be the same.

11.4.2 Wavelength

The Greek letter lambda (λ) is used to represent wavelength. The physical length of one cycle of energy is found by comparing the velocity of light (and radio waves) to the frequency of the signal energy:

$$\lambda = \frac{c}{f} \qquad (11.4)$$

where c = velocity of light
f = frequency in hertz

Although c is the standard notation for the velocity of light, the abbreviation V_c is sometimes used; be

alert to both symbols. You will want to use the speed of light that corresponds to the rest of your measurements; therefore,

$$\begin{aligned} c &= 186{,}400 \text{ miles/second} \\ &= 984 \times 10^6 \text{ feet/second} \\ &= 300 \times 10^6 \text{ meters/second} \\ &= 300 \times 10^8 \text{ centimeters/second} \\ &= 1.1808 \times 10^{10} \text{ inches/second} \end{aligned}$$

One wavelength (in inches) at a frequency of 59.04 MHz is

$$\lambda = \frac{1.1808 \times 10^{10}}{59.04 \times 10^6} = 200 \text{ inches}$$

11.4.3 Half-wave Dipole Antenna

The half-wave dipole antenna is the basic element from which all other antennas are developed. Figure 11.3 shows that the half-wave dipole is split at the center where the signal is applied. The size of the split has no effect on impedance when the frequency of the signal exceeds about 14 MHz. Above this value, the measured input impedance is about 73 Ω. At the ends of the antenna rods, where current is minimum, the antenna looks capacitive to the air that surrounds the antenna. To compensate for capacitive effects, the rod is made slightly shorter than the calculated length. The exact reduction in size depends on the material used to make the antenna. It ranges from about 0.93 to 0.96 of the calculated length. This text uses 0.95 in all examples for an average. The real half-wave dipole from Section 11.4.2, at 59.04 MHz, then becomes (200 inches/2)0.95 = 95 in.

Current moves freely into and out of the center feed point of the antenna, but at the ends of the rods, the current diminishes to zero because the ends are an open circuit where no current can flow. The antenna current and voltage are 90° out of phase so that at the center, where current is high, the voltage is low. At the ends of the antenna, where current is low, voltage is high. Review open-ended transmission lines as needed. Because the length of the antenna is one half-wavelength, one end of the antenna is high positive while the other end is high negative. This half-wave of standing voltage is necessary to generate the electric field and magnetic field around the antenna that develops the radiated energy to leave the antenna. From basic electricity, you recall that passing a current through a wire creates a magnetic field around the wire. The electric field builds from end to end of the antenna like the lines of force between the poles of a magnet. The magnetic field stays within one half-wavelength of the antenna, while the electric field radiates from the antenna to establish the antenna's polarity. The physical attitude of the antenna determines its polarization. An antenna lying flat with the horizon is horizontally polarized, while one standing up like a flag pole is said to be vertically polarized. The sending and receiving antennas should both be polarized in the same plane.

No signal is emitted from the ends of the antenna, so it has a radiation pattern of 360° that is perpendicular to the plane of the antenna. A half-pattern is seen in Figure 11.3b.

11.4.4 Folded Dipole Antenna

An expansion of the basic dipole antenna is seen in Figure 11.4b as the *folded dipole* antenna. Although there are many similarities between the two basic types, the differences are noteworthy.

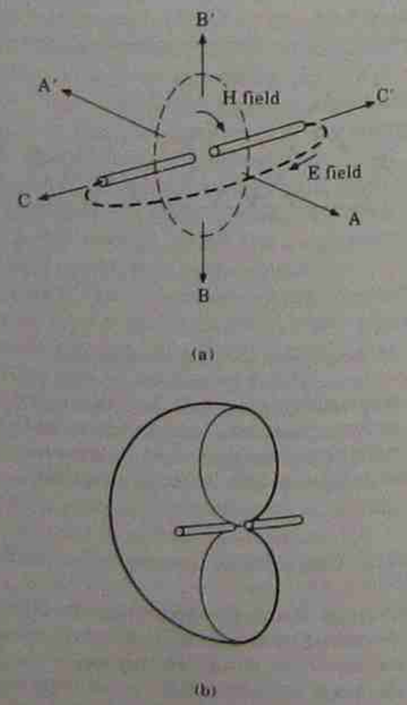


FIGURE 11.3
(a) Electric and magnetic fields of a half-wave dipole antenna. Energy propagates toward *A*, *A'*, *B*, and *B'* but *not* toward *C* or *C'*. (b) Half-field radiation pattern. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 335, Robert J. Schoenbeck, © 1992.)

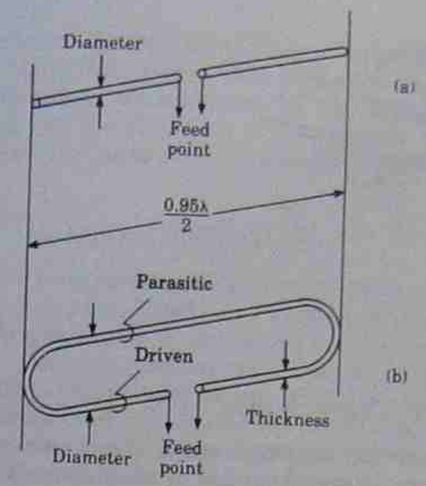


FIGURE 11.4
Comparison of the Hertz half-wave dipole (a) and the folded dipole (b) antennas. The diameter determines the antenna *Q*. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 341, Robert J. Schoenbeck, © 1992.)

The folded dipole input impedance is found by multiplying the dipole impedance (73 Ω) times the square of the number of bars in the folded dipole:

$$Z_{fd} = 73(N^2) = 73(2^2) = 292\ \Omega \qquad (11.5)$$

In general terms, the dipole is called a 75-Ω antenna, while the folded dipole is called a 300-Ω antenna.

Antennas are like resonant circuits in that they have a center frequency, a circuit *Q*, and bandwidth. Notice in Figure 11.4b that the diameter includes the distance *D* of the two bars and the length (*L*) equal to one half-wavelength. The *Q* is then found as

$$Q = \frac{L}{2D} \qquad (11.6)$$

where *D* is the diameter in Figure 11.2.

The folded dipole has a lower *Q* than the basic dipole and therefore has a wider bandwidth. Knowing the center frequency and the *Q*, you can use basic resonant circuit theory to find the bandwidth.

11.4.5 Antenna Gain

Turn a flashlight on in a darkened room and observe the spot on the wall. Now, take the flashlight apart, hold the bulb in your fingers, and attach the batteries in series with the bulb using hook-up wire. Observe the light displayed by the bulb. What conclusions can you draw from these observations?

- *Fact*: Using the same bulb and same batteries, the light output from the bulb is the same in both cases.
- *Fact*: With the bulb in your fingers, the light output is scattered in all directions. When the bulb is in the flashlight, the same amount of light is focused all in one direction.

It is in this context that we can talk about antenna gain. A piece of wire cannot have gain, but when all the antenna's radiated energy is focused in one direction, the antenna will transmit (or receive) best in that direction. It is said to have gain, compared to a half-wave dipole antenna alone. The power gain is expressed in decibels (dB) and should really be called *directivity gain*.

11.5 PARASITIC ARRAYS

The dipole and folded dipole have a signal applied at the center of the antenna. This piece of the assembly is called the *driven element*. Another rod placed parallel to (but not touching) the driven element will absorb and reradiate energy from the driven element. The additional rod is called a *parasitic element*. When the parasitic element is placed in the favored direction for radiation, called the front of the antenna, it becomes a *director*. When placed away from the favored direction, called the back of the antenna, the rod becomes a *reflector*. See Figure 11.5 for these details.

Directors are evenly spaced at 10% of one full wavelength and get progressively shorter by 5% as the distance from the driven element increases. For the case cited in Section 11.4.3, where the driven element was 95% of one half-wavelength = 95 in., the first director is 0.95 × 95 in. = 90.25 in. and is placed 20 in. away from the driven element. Director 2 is 0.95 × 90.25 in. = 85.7275 in. long and is placed 20 in. away from director 1.

Reflectors are evenly spaced at 15% of one full wavelength and get progressively longer by 5% as the distance from the driven element increases. For the same antenna, the first reflector is 1.05 × 95 in. = 99.75 in. long and is placed 30 in. away from the driven element. The second reflector (if there were

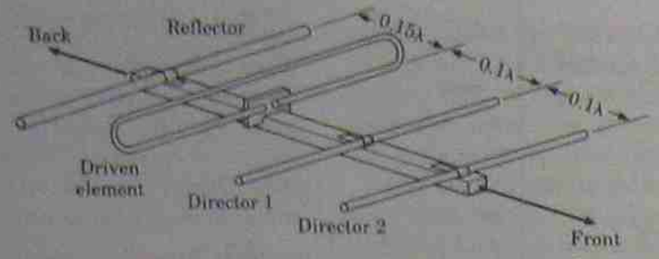


FIGURE 11.5
Assembly of a parasitic array, with a folded dipole driven element, one reflector, and two directors. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 346, Robert J. Schoenbeck, © 1992.)

one) is 1.05 × 99.75 in. = 104.7375 in. long and is placed 30 in. away from reflector 1.

Reflectors increase the antenna gain in the same way that directors do, but reflectors also reduce the signal pickup from the back of the antenna. Normally, only one reflector is used.

Adding more parasitic elements means greater gain. However, the gain curve (versus number of elements) is parabolic (like a capacitor charge curve). A point can be reached where adding one more element will increase the gain so little that it becomes undesirable when compared to the increased antenna size and the heavier wind-resistant antenna mount required to support the structure. Antenna gains of 15 dB are fairly common. Greater gains begin to identify specialty items.

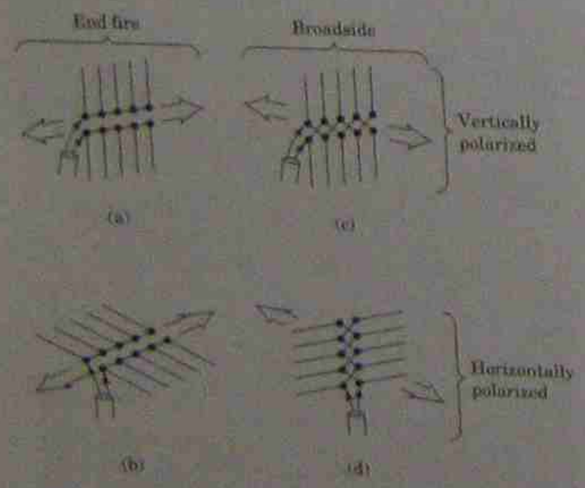


FIGURE 11.6
Driven array antennas: (a) and (b) are end fire, and (c) and (d) are broadside; (a) and (c) are vertically polarized, while (b) and (d) are horizontally polarized.

11.5.1 Driven Arrays

A drive array antenna, compared to a parasitic array, has the signal applied to every element of the antenna assembly. All elements are driven elements and none are parasitics. Figure 11.6 shows two types of driven array antennas. End-fire arrays have all elements fed in parallel. The spacing between the rods may be varied to make the antenna array either bidirectional or unidirectional. Broadside antennas are parallel fed with alternating phase to successive elements. The broadside is bidirectional, but it can be made unidirectional by placing a grounded wire screen behind the array that does the same job as a reflector element.

11.6 STACKED ANTENNAS

Any antenna gain may be increased by adding another antenna of like kind directly above one another and spaced one half-wavelength apart. Doubling the antenna size doubles the antenna power gain (+3 dB). To double again, four antennas are needed. To double once more, eight antennas are needed. Each time the area of the antenna is doubled, +3-dB gain is added. The individual antenna section is called a *bay*, so for any number of bays the total gain is

$$\text{power gain (dB)} = 10 \log N \qquad (11.7)$$

where N equals the number of bays. Eight stacked bays have a gain of $10 \log 8 = 9.0309$ dB greater than one antenna alone. You can see that eventually the increased antenna size is not worth an additional +3-dB gain. The beam spread (beamwidth) does not change. Placing two like antennas side by side would increase the beamwidth but not change the antenna gain.

There is an endless number of possibilities with antennas. We will not cover them all. You can begin to see the little bit of magic in antenna selection. Many factors may vary, such as the number and spacing of the elements, the way they are connected, and the placement of the elements. Choose the best antenna that fits your budget.

11.7 MARCONI ANTENNAS

Imagine construction of a half-wave dipole to operate at 540 kHz. Ninety-five percent of one half-wavelength is 865 ft and would be very cumbersome. Marconi discovered that a vertically polarized antenna need be only 95% of one *quarter*-wavelength and that Earth will act like the other quarter-wavelength of the dipole antenna. See Figure 11.7 for this effect. The Marconi antenna for a 540-kHz carrier is a 432.78-ft tower. The entire tower is the antenna and will radiate a vertically polarized field of energy in all 360 compass degrees.

11.8 PARABOLIC REFLECTORS

What has become known as a *dish* antenna is in reality a parasitic array antenna with a parabolic reflector. The reflector is a focusing lens with the antenna at the focal point of the lens. The polarity of the system is established by orientating the antenna rotation. Parabolic reflector antennas are primarily used at microwave (satellite) frequencies. Your flashlight and automobile headlamps use a parabolic reflector. The filament of the flashlight bulb or headlight is placed at the focal point of the parabolic reflector. The advantages of parabolic reflectors are extremely high power gains (to 50 dB) and a very narrow beamwidth angle that can be as small as 1°.

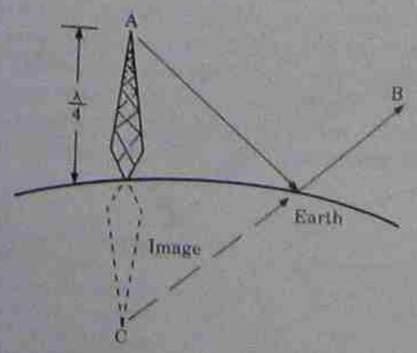


FIGURE 11.7
Basic Marconi quarter-wave antenna. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 366, Robert J. Schoenbeck, © 1992.)

The diameter (D) must be a minimum of two wavelengths at the center frequency and typically measures from 6 to 18 ft, with larger diameters producing the highest gain. The depth (d) ranges from a few inches to a few feet. Both the depth and diameter can be measured with a ruler. See Figure 11.8.

The focal point (F), where the antenna is placed, is a function of both the depth and the diameter, stated in the same units as D and d, and is found as

$$\text{focal point } (F) = \frac{D^2}{16d} \qquad (11.8)$$

A 108-in.-diameter dish 18 in. deep would have a focal length of 40.5 in. The focal length is measured from the inside back surface of the reflector.

The ratio of depth to diameter determines both the gain and the beamwidth angle. A shallow dish will have less gain than a deeper dish for the same diameter. Like all parasitic array antennas, less gain produces a wider beamwidth angle. Also, higher frequencies yield higher gains for a given parabolic reflector.

When needed, the gain can be calculated from the physical measurements as follows:

$$\text{power gain (dB)} = 10 \log \left\{2 + \left[\frac{d}{D}\left(\frac{\pi dD}{3\lambda}\right)^2\right]\right\} \qquad (11.9)$$

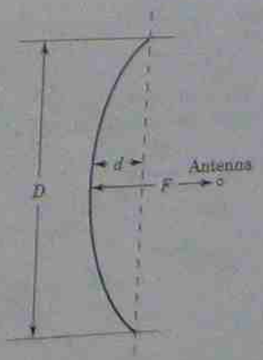


FIGURE 11.8
Parabolic reflector (dish), showing the diameter (D), the depth (d), and the focal length (F) where the antenna is placed.

At 4.6 gigahertz (GHz), wavelength = 2.567 in.

$$\text{gain} = 10 \log \left[2 + \left[\frac{18}{108}\left(\frac{3.1416 \times 18 \times 108}{3 \times 2.567}\right)^2\right]\right]$$
$$= 50.2 \text{ dB}$$

and the beamwidth angle is

$$\theta - 3 \text{ dB} = 2 \arctan \frac{\lambda F}{d^2 D} \text{ degrees} \quad (11.10)$$

$\theta = 0.34°$ in this case.

EXAMPLE 2

A 10-ft (120-in.) diameter dish that is 11.25 in. deep is to operate at 4723.2 MHz. Determine the power gain in decibels and the beamwidth angle.

Solution

1. You will need to know the wavelength (2.5 in.).
2. The focal point from eq. 11.8 is 80 in.
3. The power gain from eq. 11.9 is 44.768 dB.
4. The beamwidth angle from eq. 11.10 is 1.509°.

Did you arrive at the same answers?

Raise the frequency to 11.808 GHz and you will see the power gain increase to 52.727 dB and the beamwidth angle shrink to 0.6°.

11.9 WAVE PROPAGATION

Several facts about radio wave propagation will be of value to you when installing or servicing communication systems. It will serve well to know some basics about the atmosphere itself, the different types of waves, how they travel through the atmosphere, and how distance and frequency affect signal strength. It is assumed that the transmitting and receiving antennas are both polarized in the same plane. The three types of waves are

1. Ground waves
2. Sky waves
3. Space waves

11.9.1 Atmosphere Layers

Our globe is surrounded by a 300-mile gaseous layer called the **atmosphere.** The 2 miles closest to the surface contain enough oxygen to sustain life. Above that, as seen in Figure 11.9, the oxygen mixes with ionized molecules, which have been bombarded by ultraviolet rays from the sun and cosmic rays from space.

In full sunlight, the D, E, F_1, and F_2 layers are clearly defined. At night, the D layer disappears, the E layer almost disappears, and the F_1 and F_2 layers combine to form a single F layer.

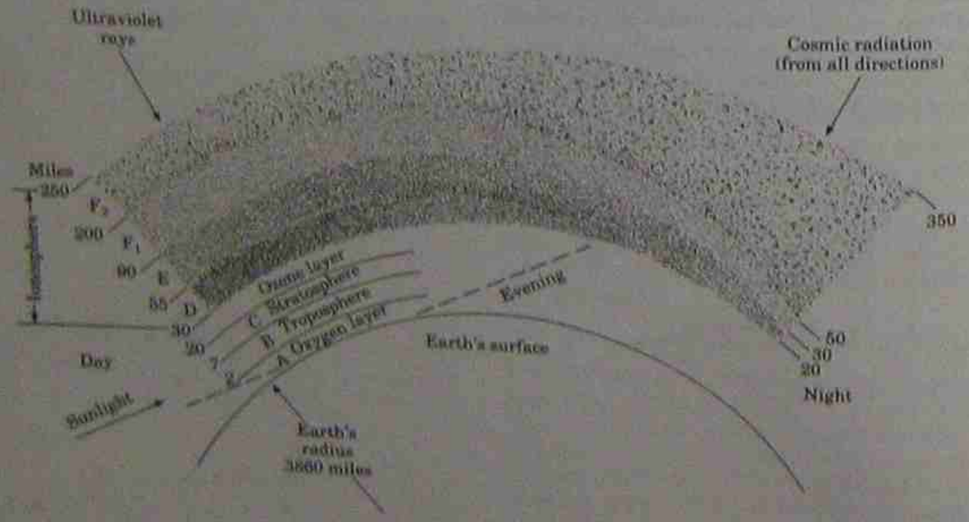


FIGURE 11.9
Atmospheric layers of earth.
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This pattern is compounded by seasonal changes, that is, hot summer sunlight compared to cool winter sunlight. Knowledge of these conditions will help you to understand why radio waves propagate farther at night than they do during daylight hours.

11.9.2 Ground Waves

Ground waves are emitted from a vertically polarized Marconi-type antenna. They tend to follow the curvature of Earth and travel the greatest distance, but are generally limited to frequencies below a few megahertz. The moisture content of Earth's surface is the key to good ground wave transmission, with salt water rated as best and arid desert lands as poorest. Vertically polarized signals at higher frequencies propagate by sky waves rather than ground waves.

11.9.3 Sky Waves

Sky waves are those waves that stay within our atmosphere. These waves are generally (but not always) horizontally polarized and rely on line-of-sight transmission. That is, the receiving antenna must be in view of the transmitting antenna. See Figure 11.10. It is also seen in Figure 11.10 that some portion of the transmitted signal may arrive at the receiving antenna by three different routes. The direct path signal is the strongest signal to arrive at the receiver. A small portion of the signal strikes Earth's surface, changes phase by 180°, and is reflected to the receiving antenna. Fortunately, this out-of-phase signal is greatly reduced by ground absorption and very little signal arrives at the receiving antenna. Another small portion of the signal propagates above the direct path by a route called the *refracted* path. This wave enters the ionosphere layer and is gradually bent (refracted) until it returns to Earth with no phase change. The amount of signal to arrive at the receiving antenna

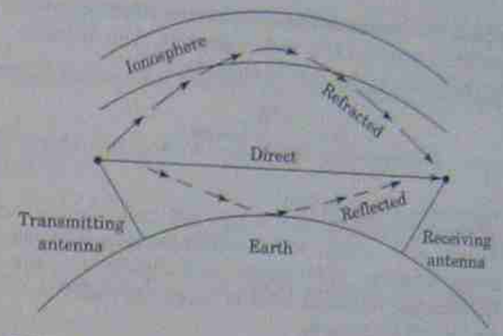

FIGURE 11.10
Three routes of the sky wave. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 385, Robert J. Schoenbeck, © 1992.)

by the refracted sky wave route is also small compared to the direct-route signal strength.

11.9.4 Space Waves

The sky waves that radiate at angles above the horizon enter the ionosphere and are refracted back to Earth. Increasing the angle above the horizon will eventually attain a direction where the amount of refraction (bending) will no longer be great enough to return the signal to Earth. At some critical angle above the horizon, the RF waves penetrate the ionosphere and venture out into free space. These space waves may be vertically or horizontally polarized and are the prime media for microwave communications to satellites.

11.10 ANTENNA HEIGHTS

You can see from Figures 11.10 and 11.11 that the curvature of Earth interferes with the direct signal between the two antennas as they get farther

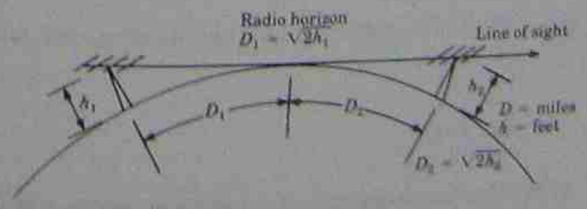

FIGURE 11.11
Radio horizon compared to antenna height.
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apart. To overcome this interference, the receiving antenna is raised to a higher position. The distance to the horizon (in miles) is found by

$$D = \sqrt{\frac{3h}{2}} \text{ (miles)}$$

where h is height in feet.

Thus a 6-ft person will see the horizon 3 miles away. However, radio waves bend slightly over the horizon and establish what is called the radio horizon, which is found by

$$D = \sqrt{2h} \text{ miles} \qquad (11.11)$$

Transmitting antennas are permitted to be 2000 ft above the average terrain. The average terrain is the average elevation within 10 miles of the transmitter site measured in eight equally spaced directions. A 2000-ft-high antenna will have a radio horizon of 63 miles in all directions. Within this circle, the receiving antenna may be at any convenient height. At the fringe of this area or distances beyond, the receiving antenna is elevated to a height that will satisfy the line-of-sight condition by using equation 11.11. A receiver 90 miles from the transmitter must be raised to a level that corresponds to a 27-mile horizon (90 − 63 = 27). The receiving antenna is raised to 365 ft (working equation 11.11 backward) in order to see the transmitter above the horizon.

QUESTIONS

11.1. Above what frequency do cables begin to act like transmission lines?

11.2. What is the characteristic impedance of a cable that has an inductance of 9.775 μH per 1000 ft and capacitance of 390 pF per 1000 ft?

11.3. What is the characteristic impedance of a flat two-wire parallel cable that uses 0.063-in.-diameter wire spaced ¼ in. apart?

11.4. What is the characteristic impedance of a coaxial cable with a 1.41-in.-diameter center conductor on the inside of a copper pipe that measures 3½ in. ID?

11.5. There should be standing waves along the transmission line.
(a) yes.
(b) no.
(c) sometimes

11.6. What load conditions would ensure that no standing waves appear along the line?

11.7. There should be standing waves on the antenna.
(a) yes.
(b) no.
(c) sometimes

11.8. Which of the following is the best standing wave ratio?
(a) 0.5 : 1
(b) 1 : 1
(c) 2 : 1
(d) 3 : 1
(e) 10 : 1

11.9. How long is one cycle of energy (in meters) at 4 MHz?

11.10. How many inches long is the same wave at 4 MHz?

11.11. How many feet long is the same wave at 4 MHz?

11.12. In what terms is the final expression stated for feet per second divided by cycles per second?

11.13. How many feet long would you make a half-wave dipole antenna to operate at 75 MHz?

11.14. How many inches long would you make a folded half-wave dipole antenna to operate at 540.6 MHz?

11.15. Using Figure 10.15 as a sample, find the length and spacing between the four elements (in feet) when operated at 90.49 MHz.

11.16. Describe how you would place a pencil on a sandy beach to demonstrate vertical polarization.

11.17. How much power gain would a nine-bay stacked array antenna have?

11.18. What size of antenna tower would be needed at the receiving station 30 miles away when the horizontally polarized transmitting antenna is on top of a 450-ft building?

12 Television Receivers

12.1 INTRODUCTION

Troubleshooting a circuit is not a big problem for the majority of technically oriented people. We do this every time we build a circuit. The problem arises in analyzing a system to determine which of the many circuits needs attention. In this respect, the analyst must know beforehand what the system is supposed to do, have a mental picture of the circuits within the system that are needed to perform the functions, and then be able to recognize normal and abnormal performance. The next problem may be to find the suspect circuit on the receiver chassis. Service manuals are extremely helpful for finding the location of the circuits, as well as supplying the circuit connections and applicable voltages at all points of interest. This chapter will deal with these situations using a top-down approach to troubleshooting.

12.2 RECEIVER BLOCK DIAGRAM

Regardless of the brand name of the product or the endless possibilities for circuit configurations, every television receiver will have the same basic block diagram. Heading the list of similarities in the receiver diagram is the **superheterodyne** concept of receiver configuration. In this process, the high-frequency station carrier signal received at the antenna is converted down to an **intermediate**-frequency carrier for amplification. Channel 2's picture carrier signal at 55.25 megahertz (MHz) is reduced to 45.75 MHz, and when tuned to channel 10, the picture carrier frequency of 193.25 MHz is also reduced to 45.75 MHz. Each channel, as it is selected, sees its picture carrier signal converted down to the common intermediate picture carrier frequency of 45.75 MHz.

The block diagram in Figure 12.1 is used to explain the functional role and the sequencing of the circuits in a typical television receiver. Knowingly or otherwise, you will eventually memorize a receiver block diagram like the one in Figure 12.1. So, if you plan to work and succeed in an environment that includes television, memorize each section of the block diagram as it is presented in this chapter.

This chapter, developed around Figure 12.1, will explain the circuit functions in detail, and the following chapters will discuss some circuits in common use for each section.

12.2.1 VHF Tuner

The section of the receiver called the *tuner* or *front end* is highlighted in Figure 12.2. This is generally a separate chassis mounted away from the main part of the receiver proper. It starts at the antenna input terminals and ends at the output of the mixer amplifier. This output signal is the reduced frequency carrier signal that goes to the intermediate-frequency amplifiers. Tuners are always enclosed in a grounded metal box that prevents external signals from getting into the tuner and affecting its operation. The enclosure also prevents the internal oscillator signal from seeping out to cause disturbances elsewhere.

There are only three signal circuits in the VHF tuner that perform three basic functions. The

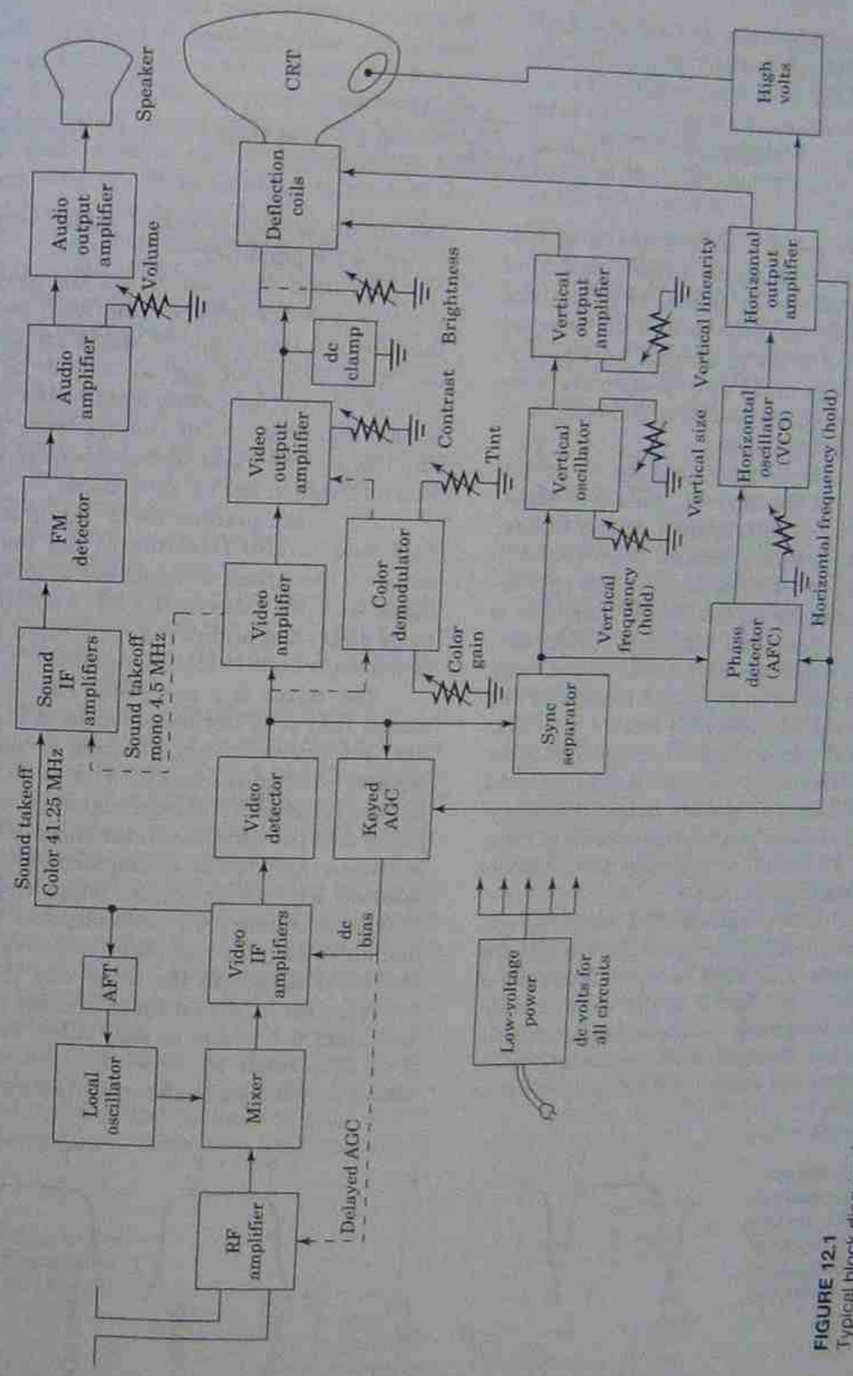
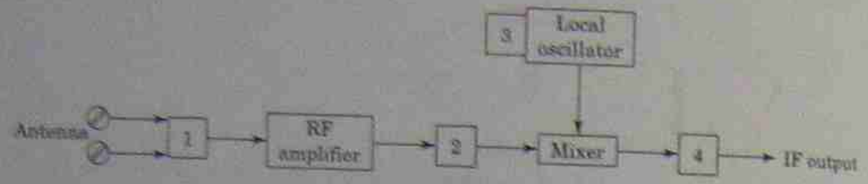


FIGURE 12.1
Typical block diagram for a television receiver.

FIGURE 12.2
Slightly expanded block diagram for a typical VHF tuner.



first function is to select a station carrier signal. The second function is to supply a small amount of gain to the selected carrier signal, and the third function is to lower the frequency of the selected carrier signal down to the intermediate frequency. All additional circuits in the tuner section are associated with the automatic operation of the tuner or the remote control of the tuner.

The antenna signal going into the RF amplifier (Figure 12.2) is the cleanest, noise-free signal that will be found at any point in the entire receiver. Each circuit that processes the signal will add a token amount of noise to the noise that already contaminates the signal. The RF amplifier is designed to be a low-noise amplifier (LNA) that supplies a small amount of gain to the signal without appreciably affecting the noise content of the signal. The tuned RF amplifier selects a 6-MHz bandwidth signal (using block 1 in Figure 12.2) for each channel within the VHF television range of 54 to 216 MHz (162-MHz frequency range). Therefore, from a gain–bandwidth and low-noise point of view, the wideband RF amplifier typically has a gain of about 10 decibels (dB) (3.1623).

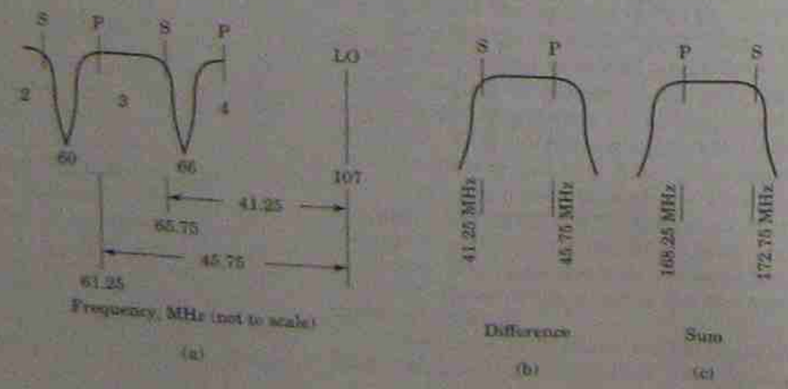
The circuit that couples the RF amplifier output to the mixer input (2 in Figure 12.2) is also frequency selectable. The input and output circuits of the RF amplifier are tuned to the same channel number. When switching channels, both tuned circuits 1 and 2 are changed at the same time to accept the new channel selection. A full description of this circuit is then a tuned input, tuned output, low-noise RF amplifier.

The final function of the RF amplifier is to serve as a buffer between the local oscillator and the antenna terminals. Without an RF amplifier, the local oscillator signal would be connected through the circuit components to the antenna terminals and would then radiate from the antenna into the air and cause disturbances to other television receivers in the neighborhood.

The exact placement of the ground connections and careful selection of the materials that make up the circuit components help to control the signal-to-noise ratio of the RF amplifier. Prudent parts placement and precision printed wiring board layout contribute to circuit stability.

The mixer is a nonlinear RF amplifier. This means that it is not operated as a class A amplifier, but rather in some degree of class B, which distorts the input signals. The two input signals are the selected RF carrier signal from the RF amplifier and the local oscillator signal. The oscillator is always operated at a frequency higher than the selected RF carrier signal frequency, and it too changes frequency for each channel selected. Unlike an adder, the nonlinear mixer responds to its two input signals in the same way that a modulator responds. The two input signals of the nonlinear mixer are added to each other and subtracted from each other to cause the *sum* and *difference* signal frequencies at the mixer output. Figure 12.3

FIGURE 12.3
Frequency response action of the tuner mixer: (a) channel 3 of 60 to 66 MHz and local oscillator of 107 MHz; (b) the difference frequencies; (c) the sum frequencies.



is an example of how this works when channel 3 is selected. Channel 3 has a picture (P) carrier frequency of 61.25 MHz and a sound (S) carrier frequency of 65.75 MHz. The local oscillator (LO) is set to 107 MHz when channel 3 is selected. The 61.25-MHz picture carrier signal mixes nonlinearly with the 107-MHz oscillator to produce the difference frequency of 45.75 MHz (107 MHz − 61.25 MHz) and the sum frequency of 168.25 MHz (107 MHz + 61.25 MHz). The 107-MHz local oscillator also mixes nonlinearly with the 65.75-MHz sound carrier signal to produce the difference frequency of 41.25 MHz (107 MHz − 65.75 MHz) and the sum frequency of 172.75 MHz (107 MHz + 65.75 MHz) as seen in Figure 12.3b. The tuned circuit 4 in Figure 12.2 is always tuned to pass only the band of frequencies from 40 to 47 MHz; therefore, the sum frequencies that result from the mixing action are far outside the passband and will not appear at the tuner output.

The mixer is a frequency converter because it changes all incoming RF carrier signals down to the IF carrier frequency level. As such, it is sometimes called the *first detector*.

The tuned circuits, identified in Figure 12.2 as 1, 2, and 3, are all retuned as each channel is selected. The output tuned circuit 4 remains fixed at 40 to 47 MHz for all channels to pass only the difference frequencies on to the next set of circuits, the intermediate-frequency amplifiers.

Note that the video information is in the upper sideband of the modulated picture carrier signal all the way up to the mixer input and that the sound carrier signal is 4.5 MHz higher than the picture carrier signal. However, at the mixer output, due to the heterodyning action, the sound carrier signal is now 4.5 MHz below the modulated picture carrier signal, and the video information is seen as the lower sideband of the modulated picture carrier. This exchange of information position, seen in Figure 12.3b, has absolutely no effect on the information content of either signal.

The signal processing and frequency management of every tuner are identical in every respect, even when the dc operating voltages differ from one brand of tuner to another. This should clue you in on the not so widely advertised servicing trick of replacing a suspected defective tuner with a known good one from *any* other television receiver with compatible dc voltage requirements.

With no input signal (tuner set to an unused channel), the mixer becomes a noise generator. We will use this information in the troubleshooting sections to follow later.

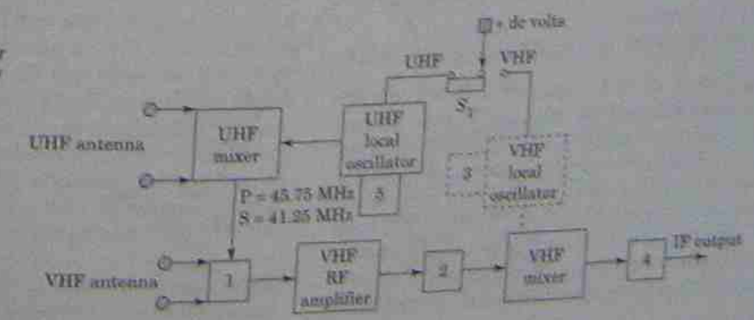
12.2.2 UHF Tuner

When the VHF tuner is set to channel 1, marked UHF on the channel selector, the connections on the inside of the tuner disable the VHF local oscillator, enable the UHF local oscillator, and place the VHF RF amplifier and mixer in series with the output of the UHF tuner.

In the UHF position, switch S_1 in Figure 12.4 removes the dc source voltage from the VHF local oscillator and attaches it to the local oscillator of the UHF tuner. The dc voltage to the VHF RF amplifier and mixer are not removed. At the same time that S_1 is activated, tuning circuits 1 and 2 are set to pass the frequency band of 40 to 47 MHz just like tuning circuit 4. Tuning circuit 1 is also disconnected from the VHF antenna and reconnected to the output of the UHF mixer circuit. The VHF RF amplifier and mixer now perform as two additional video IF amplifiers. Station tuning in the UHF band is now done by varying the frequency of tuning circuit 5 in the UHF local oscillator over the frequency range of 517 to 847 MHz for channels 14 through 69.

Because the UHF local oscillator must operate at frequencies that are more than eight times

FIGURE 12.4
A typical block diagram for the combined operation of the UHF tuner and the VHF tuner.



higher than the VHF local oscillator, the circuits are much more critical and greater care is advised when working in these circuits. Moving parts around in this circuit will change the stray capacity of the circuit and change the tuning.

The UHF mixer circuit uses a diode for nonlinearly combining the RF and oscillator signals, rather than a transistor as the VHF mixer uses. The diode accomplishes the mixing action as well as the transistor except that the diode does not have gain.

Many UHF tuners do not have an RF amplifier. If one were used, it would need to have a 330-MHz bandwidth for the UHF band and would result in very low gain, deriving no advantage. The two additional IF amplifiers of the VHF tuner will more than compensate for the absence of gain provided by the RF amplifier. The difference in the noise factor without an RF amplifier is claimed to be unnoticeable.

The UHF tuner is located in close proximity to the VHF tuner and is also a grounded metal enclosure placed away from the main chassis. Taking the UHF tuner out of one receiver and using it in another receiver works equally well provided that the dc operating voltage precautions are observed.

The antenna leads feed into the UHF tuner, and a short coaxial cable feeds the UHF tuner output signal into the VHF tuner. A second coaxial cable connects the output of the VHF tuner into the IF amplifier section.

12.3 VIDEO IF AMPLIFIER SECTION

Here is a truly unique amplifier circuit. It is usually made up of three amplifying stages that provide a voltage gain of 8000 to 10,000 over a limited frequency range, with the ability to change gain automatically depending on the signal strength at the antenna terminals. It is also the main factor for controlling the *selectivity* of the entire receiver. Selectivity describes the ability of the receiver to easily pass the signal at the desired frequency, while rejecting all adjacently close but unwanted signal frequencies or disturbances. Selectivity is recognized in Figure 12.5 by the steep skirts of the band-pass characteristic frequency response curve of the video IF amplifier section. Steeper skirts mean better selectivity.

Compare the video IF amplifier section of Figure 12.1 to the expanded version of Figure 12.6. You can see that Figure 12.1 is in the most basic form, whereas Figure 12.6 is a more detailed block diagram, but is still not down to the circuit schematic level. Figure 12.6 will be used to examine the operation of the video IF amplifier section in greater depth.

The output signal from the tuner is applied to the input filter section at the left side of Figure 12.6. The traps are commonly a high-Q narrow-bandwidth, series LC resonant circuit to ground that forms a notch filter to trap out (or remove) some specific frequency. Remember that a series tuned circuit has a low impedance at resonance (usually just the dc resistance of the coil) and is therefore a short circuit to ground for that specific frequency. Because the mixer reverses the relative position of the carrier signals, the first trap, marked **A**, is the adjacent channel sound trap at 47.25 MHz to ensure that the sound signal from the adjacent lower neighboring channel does not become part of the selected channel signal. Trap **B** is for the next higher adjacent channel picture carrier, which also needs to be removed and is tuned to 39.75 MHz.

The block marked Filter in Figure 12.6 is a band-pass filter. In earlier circuits, this was a series tuned LC circuit or a tuned coupling transformer. In later circuits, it is common to find crystal filters or SAW filters (surface acoustical wave filters). The SAW filter has the highest Q (to 35,000), followed by the crystal filter with a Q to 20,000 and the LC filters in last place with a Q of less than 500. Higher Q, again, means steeper response curve skirts and better selectivity. The input section of the video IF amplifier can be summarized as a passive network (no gain) that sets the general frequency response characteristics of the entire IF amplifier circuit.

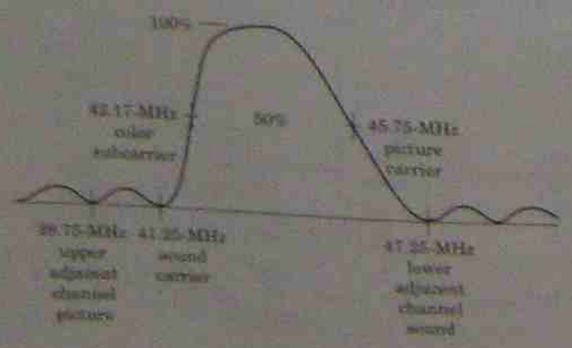


FIGURE 12.5
A typical video IF amplifier frequency response curve.

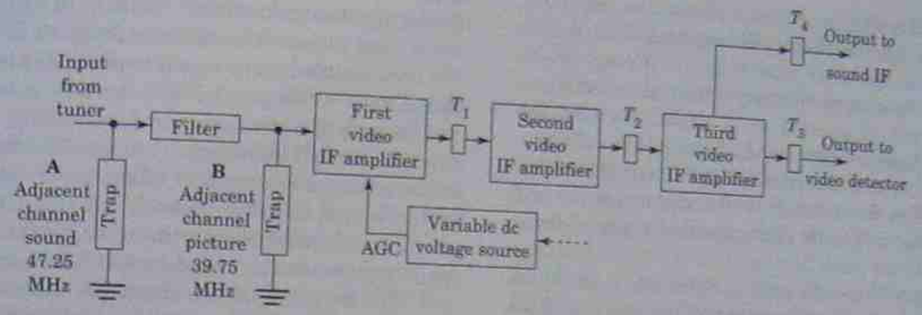


FIGURE 12.6
Expanded block diagram of a television receiver intermediate frequency (IF) amplifier series.

The three video IF amplifiers were originally vacuum tubes that progressed to discrete transistor amplifiers and have now advanced to differential amplifiers in microchip form. The vacuum tube and discrete transistor circuits were easier to locate and troubleshoot, whereas the chips require a bit more understanding of electronic circuitry, but, otherwise, present no additional problems.

The voltage gain for each video IF amplifier stage is about 20, so the overall section gain is typically $20 \times 20 \times 20 = 8000$.

The devices labeled T_1, T_2, and T_3 in Figure 11.6 indicate a tuning adjustment that couples one amplifier to another. They were originally tuned (and adjustable) transformers used to help shape the frequency response of the video IF amplifier section as seen in Figure 12.5. They are still found in some receivers but rarely need adjusting. The receivers that use crystal or SAW filters at the IF input no longer need major alignment. Therefore, in these later circuits, T_1, T_2, and T_3 become passive components that help to shape the video IF frequency response.

The device labeled T_4 marks the sound takeoff point for color television receivers where the sound signal is separated from the picture signal. The sound and picture signals are fed in parallel to their respective next circuits.

The sound carrier frequency at T_4 can be either of two frequencies.

1. It can be at 41.25 MHz as the sound carrier signal that passes through the video IF amplifiers. A tuned circuit of T_4 will pass only the sound carrier of 41.25 MHz to the sound IF amplifiers.
2. Because there are two carrier signals within the video IF amplifier signal makeup, the 41.25-MHz sound carrier signal will heterodyne with the 45.75-MHz picture carrier signal and produce new sum and difference frequencies. The sum frequency of 87 MHz is generally ignored and is filtered out. The difference frequency of 4.5 MHz is frequency selected by T_4 and is amplified by a 4.5-MHz sound IF section.

The functional performance in both cases is identical, except that each has its distinct sound carrier frequency. You will need to examine your schematic diagram to determine which sound IF frequency is preferred by the set manufacturer.

12.4 AUTOMATIC FINE TUNING

Automatic fine tuning (AFT) is a feedback frequency control loop that works much the same as a phase-locked loop (PLL). When a station is selected, the local oscillator in the tuner is set to heterodyne the station's RF signals down to the IF frequencies. Because of the IF amplifier frequency response, the best combination of picture and sound will be observed when the local oscillator is exactly 45.75 MHz higher than the received picture carrier fre-

quency. The FCC monitors each station regularly, so we can assume that their frequencies are within tolerances. However, the local oscillator, which changes frequency for each channel selected, is more likely to operate at a slightly errant frequency. Aging of parts and variations in temperature further cause a possible shift in oscillator frequency. The fine tuning control at the receiver will correct for frequency changes due to any of these causes.

The AFT circuit, seen in Figure 12.1, is like an FM detector, in that it converts frequency changes at the input to dc voltage changes at the output. When the input frequency is at a chosen frequency (41.25 or 45.75 MHz in the case of the AFT), the dc error output voltage is zero. If the local oscillator drifts higher in frequency, the carrier frequencies through the IF amplifiers will be higher and the feedback frequency to the AFT will be higher, causing the dc output voltage to change in a direction that will lower the local oscillator frequency.

If your mind runs ahead of your reading, you have already reasoned that, when the local oscillator comes back on frequency, the carrier frequencies in the IF section will be correct and the feedback frequency to the AFT will be such as to result in a zero dc correction voltage, allowing the local oscillator to go back, for whatever reasons, to its errant frequency, and you would be right. Fortunately, the dc correction voltage out of the AFT is held as a charge across a capacitor that is slow to change. This is an ambient system of checks and balances that results in a level of dc correction voltage to maintain the best compromise between what the frequency of the oscillator should be and the frequency it wants to be due to whatever causes. The search and setting routine should take only a few seconds of time.

If the receiver remains off frequency after several seconds of operation, the local oscillator frequency may need to be manually adjusted (see Chapter 13). During the service mode, it is permissible to disconnect the AFT line from the tuner and temporarily replace it with an external variable dc voltage source.

12.5 VIDEO DETECTORS

Although the video IF amplifier is a complete and distinct section in its own right, it is unfair to analyze it further without including the video detector and AGC sections. Figure 12.7 shows how the video detector is connected at the output of the video IF amplifier section. The detector is considered to be a frequency down converter. That is, it reduces the modulated picture signal down from 45.75 MHz to the unmodulated video signal covering the frequency range from 30 Hz to 4.2 MHz. Because it is the second frequency down converter found in the receiver, it is often called the *second detector*. The first detector was the mixer amplifier of the tuner circuit. The picture signal from the video IF amplifier is an amplitude-modulated carrier; therefore, the video detector is sometimes also called an *AM detector*.

The detecting action in an AM detector is performed by a diode that rectifies the ac signal and then passes the output through a low-pass filter. The filter removes the carrier frequency but passes the low-frequency (4.2 MHz) video signal on to the next section. If you understand the principles of a low-voltage power supply, then you can visualize the same type (rectifier and filter) of circuit working at a much higher frequency as the video detector circuit.

The output of the video detector has a dc component of voltage in the wave (as all rectified voltages have) and an ac component of voltage in the wave. The ac component in a low-voltage power supply is the ripple voltage and is maintained low. The ac component in the video detector circuit is the video signal and is held as large as possible. The polarity of the detector output may be either positive or negative, depending on how the diode is connected. An output from the diode cathode yields a plus dc level and positive-going sync pulses in the video signal. Reversing the diode so that the output is from the anode results in a negative dc voltage and negative-going sync pulses. The direction determination is made by the set designer and depends on how many amplifiers with phase inversion are encountered between the diode output and the input to the CRT.

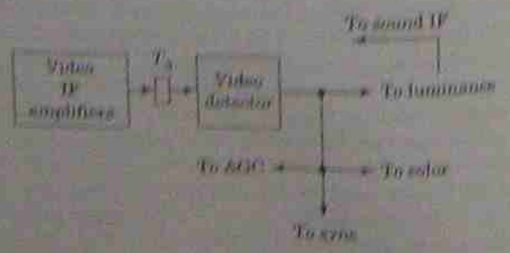


FIGURE 12.7
A block diagram showing all the sections that receive a signal from the video detector.

The output from the video detector is fed in parallel to a number of circuits that simultaneously process the separate parts of the recovered color-plex composite video signal.

Several bits of information given earlier in this chapter need to be examined here all at one time. Figure 12.1 shows the sound takeoff point from the third video IF amplifier as a solid line and a second sound takeoff point as a dashed line from the first video amplifier. This concept is followed by an explanation of the function and placement of T_4 at the third video IF amplifier. Now we see that Figure 12.7 has the sound takeoff from the luminance amplifier section. The idea was not intended to confuse the issue, but rather to convey the principle that the sound is separated from the picture signal in the third video IF amplifier in almost all color receivers and taken from the video amplifier in almost all monochrome receivers. If there is the slightest doubt about how your set is wired, start at the speaker on the schematic diagram and work your way backward through the sound system until you find the origin of the sound signal.

The video detector output may also go to the luminance (or video) amplifiers and sync circuits, to the color demodulator, and to the automatic gain control (AGC) circuits. Right now, the AGC system needs to be discussed.

12.6 AUTOMATIC GAIN CONTROL

The automatic gain control (AGC) system is the next step up from the familiar automatic volume control (AVC) circuits used in AM and FM radio receivers. In AVC, the audio signal is converted to a dc level and used to control the gain of the IF amplifiers. A strong signal at the antenna causes a large signal at the output of the detector, which in turn becomes a large dc feedback voltage to lower the gain of the IF amplifiers and hold the detector output to a medium level. A weak signal at the antenna causes a small signal at the detector output and a smaller dc voltage back to the IF amplifier that increases the gain for a medium signal out of the detector. The change in signal strength at the antenna has only minor variations during any given period of time. However, when changing from one station to another, the antenna signal strength may have wide variations. It is under the conditions of channel changing that the AGC is intended to maintain a constant signal level out of the detector, regardless of the signal strength at the antenna.

The AGC bias voltage is generally applied only to the first video IF amplifier, with the understanding that if you control the gain of the input amplifier you in effect control the gain of the entire amplifier section.

The AGC circuit in television differs in a dramatic way from the AVC circuits of radio. In radio, the audio recovered from the detector represents a peak-to-peak level of sound that you hear at the speaker. A simple rectifier and filter convert the ac audio to dc for AVC action. By examining Figure 12.8, you can see that the peak-to-peak video signal could be the same for a dark scene, at (a), or for a bright scene, at (b), that has a different dc output voltage relative to the average voltage in the wave per cycle. To prevent the scene brightness from controlling the AGC bias level, the AGC circuit is held in a cutoff condition for the scan time of the horizontal trace and then turned on by a feedback pulse from the horizontal flyback transformer during blanking time. The peak-to-peak amplitude of the horizontal blanking and sync pulses will be a true measure of signal strength that is independent of scene brightness. Because the AGC for television includes a pulsed condition, it is given the name *keyed AGC* or *gated AGC*.

The AGC control of the IF amplifiers is suitable under normal conditions. However, when an extremely strong signal arrives at the antenna, the RF amplifier in the tuner could be overdriven and distort the signal (compress the sync). A delayed AGC is used that is dormant under normal antenna signal levels and becomes active when the antenna signal exceeds a predetermined level. At this time, the delayed AGC bias voltage begins to lower the gain of the tuner RF amplifier. A possible circuit arrangement is given in Figure 12.9. Here the tuner AGC is zero for the time that the IF AGC remains below +1.4 V dc. When the IF AGC voltage exceeds +1.4 V dc, the diodes begin to conduct and apply an AGC voltage to the RF amplifier with a value of (IF)AGC − 1.4 V = delayed (RF) AGC. The word *delay* is used here to indicate a level delay, not a time delay.



FIGURE 12.8
The average voltage in the video wave for (a) a dark scene and (b) a bright scene.

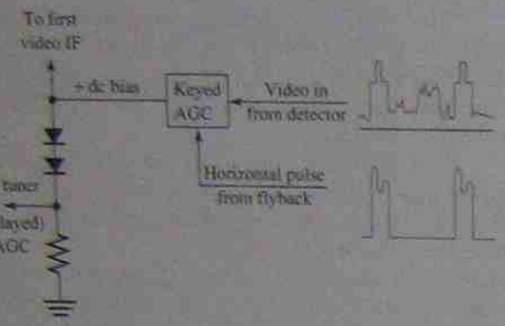


FIGURE 12.9
The block diagram for a keyed AGC system, including input and output signals plus the delayed AGC for the tuner.

The sum of Figures 12.6, 12.7, and 12.9 are all represented in the basic block diagram of Figure 12.1. Take the time now to go back to Figure 12.1 and see if you can identify each circuit and if you can signal trace through the tuner, the video IF amplifiers, the video detector, and AGC circuits for a clear understanding of the purpose and function of each section.

12.7 LUMINANCE OR VIDEO AMPLIFIERS

The output signal from the video detector, typically 2 to 6 $V_{p\text{-}p}$, is used for the five functions identified in Figures 12.1 and 12.7. The previous section explained the AGC action, and we can postpone the sound section momentarily. Then, if we declare that this should be the block diagram of a monochrome receiver (refer to Figure 12.11), we can hold off a discussion on color demodulation for the next section. This leaves only the two signal paths for the video signal to the video amplifiers and to the sync separator.

In monochrome receivers, the picture signal is called *video* and the circuits are called *video amplifiers*. The term *luminance* is reserved for the video Y signal of the color receiver. The purpose of the video amplifier is to increase the signal size to a level needed to drive the CRT. This is typically 50 to 100 $V_{p\text{-}p}$. In the review block diagram of the video amplifiers in Figure 12.10, it is common to find two subsections. The input section is a low-level signal section where provisions are made to tap off a signal for the sync separator and another for the sound takeoff, when applicable. The output of the low-level section ends at the contrast control. The second subsection is the high-level video output amplifiers that run from the contrast control to the input of the

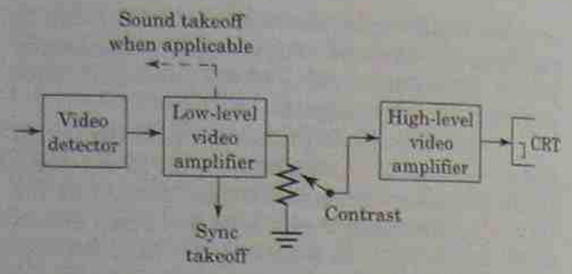


FIGURE 12.10
Monochrome video amplifier block diagram.

CRT. Here you will encounter high peak-to-peak signal levels and high dc operating voltages.

All the circuits from the antenna input terminals through the video detector generally require the use of an RF signal generator to test for valid circuit operation. After the video detector, the signal frequencies are low enough to be observed on an oscilloscope. Therefore, in television servicing the output of the video detector is considered to be the midpoint of the receiver. When troubleshooting inside the receiver, the first test point is at the video detector output. This technique of dividing the system in half is a common practice of experienced troubleshooters. If you can measure a signal at the detector output, the RF section of the receiver is working and any problems must be in the second half (video section). If you cannot measure a signal at the detector output, the problem must be in the RF half of the receiver. The same technique can be applied to the video amplifier section, using the contrast control as the mid-test point.

Briefly review the block diagram of Figure 9.1 and the schematic diagram of Figure 9.2 to recognize that the monochrome video monitor is identical to the video circuits of a television receiver. This includes the video amplifiers and sync separator, plus both the vertical and horizontal deflection sections and high voltage. The output signal from the video detector could be plugged into the video monitor for a full picture reproduction. With this point in mind, no further discussion of video circuit troubleshooting is required at this time, and the reader is referred to Chapter 9 for detailed circuit descriptions.

12.8 COLOR DEMODULATION

Using the same block diagram of Figure 12.1 but declaring it to be for a color receiver, we can pick up at the video detector output and look at the color

demodulation systems. The process used to construct the chroma signal in Chapter 8 will be run in reverse as the accepted way to recover the color signals at the receiver.

You will recall that the modulation process took the R, G, and B signals from the color camera and matrixed them to develop the I and Q signals or the R − Y and B − Y color difference signals. The I and Q signals are separately modulated onto a suppressed carrier. The carrier frequency is the same for both modulators (3.58 MHz), but the carrier is first phase delayed by 57° for use in the I modulator and then delayed by another 90° for use at the Q modulator to generate quadrature modulation. The modulated I and modulated Q signals are added to form the chroma signal, and then the chroma signal is added to the luminance video signal, which already contains the horizontal and vertical, blanking, and sync signals. This combination is the colorplex composite video signal that will be recovered at the output of the video detector of the receiver.

In the demodulation process, the chroma signal is first separated from the colorplex composite video signal by a band-pass filter. The modulated chroma signal lies in the frequency range of 2.1 to 4.2 MHz that is passed by the band-pass filter. Yes, there is still monochrome video information in this band that will be applied to the color demodulators along with the chroma signal. But, because the monochrome video is not in a modulated form, it will not pass through the color demodulator circuits. In Figure 12.11 you can see that the chroma signal out of the band-pass filter is applied to the chroma amplifier and to a burst gate amplifier. At the same time, a horizontal pulse from the flyback transformer is fed into a phase splitter that develops a positive and negative output pulse. The positive pulse turns the gated burst amplifier on during the horizontal blanking interval to pass only the color sync signal. The negative pulse turns the chroma amplifier off at the same time to pass only the color picture information to the color demodulators without the color sync signal, which could cause interference. Then the output of the chroma amplifier is applied to both demodulators in parallel.

The color balanced demodulators require that a carrier signal be reinserted in order for a color difference signal to appear at the output. The name of the demodulator and the output color difference

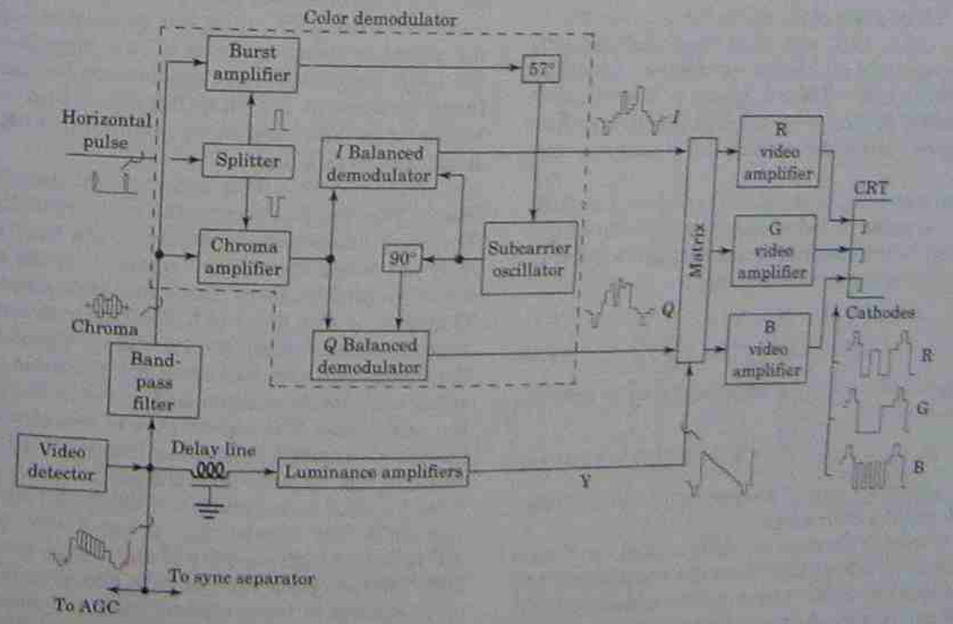


FIGURE 12.11
The block diagram of a typical color demodulator system along with the luminance amplifiers, matrix arrangement, and color video output amplifiers to the CRT.

signal that it produces depends on the phase of the reinserted subcarrier signal compared to the phase of the reference color burst signal. The frequency of the subcarrier signal is always 3.579545 MHz that is synchronized by the color burst signal. When the reinserted carrier is phase delayed by 57° from the reference burst, the *I* signal will be produced at the demodulator output. A phase delay of 90° reproduces the R − Y color difference signal. A phase delay of 147° (57 + 90) reconstructs the *Q* signal as the quadrature other half of the *I* signal, and a subcarrier phase delay of 180° (90 + 90) puts out the B − Y color difference signal as the quadrature second half of the R − Y signal. The *I* and *Q* signals are always used in pairs (as in this text), whereas the R − Y and B − Y difference signals may be used as another set of recovered signals. Then proper mixing (matrixing) of the *I* and *Q* along with the Y signal reproduces the original red, green, and blue color signals. The proportions for mixing are

$$\text{red} = 100\%\ Y + 94.5\%\ I + 62.1\%\ Q \quad (12.1)$$

$$\text{green} = 100\%\ Y - 27.1\%\ I - 64.7\%\ Q \quad (12.2)$$

$$\text{blue} = 100\%\ Y - 111\%\ I + 172\%\ Q \quad (12.3)$$

If you substitute equation 8.1 in place of the value for Y, equation 8.5 in place of the value for *I*, and equation 8.6 in place of the value for *Q* in the three equations (12.1, 12.2, and 12.3), then multiply out each term and add all like terms together, equation 12.1 would be red = 100% R, green = 100% G, and blue = 100% B. The process is simple straightforward algebra and is not carried out in detail at this time.

The matrixing of the R − Y and B − Y signals is much simpler. It takes only the addition of the +Y signal to each color difference signal in order to retrieve the original three colors:

$$\text{red} = (R - Y) + Y \quad (12.4)$$

$$\text{blue} = (B - Y) + Y \quad (12.5)$$

The green color takes an additional step to first acquire G − Y:

$$G - Y = -51\%\ (R - Y) - 19\%\ (B - Y) \quad (12.6)$$

Then add a +Y signal to the results of equation 12.6 to get the color green.

A third color recovery system used an *X* color subcarrier phase at 282° from the burst phase and a *Z* subcarrier at 333° for a system called the *X*, *Y*, *Z* system. It worked exactly like the R − Y and B − Y system, but lost industry favor because the available test equipment was not geared to unique demodulation systems. The point is that it is possible to use any two subcarrier phase angles for demodulation that you may choose. You will need to develop a new set of matrixing proportions and modify the test equipment to comply with your demodulation choices.

The *hue* or *tint* control is an adjustment of the 57° delay network in Figure 12.11. The 90° delay that follows the subcarrier oscillator remains fixed for all occasions and tracks the initial 57° delay setting. The color gain control is part of the chroma amplifiers. These controls are external to the chip and are currently operated from a digitally controlled section.

One section not shown in Figure 12.11 is the color killer. If the color channel were left open all the time, the noise of the chroma amplifier during a monochrome telecast would appear on the CRT screen as random colored dots called *confetti*. The color killer senses the absence of the color burst during a monochrome telecast and biases off the chroma amplifier for that period. Some receivers have an adjustable control to set the threshold level to activate the color killer.

Almost all color demodulators are contained within a single microchip; therefore, Figure 12.11 shows the standard signal waveforms of a demodulator when an NTSC color bar generator supplies the signal for testing. Since all the signals are at the lower frequencies, the oscilloscope becomes the ideal instrument for checking input and output waveshapes. You need to be familiar with the signals for successful testing.

The band-pass filter and the luminance amplifiers in Figure 12.11 receive the same input signals. The color demodulators require more time physically to process the chroma signal than the simple act of amplification by the luminance amplifiers. Therefore, a time delay of 0.8 to 1 microsecond (μs) is needed to slow down the luminance signal so that the luminance and recovered color signals can be added back together again and arrive at the CRT at the same time. The signal time is retarded in the luminance channel by a delay line made up of 250 turns of No. 26 wire on a 0.5-inch (in.) by 4.5-in. tube, yielding an inductance of about 182 microhenries (μH). The tube surface is laced with a metal foil to form a high capacity of about 5500 picofarads (pF) between each turn of wire and ground. From your studies of transmission lines, you may recall that the delay time is the square root of the inductance times the capacitance, which in this case is about 1 μs. Later model receivers use a lumped constant delay line that is smaller in size, but does the same work. The three terminals of the delay line are the input, output, and ground. Check with your scope for the video signal in and out of the line. The feed-through loss is negligible, so any loss of signal means that the line is shorted or opened, which can be verified with an ohmmeter.

12.9 dc RESTORATION

Every signal voltage that we could examine has an ac component and a dc component. A pure sine wave may have a dc component equal to zero; therefore, the ac wave will expand equally in the positive and negative directions from zero. These conditions are illustrated in Figure 12.12a, where the ac signal first goes to +4 V_{pk} and then to −4 V_{pk} (8 $V_{p\text{-}p}$) around the reference of 0 V dc. In Figure 12.12b, the same ac signal is joined with a +6-V dc component, where the only change is in the ac reference, now at +6 V dc. The ac component still measures 8 $V_{p\text{-}p}$ (using an oscilloscope), and the reference level (measured with a dc voltmeter) has a level of +6 V. When the signal of Figure 12.12b passes through a capacitor, it is referenced to whatever dc voltage is present at the output side of the capacitor.

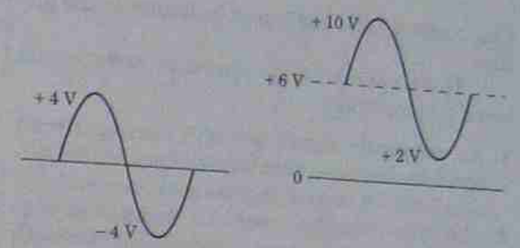


FIGURE 12.12
The ac and dc components of the wave.

At the input to the cathode ray tube, in the presence of a video signal, a dc reference must be established that will identify black at the CRT cutoff level. Without a way of tying the ac wave component to the dc reference, the conditions seen in Figure 12.13a result. That is, when the brightness control is set to establish the black level for the video signal in Figure 12.13(a1), the increase in signal strength shown in Figure 12.13(a2) and 13(a3) causes the gray portions of the signal to sink into the black region and the white portions to be less than the actual scene brightness being televised. Loss of the dc reference level causes a very

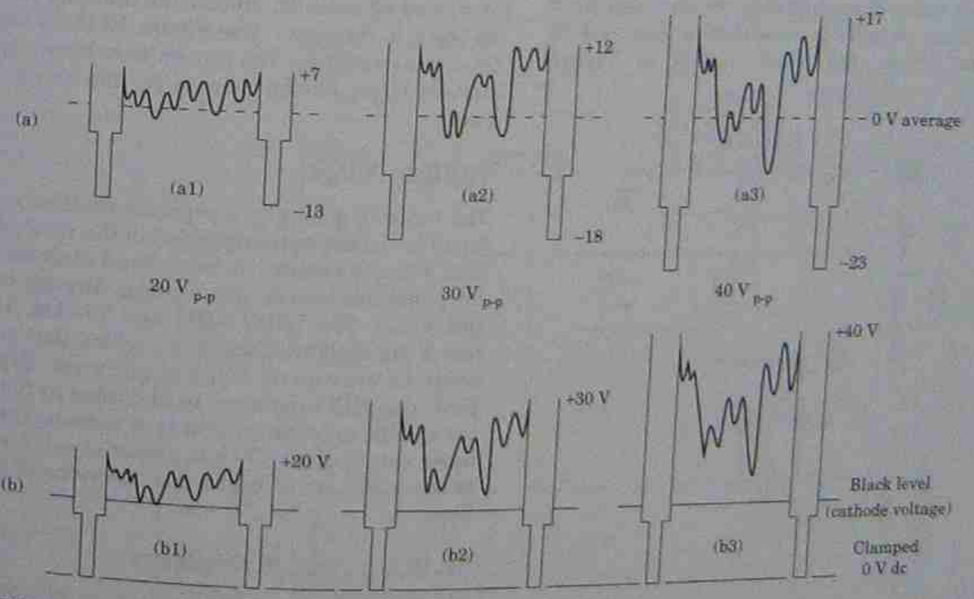


FIGURE 12.13
Three levels of video signal as they would appear at the input to the CRT for (a) varying around the average voltage level and (b) sync tips clamped to 0 V dc.

poor contrast ratio and loss of brilliance in the picture.

Three approaches to corrective action could mend this condition:

1. An automatic signal strength sensing circuit could be developed that would adjust the brightness level for varying degrees of video signal.
2. The sync pulse tips could be clamped to a dc level so that any change in video signal strength would cause changes in amplitude only in one direction (toward white).
3. Direct couple all the video amplifiers (no coupling capacitors) from the video detector to the CRT.

Method 1 is far too complex and would add unwarranted expenses to the manufacturing process. Method 2 requires only the addition of a diode, as seen in Figure 12.14, to form a clamping circuit for the negative-going sync tips when the video signal is applied to the control grid of the CRT. In the case when the video signal is applied to the CRT cathode, the diode in Figure 12.14 is reversed for the positive-going sync pulses to be clamped to a dc reference level. This diode clamping circuit is called dc restoration or dc reinsertion. The diode clamper is most commonly found in vacuum tube circuits or in transistor video amplifiers that require very high dc operating voltages in monochrome receivers or monitors. When the video signal in Figure 12.13(a1) appears at the collector in Figure 12.14, the negative 13-V_{pp} sync pulse causes diode D_1 to conduct and charge capacitor C_1 to +13 V dc. This raises the signal by +13 V and clamps the sync pulse tips to 0 V dc. The waves in Figure 12.13(a2) and 12.13(a3) are raised, respectively, by +16 V and +23 V to clamp these waves to 0 V dc, as shown in Figure 12.13b.

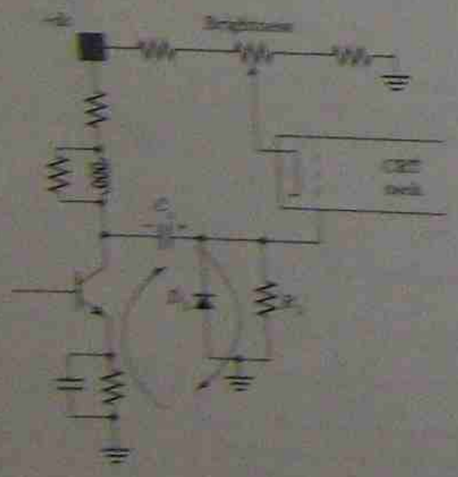


FIGURE 12.14
A video amplifier output circuit with diode clamping (dc restoration).

Method 3 is most commonly used in transistor video amplifiers that operate on lower signal levels and dc operating voltages in the direct-coupled mode. The advantage of direct coupling is that parts are removed (coupling capacitors) to achieve the added feature of dc reinsertion. Direct coupling is found in most color receivers and monitors because now there is a separate video amplifier for each color, requiring three dc restoration circuits. In the color amplifiers, the dc level is established in the early stages of the luminance circuits and carried through the three color video amplifiers to the CRT.

12.10 CHASSIS LAYOUT

As you gain even a small amount of experience, you will learn to locate many of the television circuits on the chassis without a layout guide. They will be identified by common landmarks that you can easily learn to recognize. Use Figure 12.15 for the following instructions. The system here uses a logical pattern based on the reasons for the circuit locations.

12.10.1 Tuner

The tuner is generally a separate shielded section found in the upper front section in the receiver cabinet. When a channel indicator and channel selector panel are in use, the tuner is directly behind this panel. The UHF, VHF, and 75-ohm (Ω) antenna input connections have cables that run directly to the tuners; follow these wires. Separate UHF and VHF tuners can be identified by following the specific antenna wire to each section. The VHF tuner output generally has a coaxial cable leading to the main circuit board and the video IF amplifiers.

12.10.2 Video IF Amplifiers

The video IF amplifier section is always in a shielded compartment on the main chassis board. It is located close to where the tuner output cable joins the main board. Stampings on the shielded

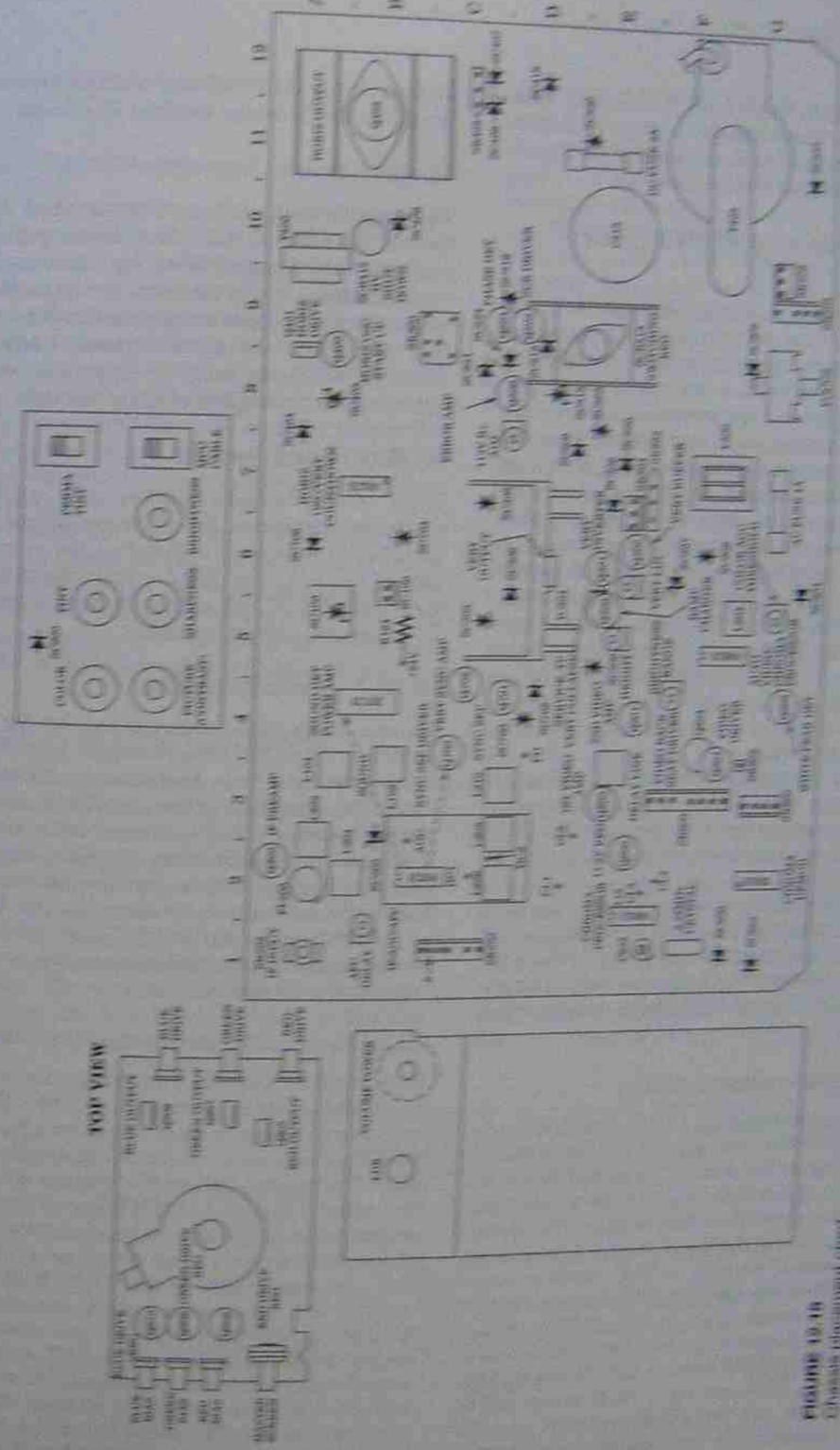


FIGURE 12.15
Chassis (terminal) layout.

cover, such as AGC, TRAP, or IF, may help to identify this section. The video IF in Figure 12.15 is Q_{200} and *IC* 204 located at 2A and 2C in Figure 12.15. The video detector is inside *IC* 204.

12.10.3 High-voltage and Horizontal Sections

Although these sections do not follow the block diagram format, they are the next in line for easy identification. The high-voltage transformer is well insulated, but still radiates a horizontal pulse into the air. To verify this phenomenon, hold an ungrounded scope probe close to (but not touching) the high-voltage transformer and observe the waveform on the scope. This radiated energy could interfere with the performance of the tuner and is therefore placed as far away from the tuner as space will permit. When the tuner is placed at the top left front of the cabinet, the high voltage is placed at the bottom right rear of the chassis. The high-voltage transformer in Figure 12.15 is T_{402}. Small diodes found near the high-voltage transformer, such as SC_{407}, SC_{415}, SC_{518}, SC_{519}, SC_{524}, SC_{527}, and SC_{530}, are often the rectifiers for the dc voltages derived from the high-voltage section.

The focus control and focus rectifier SC_{908} are also located close to the high-voltage transformer.

The heavy-gauge red wire connects the high-voltage transformer to the anode button on the bell area of the CRT.

The horizontal driver transistor Q_{401}, horizontal driver transformer T_{400}, and horizontal output amplifier Q_{402} are always located close to the high-voltage transformer. The horizontal output amplifier is generally a large TO-3 device mounted on a heat sink.

12.10.4 Low-voltage Section

Not so obvious in Figure 12.15, but unavoidably obvious when viewing the receiver chassis, is the ac line cord plug at the rear of the circuit board. In Figure 12.15, the ac line cord attaches to the chassis at the 4-ampere (A) ac fuse location (7G) shown at the center rear of the board. In the same general area, you should be able to find the four large diodes that form the low-voltage bridge rectifier circuit. In this example, they are SC_{500}, SC_{503}, SC_{506}, and SC_{509}. Look next for a very large multisection filter capacitor placed close to the diodes, in this case, C_{518}. C_{518} measures 1.5 in. in diameter and is 4 in. tall. If you can find the ac line cord, you can generally pinpoint the low-voltage power supply section. Some receivers use a standard encapsulated, four-diode, bridge rectifier IC device.

12.10.5 Sound Section

The speaker and volume controls often face the front of the cabinet, with the speaker grille placed just below the channel selecting functions. Therefore, it makes sense to place the sound section close to the volume control and speaker. In Figure 12.15, L_{108} (at 3B) is the sound takeoff transformer, *IC* 102 (at 4B) is the sound IF amplifiers, sound detector, and audio amplifiers all in one unit.

12.10.6 Color Section

Every color television receiver uses a 3.58-MHz crystal to reconstruct the subcarrier signal. In Figure 12.15, this crystal is found at the extreme left side of the board at 1F. Finding this component then identifies *IC* 600 as the chroma processor and *IC* 602 as the color demodulator.

12.10.7 Vertical Section

Because of the high current drawn by the vertical deflection yoke, the vertical output amplifier must be mounted on a large heat sink (for transistor circuits). This heat sink is found at the exact center of the PC board at 6D. The vertical deflection section is almost always found here. In older sets, a large iron core vertical output transformer would have been found in this area for identification. The plug-in deflection yoke socket (SK_{300} at 9C in Figure 12.15) is generally located between the vertical and horizontal deflection circuits.

12.10.8 Video (Luminance) Amplifiers

The output of the video or luminance amplifiers must feed a signal to the base of the CRT. There will always be one or more wires running from the CRT base to a point on the PC board for this purpose. The space between the chroma circuits and the center of the PC board is reserved for the video or luminance amplifiers. In monochrome receivers, all the video amplifiers are on the main board, with only one signal wire to the CRT. With color receivers, the color video output amplifiers (Q_{905} through Q_{910} in Figure 12.15) are mounted on a special PC board as part of the CRT socket. These amplifiers are often accompanied by three CRT bias controls and three color drive controls. The bundle of wires from the CRT socket board also runs to the area of the luminance amplifiers' socket (at 3G).

This section is further identified by the addition of a delay line.

12.10.9 Sync Section

The only space remaining on the main PC board is the rear center section. This is often the format used in product layout. That is, place the critical circuits first for minimum interference and then locate the less critical circuits in the remaining open spaces. Remember that the sync input signal must come from the low-level video amplifiers and seek the vertical and horizontal deflection oscillators as a target destination. The sync circuits, located behind the luminance amplifiers and feeding toward the deflection circuits, take up the only remaining space on the main PC board, at 4C.

IC 700 at the rear center of the PC board serves as the horizontal deflection oscillator and a locked-in vertical deflection oscillator in the vertical countdown mode. Its input signal is the sync and its output signals are the horizontal signal and vertical signal to their respective deflection circuits.

12.11 SPLIT SOUND RECEIVERS

The block diagram format of the television receivers that first entered the market were called split-sound receivers. The signal path block diagram is given in Figure 12.16 to show that the sound and picture carriers are separated at the output of the mixer in the tuner. The sound circuits were complete with a 41.25-MHz sound IF section, an FM sound detector, and an audio amplifier to the speaker. The picture carrier section was independent from the sound with its own 45.75-MHz video IF amplifier section, AM video detector, and video amplifiers to the CRT. The AGC circuits controlled the gain of the picture IF amplifiers only. The sync circuits, vertical and horizontal deflection, high- and low-voltage sections were as we know them to be currently.

The advantages were that each section (picture and sound) could be optimized for frequency response, gain, and tuning independent of each other. The system performed exceptionally well. The disadvantage was that each IF section required three stages of amplification for a total of six IF amplifiers.

It was decided several decades ago to save the cost of three amplifier sections by changing over to the intercarrier format that is seen in Figure 12.1 and is still in current use. The intercarrier receiver defines a system in which the modulated sound carrier and the modulated picture carrier are amplified by the same IF amplifiers. The advantage of the intercarrier system is lower cost. The disadvantage is that now the gain, tuning, and frequency response of the IF amplifier section are a compromise between the best combination of sound and picture.

A second complication was evident when printing appeared on the screen along with the video. The maximum transitions in the signal (max white and max black) that accompanied the lettering raised the level of modulation to a point where the vertical sync pulses could be heard in the sound channel. This condition was labeled *sync buzz* or *intercarrier buzz*. The sync buzz could be minimized by turning to the strongest channel, wait for lettering to appear, and then turning down the IF amplifier gain (by adjusting the AGC) until the buzz disappeared. It was advisable to check the reception on all other local channels to ensure that the AGC was not turned down too low. This is now part of

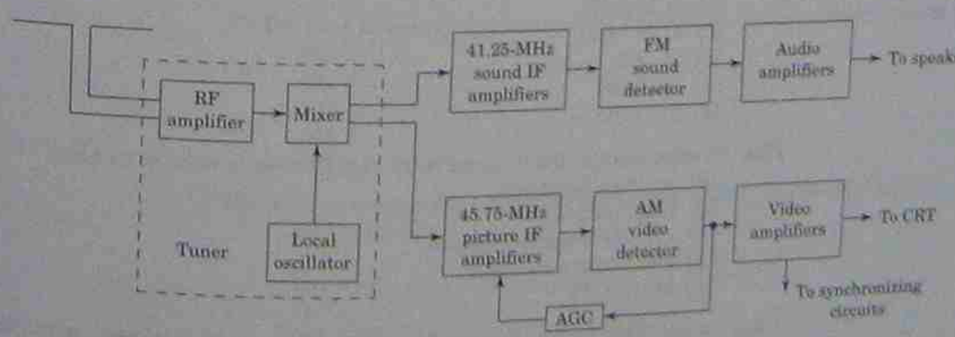


FIGURE 12.16
Partial block diagram for a split-sound television receiver (signal paths only).

the manufacturer's setup procedure before shipping. The set manufacturers and broadcasters have made great strides to neutralize this condition.

You may never see an old split-sound receiver, but look at the current television receiver schematics. There is a separate IC chip for the picture IF amplifiers and a second IC chip for the sound IF amplifiers. Don't be too surprised then if someone develops a "new" system called split sound to get rid of some of the detractions associated with the intercarrier system. Maybe in high-definition TV.

12.12 SUMMARY

You cannot begin to isolate a defective circuit in a television receiver or monitor or locate the circuit within the product until you have a good understanding of the receiver block diagram. This tool is the starting point for every examination you will make.

Although no two receiver block diagrams will be identical, they will all be close enough to the general block diagram in Figure 12.1 for you to recognize the slight variations. Study the general block diagram to the point that you can draw a similar diagram from memory and state the function and purpose of each section. Include Figure 12.11 for color along with Figure 12.1.

No two receivers will have identical circuit layout plans. But, again, if you understand which major landmarks to look for and the circuits that they are associated with, you can save considerable time in your work schedule.

QUESTIONS

12.1. How well should you know the general block diagram of a color television receiver?
- **(a)** not required,
- **(b)** recognize a block diagram drawing,
- **(c)** know the general format,
- **(d)** be able to follow through the block diagram,
- **(e)** be able to draw a block diagram from memory

12.2. What single feature describes the action of a superheterodyne receiver? They all
- **(a)** are solid state,
- **(b)** display picture and sound,
- **(c)** down convert the antenna signal to a fixed lower frequency,
- **(d)** use the interlace system of scanning,
- **(e)** have interchangeable parts.

12.3. The picture carrier frequency at the intermediate level is
- **(a)** 41.25 MHz,
- **(b)** 45.75 MHz,
- **(c)** 54 MHz,
- **(d)** 101 MHz,
- **(e)** 216 MHz.

12.4. At what point in the receiver is the signal-to-noise ratio at its best?
- **(a)** antenna terminals,
- **(b)** tuner output,
- **(c)** video IF amplifier output,
- **(d)** video detector output,
- **(e)** at the CRT

12.5. In the VHF tuner, the local oscillator frequency is always operating (a) higher or (b) lower than the selected picture carrier signal.

12.6. What frequency will the local oscillator operate at when the picture carrier of 55.25 MHz for channel 2 is selected?
- **(a)** 41.25 MHz,
- **(b)** 45.75 MHz,
- **(c)** 54 MHz,
- **(d)** 101 MHz,
- **(e)** 216 MHz

12.7. When operating the UHF tuner, the VHF tuner is
- **(a)** disabled,
- **(b)** connected as a second heterodyne section,
- **(c)** connected as additional IF amplifiers,
- **(d)** amplifies the sound carrier only,
- **(e)** amplifies the picture carrier only.

12.8. What section of the television receiver block diagram has the greatest control of the receiver's selectivity?
- **(a)** tuner RF amplifier,
- **(b)** tuner mixer,
- **(c)** tuner oscillator,
- **(d)** video IF amplifiers,
- **(e)** AGC system

12.9. In a color receiver, at what point is the sound signal separated from the picture signal?
- **(a)** at the tuner output,
- **(b)** at the third video IF amplifier,
- **(c)** at the video detector output,
- **(d)** in the video amplifier section,
- **(e)** in the AFT section

12.10. The tuner is held on frequency by the
- **(a)** AFC circuit,
- **(b)** AGC circuit,
- **(c)** AFT circuit.

12.11. Delayed AGC refers to
- **(a)** phase delay,
- **(b)** video time delay,
- **(c)** voltage-level delay.

12.12. How many color demodulators are used in the color demodulation process?
- **(a)** 1,
- **(b)** 2,
- **(c)** 3,
- **(d)** 4,
- **(e)** 5

12.13. How many color subcarrier oscillators are used in the color recovery process at the receiver?
- **(a)** 1,
- **(b)** 2,
- **(c)** 3,
- **(d)** 4,
- **(e)** 5

12.14. The circuits that come after the video detector in a color television receiver are the same as are found in a computer color monitor.
(a) true
(b) false

12.15. In which circuit will the delay line be found?
(a) chroma,
(b) *I* demodulator,
(c) *Q* demodulator,
(d) luminance amplifier,
(e) color subcarrier oscillator

12.16. All color television receiver block diagrams are similar.
(a) true
(b) false

12.17. You can find the location for many of the receiver's circuits by recognizable landmarks.
(a) true
(b) false

12.18. When you find the location of a defective circuit, you will not need a schematic.
(a) true
(b) false

12.19. Name the input and output terminals of the VHF tuner.

12.20. To what section does the output of the UHF tuner connect?

12.21. Name the three signal circuits of the VHF tuner.

12.22. Name the three functions of the VHF tuner.

12.23. Which tuner circuit acts as a buffer to prevent RF radiation to other nearby receivers?

12.24. The VHF RF amplifier is a high-frequency, low-gain, low-noise, tuned, wideband amplifier.
(a) true
(b) false

12.25. The VHF mixer is a (a) linear or (b) nonlinear amplifier.

12.26. When switched to the UHF position, name the VHF tuner circuits that remain active and those that are disabled.

12.27. Diodes are (a) linear or (b) nonlinear devices.

12.28. Define the action described by the term *selectivity*.

12.29. What section of the television receiver has the greatest effect on the receiver's selectivity?

12.30. The adjacent channel sound carrier trap is set to what frequency in the video IF amplifier section?

12.31. The adjacent channel picture carrier trap is set to what frequency in the video IF amplifier section?

12.32. What does the acronym SAW stand for?

12.33. A SAW filter is a (a) low *Q* or (b) high *Q* filter device.

12.34. List three names that apply to the picture signal detector.

12.35. In the block diagram, identify the name of the section that precedes the video detector and the name of the section that follows the video detector.

12.36. From what section in the block diagram does the automatic gain control get its input signal?

12.37. Where is the output voltage of the AGC section applied in the block diagram?

12.38. What single feature makes the television AGC circuit different from the AVC circuits found in radio?

12.39. Given the following list of peak-to-peak voltages, which would be most appropriate at the output of the video detector?
(a) 0.25 V,
(b) 1.5 V,
(c) 8 V,
(d) 17.5 V,
(e) 21 V

12.40. State a typical range of peak-to-peak video signal voltage at the input to the CRT.

12.41. Where is the testing midpoint that will divide the television receiver into two parts?

12.42. With zero video signal at the CRT, there will be no raster.
(a) true
(b) false

12.43. The video signal is fed to the sync separator (a) before or (b) after the contrast control.

12.44. The sync separator separates the vertical sync pulses from the horizontal sync pulses.
(a) true
(b) false

12.45. After the video detector in the block diagram, the greatest amount of information from a single measurement is obtained when using the
(a) spectrum analyzer,
(b) oscilloscope,
(c) signal generator,
(d) dc voltmeter,
(e) distortion meter.

12.46. Compare the color signal dissecting sequence at the receiver to the construction process of the color signal at the transmitter.

12.47. How many color demodulators are used in the color recovery process at the receiver?

12.48. How many color subcarrier oscillators are used in the color recovery process at the receiver?

12.49. Compared to the phase of the color burst signal, state the phase delay of the *I* demodulator subcarrier signal and of the *Q* demodulator subcarrier signal.

12.50. Compared to the phase of the color burst signal, state the phase delay of the R − Y demodulator subcarrier signal and of the B − Y demodulator subcarrier signal.

12.51. In which subcircuit will you find the tint control?

12.52. In which subcircuit will you find the color control?

12.53. What is the function of the delay line?

12.54. How much time delay is accounted for by the delay line?

12.55. In which circuit will the delay line be found?
(a) chroma,
(b) *I* demodulator,
(c) *Q* demodulator,
(d) luminance amplifier,
(e) subcarrier oscillator circuit

13 Tuners and Remote Controls

13.1 INTRODUCTION

This chapter should start with the same three words as the first paragraph of the Old Testament, but end differently: "In the beginning, stay out of the tuner." With no intent to be disrespectful or flippant, this warning is extended to advise you to master your technical skills at the lower frequencies before attempting to work on tuners. This does not mean that you should be ignorant of the tuner's operation or of its circuits; simply, proceed slowly.

13.2 TUNER TYPES

There are only two types of tuners, the mechanical and the electronic. Both are used at the lower VHF frequencies and the higher UHF frequencies. The mechanical types have served the industry for well over 40 years but are becoming obsolete. They are covered here briefly because they may still be found in some products. The electronic types use dc-controlled varactor diodes for changing frequency and are fast becoming the standard for the industry. Vacuum-tube types are omitted from this text.

A reminder about substitute tuners, called *tuner subbers*, at this time should prompt you to use this tool as a proof tester before getting too involved in tuner parts changing or circuit adjusting.

Mechanical tuner types are broken down as follows:

1. Wafer switch VHF tuners
2. Turret VHF tuners
3. Continuous tuning UHF tuners

A fourth type is the electronic tuners that use varactor diodes for both VHF and UHF operation.

13.3 MECHANICAL TUNERS

We know that all tuners are electronic circuits. The name *mechanical* refers to the methods used to change the electronic circuits for channel selection.

13.3.1 Wafer Switch Tuners

Figure 13.1 is a photograph of a wafer switch tuner with the shielding cover removed. It contains four wafer switch sections ganged together on a single

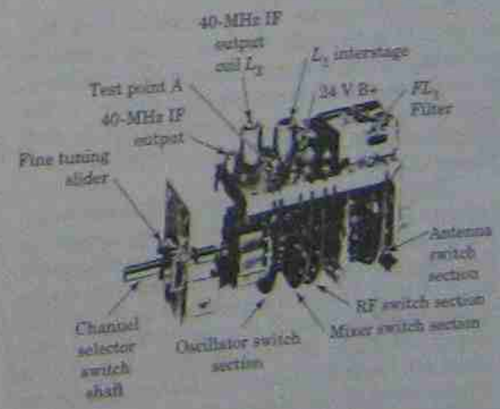


FIGURE 13.1
Partially exploded view of a wafer-type tuner with the shielding cover removed.

shaft. When the shaft is turned for channel selection, all four switch sections change contacts at the same time.

In earlier discussions, we learned that the RF amplifier feeds the amplified antenna signal to the mixer, and the local oscillator also feeds its output signal to the mixer. Therefore, by common sense, the mixer section is at the center of the in-line tuner. The local oscillator has an adjustment for each channel that is accessible from the front of the receiver by removing the channel selector knob. This requires that the local oscillator be placed in the forward position in the tuner lineup. The antenna lead-in wire enters the tuner at the back end, so the antenna wafer switch section is at the back of the tuner. The RF amplifier and its wafer switch are between the antenna section and the mixer section. Then the order of the in-line wafer tuner from front to back is the local oscillator wafer section, the mixer amplifier wafer section with the output to the IF amplifiers, then the RF amplifier wafer section and the antenna wafer section.

As can be seen in Figure 13.2, individual coils are connected between each the wafer switch contacts to form a series inductance with taps for each channel. Channel 13, at the highest frequency, has the smallest inductance. As each progressively lower channel is selected, more inductance is added per step on each of the four wafers. Channel 2, at the lowest frequency, uses the total inductance (switch contacts 1 through 12) for tuning to its required frequencies. Finally, at the channel 1 position, the VHF tuner switches over to the UHF mode, as described earlier.

If we examine the RF wafer switch from Figure 13.2, as an example, you can see the principles of channel tuning that will apply in like manner to all switch sections, except the local oscillator. The local oscillator has a separate isolated coil for each channel at switch S1F (switch 1, front), although Figure 13.2 shows only one coil.

Figure 13.3 is the RF wafer and mixer wafer, redrawn from Figure 13.2. The biasing circuits for the RF amplifier and mixer have been omitted from this diagram, since we need to discuss only the associated coils. The coils are made to have a slightly higher inductance value than is needed for correct tuning. Adjusting the coils by spreading the turns apart will lower the inductance to the needed value. Always start at the highest channel number. Figure 13.3 is drawn with channel 13 selected. In both switches, the coils between contacts 1 and 13 are shorted out so that only the coil for channel 13 is in the circuit. Notice that not only does each coil adjust to the correct frequency by separating or compressing the turns, but also that the relative position between the RF channel 13 coil and the mixer channel 13 coil will control the mutual coupling (designated M) from primary to secondary of this interstage coupling transformer. See mutual coupling later.

When channel 13 is correctly tuned, move the channel selector switch to channel 12. The channel 12 coil is in series with the channel 13 coil for the total inductance needed for tuning channel 12. Since the channel 13 coil has already been tuned, you can only adjust the channel 12 coil for this setting. At the same time, you will also be adjusting the antenna coil and the local oscillator coil for each channel setting.

Continue this process for all 12 channels until the switch wiper blade is at switch contact 12 on both wafers. At this time, the tuner is completely adjusted to receive all 12 channels.

The last coil (between contacts 12 and 13) is still shorted out when the 12 channels are aligned. Moving the switch wiper blade to contact 13 adds in the last coil, lowering the resonant frequency to the 40 to 47-megahertz (MHz) range to make the RF amplifier and mixer function as two additional stages of IF amplification.

Look again at Figure 13.2; the +24-V dc source is applied through the IF output transformer primary to the collector of Q_2 mixer and, from the source, through 680 ohms (Ω) to the swing arm of switch S3R, through channel 13 coil to the collector of the RF amplifier, Q_1. The dc voltage is applied to pin 5 of switch S6F and out pin 9 to the collector of oscillator Q_3 for all switch positions except when set to channel 1, UHF. Here the notch in the switch rotor, shown at pin 8, is aligned with pin 9, which is too short to make contact with the stator. The dc voltage will be removed from the VHF oscillator Q_3 and applied through pin 1 to the UHF local oscillator.

The signal path through the tuner starts at the VHF 300-Ω input terminals (lower left, Figure 13.2), through the *balun* transformer (T_1), through the FM radio trap circuit, through a coupling capacitor (C_3), to pin 1 of the antenna preselector switch S5R.

The impedance matching balun transformer converts the 300-Ω balanced antenna input to a 75-Ω unbalanced (single-ended) output. The name **balun** is a conjunction of the words balanced to un-

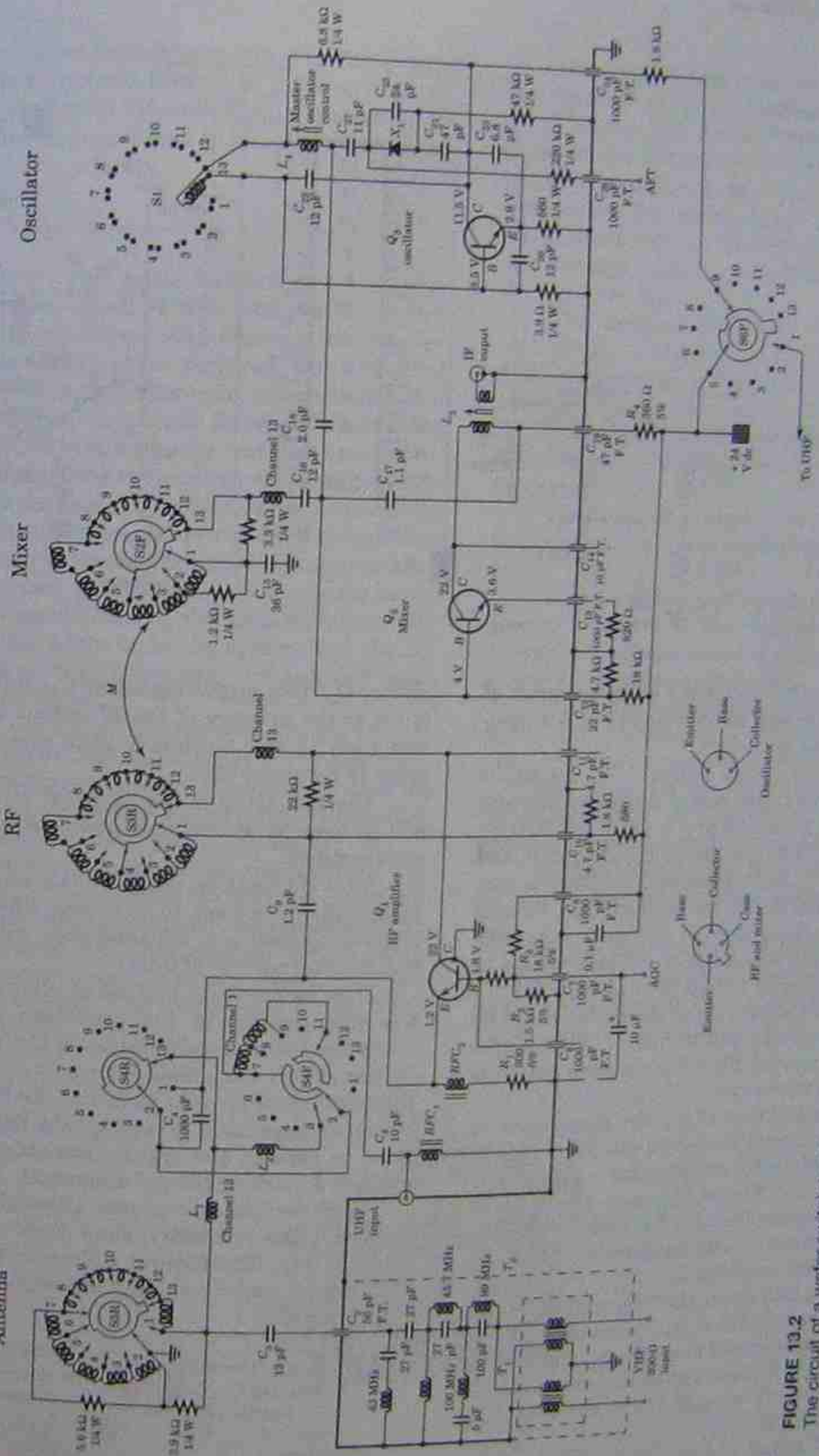
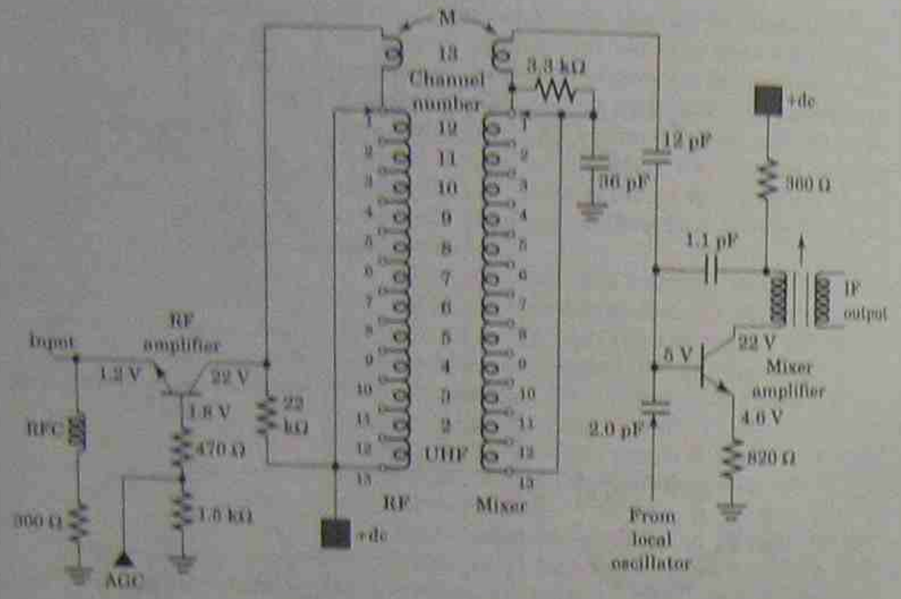


FIGURE 13.2
The circuit of a wafer switch tuner.

FIGURE 13.3
The RF amplifier and mixer wafer switch sections from Figure 12.2.



balanced. Figure 13.4 shows the effective circuit of a grounded center tap input primary to a single-ended 75-Ω output secondary.

Back at the antenna switch, S5R, the signal voltage that is developed across the preselector coil from pin 1 (and grounded at pin 13) is fed through L_1, the channel 13 coil, to pin 13 of switch S4R, and then out of pin 2 (S4R), through a coupling capacitor (C_4) to the emitter of the common-base RF amplifier, Q_1. The delayed AGC voltage is connected to the base of Q_1, which has a self-bias voltage of +1.8 V dc provided by voltage dividers R_2 and R_3.

The ground connection at the circle symbol for Q_1 indicates a metal-cased transistor with the case acting as a grounded RF shield to keep out noise and other RF interference.

From the collector of Q_1, the signal goes up through the channel 13 coil to pin 13 of the RF switch. Pin 1 of the RF switch is the +24-V dc supply and ac ground. Figure 13.3 more closely shows the mutual coupling from the RF channel 13 coil to the mixer channel 13 coil and through C_{15} to the base of the mixer amplifier, Q_2.

In Figure 13.2 again, the local oscillator signal comes from the collector of Q_3, up through capacitor C_{29} to the adjustable coil at switch S_1, and then out of pin 13 at S_1, through the oscillator master control coil, to the left, through C_{18} to the base of the mixer amplifier, Q_2.

The RF signal and the local oscillator signal heterodyne as they are amplified by the mixer amplifier, Q_2. The output signal at the collector of Q_2 is fed to the primary of the IF output transformer and then to the secondary that connects to the video IF amplifier chain.

The test setup is the same for all tuners and will be covered at one time after electronic tuners are examined.

It is difficult to pinpoint the advantages of wafer tuners, except to say that when they are properly aligned and adjusted they will work very well for long periods of time.

The painstaking process of alignment, which was just covered in the preceding paragraphs, heads the list of disadvantages of the wafer tuner. As you closely reexamine Figure 13.1, imagine the three transistor circuits buried at the bottom of the switch arrangement. It requires the hands of a surgeon to replace the transistors (or other parts) without disturbing the coil alignment.

The mechanical contacts, although gold plated for maximum reliability, show wear after several years of use. The natural collection of dust, dirt, and grease made switching of components a difficult task at these high frequencies. The switch contact problem was not limited to the wafer switch tuners; it applied to all mechanical tuners and will be identified in less detail as other tuners are examined.



FIGURE 13.4
The circuit of a balun transformer.

13.3.2 Turret Tuners

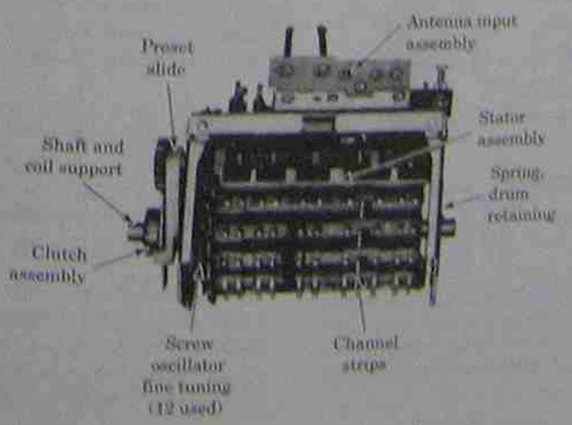
Although the turret tuner had several advantages over the wafer tuner, it still retained the switch contact problem. Figure 13.5 shows a turret tuner with the shielding cover removed. The advanced tuner design has each channel's coils mounted on a plastic strip with rivet heads forming the switching contacts. When one coil strip was found defective, then only that channel strip was replaced by a new one. All the channel strips could be removed, except one working channel, to provide maximum free working space for testing or replacing components.

The circuit location remains the same as for all in-line tuners. That is, the local oscillator is at the front, the mixer is in the center, and the RF amplifier is at the rear where the antenna input terminals are found.

There are many similarities between the circuit of the turret and wafer tuners. The major differences are the mechanics of switching coils for channel selection, as seen at the top of Figure 13.6, a typical circuit for the turret tuner family.

Channels 2 through 12 are mechanically the same except for the value of the inductances, which are not noted. All 12 channels are represented by one channel strip. The UHF channel strip is designated as channel 1 in the figure. The UHF input terminal to contact 1 is a dead end for all VHF channels.

FIGURE 13.5
Side view of a turret tuner with the cover shield removed.



The input signal from the VHF antenna enters the tuner at the balun transformer in the lower left of Figure 13.6. From the balun transformer it passes to the FM radio trap circuit, then through a coupling capacitor C_2 to contact 3 on the channel strip, where the signal voltage is developed across the antenna coil L_4. The voltage across L_4 is coupled through C_3 to the base of the common-emitter RF amplifier, Q_1.

The delayed AGC bias voltage is applied through R_2 to the base of Q_1. The recommended AGC voltage range is from +1.2 to +3.5 V dc; 1.2 V provides the lowest gain, whereas 3.5 V achieves the highest gain. Without an external bias voltage, the base has no self-bias and the amplifier will go into cutoff.

The transistor symbol for the RF amplifier and mixer shows the grounded metal case as an RF shield.

The collector output signal of the RF amplifier goes to contact 6 on the channel strip, where the energy is mutually coupled from L_5 primary (RF coil) to L_6 secondary (mixer coil).

The dc collector voltage of Q_1 arrives at contact 7 of the channel strip, coming through R_1 from the +18-V dc source at the lower left of Figure 13.6.

The signal voltage that was coupled into L_6 leaves the channel strip at contact 9 and goes to the base of the common-emitter mixer amplifier, Q_2.

The base bias for the mixer, Q_2, is developed by the voltage-divider circuit consisting of R_5 and R_4.

The local oscillator signal developed across the oscillator coil L_7 primary is mutually coupled to the mixer coil L_8 secondary and into the base of the common-emitter mixer amplifier, Q_2.

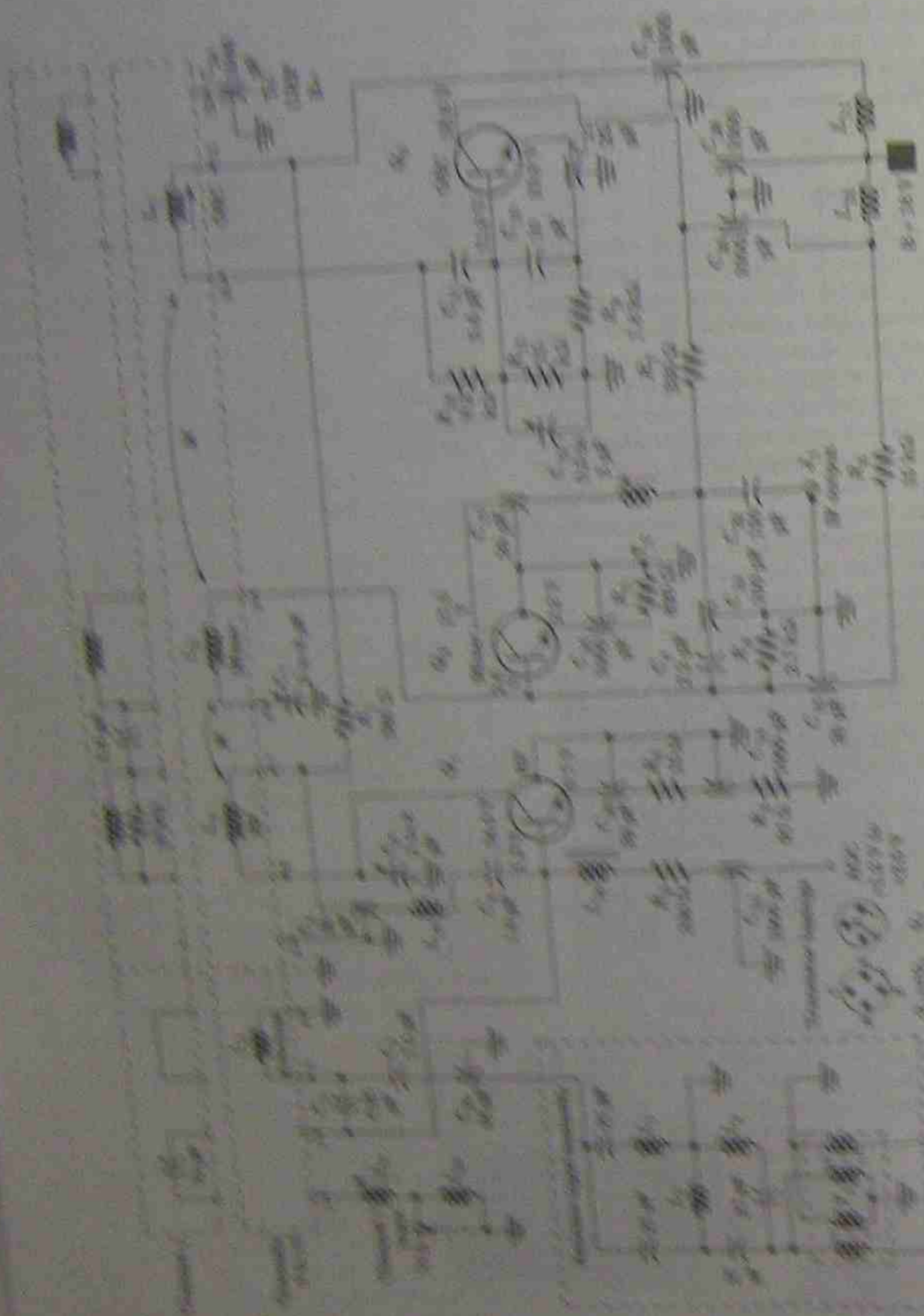


FIGURE 13.5
A typical turret tuner circuit. (Courtesy of Sylvania and GTE.)

Notice the high dc voltage (11.0 V) at the base of oscillator Q_3, which comes from the +18-V source, through the oscillator coil L_7, and then to the voltage-divider network of R_{10} and R_{11}.

The RF signal and the oscillator signal, both mutually coupled into the mixer coil L_6, are fed to the base of the mixer amplifier Q_2 and heterodyned as they are amplified by the mixer amplifier.

The IF signal at the collector output of Q_2 is capacitively coupled through C_{20} to the IF output terminal.

Alignment of the turret tuner is still accomplished by separating or compressing the turns of coils L_4, L_5, and L_6. However, very little can be done to change the mutual coupling between coils L_4, L_5, and L_6 because the coils are rigidly anchored to the coil strip and are almost immovable. All the VHF channels will operate as described above except for the frequency range as determined by L_4 and the oscillator frequency for each channel as determined by L_7.

When the UHF position is selected, the channel 1 strip is active and the tuner operation is modified as follows: (1) The UHF tuner will down convert all the input signals in the 40- to 47-MHz band of frequencies. (2) The UHF signal arrives from the UHF tuner into contact 1 of the channel 1 strip, through the 10-picofarad (pF) capacitor and out contact 2 to the base of Q_1. Contacts 3 and 4 are shorted to ground at terminal 4. Any VHF signal through C_3 will now be bypassed to ground at contact 4. The coupling capacitor C_1 is connected to ground at 4 to become a bypass capacitor for the UHF signal at contact 2.

Coils L_4 and L_5 on the channel 1 strip become an interstage, bridged-T coupling transformer using the 56-pF capacitor. This transformer is tuned to the 40- to 47-MHz frequency band. Transistors Q_1 and Q_2 are now two video IF amplifiers in this frequency band.

The dc voltage arriving at contact 11 is no longer connected through the oscillator coil for dc biasing the base of transistor Q_3. Without dc bias from Q_3 oscillator stops working. Instead, the dc voltage source is connected from contact 11 to contact 12 and becomes the dc source voltage for the UHF local oscillator.

The advantages of the turret tuner are the simplicity of the coil changing mechanism. Each channel strip is tuned independently of the other channel, coil's tuning. Each channel strip can be changed without affecting the other channels. All but the operating channel strips can be removed for easy testing and parts replacement.

The disadvantage is that it is still a mechanical tuner that changes electronic components at very high and ultrahigh frequencies. It does not depart from metal contacts and the problems associated with contact wear and dirt that cause poor electrical connections.

13.4 MUTUAL COUPLING

This term describes the degree of energy applied to the primary of a transformer, as compared to the energy that arrives at the secondary of the transformer. It affects the signal amplitude and bandwidth characteristics of the transformer. Although somewhat relative to all transformers, it takes on the greatest importance at the higher frequencies. Once past the design stage, the mutual coupling of a transformer is generally a fixed condition, and the technical staff farther down the chain of command has little or no control over the coupling factor.

The inductance of each coil and the coil capacity between the turns of the wires set the resonant frequency of the primary and secondary circuits. The distance between the windings establishes the mutual coupling. The coupling is the same when the coils are placed side by side or when both coils are wound on the same coil form, as seen in Figure 13.7a.

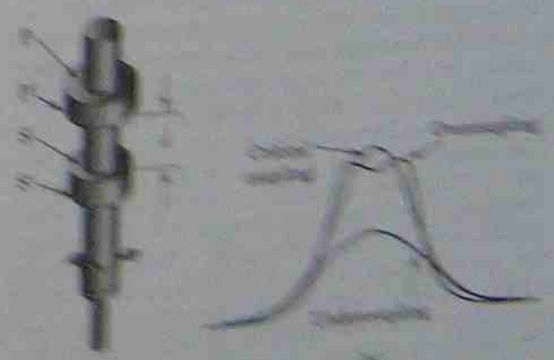


FIGURE 13.7
Mutual coupling. (Courtesy of Hayden Publishing Co., Inc., from A. Van Deventer, *Maximum Miniature Radio Receiver Techniques*, Vol. 2, © 1967, Hayden, p. 182.)

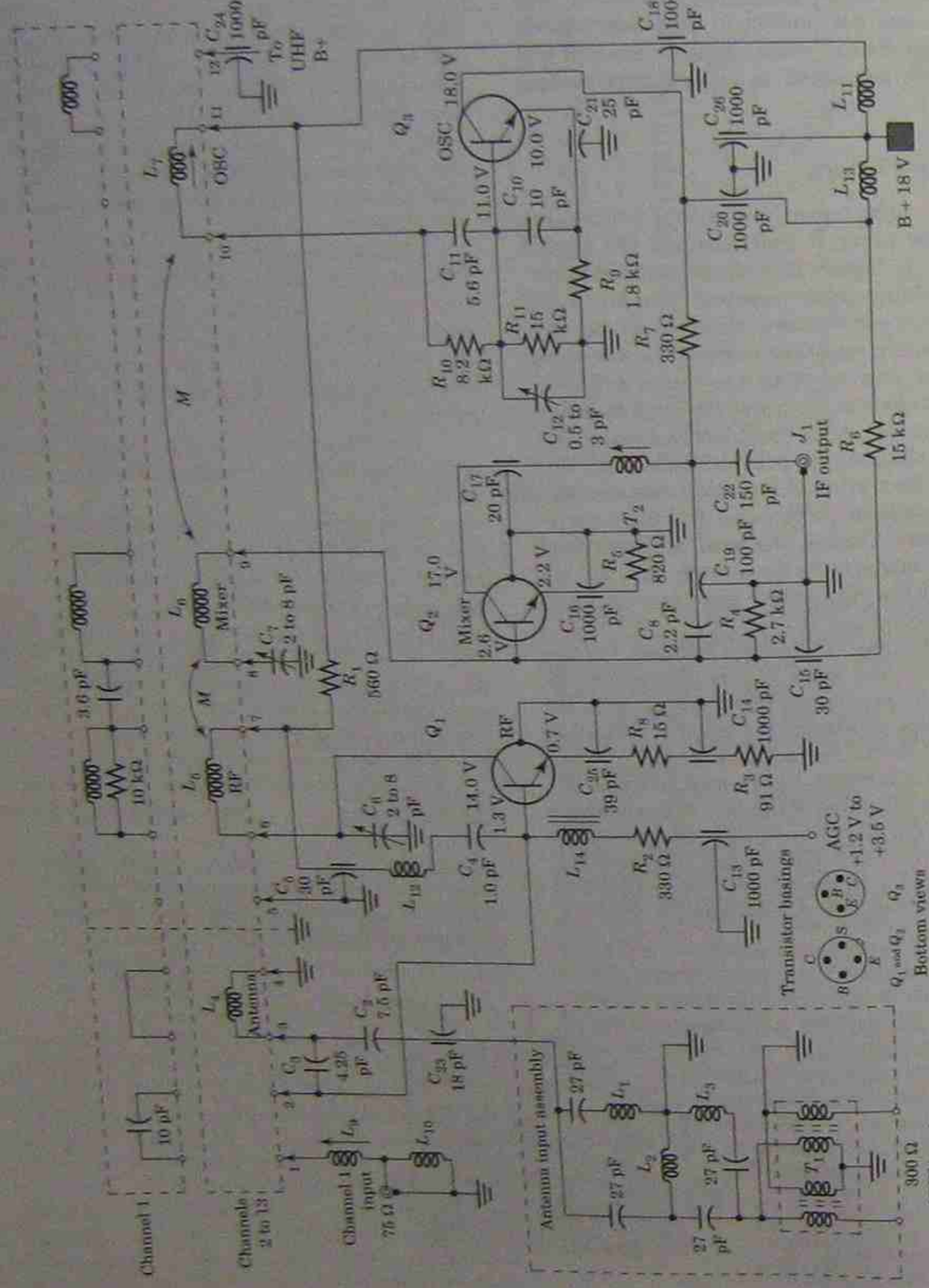


FIGURE 13.6
The circuit diagram of a typical turret tuner.

Notice the high dc voltage (11.0 V) at the base of oscillator Q_3, which comes from the +18-V source, through the oscillator coil L_7, and then to the voltage-divider network of R_{10} and R_{11}.

The RF signal and the oscillator signal, both mutually coupled into the mixer coil L_6, are fed to the base of the mixer amplifier Q_2 and heterodyned as they are amplified by the mixer amplifier.

The IF signal at the collector output of Q_2 is capacitively coupled through C_{22} to the IF output terminal.

Alignment of the turret tuner is still accomplished by separating or compressing the turns of coils L_4, L_5, and L_6. However, very little can be done to change the mutual coupling between coils L_5, L_6, and L_7 because the coils are rigidly anchored to the coil strip and are almost immovable. All the VHF channels will operate as described above except for the frequency range as determined by L_4 and the oscillator frequency for each channel as determined by L_7.

When the UHF position is selected, the channel 1 strip is active and the tuner operation is modified as follows: (1) The UHF tuner will down convert all the input signals to the 40- to 47-MHz band of frequencies. (2) The UHF signal arrives from the UHF tuner into contact 1 of the channel 1 strip, through the 10-picofarad (pF) capacitor and out contact 2 to the base of Q_1. Contacts 3 and 4 are shorted to ground at terminal 4. Any VHF signal through C_2 will now be bypassed to ground at contact 4. The coupling capacitor C_3 is connected to ground at 4 to become a bypass capacitor for the UHF signal at contact 2.

Coils L_5 and L_6 on the channel 1 strip become an interstage, bridged-T coupling transformer using the 36-pF capacitor. This transformer is tuned to the 40- to 47-MHz frequency band. Transistors Q_1 and Q_2 are now two video IF amplifiers in this frequency band.

The dc voltage arriving at contact 11 is no longer connected through the oscillator coil for dc biasing the base of transistor Q_3. Without dc base bias, Q_3 oscillator stops working. Instead, the dc voltage source is connected from contact 11 to contact 12 and becomes the dc source voltage for the UHF local oscillator.

The advantages of the turret tuner are the simplicity of the coil changing mechanism. Each channel strip is tuned independently of the other channel coil's tuning. Each channel strip can be changed without affecting the other channels. All but the operating channel strips can be removed for easy testing and parts replacement.

The disadvantage is that it is still a mechanical tuner that changes electronic components at very high and ultrahigh frequencies. It does not depart from metal contacts and the problems associated with contact wear and dirt that cause poor electrical connections.

13.4 MUTUAL COUPLING

This term describes the degree of energy applied to the primary of a transformer, as compared to the energy that arrives at the secondary of the transformer. It affects the signal amplitude and bandwidth characteristics of the transformer. Although somewhat relative to all transformers, it takes on the greatest importance at the higher frequencies. Once past the design stage, the mutual coupling of a transformer is generally a fixed condition, and the technical staff farther down the chain of command has little or no control over the coupling factor.

The inductance of each coil and the self-capacity between the turns of the wires set the resonant frequency of the primary and secondary circuits. The distance between the windings establishes the mutual coupling. The coupling is the same when the coils are placed side by side or when both coils are wound on the same coil form, as seen in Figure 13.7a.

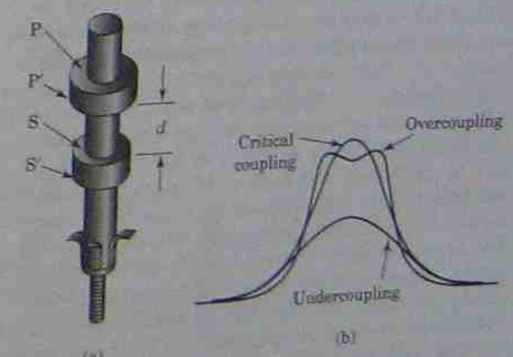


FIGURE 13.7
Mutual coupling. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 129, Robert J. Schoenbeck, © 1992.)

Inductive coupling begins when the primary and secondary are far apart. The energy that is transferred to the secondary is small, and the condition is called **undercoupled.** The effects of undercoupling are seen in Figure 12.7b as a low-amplitude output signal.

As the coils are moved closer together, the coupling increases to a condition called **critical coupling.** This is the point where the output signal reaches maximum amplitude. The center frequency and the circuit bandwidth remain constant for undercoupling and critical coupling.

Moving the windings closer together still creates a condition called **overcoupling.** Several important things begin to happen. The center frequency response begins to decrease below maximum output. In so doing, a double-humped frequency response curve takes shape, as seen in Figure 13.7b. The −3-decibel (dB) bandwidth is broader, and the skirts of the frequency response curve become steeper. The overall effect of overcoupling is to produce a relatively flat frequency response curve over a wider frequency range, with better selectivity at a slight sacrifice in output signal level. Many RF and IF transformers in television are overcoupled to take advantage of these conditions.

13.5 NEUTRALIZATION

Neutralizing a circuit means to cancel the effects of the interelectrode capacity of the active device in the circuit (tubes or transistors). Capacity is formed when any two conducting materials are separated by an insulator (or semiconductor). For transistors, there is a measurable capacity between the base and emitter, between the base and collector, and between the emitter and collector. The base-to-collector capacity is the most offensive in amplifiers that have a collector output signal that is 180° out of phase from the base input signal. Some of the output signal will feed back to the base through the base-to-collector interelectrode capacity with enough additional phase change to cause the amplifier to break into oscillations at some high frequency. These are unwanted and are called **parasitic** oscillations because they feed on the good characteristics of the circuit. They cause overheating and distortion and reduce the normal gain of the amplifier. Parasitic oscillations can be seen on an oscilloscope. Figure 13.8 shows various degrees of parasitic oscillations.

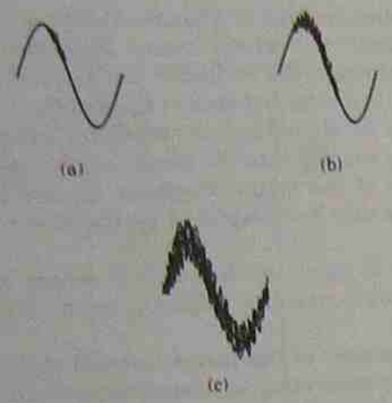


FIGURE 13.8
Various degrees of parasitic oscillations: (a) causes overheating only; (b) causes overheating and distortion; (c) severe overheating and distortion. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 60, Robert J. Schoenbeck, © 1992.)

Although this condition can occur in any amplifier, even audio circuits, it is most likely to be found

1. At frequencies generally over 25 MHz.
2. In tuned RF amplifiers that have the input and output tuned to the same frequency.
3. In any three-element active device (tubes or transistors).

Interelectrode capacity is canceled and parasitic oscillations are neutralized by finding a point in the circuit that has a signal phase opposite the signal phase at the collector (usually across the output transformer primary) and by feeding some of this signal back to the base of the amplifier through a capacitor having a value approximately equal to the base-to-collector interelectrode capacity.

Several circuits are used to neutralize an amplifier. C_9 and C_{12} in Figure 13.2 are neutralizing capacities. L_7, C_4, and C_8 are neutralizing elements in Figure 13.6.

See *Electronic Communications: Modulation and Transmission*, 2 ed., by Robert Schoenbeck (Macmillan, Inc., New York, 1992) for in-depth studies of neutralization (p. 57 to 61) and mutual coupling (p. 127 to 131).

13.6 UHF TUNERS

The basic block diagram of the UHF tuner is the same as for the tuners covered so far in this chapter. The housing is divided into three totally shielded chambers to control the interaction between circuits (Figure 13.9). Several important differences set these tuners apart from those previously discussed and need to be addressed here. Although all UHF tuners change frequency selection with a set of ganged variable capacitors, some tuners have a 56-position detente to mechanically center the tuner selection, while others are continuously tuned. These UHF tuners have been given many type designations, and all are partly correct. The tuner operation is a combination of basic communication skills, transmission line theory, waveguide theory with resonant cavities, and slot coupling applications. The finished model that endured through many trial and error experiments remained virtually unchanged over the years of its popularity.

The RF section serves as a preselector in which the antenna signal is coupled from L_1 into L_2 in Figure 13.10. The series tuned L_2 (with C_1) depends on the Q rise in voltage across the coil for maximum energy output at the channel frequency. L_2 is a transmission line coil equivalent, as seen in Figure 13.10. The energy across L_2 is coupled through a slot in the partition (designated M in Figure 13.10) and appears across coil L_3 in the mixer section. After mixing with the oscillator signal, the heterodyned signal is coupled from L_3 to L_4 and output to the VHF tuner in the 40-MHz frequency band.

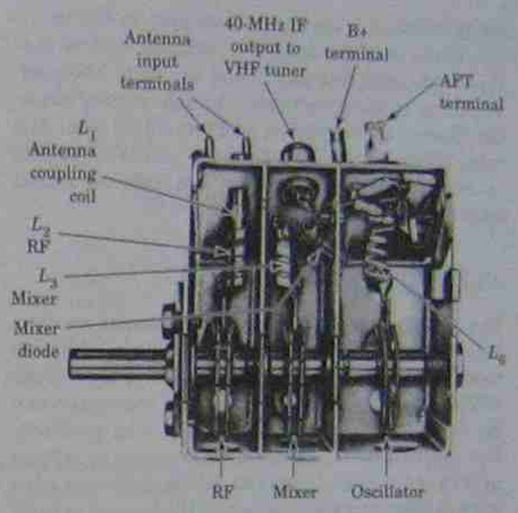
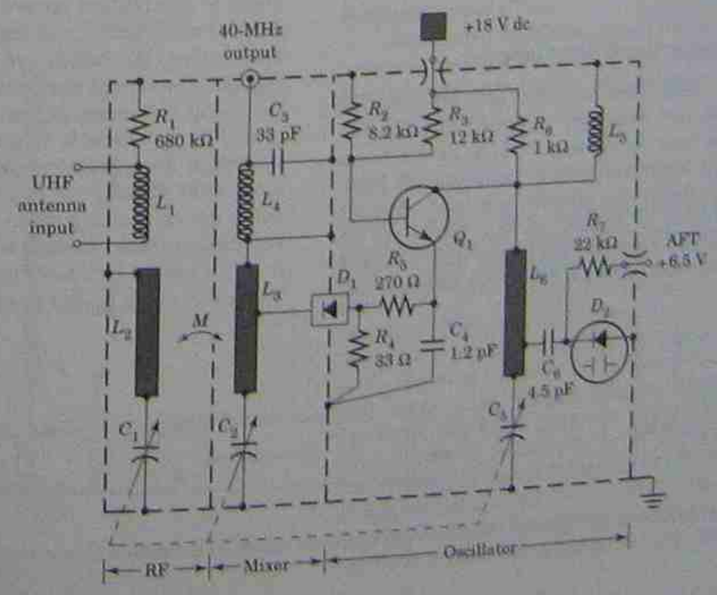


FIGURE 13.9
Side view of a UHF tuner with shielding cover removed.

The UHF local oscillator, Q_1, is also transmission line tuned by L_6 and C_5. The collector lead of Q_1 is soldered to the metal case as an RF shield. The oscillator output signal is emitter coupled through the mixer diode (D_1) and to the mixer coil L_3. The mixer diode is drawn with a different sym-

FIGURE 13.10
The circuit diagram of a UHF tuner.



bol to emphasize its physical position in the tuner. The diode is centered at the partition wall so that the anode lead remains in the oscillator chamber, while the cathode lead is fixed in the mixing chamber. Notice this condition in Figure 13.9 also. Any other diode position would cause oscillator pulling (oscillator frequency change) and reduced output with noise.

13.7 ELECTRONIC TUNERS

The changeover from mechanical tuners to electronic tuners was the greatest advance in television receiver design since the introduction of color in the 1950s. It is doubtful that you will encounter any mechanical tuners in modern television products. The mechanical tuner models are simple to explain and easy for the student to follow and were used here to start you thinking along the lines of general tuner operation.

As we open the discussion on electronic tuners, several advances need to be explored before actively digging into the new tuners. Some of the new circuits are three tuners in one. That is, they cover the VHF bands and UHF bands and have added the cable bands. The cable channels need to be examined. The tuners change from band to band using diode switching techniques that deserve an explanation. Third, individual channels are selected using *varactor* diode tuning, and this should be covered in advance of circuit analysis.

13.7.1 Cable Band Frequencies

When the television signals are transmitted through the air, they are assigned specific frequencies, as seen in Figure 13.11, so as not to interfere with other services transmissions. However, when the same signals are sent through cables, as seen in Figure 13.12a, there are no other signals on the cable that need to be avoided. The cable system is a closed network that can use the entire frequency spectrum for whatever purposes are deemed desirable. These signals will not radiate outside the cable, and outside signals cannot enter the cable. The television receivers (tuners) are designed to receive channels 2 through 6 (54 to 88 MHz), channels 7 through 13 (174 to 216 MHz), and channels 14 through 69 (470 to 806 MHz). The cable systems receive these signals and feed them into the cable unchanged. However, all the frequencies between these bands are void of signals. The cable companies then receive other signals, usually from satellites, and down convert them to fit in the spaces between the standard television broadcasts bands. These spaces are assigned channel numbers and frequencies. Figure 13.12b shows the **midband** from 120 to 174 MHz with nine channels labeled A through I. At some later date, the band from 108 to 120 MHz was opened up to cable. A problem came up in the numbering assignment as to how to number the channels below the letter A. They are called A minus 2, A minus 1, then A, B, and so on (A − 2, A − 1, A, B, etc.). The **superband** was added from 216 to 300 MHz with 14 channels labeled J through W. Still later, the **hyperband** was added from 300 to 408 MHz, with 18 more channels labeled AA through RR.

13.7.2 Diode Band Switching

In the tuner that we will examine, the frequency range of one section covers the low VHF channels, the mid cable band, and the high VHF channels. In this section, the bands are specified as bands I, II and III. The circuit changes frequency by adding or removing inductances, as was seen in the wafer tuner, except here it is done electronically using switching diodes. Switching diodes are special devices that appear as extremely high resistances when not conducting (open circuit) and as very low resistances (short circuit) when conducting.

Figure 13.13 shows one possible arrangement using switching diodes to change frequency ranges.

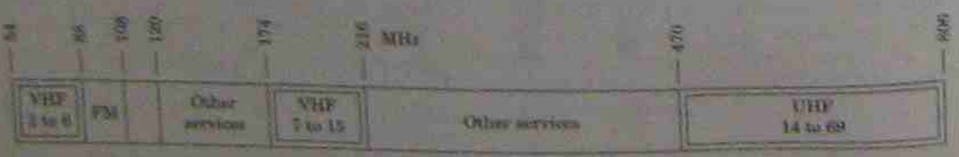


FIGURE 13.11
The television broadcast bands as they appear in the frequency spectrum along with other services.

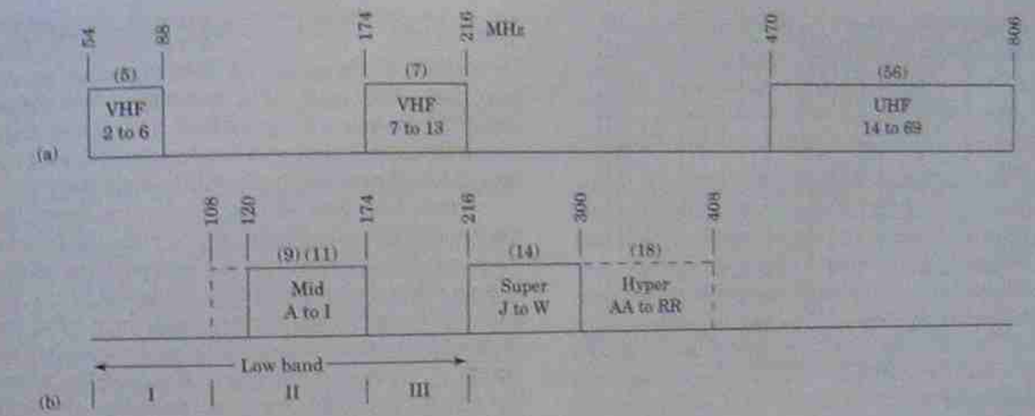


FIGURE 13.12
(a) The television broadcast bands as they appear on cable, void of all other transmissions. (b) The placement of the cable channels with respect to the broadcast channels.

This is a partial circuit of the RF amplifier output tuning and the mixer input tuning circuits.

Voltages V_1 and V_2 are the control voltages, which may be either high (+dc) or low (0 or ground). When V_1 and V_2 are low, none of the four switching diodes is conducting. L_1, L_2, and L_3 are in series, as are L_4, L_5, and L_6. The inductance in the circuit is maximum to pass the lowest band of frequencies, band I.

When V_2 is high while V_1 is low, the anodes of D_3 and D_4 (although at some dc level) are at ac ground potential and remove L_3 and L_6 from the tuning circuit. The total inductance is a medium value that selects the midband of frequencies, band II.

When V_1 is high and V_2 is low, the anodes of diodes D_1 and D_2 are at ac ground potential, and only the smallest of inductance L_1 and L_4 is in the circuit. The lowest inductance tunes to the highest frequency, band III.

Remember that the same switching arrangements are simultaneously taking place in the antenna preselector circuit and the local oscillator circuit.

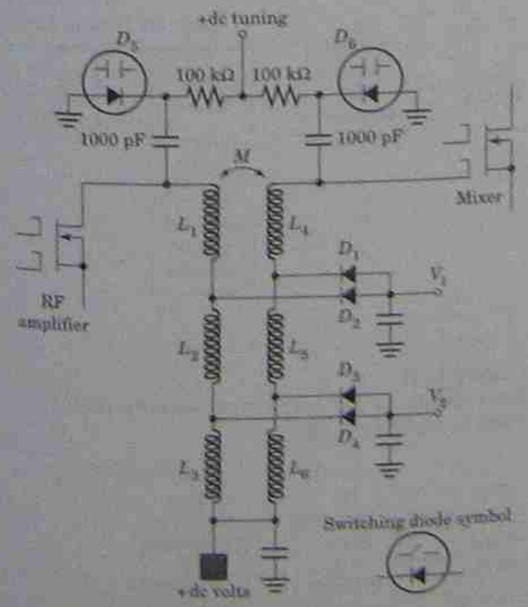


FIGURE 13.13
Switching diodes used for band selection, with symbol.

13.7.3 Varactor Diode Tuning

When reverse biased, all diodes resemble a value of capacitance between their terminals. Special diodes that enhance this characteristic are called **varactor** diodes, or **varicaps** or **voltage variable capacitors.** The value of capacitance changes with the specific amount of dc voltage placed across the diode terminals. Figure 13.14 shows the characteristic curve of the MV109 varactor diode. It will be the same as a 40-pF capacitor when −1 V dc is applied across the diode and 5 pF of capacity when the reverse voltage is increased to −30 V dc. Other diodes can range from 300 to 400 pF of capacity.

Diode D_5 in Figure 13.13 is the varactor tuning diode for the RF amplifier output and is electri-

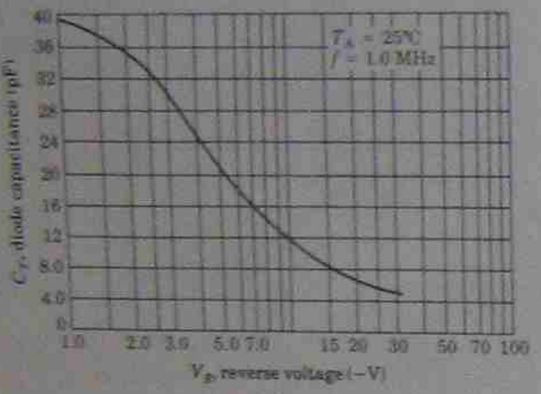


FIGURE 13.14
Capacitance versus reverse bias voltage curve for the MV109 varactor diode. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 205, Robert J. Schoenbeck, © 1992.)

cally in parallel with the primary inductance L_1, L_2, and L_3. The dc tuning voltage is isolated from the dc drain voltage by any large-value capacitor, 1000 pF in this example. Diode D_4 is the counterpart to D_3. D_4 tunes the secondary of the coupling transformer as the mixer input by its connection in parallel with L_4, L_5, and L_6. Both D_5 and D_6 get their dc tuning voltage through separate 100-kilohm (kΩ) isolation resistors.

A typical dc voltage change on a varactor diode of about 0.23 V will result in a frequency change for one channel shift in this example and the circuit to follow. Some diodes require as little as 0.10 V dc for one channel number change. Therefore, it is essential that a digital multimeter be used to measure the tuning voltage. Occasionally, students who learn the basics of electronics in digital circuitry are instructed to measure voltage with an oscilloscope. There are times when this practice is acceptable, but this is not one of those times. Use a voltmeter!

13.8 ELECTRONIC TUNER SCHEMATICS

Look ahead to Figure 13.19. This diagram may appear overpowering at first, but after a few simple observations, you will agree that it is not as tough as you thought. Think about using the following approach for all new and unfamiliar schematics.

First, look just at the transistors across the top row of circuits in Figure 13.19. Note the transistor name, the Q number, and their relative position to each other. Don't forget to include CR_1, the UHF mixer diode in the top center. Next, from what you have already learned about tuners, draw a block diagram of these circuits. Place the drawing across the top of the page, leaving room for two more sketches. Include arrowheads on the connecting lines to indicate the direction of signal flow. Figure 13.15 is one possible example of this exercise.

Do the same thing for the second row of transistors in Figure 13.19, including the mixer diode CR_2. Draw the second sketch on the same page for these circuits with lines and arrowheads for what you know to be a standard tuner block diagram. Did you end up with one block that does not fit into the general pattern? That's good if you did, because Q_3 does not belong to the superband circuit. Its

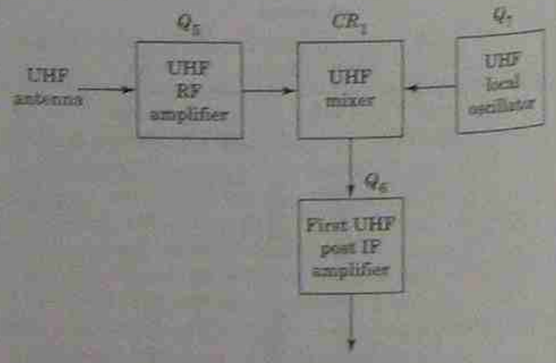
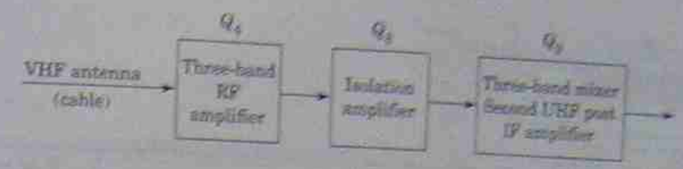


FIGURE 13.15
Block diagram for the top row of circuits in the electronic tuner (Figure 13.19).

FIGURE 13.16
Block diagram for the center row of circuits in the electronic tuner (Figure 13.19).



FIGURE 13.17
Block diagram for the bottom row of circuits in the electronic tuner (Figure 13.19).



place will show up later. Figure 13.16 is an example of this second exercise.

Once more, examine the bottom row of transistors in Figure 13.19 and draw a block diagram for this section at the bottom of the page along with the other two sketches. Include circuit names, Q numbers, and connecting lines with arrowheads. Here you may encounter some variations to what you have seen in other tuners. Use logic to complete the third sketch before comparing it to Figure 13.17. Finally, think about how these three tuners in one package must operate when called on to function on UHF or superband or VHF (three bands). Draw interconnecting lines with arrowheads to indicate how your circuits may be joined together into a single unit. Figure 13.18 is the solution to this exercise and is the block diagram for Figure 13.19.

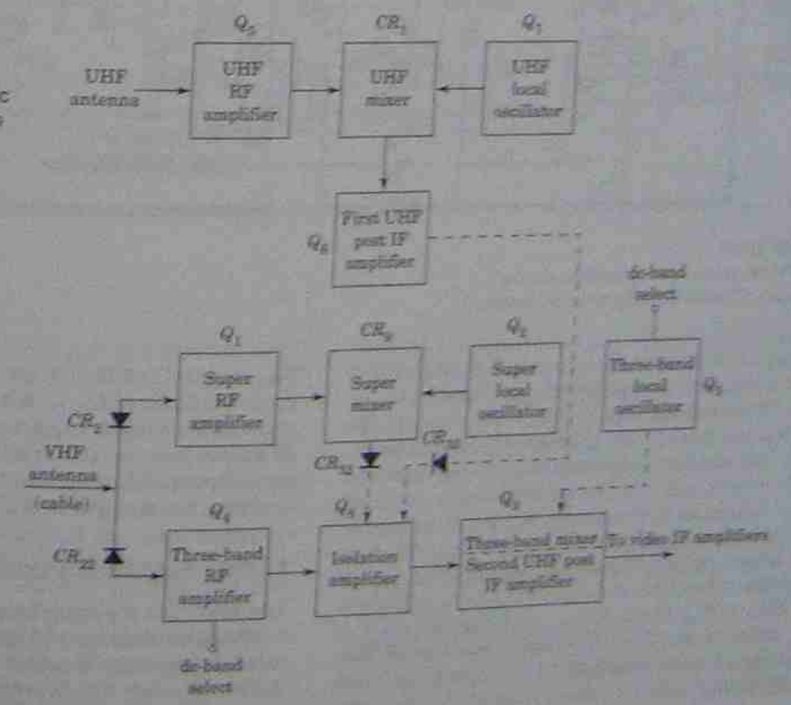
Some explanations are in order. An isolation amplifier, Q_8, is like a buffer amplifier or a linear mixer. There are three input signals in this case, but only one is processed at a time. The amplification and the output must be the same for either of the input signals and must be independent of the status of the other two signals. This is not an adder.

Diodes CR_{21}, CR_{22}, CR_{23}, and CR_{24} are switching diodes. When active, they are a short circuit to pass the signal and appear as almost zero impedance. When inactive, they appear as an open circuit with infinite impedance to block passage of the signal.

13.8.1 Low-band Operation

For three-band operation, diode CR_{23} is a short circuit, while CR_{21}, CR_{22}, and CR_{24} are open circuits. The UHF band and the superband are excluded from operation. The dc band-select voltages are enabled to select band I (channel 2 through 6), band II (midca-

FIGURE 13.18
Combination of the three previous block diagrams for the complete electronic tuner of Figure 13.19, with full interconnections.



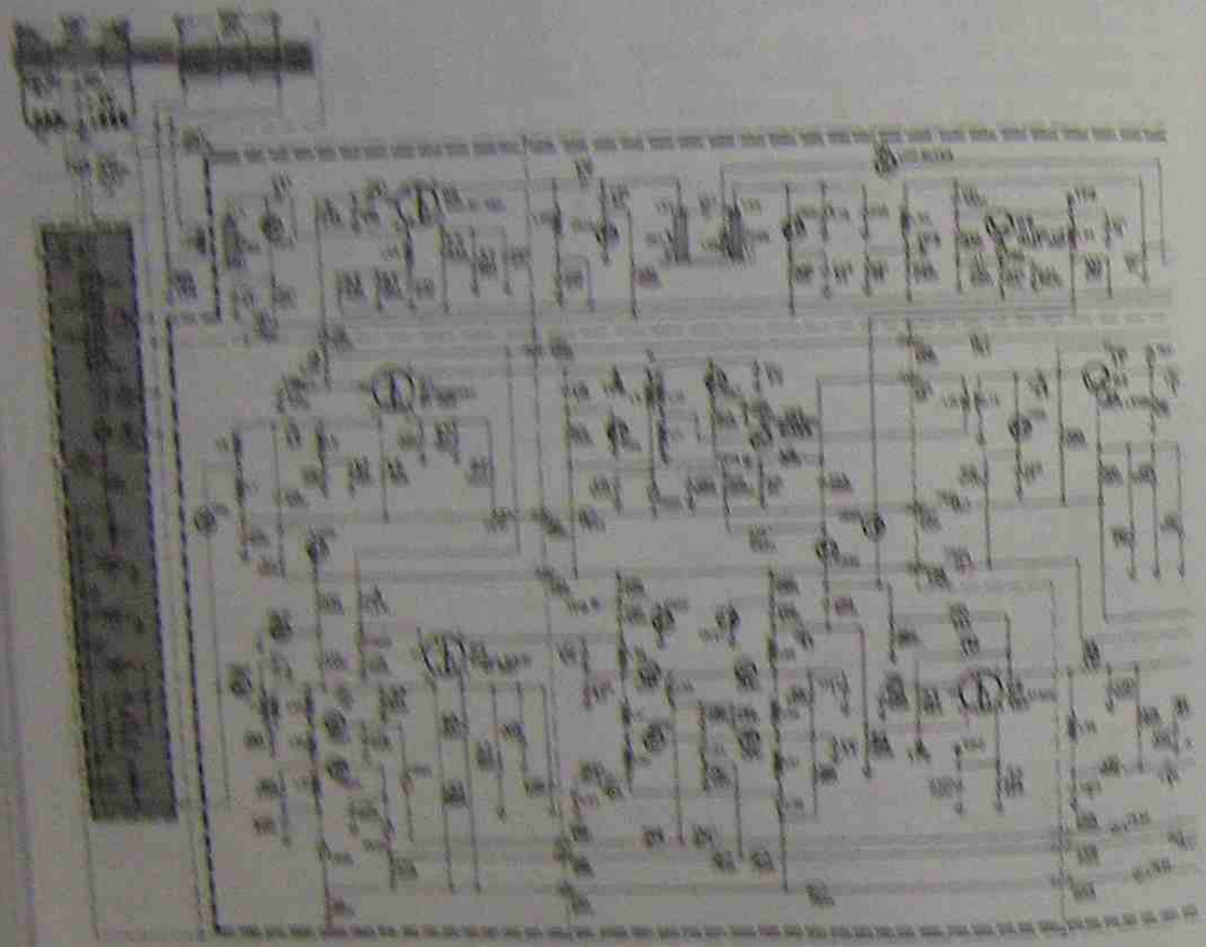


FIGURE 13.18
J.C. Penney & Co. electronic tuner circuit
(Courtesy of Howard W. Sams and Company.)

ble channels), or band III (channels 7 through 13) at the RF amplifier Q_1 and the local oscillator Q_2.

The low-band signal enters the tuner at the top left of Figure 13.18. VHF 300-Ω antenna terminals. The signal travels down through the filter and trap circuits, out the bottom terminal to CN_1 and CN_{20}. CN_1 is an open circuit, CN_{20} is a short circuit, and the signal appears across transformer T_1, out the secondary and through C_{12} to gate 1 of Q_1, RF amplifier. Then from the drain of Q_1 to L_{12} mutually coupled to L_{11}, through C_{10} and down to gate 1 of Q_2, isolation amplifier. This is the same circuit that was described in Figure 13.15. Then from the drain of Q_2 to the right and down through L_{14}, L_{15} and C_{100} to gate 1 of the mixer amplifier Q_3. Finally, from the drain of Q_3, to the right, down and right again to the output transformer L_{16} and L_{18} and the IF output jack J_1. The local oscillator signal leaves the collector of Q_2, up and to the left through C_{10} and then down to gate 1 of the mixer amplifier Q_3.

13.8.2 Superband Operation

The setup for the superband comes from our diagnostic block diagram of Figure 13.18. The dc band select voltages are disabled, the three-band RF amplifier Q_1 and the three-band oscillator Q_2 are inoperative. Switching diode CN_{20} is biased open.

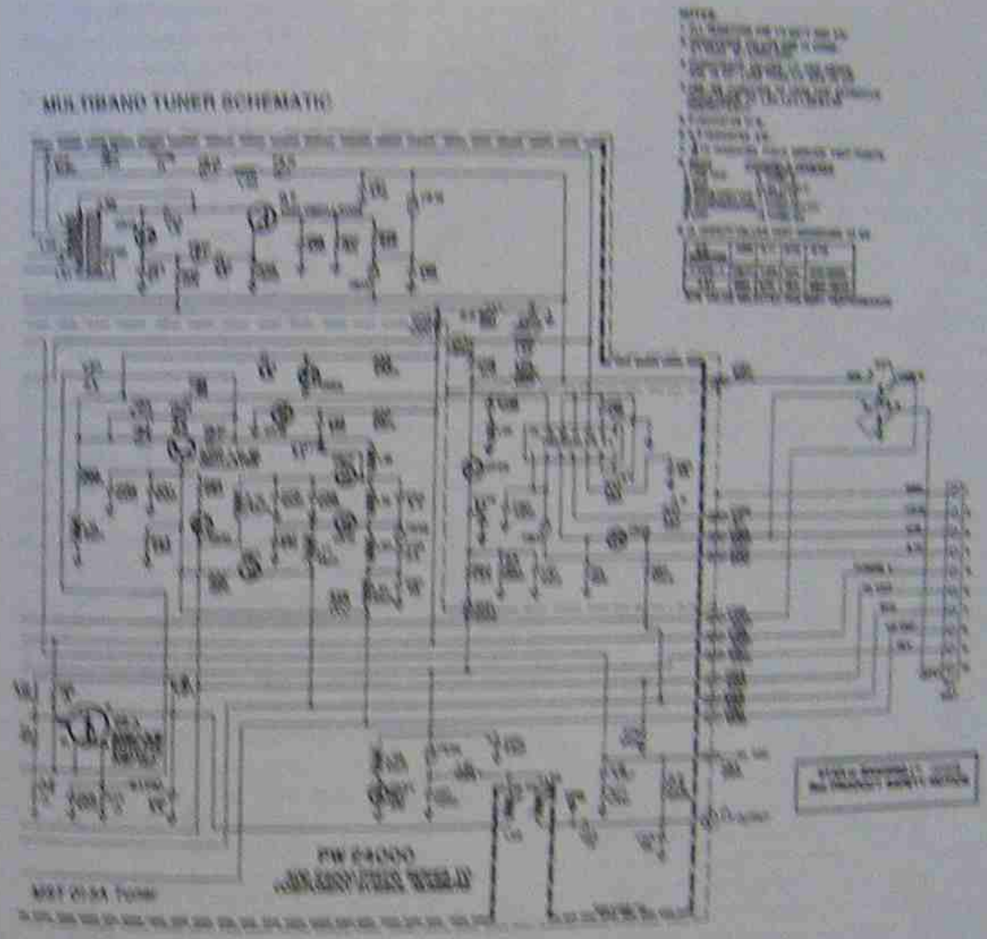


FIGURE 13.19
(Continued)

CN_1 is biased short circuit, and the antenna signal enters the superband RF amplifier Q_1. The Q_1 RF amplifier signal and the Q_2 local oscillator signal are mixed at CN_1 mixer and fed through CN_{20}, which is biased to pass the mixer signal to the isolation amplifier Q_2. Switching diode CN_{21} is biased open to block the UHF signal from the operation.

The signal path starts at the cable input, upper-left corner of Figure 13.19, down through the filter and trap circuits and then through CN_1, tuning coil L_8 and capacitor C_{10} to gate 1 of the superband RF amplifier Q_1. Then from the drain of Q_1, to the right and into transformer primary L_9. It is then coupled into L_{10} and L_{11} to the mixer diode CN_1 and the secondary L_{12} of the mixer transformer. The signal from the collector of the local oscillator Q_2 moves to the right through C_{11} and is coupled from the primary L_{13} to the secondary L_{14}. The mixer diode current and the oscillator signal current both flow through the secondary coil L_{14}, out the top of the winding and to the left, then down through C_{12}, CN_{20} and C_{10} to gate 1 of the isolation amplifier Q_2. From the drain of Q_2, through Q_3, to the IF output jack J_1 is the same as was described for lower-band operation.

13.8.3 UHF-band Operation

Look at Figure 13.18 one more time to see that CN_1, CN_{20}, and CN_{21} are switched to open circuits

so that they will block signal in this mode. The dc band-select voltages are set to zero to render the three-band RF amplifier and the three-band oscillator circuits nonoperational. However, CR_{3a} is shorted/terminated to pass the UHF heterodyned signal to Q_3.

The signal enters at the top-left corner of Figure 13.19 on a separate 300-Ω UHF antenna input terminal. The signal transfers from L_{3a} to L_4 (transmission line secondary), through C_{4a} to gate 1 of Q_3, UHF RF amplifier. From the drain of Q_3, the signal passes through C_{4c} to the primary L_{4b}. This transmission line transformer has two secondaries. Secondary L_{4a} is used for tuning only. Secondary L_{4b} couples the RF signal out to CR_1, the mixer diode. The mixer diode current, due to the RF signal, passes through L_{5b}, oscillator transformer secondary, where it is joined with the oscillator signal for mixing.

The oscillator signal passes from the collector of Q_2 to the primary L_{5a} of the oscillator transformer and joins the RF signal current in the secondary coil L_{5b}. The two signals (RF and oscillator) come out the top side of winding L_{5b}, to the left through C_{5b} and into the emitter of the common-base post IF amplifier 1, Q_4.

The collector output of Q_4 goes down through L_{6a}, to the left, and down through CR_{2a} and C_{6a} to gate 1 of the isolation amplifier Q_5, and from the drain of Q_5 through Q_6 and to the IF output jack J_1 as before.

The transmission line coils in the UHF tuner section L_3, L_{3a}, L_{3b}, and L_{3c} are printed copper foil on the circuit board. Their physical size determines the inductance and the resonant frequency of the circuit. If the size of the foil pad is not 100% accurate, the frequency of the resonant circuit could be in error by several megahertz. These coils are tuned by scraping off some of the circuit board foil to decrease the inductance and by adding a layer of solder to increase the inductance. This skill takes considerable practice before it can be mastered. A separate small strip of foil (or wire), soldered to ground at one end and floating at the other end, is placed close to the inductance pad. The relative position to the pad forms a tuning capacitor, noted in Figure 13.19 as C_{3a}, C_{3b}, C_{3c}, and C_{3d}. These are called **gimmicks** and are used to tune the circuits to resonance. Do not move these tabs or wires unless you are in the process of aligning the tuner.

13.9 RF AMPLIFIERS

We have already seen three of the five most common RF amplifier circuits to be used in late-model television receivers. These are the common-emitter RF amplifier of Figure 13.6, the common-base RF amplifier of Figure 13.3, and the dual-gate MOSFET RF amplifier in Figure 13.19. The remaining two are the cascode RF amplifier and the integrated circuit RF amplifier.

The common-emitter (or common-source) amplifier is popular because of its high-gain and low-noise characteristics. Its major drawback is the high value of base-to-collector interelectrode capacity. At these high frequencies, parasitic oscillations become a problem, and neutralization is necessary. The stability of the common-emitter RF amplifier is marginal.

The common-base amplifier has no phase shift from input to output and has less interelectrode capacity from emitter to collector, which makes the common-base amplifier more stable than the common-emitter amplifier. Neutralization is not required for most common-base amplifiers and is a trade-off for slightly less gain and slightly more noise than the common-emitter amplifier.

The **cascode RF amplifier**, given in Figure 13.20, has all the advantages of high gain, low noise, and low interelectrode capacity from input to output (base of Q_1 to collector of Q_2). It is stable and does not need to be neutralized. The cascode amplifier, for all its good features, has given way to the single-transistor, dual-gate MOSFET in popularity.

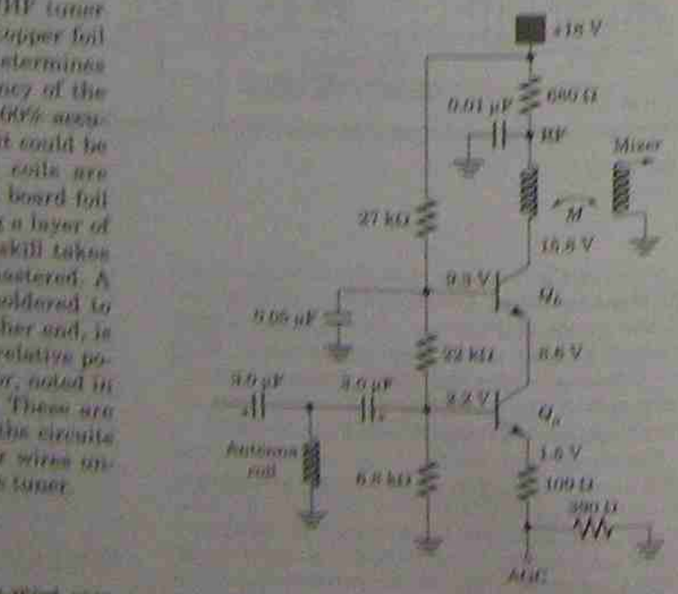


FIGURE 13.20
Cascode RF amplifier with AGC.

The dual-gate MOSFET operated in the enhancement mode (normally off) is a good compromise that achieves all the beneficial features and minimizes all the negative aspects that RF solid-state devices can offer. Any one of the RF amplifiers in Figure 13.19 can be used as an example. In Figure 13.21 we see that gate 1 (signal input terminal) is farthest from the drain output, which reduces the interelectrode capacity and minimizes the need for neutralization. This condition is further enhanced with gate 2 at ac ground potential, which acts as a shield placed between gate 1 and the drain output.

Field-effect transistors act more nearly like vacuum tubes because they are voltage-controlled devices, as opposed to other solid-state devices, which are current operated. For all practical purposes, we can say that there is zero gate current. Gate 2 has the same effect as a second control grid in a vacuum tube, and either gate may control the channel current as well as pinch off the drain current. Because of this feature, the dual-gate FET circuit resembles (but is not the same as) a cascode RF amplifier. The input signal is applied to gate 1, and the drain serves as the output. The AGC voltage (dc) is applied to gate 2 to change the gain without changing the operating point or affecting the linearity of the amplifier.

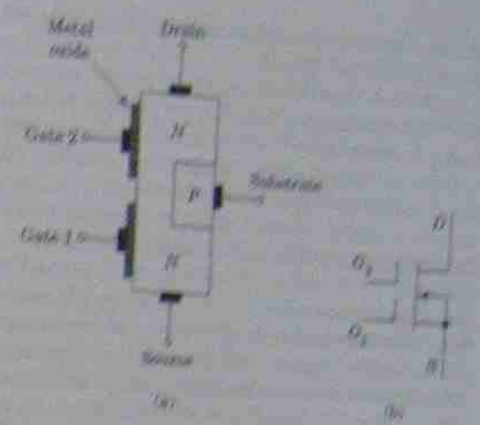
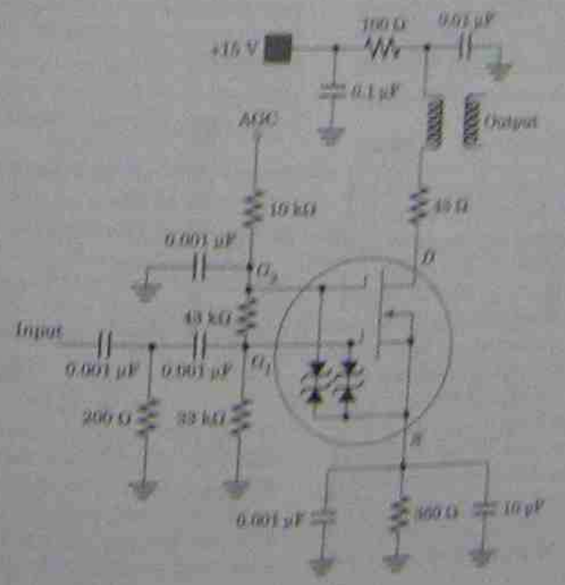


FIGURE 13.21
The model (a) and symbol (b) for a dual-gate, metal oxide, silicon, field-effect transistor (MOSFET).

The metal oxide used as the isolation between the gate and the channel is so thin that it is subject to puncture due to static voltages. To protect the transistor from damage, a pair of back-to-back diodes is added from each gate to the source, as seen in Figure 13.22.

All RF amplifiers are operated as class A amplifiers. The simple test question is whether you want to distort the signal. If you do not want distortion, use class A operation. Mixers use distortion that generates the sum and difference frequencies.

FIGURE 13.22
Field-effect transistor with diode protection at each gate.



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Mixers are operated in class A–B. Not truly class B, but definitely not class A.

Some LSI packages are finding their way into the RF amplifier position. Figure 13.23 is just one example. Because of the tight spacing between conducting surfaces in the integrated circuits, the shunt capacities and the interelectrode capacities present major problems. As the industry improves its construction techniques, more integrated circuits will be found at these high frequencies. To date, the integrated circuits offered as RF amplifiers have balanced input and balanced output connections. This is not a problem in circuit operation because the tuners are tested as a single unit. However, applying a signal to a balanced input circuit or measuring the output of a balanced circuit is more demanding when one side of the signal is not referenced to a ground potential.

13.9.1 Sensitivity

The specification known as **sensitivity** is a measure of the lowest input signal at the antenna terminals that will result in a demodulated output signal from the video detector that is 20 decibels (dB) greater than the noise alone at the detector output.

The input signal is a standard picture carrier frequency at the channel of your choice, 30% amplitude modulated by a 1-kilohertz (kHz) sine wave. The output noise is the peak-to-peak noise at the video detector when the test generator is connected to the antenna terminals, but with the generator power turned off. The receiver power is obviously turned on. The 20-dB ratio is used because 20 dB represents a voltage gain of 10. A noise measurement of 50 millivolts (mV) at the detector requires 500 mV (0.5 V) of signal at the detector output to achieve the 20-dB signal-to-noise ratio.

The sensitivity statement must contain two parts: the input signal level at the antenna in microvolts and the signal-to-noise ratio in decibels at the detector output. An example would be

sensitivity = 200 μV for 20 dB S/N

The sensitivity measurement is used to compare the performance of one receiver to another. The noise ratio must be the same for measurements to be comparable. Two hundred microvolts (μV) for 10-dB S/N would have an entirely different meaning than 200 μV for 20-dB S/N, since there is no correlation between the two noise figures.

A theoretical receiver that passes the antenna input signal through an RF amplifier with a gain of 10 dB (3.16), which adds 1 microvolt (μV) of noise, and then through the tuner mixer with a conversion gain of 6 dB (2), which adds 10 μV of noise, and then through three video IF amplifiers each with a wide open gain of 26 dB (20) and each adding 3 μV of noise, would have a detector output noise level of about 100 $mV_{p\text{-}p}$.

A 1-$V_{p\text{-}p}$ signal at the detector output represents a 20-dB signal-to-noise ratio. However, as the input signal increases through the IF amplifiers, the AGC voltage lowers the gain of the IF so that more input signal is required to compensate for the reduced gain. Practical experiments have shown that under these conditions about 500 μV of antenna signal are required to yield a 1-$V_{p\text{-}p}$ detector output signal.

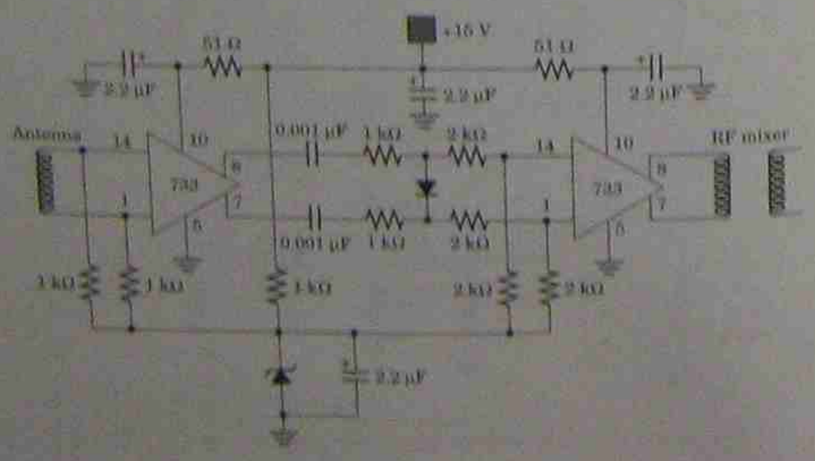


FIGURE 13.23
Microchip RF amplifier for the VHF band.

This example is given to acquaint you with real receiver values that you can use as a starting point when measuring sensitivity. It also shows that the mixer can have 10 (or more) times as much noise as the RF amplifier. This is because of the nonlinear operation of the mixer amplifier. It further emphasizes that the RF amplifier must be a really low noise amplifier that will add enough gain to override the mixer noise.

The noise in electronic circuits is due to the random movement of electrons through the components. We generally think of dc current as a constant flow of electrons, when, in reality, it is not perfectly constant. Current will fluctuate slightly depending on the exact path each electron takes through the component.

Electron collisions may cause one electron to speed up and another to slow down slightly. The net result is that the dc current is not 100% constant. These microscopic changes in dc current are measured as noise. Noise is random and covers a very wide range of frequencies. It has been labeled **white noise,** but is also referred to as **Johnson noise,** after the engineer who did a great deal of research into the causes of circuit noises.

13.10 TESTING TUNERS

The testing phase is divided into two groups, mechanical tuners and electronic tuners. However, three basic rules are applicable to all tuners.

1. When there is no picture and no sound on any channel, but there is snow (noise) on the CRT screen, it almost always indicates a defective RF amplifier. A broken antenna wire produces a very weak and snowy picture with some sound.
2. When there is snow (noise) on the CRT screen, the mixer amplifier must be working. Remember that the mixer is a noise generator because of its nonlinear operation.
3. When the performance of the tuner is different from one channel to the next, particularly when the lower channels work better than the higher channels, it indicates trouble in the local oscillator.

A substitute tuner may be your first test or your last test. When you have a working substitute tuner that requires a one-step cable change to complete the setup, this may be your first test. When the replacement tuner requires unsoldering and resoldering several wires, this may be your last test. Whichever way saves you the most time is the correct way.

Remember also that most large cities have a specialty repair business that repairs tuners only. You can find these in the yellow pages of your phone book, and many advertise in electronic trade journals. Let your degree of experience help you to decide when to use outside expert assistance.

When you have decided to test the tuner yourself and have made all of the preliminary tests that define a defective tuner, then check all externally applied voltages first. These are the B+ dc supply voltage, the automatic fine tuning voltage (AFT), and the automatic gain control voltage (AGC). Electronic tuners also have band switching voltages from an external source.

If the B+ supply voltage is not normal (check your schematic), this could be your only defect. Find the cause of this abnormal voltage and test the tuner again.

There are normally two wires into the tuner for the AFT circuit. Short these two terminals together at the tuner to eliminate the AFT as a cause for bad performance. This will not damage the receiver.

Some tuners will operate with the AGC voltage removed; others will stop operating with the AGC voltage removed. Check your schematic to determine the normal AGC voltage range; then remove the AGC wire and, in its place, connect a variable dc bias supply set to the center of the AGC voltage range. This voltage may be adjusted later as needed. Test the tuner again.

If the defect has not been found to this point, go to the signal injection test A or B for mechanical tuners in the next section.

13.10.1 Mechanical Tuners

Set the tuner to the UHF position and apply the signal to the UHF input jack on the VHF tuner. This will eliminate the local oscillator from this test.

Signal A is a 44-MHz carrier, amplitude modulated to 30% by a 1-kHz sine wave. The output for signal A is measured with an oscilloscope at the output of the video detector. Remember that the original tests determined that the video IF amplifiers and video detector are OK and that the defect is in the tuner. Start with the output of the 44-MHz generator set to zero and gradually increase the signal strength until you can measure 1 $V_{p\text{-}p}$ at 1 kHz on the scope at the video detector output.

When you do get an output signal, this tells you that the RF amplifier and mixer are OK and

the problem must be in the local oscillator. When you do not get an output, then reexamine your original test results. Was there snow (noise) on the CRT screen in the first tests? If there was, then the mixer is probably OK and the RF amplifier is not working. If there was no snow (noise), then this already hinted at a defective mixer amplifier.

When one of the three circuits has been identified as the probable cause of the malfunction, measure the dc voltages on the source, gate, and drain (emitter, base, and collector) of the active device in the defective circuit. This will almost always lead you to a single defective component.

The local oscillator is the only circuit that may not follow this pattern true to form. That is, the dc operating voltages on the oscillator may be near normal, but the circuit simply refuses to oscillate. This condition can be caused by changes in the characteristics of the transistor (or other components) due to aging and sustained temperature exposure. Often, simply changing the oscillator transistor with an exact replacement will correct the problem.

When you do not have a signal generator that can be amplitude modulated as for signal A, then use signal B. Signal B is a 44-MHz unmodulated carrier only. The output at the video detector is sensed with a dc voltmeter set to a low range. Remember that the video detector is a rectifier and filter that changes the IF signal (ac) to a dc output. Increasing the signal generator input level changes the dc level out of the detector. The signal B test will give you all the same results as the signal A test, but with slightly less accuracy, especially concerning distortion.

13.10.2 Electronic Tuners

The electronic tuner of Figure 13.19 may at first appear more complicated because of the increased number of circuits, compared to the mechanical tuner. However, the increased number of circuits makes the electronic tuner easier to troubleshoot. We will use the block diagram in Figure 13.18 (circuit of Figure 13.19) as a model and attack the system with the assumption that all the preliminary tests have been completed. That is, the tuner has been found to be the trouble area and the B+ voltage, AFT, and AGC voltages have been eliminated as probable sources of concern. Second, since it is unlikely that two circuits will malfunction at one time, we assume that there is only one defect in the tuner.

Other external voltages for electronic tuners are the band-select voltage and the varactor diode tuning voltages. These voltages may originate at a front panel key pad or from a remote control chassis, which are covered later. For simplicity, we will refer to these as control voltages and, for now, say that they are all normal. The control voltages in Figure 13.19 are applied to plug (P_1) in the lower-right corner of the schematic. The service manual includes a truth table by pin number and channel number for these voltages, that is, high–low for band-select voltages and dc step voltage levels for channel selection.

Close examination of Figure 13.18 shows that this electronic tuner is really three tuners in one assembly. Also, all three tuners use Q_6 isolation amplifier and Q_5 mixer–IF amplifier. Therefore, if any one of the 111 channels can be received, Q_6 and Q_5 must be in working order. When no signal can be received on any band, then Q_6 and Q_5 are automatically suspect because they pass all signals.

Case I. The VHF band is OK (three-band section), the superband is receiving signals, but there is no UHF reception. The UHF antenna, Q_8 UHF RF amplifier, CR_1 UHF mixer, Q_7 UHF local oscillator, Q_4 first IF amplifier, and CR_{33} UHF band switching diode are all open to investigative action.

Case II. The VHF band is OK (three-band section), the UHF band is OK, but there is no reception on the superband. The parts of the tuner that can cause this kind of malfunction are CR_2 input switching diode, Q_1 superband RF amplifier, CR_3 superband mixer, Q_2 superband local oscillator, and CR_{32} superband output switching diode.

Case III. Reception on the superband is OK and the UHF band is OK, but there is no reception on the VHF band (three-band section). The items to check in this case are CR_{22} VHF input switching diode, Q_4 VHF RF amplifier, and Q_3 VHF local oscillator. Remember that the control voltages are all normal, so the band-select voltages are not part of this problem, and because Q_6 and Q_5 operate on all bands, they can be eliminated also.

The circuits of each tuner section cannot be tested as simply as the mechanical tuners because they cannot be switched to the IF mode individually. However, Q_4 first IF amplifier, CR_{33} UHF switching diode, Q_6 isolation amplifier, and Q_5 second IF amplifier may be tested at the 44-MHz frequency when the UHF band is selected. Set the tuner to the lowest channel in the band to be tested. Set the input signal generator at the picture carrier frequency of the lowest channel in the band to be tested. These are 55.25 MHz for channel 2 in the VHF band, 217.25 MHz for channel AA in the superband, and 471.25 MHz for channel 14 in the UHF band.

Apply the input signal through an impedance matching pad (see Section 13.11) to the antenna terminals of the band to be tested. We will use channel AA in the superband as an example, with a carrier frequency of 217.25 MHz. If a signal is not noted at the detector output, test the two switching diodes by placing a 0.001-microfarad (μF) capacitor in parallel with each diode separately. The capacitor will pass the signal when the diode is defective.

If bypassing the diode does not produce results at the output, move the input signal to gate 2 of the RF amplifier. Follow the service manual for the correct procedure in this test. When the service manual does not give specific instructions, loosely couple a signal into the circuit as shown in Figure 13.24. Loose coupling is executed by attaching an open-ended loop coil from the signal generator to the point where you wish to inject a signal. The signal coil may be placed next to a circuit coil where it will act as a transformer. It may be placed to surround a transistor and induce a signal into the transistor by magnetic flux. The signal generator output level may need to be increased substantially, and herein lies the problem. You have no assurance of where the signal enters the circuit. If you place the loop coil around a transistor, is the transistor picking up the signal or is the signal strong enough to be coupled into the circuit coil next to the transistor? Placing a grounded metal shield between the loop coil and the circuit coil causes the output to decrease sharply when the coupling is from coil to coil and changes very little when the signal is induced into the transistor. This technique requires patience and practice before it can be mastered. The object is to find the circuit that is not doing the job it was designed to do. Then measure the dc operating voltages on the transistor to pinpoint the component that causes the malfunction.

The loose coupling signal injection method works exceptionally well in cases when you suspect a nonworking local oscillator. Set the tuner to the lowest channel in the band to be tested and loosely couple a signal into the local oscillator transistor at 45.75 MHz higher than the picture carrier frequency for that channel. Rock the generator frequency dial slightly while observing the CRT.

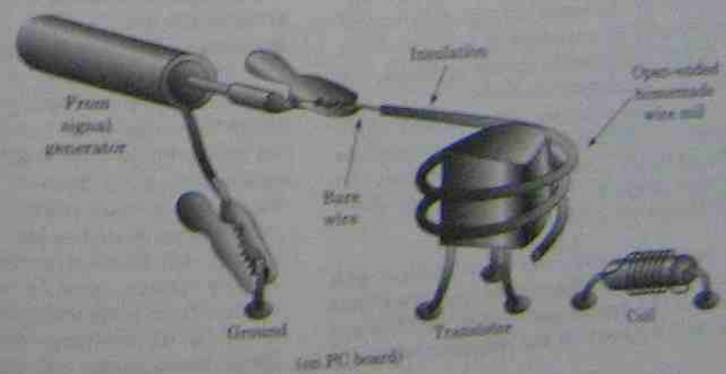
13.11 TUNER ALIGNMENT

Chances are that you will never need to align a tuner in your lifetime. The tuner will almost never misalign by itself, even with aging and temperature effects. These conditions have been planned for in the design of the tuner. The only time that you may consider aligning a tuner is in the case of major parts replacement. Replacing a transistor, resistor, or capacitor (other than tuning) should not require alignment.

When you are convinced that tuner alignment is your only course of action, first check the procedure described in the service manual for that particular receiver. The tuner should either be completely removed from the receiver or at least repositioned to allow for the maximum freedom of space that is needed for easy tuning adjustments. Figure 13.25 is a typical example of the alignment setup as prescribed by one manufacturer.

1. If the tuner is electrically connected to the receiver, ensure that the +dc power connection is as recommended. If not in the receiver, attach a

FIGURE 13.24
An example of loose coupling a signal into a transistor circuit.



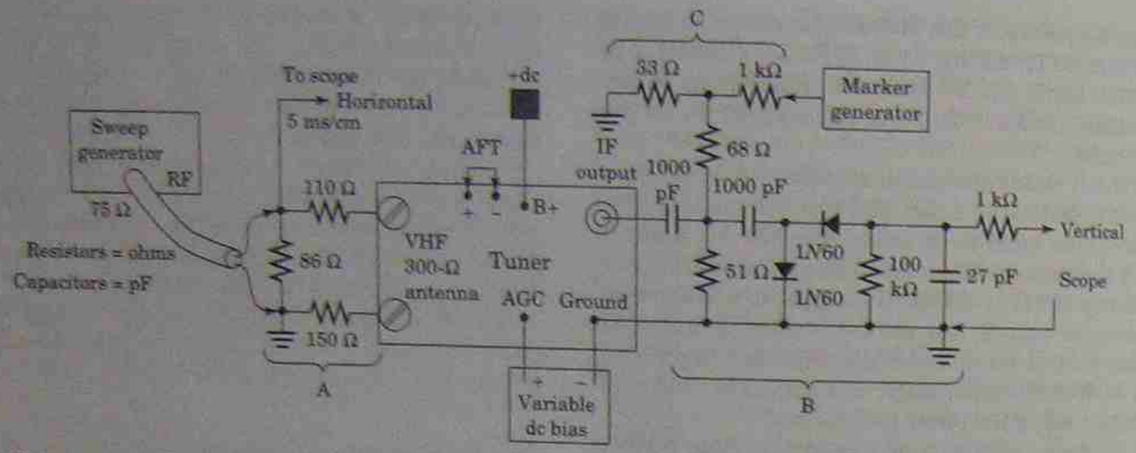


FIGURE 13.25
Sweep alignment setup for a typical tuner.

regulated external power supply set to the recommended voltage.

2. Remove the AFT lines and short the AFT terminals together at the tuner.
3. Remove the AGC line and replace it with an external variable dc bias supply set for the highest AGC voltage. Check your schematic for this value.
4. Disconnect the antenna. Replace it with the impedance matching pad A and the RF sweep generator. Pad A matches 75 Ω to 300 Ω. Also connect the sweep generator output to the horizontal input to the oscilloscope. Set the scope for external input.
5. Set the sweep generator to the center frequency of the channel to be tuned and for 10-MHz sweep width.
6. Remove the IF cable from the receiver at the video IF input terminal and attach the voltage doubler video detector circuit B at the output end of the cable. The 1N60 diodes are germanium because of the lower voltage drop across the diode (0.3 V) as compared to a silicon diode (0.7 V). When 1N60 diodes cannot be found, use any small-signal germanium diode.
7. Feed in the dual markers of 41.25 and 45.75 MHz through pad C. Remember that, regardless of which channel you feed into the tuner, the output will always be the heterodyned down video IF frequencies.

The service manual will next instruct you about the order of the adjustments and the effects to be noted on the oscilloscope. Figure 13.26 shows the limitations imposed on the response curve and that the output takes the form of a double-hump curve observed on the scope, with Figure 13.26d as the ideal response for all channels.

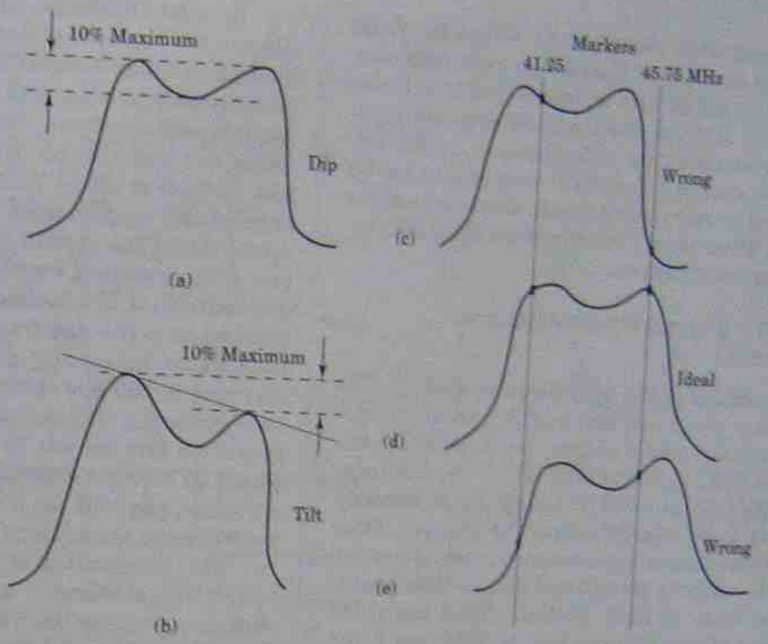
13.12 REMOTE CONTROL

This remote control feature is self-explanatory. The number of functions that can be controlled has expanded over the years, but what is more important about the changes are how they are done now as compared to then. The original hand-held transmitters were spring-loaded resonant rods (or bars), like a door chime, that when struck produced ultrasonic sounds in the 25- to 50-kHz frequency range. The length of the chime determined the frequency. Because of the bulk of the rods, generally only three or four functions could be controlled. The most common were (1) on–volume up, (2) volume down–off, (3) channel up, and (4) channel down. The receivers were made up of a group of narrowband resonant circuits that controlled relays or stepper motors to perform the actual work in the receiver that was associated with each function.

The disadvantage of these systems is that they are sound oriented. Although the sounds are above the range of the human ear, certain mechanical noises would false trigger the remote-controlled system. Jangling keys or rattling coins together would sometimes activate the remote control. The interference was random and unpredictable. No remedy was found to correct the problem. Because of their vintage, resonant rod remote controllers are omitted from further discussion.

The transmitters were the first to advance. They went to an all electronic oscillator that

FIGURE 13.26
Limitations on the frequency response case for tuner alignment: (a) maximum center dip; (b) maximum tilt; (c) frequency too low; (d) ideal curve; (e) frequency too high.



changed frequency depending on which button was pressed. Pressing a button applied the dc operating voltage and placed a selected value of capacity in the oscillator circuit that established the required frequency. The output was still acoustically coupled to the receiver and the false triggering remained, but now they were able to control many more functions, especially with the introduction of color television. The receivers remained almost unchanged during this period. Figure 13.27 illustrates this form of system. These units are easily tested with a dc voltmeter to ensure that the transistor can be powered up. Then use an oscilloscope low-capacity probe across the speaker terminals to see if each of the secondary circuits will induce an output signal of at least 1 V_{p-p}. The transmitter speaker is tested by substituting a high-impedance audio output transformer and small speaker in its place. The receiver is tested by disconnecting the input microphone and applying a sine-wave signal to the am-

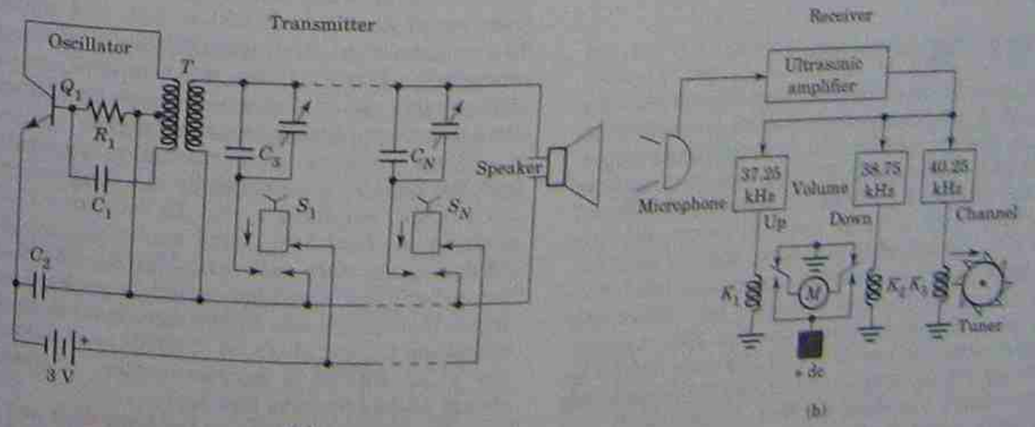


FIGURE 13.27
An electronic–ultrasonic remote control (a) transmitter and (b) receiver.

plifier input while observing the output for about $6V_{p\text{-}p}$ sine-wave signal. Change the input frequency between 25 and 50 kHz to ensure that each tuned circuit will activate. The functions were never assigned a standard set of frequencies, so the frequencies noted in Figure 13.27 may or may not be applicable to your specific circuit. Check the service manual. There should be a minimum of 1.5 kHz between any two functions.

13.12.1 Infrared Transmitters and Receivers

The invention of the light-emitting diode (LED) sparked a whole new series of remote-control devices because it freed us from the acoustical transmission link. Light-emitting diodes are PN junctions that, when forward biased, cause minority carriers to be injected across the junction. Once across the junction, the minority carriers recombine with the majority carriers and give up their energy in the form of light photons. With controlled amounts of zinc diffused into the tellurium doped gallium arsenide N wafer, the light photons peak at 1.1 micrometers (μm) of the infrared light region. The turn on and off time is less than 25 nanoseconds (ns). Infrared is not visible to the human eye, and these low-power-level infrared LEDs will not harm the eye. A red glow bar (RCA part 153093) placed in front of the LEDs converts the infrared light to a visible glow that is used to test the diodes.

The receivers use a light-sensitive diode (LSD) that outputs a voltage only in the infrared light range. Sunlight or incandescent light will not activate the LSDs.

13.12.2 Digital Encoding

A schematic diagram of a digitally encoded, infrared, hand-held, remote-control transmitter is given in Figure 13.28. The keyboard has been expanded to 36 functions (6 × 6 matrix), as many later model remotes have been. To transmit 36 different carriers, each 1.5 kHz apart as before, requires 54 kHz of bandwidth. This is too wide for what has become known as the ultrasonic remote band. Furthermore, since all 36 messages are individually encoded, only one carrier is needed. This manufacturer elected to use 45.5 kHz (455 kHz divided by 10) as the ultrasonic carrier and then amplitude modulated the data on this single carrier frequency, using a return to zero format as seen in Figure 13.29.

In binary language, 36 different messages requires a 6-bit code. How does the receiver recognize a code containing 6 zeros? To answer that question takes us back to basic data communications, where the message must contain a start frame, a data frame, and a stop frame. The start frame contains 6 bits, all high or all 1s. This signal opens the signal channel and synchronizes the bit timing to the receiver clock. The second frame, also containing 6 bits, is the command frame, which instructs the microcomputer of the function to be performed. The third frame is the stop frame and is exactly like the start frame, containing all 1s. The data transmission rate is 200 bps (100 Hz), so the 18-bit serial data stream is transmitted in 0.18 sec. Although this is too fast for you to see the data stream displayed on your oscilloscope, unless you have a storage scope, you will see a momentary pulse display on your scope as each button is depressed.

The transmitter contains a 36-position key pad, a digital encoder and amplitude modulator chip, a crystal-controlled oscillator, and a driver amplifier for two output LEDs in parallel. If one LED fails, the other will continue to operate, possibly with less efficiency. As you examine Figure 13.29, you will see that this remote is designed to control the television receiver and a VCR.

The receiver in Figure 13.30 is presented in block diagram form to emulate the schematic diagram. The chip circuits in the schematic are treated as *black boxes*. That is, a block is drawn to represent a function with input and output lines, but with no explanation of how the signal passes through the box, how the signal is internally modified, or what form the signal has at the output. The front panel assembly (FPA) is a 4 × 4 matrix, 16-key instrument that controls the television receiver only. The functions are commonly power, channel up, channel down, volume up, volume down, setup, and the 10 numerical digits.

When a channel change signal is transmitted from the remote, it is sensed by the light sensitive diode (LSD), amplified by the IR receiver (*U*3400) amplifier to about 5 $V_{p\text{-}p}$, and applied to pin 36 of the analog interface unit (AIU-*U*3300). *U*3400 is a narrowband RF amplifier tuned to peak at 45.5 kHz in this case. Inside *U*3300, the signal is demodulated and fed out at pin 34 (*U*3300) as raw data to pin 31 of *U*3100, a microcomputer. A channel change always requires two digits.

The first data stream is the ten's digit and the second data stream is the unit's digit. Channel 3 is selected as 0, 3. The microcomputer sends the ten's

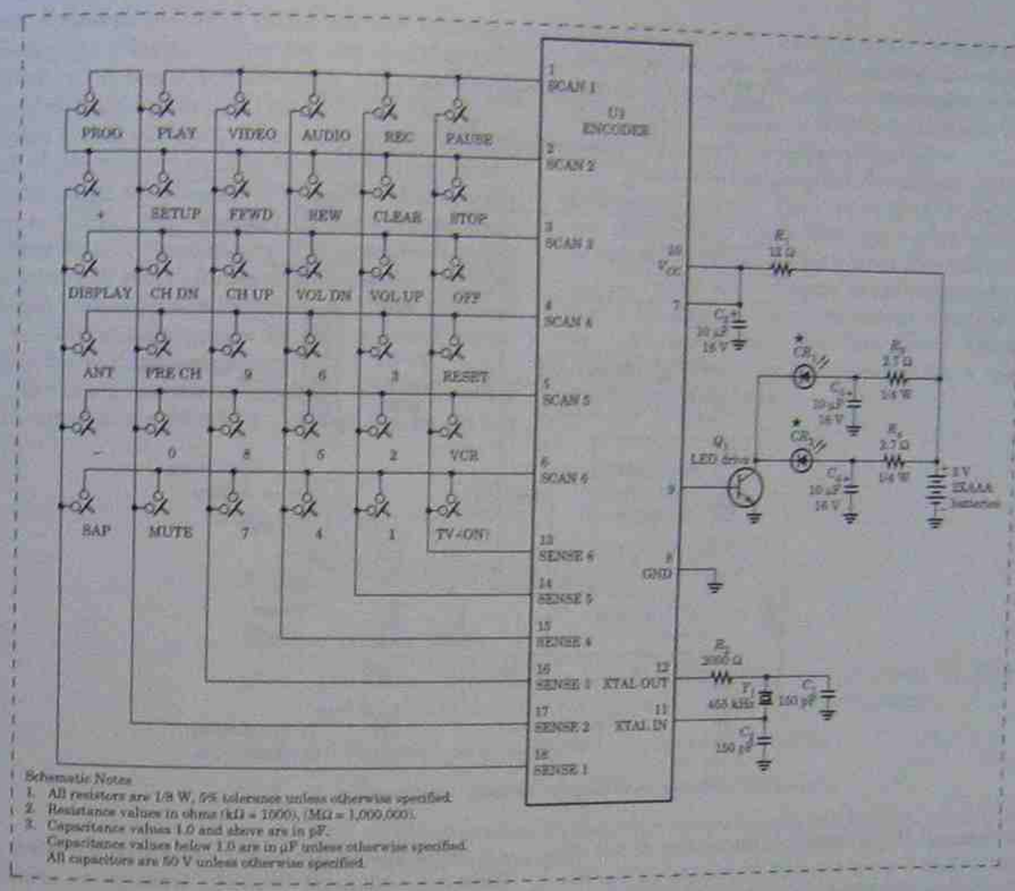


FIGURE 13.28
Digital remote control infrared transmitter schematic. (Courtesy of Thomson Consumer Electronics, Inc.)

digit out of pin 32, back to the AIU with instructions for "On Screen Display" (OSD) out of pin 24 of the AIU. The computer holds the ten's digit until it receives the second transmission, containing the unit digit data, before instructing the AIU to change channels via the tuning voltage (VT) line, pin 1 of *U*3300. When the second transmission is received, the unit's number is displayed on the screen immediately. The microcomputer analyzes both data packets and generates a new data message that instructs the AIU of the correct tuning voltage needed at the AIU output, pin 1, to tune

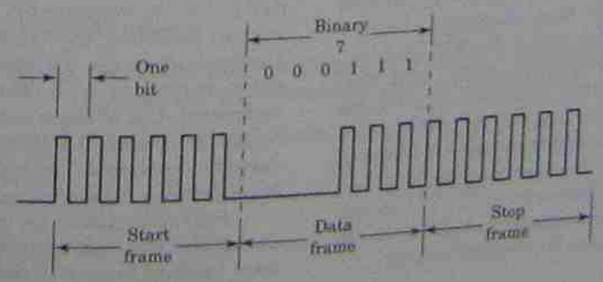
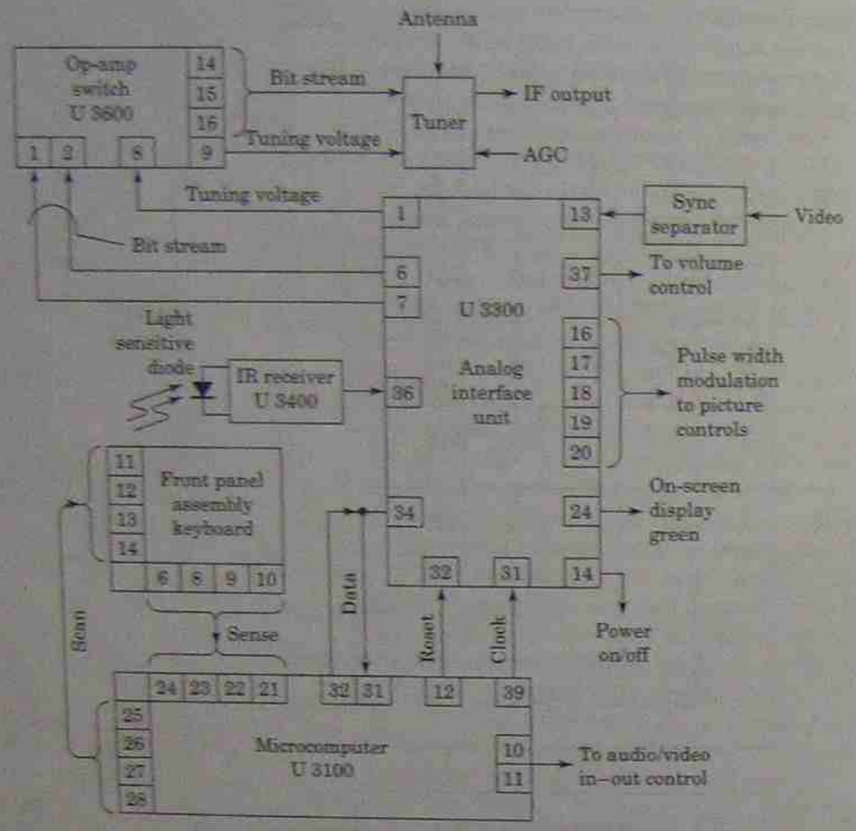


FIGURE 13.29
Bisync data communication message format used in digital remote control systems.

FIGURE 13.30
Infrared remote control receiver electronics as described in the text.



that channel. If the second transmission is not received within 5 sec of the first transmission, the microcomputer resets out of pin 12 and aborts the command. When the channel selection comes from the front panel assembly (FPA) keyboard, the process is the same except for the demodulation of the data stream of the analog IR signal.

A vertical and horizontal sync signal is needed at the AIU in order to locate the on-screen display for the menu and bar graphs that accompany the picture and sound control settings. A video signal is fed back from the luminance amplifier, through a second sync separator, to pin 13 of the AIU (*U3300*) for this purpose. The AIU is internally programmed to generate the signals for these display printouts.

The six control lines out of the AIU (volume, contrast, sharpness, brightness, color, and tint) carry an analog pulse width modulated signal to the destination circuits where it is filtered and changed to a dc voltage. The dc voltages set the conditions at the destination circuits by controlling the bias voltage on the amplifiers. Memory circuits in the AIU reestablish these signal voltages from the last setting each time the receiver is turned off and on.

Changes to the picture and sound control settings may originate from the front panel assembly (FPA) key pad or from the remote-control transmitter. The commands will be treated in the same way as the channel change commands until the data enter the microcomputer. Here the coded data directs the AIU to access the pulse width modulator of the selected control line and present a graphic display for that control setting. Pressing the +/− key increases or decreases the percent of pulse width modulation, which in turn alters the dc bias voltage on the affected circuit, as well as making the changes to the graphic on-screen display. After 3 sec of inactivity, the microcomputer resets the AIU to the standby condition. The audio–video in–out controls are used when the TV receiver is used as a computer monitor or with other external audio–video equipment. Use of these control functions will be included in Chapter 15. Remember where they originate from and how they operate so that a minimum of repetition will be necessary at that time.

Servicing tuners by using test instruments is by far the most accurate way, but only when you have total confidence in the accuracy of your equipment. A slower, but more rewarding way is to measure the dc voltages. After having diagnosed the problem as a tuner malfunction, measure the dc supply voltage, the dc AGC bias voltage, the dc AFT voltage, the dc collector, base, and emitter voltages in all of the suspect circuits to see if you can draw a conclusion as to where the fault lies. Include the band switching and channel tuning voltages when working on electronic tuners. The greatest majority of defects will result in a recognizable change in dc voltages somewhere in this testing phase. When all the dc voltages appear to be near normal, signal testing is the final test phase.

Servicing remote transmitters and receivers is much simpler because all the signals are at the lower frequencies. A dc voltmeter and an oscilloscope will help to locate almost any fault. Remember to compare the front panel assembly key pad operation with the hand-held IR transmitter performance as a means of isolating the defect.

Know what is expected of a circuit. Study the schematic diagram. Know what kind of signals enter the section. Know the input pins when microchips are involved. Know what pins are the output and what kind of signal should be found there. Know the section where the output signal is to be sent and how it will affect that circuit. These are your goals. When you have achieved them, you are a *television technician*.

QUESTIONS

Tuners and Remote Controls

Answer true or false.

13.1. The three major functions of the tuner are (a) channel select, (b) RF gain, and (c) reduction of the RF carrier to an intermediate frequency.

13.2. In the tuner, AGC is applied only to the RF amplifier.

13.3. A common emitter RF amplifier needs neutralization.

13.4. The major advantage of electronic tuners (over mechanical tuners) is that there are no moving parts.

13.5. The automatic fine tuning voltage (AFT) is applied to all circuits that have varactor diodes.

13.6. Switching diodes are used for frequency band changing only.

13.7. Switching diodes are active (on) with forward bias.

13.8. Varactor diodes are active (on) with reverse bias.

13.9. The sensitivity of a receiver states the lowest RF input level under specific conditions.

13.10. The circuits of an infrared remote control transmitter operate at the near-light frequencies of 270 terahertz.

Multiple Choice

13.11. The tuner local oscillator frequency is (a) higher than, (b) lower than, (c) the same as the selected RF carrier frequency.

13.12. What is the local oscillator frequency when channel 4 is selected?
(a) 67.25 MHz,
(b) 77.25 MHz,
(c) 113 MHz,
(d) 134 MHz,
(e) 216 MHz

13.13. What frequency is the VHF RF amplifier set to pass when the mechanical tuner is set for UHF reception?

13.14. Another name for the tuner is the _____.

13.15. Electronic tuners use _____ as the tuning element.

13.16. A balun transformer matches a _____ line to an _____ line.

13.17. An RF amplifier must be a good low _____ amplifier.

13.18. Two amplifiers connected in series to pass the same dc current are called a _____ amplifier.

13.19. The input transistor in Question 13.18 circuit is connected as a common _____ amplifier.

13.20. The output transistor in Question 13.18 circuit is connected as a common _____ amplifier.

13.21. The dc, AGC voltage is always applied to _____ of a dual-gate field-effect transistor.

13.22. The automatic circuit that locks the local oscillator onto the correct frequency is abbreviated _____.

13.23. A tuner with three active circuits will generally have how many varactor diodes?

13.24. What observed conditions would lead you to suspect a tuner malfunction?

13.25. Switching diodes are used to select channels.
(a) true
(b) false

13.26. Identify the circuit location in a standard three-transistor in-line tuner.

13.27. A tuner that uses a tapped coil for channel selection uses (a) the smallest, (b) the largest inductance to select the lowest channel frequency.

13.28. The mutual inductance of all transformers can be adjusted.
(a) true
(b) false

13.29. Neutralization cancels the effects of interelectrode capacity by feeding a signal back to the input that is _____.

13.30. The tuning voltage on a varactor diode should be measured with an oscilloscope.
(a) true
(b) false

13.31. The sensitivity measurement for a receiver must contain two values.
(a) true
(b) false

13.32. Sensitivity is a property of the first RF amplifier.
(a) true
(b) false

13.33. The two APT tuner terminals may be shorted together while testing a tuner with no ill effects to the system.
(a) true
(b) false

13.34. The tuner AGC line may be grounded while testing a tuner.
(a) true
(b) false

13.35. The dc voltages are always verified first before further tuner tests are conducted.
(a) true
(b) false

13.36. Tuner alignment is a fast and easy way to test the tuner.
(a) true
(b) false

13.37. A dc voltmeter, an oscilloscope, and a schematic will help you to find almost all remote-control defects.
(a) true
(b) false

14 Video IF Amplifiers, Video Detectors, and Automatic Gain Control

14.1 INTRODUCTION

This section of the television receiver has changed the least in function since the 1960s, even though the active devices have kept pace with the advancing technology. The amplifiers must still provide 60 to 80 decibels (dB) of gain over the frequency range of 41 to 47 megahertz (MHz) with a specific response curve. The AM detector still removes the composite video signal from the modulated carrier, and automatic gain control (AGC) is required to maintain a constant signal level out of the detector (within limits), regardless of the signal strength at the antenna.

The devices in the circuits have changed from vacuum tubes to solid-state transistors to microchips to large-scale integrated circuits, but all the assigned functions remain unchanged.

Many of the improvements to the circuits over the years are now buried inside the microchips and may never be made obvious to the modern technician. After all, the end question is, "Does the chip do what it is supposed to do when the correct signals and dc voltages are applied?" We will examine some of the circuits in the following text so that you can become familiar with the circuit input and output requirements.

14.2 IF AMPLIFIER CIRCUIT

You will notice that the block diagram has been passed over entirely in favor of a microchip schematic diagram. The reason for this is that the circuit diagram for a microchip or LSI circuit uses the black box approach to circuit diagrams. That is, devices are drawn in block diagram form with peripheral passive components. The microcircuit is readily adaptable to transistors, resistors, and diodes. There may be 10 or more transistors inside each amplifier in Figure 14.1, which would make for a very elaborate schematic diagram. Although capacitor and inductor techniques for microcircuits are well known, they consume a great deal of space so are best left as discrete external components, especially for adjustable coils. The manufacturers have chosen a compromise between a full disclosure discrete component schematic diagram and a block diagram as the way to present the greatest amount of information in the simplest form.

The amplifiers in Figure 14.1 are all in one microchip. The chip is shown separated into three parts for use in the drawing. U1-A is the first video IF amplifier, U1-B is the second video IF amplifier and U1-C is the third video IF amplifier, video detector, and gated AGC amplifier. The dc supply voltage is applied to pin 12 of U1-C and ground is at pin 4 of U1-A, representative for all sections.

The input signal from the tuner comes in at J_1, through an input tuning section, to pin 3 of U1-A and out at pin 6. Pin 6 is also the input to U1-B, the second video IF amplifier. The reason for bringing pin 6 to an output is to provide a terminal to connect the impedance-coupled load (L_3) for the output transistor of U1-A and the feedback gain resistors (R_4 and R_5) of the second IF amplifier.

Pin 9 is the output of U1-B in Figure 14.1 and sends the signal to three different destinations. The

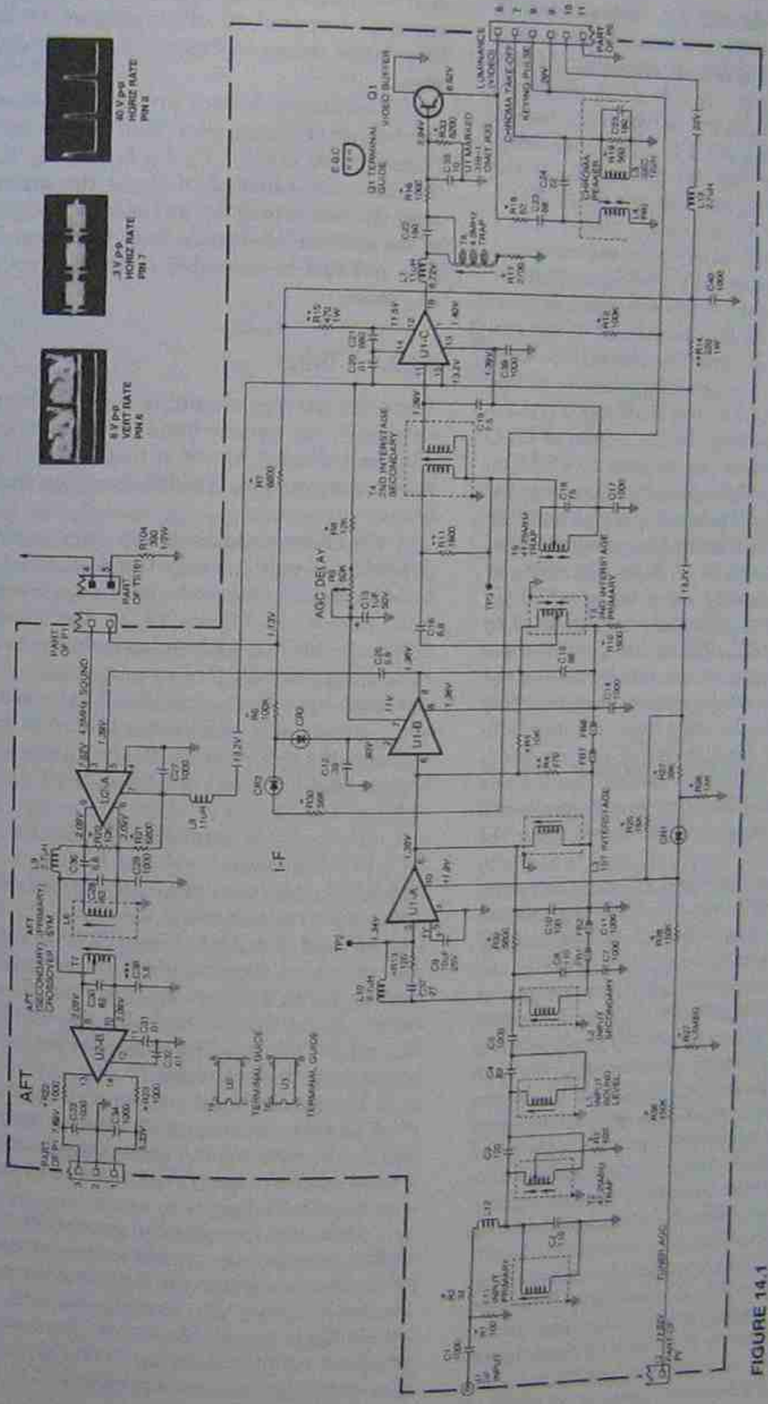


FIGURE 14.1
Wiring diagram for a video IF amplifier board including the automatic fine tuning (AFT) and sound carrier takeoff point.
(Courtesy of Thomson Consumer Electronics, Inc.)

output signal passes through C_{28} to the sound IF amplifiers and also to the automatic fine tuning (AFT) section of U2. The output signal at pin 9 is also sent downward to the top side of the second interstage transformer T_3, which serves as the output collector load impedance of U1-B. The signal comes out of T_3 at the center tap and through C_{16} to the coupling transformer T_4 and into pin 11 of U1-C. At the bottom end of T_4 is a notch filter called a **trap** that reduces the level of the sound carrier at 41.25 MHz that arrives at the third IF amplifier.

The schematic does not tell you that the video detector is inside U1-C. It is mentioned in the service manual. If you have only the schematic to work with, you can make a correct determination of this event as follows: At the input of U1-C (pin 11) there is a 41.25-MHz sound trap. At the output of U1-C (pin 16) there is another sound trap at 4.5 MHz. This is the frequency of the sound carrier after the picture carrier has been reduced to zero hertz. The picture carrier is removed by the video detector, placing the sound carrier at 4.5 MHz. Therefore, by deduction, the video detector must be part of U1-C.

T_5 is a bifilar wound transformer as noted by the special drawing of T_5. This is two parallel wires that are simultaneously wound side by side on the coil. One wire serves as the primary and the other as the secondary. Bifilar coils have a high coefficient of coupling, a high Q, and a narrow bandwidth. T_5 is a notch filter to further remove any sound carrier (at 4.5 MHz) that may be recovered, along with the composite video signal from the video detector.

The output signal of U1-C at pin 16 is passed along to the base of Q_1, the video buffer amplifier. Buffer amplifiers are used for isolation and impedance matching. As a common collector amplifier, Q_1 has a gain of less than 1. The luminance signal is taken directly from the emitter of Q_1 to the output terminal 6 of plug P_2 at 6 volts (V) p-p. The same video signal is fed from the emitter of Q_1 through R_{24} and C_{25} (high-pass filter) to L_4 and L_5 chroma peaker circuit. The chroma peaker is a band-pass filter that will pass only the frequency range of 2.1 to 4.1 MHz, which is the frequency band of the combined modulated I and modulated Q color signals. The chroma signal is output at terminal 7 of plug P_2 at 300 millivolts (mV) p-p.

Generally, only three signal waveshapes are associated with the video IF amplifiers: The luminance video output signal at terminal 6, the chroma output signal at terminal 7, and an input pulse voltage from the horizontal output transformer used to key the AGC circuit, seen at terminals 8 and 9 of plug P_2 as 40 $V_{p\text{-}p}$. The dc supply voltage is input at terminal 10 of plug P_2 at 22 V dc. The waveforms appear in Figure 14-1 in the upper-right corner.

The tuning devices are all coils shown along the bottom of Figure 14.1. Starting at the left side (input), these are L_{11}, T_2, L_{11}, L_{12}, L_{13}, T_3, T_4, and T_5. The coils are adjusted to shape the desired band-pass characteristics for this circuit design. Several of the coils are adjustable from the top and the bottom and will be attended to in the section on IF alignment.

14.2.1 Traps

Traps are used to eliminate a single frequency or at least a very narrow band of frequencies and are often called *notch filters*. A trap with a high Q will have a narrower bandwidth than one with a lower Q.

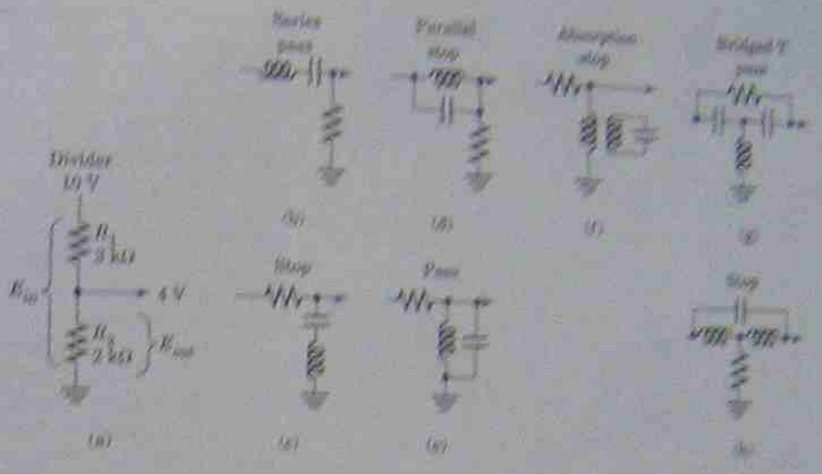
An understanding of the very basic voltage-divider rule will simplify the discussion on traps and the coupling methods, which are covered in the next section. In Figure 14.2a, the input voltage (10 V) is divided proportionately across the two resistors R_1 and R_2. The output voltage is the voltage that appears across R_2. The output voltage (E_{out}) = the value of R_2 times the input voltage, divided by the sum of $R_1 + R_2$. As shown, the output voltage (E_{out}) is (2 kΩ (kilohms) × 10 V) divided by (2 kΩ + 3 kΩ) = 4 V.

When R_1 is unchanged and R_2 increases to 5 kΩ, the output voltage for the same input is 6.25 V; do your own calculations. The input and output resistances of the circuit have changed from 5 and 2 kΩ to 8 and 5 kΩ, respectively. The same end result could have been achieved by holding R_2 at 2 kΩ and decreasing R_1 to 1.2 kΩ. Again, E_{out} = 6.25 V, with R_{in} now at 3.2 kΩ and R_{out} = 2 kΩ. The loading effects on the input voltage source have been changed.

With an ac input voltage, the same conditions exist in traps using inductors and capacitors (X_L and X_C) in place of the resistors. Since reactances change with frequency, the output voltage will also change with frequency.

Inductive reactance increases for an increase in frequency, while capacitive reactance decreases as the frequency goes up. Coupling these facts with the basic theory of resonant circuits, where X_L equals X_C, it is possible to describe some trap and coupling network behavior. The final point to remember is that in a series resonant circuit the voltages across the reactances are opposite in phase and cancel each other, leaving the circuit impedance low, typically the dc resistance of the coil, whereas, in a parallel resonant circuit, the reactances add vectorially to create a high impedance at resonance.

FIGURE 14.2
Traps, their circuit configurations and response to the resonant frequency.



The **series resonant** circuit of Figure 14.2b and c can be used as a pass or trap frequency circuit. At resonance and low impedance in series with the signal, Figure 14.2b passes the selected frequency the same as when R_1 is made small in the voltage divider, whereas the shunt configuration of the series trap in Figure 14.2c acts like a short circuit to ground for the signal at the resonant frequency.

The **parallel resonant** trap circuit of Figure 14.2d and e does exactly the opposite of the series resonant traps. In Figure 14.2d, the high impedance at resonance is like making R_1 of the voltage divider larger with a bigger voltage across it, leaving less voltage for the output across the equivalent of R_2. You might recognize L_1 and L_{10} of Figure 14.1 as this type of circuit. The shunt connected parallel resonant circuit of Figure 14.2e raises the output voltage at resonance as do L_2 and T_5 in Figure 14.1.

The **absorption** trap in Figure 14.2f acts like a double-edged sword. The output will resemble the Gaussian response curve of a typical parallel resonant circuit, but it has a suckout notch at the center resonant frequency due to the counter emf reflected back into the primary by the secondary at resonance. The secondary is floating and makes no connection with any other part of the circuit.

The **bridge T** circuit of Figure 14.2g and h has higher Q and narrower bandwidth, which suggest more care when tuning. For example, trying to find the highest point on a round ball would allow a reasonable variance from center before you would notice a change in height. However, finding the highest point on a vertically standing needle would allow less room for error. A small change in tuning of the bridged T will make a large change in the effectiveness of the trap. Look at T_2 and T_4 in Figure 14.1 for this type of trap circuit.

14.2.2 Coupling Circuits

The ac signal is coupled from one circuit to the next in one of four standard ways. The most common of these is seen in Figure 14.3a as **resistance-capacitance** (*RC*) coupling, which is used in the majority of low-frequency amplifier circuits. The effects of the ac signal at the collector of Q_1 are passed through the capacitor to the base of Q_2. The dc voltages of Q_1 are totally isolated from the dc base voltage of Q_2. The value of the coupling capacitor (C) affects the lowest frequency of the signal to be passed between the amplifiers. As a series impedance, C should be large for X_C to be small at low frequencies. The −3-dB point of the low-frequency response is reached at the frequency where $X_C = R$.

The best low-frequency response is achieved by eliminating the series reactance, as seen in the **direct-coupled circuit** of Figure 14.3b. Doing so allows a frequency response down to dc and saves the cost of the capacitor plus the labor to connect it into the circuit. However, it carries with it two distinct disadvantages: (1) The circuit is harder to troubleshoot because a defect in either transistor will change the dc voltages on the other transistor.

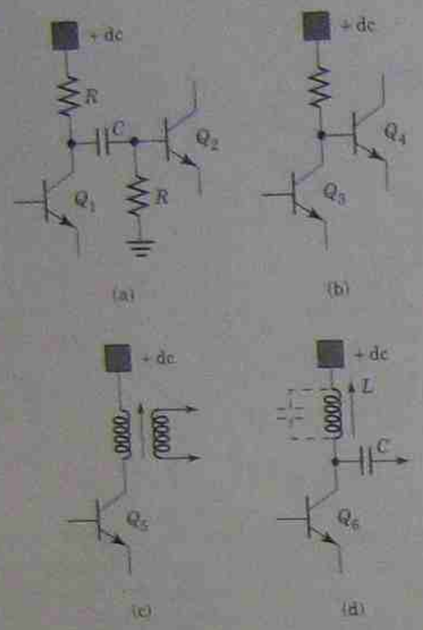


FIGURE 14.3
Four common coupling methods: (a) RC; (b) direct; (c) transformer; (d) impedance.

making it harder to pinpoint the problem. (2) When the collector dc voltage of Q_2 is one-half of V_{cc}, the base of Q_4 is also at the same dc voltage. Since the collector dc voltage of Q_4 must be higher than its base dc voltage, there is less available room for a large collector voltage swing, which limits the gain of Q_4. When several amplifiers are coupled in this fashion, you may see alternate PNP and NPN transistors used to avoid this voltage pileup. Again, direct coupling is common in low-frequency amplifiers.

The **transformer-coupled** amplifier of Figure 14.3c is the most common high-frequency tuned amplifier configuration. This circuit allows the ac signal to be transferred from the primary winding into the secondary without a direct dc connection. A capacitor may be found across either or both windings to complete the resonant circuit for tuning. At very high frequencies, the distributed capacity between the turns of coil wire is sufficient to make the coil self-resonant at some frequency. Tunable coupling transformers include a movable powdered iron core to vary the inductance and change the resonant frequency, as seen in all the frequency adjustments of Figure 14.1. At very low values of inductance, the turns of wire may be compressed or separated to change the tuning, as was discussed in the section on tuners.

The transformers in the video IF section will rarely all be tuned to a single center frequency. Tests have proved over the years that a relatively flat response can be maintained over a wide frequency range by a process called **staggered tuning.** An example is seen in Figure 14.4, which also shows a steeper rise and fall response (seen dashed) than any of the individual circuits alone. This added characteristic enhances the selectivity of the IF amplifiers.

Impedance coupling (Figure 14.3d) is used primarily in wideband amplifiers. The inductive reactance (X_L) replaces the load resistor (R_c). Since reactance increases at higher frequencies, the load impedance increases to provide more gain at higher frequencies. The upper limit is where the stray capacity forms a parallel resonant circuit with the inductance. Beyond this point, the gain drops rapidly.

14.2.3 Crystal and SAW Filters

Quartz crystal, as found in nature, exhibits a piezoelectric effect. That is, when mechanically distorted, a difference of potential can be measured across two opposite surfaces of the crystal. This effect can be carried one step further, in that the crystal will mechanically distort when a difference of potential is placed across two opposite surfaces. An ac voltage will warp the crystal first in one direction and then in the other direction, causing the crystal to mechanically oscillate. The frequency of oscillation is a function of the physical size of the crystal stock, with thickness being the major dimension. The low-frequency range seldom goes below 100 kilohertz (kHz) in communication crystals and rarely above 10 MHz. A crystal cut to operate

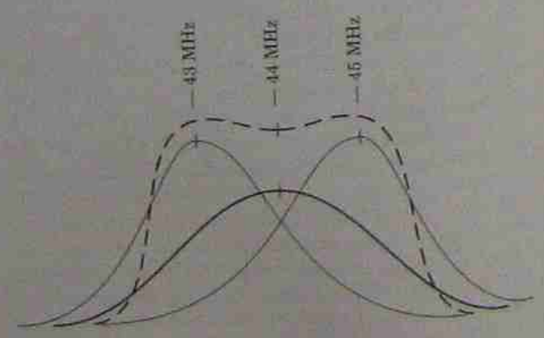


FIGURE 14.4
Staggered tuned video IF response curve.

above 10 MHz would be extremely thin and fragile. However, crystals may oscillate at multiples of their fundamental frequency and are then called **overtone** crystals. Electrically, the crystal has the characteristics of a series resonant circuit. The equivalent circuit is a series inductor, capacitor, and resistance with extremely high Q and narrow bandwidth. The mechanical mounting hardware, in effect, adds a capacitor in parallel with the crystal. This holder capacity forms a parallel resonant circuit with the inductance so that each crystal has two resonant frequencies: a series resonant frequency with very low impedance and a parallel resonant frequency, slightly higher in frequency, with very high impedance. Scientists have learned how to grow crystals in the laboratory where they can control the properties of the structure. They are vat dipped in the same way that candles are made. These are known as *ceramic* crystals and are the forerunners of today's integrated circuit wafers. A sample crystal filter is shown in Figure 14.5 as three separate crystals and then again as a single common crystal slice. In both cases, there is a crystal structure from the input (a) to ground (c), a crystal structure at the output from (b) to ground (c), and a crystal structure in series with the signal from the input (a) to the output (b). The response curve resembles that of the staggered tuned circuit, but with higher Q and steeper skirts.

The **surface acoustical wave (SAW) filter** of Figure 14.6 is the latest entry into the filter family. Input and output transducers are mounted on a highly polished substrate of thin-film zinc oxides

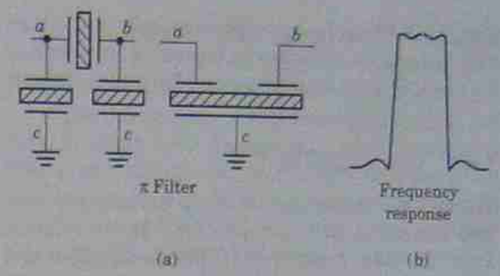
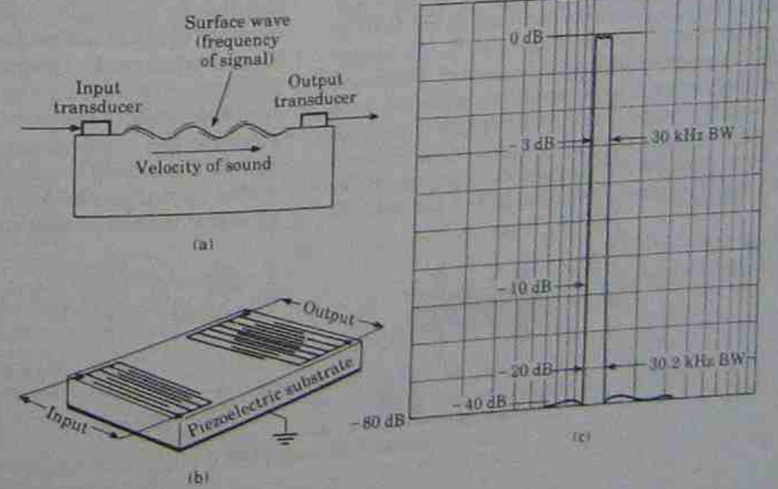


FIGURE 14.5
Crystal filters: (a) π filter with separate and combined crystal slices; (b) frequency response. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 91, Robert J. Schoenbeck, © 1992.)

with a ground plane on the opposite side of the substrate. The finger size, shape, and spacing of the transducers establish the frequency response of the filter. When a signal is applied to the input transducer, the surface of the substrate will ripple in a wave that moves across the substrate to the output transducer at the velocity of a sound wave in free air. It is from this action that the filter gets its name, surface acoustical wave. The SAW filter is generally placed at the input to the IF section, ahead of the amplifiers. One SAW filter replaces L_{11}, T_2, L_1, L_2, and T_5 in Figure 14.1, for instance. SAW filters are not adjustable. Seventy-five-ohm input and output impedances are common for television receivers, but other impedances are avail-

FIGURE 14.6
Surface acoustical wave (SAW) filter: (a) surface wave; (b) input–output transducers; (c) response curve. (Reprinted by permission of Prentice Hall, Upper Saddle River, N.J. From *Electronic Communications: Modulation and Transmission*, 2 ed., p. 91, Robert J. Schoenbeck, © 1992.)



able. SAW filters have the greatest selectivity; they will respond at 100% at one frequency and drop to 1% output signal for a very small frequency change.

14.3 VIDEO DETECTORS

The AM detectors used in radio are carried over into television as video detectors. In its original form, the video detector is a half-wave rectifier and filter. The frequency of the ac input signal and the value of the filter components are the only differences between the video detector and the low-voltage power supply circuits. Figure 14.7 shows that the ac input signal is converted to a dc output voltage. Changing the amplitude of the input voltage changes the dc output voltage. Therefore, an amplitude-modulated input signal is seen at the output as a changing dc voltage that corresponds to the shape of the input wave's modulated envelope. Examining the envelope of the modulated wave as it appears going into the detector, we see that the video detector is a frequency changer. It changes the high-frequency video IF carrier down to the low frequencies of the video signal. It is the second frequency changer in the television receiver. The mixer in the tuner, which changed the RF carrier signal to the intermediate-frequency carrier, is the first detector. The video detector is sometimes referred to as the second detector. Germanium crystal diodes are preferred here because of the low voltage drop across the germanium junction.

Generally, no dc voltage is applied to the diode detector circuit. Any dc voltage that appears across R_L in Figure 14.7 is the result of the rectified signal voltage. The polarity of the detector output voltage is determined by the direction in which the diode is wired into the circuit. In Figure 14.7, the output voltage is positive compared to ground. When the diode is reversed, the current flows in the opposite direction; the output voltage is negative compared to ground and the negative peaks of the modulated wave are detected. Either polarity is correct, under given circumstances. The direction of the diode is determined in each case by the number of phase reversals that the video signal encounters between the video detector circuit and the CRT.

Circuits that perform better than the simple diode detector have been known in the industry for a long time, but they were much more expensive. The disadvantages of the simple diode detector are the 0.3-V drop across the diode and the output distortion at low signal levels. The need for an input coupling transformer was looked on as another disadvantage. These disadvantages were considered to be minor in light of any other alternative circuits.

14.3.1 Synchronous Detection

Even as a separate microchip, the synchronous detector of Figure 14.8 was more expensive than the simple diode detector. It was not until large-scale integration became a reality that the synchronous detector became a practical circuit for video signal recovery.

From your study of single-sideband or suppressed carrier amplitude modulation, you may recall the operation of the product detector. A common product detector chip is the LM1496, in which the same circuit is used for balanced modulation and balanced demodulation. The difference between these two functions has to do with the input signals. The carrier and the signal that is to modulate the carrier are the two input signals for the balanced modulator. The output is an amplitude-modulated carrier for which you can balance out (cancel) the carrier to produce double-sideband suppressed carrier AM. If you change the input signals to be the modulated signal, the unmodulated carrier signals will again cancel the carrier and reproduce the original modulating signal (demodulation). As you examine the synchronous detector in Figure 14.8, you will find it to be the same circuit as the LM1496 product detector. The modulated carrier signal to the synchronous detector is the video IF signal. The second input signal must be an unmodulated carrier at 45.75 MHz. The modulated video IF signal is used to synchronize a 45.75-MHz oscillator that will supply only the carrier to be used for demodulation. The high Q and narrow-bandwidth resonant circuit in the carrier generator eliminate the sidebands and furnish the single carrier signal frequency. The recovered output signal of the synchronous detector may have positive or negative

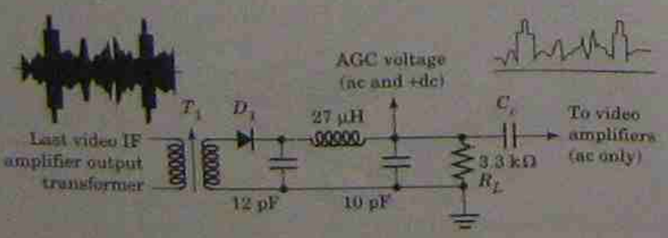


FIGURE 14.7
Diode video detector.

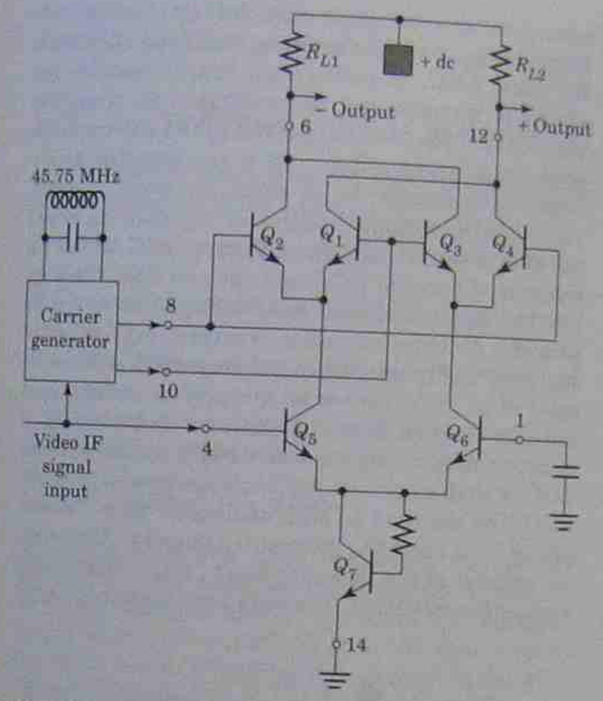


FIGURE 14.8
The circuit for a synchronous detector. The pin numbers are for the LM1496 product detector for comparison purposes only.

sync pulses, depending on which output terminal is used by the receiver manufacturer. Be prepared to see either polarity composite video output signal.

The advantages of synchronous detection are total freedom from distortion, even at low signal levels, and this detector will supply gain instead of losses. It is often possible to supply enough gain to eliminate one of the video IF amplifiers. A tuned circuit is still required, however.

14.4 KEYED (GATED) AGC

The output level of the AGC voltage is based on the strength of the composite video signal from the detector. Large video signals equate to higher AGC voltages, while smaller video signals mean less AGC voltage. However, the video signal from the detector is directly proportional (without AGC) to the signal strength at the antenna. The blanking and sync pulses are the only part of the video signal that is independent of the scene brightness. The horizontal sync and blanking levels were chosen to represent the video signal strength because of the timing relationship to the readily available horizontal output pulses from the flyback transformer. Figure 14.9a features a gated AGC amplifier circuit showing a composite video signal with positive sync pulses applied to the base. There is no full-time dc power supply voltages to the collector in this circuit. Instead, a positive pulse from the flyback transformer becomes the temporary voltage supply. When a positive flyback pulse appears at the collector and a positive blanking pulse appears at the base at the same time, the transistor will conduct and charge up capacitor C_2 in Figure 14.9. The

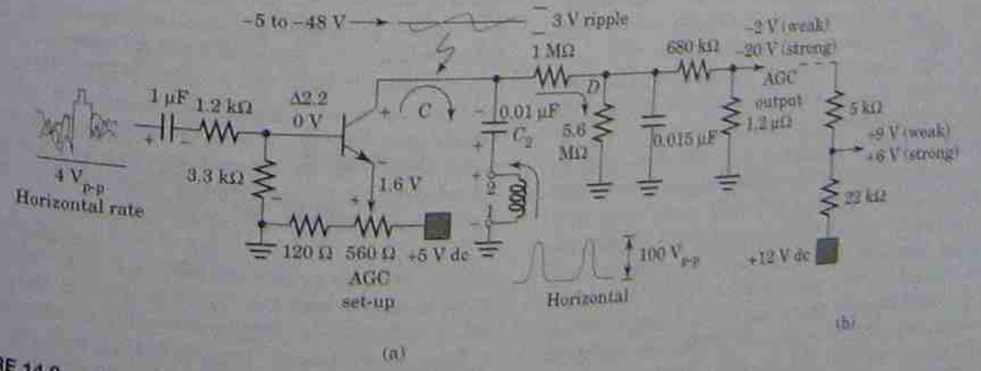


FIGURE 14.9
A sample of a discrete component gated AGC circuit: (a) negative AGC output; (b) one way to change polarity to positive AGC output.

charge path is denoted as C on the diagram. The polarities of the charge voltages are also noted in the figure, with C_1 negative toward the collector of the transistor. During the trace time, when both pulses are shown, the transistor becomes an open circuit. C_1 becomes the voltage source and discharges through the high resistance of the AGC filter denoted as R in the figure. The polarity of the 'AGC' voltage is negative compared to ground in this circuit.

Figure 14.10b shows one way that the polarity of the AGC may be altered from $-$ dc to $+$ dc. A dc-coupled common-emitter amplifier will do the same thing. The three variables that go into selecting the polarity of the AGC voltage are the polarity of the input video signal, choice of NPN or PNP transistors, and the polarity of the horizontal flyback pulse. The flyback pulse is reversed in Figure 14.9 by taking the signal from pin 1 and grounding pin 2 of the flyback transformer.

The gain of a transistor is a function of the collector current. A typical collector current–gain curve is given in Figure 14.10, which shows that as the collector current increases the gain also increases, to an optimum point (Q_2). Beyond optimum, further increases in collector current cause the gain to decrease. The actual operating point of the transistor may be anywhere along this curve. When an operating point is chosen by the manufacturer to be at Q_0, we can see that a more positive base voltage (for a PNP transistor) causes an increase in collector current and an increase in gain. An operating point at Q_1 indicates that a more positive base voltage (for a PNP transistor) would cause an increase in collector current and a decrease in gain. The change in base voltage is used here to mean a change in AGC voltage. The operating point Q_2 identifies **reverse AGC** and Q_1 means **forward AGC**. In both cases, there must be the ability to increase and decrease gain by changing the AGC voltage. A stronger voltage at the antenna produces a larger voltage out of the detector and a larger AGC voltage. In all cases, we want a large value of AGC voltage (positive or negative) to lower the gain of the IF amplifiers. Figure 14.11 shows an example of forward AGC and reverse AGC. In Figure 14.11a, an increased AGC voltage (-4 to -8 V) causes a decrease in emitter current (and collector current). In Figure 14.11b, an increased AGC voltage ($+4$ to $+8$ V) causes an increase in emitter and collector current. Don't be misled to believe that a negative AGC voltage automatically means reverse AGC or that a positive AGC voltage means forward AGC. The choice of an NPN transistor as an IF amplifier, or if the AGC voltage is applied to the emitter instead of the base as shown, could completely change the situation. The only sure statement we

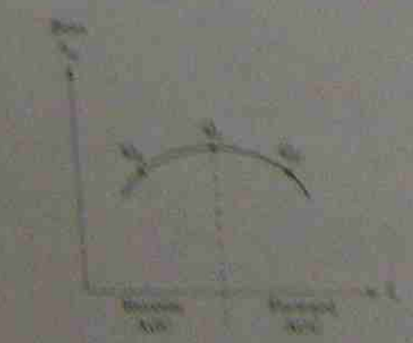


FIGURE 14.10
A complete gain control characteristic curve.

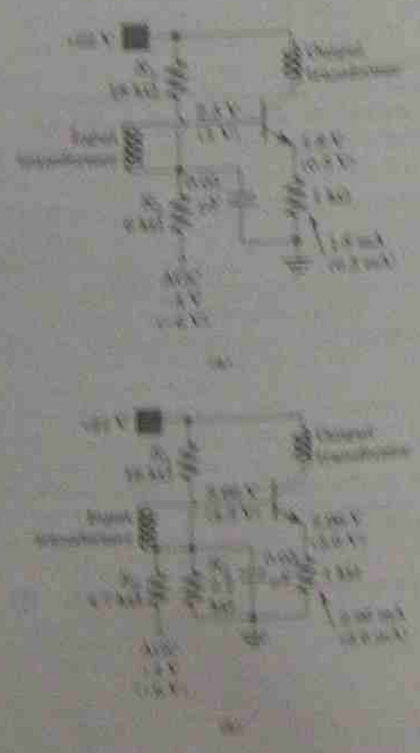


FIGURE 14.11
Examples of (a) reverse AGC, (b) forward AGC.

can make is that when the antenna signal gets stronger the AGC voltage should get numerically larger.

14.3 TESTING THE VIDEO IF AMPLIFIERS

The symptoms that indicate a defect in this section can be broken down as follows:

1. Clean bright raster, no picture, no snow, no sound
2. Clean bright raster, no picture, no snow, normal sound
3. Clean bright raster, weak picture, noise and sound
4. Negative picture out of sync, buzz in sound
5. Ghosts in picture, all channels

14.3.1 Testing the AGC

Assuming that you have diagnosed the picture symptoms, have made all the preliminary tests for dc supply voltages, and are confident that the problem is in the IF amplifiers, then the first place to look is the AGC voltage line. A fault in the AGC system can cause several of the above specified conditions (1 to 4). Without the correct AGC bias, the amplifiers will not work normally, or not at all. Find the AGC line. It is not given on the original manufacturer's schematic of Figure 14.1 nor is it identified in the circuit description section of the service manual. When you run across this situation, go directly to the alignment procedure where it tells you to remove the connector from plug J and attach a variable 0- to $+10$-V dc supply to pin 3 and ground. The voltage on the schematic reads 4.15 V dc at this point, which we know to be the AGC for maximum gain (no signal). You may want to adjust the voltage slightly higher so as to avoid a maximum gain situation and signal compression. If a picture appears on the CRT screen when the bias is touched, the trouble is in the AGC circuit. If a picture does not appear, you have at least set the AGC conditions for a normal picture. Always turn the receiver off and connect the ground side first when removing the bias supply. Many solid-state devices are sensitive to static shocks that destroy microcircuits.

When you are working with a discrete component AGC circuit, you can use the oscilloscope to look for the input video signal, the flyback pulse from the horizontal output transformer, and a ground connection. As the circuits become more functional in microchips, there will be fewer points that you can check. However, all AGC circuits will have a dc supply voltage, a horizontal pulse, and a ground connection. Make sure that these inputs are supplied before charging chips.

14.3.2 Testing the Amplifiers and Video Detector

Attach an external AGC bias supply even when you know that the AGC circuit is normal. This will ensure that you will have an output signal for any level of input signal that you use. Apply a test signal to the IF input.

On some receivers, there is an exposed screwdriver on the tuner called 'fine tune' or 'tuner.' This control provides a place to feed in a test signal (see Section 14.7). As a second choice, you can remove the IF input cable that comes from the tuner and apply the signal directly to the IF amplifiers (J in Figure 14.1). Observe the output after the video detector.

There are three test setup systems, which depend on the test equipment that is available. We will start with the simplest system.

With the receiver turned on and using an RF sine-wave signal generator, select a frequency at the center of the IF band pass (44 MHz is a common frequency). Apply this signal to the signal port (J) in Figure 14.1 at a very low signal voltage setting. Connect a dc voltmeter set for 5 or 10 V dc full scale to the output of the video detector, pin 10 of J3 in Figure 14.1. As you increase and decrease the input signal level, the dc output voltage should follow in step with your changes when the amplifiers are good. If the meter does not change, move the signal generator, now through a 0.002 microfarad (μF) capacitor, to pin 3 of J1 and repeat the input amplitude changes. Repeat the tests at pin 8, then pin 8, and then pin 11 of J1 until you are successful at changing the dc reading on the meter as you did at changing the dc reading on the meter as you change the amplitude of the input signal.

You will need a stronger signal at pin 11 than that required at pin 3. For example, pin 3 at 100 mV$_{p-p}$ pin 8 may be 0.65 V$_{p-p}$, and pin 8 may be 3 V$_{p-p}$. Unless the meter is on the last IF amplifier section, you will need an input point where the output will respond to your changing input voltage. You then know that the section between the two test points is working and the defect was in the previous section. For instance, when an input signal at pin 8 of J1 does not show an output change, but a signal at pin 8 does, you know that section J1A is defective. Be sure to check the dc voltages at all the pins associated with J1A before deciding to change the chip. J1 is a 16-pin dual in-line package and may be soldered into the PC board

Practice unsoldering these chips on a discarded board before working on a customer's receiver.

An easier testing method that gives more positive results is shown in Figure 14.12, but it requires slightly more sophisticated test equipment. The RF signal generator must be capable of internally or externally amplitude modulating the 44-MHz sine-wave carrier to 30%. The modulating signal is also a sine wave at either 400 Hz or 1 kHz. Generators that have an internal modulation feature are generally at 400 Hz and automatically amplitude modulate the carrier to 30%. You will need to observe or calculate the 30% modulation when using an externally modulated generator. Any low audio frequency may be used for this signal; 1 kHz is a popular choice.

Attach the external bias box to the AGC line as previously outlined. Apply the modulated carrier signal to the IF input jack J_1 at a low signal level, typically 100 $mV_{p\text{-}p}$. Use an oscilloscope to observe the recovered 1-kHz sine wave at the output of the video detector, pin 16 of $U1$, then at the base of Q_1, and finally at the output terminal 6 of plug 2. The block diagram of Figure 14.12a is a simplified version of Figure 14.1. If no signal is observed at the output, then use a demodulator probe, such as described in Figure 14.12b and progressively look at pin 11, then pin 9, then pin 6, and finally at pin 3 of $U1$.

When you have an oscilloscope that is capable of 50 MHz or higher frequency response, you may be able to observe the modulated signal directly without a demodulator probe at these test points. The vertical sensitivity of the oscilloscope will need to be good down to about 0.5 mV/cm.

14.6 LARGE-SCALE INTEGRATED CIRCUITS

You will have the opportunity to examine the full receiver block diagram and then the full schematic a little further on in this text. For now, the LSI chip circuit only is shown in Figure 14.13 along with its associated circuits and signals. The only real difference between this diagram and the one shown in Figure 14.1 is the concentration of the sections on a single chip and the addition of the digital controller. Let's examine these differences.

The output from the electronic tuner is fed to an IF preamplifier. The suffix *pre* means *before*. As used in electronics, a preamplifier signifies a very low signal level amplifier. The SAW filter that follows is used to tailor the frequency response of the

FIGURE 14.12
Video IF amplifier under test: (a) simplified block diagram with test points; (b) quadrupler detector probe

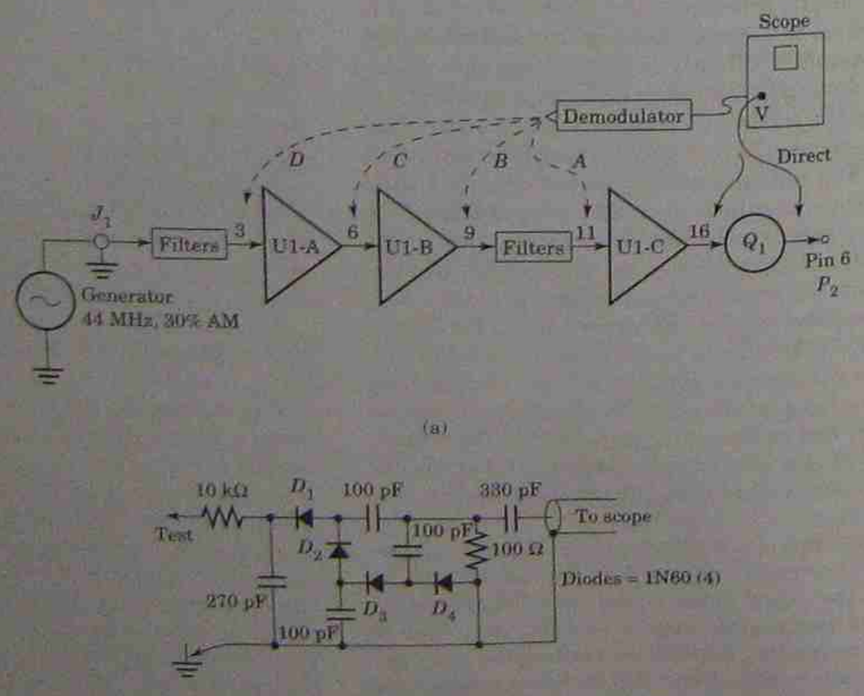
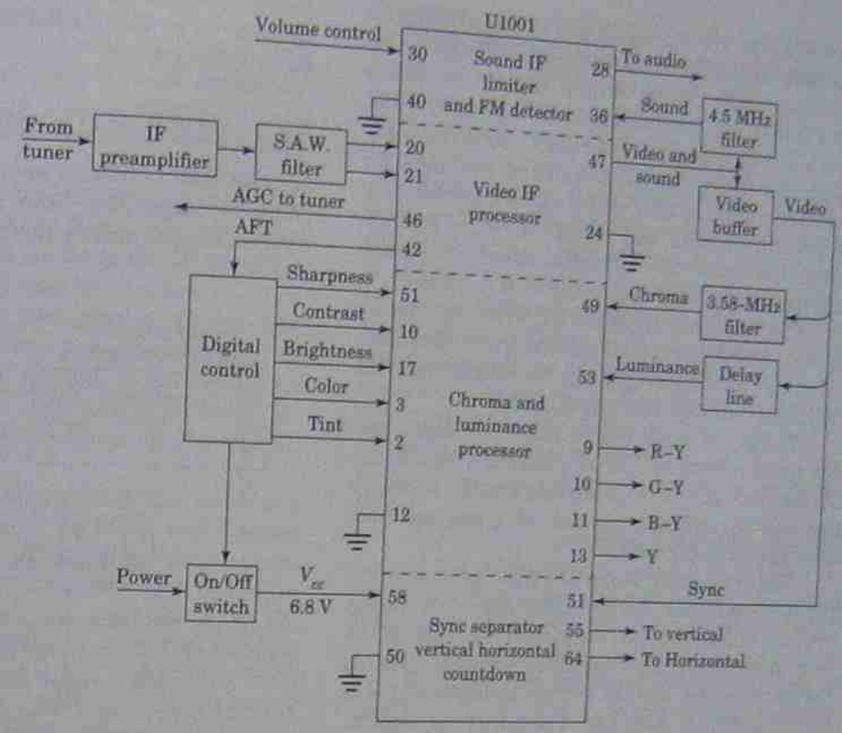


FIGURE 14.13
Partial block diagram of an RCA-CTC156 large-scale integrated circuit. (Courtesy Thompson Consumer Electronics.)



video IF section and supplies no gain. This SAW filter has a balanced output that is shown feeding into pins 20 and 21 of the video IF processor section. The term **processor** is normally associated with computer systems, but is used here to describe an analog system because it is the most modern term that fits the description of a multifunctional section. There are three output signals from this segment of the LSI. They are the tuner AGC output at pin 46, the AFT output at pin 42, and the composite picture and sound signal at pin 47. This last sentence provides you with a mountain of information. It tells you that this section contains the video IF amplifiers (probably two or more) and the video detector, because the pin 47 output signal is the 4.5-MHz sound carrier plus the composite video signal; it has the AGC section because it sends the tuner AGC out from pin 46, and it includes the AFT section with the output at pin 42.

As we examine the schematic diagram later you will see two tuned circuits connected to this section. One is labeled *Video Det. Tank* and the other *AFT tank*, so we can conclude that the video detector is a synchronous detector as described in the last section. All the other IF alignment coils have been replaced by the single SAW filter, so no IF alignment is ever needed.

The output signal from pin 47 that goes to a 4.5-MHz filter and a video buffer must contain all the luminance signal (30 Hz to 4.2 MHz), the chrominance signal (2.1 to 4.1 MHz), and the modulated sound carrier at 4.5 MHz. The signals are separated from each other by individual circuits external to the LSI.

The sound carrier passes through a crystal filter and back into pin 36 of the sound IF, limiter, and FM detector section. The limiter removes any amplitude changes that may have contaminated the frequency-modulated sound carrier; it is then demodulated and amplified for the audio output at pin 28. A dc control voltage applied to pin 30 adjusts the gain of the audio amplifier.

The video signal that comes out of pin 47 passes through a video buffer amplifier containing a 4.5-MHz crystal filter sound trap. If any of the 4.5-MHz sound carrier gets past this point, it could heterodyne with the 3.58-MHz color subcarrier and produce a 920-kHz interference pattern in the picture.

From the buffer amplifier, the 4.2-MHz bandlimited video signal is applied to the chrome bandpass filter for the color signal into pin 49. It also goes through the delay line for the luminance to pin 53 and then into pin 51 to the sync separator for pic-

ture lock. The chroma signal into pin 49 will find all the color recovery circuits discussed in Chapter 8 for receivers. They include several chroma amplifiers that feed the color demodulators, the color burst amplifiers to synchronize the color subcarrier oscillator, the subcarrier phase-shifting networks for color separation of the I and Q signals, the two balanced demodulators, and the matrix section that develops the three color difference signals. The color difference signals are output at pins 9, 10, and 11.

The delay line feeds pin 53, which has access to several luminance amplifiers where the gain (contrast) and the brightness (dc reinsertion) are controlled and then sent out at pin 13.

The R − Y signal (pin 9), the G − Y signal (pin 10), the B − Y signal (pin 11), and the Y-signal (pin 13) are then sent to the matrixing amplifiers, where they will be combined into the red, green, and blue color signals to the CRT.

The video input at pin 51 (called sync) will find the sync separator, the horizontal deflection oscillator, and the countdown circuits to the vertical deflection oscillator. The horizontal oscillator signal is fed out of pin 64, and the vertical oscillator signal is fed out of pin 55. This circuit is exactly the same as the countdown system described in Section 7.5.

The control signals fed into pins 30, 51, 10, 17, 3, and 2 are digitally developed dc voltages. You can override the controls by attaching an external variable dc bias box to either pin; then change the voltage to notice the effects on the picture for each function. Check the schematic first for voltage levels.

A switched dc supply voltage to pin 58 will turn the LSI, and the operation of the receiver on and off. The control section will remain on in a standby mode. Note, also, that there is a separate signal ground for each of the four major divisions of the LSI.

There is no difference between this LSI diagram and the equivalent parts of the Figure 12.1 block diagram. It is drawn differently, and the signal may go into and out of the same chip several times, but it has all the same basic circuits in the same basic sequence.

This has been a more detailed description, given in a write-up than can be derived from the block diagram in Figure 14.13 alone. For you to do this on your own, you *must* know the functional block diagram of a color television receiver from memory. The television manufacturer expects you to know this basic step. Armed with this tool, you then need to study the block diagram in the service manual and, finally, compare the block diagram to the complete circuit diagram. Prepare yourself now in order to be able to follow the diagrams and circuits in Chapter 15.

14.7 VIDEO IF ALIGNMENT

A great deal of time is spent designing and testing video IF amplifiers. They are extremely temperature stable and widely tolerant to replacement components. A weak amplifier will change only the gain of the circuit but will not affect the IF alignment. Even replacement coils are prealigned before sales and will often work correctly without further adjustments. Less than 1% of your adventures with IF amplifiers will suggest that you consider alignment as an alternative. The introduction of LSI circuits has reduced that number again by a factor of 10. When all other choices have been exhausted and the malfunction still points to the IF amplifiers as the culprit, alignment may be in order.

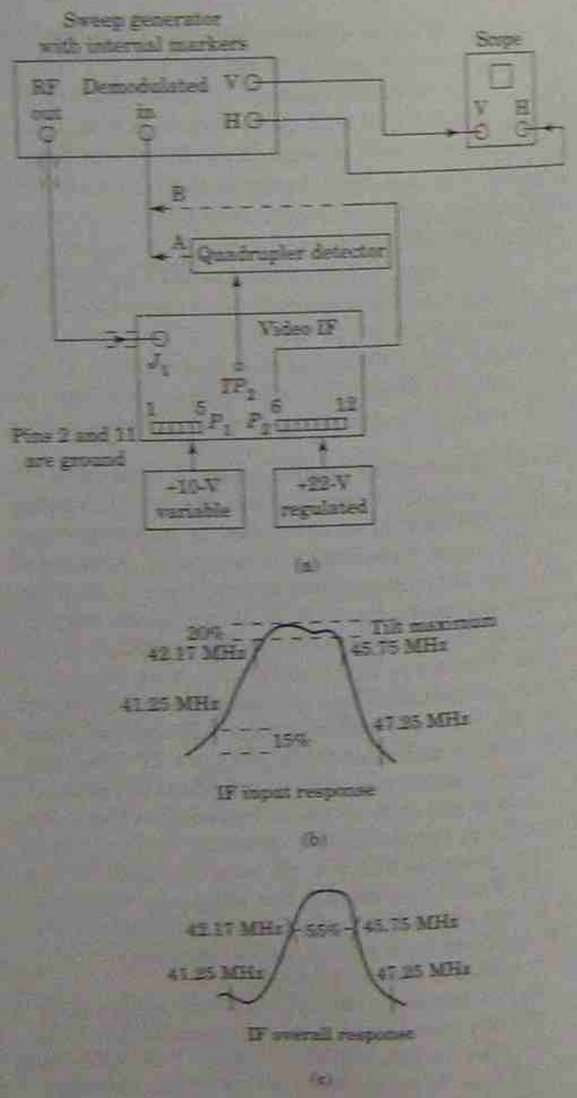


FIGURE 14.14
TV video IF amplifier section alignment setup: (a) equipment setup; (b) input section response curve; (c) overall IF response curve.

Figure 14.14 shows the setup for proper video IF sweep alignment. Find the procedure for IF alignment in the service manual of the receiver in question and follow the instructions exactly. The service procedure for the receiver in Figure 14.1 goes as follows.

A sweep generator is required that has a center frequency adjustable to 44 MHz and a sweep width of at least 10 MHz. That is, it will scan from 39 to 49 MHz at a 60-Hz rate. The sweep generator shall have crystal-controlled markers at 41.25, 42.17, 45.74, and 47.25 MHz. A +10-V dc variable voltage supply is connected to pin 5 of P_1 (AGC bus) and ground. A regulated +22-V dc supply (B+) is connected to terminal 10 of P_2 and ground. An oscilloscope is connected at the detector output (pin 16) of $U1$. The oscilloscope is turned to horizontal input and the vertical sensitivity is adjusted for 0.5 V/cm.

The sweep generator is first connected through the quadrupler demodulator probe, shown in Figure 14.12b, and then back into the demodulated input jack of the sweep generator. Set the RF generator output until you see a 2.5-$V_{p\text{-}p}$ pattern on the oscilloscope (through the quadrature demodulator probe), which equates to 100 $mV_{p\text{-}p}$ from the generator. Do *not* change the generator output signal level for the remainder of these tests.

Disconnect the sweep generator from the demodulator probe and apply the RF signal to the IF input jack J_1 of the amplifier under test. Connect the quadrupler detector between test point 2 (TP-2 in Figure 14-1) and the demodulated input signal connection of the sweep generator. This is shown as test point A in Figure 14.14. This will also allow you to align all the waveshaping networks in Figure 14-1 from the input J_1 to the input terminal (pin 3) of U1-A. The alignment procedure will describe how to adjust the input coils L_{10}, T_9, L_9, and L_8 to achieve the response curve shown in Figure 14.14b.

Remove the quadrupler probe altogether and connect the video output terminal 6 of P_2 to the demodulated input of the sweep generator (connection B in Figure 14.14). Adjust the dc bias supply (AGC) at pin 5 to display a 6-$V_{p\text{-}p}$ pattern on the scope.

The alignment procedure will tell you how to adjust L_7, T_8, T_6, and T_5 to achieve the response curve in Figure 14.14c.

As you can see, the equipment, the setup, and the procedure are not simple. You may need to go through the full alignment procedure a second time in order to obtain an ideal response curve. This should advise you to check the alignment only after you have exhausted all other possibilities, even though you are capable of this task.

QUESTIONS

14.1. Name the two main functions of the video IF amplifier section.

14.2. What range of frequencies is covered by the video IF amplifiers?

14.3. At what frequency is the video IF picture carrier?

14.4. At what frequency is the video IF sound carrier?

14.5. The sound carrier takeoff circuit may be tuned to what frequencies?

14.6. The video detector is
(a) an AM detector,
(b) an FM detector,
(c) an SSB detector,
(d) a quadrature detector.

14.7. The sync pulses out of the video detector are
(a) positive pulses,
(b) negative pulses,
(c) not a standard positive or negative pulse.

14.8. What other name is used to identify the video detector?
(a) AM detector,
(b) second detector,
(c) peak envelope detector,
(d) synchronous detector,
(e) all of the above

14.9. What part of the composite video signal will not change with scene brightness?

14.10. The gated AGC amplifier conducts during the (a) trace time or (b) retrace time of the horizontal cycle.

14.11. Name the input signal(s) to the gated AGC amplifier.

14.12. How will the AGC voltage change when the antenna signal gets stronger?

14.13. A low value of AGC voltage represents (a) maximum gain or (b) minimum gain of the IF amplifiers.

14.14. The polarity of the AGC voltage (+dc or −dc) will identify forward or reverse AGC.
(a) true,
(b) false

14.15. The AGC voltage is always applied to the first video IF amplifier.
(a) true,
(b) false

14.16. How does the tuner AGC differ from the video IF AGC?

14.17. Delayed AGC refers to a
(a) phase delay,
(b) time delay,
(c) level delay,
(d) frequency delay.

14.18. Give two reasons why it is advisable to use an AGC bias box when testing the video IF amplifiers.

14.19. Where in the service manual will you find the AGC point and voltage when the AGC line is not identified on the schematic?

14.20. What is the function of a SAW filter?

14.21. What are the advantages of a synchronous detector?

14.22. What is the function of the video IF section traps?

14.23. What can cause the 920-kHz pattern in the picture?

14.24. What should be the first apparatus that you connect to the circuit when testing the video IF amplifiers?

14.25. What is the absolutely last procedure you should consider when testing the video IF amplifier section?

15 Receiver Troubleshooting

15.1 INTRODUCTION

The text to this point has been devoted to the individual subsections of the television receiver. It was a discussion on what is required from each section and the theory of how the typical circuits worked. There was no coverage of the interaction between sections. Chapter 15 is written around a full television receiver that describes troubleshooting by sight and sound. Analyzing what you see on the CRT face and what you hear from the speaker will help you to isolate the defective section. You will carry this information to a full-size circuit schematic where you will examine the signal waveforms and dc voltages in the suspect section to help you locate the defective component.

However, the measure of your success will depend on how safely you handle yourself. Some electric shocks can be lethal and all are unpleasant. Repeated uncomfortable experiences like this could turn you away from an otherwise enjoyable occupation.

15.2 SAFETY

All electronic circuits operate on direct current (dc). Except for portable equipment, this dc voltage is derived from the 120-V ac power line. One wire of the 120-V ac line is connected (somewhere in your building) to a cold-water pipe ground. The other wire is electrically 120 V rms away from the ground. This voltage is fed through the power cord, safety fuse, on–off power switch, to the primary winding of the power transformer. Do *not*, for any reason, defeat the purpose of the safety fuse. A fire hazard exists when a larger fuse is used or when the fuse holder is bypassed.

It is essential to note that the secondary system of the power transformer is totally isolated from the primary winding. The secondary circuits are free floating, like the circuit of a flashlight. The batteries, case, switch, and bulb of the flashlight form a complete circuit with no reference to any other point in the universe. There is a common connection between all the circuits in the television receiver that we call *chassis ground*, but it too is part of the floating secondary system. When you attach the chassis ground to the common connection of your test equipment, the chassis ground becomes common to the entire test setup. The point is that the power transformer is a safety feature to separate the television receiver from the 120-V ac power line.

15.2.1 Isolation Transformers

The power transformer is large, bulky, and expensive. Space, weight, and costs are reduced by doing away with power transformers. Solid-state television products require voltages less than 120 V dc, and there are several ways to lower the voltage without a step-down transformer. However, without the transformer, the safety feature of isolation from the ac line is also lost. When your receiver does not have a power transformer, which you can easily verify by sight, then an **isolation transformer** is an absolute requirement. The isolation transformer has a 1:1 turns ratio so that no voltage

is lost, and it will protect you and your test equipment from severe damage. It is a good idea to use an isolation transformer even when your set has a power transformer. This practice will help you to establish good safety habits.

15.2.2 Leakage Current Hot Tests

When service is completed and the receiver is closed up with the back cover in place, a leakage current test should be conducted. Do not use an isolation transformer for this test. Plug the ac line cord of the receiver directly into the 120-V ac outlet and turn on the power switch. Using a dc current meter with the negative side attached to a known earth ground (cold water pipe, conduit, etc.), use the positive lead of the meter to measure the current at all the exposed metal parts of the receiver, that is, the antenna terminals, handle brackets, metal cabinet parts, screwheads, metal overlays, control shafts, or any other metal that may have a current path to chassis ground. *All* current measurements must be less than 0.5 milliamperes (mA). With the line cord plugged in, turn the set off and repeat the measurements. Reverse the line cord in the socket and repeat both tests one more time. Any current measurements that exceed this limit indicate a potential shock hazard and should be corrected before returning the receiver to the customer.

15.2.3 High-voltage Measurements

The second anode voltage of the CRT (high voltage) and the focus voltage are commonly in the thousands of volts. A special high-voltage meter or high-voltage attachment to a standard meter is the recommended tool for this task. A typical high-voltage tester has a 999-megohm (MΩ) resistor inside the probe. At the meter end, a voltmeter with a zero to 50-V dc scale is placed across a 1-MΩ resistor to ground. This combination forms a 1000 : 1 voltage divider so that the meter reads directly in kilovolts (kV). The probe is made long (8 to 12 in.) and sometimes has an irregular surface so that the high voltage will not ionize the air along the probe surface and cause an arc path to the meter, or ground, or hand of the user. Using a high-voltage probe (or meter) is the only recommended way to test these high potentials.

If you are unfortunate enough to make contact with the 120-V ac power line, the ac will prevent you from releasing your grip from the shock point until the 30-ampere (A) circuit breaker drops out. This calculates to $E \times I = 3600$ watts (W) of shock power.

The CRT with its three electron guns is limited to about 1.8 mA per gun, or 5.4 mA total. At 30 kV, this is about 162 W of shock power. The point is that no electric shock is pleasant and that, although the high voltage is much higher than the power line voltage, the power line is the more dangerous of the two. Treat all voltages with respect.

15.2.4 Handling CRTs

The cathode ray tube is a highly evacuated glass bulb. When fractured, the outside air pressure forces the broken glass inward, past the center, to scatter in all directions. The glass envelope is thick and strong. It will tolerate a fair amount of abuse, but it can be broken. The weakest point of the CRT is where the neck joins the bell area of the tube; therefore, *never* carry a CRT by the neck. Always carry it with two hands and with the face downward. Wear safety glasses with side protection when handling CRTs.

15.3 TROUBLESHOOTING OUTLINE

Three points are essential to troubleshooting television receivers and cannot be repeated too many times:

1. Listen to the customer's complaint about the problem.
2. Memorize the block diagram of a color television receiver.
3. Formulate a flow chart plan to analyze the trouble symptoms.

Always listen to the original complaint about the television. Customers may want something fixed that cannot be fixed, or they may want something fixed that you did not see. Good customer relations always starts and ends with a discussion of what needs repairing.

You begin to apply your knowledge when you turn on the television receiver and start a series of "do you have" tests. The "do you have" tests are mental observations by sight and sound that help you to decide if there is a circuit defect. You then decide which circuits should be eliminated as a possible source of the trouble or which circuits are the most likely to cause the defect.

You need to know what the product is intended to do (a television receiver in this case) and have a general idea of how it performs these tasks. In other words, you need to know the block diagram of a typical color television receiver. This will help you to isolate the trouble section by ruling out the sections that you observe to be working normally. Figure 15.1 is a review of such a detailed block diagram.

Next, you need a consistent plan of attack. A very popular, but not the only, plan is outlined in Figure 15.2 in the form of a flow chart. As you sharpen your skills, you will generate your own plan of examination, which may be similar to this one. We will use three visual aids to help us isolate the defect conditions that follow.

The block diagram of Figure 15.1, the flow chart in Figure 15.2, and the picture guide to television troubleshooting series.*

15.3.1 No Raster

Some receivers have the CRT heaters permanently connected to power so that as soon as the power switch is activated a raster appears; others require warm-up time. A **no raster** condition is seen in photo 1 of the picture guide series. During the warm-up time, make sure that the brightness and contrast controls are set to maximum and look for other signs of life. Almost all receivers have either an illuminated channel number readout or a pilot light to indicate an *on* condition. Wait for not more than 1 minute for the raster to appear. Turn up the volume control and listen for any sounds from the speakers. You now have enough information to start making decisions.

15.3.2 No Raster, No Sound, No ON Condition

At test 1 on the flow chart, "Do you have a raster?", the answer will be *no*. This heads in the direction of test 2A, "Do you have sound?" Sound will be anything from program material to static noise. A *no* answer here leads you to trouble area A, the low-voltage power supply circuit, which is common to all the circuits in the receiver. If the power supply does not work, none of the other circuits will work either. See Section 15.5.3 for servicing power supply circuits.

15.3.3 No Raster, Normal Sound

Look at the block diagram first. The sound signal is received at the antenna and passes through the tuner and video IF amplifiers to the sound takeoff point. The sound then goes through the complete sound section to the speaker. All these circuits are working properly. The video signal may also be passed through the luminance circuits to the picture tube; but without a raster, there is no way to display the picture. Turn the brightness control up to maximum (full clockwise) and look for a second brightness control. Most monitors and many television receivers have a second brightness control called the *Brightness range* or *Subbrightness*.

From the flow chart in Figure 15.2, a *no* response from test 1 (Do you have a raster?) will lead you to test 2A. A *yes* response to the sound test tells you to check the horizontal deflection and high voltage. Scope several points in the horizontal section and measure the high voltage with a high-voltage meter. You will generally find one of these circuits nonoperational, and you have isolated the problem in trouble area B. Advance to Section 15.5.2 for a full description on how to service the horizontal and high-voltage sections.

However, if you have high voltage, with a *yes* response to test 3A and a *no* response to test 4A, "Do you have brightness?", then go to the base of the CRT and measure the dc voltages that operate the CRT, trouble area C. Trouble area C includes the picture tube. Make sure that the CRT heaters are working. When all the voltages are found to be correct, test the CRT to see if it needs to be replaced. Section 15.5.4 covers the step-by-step testing of the CRT circuits.

We will leave the A section testing until we start the quality testing, because if you had a *yes* response to test 4A, then you would not have had a *no* response to test 1.

15.3.4 Good Raster

A *yes* response to test 1 is seen in photos 2 and 3 of the troubleshooting picture guide series for two different conditions. We will start with photo 2, raster with no snow. A *yes* answer to test 1 directs you to two parallel paths of inquiry. "Do you have sound?" (test 2) and "Do you have picture?" (test 3). It is important to note the duality of the sound test, when you have a raster and when you do not have a raster. With only a small amount of practice, you will soon see how testing for sound under both

*This series of pictures appears as a color insert in the text. The photo numbers in the following text refer to these pictures.

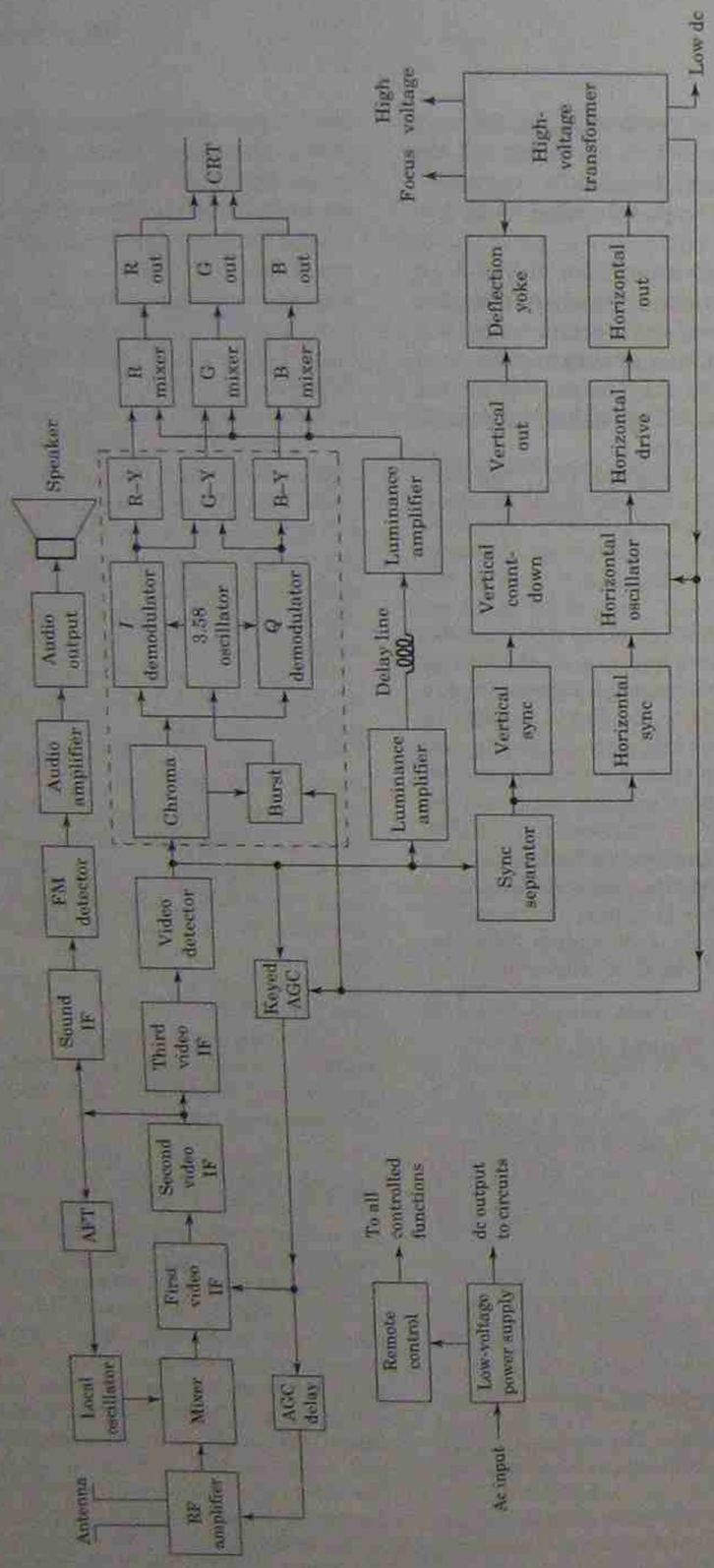
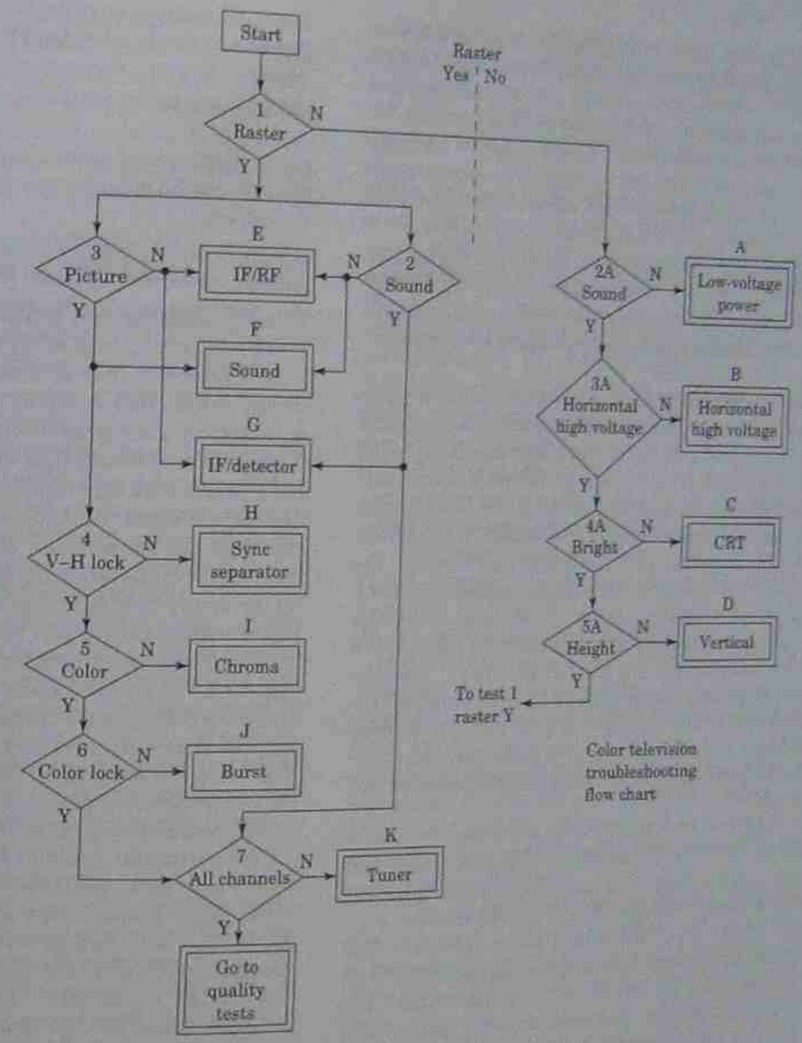


FIGURE 15.1
Detailed block diagram of a typical color television receiver with remote control.

FIGURE 15.2
Color television troubleshooting flow chart.



Color television troubleshooting flow chart

raster conditions will speed your search for the faulty section. It is used to divide your search between the power supply and the signal circuits.

Raster with No Picture, No Sound, No Snow. A *no* response to test 2 (sound) and a *no* response to test 3 (picture) of the flow chart tell you to look at the RF and IF for this defect, trouble area E. A sample is seen in photo 2 of the troubleshooting series. Comparing these findings to the block diagram, you can see that the picture and sound are together through the tuner and the first two video IF amplifiers only. Therefore, the problem must be in the circuits that are common to both signals. The AGC could be defective and be holding the first video IF amplifier in a cutoff condition, but this is the same general area and would be found when troubleshooting the circuits. Try applying an AGC bias voltage to the video IF section to further isolate this problem. Sections 15.5.8 and 15.5.9 describe the servicing techniques for troubleshooting the RF and video IF amplifier circuits.

Raster with Heavy Snow, No Picture, No Sound. Photo 3 of the troubleshooting series shows the presence of snow with no picture. It was said earlier that the mixer is the noise generator, and when the noise reaches the CRT, all the circuits between the mixer and the CRT (video wise) must be working well enough to pass this noise signal. The

search area then is before the mixer amplifier, which would be the RF amplifier and the antenna, trouble area E again. It may be possible to eliminate the antenna as a cause of this problem because even a broken wire on the antenna lead will give you a weak but snowy picture, as seen in photo 49. But check the antenna anyway. Many service technicians carry a small portable TV receiver as part of their test equipment. Connect a working receiver to the suspected antenna to isolate a defective antenna from a defective receiver and examine Section 15.5.9 for RF troubleshooting techniques.

Good Picture, No Sound. Look at the flow chart and the block diagram to examine this condition. Both of these aids will direct you to check the sound circuits. This problem will be found at some place after the sound is separated from the video signal. The sound circuits include the sound IF amplifiers, the FM detector, and the audio amplifiers to the speaker. A defect in the remote control of the volume (including the mute function) could also cause this type of problem. The flow chart for good picture but no sound will identify trouble area F. See Section 15.5.10 to troubleshoot the sound circuits. Photos 5 and 6 are examples of good pictures for color or black and white. There is no example in the troubleshooting picture guide section for good or bad sound.

Raster with No Picture but Good Sound. From a visual point of view, you are back at photo 2, a clean white raster with no snow. You will have to imagine normal program sound. Figure 15.2, the flow chart, shows that a *yes* response for sound and a *no* response for picture tells you to check the third video IF amplifier and video detector, trouble area G. The block diagram in Figure 15.1 suggests the same circuits could be at fault. Look at Figure 15.1 again carefully. After the video detector, the signal goes to the chroma amplifiers, the luminance amplifiers, the AGC circuits, and the picture sync separator. If the chroma circuits were at fault, the luminance signal would still get to the CRT for a black and white picture; see photo 6. If the luminance circuits are defective, the color video would still get to the CRT, as seen in photo 23. A defective sync separator would show the picture torn and rolling, as seen in photo 17, and a fault in the AGC circuit would kill the sound as well as the picture. In each of these cases, some manner of picture would arrive at the CRT. Since there is no picture at all, these circuits cannot be the fault areas. When all of these circuits are working, the problem must be in the third video IF amplifier or the video detector circuit. Section 15.5.8 describes how to troubleshoot these circuits.

Good Picture and Good Sound. A *yes* answer to tests 2 and 3 tells you to advance to test 4 in the flow chart.

15.3.5 Loss of Picture Synchronization

Of the remaining two picture functions, color and synchronization, loss of picture sync will be the most noticeable. We will examine three separate conditions in this category. Loss of vertical hold only (picture rolling up or down at any rate), photo 15; loss of horizontal hold only (picture slanted to right or left with any number of lines), photo 16; or loss of all synchronization (picture slanted and rolling at the same time), photo 17. The flow chart indicates trouble area H, sync circuits, which are all inclusive. The block diagram shows a sync separator, a separate vertical sync section, and a separate horizontal sync section. Use the oscilloscope to look for a video signal going into the sync separator and the sync signals coming out of the sync separator. No sync output is characterized in photo 17. The vertical sync section may be an amplifier or a simple integrating filter (low pass), where a defect would result in a picture display as seen in photo 15. No horizontal sync out of the horizontal section, which may be an amplifier or a differentiator (high pass) filter, would result in the conditions seen in photo 16. These signals can all be seen on the oscilloscope, which will help to isolate the defect for the individual conditions. Troubleshooting Section 15.5.5 outlines the full test procedure for these circuits.

A slowly rolling picture (vertical) or a few slanted lines (horizontal) mean that the sync signal is not getting to the deflection oscillator to lock it on frequency and indicate a defect in the sync circuits. A fast rolling picture (vertical) or many slanted horizontal lines mean that the respective oscillator is too far off frequency and outside the capture range of the sync signal. This is generally caused by a defective frequency-determining component in the oscillator circuit.

15.3.6 Color

Having passed tests 2, 3, and 4 of the flow chart successfully with a *yes* answer, test 5 asks, "Do you have color?" Remember that the "do you have" tests

are used only to identify which circuits of the receiver should be looked at and which circuits do not need attention. They ask nothing about quality. Test 5 asks you to check for the presence of any color in the picture. When there is no color, as seen in photo 6, then the chroma section, outlined by the dashed lines in Figure 15.1, are defective in some way, trouble area I.

The block diagram of Figure 15.1 is more specific in this matter. The circuits that affect all color are the chroma amplifier, the burst amplifier, and the 3.58-MHz color subcarrier oscillator. The signals in these three circuits can be examined with an oscilloscope for waveshape and amplitude as found on the schematic diagram.

The remaining circuits in the chroma section will react differently to the three primary colors (red, green, and blue) and produce some color on the CRT and are thus omitted when the defect causes a total loss of color in the picture. The full chroma testing is covered in Section 15.5.7.

Another possibility here is the fine tuning control in the tuner. It is possible to adjust the fine tuning to pass the station picture carrier for a normal black and white picture but not pass enough of the sideband with sufficient amplitude to activate the chroma section. When this happens, the sound level will also be reduced, but this is rarely detected because the volume control is unconsciously turned up to compensate for the losses.

This is an ideal time to jump ahead to test 7 of the flow chart to see if this no-color condition exists on all channels or just on the one channel. When the no-color problem is associated with only one channel, the fine tuning control is probably misadjusted. When the problem is the same on all channels, the no-color problem will be found in the three chroma circuits mentioned before, the chroma amplifier, burst amplifier, or color subcarrier oscillator.

On receivers that have a manually adjustable fine tuning control, turn the fine tuning control until sound bars appear in the picture, as seen in photo 29. Then reverse the direction of tuning until the sound bars just disappear. This setting will give you the best color picture and sound combination. Sound bars are dark horizontal shaded areas that appear in the picture when the performer is speaking and vanish when the performer stops speaking. Turn the volume control up so that you can hear the sound while watching the picture.

On television receivers that are fully automatic with digitally controlled electronic tuners and/or are remote controlled, you will need to measure the voltage on the tuning control line (AFT) for that specific channel. A channel-by-channel voltage chart can be found in the service manual.

15.3.7 Color Lock

When you have a *yes* response to test 5 of the flow chart, carry this information over to the block diagram to see that the chroma amplifier, the two demodulators, the three color difference amplifiers (R −Y, G − Y, and B −Y), the three color mixer amplifiers, and the three color output amplifiers are all working OK. The 3.58-MHz color subcarrier oscillator must be working in order to reinsert the carrier signal at the two demodulators, but it is at the wrong frequency, as seen in photo 35. The cause for this condition is that one of the frequency-determining components in the 3.58-MHz oscillator circuit has failed or changed value with age.

A *no* response to test 6 for color lock, trouble area J, suggests that the color burst amplifier may be defective, or the horizontal pulse, which gates the amplifier on, may be distorted or missing.

In later-model television receivers, the 3.58-MHz color subcarrier oscillator will stop oscillating when the color burst signal fails to reach the oscillator. This is a practical way to turn off the color circuits during a black and white transmission to prevent the noise of the color amplifiers, called *confetti*, from appearing on the screen as colored dots (photo 30). The burst signal is not included in the monochrome video signal.

It is reasonable to assume that a defect in trouble area J, the burst amplifier, will cause loss of color sync in some cases and total loss of color in other cases. Section 15.5.7 covers these test procedures.

15.3.8 All Channels

When you have a raster with a locked-in color picture and sound, you need to assess the reception on all channels that the television is capable of receiving.

When the reception is not the same for all channels, trouble area K, the tuner, and sometimes the antenna are the sections that need to be inspected. Defects in this general area are difficult to isolate when using the customer's antenna and possibly defective receiver. Always use a known-good all-band antenna for this test. The higher-numbered and higher-frequency channels will perform poorer with a low-grade antenna or with a poorly performing tuner.

A weak and snowy picture, as seen in photo 49, can often be isolated to antenna problems at the higher frequencies. Ghosts, as seen in photo 50, when found on only one channel or a few closely related channels, are generally the result of a poorly orientated antenna.

A defective tuner will often stop working at the higher channels, but perform normally at the lower channels, as described in Section 15.5.9 for RF testing.

15.4 QUALITY

You may have noticed that it would be difficult to separate a "do you have" set of tests from what could be called quality tests. The procedure was outlined in order to establish a line of thinking, and that is the main intent of this text, to help you to develop a logical thinking process.

For instance, when you turn on the television and the raster first appears, your eyes and your mind will immediately judge the height and width of the raster, as well as its color and brightness level. If a picture also appears, there will be a number of other characteristics that you will also see. Since it would be impossible to predict which defect will occur and since we can only discuss one condition at a time, the following section will examine each of the photos in the picture guide series. Here we can describe what kind of a defect the picture represents and what sections of the television receiver or computer monitor could cause that defect.

You turn on the set and have one bright line horizontally across the face of the CRT, as seen in the picture guide photo 7. Do you have a raster? Well, yes you do have a raster, but you also have a problem with the raster. You can say that the low-voltage power supply is working, the horizontal deflection and high-voltage circuits are working, and the CRT with its bias circuits is working. You simply do not have vertical deflection. Without a complete raster, further tests must be put on hold until the vertical deflection is restored. No vertical deflection can only be caused by a complete failure in the vertical oscillator, the vertical output amplifiers, or the vertical coils of the deflection yoke. However, many television receivers have a service-normal switch on the back of the cabinet. This switch, when in the service position, will kill the vertical deflection and is used to make some of the initial setup adjustments. When the switch has an IN/OUT action, the IN position is for normal operation and the OUT position is the service position. Make sure this switch is in the normal position. Section 15.5.1 gives a complete outline for servicing the vertical deflection circuits. Do this repair before continuing with the flow chart tests.

Photo 8 is another vertical deflection problem that must be cleared up before completing the flow chart tests. The circuit defect that caused the condition of photo 8 is an open yoke coil where the two halves of the vertical yoke are in parallel. In Chapters 3 and 4, you learned that the deflection yoke has a vertical section and a horizontal section. Each half of the yoke is made up of two coils. In the vertical half, the two coils are placed on the left and right sides of the CRT neck. These coils may be connected in series or in parallel with each other, depending on the design of the circuit. The same is true for the two horizontal coils of the deflection yoke, except that the coils are on the top and bottom of the CRT neck. In many receivers, an open coil in a parallel yoke would cause vertical keystoning, similar to the horizontal keystone in photo 11 (except vertically). The receiver used for these photos did not produce the keystone as expected, but rather broke into oscillation of the vertical output amplifier due to an improper load impedance for the vertical output amplifier. The frequency of oscillation is about 150 kilohertz (kHz). Series-connected vertical yokes, as found in the service schematic to follow, would display no vertical deflection like that of photo 7 when one-half of the yoke is open.

Horizontal keystone, as seen in photo 11, also caused by an open coil in a parallel-connected horizontal yoke, would require repair before continuing on with the quality testing. See Section 15.5.1 for testing and repair of the vertical deflection circuits and Section 15.5.2 for testing and repair of the horizontal deflection circuits.

15.4.1 Raster Size

The size of the raster will also be one of the observations noted in the initial examination. A short raster is seen in photo 9 as not enough vertical deflection to fill the CRT face from top to bottom. You may see nonlinearity and vertical foldover like that shown in photo 10. You should first try to adjust the vertical size (height) and vertical linearity controls to remedy these conditions.

The raster is too short when there is not enough signal to fully drive the deflection yoke. The vertical oscillator may have a weak output signal or the vertical output amplifier may not have enough gain to supply the yoke with the required current. Small size in either the vertical or horizontal direction is generally due to low gain in the output amplifier.

The raster may be too narrow, as seen in photo 12, or have white vertical lines (ringing in the yoke) similar to those seen in photo 13. These two photos suggest a defect in the horizontal deflection section. Low gain is generally caused by a weak output amplifier, whereas the distortion shown in photo 13 is often the result of low dc voltage to the horizontal output, which will include the boosted B+ supply, or a failure in the damping circuit.

You may detect a small raster for the size of the CRT as seen in photo 14, with a dark border at the top, bottom, and both sides of the raster. A small raster in both directions can generally be traced to decreased output voltage from the low-voltage power supply.

When you have a full-sized raster, look for color contamination as seen in photo 4, called color purity. Photo 4 is an exaggerated case of color contamination, but shows that any variation from a pure white raster will need attention. Discoloration of the raster like that seen in photo 4 is due to the shadow mask being magnetized. The shadow mask will be gradually magnetized by the constant bombardment of the negative electrons in the beam current. A magnetized shadow mask will deflect each electron beam in a random fashion such that the beam will pass through the shadow mask out of alignment from its intended phosphor color dots at different areas across the face of the CRT. Stereo speakers placed on top of or alongside the CRT will also magnetize the CRT. However, small amounts of magnetism will be neutralized by the degaussing coil during the first few seconds that the set is turned on. The internal degaussing coil is placed around the outside of the CRT at the face end of the tube and is electrically part of the low-voltage power supply circuit. See Section 1.5.5 for the original description of degaussing, and Section 15.5.3, power supply testing, for circuit repairs.

In extreme cases, you may choose to manually degause the CRT. Figure 1.10 shows the degaussing coil action and procedure. Place the degaussing coil parallel to and a few inches away from the face of the CRT. Turn the coil power on and move the coil in any pattern around the face of the CRT that will cover the full face area. After about 1 minute, move the coil (still in a parallel plane) away from the CRT face to a distance of 3 or 4 feet, turn the coil sideways to the CRT, and turn off the coil power. The set may be on or off for this procedure. Correction for color purity can be postponed as one of the last steps of the repair routine.

15.4.2 Raster Brightness

Barring any major defects, this first examination of the raster should take less than a minute after the raster has come on. A quick look at the brightness level is next in order. For television receivers, the raster should be bright enough to be seen in a well-sunlit room (not direct sunlight). For computer monitors, the raster should be lightly visible at maximum brightness control settings in average room lighting. Adjust the brightness controls to achieve this condition.

When, in your opinion, the raster is not bright enough within the first minute or so after turn on, go immediately to the next step.

Set the tuner to a low-frequency local channel and observe the picture as you rapidly advance and retard the brightness control to its full limits several times. If the brightest areas of the picture appear as sparkling, silvery patches at the high brightness levels, as seen in photo 53, you have a defective picture tube. The CRT may have low cathode emission or air may have seeped into the tube through the pores of the glass to degrade the high vacuum of the tube, called a *soft tube*.

The reason for this test at an early time in the testing process is to determine if the CRT is good or bad. A soft picture tube may work reasonably well after a short time, and the opportunity for this test will be lost when delayed to a later time. A picture tube tester will verify your findings. When the CRT is determined to be bad, the customer should be notified immediately. They may not want to invest the cost of the CRT plus other repairs into an old receiver. Let the customer make this decision; it is called good customer relations. The three most expensive parts of the receiver are the CRT, the tuner, and the horizontal output transformer. Do not make these decisions for the customer.

15.4.3 Picture Synchronization

When you select a channel and get a picture, you can only examine the quality of what you see when the picture is stable. The vertical roll in photo 15 will appear as a series of pictures separated by a black bar (sync bar) that is moving up or down at a steady rate. The rate of movement may be slow, as photo 15 implies, or it may be moving rapidly to

give the illusion of several overlapping vertical pictures. When your receiver has a vertical hold control, and many sets no longer have them, adjust this control to stop the picture from rolling. When you can get the picture to stand still, even if only for a moment, you know that the vertical oscillator is able to run at the correct frequency and that it is not receiving the vertical sync signal to hold it at that frequency. The horizontal section is stable, so the sync separator and the differentiator (high-pass filter) and possibly an amplifier are all OK. This will indicate a problem in the section after the sync separator but before the vertical oscillator, in the low-pass filter and a possible amplifier. Under these conditions, you should be able to make the picture roll in one direction and then in the other direction, faster than 60 Hz and slower than 60 Hz.

When you cannot make the picture stop rolling or change the direction of rolling, you know that the vertical oscillator is too far from the correct frequency to be controlled by the vertical sync pulse. This indicates a vertical oscillator problem in the area of the components that determine the frequency of oscillation.

A picture that has an upward movement indicates a vertical oscillator frequency higher than 60 Hz. A downward movement then means that the frequency is below 60 Hz.

Locking the horizontal deflection oscillator to the transmitted sync signal has similar implications. Photo 16 has the horizontal sync bars slanted to the right (top more to the right than the bottom). Slanting to the right tells you that the horizontal oscillator is at a frequency higher than 15,750 Hz. Left slanting lines are not shown, but would identify a horizontal oscillator at a frequency lower than 15,750 Hz.

Testing the horizontal locking action follows the same pattern as was used for the vertical oscillator. The variations will depend on the available controls of the receiver. Television sets that have horizontal countdown circuits generally have no frequency adjustments. Other models may have only a horizontal hold control, while still other sets may have a horizontal hold control for the user and a horizontal frequency range control for the technician. On receivers that have a horizontal hold control, turn the control in the direction that causes fewer slanted lines. When the control can be adjusted to change the lines from slanted in one direction to upright, to slanted in the other direction, you know that the oscillator is able to run at the correct frequency, but is not getting the horizontal sync signal that will lock it onto the transmitter. When the picture is not rolling at the same time that the lines are slanted, you know that the sync separator and the integrator (low-pass filter with a possible amplifier) are all OK and the problem is in the differentiator (high-pass filter and possible amplifier). When the picture cannot be set upright at any time, the problem is in the horizontal oscillator.

Photo 17 shows the picture rolling at the same time that it has slanted lines. The defect must be in a circuit that is common to both the horizontal and vertical sync signals. The sync separator is the only circuit that has this common bond. Remember that the sync separator is a class C clipping amplifier with a full video signal at the input and only the sync signals at the output. See Section 15.5.5 for instructions on testing the sync separators.

15.4.4 Luminance Amplifiers

You will get your best results by checking the luminance circuits for quality when the picture on the CRT is displayed in black and white. You may recall that all picture detail is contained in the 4-MHz-wide luminance video signal, as evidenced by photo 6. This is further supported by the chroma only of photo 23, showing that only color smears with a frequency content of 1 MHz (or less) are recovered by the chroma circuits.

Set the brightness and contrast controls to what, in your opinion, is a good black and white picture. The whites should not be so brilliant as to compress the highlighted details. For instance, in photo 6, you should be able to see the folds, creases, and shadings of the dress worn by the lady seated at the right. The contrast should not be so dark as to make the deepest areas look like silhouettes. The fountain at the top center has a marbleized curved surface with highlights and shadows. We will be looking for defects in the luminance amplifiers, such as the low-contrast picture seen in photo 19, or those that show frequency response degradations, such as photos 20 and 21. Delay line problems like the one shown in photo 22 are compared at the end of this section to other defects that cause similar looking pictures. All these problems can be analyzed with an oscilloscope as described in the following paragraphs.

The insufficient contrast of photo 19 is characterized by a weak and washed out picture that is clouded and lacks crispness. Some part of the luminance amplifier chain has low gain, or losses have been added to the signal that should not be there.

From the block diagram of Figure 15.1, we will examine the circuits of the two luminance amplifiers and the delay line. Note that this problem cannot be caused by either of the three color mixer amplifiers or the three color output amplifiers. A defect in these circuits would need to be something common to all three circuit sets, or else it would cause a picture display like one of the photos 43 through 48, covered later.

Using a strong local channel, determine the peak-to-peak video signal at the output of the video detector. View the signal at the vertical rate (60 Hz) to establish the peak white level indicated by the vertical interval tests signals (VITS), shown in photo 26, and the tip of the sync pulse as the maximum black level. Compare this measurement to the signal level noted on the schematic diagram. Then set the contrast control to maximum and test the signal strength at all the other vital test points in the luminance amplifiers until you find a low-amplitude reading.

Photo 20 shows how the picture will look when the section loses the high frequencies in the video signal. Poor high-frequency response is generally caused by an open peaking coil, a defect in the delay line, or some component in a feedback circuit. An increase in shunt capacity will route the high frequencies to ground. The smear is caused by the accompanying phase distortion, which will always be streaked to the right.

Photo 21 shows how the picture would look when the amplitude of the signal is reduced at the low frequencies compared to the high video frequencies. It is said to have poor low-frequency response. This condition is generally caused by a defective coupling capacitor (in series with the signal) or an open emitter bypass capacitor. What you will see is a picture in which the large areas (low frequencies) are not as prominent as the sharp details of the picture (high frequencies) and, as a result, the picture appears to be heavily outlined.

Effects of a shorted delay line are seen in photo 22. In the magnified section, the luminance signal (black and white) has arrived 1 microsecond (μs) before the chroma signal and causes a shadow to the left of the man's head. The chroma signal is still displayed 1 μs after the luminance signal is completed and appears as a color smear after (to the right of) the man's head.

The delay line has been shown to be an inductance that forms one plate of a capacitor. The ground plane (coil form) provides the second plate of the capacitor at ground potential. The inductance of the coil is in series with the signal path, while the capacity is in parallel across the signal path. You may recall from your earlier studies of transmission lines that this configuration causes a signal time delay. The coil may become open and interrupt the flow of signal to the CRT, resulting in no monochrome picture. When there is a color signal, it may arrive at the CRT without the luminance signal, as seen in photo 23. When the coil shorts to the ground plane, exactly the same conditions will result as an open coil.

The input end of the coil could short to the output end of the coil, setting up zero delay time. The monochrome signal will arrive at the CRT about 1 μs before the color signal to cause misregistration of the two components of the color picture. The delay is emphasized in the magnified part of photo 22, but it will be more obvious in a real-life situation. The ground plane connection could become open so that the inductance of the coil is the only component of the delay line in the circuit. A series inductance will restrict the high frequencies more than it will the low frequencies, resulting in poor high-frequency response, such as in photo 20. Later, after discussing ghosts and poor convergence, which may have similar-looking effects, we will compare the three defects so that you can recognize the differences. The step by step testing of the luminance circuits is found in Section 15.5.6.

Photo 23 is titled "Chroma only." It could just as easily be called "No luminance." It shows the condition when the luminance amplifiers do not pass the video signal. The defect could be an open delay line or any reason for the luminance amplifiers to be completely inoperative. It shows how the recovered chroma signal will display only the chroma frequencies through the three mixer and three color output amplifiers below about 1 MHz. The colors appear as blotches with no picture detail. When the 4-MHz monochrome video signal that made up photo 6 is added to the chroma only of photo 23, the result will be the good color picture of photo 5.

Photo 24 shows the effects on the picture when the B+ voltage from the low-voltage power supply is not filtered sufficiently. It generally means that a power supply filter capacitor or a decoupling capacitor (also a filter) in the dc supply line to the luminance amplifiers is open. The ripple voltage is shown as 120 Hz (two cycles vertically) when the low voltage has a full-wave rectifier. A half-wave power supply rectifier will have a 60-Hz ripple (one cycle vertically). The same effects were

seen in photo 18, in which the 120-Hz ripple gets into the horizontal sync circuits.

These defects are easily found by momentarily touching a replacement capacitor across the terminals of the suspected defective capacitor. Select any large-value capacitor, 100 microfarads (μF) or greater, that has a dc voltage rating equal to or greater than the capacitor in the circuit. Add a 10 kilohm (kΩ) resistor in series with the substitute capacitor and momentarily touch this test circuit in parallel with the defective capacitor. If the problem clears up, you have found the defective component. If not, go on to the next most likely capacitor until you find the defective component. This does not mean to randomly wander all over the receiver. It requires that you study the schematic and test only those capacitors that affect that circuit.

The video portion of the composite wave, from photos 25 and 26, is changing constantly during a live program. These waves are what you will see on your oscilloscope when viewing the video signal at the output of the video detector at the horizontal frequency (photo 25) and at the vertical frequency (photo 26). These are the real-time waves of the video signal that are developed in Chapter 5. They are given here, again, as a time saver.

It would be difficult to identify the frequencies that make up the video part of these waves from photos 25 and 26. However, the blanking and sync pulses are true square waves at a fixed frequency and can be used to gauge the high- and low-frequency response of the luminance amplifiers. A standard square-wave test procedure is included in Section 15.5.6.

Photo 26 should be viewed first in order to establish the peak-to-peak signal level, using the VITS signals immediately following the vertical blanking signal. Examine the relative squareness of the blanking and sync pulses at this time. The horizontal rate video signal in photo 25 will reveal the presence of the color sync burst on the back porch of the horizontal blanking pedestal.

Photo 27 shows a picture tube that is out of convergence. Recall that color purity is a condition in which each electron beam does not strike all its intended color dots. The green beam may strike the green dots at some part of the phosphor screen, but not at other parts of the screen. Convergence describes the behavior when all three electron beams meet as they pass through each hole in the shadow mask to energize their respective color dots. When the blue and red electron beams pass through one hole in the mask as the green beam passes through a completely different hole, the picture will show a green edge to the figures on the screen. Misconvergence will be only marginally noticeable on a color picture and is best viewed on a black and white picture. Photo 27 has a red fringe to the left of the objects and a blue fringe to the right, made more noticeable in the magnified section.

Photo 28 is a crosshatch test pattern from a generator that is used to adjust the convergence. The correction is accomplished by a series of three magnet sets (six magnets) placed around the outside of the CRT neck. The set closest to the front of the CRT is a two-pole set with a north and south pole field. The second set is a four-pole set, quartered into two north and two south pole sections. The third set is a six-pole set with three north pole sections separated by three south pole sections. Each manufacturer has a favorite adjustment procedure in their service manual. See Section 15.5.4 on CRT servicing and adjustments.

Photo 29 shows sound bars in the picture. This will happen when the fine tuning is misadjusted or defective. Dark horizontal streaks appear as the performer is talking and vanish when the talking stops.

Photo 30 is colored snow called *confetti*. It is the noise produced by the chroma section when no color video signal is transmitted and the chroma AGC is misadjusted. The color AGC is often called the *color killer circuit*. It turns the chroma circuits off when the color burst is not transmitted.

15.4.5 Color

Adding color to an already existing black and white television picture sounds like a one-step process. In reality, there are many variations to the visual results such that each separate condition almost identifies itself. Photo 31 is a repeat of photo 5, a good color picture. Photo 32 shows too much color; the color control is set too high. Photo 33 shows when the tint control is set too much toward green, and photo 34 is set too much toward purple. The color and tint are customer preference controls that are adjusted to what the customer finds most pleasing; but you want to make sure that the color gain control is at mid-position for normal color and that the tint will change over the range from too green to too purple. Since you do not know what the clothing colors are, you need to adjust the tint control for the best flesh tones. It doesn't matter what color the skin is; you will always recognize correct flesh tones.

Photo 35 shows the color subcarrier oscillator out of sync with the color burst signal. When the oscillator is far off frequency, as in this photo, the red, green, and blue diagonal stripes will be thin and close together. As the oscillator comes closer to the correct frequency, the color bars will get thicker and less slanted. This condition is caused by the loss of the color burst signal to the oscillator or by a frequency determining component in the oscillator having changed value.

The best testing results are achieved when you use a color bar generator as a signal source. There are two generator types in general use. They develop (1) the NTSC color bar pattern of photo 37 and (2) the rainbow color bar pattern of photo 41.

The NTSC color bar signal sets a different dc brightness level for each of the eight bars represented in photo 37. This is seen in photo 39, which is called the gray scale, along with the associated voltage waveform pattern seen in photo 40. These two photos represent the luminance portion of the video signal for the NTSC color bar pattern. The modulated chroma signal waveform is shown in photo 36. When the voltage of photo 36 is added to the voltage of photo 40, the result is the waveform found in photo 38. The waveform in photo 38 produces the color bar pattern seen in photo 37. These five photos support and finalize the development of the colorplex composite video signal from Chapter 8. The colors in photo 37 are, from left to right, white, yellow, cyan, green, magenta, red, blue, and black. They are *precisely* the three primary and three secondary colors plus black and white for the NTSC color system. Learn to recognize particularly the colors of cyan and magenta. They are the colors you will seek and adjust for when tuning the chroma circuits or setting the tint control.

The rainbow color bar pattern, seen in photo 41, represents a phase-induced chroma pattern of ten colors. The color sequence and phase angle of the chroma signal for the colors are, from left to right, yellowish-orange (30°), orange (60°), red (90°), magenta (120°), reddish-blue (150°), blue (180°), greenish-blue (210°), cyan (240°), bluish-green (270°), and green (300°). The colorplex composite video wave for the rainbow color bar pattern is given in photo 42. You can see from photo 42 that there is no different dc voltage level for the individual color bars, so the gray scale cannot be examined. Only two of the ten colors match the exact shade and phase angle that are specified by the NTSC color system. They are, magenta at 120° and green at 300°. These colors in the NTSC system are 119.4° for magenta and 299.4° for green, close enough. The remaining primary and secondary colors are far enough off angle as to be only indications of the true colors. Red at 90° should be 76.5°. Blue at 180° should be 192.4°, and cyan at 240° should be 256°. Yellow is not represented, nor are black and white. Note further that only nine color bars appear in photo 41 because the television receiver overscans in the horizontal direction and one of the bars is missing. Is the yellow-orange bar on the left missing or is it the green bar on the right? You are left to make this judgment.

The NTSC color bar generator is typically five times more expensive than the rainbow color bar generator, which explains the popularity of the rainbow bar generator in the service industry.

We already know from the block diagram of Figure 15.1 that the luminance signal is fed into three parallel sets of amplifiers. Each amplifier set is used to operate one of the electron guns inside the tricolor CRT. Then, from Chapter 8, where we learned that the sum of red, green, and blue makes white, we know that the three branch signals of the luminance will look like a black and white picture when viewed together without chroma.

If we examine each branch all by itself, the red set of amplifiers driving the red electron gun will produce a red and black picture (photo 56). The green branch will produce a green and black picture (photo 58), and the blue branch, a blue and black picture (photo 60). A raster produced by only one electron gun at a time will display the three primary colors as are seen in photo 55 (red), photo 57 (green), and photo 59 (blue).

Each amplifier set is direct coupled to the CRT as a means for setting up the dc voltage at the CRT cathodes. The color is then added by the R − Y, G − Y, and B − Y output signals from the chroma circuits to the respective branch set of amplifiers.

From here, we could escalate into a full brigade of "What if" conditions. So, to develop a systematic plan of analysis, think through a color flow chart that expands Figure 15.2 in the areas of test 1 (raster) through test 6 (color sync) that will cover all your questions for quality color. Assume a yes answer to test 1, you have a raster, and omit any references to sound since these areas have already been tested. Figure 15.3a is one example of such a flow chart.

Test 1A is added following a yes response to the raster question. We have already checked for raster size with enough brightness, and now we

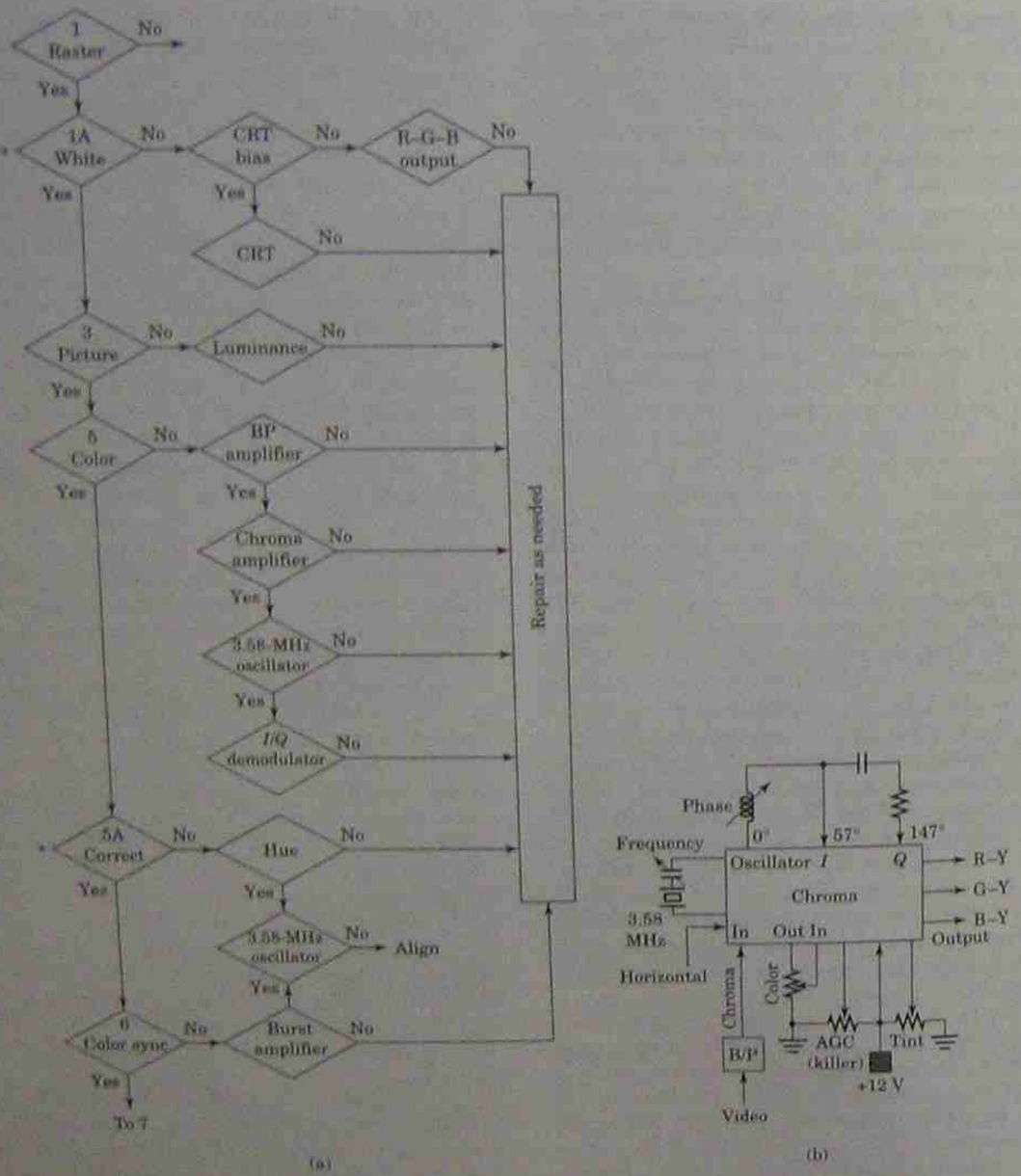


FIGURE 15.3
(a) Troubleshooting flow chart for color; (b) chroma microchip circuit.

want to make sure that the raster is white. When it is not white (in your opinion), try adjusting the red, green, or blue screen controls to establish a standard white raster. An alternative to a white raster is one that has a slight green overcast, rather than a red or blue overcast. Compare photos 2 and 3. Measuring the dc voltages at the base pins of the CRT and comparing these to the schematic values is the more positive way to set up a white raster. In the test routine, normal voltages at the CRT base when the raster is not white will direct you to test the CRT.

Again, testing the CRT early in the examination process may be a time saver in the long run. When either of these two conditions is found, stop the preliminary examination and go directly to the schematic for testing these circuits.

Skip test 3 in Figure 15.3 since the luminance amplifiers have already been evaluated.

The color test is divided into two parts. *No*, you do not have color at all, and *yes*, you have color, but the colors are wrong. When the color is totally missing, test the band-pass amplifier or filter first, then the chroma amplifiers, then the 3.58-MHz subcarrier oscillator, and, finally, the I and Q demodulators.

The chroma section in color television was the first to go to integrated circuits, and it is doubtful that you will ever see a discrete component chroma circuit. You are more likely to see a circuit similar to Figure 15.3b. It is strongly recommended that you use an NTSC color bar generator to test these circuits because of the predictable input and output signals.

There is enough data known about the microchip chroma circuit that it can be tested with confidence almost like a discrete circuit. In Figure 15.3b, first measure the video signal going into the band-pass filter and then the chroma signal into the chroma chip. The signal will come out to the color control and back in again to the color demodulators. Measure the subcarrier signal at the crystal oscillator and again out to the two phase shift networks to the two demodulators. Measure the color difference signals out at the R – Y, G – Y, and B – Y outputs.

Test to see that the dc supply voltage is present and that the color AGC and tint dc voltages are intact. This will give you more than enough information to make a determination about any part of this circuit. The procedure is outlined in Section 15.5.7.

Photo 43 of the picture guide series is the display that you will see for an inoperative red electron gun. The fault area could be a dead red electron gun, a defective red screen control, or an incorrect cathode voltage. The cathode voltage is the dc collector voltage of the direct-coupled red output amplifier. A defect in the red video output amplifier and sometimes in the red mixer amplifier will change the red electron gun cathode voltage and shut down the red electron gun. Photo 44 is the cyan raster that you will see for a dead red electron gun with no video signal applied. The same conditions apply to the green and blue video amplifiers, as follows.

Photo 45 represents the conditions that you will see when the green electron gun fails to contribute its share of the monochrome picture. Photo 46 is the magenta raster that results from a dead green electron gun. The cause of these conditions can be traced to the electron gun itself or to a failure in the direct-coupled green output amplifier or mixer amplifier.

Photo 47 shows a color picture with no contribution from the blue electron gun, and photo 48 is the yellow raster when the blue gun is inoperative.

15.4.6 RF Circuits and Other Conditions

Photo 49 shows a weak and snowy picture caused by a broken antenna lead or a signal from a distant station. Notice that the contrast ratio from white to black in photo 49 remains reasonably good compared to photo 19, which shows weak video due to reduced gain in the luminance amplifier circuits. The structure of the picture is grainier in photo 49 than it is in photo 19, and photo 49 has more noise, including confetti; photo 19 does not. Compare these two photos to become familiar with weak video due to reduced gain (19) and weak video due to antenna signal strength (49).

Photo 50 shows ghosts in the picture. A *ghost* is a displaced multiple image that appears slightly to the right of the main image. The ghost is the transmitter signal from the same station that reflects off of a structure and arrives at your antenna later in time than the direct-path main signal. A ghost signal is generally limited to a signal channel and is corrected by changing the antenna orientation. In some congested urban areas, rotating the antenna to clear a ghost on one channel will cause a ghost to appear on another channel. In severe cases, special single channel Yagi antennas are used for each channel to be received. Occasionally, the same ghost may appear on all channels. This is an indication of a video IF amplifier that is out of

alignment. IF misalignment is extremely rare, particularly in the more modern receiver circuitry, unless someone has attempted alignment and failed.

Photo 51 shows radio-frequency interference (RFI). This refers to any annoyance in the picture that arrives by way of the antenna. Only one source disturbance is shown in this series, although there are a number of other sources. Photo 51 is a continuous wave at a frequency close to the picture carrier frequency. Other types of interference may include diathermy radiation from medical devices, cochannel or adjacent channel interference, or harmonics of other service transmissions. The citizens band radio, at 27 MHz, has a second harmonic at 54 MHz, at channel 2. However, all transmitters guard against interfering with other transmissions, and the receivers have input filters at the antenna terminals that eliminate most of the probable annoying RF signals.

Photo 52 shows a case in which the video IF amplifiers are overloaded. This condition is caused by a radical change in the AGC voltage. This change increases the video IF gain to the point that the last video IF amplifier becomes saturated and compresses the sync pulses. It may affect only one channel or all channels. When only one channel is affected, adjusting the AGC voltage control may cure the problem. Be sure to check all channels to see how the AGC change affects them. Severe cases may affect all channels. An external AGC voltage may be applied and adjusted to verify a defective AGC circuit.

Photo 53 shows the silvery effects seen when the CRT has low emission or is a soft tube. There is no other cause for this effect.

Photo 54 shows poor focus. The camera is in focus but the picture tube is not. You can adjust focus with or without a picture. Look for focus of the horizontal scan lines.

15.4.7 Comparing Similar Effects

The shorted delay line in photo 22 and the ghosts in photo 50 look much like the poor convergence seen in photo 27. The double imaging caused by the shorted delay line in photo 22 will be there on all channels, but will disappear when the color control is turned down and only the monochrome picture is viewed. This will not happen for the other two defects. Poor convergence as seen in photo 27 is there all of the time, on all channels, with or without color. It is best viewed with a monochrome picture and will evidence itself as a color fringe to the left or right, or both, of the figures. The ghosts seen in photo 50 will be seen on one channel but not on others, with or without color.

15.5 TROUBLESHOOTING BY SCHEMATIC

Where can you get schematics? The fastest and cheapest source is the main public library in most larger cities. You cannot buy these schematics, but you can photocopy all the data that you need. You will want the brand name and the model number or chassis number of the receiver to speed your search for the right document. The libraries get their material from Howard W. Sams and Company, which you can also use as a source. Some electronic parts distributors carry the Sams literature that you may purchase locally. If you have a major department store service center in your area, they will copy schematics of their products for a fee. The receiver manufacturers service center also has schematics and replacement parts that you can order.

Howard W. Sams & Company publishes an annual index that lists over 900 products from as far back as the 1940s by brand name, model, and chassis number that are cross indexed to the Sams PHOTOFACTS® service folder. Service data from Sams is available back to the 1920s on special request. The index also includes the name, address, and phone numbers for the service departments of all the major OEMs (original equipment manufacturers) of home entertainment products. Call or write to Howard W. Sams & Company, 2647 Waterfront Parkway East Drive, Indianapolis, Indiana 46214; the phone is 1-800-428-7267.

Small parts are purchased from your local distributor in urban areas or from one of the catalog mail order houses such as Newark Electronics or Allied Radio in Chicago, Illinois, or MCM Electronics in Centerville, Ohio.

When you have the service literature (we will use the folded schematic diagram), locate the major sections of the receiver on the schematic diagram by following the format of a block diagram, such as Figure 15.1. Highlight all the controls with one color marker and the transistors and chips in another color marker. Find the chassis layout drawing (like Figure 15.4) and mark the controls and active devices in the same color markers as on the schematic.

Next, you will need some basic equipment. It is assumed that you already have the hand tools to do the repair, such as a long-nose pliers, diagonal pliers (cutters), wire stripper, assorted screw-

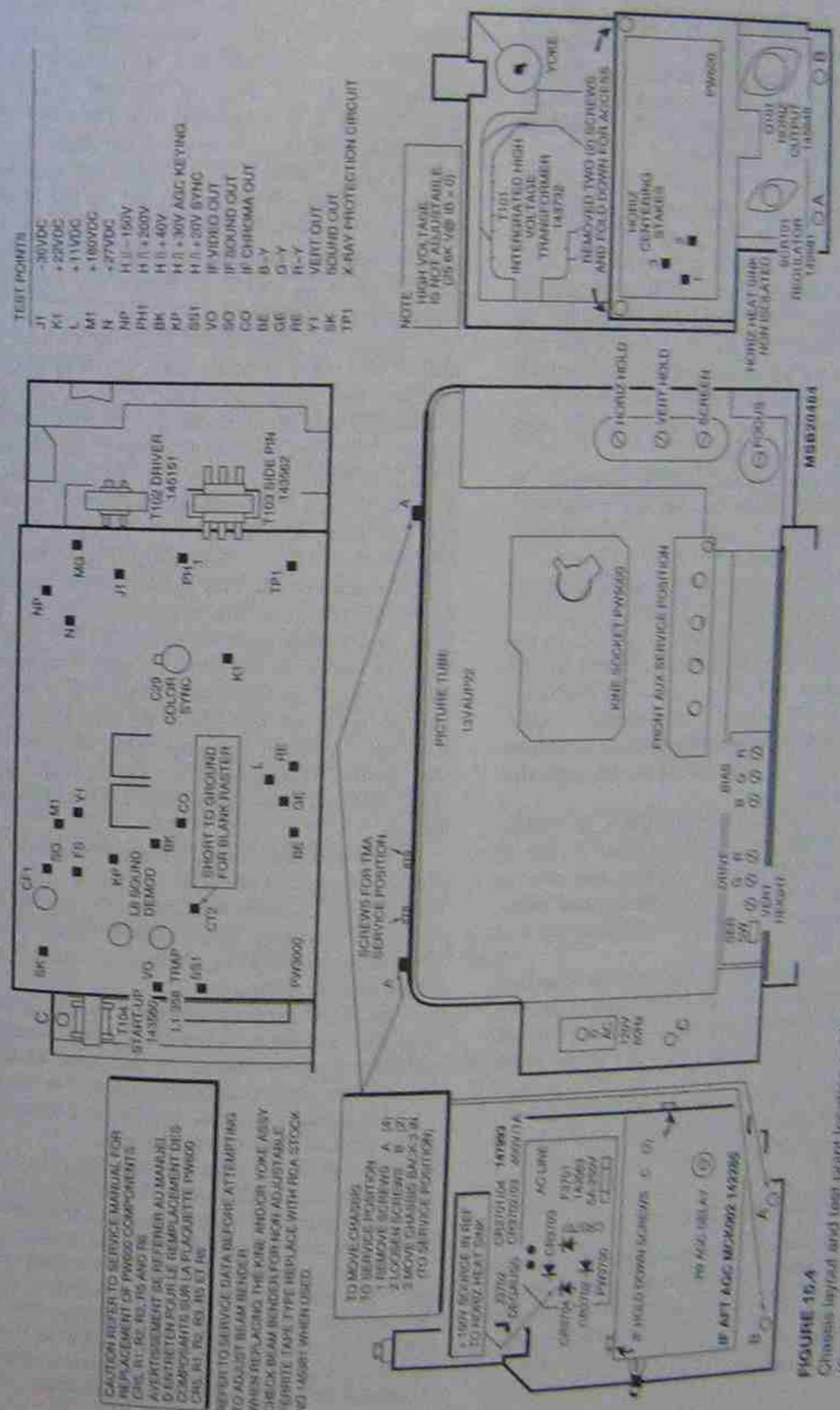


FIGURE 15.4
Chassis layout and test point location guide. (Courtesy Thomson Consumer Electronics, Inc.)

drivers, and a soldering iron. The *minimum* test equipment should include an isolation transformer, a multimeter, and a 35-MHz or better oscilloscope with a low-capacity probe. Your second expenditure for test equipment should include a high-voltage tester and a good RF signal generator.

A typical procedure for troubleshooting instructs you to first isolate the trouble section by sight and sound observations, using simple control adjustments. Having determined the probable fault section, measure the waveforms in that section for amplitude, frequency, and distortion to further reduce the search area to a specific part of the section. The dc voltages are measured at the terminals of the active devices in that section to identify the faulty circuit, and then the dc resistances are measured to find the defective part.

The dc voltages marked on the schematic at each terminal of the active devices are the normal operating voltages with no signal. The line voltage is set to 120 V rms, and a 1% tolerance meter is used. Learning what voltage variations to accept or reject will define your expertise in the area of trouble analysis. Up to 10% differences in voltage are considered acceptable in many cases. When the difference approaches 20%, they should be evaluated based on the other findings in the circuit. Oscillators and the circuits that are affected by the oscillator signal show the dc voltages when the oscillator is operating normally.

The ac waveforms do not include a dc voltage reference. Therefore, set the oscilloscope on the ac input setting. The dc setting is sometimes used to examine signal voltages for distortion, but *never* use the oscilloscope to measure dc voltages; use a dc reading voltmeter.

The controls are left in the position that best represents normal operation at the time of failure, except for the contrast control, the color control, and the brightness control, which are set to maximum.

Based on all of this lead-in material, we will use the folded schematic to troubleshoot a television receiver section by section.

15.5.1 Vertical Deflection

We start with the vertical section because it is the simplest and most straightforward. It includes the 10 transistors in the service schematic at locations 13, 14, 15, and 16, layers A and B, with the deflection yoke found at location 17. You should have had this section marked off as directed in Section 15.5.

Q_{3603} and Q_{3604} are both common-emitter amplifiers (gain with phase reversal) that make up the vertical relaxation oscillator. Any change in voltage at the collector of Q_{3603} is applied to the base of Q_{3604}, where it is amplified and inverted. The collector output of Q_{3604} is applied through R_{3607} to the base of Q_{3602}, where it is amplified and inverted again. The twice-inverted signal at the collector of Q_{3602} is in phase with the original change that will sustain oscillations. The vertical hold control R_{3606} along with R_{3608} and C_{3602} forms the frequency determination components.

Q_{3601} and Q_{3602} are a Darlington pair as one-half of the class B push–pull vertical output that matches the Darlington pair of Q_{3605} and Q_{3606} as the second half of the push–pull vertical output amplifier. The final vertical output signal is taken from the common connection between Q_{3601} and Q_{3605} to terminal Y_2 and the deflection yoke socket, pin 1 in schematic section 17. Pin 1 of yoke socket (J_{101}) connects to the yoke plug (P_{101}), then through a yellow wire to the two halves of the vertical yoke in series, then out the green wire at pin 2 of the plug and socket back to terminal Y_1, vertical return, to complete the yoke circuit. The jumper between yoke plug terminals 4 and 5 is a safety measure to interrupt the 150-V dc line and shut down the receiver when the yoke plug is removed from the socket. The dashed circles around Q_{3601} and Q_{3604} tell you that these two transistors are heat sinked.

The oscillator output signal from the collector of Q_{3603} is applied through the diode (CR_{3601}) to the base of Q_{3602}, where it is compared to the feedback signal for linearity. The feedback signal comes from the output terminal Y_1, through resistor R_{3609} back to the emitter of Q_{3602}.

Q_{3603} is directly coupled to the collector of Q_{3602} and serves as a low-level power amplifier. Its collector feeds a signal to the base of Q_{3605} and Q_{3606} of the push–pull output amplifier circuit.

Q_{3610} and Q_{3609} act as a switch to enhance the decay time of the wave for retrace.

The eight transistors from Q_{3601} to Q_{3604} work like an op-amp with the oscillator signal to the noninverting input (base of Q_{3602}) and the feedback signal to the inverting input (emitter of Q_{3602}).

When troubleshooting the vertical circuit, divide the section in half by observing the signal waveshape (29) at the base of Q_{3602}. No signal at this point means that the oscillator is dead. Next, measure the dc voltages at the base, emitter, and collector of both oscillator transistors. Note that these amplifiers are direct coupled, so a defect in one amplifier will change the dc voltages on the other amplifier. Check the dc source voltage to ensure that the section is adequately powered. Turn the power off and use the tester in Figure 15.5 to check the transistors. Substitute a known-good capacitor for C_{3602} to evaluate the timing of the oscillator when frequency is a problem. Measure resistances and check the capacitors until the defective component is located.

When a 2.0-$V_{p\text{-}p}$ signal that looks like wave 29 is found at the base of Q_{3602}, go directly to the output terminal Y_2. Here you should observe the 55-$V_{p\text{-}p}$ trapezoidal signal of wave 35. A signal found at Y_2 means that the vertical output section is working and that the defect is in the yoke itself. Measure the dc resistance of the yoke. No signal found at terminal Y_2 means that the vertical output amplifiers are defective. Subdivide the remaining circuits. Check the signal at the base of Q_{3605}, waveform 30, which should be a 55-$V_{p\text{-}p}$ trapezoidal wave. A *yes* response at the base of Q_{3605} tells you that Q_{3601} and Q_{3605} are OK and the defect is in the output amplifier. A *no* response here means that Q_{3605} or Q_{3606} is in trouble. As direct-coupled, voltage-divider-biased, common-emitter amplifiers, a defect in either circuit will cause false voltage readings in the other circuit. Unsolder the base of Q_{3606} to open that circuit and test Q_{3605} all by itself. The voltage wave at the collector of Q_{3605} should be several times larger than the 2-V base signal. A signal here tells you that Q_{3605} is OK and Q_{3606} is bad. No signal here identifies Q_{3605} as the defective circuit. Test the transistors, and measure the dc voltages or resistances to find the defective component. Q_{3610} and Q_{3609} are part of the Q_{3605} and Q_{3606} circuit and will identify themselves when there is a defect in that section.

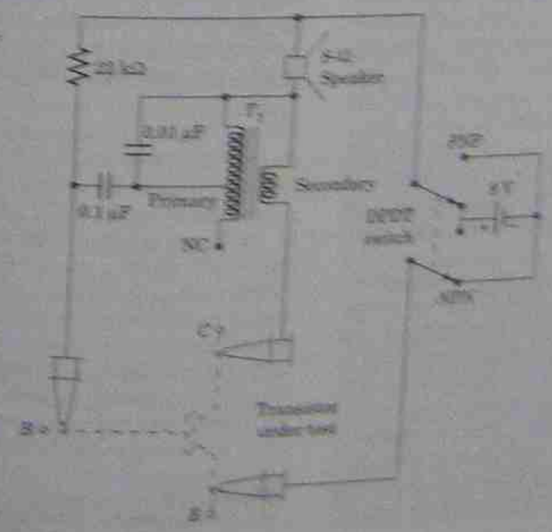
When a signal is found at the base of Q_{3605} but not at the output terminal Y_2, the push–pull output amplifier is the cause of the problem. But think about push–pull amplifiers. When the *top* output amplifier (Q_{3605} and Q_{3610}) stop working, the *bottom* output (Q_{3606} and Q_{3609}) may still be OK and produce a vertical raster like either photos 6, 8, or 10. It is possible that the additional strain on Q_{3606} and Q_{3609} brought on by the failure of Q_{3605} or Q_{3610} could cause the bottom amplifier to burn out also. The same conditions will prevail (but inverted) when the bottom set of amplifiers goes out first. The exact cause of the failure will be found by voltage and resistance measurements. Often push–pull amplifiers are balanced for symmetry by using a matched pair of transistors. A defect in one transistor requires that both transistors be replaced. Check the parts list for this feature.

The vertical sync signal is coupled into the oscillator circuit by way of R_{3608} and C_{3602} from the sync separator.

15.5.2 Horizontal Deflection and High Voltage

The automatic frequency control (AFC) circuit lies at location 13D in the folded schematic and op-

FIGURE 15.5
Simple in-circuit transistor tester.



ates exactly like the system described in Section 4.6. The positive horizontal sync pulse is shown as waveform 37 to the anodes of diodes CR_{3110} and CR_{3111}. The positive horizontal feedback pulse comes from terminal PH_1 (pin 8 at 19E) of the horizontal output transformer and is applied to resistors R_{3128} and R_{3129}. The resulting +dc control voltage feeds through R_{3136} to the base of Q_{3029} to maintain the oscillator frequency.

The horizontal multivibrator serves as the oscillator at location 14 and 15D and is made up of Q_{3030} and Q_{3032}. As power is turned on, +22 V dc sets Q_{3030} into conduction. The collector voltage of Q_{3030} turns on Q_{3032} and drives it into saturation. The collector voltage of Q_{3032} feeds back to the base of Q_{3030} and drives it into saturation.

The base current of Q_{3030} feeds through R_{3147}, down through the factory selected resistors R_{3196} and R_{3197} and R_{3150} to charge capacitor C_{3146} (3900 pF). As the charge on C_{3146} builds, it raises the base voltage of Q_{3031} and increases the emitter voltage of Q_{3031}, Q_{3029}, and Q_{3030}. A rise in emitter voltage of Q_{3030} turns this transistor off, which turns Q_{3032} off, and C_{3146} is allowed to discharge through R_{3150}, the factory-selected resistors, and through R_{3152} and R_{3182} back to ground. As C_{3146}'s charge drops, the base voltage of Q_{3031} turns this transistor off, and the common-emitter voltage drops and allows Q_{3030} to start conducting and to start the cycle over again. The dc base voltage on Q_{3029} (AFC) will affect the common-emitter voltage and determine when Q_{3030} is to start the next cycle.

The collector output signal of Q_{3032} is applied to the horizontal driver amplifier Q_{3034} by direct coupling. Q_{3034} is an NPN common-emitter, signal-biased, class C, low-level power amplifier. The charge on C_{3153} holds the base of Q_{3034} at −1.3 V dc as compared to the voltage on the left side of R_{3154} at +9.6 V dc, placing Q_{3034} in a cutoff state except for the time that the horizontal output amplifier draws base current. The output signal from Q_{3034} is transformer coupled to the base of Q_{101}, the horizontal output amplifier.

Several points of interest can be noted about this coupling transformer. It is a step-down transformer (voltage wise) as noted by the dc resistance of the windings, 7.6 Ω on the primary compared to 0.15 Ω on the secondary. This should not be used to judge the turns ratio unless the wire gauge is the same for both windings, and we have no assurance that it is at this time. Iron core transformers that do not have the pin numbers labeled on the frame will follow the old-fashioned numbering system. This system deals with six pin positions that are counted clockwise as the pins face you. A color paint dot identifies pin 1. The horizontal driver transformer (T_{102}) does not have pins 2 or 5, but has the remaining four pins seen in Figure 15.6. Transformers separate the dc voltage on the primary from the secondary dc voltage. This is an essential point for transformer T_{102} since pin 3 is attached to the common connection for the horizontal output circuit, called **hot ground.** Hot ground is depicted in Figure 15.7 as a common circuit connection that is elevated above chassis ground by some value of dc voltage. In either of the power circuits of Figure 15.7, there is no set rule to dictate where ground is to be placed within the system. As drawn in solid lines, each system will function independently without a ground connection, like two flashlight circuits. In the case when the negative side of the power supply is attached to the chassis, the positive end of the supply is floating and indicates a positive dc power source. The positive terminal of the source could have been attached to the chassis to establish a negative dc power source. Both of these systems of polarity designation can exist within a single product.

The case for the hot ground connection is seen in Figure 15.7 by the dashed lines in the drawing. The negative side of source B is chassis ground, which represents the 150-V dc power supply in the foldout schematic. Power source A represents the voltage that results when part of the horizontal output signal is rectified, converted to dc, and then added on top of the source B voltage. The positive end of source B and the negative end of source A now become hot ground for circuit A. The horizontal output transistor Q_{101}, the damper diode CR_{101}, and

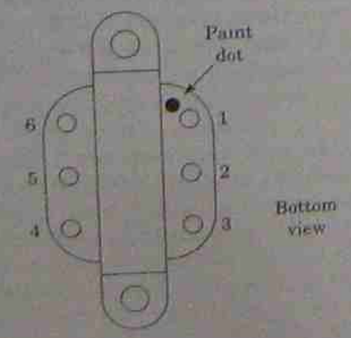


FIGURE 15.6
Iron core transformer terminal identification.

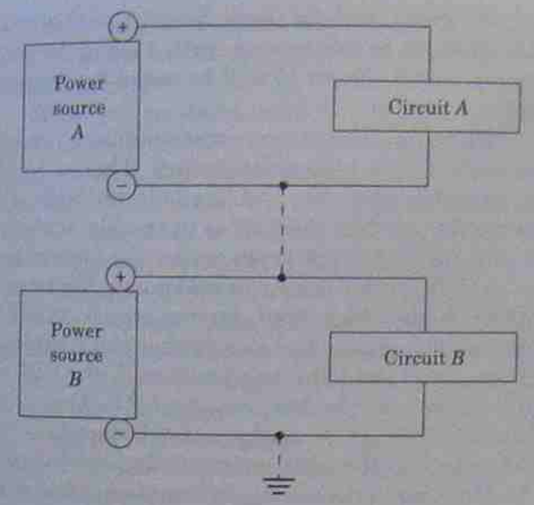


FIGURE 15.7
Example of a hot ground system.

the regulator diode SCR_{101} are all mounted on the heat sink, and the heat sink is at hot ground potential. The negative end of the scope connection is generally not at house ground potential and may be attached to the hot ground in this circuit for waveform comparisons.

The output side of transformer T_{102} feeds the horizontal signal to the base of Q_{101}, the horizontal output amplifier, which is a signal-biased, class B, NPN common-emitter power amplifier in a TO-204 case (formally TO-3 case). The collector of Q_{101} feeds the signal to pin 2, the primary of the horizontal output (high-voltage) transformer T_{101}. The damper diode is in parallel with Q_{101} but is polarized in the opposite direction. The high voltage exits the transformer by way of a heavy wire after going through two diodes and a resistor that are built into the transformer housing. The focus and CRT screen grid voltage is developed across the same winding at terminals 1 and 14 of the high-voltage transformer. The CRT filaments use a 22-$V_{p\text{-}p}$ signal out of pin 10 of the transformer as the heater voltage. The windings at the bottom of the horizontal output transformer (T_{101}) are used to develop the various pulses at the horizontal rate that are used as gating pulses for the AGC, the AFC, and the chroma circuits. Two of these pulses are also used to generate the +22-V dc source, the +27-V dc source, and the +180-V dc source. It is becoming more common to use the horizontal signal to develop low-voltage sources that deliver low current because of the better efficiency at the higher source frequency.

The X-ray protection circuit using Q_{3038}, at location 14E, is in reality an overvoltage sensor. There is no simple X-ray detector that can be installed economically in every television receiver. However, a correlation between beam current and X-ray radiation has been well documented. Additionally, current changes can be translated from a voltage change across a fixed resistance. Based on these factors and the dialog from Section 4.9.2, the operation of the X-ray protection circuit can be described and understood.

Q_{3038} is a PNP transistor that is voltage divider biased from the +180-V dc power supply and, with diode CR_{3134} across the base–emitter junction, is held in a cutoff state. A positive 55-$V_{p\text{-}p}$ pulse from pins 6 and 7 of the horizontal output transformer is rectified by diode CR_{3132} and applied to the emitter of Q_{3038}. Under normal operations, this rectified pulse voltage has no influence on the status of Q_{3038}.

An increased signal voltage (overvoltage) at transformer T_{101} will increase the rectified voltage at the emitter of Q_{3038}, causing it to conduct and remain latched until a counteraction is taken. The resulting change in Q_{3038}'s collector voltage is applied to the base of Q_{3029} (AFC control), which will set the horizontal oscillator to an unusually high frequency. Now, drawing from an earlier discussion, which stated that because the vertical and horizontal systems are each operated at a single frequency into a reactive load (the yoke), the load impedances could be designed for maximum efficiency at that designated single frequency. It stands to reason then that a radical change in horizontal frequency would cause the output transformer to function at a point that is far away from its peak efficiency, which would decrease the signal voltage and cause an unviewable raster (or picture). The X-ray latch may be reset by turning the receiver off for a few seconds. If the condition that caused the latch to activate was only temporary, the set will function normally after reset, whereas a permanent defect will reactivate the latch and shut the set down again.

The PW_{600} regulator board found at locations 18, 19, 20, and 21, layer B, is also part of the horizontal circuit and controls the +114 V dc to the collector of the horizontal output amplifier Q_{101}. The 114 V is the bootstrap voltage. That is, the dc voltage for the output amplifier is supplied by the signal from the same amplifier. When the 150 V dc comes on, Q_{101} begins to conduct and sends a signal to the primary (pins 2 and 3) of the output transformer. The signal is coupled into the secondary

(pins 4 and 5) and then through the silicon-controlled rectifier SCR_{101}, converting the signal to a dc voltage that feeds back through the primary to the collector of Q_{101}. The gate of the SCR is controlled by the oscillator circuit Q_{604} and Q_{605}, which acts like an automatic light dimmer control. Q_{604} and Q_{605} oscillator is the same circuit that is used for the vertical oscillator, except at a higher frequency. Q_{601}, Q_{602}, and Q_{603} adjust the amplitude and frequency of the oscillator. When the +114 V dc increases, the error amplifier lowers the regulator signal and pinches off some of the current through the SCR to reduce the voltage. Inversely, a decrease in the 114-V level will direct the error amplifier to increase the regulator signal so that the SCR will pass more current. The dc voltage to the horizontal output amplifier is regulated to prevent raster blooming when the brightness control is advanced. Without regulation, the raster would get larger at higher brightness levels, until the raster faded away. Higher horizontal output currents due to short circuits or a sudden change in load impedances will force the regulator to shut down the regulated 114-V dc supply. The horizontal-deflection and high-voltage sections are then protected from overvoltage by the X-ray protection circuit and from overcurrent by the regulator circuits. These functions were at one time the job of a ½-A fuse. However, transistors are so sensitive that they will burn out before the fuse can protect them.

Defects such as those found in photos 1 (no raster), 11 (keystoning), 12 (narrow raster), 13 (yoke ringing), and 54 (poor focus) would attract your attention to this section, with 1 being the most common defect. Photo 16 will be saved for the sync section.

When you have a no raster condition, remember to check the high voltage first. This will help you to decide when the problem is in the high-voltage section or when the CRT is in trouble. Slide the tip of the high-voltage probe under the suction cup at the CRT button until you make metallic contact with the high-voltage lead. Approximately 25,000 V here (for this schematic) means that the horizontal section is OK, and the trouble is with the CRT or the voltages at the base of the CRT. Less than about 15,000 V at the high-voltage button tells you that you are in the right section to find the trouble.

Now, let's take all this information, along with Figure 15.8, and use it to troubleshoot the horizontal-deflection and high-voltage circuits in the schematic. Figure 15.8 is a block diagram drawn to match the circuit of our specific schematic, and it meets all the requirements of the generic (typical or general) block diagram.

When no high voltage is measured at the anode of the CRT, the next step would be to divide the circuit in half. It is suggested that the primary of the driver transformer (T_{102}) be considered as the midpoint in this section. This transformer is easy to find, as seen in Figure 15.4, and it separates the low-level signals from the high-level power circuits. The collector of Q_{3034}, the PC board contact HD_4, or pin 4 of T_{102} are all the same place. The following

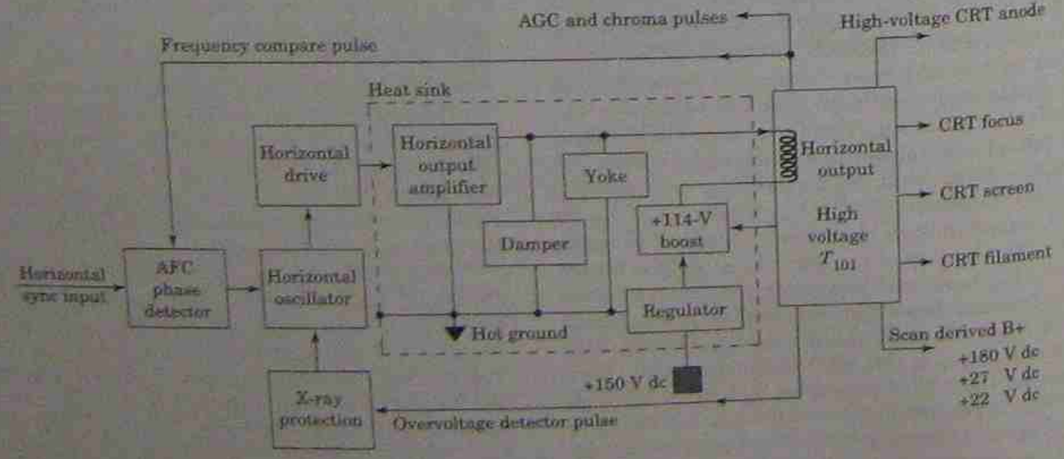


FIGURE 15.8
Horizontal-deflection block diagram for the circuit of the schematic.

test routine will take on the appearance of a pyramid that starts at the top, with a good or bad response to each test.

When you measure a 45-$V_{p\text{-}p}$ square wave at 15,750 Hz (waveform 43) on the primary of T_{102}, you know that the horizontal oscillator, the inverter, and the driver are all working correctly. When the frequency is near 15,750 Hz, the X-ray protection circuit is inactive and is basically out of the system, like an open switch. The problem must be at Q_{101} or beyond. We will first discuss all the negative aspects of this waveform measurement before venturing into the high-level signal section. We will examine the signal for waveshape, amplitude, and frequency. Each time a wrong signal is observed, the remaining part of the circuit will be divided in half again (when possible) until a single defective circuit has been isolated.

No signal or a low-amplitude signal on the primary of T_{102} will suggest that you look at the base of Q_{3034}. If it has a 3.3-$V_{p\text{-}p}$ square wave, then you know that the Q_{3034} circuit is defective. Measure the dc voltages on Q_{3034}, test the transistor using Figure 15.5, and then check the resistances. This last three-step procedure will become a ritual as each defective circuit is found.

Wave distortion could be attributed to C_{3154}, R_{3155}, and C_{3155} in the collector circuit of Q_{3034} driver amplifier or C_{3149}, R_{3186} and C_{3186} between Q_{3030} and Q_{3032} when distortion is seen at the base of Q_{3034}.

Changes in oscillator frequency of less than ±10% are likely caused by the charging time constant of C_{3146}. Look at waveform 39 (base of Q_{3031}) for this examination. Measure R_{3147}, R_{3197}, and R_{3150}. When these are all OK, change capacitor C_{3146} with a 3900-pF, 5%, 600-V film capacitor (from the parts list). When the signal frequency is much higher than 15,750 Hz (18 kHz or higher), an overvoltage condition may exist and the X-ray protection circuit has taken control of the horizontal oscillator. Turn the set off and unsolder the collector lead of Q_{3038} or one side of resistor R_{3130} so as to remove the X-ray protection from being an influence on the oscillator. **WARNING!** Before turning the set back on, connect a dc voltmeter between hot ground and pin 3 of the high-voltage flyback transformer to measure the regulated +114 V. Turn the set on while observing the meter. If it reads up to 120 V dc, continue the tests. If the voltage exceeds 122 V dc, turn the set off immediately. Continued testing of the high-voltage section may be accomplished in one of two ways. Do all resistance tests only, or connect a heavy-duty light dimmer between the isolation transformer and the ac input line cord. Turn the set on and reduce the input power until the regulated voltage reads 114 V. Further voltage measurements on the set will be lower than those marked on the schematic. Find a voltage source (say the +27-V supply) and compare the voltage *now* to what it should be normally to find the reduction factor. For example, 21.6 V dc would be 80% of 27 V. All voltages will now be lower by 20%.

A good waveform measured on the primary of T_{102} suggests that you next check the secondary wave (51) as measured from hot ground. (Note the hot ground symbol at the waveform number.) The base wave of Q_{101} would be almost identical to wave 51. No signal on the secondary of T_{102} indicates a defective transformer, while no signal at the base of Q_{101} suggests that either R_{102}, C_{105}, L_{101}, or R_{103} is defective. All these can be verified with an ohmmeter.

The 0.2 V dc at the base of Q_{101} (from hot ground) indicates the presence of a signal charge across C_{105} and can be verified with a voltmeter. No dc voltage at the base of Q_{101} indicates either no collector dc voltage, a defective transistor, or no signal at the base due to a defective base circuit component. Resistors are generally rated at least two times the power that they are expected to dissipate safely, so the 0.68-Ω, 2-W wire-wound (2WWW) resistor R_{102} can handle over 1 A of base current to charge C_{105}.

A good signal found at the base of Q_{101} suggests that you check the collector signal next, but the schematic is marked "Do not measure." Yet you know that someone at sometime had to measure this voltage in order to declare waveshape 52 as 900 $V_{p\text{-}p}$. They are warning you not to damage your test equipment. Older oscilloscopes had a vertical input rating of 600 $V_{p\text{-}p}$ max. Newer scopes are rated at 200 to 300 $V_{p\text{-}p}$ max. The collector signal of Q_{101} of +114 V dc plus the 900-$V_{p\text{-}p}$ ac could burn out the input section of your scope. You can circumvent this situation by using a large-value voltage divider from the collector of Q_{101}, through a 10-MΩ resistor and a 100-kΩ resistor in series to hot ground. Measuring the voltage across the 100-kΩ resistor to hot ground gives you a 100:1 reduction or about a 9-$V_{p\text{-}p}$ signal that you can measure on your oscilloscope.

If you are not that adventurous, you may take the more conservative route of measuring the pulse output voltages at pins 6, 8, 9, 10, and 12 of the high-voltage transformer. The transformer pin-out

diagram is given at location 24E on the schematic. Remember that it is the collapse of the magnetic field around the high-voltage secondary of T_{101} that gives you the large pulses on all the other windings. Even with an open high-voltage secondary (or open high-voltage diode), there will be a reduced pulse at each of these pins when a good input signal is applied to the base of a working horizontal output amplifier.

You may still need a voltage divider to measure wave 47 from pin 12 (220 $V_{p\text{-}p}$) and wave 48 from pin 8 (240 $V_{p\text{-}p}$) of the horizontal output transformer. A 100-kΩ and a 10-kΩ resistor will give you a 10 : 1 ratio so that, across the 10 kΩ, you would measure 22 and 24 $V_{p\text{-}p}$, respectively.

Figure 15.8 shows the damper diode and deflection yoke across the output of Q_{101} horizontal amplifier. The signal at pin 5 is rectified to +114 V dc and added to the +150 V dc to be fed back into pin 3 and through the primary to the collector of Q_{101}. The output of pin 6 is used for X-ray protection. Pin 8 output is used for the AFC and to develop the +180 V dc via rectifier CR_{3014} at 18E. Pin 9 feeds the pulse voltage to the AGC and the chroma circuits. Pin 10 is the CRT filament supply, and pin 12 is used to develop the +27- and +22-V dc source voltages, while pins 1 and 14 furnish the focus and CRT screen grid voltages.

If you need to replace the horizontal amplifier Q_{101} or regulator SCR_{101} for any reason, remember to use silicon grease on both sides of the mica insulator for good heat transfer to the heat sink.

The horizontal-deflection and high-voltage section is the most involved and least understood circuit in the entire television receiver by a large majority of the technical people in television. If you feel that you do not have a basic understanding of this section, take the time now to reread Section 15.5.2. Different television receivers have different circuits from what has been described here, but they all have the same general functions in the same order. Understand the order and interaction between the functions in this section.

15.5.3 Low-voltage Sources

We can neither create nor destroy power, we can only change its form.

In the preceding section we identified three of the scan-derived power sources as the +180-, +27-, and +22-V dc sources. There is a fourth source from pin 6 of the flyback transformer to terminal PH_5, over to location 16E, where diode CR_{3015} is used to develop the −30-V dc source, noted at the primary (pin 5) of transformer T_{102}. The −30-V dc source is used to operate the vertical-deflection circuits. As we examine all the other circuits (later paragraphs), you will see that every circuit (except one) draws its power from one of these four sources. If the horizontal section fails, all four of these sources are rendered inoperative. However, when the horizontal section fails, there is no raster. Without a raster, there is no need for vertical deflection (−30-V dc source), video (+180- and +27-V dc sources), the tuner and video IF amplifiers (+22-V dc source), or color (+27-V dc source), and they all shut down. The only deviation from the standard format is that the sound section is also operated from the +27-V dc source, so when horizontal deflection fails, the sound circuits also become inoperative. A no raster, no sound condition has been established as a low-voltage power supply problem, which this is in reality. Except that in this case it is a secondhand power supply problem that stems from a failure in the horizontal-deflection circuits.

All four of these sources are generated by an operating horizontal output amplifier. Since the horizontal output circuit cannot create power, it must in turn draw power from some other source. This other source is the 150-V dc power circuit that comes from the low-voltage power supply located at 23E and F on the schematic and that, in turn, draws power from the 120-V ac power line.

This supply is a full-wave bridge rectifier circuit and filter that converts ac voltage to dc voltage. The 120-V ac enters through the plug at the lower right on the schematic, through the power cord to the socket of the interlock S_{101}, which is attached to the cabinet back. When the cabinet back is removed, the interlock is open circuited to protect inexperienced persons from electric shock. On the service bench, a cheater cord is used to replace the interlock cord when the back of the cabinet is removed. With the back in place, the interlock socket, denoted by the open circles, makes contact with the interlock plug, solid circles, which is attached to the printed circuit board to complete the input power connection. The lower prong on the ac plug is shown thicker, and the lower interlock circles are larger to identify that this cord is polarized for safety.

Once onto the PW_{3700} power supply board, the lines run through a saturable reactor L_{3701}. The function of the saturable reactor is to limit the amplitude of the ac input voltage by slightly flat topping both peaks of the input wave. Power companies are proud of their record for maintaining the lines at exactly 120 V rms and 60 Hz, and well they should be. However, sudden load changes on the line due to customer demand or equipment failure may cause line surges that are undesirable in the television receiver, even when quickly corrected. The saturable reactor helps to compensate for these changes, as well as to remove noise spikes that are all amplitude changes.

At the output of the saturable reactor, the L_{1W} terminal goes directly to one side of the bridge rectifier input. The other side of the line (L_{1R}) goes through a 5-A fuse, the voltage varible (V) and back to terminal L_{1W}. The switch output goes through the temperature variable resistor (T) and the degaussing coil to terminal L_{1W}. The capacitors across the diodes are to remove noise spikes. The output of the bridge rectifier, at terminals ST_1 and RZ, go to the low-voltage supply filter. When redrawn, as in Figure 15.9, you can see that this is a choke input filter with the primary of T_{104} serving as the choke. The voltage across C_{114A} represents the +150-V dc output as measured from pin 3 of T_{104} (+) to the RZ terminal (−) on the PW_{3700} board. The ripple voltage that the filter choke removes from the rectifiers pulsating dc appears as an ac voltage across the choke. This ac can be stepped up when the choke is the primary of a transformer. The stepped-up ac on the secondary of T_{104} is used as a start-up voltage (+27 V start) after being rectified by diodes CR_{3123} and CR_{3129}.

A no raster condition like photo 1 along with no sound suggests that you start your trouble search in the low-voltage power supply. When you have the back off and before you plug into power, check the 5-A fuse. Then plug in the ac line cord, remembering to use an isolation transformer, then turn the power on and measure the dc voltage across C_{114A}. In power supplies, it is safest to start from the dc output end and work toward the ac input terminals. The most common faults will be an open C_{114A} filter capacitor, an open 3.9-Ω fusible resistor, a burned-out 5-A fuse, an open bridge rectifier, a defective line cord, and, finally, a defective switch. These will be found by voltage measurements and then, with the set unplugged, verified by resistance measurements.

A burned-out 5-A fuse hints at a heavy current demand by the set due to a short circuit or simply a fatigued fuse that burned out due to age. When the replacement fuse burns out immediately upon application of power, the supply or the load on the supply has a short circuit. The fastest way to isolate the defective circuit is to divorce the load

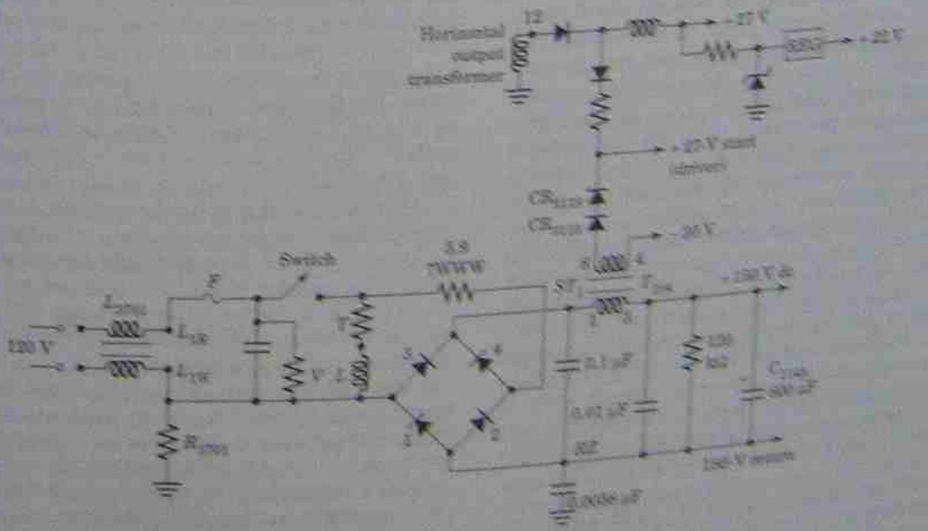


FIGURE 15.9
Low-voltage power supply circuit, CTC 96 series. (Courtesy Thomson Consumer Electronics, Inc.)

from the supply and test the unloaded supply separately. In the schematic, the PW_{800} regulator board is the only load on the 150-V dc supply and the separation is made easy by unplugging the deflection yoke from its socket. Follow the +150-V dc line from the plus terminal of C_{114S} through pins 4 and 5 of the yoke socket to the Y_S terminal of the PW_{800} board. Now, if a replacement fuse burns out, you know that the short circuit is in the power supply and not in the load. If the fuse holds, then the short circuit is on the PW_{800} board.

Remove the PW_{800} board from the receiver and bench test the circuit using a reduced dc supply voltage. A 30-V dc supply with plus at the Y_S terminal and minus at the *RZ* terminal will cause all the operating voltages to be about one-fifth of the values marked on the schematic.

Totally ignore the +27-V start voltage until after you have the +150-V dc line up and running.

A contaminated raster like photo 4, poor purity, tells you that the degaussing coil is not working. Remove the coil plug (P_{3702}) from the socket and turn the set on. After a stable raster (or picture) is obtained, plug the degaussing coil back into the socket while viewing the CRT screen. A properly working degaussing coil will cause a disturbance on the CRT face similar to that seen in Figure 1.10, which will last for only a few seconds. No such pattern means that the degaussing circuit is defective. Turn the set off and measure the dc resistance of the three circuit parts. No values are given on the schematic or on the parts list, but the general values can be used. Temperature-variable resistors (thermistors (Th) like RT_{3701} at room temperature measure around 10 Ω. Voltage-variable resistors (varistors (Vr) like RV_{3701} at room temperature measure about 100 kΩ, while the coil should be only a few ohms of wire resistance.

It was mentioned earlier that when the frequency of the ac voltage to a power supply was increased, as was the case for the scan-derived voltages, the circuit efficiency is improved. What this means is that less iron is required for the core of the transformer and lower-value filter capacitors are needed to achieve the same effective filtering. It reduces the size and cost of the components and also provides a ripple frequency that is less objectionable when it gets into the signal circuits.

Switching Power Supplies. We will leave the schematic only long enough to examine the power supply of Figure 15.10, as found in the computer monitor of Figure 9.9. The ac line voltage is fed through a saturable reactor (S_{102}) to the bridge rectifier circuit D_{107} to D_{110}. The dc output voltage (about 150 V) appears across C_{113}, with the plus voltage going to the primary, pin 2, of transformer T_{101}. How can a dc voltage be transformed to the secondaries of T_{101}? The answer is that it cannot! The dc voltage is used to operate a power oscillator TS_{132} and TS_{131} that generates an ac signal, which can be transformed. TS_{132} is the power stage. The oscillator signal voltage across the primary is a square wave of about 400 $V_{p\text{-}p}$ at a frequency of 30 kHz. The frequency of the ac is possibly the least important characteristic of this type of system, and although 30 kHz is higher than the common 400- to 600-Hz typical frequency, it still meets the essential requirement of five or more times higher than the 60-Hz line frequency. Military aircraft use a 400-Hz generator as the ac input source, while some mobile units use a mechanical vibrator to chop the 12-V battery voltage supply into a 400-Hz pulsating dc voltage that can be transformed to a higher voltage level before rectifying and filtering takes place.

The output voltage is taken across three secondary windings to develop a total of 10 levels of dc voltages for this product. Output *A* is at +125 V dc. Output B fans out into six separate dc sources: a +16-V dc level, two +12-V dc levels with different degrees of filtering, two switched +12-V dc sources for the TTL and RGB input signals, and a regulated +5-V dc level for the logic chips. The *C* output breaks up into three sources, all at +26 V dc and each with a different filtering system. They are labeled +26, +26A, and +26B (see Figure 9.9).

The output at *A* is fed down through a voltage divider that will change the base voltage of TS_{131} by adjusting R_1 at the lower-right corner of Figure 15.10. The emitter of TS_{131} is clamped by a zener diode so that a change in base voltage will cause a change in collector current through the light-emitting diode (LED) at pins 1 and 2 of IC_{101}. IC_{101} is an **optical coupler.** The light-sensitive diode (pins 4 and 5) acts like a variable resistor with high resistance for a dark condition and low resistance at maximum LED current. It provides a means of changing the resistance in one circuit with no mechanical or electrical connection to the controlling circuit. Changing the value of the light-dependent resistor (LDR) at pins 4 and 5 will change the base voltage on TS_{131} and control the amplitude of the signal out of TS_{132} to the primary (pins 1 and 2) of transformer T_{101}. Therefore, the setting of R_1 will adjust the dc output voltage at A, B, and C.

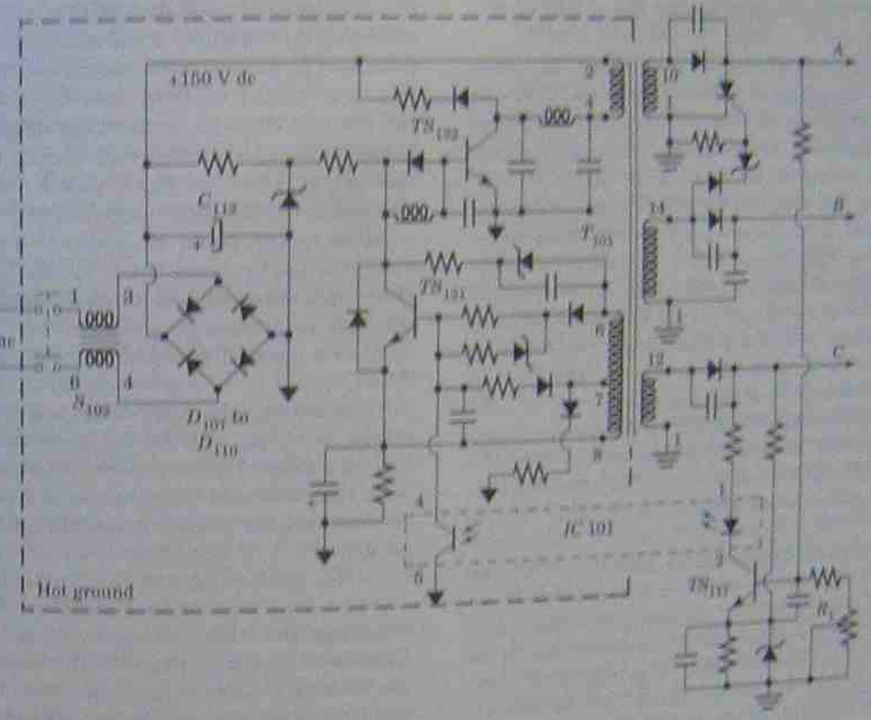


FIGURE 15.10
High-frequency, low-voltage power supply (switching power supply). (Courtesy Philips Consumer Electronics Company.)

Extreme care is advised when working on this type of supply, because hot ground is at one side of the ac line. The use of an isolation transformer is an *absolute* must in this case.

15.5.4 Cathode Ray Tubes

Some picture tube problems can be reversed, but the procedure may not be effective every time. Since the picture tube is the most expensive single component in the television receiver, a short amount of time invested in repair attempts is money well spent. Replacement costs include the labor time to remove and replace the CRT and may include the time to set the color purity, the gray scale, and convergence. Several hours could be involved.

Turn the set on and listen for the horizontal circuit to start up. The 15,750 Hz is well within the audible range and may cause the components to vibrate, giving off a low audible sound. Not all ears can hear this whine, and since the high-frequency capability of the ear diminishes with age, the mature ear may never hear it. Also listen for the crackling sound of the static charge building on the CRT surface when the set is first turned on. Evidence of these two sounds suggests the presence of high voltage. If you are not confident about hearing high voltage, measure it with a high-voltage probe.

No raster, like photo 1 of the troubleshooting series, indicates (1) no high voltage, (2) a defective CRT (probably open filaments), or (3) incorrect voltages at the base of the CRT. Check to see if all three filaments are glowing. Heaters in cathode ray tubes may be wired in series or in parallel on the inside of the CRT and are out of reach of the technician. Only two pins are assigned for heater use at

the base. A single, open, parallel heater will be covered later.

Turn the brightness up to maximum and measure the dc voltages on all the base pins shown in the schematic. By this time, you should have found a fault condition, unless the control grid or screen grid has an open on the inside of the CRT.

The only true test for a CRT is a commercial CRT tester. Some testers also have rejuvenation capabilities. They come with a collection of interchangeable sockets that match most of the CRT bases. Pin voltages are set up from a chart that comes along with the tester and are indexed by tube number. Tests include opens, shorts, and emission tests on each gun separately.

Low emission is caused by a buildup of contamination on the cathode during the time that the heated cathode boils off electrons. This buildup lowers cathode emission and results in lower brightness.

A countermeasure to low emission takes two forms. A picture tube brightener is installed by removing the CRT socket, plugging the brightener onto the CRT, and then attaching the socket to the other end of the brightener. The brightener steps up the heater voltage by about 30% for greater cathode current, so you need to be aware of the type of heaters in your set, whether series or parallel.

Picture tube rejuvenators can apply a high voltage between the cathode and the control grid that strips off the contaminants to restore cathode emission. Low emission is evidenced by long warm-up time, low brightness, poor focus, like photo 54, or the silvery condition seen in photo 53. Rejuvenators can occasionally repair shorts and opens on the inside of the CRT. Shorts are burned open by applying a high voltage across the shorted elements. Opens are repaired by applying a high voltage across the open elements while lightly tapping on the neck of the CRT with the hope that the two ends of the open will touch and weld together. Both of these procedures are chancy and can completely destroy the CRT. But you already have a nonworking device, which may be saved with just a little more effort.

In color receivers, when one of the electron guns is defective, there will be a raster or picture to match the color series in photos 43 through 48. When you suspect that one of the guns is defective, do *not* change any of the control settings in an attempt to correct the problem. It is sometimes difficult to determine which electron gun is in trouble since you do not know what colors should be in the picture. The best determination can be made when you turn off the station, turn down the color and the contrast controls, and set the brightness control to view a blank raster. A cyan raster, like photo 44, tells you that the red gun is out. A magenta raster, like photo 46, identifies a defective green gun, and a yellow raster, photo 48, points to a defective blue gun. But don't replace the CRT yet, until you have either measured all the dc base voltages or tested the CRT to confirm your suspicions. One open filament of a parallel-wired heater can cause this condition.

Replacing the CRT may not be the simple matter of taking out the old tube and plugging in the new tube. Those picture tubes that are sold with the yoke and convergence assembly already attached are the easiest to install, but are the highest priced.

The back of the device may already be removed during your tests. Then, turn the set off and discharge the high voltage using a shorting wire from chassis ground (first) to the high-voltage button under the suction cup, and unclip the high-voltage lead. Take the base socket off next. Loosen the hold-down clamp on the convergence assembly (there may be two, one at each end) and slide the assembly off the tube neck. Mark the assembly to indicate the front, back, and top for correct return onto the new tube.

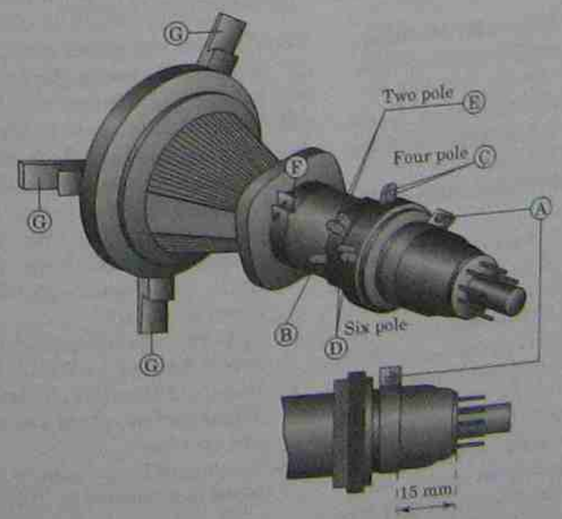
Unplug the degaussing coil and detach any grounding springs that you see around the front end of the CRT. Remove the two (or more) yoke hold-down screws and the yoke clamp, unplug the yoke, and remove it from the CRT neck with a twisting (left and right) motion. Yokes that have been in place for long periods of time may tend to stick to the glass neck. This can be relieved by blowing some talcum powder between the glass and the yoke center opening. Then remove the four corner hold-down screws and remove the CRT along with the degaussing coil. When installing the new tube (when possible), place the picture tube mask face down on a blanket or pad to protect the tube face. Slide the degaussing coil and tube retainer ring onto the new CRT to start the assembly process. Complete the process by running through the checklist in a reverse order. When completed, turn the set on to ensure that you have a raster (or picture) and prepare to go through the setup adjustments.

Each manufacturer has its own procedure because of the individualized nature of the components that they use. It is recommended that you follow the procedure that is tailored for your product. The following outline is given in order to acquaint you with the type of adjustments that go into the makeup of such literature. It is taken from the service manual of a computer monitor manufacturer.*

Purity Adjustments

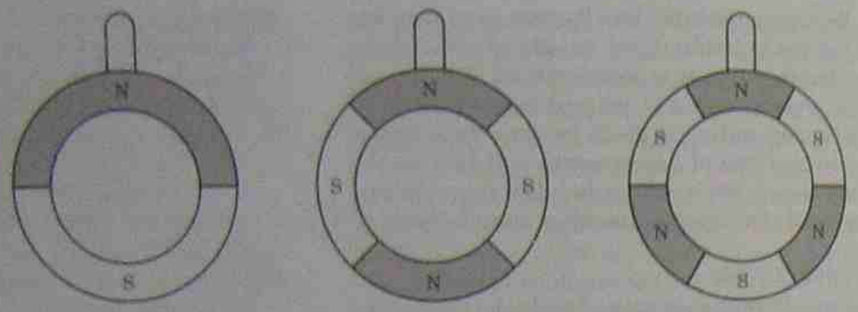
1. Loosen the yoke clamp and slide the yoke away from the rubber wedges. On new CRT installations, you would omit this step.
2. Remove the rubber wedges (G in Figure 15.11) and slide the yoke forward until it rests firmly against the bell of the CRT.
3. Tighten the yoke clamp screws slightly so that the yoke can be moved with some friction.
4. Place the multipole purity and convergence assembly in the position shown in Figure 15.11, 15 mm or $\frac{5}{8}$ in. from the base of the CRT. All tabs together and at top center.
5. Tighten the convergence hold-down screw (A) and turn the securing ring (B) counterclockwise. Position the unit so that it faces in an east–west direction and degauss the instrument.
6. Turn the unit on and feed in a crosshatch test pattern, like photo 28. Allow a 10-min warm-up period. Position the yoke to ensure that the raster is not slanted left or right.
7. Roughly adjust the static convergence, using tabs C and D. Convergence at the center of the CRT is called *static* convergence, and *dynamic* convergence (later) relates to the outer edges of the CRT face.
8. Set the vertical centering control to its mechanical center. Disconnect R_{723} and R_{724} to turn off the green and blue guns. (These resistor numbers [see Figure 9.9] are specific for this product only.)
9. Adjust the two-pole purity rings (E) to center the red vertical and red horizontal lines.
10. Disconnect the crosshatch generator and position the yoke for a full, pure red raster; see photo 55.
11. Reconnect R_{723} and R_{724} to reestablish the green and blue gun operation. Selectively adjust the three bias controls to observe a red raster, photo 55, then a green raster, photo 57, and then a blue raster, photo 59. Make minor adjustments to the purity rings (E) as needed. Purity rings (E) are a pair of two-pole magnets, (C) is a pair of four-pole magnets, and the rings

FIGURE 15.11
Deflection yoke and convergence magnets mounting arrangements. (Courtesy Philips Consumer Electronics Co.)



*Information adapted from Technical Service Data Manual No. 6523. Philips Consumer Electronics Co., Jefferson City, TX, pp. 4–5. Adapted with permission.

FIGURE 15.12
Two-, four-, and six-pole magnetic rings used in the convergence assembly. Each pole set will have two identical rings.



Two pole Four pole Six pole

(D) are a pair of six-pole magnets as portrayed in Figure 15.12. The interaction between pairs is identical to the discussion in section 2.11 and as seen in Figure 2.9.

Gray Scale Adjustments

1. Preset the brightness and tint controls to midrange, the color control to minimum, all bias controls to minimum, all drive controls to maximum, and the screen control to minimum, and disable the vertical-deflection section. Some products have a service normal switch for this purpose; others have a vertical collapse shorting terminal. Or you may need to improvise a way to defeat the vertical deflection without damaging the set.
2. Turn the set on and allow 10 min for warm-up. Advance the screen control until a faint horizontal line appears (any color).
3. Depending on the color obtained in step 2, advance the other two bias controls to obtain a faint white line across the CRT face.
4. Restore the vertical to its normal operating condition.
5. Advance the brightness and contrast controls to maximum and short the video input (or luminance) to ground. *Note:* On your device, make sure that this short will not damage the receiver. Any large value capacitor connected between a luminance signal point and ground will remove the video signal.
6. Adjust the color drive controls to obtain a 6500-kelvin color temperature white raster (warm white); then remove the short from step 5. With video applied, no color, the picture should remain in normal black and white for all settings of the brightness and contrast controls. There is no way to identify a 6500-kelvin white, so adjust for a white raster that, in your opinion, most nearly represents white snow.

Static Convergence

1. Disconnect R_{723} to turn the green gun off and loosen the locking ring (B) in Figure 15.11.
2. Apply a crosshatch test pattern, like photo 28, and allow a 10-min warm-up period.
3. Slowly spread and, if necessary, rotate the four-pole magnet ring (C) to converge the red and blue lines at the center of the CRT.
4. Reconnect R_{723} (green) and disconnect R_{734} (blue).
5. Slowly spread and, if necessary, rotate the six-pole magnet ring (D) to converge the red and green lines at the center of the CRT.
6. Reconnect R_{734} (blue).

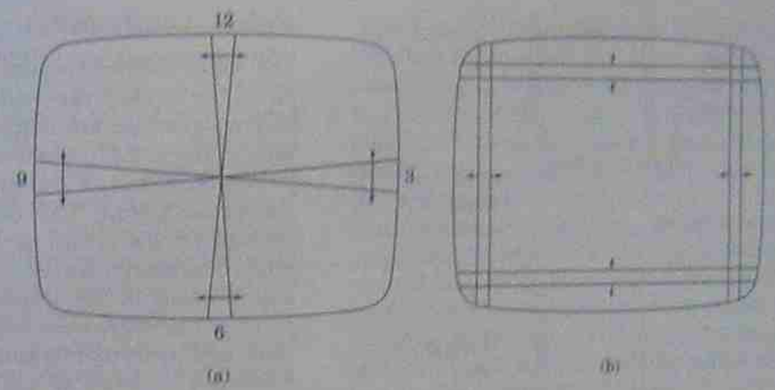
Dynamic Convergence

1. Turn off the green gun by opening R_{723}. Apply a crosshatch test pattern like photo 28, turn the set on, and allow a 10-min warm-up period.
2. Tilt the yoke up or down to achieve the best convergence at the edges of the CRT at 3, 6, 9 and 12 o'clock positions, as described in Figure 15.13a.
3. When the best position has been found, place a rubber wedge (G) between the yoke and the CRT neck. See Figure 15.14a for yoke up or yoke down position.
4. Tilt the yoke left or right to find the best convergence for red and blue across the full top and bottom of the CRT, as seen in Figure 15.13b.
5. When correct, place two wedges as shown in Figure 15.14b.
6. Reconnect R_{723}. Remove wedge 1 from step 3 and place it as shown in Figure 15.14c.

15.5.5 Servicing Sync Circuits

Possibly the smallest circuit to be encountered in a video product may be the synchronizing circuit (refer to the large folded schematic again). In our sam-

FIGURE 15.13
Interim steps when setting the dynamic convergence.



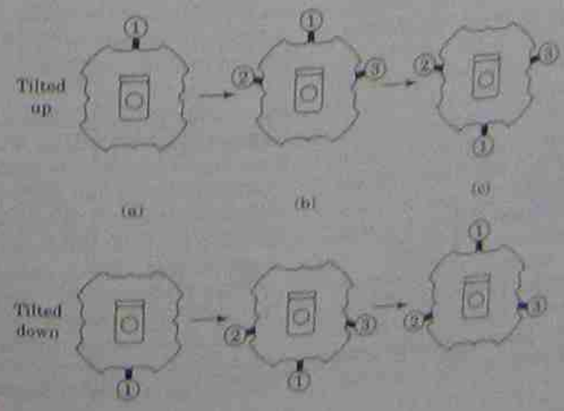
ple circuit in the schematic, the entire circuit is comprised of a single transistor, Q_{3003} at location 8E, with a low-pass filter at 13C (R_{3101} and C_{3101}) and a high-pass filter at 13D (R_{3131} and C_{3131}). Remember the two vital functions of the sync separator circuit. First, the circuit clamps the sync pulse tips to an established dc level. Second, as a class C amplifier, it clips and amplifies only the sync pulses. No dc source voltage is applied to the base of Q_{3003}. All dc paths are blocked by a diode or a capacitor. The self-bias is developed by about 16.54 microamperes (μA) of base current through the 1.3 MΩ of R_{3016}. Again remember that the schematic dc voltages are recorded with no signal applied.

The video signal comes from the video IF amplifier section at terminal board TS_{102}, pin 6, marked luminance at location 6E. It enters the main circuit board (mother board) at terminal V_o, then passes down through R_{3014} and C_{3016} to the base of Q_{3003}. The strength of the signal, waveform 1, 6-$V_{p\text{-}p}$ negative sync, appears as a charge across C_{3016} and adds to the 21.5 V dc at the base of Q_{3003}. The change in the base dc voltage sets the level of clipping to provide good sync for a strong or weak video signal. The collector output is denoted by waveform 4, 22-$V_{p\text{-}p}$ horizontal sync, and again as waveform 4, 22-$V_{p\text{-}p}$ vertical sync.

Troubleshooting this circuit becomes a simple exercise in waveform measurements at terminal V_o, first to ensure that you have a video signal. Next, look at the base of Q_{3003} to see if the video signal gets to the sync separator. Then look at the collector to make sure that the clipper–amplifier is working.

The sync signals leave the schematic here at terminal SS_1 to reenter at terminal SS_2, location 13C. Testing the horizontal differentiator, high-pass filter, R_{3131} and C_{3131}, is achieved by observing waveform 37 at the output of the differentiator as 6 $V_{p\text{-}p}$. When this circuit is defective, the output will be essentially a flat line. Testing the vertical integrator, low-pass filter, R_{3201} and C_{3201}, requires one more step. Waveform 26, shown as the output of the

FIGURE 15.14
Placement of the rubber wedges between the CRT and deflection yoke during the convergence setup. (Courtesy of Philips Consumer Electronics Co.)



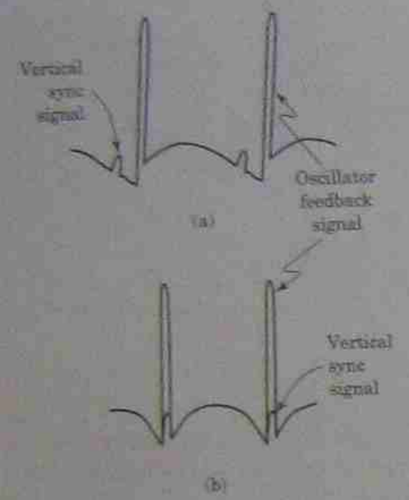


FIGURE 15.15
The vertical oscillator feedback signal (a) out of sync with the sync pulse, and (b) in sync with the sync pulse.

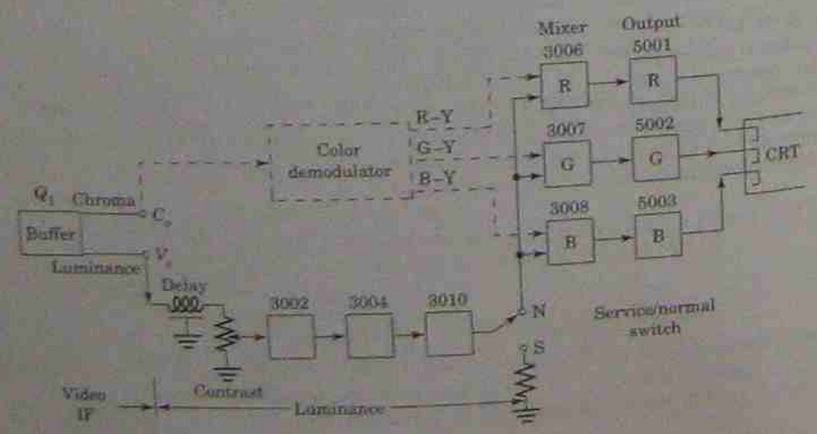
vertical integrator, is, in reality, the feedback signal of the vertical oscillator and will be seen here whether the sync pulse is present or not. You will need to slow the vertical oscillator by adjusting the vertical hold control to make the picture roll up (more time per cycle). As seen in Figure 15.15a, the small vertical sync pulse does not appear at the same time as the oscillator feedback pulse, and the sync pulse can be recognized. In Figure 15.15b, both pulses appear at the same time when the vertical circuit is locked in and the picture is stationary.

15.5.6 Luminance

The same troubleshooting procedure will be used for all the intelligence-bearing signal circuits. That is, arrangements are made so that a signal is present in the circuit, whether that be a transmitted television signal, a computer signal, or a bench-generated signal. The customer-accessible gain controls for the circuit under test are set to maximum. The search starts at the input to the section and proceeds to the output of the section. Oscilloscope patterns are examined for waveshape, amplitude, and distortion. It is at first assumed that the frequency is correct or has been set correctly and is not a factor. When an untrue wave is detected, the dc voltages surrounding that circuit are measured and compared to the voltages marked on the schematic. The final step then is to measure the dc resistance and/or substitute parts in order to find the defective component.

In our earlier discussion, it was established that the chroma signal was separated from the composite video signal at the output of the video detector and then handed off to the color demodulators. The remainder of the signal, now called the luminance signal, was delayed by 1 μs and then amplified. The amplified luminance signal was then added individually to each of the three color signals out of the color demodulator, where the three separate color signals went through three separate amplifier sets to the CRT. The same principles were expounded again in Chapter 12 using figure 12.11 to show greater detail. Figure 15.16 is a replay of that block diagram to match our schematic.

FIGURE 15.16
The luminance and color amplifier block diagram associated with the schematic.



In Figure 15.16 and the schematic, each mixer (matrix) and output amplifier are associated with a separate color. A defect in Q_{3006} or Q_{5001} will result in a CRT display like photos 43 and 44, with no red in the picture or raster. Q_{3007} and Q_{5002} will cause no green in the picture or raster, as seen in photos 45 and 46. No blue in the picture or raster, caused by a defect in Q_{3008} or Q_{5003}, will look like photos 47 or 48. Therefore, the only luminance amplifiers are Q_{3002}, Q_{3004}, and Q_{3010} from Figure 15.16 and the schematic. The remaining four transistors in the schematic, Q_{3035}, Q_{3001}, Q_{3011}, and Q_{3009}, are control circuits. In later receiver versions, these seven transistors will probably become a single-chip circuit that is used here as a reliability test circuit for the future chip.

The input luminance signal from terminal V_o, at 7E, is 6 $V_{p\text{-}p}$ with negative sync (waveform 1). The signal goes to the right (follow the arrow on the schematic) through R_{3011}, R_{3024}, L_{3002}, DL_{3001}, and L_{3003}, then up to the contrast control, in pin 3 and out pin 2, and then through L_{3007} to the base of Q_{3002}. The base signal of Q_{3002} (waveform 5) is listed as 0.5 to 2.0 $V_{p\text{-}p}$ depending on how the contrast control is set. At maximum contrast, we will be looking for 2 $V_{p\text{-}p}$ at the base of Q_{3002}.

Q_{3002} is a voltage-divider-biased, NPN, common-emitter, class A amplifier. It has gain with phase change. The output signal (wave 6) is 3 $V_{p\text{-}p}$ with positive sync, but notice that the sync pulses are compressed. The 11-V dc regulator, Q_{3035}, applies its output through R_{3059} to the emitter of Q_{3002}, and then from the emitter of Q_{3002}, down through R_{3012} to ground. This semifixed emitter voltage limits the gain of the positive sync pulses and concentrates the gain to the signal area between reference white and reference black of the composite video signal. The video signal had already been applied to the sync separator at terminal V_o, and the sync has no further function beyond that point.

The collector of Q_{3002} is direct coupled to the base of Q_{3004}. A defect in either transistor would cause an erroneous reading of wave 6. Should such a state exist, disconnect R_{3008} and measure wave 6 again. If the poor reading still persists, open the base of Q_{3004} and measure again. If wave 6 is still bad, the defect is in the Q_{3002} circuit. Had the measurement improved during the disconnect process, the defect would be found in the circuit that was disconnected before the improvement was noted.

Q_{3004} is a voltage-divider-biased, PNP, common-collector, class A amplifier with a gain of less than 1 and no phase change. It shows 3.5 $V_{p\text{-}p}$ at the base input and 2 $V_{p\text{-}p}$ at the emitter output (wave 7). Q_{3004} is capacitively coupled through C_{3013} to the base of Q_{3010}, which is a voltage-divider-biased, PNP, common-collector, class A amplifier. Having a gain of less than 1 and no phase change, the emitter output is seen in wave 8 as 1 $V_{p\text{-}p}$ and positive sync. Q_{3004} and Q_{3010} are straightforward amplifiers. A defect in waves 7 or 8 would direct you to measure the dc voltages on the amplifier in question and then check the dc resistance of the components. The signal at the emitter of Q_{3010} goes into pin 2 and out pin 3 of the service normal switch, then through the drive controls to the emitters of all three matrix (mixer) amplifiers, where we will leave this circuit for now.

At the emitter of Q_{3010} you will see a ferrite bead (FB_{3002}). Ferrite beads are compressed ferris iron oxide cylinders with a hollow center that slides over the wire in the circuit. They are a very inexpensive but effective way of adding inductance to the circuit without the need for terminals or solder connections. They are used to suppress parasitic oscillations and to tailor the frequency response of the circuit. You will see other ferrite beads throughout this schematic.

15.5.7 Color Circuit Troubleshooting

The chroma processor, U_{3001}, in the schematic (at 6A) is the first large-scale integrated (LSI) circuit to be examined in this series. The chroma circuit was the first section to go LSI, and it is doubtful that you will ever see a discrete chroma circuit again.

What do you remember about the chroma circuits that will help you to troubleshoot this block-box chroma diagram? We know that we need a chroma signal at the input. This is an amplitude-modulated signal in the frequency range between 2.1 and 4.1 MHz. You also know that there should be three color signals at the output, R, G, and B, or the color difference signals R – Y, G – Y, and B – Y. We need a subcarrier oscillator signal at 3.579545 MHz that feeds the two demodulators through some phase shifting networks and includes the color and tint controls. Can you find these signals and conditions in the schematic?

While you are searching for these key test points, notice that the waveforms have changed from the standard "off the air" composite video signal in the luminance section to a rainbow color bar test pattern for the chroma circuits. You will need a rainbow color bar generator, set to channel 3 or 4,

applied to the antenna terminals in order to match these waveforms.

The color signal is separated from the composite video by the chroma peaker circuit (band-pass filter) in the emitter of Q_1, located at 6E on the schematic, at the output of the video IF amplifier circuits. The signal is taken from pin 7 of TS_{102}, up to terminal C_e on the *PW*3000 board, where there should be 0.3-$V_{p\text{-}p}$ chroma, seen in waveform 2. There will be about one-half this amount at pin 1 of the chroma processor due to the voltage divider R_{3027} and R_{3058}.

If you have the correct input signal, go directly to the output at pins 8, 9, and 10. Turn the color gain control to maximum and read waveforms 17, 18, and 19, each with a different peak-to-peak amplitude. If you are satisfied with the output signals, the chroma processor may be all right and the problem lies elsewhere. When no output signals are found or are found to have very low amplitude, you need to examine this circuit. If the chroma processor is a plug-in chip and you have access to replacement chips, change the chip first. When the chip is soldered onto the PC board, do the interim tests before attempting to change the chip.

The manufacturer included an internal diagram of *U*3001 in the service manual, with no attached components. Figure 15.17 has been prepared to show the internal and external parts of this section. The input signal, at pin 1, goes through the first chroma amplifier, keyer 1, and the second chroma amplifier with an output at pin 6. Waveform 14 says that there should be 1.5 $V_{p\text{-}p}$ when the color control is set for maximum gain. The signal then goes through C_{3040} and back into pin 13 to the *I* and *Q* demodulators.

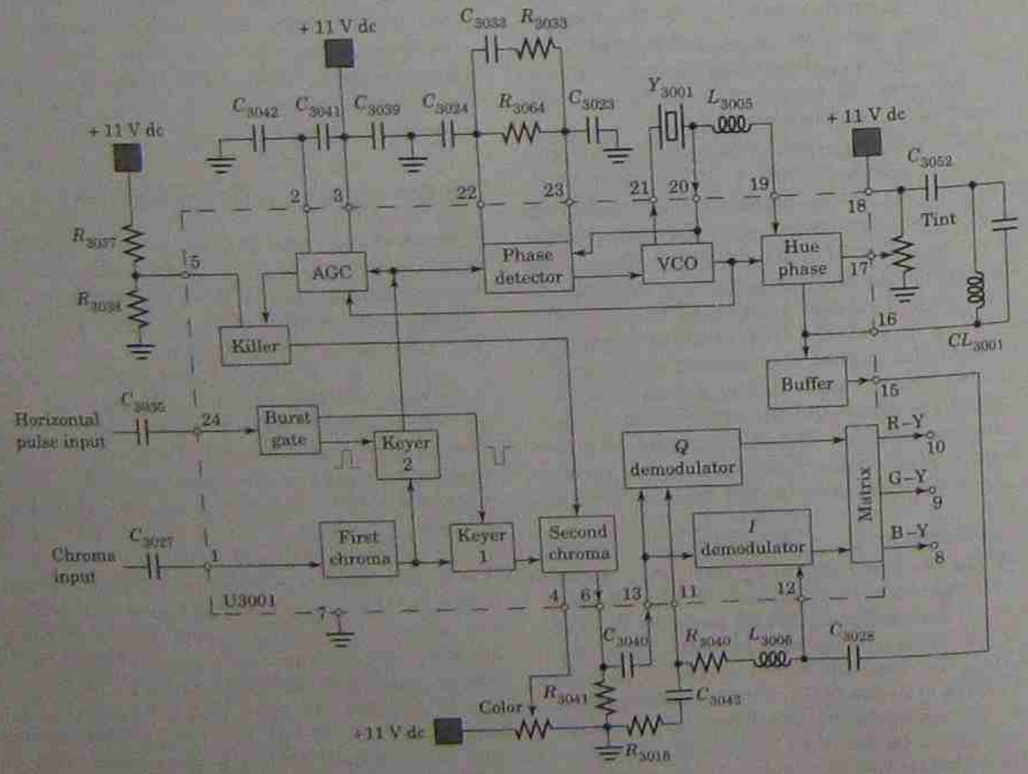


FIGURE 15.17
The internal circuit and external components of the U3001 chroma processor from the schematic diagram.

At the same time, a 4-$V_{p\text{-}p}$ horizontal pulse is applied to pin 24 and into a phase splitter (burst gate) that offers a positive and negative replica of the input signal. The negative pulse is applied to keyer 1 to turn this amplifier off during horizontal retrace time and remove the color sync from the output at pin 6. Compare waves 2 and 13 for this observation.

The output of the first chroma amplifier is also applied to the second keyer. The positive horizontal pulse from the burst gate turns keyer 2 on during retrace time to pass the color sync to the phase detector and the color AGC circuit. The color burst signal, along with a feedback signal from the color subcarrier oscillator (VCO), will establish a dc output voltage from the AGC circuit that is applied to the color killer circuit. The color killer is a comparator that compares the level of dc voltage from the AGC circuit to the level of dc voltage on pin 5. When the AGC voltage is high, in the presence of a color sync signal, the comparator output goes high and turns on the second chroma amplifier for an output at pin 6. A low AGC voltage or an erroneous voltage at pin 5 could hold the comparator low, keeping the second chroma amplifier in cutoff for no output at pin 6. Some receivers have the pin 5 voltage variable, which is called *chroma AGC* or *color killer threshold*.

The phase detector at pins 22 and 23 plus the VCO at pins 20 and 21 form a phase-locked loop (PLL). The subcarrier oscillator signal out of pin 21 passes through the 3.579545-MHz series resonant crystal (Y_{3001}) and back into the oscillator at pin 20. This same feedback signal is applied to the phase detector to be compared to the color sync signal to develop the dc error voltage out of the phase detector that keeps the oscillator on frequency. The VCO output signal is twice fed to the hue phase detector, once directly by an internal connection and again through the oscillator signal into pin 19. These two signals plus the setting of the tint control and the tuning of CL_{3001} will set the 57° phase delay of the subcarrier that is needed for the *I* demodulator carrier signal. The oscillator signal is then buffered and passed out pin 15, through C_{3028}, to pin 12 and into the *I* demodulator. The oscillator signal at pin 12 is phase shifted by another 90° through the lead–lag network of L_{3006}, R_{3040}, C_{3043}, and R_{3018} with application at pin 11 and the *Q* demodulator. Demodulation and mixing are internal functions of the chip that develop the output signals at pins 8, 9, and 10. The carrier at 57° will combine with the chroma to recover the *I* signal, while the carrier at 147° and the chroma signal will combine to recover the *Q* signal. The demodulated *I* and *Q* signals are proportionally mixed to produce the desired color output signals, as described mathematically in Chapter 8. In this case, the outputs are the color difference signals R – Y, G – Y, and B – Y.

The situations that would lead you to suspect a defect in this circuit are seen in photos 6, 32, 33, 34, and 35 of the picture guide series. No color, photo 6, is the most common symptom and has the widest range of possible causes. Some are defective chip, no color, photo 6; open chroma peaker or input network R_{3027}, R_{3058}, or C_{3027}, no color, photo 6 (or weak color); open coupling capacitor C_{3028} or C_{3040}, no color, photo 6; missing horizontal input pulse, no color, photo 6; defective oscillator component at pins 20 or 21, no color, photo 6, or loss of color sync, photo 35; open chroma gain control, too much color, photo 32; on open phase components, wrong colors, photos 33 and 34.

The correct colors are identified and adjusted by viewing the Lissajous phase pattern on the oscilloscope for the NTSC color bar test signal input. This method of injecting the R – Y signal to the horizontal input of the oscilloscope and the B – Y signal to the vertical input of the scope will produce the phase display of Figure 15.18. To set the scope up, remove the vertical signal and set the horizontal gain for 4 cm of width. Reconnect the vertical signal and remove the horizontal signal. Set the vertical gain to 5.6 cm of height (1.4 times the horizontal); then reenter the horizontal signal. For the rainbow

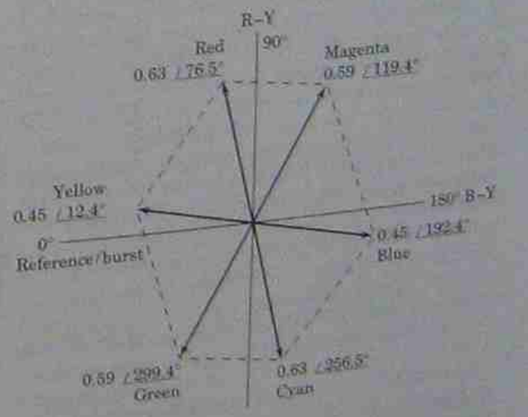


FIGURE 15.18
Vector scope display of the NTSC color bar signals showing relative amplitude and phase.

test pattern, the vertical and horizontal scope displays are the same amplitude. The pattern can be made larger or smaller by adjusting the color control and can be rotated by adjusting the tint control.

Color Output Amplifiers. The color output amplifiers of the schematic include Q_{3006}, Q_{3007}, and Q_{3008} as the mixer (matrix) amplifiers and Q_{5001}, Q_{5002}, and Q_{5003} by color as the output amplifiers. We left the luminance circuit testing (Section 15.5.6), showing that the luminance signal is applied to all three matrix amplifier emitters. We will pick up the discussion where Sections 15.5.6 (luminance) and 15.5.7 (color) left off. Furthermore, the circuit of Q_{3006} and Q_{5001} is exactly the same as the circuit Q_{3007} and Q_{5002} or Q_{3008} and Q_{5003}, with each processing a different color signal. If we can help you to thoroughly understand one of the three amplifier sets, there will be no need to explain the other two sets. The red chain of circuits is used as the example.

Compare Figure 15.19a with the red matrix and red output amplifiers of the schematic and you will see that the only difference is the layout of the circuit. You may recognize that Q_{3006} and Q_{5001} are connected to form a cascode amplifier, as first discussed in Section 6.6 (Figure 6.8). The dc current from the negative terminal of the power supply flows through ground, up through the 4700-Ω emitter resistor, out the collector of Q_{3006}, and into the emitter of Q_{5001}. Then from the collector of Q_{5001}, through the 10-kΩ collector load resistor, plus the few ohms of the 220-microhenry (μH) coil, back to the positive terminal of the 180-V supply. A variation to the typical cascode amplifier is the second current path through the red bias control to the emitter of Q_{5001}. The amount of this current depends on the resistance setting of the bias control. In Figure 15.19b, the transistors are replaced with an equivalent resistance value to show that troubleshooting this circuit is like looking at a series multivalue resistor voltage-divider circuit.

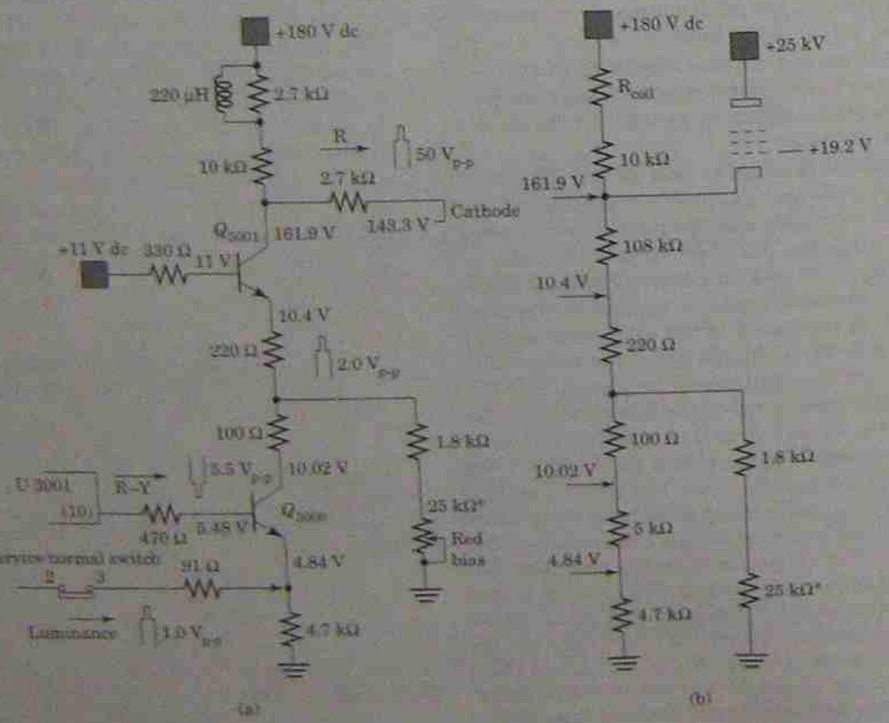


FIGURE 15.19
The red color amplifiers from the schematic (a) arranged to show a cascode amplifier circuit and (b) the equivalent resistor circuit.

For the circuit operation, the luminance signal comes from the service normal switch to the emitter of Q_{3006}. For this signal, Q_{3006} is a base-biased, NPN, common-base amplifier with gain and no phase change. The signal comes out the collector of Q_{3006} and into the emitter of Q_{5001}. Q_{5001} is a base-biased, NPN, common-base amplifier with gain and no phase change. The signal at the collector of Q_{5001} is tied directly into the CRT red cathode. The luminance signal into the emitter of Q_{3006} carries the positive sync polarity characteristic all the way through the circuit to the CRT.

The color difference signal, R – Y for this circuit, leaves the *U*3001 chroma processor at pin 10 and enters the base of Q_{3006}. For color, Q_{3006} is a base-biased, NPN, common-emitter amplifier with gain and phase change. Q_{3006} is not an adder, but a mixer. Do not look for the sum of the two input signals as the output signal.

Let's approach the troubleshooting routine of this circuit from the point of view that it resembles the voltage divider in Figure 15.19b. With these values of resistance, the current through Q_{3006} (5 kΩ) will be about 1.03 mA, which is joined by the 0.376 mA of current through the bias control, to pass 1.406 mA through Q_{5001} (108 kΩ) when the CRT is in cutoff. The CRT control grid, at +19.2 V dc, is 124.1 V negative compared to the cathode at +143.3 V dc, which implies a cutoff state.

If the 10-kΩ load resistor opens, the +180 V dc will no longer be applied to the collector of Q_{5001} and, subsequently, to the red electron gun cathode. The collector voltage drops dramatically, normally to (or near) zero volts. However, as the collector voltage (and cathode voltage) gets lower, the red gun begins to conduct and a current will flow from ground, through the resistor chain, to the red cathode and through the CRT as red beam current. The fixed bias on the base of Q_{5001} limits the current to about 1.5 mA. The internal resistance of Q_{5001} decreases to about 5 kΩ so that the Q_{5001} collector voltage (and red cathode voltage) are maintained at about +22 V dc. The red gun will be on hard, and the picture or raster will have an excess of red, as seen in photos 55 and 56.

If Q_{5001} opens (normal transistor burnout behavior), the signal path to the red electron gun is interrupted, so there is no red in the picture, as seen in photo 43. Furthermore, there is no current flow through the 10-kΩ resistor and no voltage drop across it. With no voltage drop across the 10-kΩ resistor, the red cathode is at +180 V dc and the red gun is held in very deep cutoff, resulting in no red in the raster, as seen in photo 44 (cyan raster). The same conditions hold true if the 220-Ω resistor opens up and will act the same for color or black and white video. When a defect occurs in Q_{3006} or its two immediate resistors (100 and 4700 Ω), there is no red video through this amplifier set (like photo 43). However, because there is still a current path through the red bias control and up through Q_{5001}, the raster may be near normal white.

If the green circuit had been selected as the example, we would have used photo 45 for no green in the picture and photo 46 with the magenta raster. Excessive green would involve photos 57 and 58.

Examine photos 47, 48, 59, and 60 when the defects occur in the blue amplifier set.

The frequency response of the video circuits, from the input terminal V_{in} on the *PW*3000 board to the three cathodes of the CRT, can be tested by the usual sine-wave input at regular frequency intervals or by a single square-wave input signal. The sine-wave signal is measured at the output end of the circuit and plotted on semilog graph paper. The output levels are joined by a smoothly interpolated line to graph the frequency response of the amplifier. The square-wave test proposes a single input frequency at about one-ninth of the highest frequency of interest to be tested. A square wave can be shown to contain a sine wave at the fundamental frequency plus all the *odd* harmonics of that frequency. Beyond the ninth harmonic, the odd multiples add so little to the shape of the wave that they may be omitted. In the color television video circuits, care is taken to remove the color subcarrier frequency at 3.579545 MHz. A 350-kHz square wave contains nine harmonics out to 3.15 MHz and fits our test conditions. Figure 15.20 shows a series of output test results; *a* = the input and ideal output wave, *b* = a slight increase in high-frequency response, or a slight loss of low frequencies, *c* = excessive high frequencies, or a severe loss of low frequencies, as seen in photo 21; *d* = a slight loss of high frequencies; *e* shows a great loss of high frequencies, as seen in photo 20; *f* shows good frequency response with a leading phase shift; and *g* shows a lagging phase shift.

Applying equation 5.1 to the 3.15-MHz frequency response prediction will yield about 230 lines of resolution, which is typical for color television receivers.

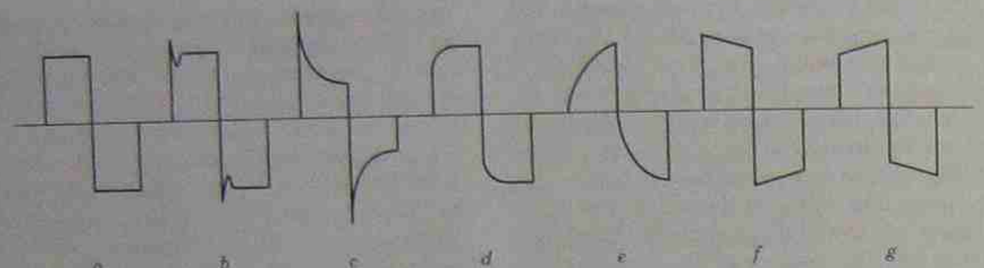


FIGURE 15.20
Frequency response to a square-wave input test signal.

15.5.8 Video IF Amplifiers, Video Detectors, and AGC

This is the first of the high-frequency circuits to be tested in detail, so let's set the stage for this new environment. These circuits will not be found in computer monitors, and the discussion is therefore limited to television receivers only. In the early days of your experience, there could be some doubt about the actual location of the defect, which may be either in the tuner or in the video IF amplifiers. Rereading Section 15.3.4 (raster with no picture, no sound, and no snow) is recommended before continuing on. On the schematic diagram, the circuits at locations 1 through 6 and at levels D and E will contribute to this section.

RF and IF repairs are not normally completed in the home. When you are absolutely sure that the IF amplifier is the cause of the problem, when the active device is accessible without unsoldering the electrostatic shield, when the active device is a plug-in unit, and when you have a replacement part with you, only then would you attempt to repair the IF section in the customer's home in the interest of saving time for you and expenses for the customer. However, if any of the above ingredients are missing, bench repair is the only answer.

On the bench, plug the receiver into the line isolation transformer. Remove the tuner cable from the IF input and replace it with a tuner subber at jack J_1. This will eliminate the tuner and the tuner AGC as a possible cause of the trouble. It will also make the AFT ineffective while providing a known-good test signal. Remove only as much of the electrostatic shield that will allow access to the active device. Try replacing the chip at this time when it is a plug-in unit. Omit this step when the chip is soldered onto the PC board. When replacement does not correct the problem, return the original chip back into service and connect a bias supply to the AGC line, +2.5 V dc at pin 5 of TS_{101} in this case. Measure the supply dc voltage of +22 V at pin 10 and scope the horizontal pulse voltage of +40 $V_{p\text{-}p}$ at pin 9 (wave 3) of TS_{102}. If no picture appears on the CRT, start testing with your oscilloscope at pin 6, the luminance output of TS_{102}. The scope will be useful back to pin 16 at the output of U1-C, the detector output. Defects in the Q_1 circuit can be isolated by scope observations; then measure the dc voltages on the base, emitter, and collector of Q_1 to find the circuit fault. Every test point preceding pin 16 will be at a picture carrier frequency of 45.75 MHz, which may be too high in frequency for the average scope to view. An attractive scope addition is the quadrupler-demodulator probe from Section 15.5.1, shown in Figure 15.12. This probe will allow you to view the signal on the scope all the way back to the IF input terminal, jack J_1. The quadrupler-demodulator probe must convert the high-frequency modulated peak-to-peak signal into a low-frequency video signal that accompanies the quadrupling action. The net result will be about 125-$mV_{p\text{-}p}$ video recovered from a 100-$mV_{p\text{-}p}$ amplitude-modulated carrier signal. Based on these conditions, you may expect to find the following signal strengths through the video IF amplifier section when the receiver is set up as described in the previous paragraph: at J_1, about 125 $mV_{p\text{-}p}$, at the pins of the microchip, 100 $mV_{p\text{-}p}$ at pin 3, 600 $mV_{p\text{-}p}$ at pin 6, 3.6 $V_{p\text{-}p}$ at pin 9, and 3.25 $V_{p\text{-}p}$ at pin 11. An additional stage of amplification and the diode video detector inside of U1-C will put out a direct scope measurement of about 7.25-$V_{p\text{-}p}$ video at pin 16 that is reduced to 6 $V_{p\text{-}p}$ at the luminance output terminal 6 of TS_{102} after going through emitter follower Q_1. These approximations will assist you to find the section of the microchip that is not functioning as intended. The final fault could still be the microchip, or it could be any of the components that support the chip operation. This can be determined by measuring the dc voltages (with no input signal) on the pins of the chip section that is found to be inoperative. *Note:* Do not adjust any of the coils or transformers during this test procedure.

15.5.9 RF Section

The usefulness of a substitute tuner cannot be stressed too strongly when your income depends on fast and accurate solutions to television problems. This is particularly important in light of how television manufacturers develop the different models in their arsenal of products. Excluding portables and specialty models, a specific manufacturer may base the entire year's production on only three model chassis, an economy model, a high-performance model, and a deluxe model. Each chassis may be fitted with a variety of picture tube sizes, to which a number of tuners may be added. The range of tuners spans from the simple mechanical tuner to a push-button tuner, to a remote control tuner, to the electronic multifunction all-band tuner. When you consider that any combination of the above electronic systems may be fitted into a table-model cabinet, a floor-model cabinet or a deluxe console, you can envision over 30 different models on the showroom floor. The point is that the substitute tuner will work to your advantage in 99.9% of the cases. Do not hesitate to use it at every opportunity.

Chapter 13, in addition to examining a cross section of tuner circuits, was instrumental in determining tuner troubles and how to isolate the trouble to a specific circuit. In this paragraph, you will study how to test and repair the defective tuner circuits.

Hold off tuner adjustments or alignment as the last consideration. Measure the dc voltages on the transistor in question; they are marked on the tuner schematic. For RF amplifiers and mixer amplifiers, this is a sure way to confirm if the circuit is working or not. You will need to ensure that the correct dc power supply voltages and bias voltages (AGC and AFT) are present in order that the base, emitter, and collector voltages will be right.

The dc collector voltages are most often applied through a tuned circuit that consumes only a few tenths of 1 V and are therefore not an indication of a working circuit; but make sure that the dc voltage is getting to the collector (or drain). The base dc voltage is generally applied through a voltage divider of some sort, so this voltage is dependent on the voltage-divider resistors. The emitter (or source) dc voltage is developed by the current that flows through the transistor. No current means no emitter voltage, a sure indication that the transistor is not conducting. An open emitter resistor will cause the emitter lead to measure at a small negative dc voltage.

High-frequency oscillator transistors, on the other hand, may be connected to the correct voltages and still not oscillate. The oscillator transistor is biased as a class A amplifier that will amplify its own output signal, thus sustaining oscillations. The tuning of the circuit is based on the interelectrode capacities of the transistor plus a fixed inductor and all the stray capacities in the circuit. As the transistor ages, the interelectrode capacities may change enough that the feedback signal is insufficient to cause oscillations. The dc voltages may still be correct, but the circuit does not oscillate. You can verify this condition by feeding in the signal from an external sine-wave generator to the point and at the frequency that the oscillator feeds the mixer amplifier. Feed the generator signal through a small coupling capacitor (5 pF) at a fairly high signal level, several tenths of a volt peak to peak. The tuner will work correctly with this external signal when the oscillator is the cause of the defect.

On occasion, the oscillator will begin working when you touch the dc meter probe to the base or emitter. It indicates a borderline transistor and, in each of these cases, change the transistor immediately. The same procedure holds true for any of the different frequency range tuners.

Based on your experience, talents, and courage, you may want to limit your first few encounters with tuner repair to the transistors and diodes of the circuits. Beyond that, seek the help of a professional tuner repair group. They may be found in the yellow pages of the telephone book and in all electronic trade magazines. Learn from these transactions by finding out what had to be done to fix the defect.

Your next level of repair should include any or all of the capacitors in the circuits. Electrolytic capacitors require no additional discussion, except to say that they may fault as an open, a short, or as a high-resistance leakage path. Shorted capacitors can be measured with an ohmmeter. Open capacitors can be found by placing a second capacitor in parallel with the open capacitor. Leaky capacitors are found by the parallel method when one side of

the capacitor is grounded and by measuring the dc voltages on both sides of the capacitor when neither side is grounded. The voltage reading on the low-voltage side will be higher than expected when the capacitor is leaky.

Exact capacitor replacement is critical; check the parts list for these specifications. Specifications for a capacitor might be 39 pF, ±5%, silver mica, 100 V, NPO. The 39-pF value with a ±5% tolerance is understood without explanation. The 100-V rating states that the maximum of dc plus peak-to-peak ac should not exceed 100 V. NPO is a temperature coefficient. It reads "negative, positive, zero." It tells you that the change in capacity is zero when the temperature goes up or down. It is sometimes desirable to have the capacity increase in value when the temperature goes up to compensate for other components that also change when the temperature goes up. These are called *positive* temperature coefficient capacitors. It may sometimes be better for the capacitor to decrease in value when the temperature goes up, for the same reasons. These are called *negative* temperature coefficient capacitors. All these selections are made to stabilize the high-frequency circuits.

Resistors may be carbon resistors, ribbon resistors, or film resistors to keep the noise contamination down in a low-noise amplifier. Remember that all amplifiers add noise to the signal. They cannot improve the signal-to-noise ratio, but they can be made to add the minimum amount of noise to the signal. Replace resistors in tuners with exactly the same type of construction.

Return all grounded components to the same ground terminal at which you found them, even though another ground point may seem more logical or convenient. Ground currents can also add noise to the amplifier. Moving the ground to a different location may seemingly make the amplifier work just as well, but it may also produce more snow in the picture.

Your final step as a tuner technician will come when you decide to tune or align the tuner. This advance comes with two precautions: (1) Always use nonmetallic tools to adjust coils, transformers, or variable capacitors. When using metal tools, they look like inductances to the tuned circuit and your hand looks like a capacitor. When you remove them, the circuit is mistuned. (2) Have your signal generator, marker generator, and frequency counter calibrated on a regular schedule. When using the signal generator as a test source in the video IF amplifiers, for example, you want a signal somewhere between 41.25 and 45.75 MHz, so you select 43.5 MHz at the center frequency. It will make little difference if the generator puts out 42.5 or 44.5 MHz; the signal will pass through the amplifier circuit. In alignment or tuning, your generator becomes the standard for the system, and if your standard is wrong, your circuit is also wrong. You could be worse off after alignment than you were before attempting alignment. This is not intended to scare you away from these tasks, but simply to advise you to know your equipment, go slowly, be careful, and be as accurate as you can be.

In almost all late-model television tuners, the fine tuning control has been replaced by the AFT (automatic fine tuning) circuit. This is certainly better for the set owner, but the technician has lost a valuable diagnostic tool.

15.5.10 Sound Circuits

The sound carrier may be separated from the video carrier in the video IF amplifier by a simple resonant circuit tuned to 41.25 MHz. The video and sound carrier signals passing through the video IF amplifiers will heterodyne together, whether we want them to or not. The sum frequency will be 87 MHz (45.75 + 41.25 MHz), and the difference frequency will be 4.5 MHz (45.75 MHz − 41.25 MHz). The schematic shows that the designer's choice was to use the 4.5-MHz sound carrier signal.

Fortunately, the service manual has included the internal circuit for U3002 in the form of black boxes inside a black box. This does not tell us all that we want to know about the circuit, but it does give us a block diagram and signal paths for the system. Figure 15.21 is a combination of the schematic and the internal circuit of U3002.

Tracing the circuit starts at pin 9 of U1-B, the output of the second video IF amplifier. Both picture and sound carriers leave pin 9 and go down to transformer T_2. The tuning of T_2 and T_3 prevent the sound carrier from further progress in this direction. Both the picture and sound carriers leave pin 9 and go up through C_{26} to pin 5 of U2-A. U2-A has a balanced output at pins 6 and 9 into a 4.5-MHz resonant circuit. This is the difference frequency between the two carrier signals, so the sound carrier is accepted and all other frequencies are rejected. The signal at pin 6 of U2-A feeds through the 6.8-kΩ resistor and back into pin 7 (and possibly another amplifier) to come out of pin 3 of U2-A. The sound signal then goes to pin 4 of the plug-in connector and on to the S_o terminal of the *PW3000* board.

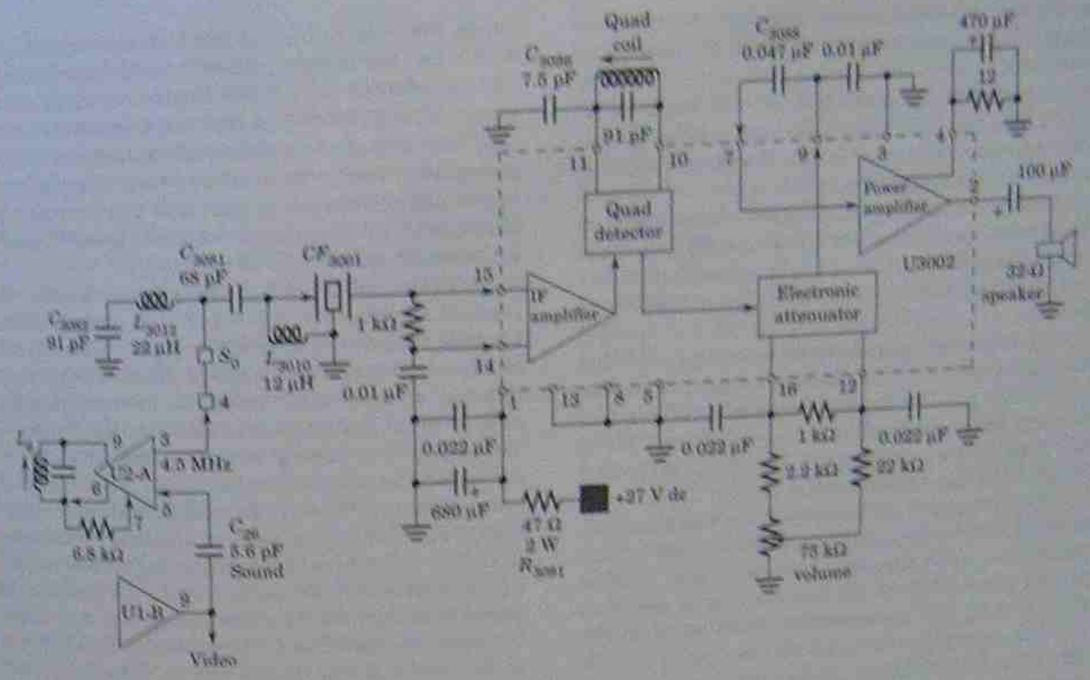


FIGURE 15.21
The complete sound circuits assembled from the schematic and the service manual.

On the *PW3000* board, we run into three filters. L_{3012} with C_{3002} form a series resonant trap at about the color subcarrier frequency. L_{3012} would need to be 21.75 microhenries (μH) in order to be exactly at 3.579545 MHz and is possibly adjusted on the assembly line to trap out this signal. L_{3010} and C_{3001} form a series resonant trap at about 5.57 MHz to remove any high-frequency signals. C_{3001} also couples the sound carrier signal to the crystal filter CF_{3001}, peaked at 4.5 MHz. The sound carrier enters U3002 at pin 15 into what appears to be a differential amplifier. Out of the sound IF amplifier the signal goes to a quadrature FM detector. This circuit works much like the synchronous detector described earlier. That is, when the carrier signal is fed into the detector, part of the circuit begins to oscillate at the carrier frequency, but shifted by 90°, which will be found at pin 10. Off station, when no sound carrier is present, the circuit will not oscillate. The signal carrier and the oscillator signal will heterodyne together to produce the difference frequency, the audio signal. The audio signal is applied to the electronic attenuator to control the volume. Pins 12 and 16 are purely dc voltage adjustments for the attenuator, and no audio signal will be found here. The schematic shows maximum volume when pin 12 is 5.98 V dc and minimum volume when pin 12 is 5.7 V dc. The audio signal leaves the attenuator at pin 9, through the coupling capacitor C_{3088}, and back into pin 7 to the power output amplifier. The output signal at pin 2 goes through a 100-μF capacitor to the 32-Ω speaker. Pin 4 is a frequency tailoring circuit to prevent oscillations in the audio circuit. Pin 4 could be grounded with little noticeable effect on the audio signal.

What did you learn from this discussion and how will it help you to troubleshoot the sound circuits? You should be able to signal trace a 4.5-MHz carrier with your oscilloscope out of pin 6 of U2-A, into pin 7 of U2-A, out of pin 3 of U2-A, and through the crystal filter to pin 15 of U3002. From the output of U1-B (video IF), pin 9, to the input of U2-A at pin 5, the signal frequencies are at the 40+ MHz range and could be beyond the capabilities of your oscilloscope. When you have a picture and find no sound signal at pin 6 of U2-A, then either C_{26} is open or U2-A is defective. It is a simple matter to temporarily replace C_{26} with any small capacitor value in order to isolate the defective part. When

pins have a 4.5-MHz signal out of pin 6 and back into pin 7, but no signal out of pin 2, U2-A again is defective.

A signal at pin 3 of U2-A but not at pin 15 of U3002 tells you that either the crystal filter CF_{3001} is defective or the signal is not reaching the filter. Test the interconnecting points.

A signal at the input of U3002 but no signal at pin 10 tells you that either the sound IF amplifier, the quadrature detector, or the quad coil are defective. Only the tank circuit can be tested individually.

The detector output signal is fed through the attenuator, out of pin 9, through a coupling capacitor and into pin 7 to the power amplifier. These signals are easily observed on the oscilloscope. Make sure that you can change the dc voltage on pin 12 by adjusting the volume control.

The output signal leaves the chip at pin 2, through a 100-μF capacitor, to the speaker. Your oscilloscope will help you here again. The speaker has an impedance of 32 Ω, which will measure about 8 to 12 Ω of dc resistance. Don't overlook the speaker as a possible cause of the loss of sound. Pin 4 can be shorted to ground with only a slight change in sound quality.

There are two other points that should be covered before ending this lesson on troubleshooting. Both are centered around pin 1, the dc supply point to U3002; these points will take you back to your basic electronics. For instance, why are there two capacitors from pin 1 to ground? Their purpose is to remove any 60- or 120-Hz ripple that may still be on the dc power line. Two capacitors in parallel will add together directly, for a total of 600.522 μF in this case. It is thus little different from the 600-μF capacitor alone.

Electrolytic capacitors are constructed by rolling a long sheets of foil, separated by the electrolyte, into a cramped cylinder. The roll of foil will look like an inductor, so the smaller capacitor is added to combat the inductive effects of the larger capacitor.

The second point asks, what kind of an amplifier is the power output amplifier inside of U3002? You might respond that we don't have a schematic of the circuit and, besides, what difference does it make? The difference has to do with the 47-Ω, 2-W resistor R_{3001}. You find this resistor burned open and no dc voltage can get to pin 1, resulting in no output signal. In your parts supply, you find 47-Ω, 1-W and 1-W resistors. Will either of these resistors work to replace the burned out resistor? You next notice that the voltage at pin 1 on the schematic is 25.9 V dc. The supply voltage is stated as +27 V dc, with a difference of a 1.1-V drop across the 47-Ω resistor. This will tell you that there is a little more than 23.4 mA of current through the resistor. Using the power formula (power equals the current squared times the resistance) tells you that there is about 1/40 W dissipated by this resistor, which sounds safe so far.

At the other end of the circuit, the service manual specifies 1 W of audio output power. A 32-Ω speaker with 0.5 W across it would require 125 mA of current through the speaker. For the sake of argument, another assumption can be made that the output amplifier is 66.2% efficient, which means that the power supply must furnish 125/0.662 = 145 mA of current to the microchip. Now 145 mA of current through the 47-Ω resistor will cause it to dissipate 1 full watt of heat at maximum audio output power. The general rule is to use a resistor that can dissipate two times the maximum anticipated power under worst-case conditions. The 2-W resistor is an absolute must. You may also find out that at full audio power output the dc voltage at pin 1 will drop to about 26 V dc due to the increased current.

Now to answer the original question. The dc voltages on the schematic are measured under no-signal conditions. A class A amplifier will draw a constant dc collector current regardless of the volume level. Only a class B push–pull amplifier will draw a trickle current with no signal and increase the current drain as the volume is increased. This is what happened with the 23.4-mA no-signal current and the 145-mA full-signal current. The power output amplifier is then a class B push–pull amplifier. But you may have guessed this when you saw the 100-μF capacitor in series with the speaker.

15.6 LSI SCHEMATIC

Now that you are an experienced schematic reader, Figure 15.22 can be examined with somewhat less hand holding than before. You will want to mark all the active devices on the schematic with one color highlighter and the controls with another color marker. As you do this, you will see that *IC* 1200 appears at five locations, labeled A, B, C, D, and E. Although these five sections are all part of one chip, there are three separate power input terminals, pin 11 in section A, pin 14 in section D, and pin 30 in section E. The other sections draw power from these supplies. The controls to be marked are

the RF AGC, vertical size, width, red drive, green drive, blue drive, screen grid, and the focus controls. This schematic represents a fully automatic remote-controlled receiver. It has six variable functions that are transistors that receive a control voltage from a microcomputer. Highlight the following variables: Q_{1201}, tint; Q_{1202}, contrast; Q_{1203}, color; Q_{1204}, peaking (sharpness); Q_{1205}, brightness; and Q_{1206}, stable display. Except for these modernized changes, the troubleshooting procedure is the same as before.

The tuner schematic for this receiver appears on a separate page in the service manual, and because any number of different tuners may be used, the tuner schematic has been omitted for now. The output from the tuner into the video IF amplifiers is found at the upper-left side of the diagram. The tuner signal comes through a 30-pF coupling capacitor, through a surface acoustical wave (SAW) filter 1/1201, and into pins 8 and 9 of *IC* 1200-A. The output of *IC* 1200-A is at pin 44, where the waveshape indicates a 2.0-$V_{p\text{-}p}$ recovered video signal. This declares that all the video IF amplifiers, video detector, gated AGC, and the automatic fine tuning (AFT) are contained within *IC* 1200-A. Verification of this statement and a service run through will be conducted at the same time. A known good input signal from a substitute tuner or RF signal generator applied through the 30-pF input capacitor C_{1204} will produce an output signal at pin 44 when section A is good. No output signal suggests that you inspect pin 11 first to verify the presence of the 9-V dc supply. Then check the AGC voltage. The internally developed AGC voltage rides on a dc level that is set at pin 10 by the control R_{1201}. Set pin 10 to 5.5 V dc. Measure pin 2 for the voltage range of 5.7 to 8.7 V dc of a working AGC circuit. Either of two capacitor values will be found at pin 2 depending on the current chassis revision. The RF AGC at pin 49, in the range of 5.6 to 7.9 V dc, may be temporarily disregarded if a substitute tuner or RF signal generator is being used as a signal source. The horizontal pulse for the gated AGC originates at pin 6 of the horizontal output transformer and is applied to pin 24 at *IC* 1200-E (see A1 cabling). It then threads through the chip for use at the gated AGC circuits and the chroma circuit, to be discussed later. Verify that a probable 4-$V_{p\text{-}p}$ horizontal pulse (not specified on the schematic) arrives at pin 24 of *IC* 1200-E.

Your next test point when there is no signal output at pin 44 is the VCO terminals 50 and 51. The only video detector to use an oscillator is the synchronous detector that reconstructs the picture carrier at 45.75 MHz. Use a low-capacity scope probe to view this signal. Without a 40+ MHz scope, the 8 V dc at pins 50 and 51 should validate the existence of oscillator signal.

An external video source such as a camcorder may be fed into jack J_1 on the back of the receiver to arrive at pin 40 of *IC* 1200-A. The viewing choice is determined by the dc voltage on pin 43. A binary low (0.1 V dc) at pin 43 sets the AV (audiovisual) function for normal television viewing. A binary high (+5 V dc) at pin 43 will pass the external video to the viewing screen. C_{1205} is a nonpolarized electrolytic capacitor and does not require a specified plus or minus terminal.

The AFT voltage out of pin 47 should measure 0 V when the tuner oscillator is on frequency and the video IF section is in working order. This can be verified by removing one end of R_{1001} while measuring the dc voltage on pin 47, adjust the AFT coil L_{1201}. A plus or minus change in voltage on pin 47 indicates a working AFT circuit. Return the voltage setting back to 0 V and reconnect R_{1001}.

It is assumed that you will check the external components at each of the locations when a faulty function is found and consider changing the microchip only as a last resort.

The standard precautions that go along with testing microchips are advised here and are magnified when working with LSI circuits. A small mistake now could result in a large expense. Never use a meter or scope probe directly on the pins of the chip. Any small movement could cause a short between pins and destroy the chip. Take the measurements on the component lead that connects to the chip pin or on the wiring side of the printed circuit board.

Second, small hairline cracks have been known to form at the junction of the chip pins and the PC board. Inspect these with a magnifying glass and reheat as needed to ensure a good connection.

The heterodyning action of the synchronous video detector will lower all the signal frequencies associated with the modulated picture carrier by an amount equal to the picture carrier frequency. That is, video information in the sidebands of the video IF signal that is 3 MHz away from the IF picture carrier will be recovered as a 3-MHz video intelligence signal.

This also means that the frequency-modulated sound carrier that is 4.5 MHz away from the video IF picture carrier will be recovered as the 4.5-MHz

FIGURE 15.22
(Continued)

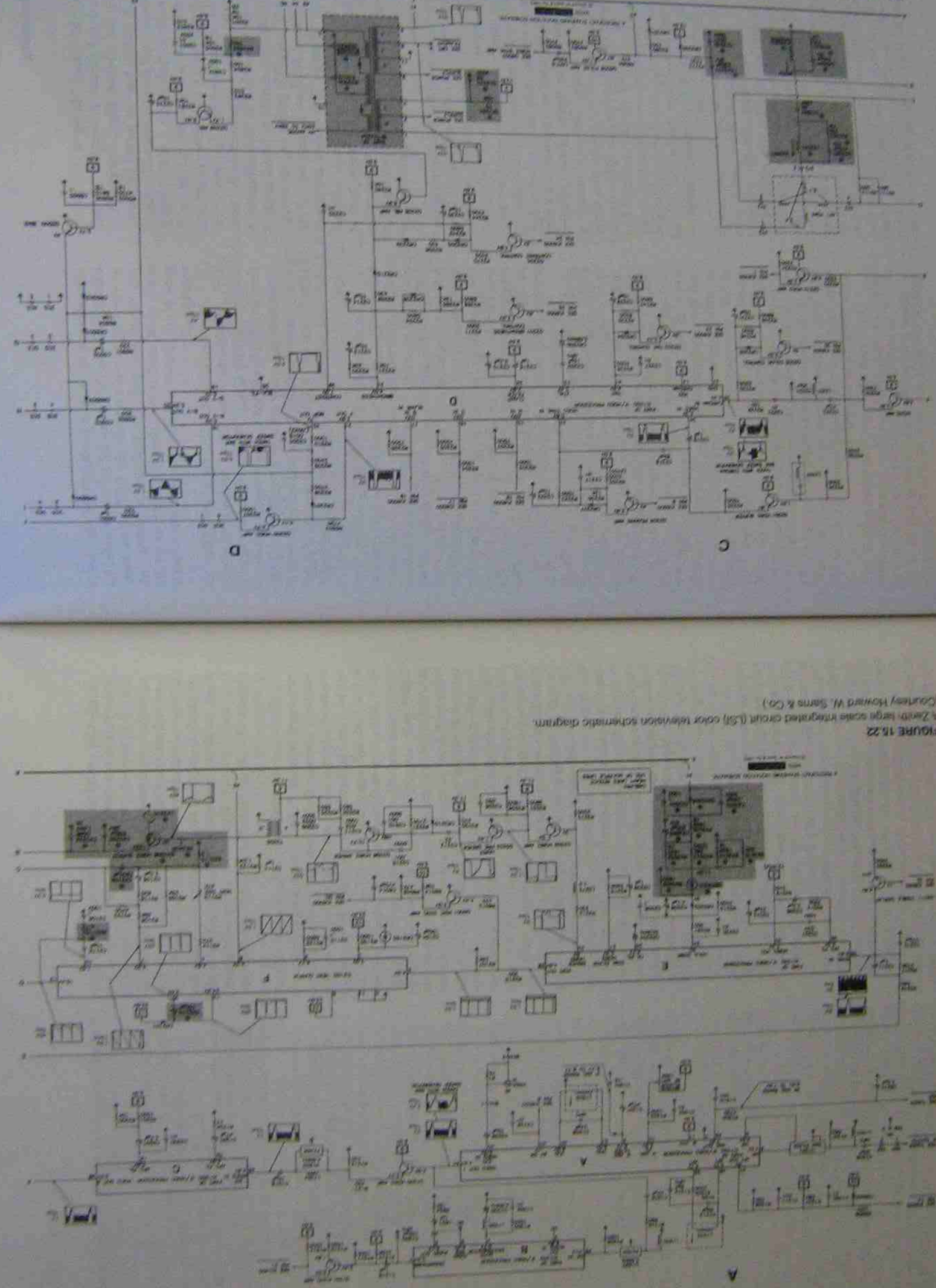


FIGURE 15.22
A Zenith large scale integrated circuit (LSI) color television schematic diagram.
(Courtesy Howard W. Sams & Co.)

sound carrier at the output pin 44 of *IC* 1200-A. From here, the sound carrier is coupled through C_{1215} and *U*1202, the 4.5-MHz filter, into pin 48 of *IC* 1200-B. The B section has the sound IF amplifier, the FM detector, and possibly one audio amplifier, giving an audio output at pin 1 of *IC* 1200-B. The input filter *U*1202 is a sharply tuned bandpass filter. Pin 5 may have a noise filter to ground, depending on the chassis revision that you have. Pin 4 has a 4.5-MHz crystal to ground as the resonant circuit for the 4.5-MHz FM discriminator. A strong 4.5-MHz sine wave should be found at pin 4 when the sound IF amplifier passes the sound signal to the FM detector. All these signals can be observed on your oscilloscope. You should anticipate less than $\frac{1}{2}$-$V_{p\text{-}p}$ audio signal out of pin 1, followed by the audio amplifier Q_{1201} with a possible gain of 1.5 and wide bandwidth to pass the stereo audio signal. The sound section ends here with an indicator to see *IC* 1400. The audio output amplifiers may be monaural or stereo.

Each audio output amplifier version has a separate schematic shown on different pages of the service manual. You would need to use the schematic that matches your receiver. Testing audio amplifiers is usually associated with basic electronics education and is not covered at this time.

Never test a crystal with an ohmmeter! The 1.5-V dc meter supply used to measure resistance will be present across the meter probes and can crack the crystal structure. Instead, connect a 10-kΩ resistor in series with the crystal and apply a signal generator voltage across this series circuit set to about 1 $V_{p\text{-}p}$ at the crystal resonant frequency. Connect the oscilloscope across the crystal set to read about 100 $mV_{p\text{-}p}$. As you change the generator frequency, the voltage across the crystal should peak at the resonant frequency. When no peak is found, the crystal is bad.

Back to the video signal at pin 44 (video out 1) of *IC* 1200-A. The composite video signal goes through Q_{1200}, a 4.5-MHz filter, and into pin 42 of *IC* 1200-C (intermediate video in). The output of *IC* 1200-C is at pin 38 (video out 2). Q_{1200} is an emitter follower (common collector) with a gain of less than 1 that serves as a video buffer amplifier and prevents interaction between any of the three chip sections. The 4.5-MHz filter is connected as a notch filter to stop the sound carrier from any further progress in this direction. The APC filters at pins 12 and 52 appear to be either frequency or phase correction networks. If either of these capacitors shorts, it will kill the video signal. If either of these capacitors is open, it is doubtful that you would be able to tell the difference by viewing a waveshape or viewing the picture on the CRT screen, unless you could see both conditions alternately, good, open, good, and so on. The dc voltages on the four pins of *IC* 1200-C will clue you in on any defects in this circuit.

At video output 2 (pin 38 of *IC* 1200-C), the 1-$V_{p\text{-}p}$ composite video signal enters another video buffer amplifier Q_{2202}. The emitter output signal is then parallel branched to four different circuits, the luminance Q_{2201}; the chroma *IC* 1200-D, pin 36; the tuner buffer amplifier Q_{2210}; and the sync circuit *IC* 1200-E, pin 29. We will start at the top of page C and work downward in order of the circuit appearance.

The video signal out of Q_{2202} goes up to the base of Q_{2201} video buffer. This is the luminance emitter follower that supplies 0.5-$V_{p\text{-}p}$ video signal (negative sync) to pin 34 of *IC* 1200-D. It has a 3.579545-MHz series resonant trap in the base circuit that keeps the color subcarrier out of the *Y* signal system. If the capacitor shorts, you will lose the low frequencies, as seen in photo 21 of the picture guide series. If the trap defaults open, a fine herringbone pattern will be seen in the picture. The pattern is annoying and lessens the quality of the picture, but it will not damage the set.

The luminance signal leaves *IC* 1200-D at pin 21 and is clamped to a horizontal pulse from QX_{3208} horizontal output amplifier (A_3) at the base of Q_{2200}. Q_{2200} is an emitter-follower buffer amplifier. Its output can be traced across the top of page D, then down the left side of page E to the base of Q_{5106}. The emitter output of Q_{5106} goes through the service normal switch and to the emitters of all three color output amplifiers. Except for an identifiable delay line, this luminance amplifier sequence looks very similar to the luminance circuits seen in the earlier chapter schematic. Pin 14 of *IC* 1200-D specifies VDD chroma. It is inconclusive as to whether the same dc supply voltage is used for the luminance circuits in this section. Measure the dc voltage on pin 14 to ensure that nothing is overlooked. We will look at the chroma circuits next and then come back and review the operation for all the other functions of *IC* 1200-D.

The output of Q_{2202} is where the signals were separated. L_{2201} and C_{2234} form a parallel resonant circuit to pass only the chroma signal and to bar all other frequencies from entering pin 36 of *IC* 1200-D. The color output of *IC* 1200-D is at pins 18,

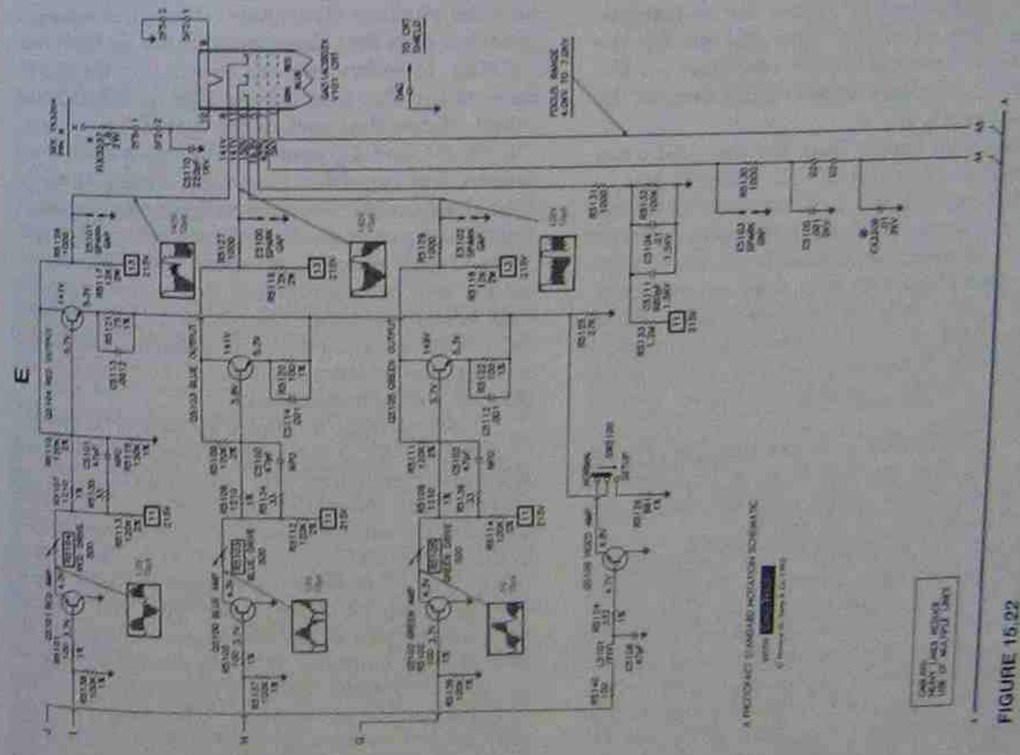


FIGURE 15.22
(Continued)

19, and 20, as the R – Y, G – Y, and B – Y color difference signals. If you take a quick look at Figure 15.17, you will realize that all the circuits described in Figure 15.17 are contained within *IC* 1200-D. Do you remember what you had to look for when troubleshooting the chroma section?

In Figure 15.17 we looked for a chroma signal input and a horizontal pulse input. The minimum effect would be loss of horizontal sync if there were no horizontal pulse into pin 24 of *IC* 1200-E. The worst-case conditions would be no horizontal deflection, no high voltage and no raster, not to mention no AGC and loss of video. Your search for the causes of these problem would not start in the chroma section. The only input signal then is the chroma signal at pin 36.

The next step was to look for the subcarrier oscillator signal. Pin 13 of *IC* 1200-D has a 3.579545-MHz crystal and is surely part of the oscillator circuit. Look for about a 300-$mV_{p\text{-}p}$ carrier signal at pin 13 when the circuit is working. Temporarily replace C_{2202} with any close-value capacitor and check the crystal as described earlier when no signal is found at pin 13. Removing the crystal and substituting a signal generator in its place with about a 300-$mV_{p\text{-}p}$ signal is another way of testing the circuit.

After verifying that a chroma signal is present at pin 36 and that the oscillator is operational, there are no other test points until the three color output terminals, pins 18, 19, and 20.

Using the red amplifier set again, the output signal from pin 18 goes through a small resistor and a nonpolarized coupling capacitor. CR_{2009} sets the dc voltage from Q_{2009} as the bias for Q_{3101}, the red video amplifier. The red drive control adjusts the bias to the red output amplifier Q_{3104}, as well as alters the signal level to arrive at the output amplifier, thereby controlling the contrast of the red signal compared to the other color signal levels.

The luminance amplifiers Q_{2201} and Q_{2106} are dc coupled from the output of *IC* 1200-D to the connection at the emitter of the three color output amplifiers. The color amplifiers are dc coupled from the nonpolarized coupling capacitor and the bias circuit (CR_{2009} for red) to the cathode of the CRT. Be mindful of the service techniques that are used to troubleshoot direct-coupled amplifiers as described earlier in the text.

Pins 15, 16, and 17 of *IC* 1200-D are used for the OSD (on screen display) used for channel change and the bar graphs used for volume, color, contrast, and tint, as well as other menu functions. The signals arrive from the microcomputer on command. You would need to know the color associated with each command in advance of any testing. The best command is menu select, which will display several functions, each in a different color. When the menu command is executed, all three inputs can be tested at one time for the full minute that the display is on screen.

The control functions of *IC* 1200-D that remain are color gain, color tint, contrast, brightness, and the peaking (sharpness) controls. A schematic notation says that these controls are set for normal viewing; therefore, we can expect that the dc voltages on the chip pins may be slightly different than noted. Notice that each of the control lines (pins 31, 33, 36, 39, and 41) connects through a resistor to a large-value capacitor to ground. This is to ensure that the dc control voltage will not change with instantaneous changes in ac signal voltage. The operation of each circuit is identical; therefore, only one circuit will be examined with the understanding that it represents all the circuits. Q_{2205}, the color gain control, is used as the example and is compared to the brightness circuit of the schematic as a discrete circuit comparison.

Look at Q_{2205} in Figure 15.23 and its collector load resistor R_{2248} as a start. When the base voltage is lowered, less current flows through Q_{2205} and the resistor. The voltage drop across R_{2248} is less and the collector voltage rises. Q_{2205} can be compared to a variable resistor that would cause the same effects. When the collector voltage changes, the dc voltage at pin 36 changes also. This entire assembly could be part of the bias voltage divider for the first chroma amplifier, noted in dashed lines inside *IC* 1200-D. Figure 15.23b is the brightness circuit of the schematic at location E. Changing the brightness control changes the base voltage of Q_{3009}. The change in collector voltage of Q_{3009} changes the base voltage of Q_{3010} and the dc voltage to the CRT, changing the brightness. Q_{2203}, Q_{2204}, Q_{2208}, Q_{2206}, and Q_{2207} on the schematic will all change the dc voltage on their associated pins when a base voltage change arrives from the microcomputer.

Figure 15.23c shows the collector characteristic curves to remind you that a voltage drop of less than 1 V across the transistor will place the transistor in a region of unpredictable operation. A very small increase in base voltage could result in this operating mode. Furthermore, bar graphs with 16 levels of variation mean that the base voltage will change in small steps for each change in bar graph count. The base voltage variations come from the microcomputer.

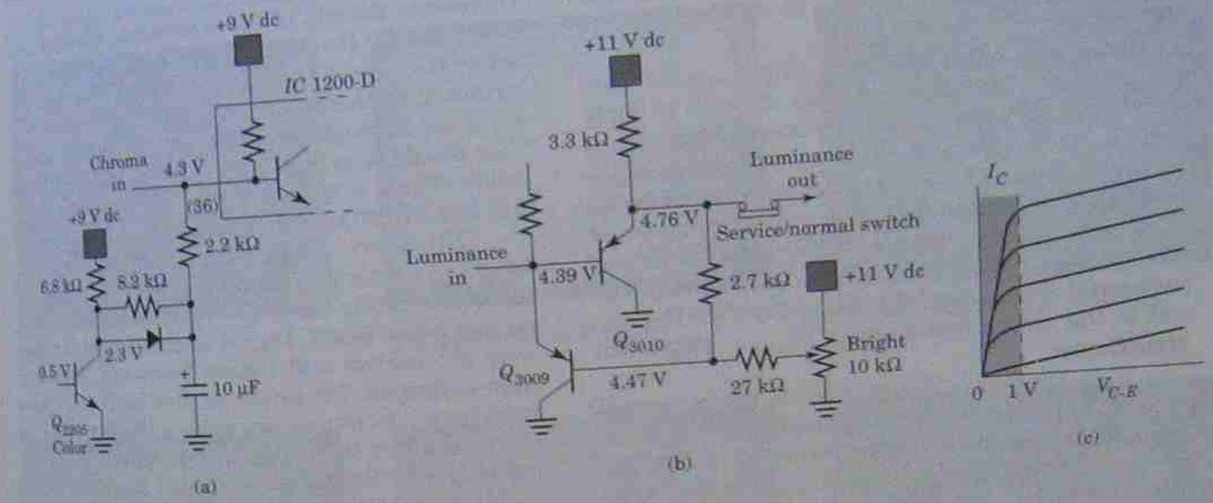


FIGURE 15.23
Solid-state control functions: (a) the color control circuit from Figure 15.22; (b) the brightness control circuit from the schematic; (c) typical collector characteristic curve.

The third destination for the output of Q_{2202} is Q_{2106}, simply called the video amplifier. Its output directs you to *IC* 6200, which is the tuning circuit for the microcomputer. The horizontal and vertical sync signals are used by the computer for on-screen displays and other similar functions.

The last destination of the video signal out of Q_{2202} is the sync section of the LSI at *IC* 1200-E, pin 29. The prime terminals of interest for *IC* 1200-E are the input (pin 29), the horizontal pulse input (pin 24), the countdown oscillator (pin 25), the horizontal output (pin 23), and the vertical output (pin 28).

IC 1200-E contains all the circuitry shown in Figure 7.5 and described in Section 7.5. The 503.5-kHz crystal oscillator is divided down by 32 to 15,734 Hz to work with the VCO as the horizontal-deflection oscillator. The 503.5 kHz is divided down by 16 and by 525 to produce 59.94 Hz in the vertical section. The sync separator, the differentiating and integrating filters, the vertical deflection oscillator, the automatic frequency control, and the horizontal-deflection oscillator are all part of this LSI section.

First look for the dc voltage input at pin 30 and then the signal waveforms in the following order: the horizontal feedback pulse at pin 24, the video input at pin 29, the 503.5-kHz oscillator signal at pin 25, the vertical output at pin 28, and, finally, the horizontal output at pin 23. The 503.5-kHz crystal oscillator is the originating point for the horizontal-deflection signal and the vertical-deflection signal and is active all the time, on or off channel. Defects that resemble photos 15, 16, or 17 can be traced to *IC* 1200-E.

The components that contain an X in the part number are sensitive to the X-ray protection of the receiver. These parts are also shown in the shaded areas so that they cannot be overlooked. When found to be defective, they should be replaced by components that are recommended by the manufacturer.

IC 2100 is the vertical output amplifier section. The dc voltages to this section appear at pin 1, 23 V reduced to 7.5 V, and at pins 8 and 13 at the full 23-V dc level. The output at pin 23 goes directly to the vertical-deflection yoke terminal 4 at plug 3Y3. The yoke return is at terminal 3 of plug 3Y3 and comes back to pin 7 of *IC* 1200-E for linearity. The same return signal is passed through the series resistor R_{2112} for vertical size (height) to pin 4. When the measured voltages on pins 4 and 7 do not compare favorably with schematic voltages, the nine components in this feedback system should be measured carefully and individually. The voltage wave across RX_{2115} (not shown) is a good place to check for vertical linearity, although both pins 6 and 7 show a linear waveshape. R_{2111} and R_{2113} are

vertical damping resistors. Picture problems that compare to photos 7, 8, 9, and 10 will be traced to this section.

The horizontal oscillator output signal from pin 23 of *IC* 1200-E progresses through a fairly conventional horizontal-deflection circuit. Q_{3209} and Q_{3202} are typical direct-coupled common-emitter amplifiers. The associated waveforms make them easy to troubleshoot. The collector resistor of Q_{3209} is part of the voltage-divider network for the base of Q_{3202}, to be examined when testing. The horizontal driver amplifier Q_{3206} supplies the signal to the driver transformer T_{3205}, a step-down transformer.

T_{3205} secondary signal is fed to the horizontal output amplifier QX_{3208}. The damper diode is an integral part of the output transistor and does not have a separate part number. L_{3210} is a toroid coil that acts like a large ferrite bead. It is used to control parasitic oscillations in the horizontal output amplifier. The collector output signal of QX_{3208} goes directly to pin 1 of plug 3Y3 and the horizontal-deflection coils. The yoke output is at pin 2 of plug 3Y3, which goes through a linearity coil and then through the width coil to ground. Problems represented by photos 11, 12, and 13 can be traced to this section. The horizontal output signal also goes to pin 1 on the high-voltage transformer TX_{3204}. No waveform is given for this connection, but measurement of the signals at pins 6 or 8 will verify that the horizontal-deflection amplifiers are working.

The low-voltage power section is a switching power supply like the one discussed in Section 15.3.5 and shown in Figure 15.10. Part of the high-voltage transformer is found on the low-voltage power supply diagram (not shown) for this receiver. It is drawn separately and shaded to attract your attention to the electrical significance in the system. It identifies that the 215-V dc source and the 23-V dc source are both scan-derived voltages.

More than one-half of no raster, no sound problems will be traceable back to horizontal countdown and scan-derived voltage sections of the receiver.

15.7 CONCLUSIONS

It is not at all surprising that the schematic and Figure 15.22 have so much in common. The schematic represents the end of one generation, whereas Figure 15.22 is the start of the next generation of schematics over a short period of time. The block diagram and schematic have a standard layout pattern, and although there will continue to be changes, they should be gradual enough for any individual to follow. There is no guarantee what the schematics will look like 20 years from now.

The devices and circuits have seen improvements over the years, but the functions have remained basically the same. Color has been added, as was stereo sound. Digital electronics have taken over the control and tuning functions, and now high-definition TV looms on the horizon. There have been adventures into various display schemes (covered later) that bring new possibilities to the industry, but they are all somewhat familiar.

This chapter is an intensive effort to cover the widest variety of trouble symptoms and cures that could be to your benefit. The receivers from the schematic and from Figure 15.22 have over 450 electronic components each. And even if each part failure was explained, it would cover only two receivers. Not every possible problem could be included.

Although the testing procedure is fairly routine, it is limited to sight and sound observations and then whatever electrical measurements that you can add to the information stockpile. The electrical measurements will come from the oscilloscope waveshapes of signals (natural or injected), the dc voltages, and the dc resistances. A decision is made after each new bit of information is added, which will point you toward the defective component. But you cannot make these decisions only from memory. It is hoped that the depth of this chapter will encourage you to *think* as you analyze the problems. It is essential to know what the product is intended to do. You should be aware of how these tasks are generally accomplished within the product. Then you can apply your understanding of basic electronic circuitry. In this manner, you will progress and succeed in your chosen area of electronics.

Picture Guide to Television Trou[illegible]ooting



1. No raster.



2. Clean white raster only.



3. Raster with noise (snow), no picture.



4. Poor color purity.



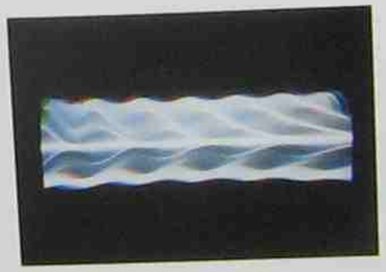
5. Good color picture.



6. Good black and white picture (no color).



7. One bright horizontal line.



8. Oscillations in the vertical yoke.



9. Short raster.



10. Poor vertical linearity with foldover.



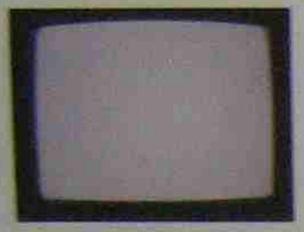
11. Horizontal keystone.



12. Narrow raster.



45. No green in color picture.



46. Magenta raster.



47. No blue in color picture.



48. Yellow raster.



49. Weak and snowy picture.



50. Ghosts.



51. Radio frequency interference (RFI).



52. Overloaded video IF amplifiers (AGC).



53. Silvery picture.



54. Poor focus.



55. Red raster only.



56. Monochrome video on red raster.



57. Green raster only.



58. Monochrome video on raster.



59. Blue raster only.



60. Monochrome video on blue raster.

These images do not reflect the quality of the original content or program but rather are simulations of problems or conditions encountered in television troubleshooting.

16 Light Exchangers

16.1 INTRODUCTION

We need a device at both ends of the video system that will take us from the real world into the electronic world and then back out again to the real world. The inputs are called *pickup* or *image-sensing* devices. At the output end, they are called *display* devices. Common sense tells you that, over the years, more than one of each device has been developed. You are already familiar with one of the devices at the receiving end called the CRT, so let's complete that segment and then cover the pickup devices later.

The RCA model 630TS television receiver hit the market around 1949 with a 10-inch round picture tube having a length of about 14 in. Other receivers at that time had 3- and 5-in. round picture tubes. The goal was to produce larger screens without increasing the CRT length and eventually to develop a flat-pack screen that would hang on the wall like a portrait. The goals are still the same today.

The length of the CRT could be shortened by increasing the deflection angle to the limits of acceptability. From 114° to 120° deflection angle tubes were developed that maintained the length of 12 to 14 in. and a diagonally measured screen size up to 36 in. Beyond this point, linearity and the addition of color became the limiting factors.

16.2 PROJECTION SYSTEMS

The two-piece projection system was first developed for movie theaters and then downsized for home use as shown in Figure 16.1a. The projector was a standard receiver circuit, except that the color video output amplifiers drove three separate high-intensity cathode ray tubes, one for each color. Because each CRT handles only one color, there is no need for a shadow mask inside the tube, resulting in a higher brightness level than for the trinitron CRT alone. Three separate CRTs used three separate deflection yokes and each had a size, linearity, and centering control that had to be set up identically in the vertical and horizontal directions. Then the three tubes were mechanically adjusted to overlay the three pictures exactly or a condition like misconvergence would result. Each CRT is fitted with a special focusing lens to concentrate all the light in one direction, and the high voltage was increased to 30 or 40 kilovolts (kV) to compensate for the projection distance. Viewing areas ranging from 3 by 4 ft to 6 by 8 ft can be projected onto a curved lenticular screen across a darkened room. Lenticular screens are coated with clear crystal beads that reflect light five times better than a flat, white, matted screen.

The one-piece projection receiver seen in Figure 16.1b has all the same specifications as the two-piece unit. The major difference is that the one-piece unit has a single high-intensity color CRT. This means that the shadow mask is back inside the CRT, and the high voltage had to be stepped up once again. The CRT again has a focusing lens to concentrate all the light in one direction. A special CRT called the Schmidt projection tube has the lens built into the CRT envelope and is common in one-piece projection receivers.

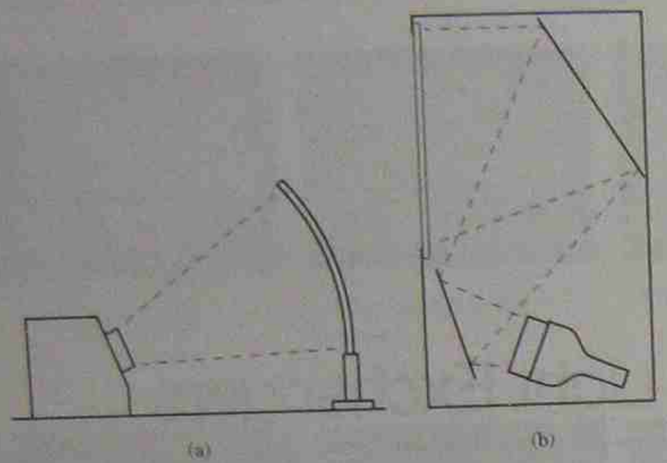


FIGURE 16.1
Projection television receivers: (a) two piece; (b) one piece.

Servicing projection receivers differs only by the mechanical setup of the parts. A word of caution: in some receivers the yoke wires are reversed to account for the image inversion with certain models for both the vertical and horizontal direction. This can be a last-minute check at the end of the service routine.

The advantage of projection television is large-screen pictures, approaching life size. The disadvantage is that they must be viewed in low ambient light, although there are improvements in this area on later-model receivers. The viewing angle is still restricted to about 30° each side of center (60° total), where the brightness falls off to an unviewable picture. Direct-view CRT screens are still bright enough at 75° off center (150° total). The costs of projection receivers are two to three times higher than a direct-view receiver, but that's a personal option.

16.3 LIGHT-EMITTING DIODES

A great deal of experimentation is still going on in this discipline. The major problems are threefold: (1) The chemicals that go into LEDs do not color match the NTSC standard colors. Green is best, with red and blue far enough off the correct hue to make the secondary colors difficult to achieve. Because of this, a good gray scale is not obtainable. (2) LEDs consume from 0.5 to 5 milliamperes (mA) per pixel. In a 680 by 480 pixel matrix, the total current is quite high and the light output is still below a desired level. Increasing the diode current to bring up the brightness exceeds the power dissipation of the LEDs. (3) The off-center viewing angle, although much better than for projection receivers, is still substandard. On center axis, the LED display is comparable to the CRT display, except for the color rendition. At 45° off center axis, the colors of the LED unit change as compared to the CRT unit, which remains almost unchanged. At 60° off center, the colors of the LED unit are badly misrepresented, and the brightness level is down by a considerable margin, compared to the CRT unit. However, the performance of the LED challenges the performance of the CRT, and there is a high degree of expectation for the LED display in the near future.

The term **pixel** is used extensively in these paragraphs; therefore, it is wise to know exactly what the term means as it is used. A pixel is an area that can be any size or shape that we choose to make it. It may measure 0.5 micrometer (μm) in one case and 50 μm in the next case. It is our attempt, however ill conceived, to divide a solid line into segments without further definition. Pixels were born when we compared the performance of a solid-state display to the performance of a CRT.

In Section 5.14, we explained lines of definition as the number of on–off cycles that could be achieved during one active horizontal scan line of a television picture or computer monitor picture. We concluded that quality television had 309 lines and computer monitors had 1103 lines. Each line of resolution had an on period and an off period, so one scan line for television has 618 on–off half-cycles. The 4:3 aspect ratio then dictates that we need 464 lines of vertical resolution.

A solid-state array needs a 618 × 464 matrix in order to perform comparably to a quality CRT performance. The size of each of the 286,752 pixels would now depend on the size of the CRT screen. The pixels of a 25-in. diagonal screen would be about 0.00105 in. in size, while the pixels on a 13-in. diagonal screen would be about 0.000283 in.

16.4 LIQUID-CRYSTAL DISPLAYS

When a liquid-crystal material is heated above its melting point, it will reach a highly ordered state called **mesophase,** which has some of the properties of a crystalline solid, while retaining the flow properties of a liquid. In this state, the liquid-crystal molecules are rodlike, with a 3:1 length-to-diameter ratio, and contain polar groups that establish the forces to orient the molecules into alignment. The liquid crystal is sandwiched between two glass plates. Certain chemical substances deposited on the outside of the plates will align the long axes of the molecules of the liquid crystal to be parallel with the surface of the glass plates. During assembly, the long axes of the molecules at the top plate are oriented to be parallel, but rotated by 90° with respect to the direction of the molecules at the bottom plate to create a spiral column of rods between the plates as seen in Figure 16.2a.

A polarizer is placed on top of the cell and oriented to allow polarized light to enter the cell and follow the spiral path across the cell. A second polarizer placed behind the bottom plate allows the light with the altered polarity (from the spiral rod twist) to pass out of the cell. The cell then appears as light to the observer.

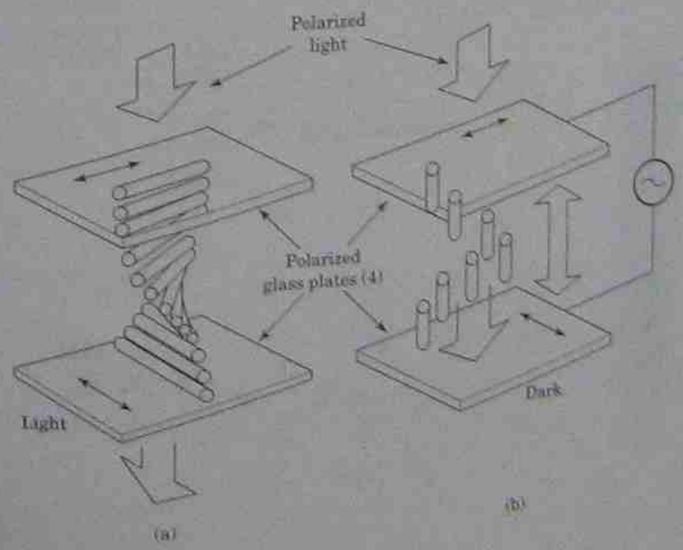


FIGURE 16.2
Liquid crystal display (LCD) structure: (a) aligned to pass light and (b) aligned to block light passage. The thick headed arrows represent the polarized light. The double headed thin arrows indicate the polarization of the glass. The thick double headed arrow shows the polarization of the applied electric field.

The mesophase structure can be altered with the application of an electric field that affects the transmission of polarized light passing through the liquid-crystal material. When an electric field is applied to the cell, the molecules are realigned so that their long axes are parallel to the direction of the electric field. See Figure 16.2b. The polarized light entering the cell is no longer twisted and will not pass through the second polarizer. The observer will see a dark screen.

Computer monitors that use LCDs cannot be operated in the dark, so for daylight use the polarization is arranged to reflect the ambient light and the observer will see white. The data become the applied electric field to absorb the light and the observer will see black (or dark).

Note in Figure 16.2b that the applied electric field is an ac voltage. In television, the applied electric field is the video signal with the blanking and sync pulses representing black. Varying the amplitude of the video signal (elements of the picture) will set up shades of gray between full white and full black. Because television may be viewed in daylight or in the dark, a trap door on the back of the receiver is opened to let in ambient light for daytime viewing, and the screen is backlighted with a fluorescent lamp for viewing in the dark.

16.5 PICKUP DEVICES

Television picture scanning started with a revolving mechanical disk, but soon changed to electronic

systems. The first camera tube was the image dissector, followed soon by the iconoscope, which you can see in museums. The image orthocon followed next in order and is still used in only the highest-quality studio equipment.

16.5.1 Image Orthocon

The light image from the scene passes through the lens and is focused on the photocathode of the tube in Figure 16.3a. The photocathode emits an electron image that is attracted across the sealed image section of the tube to the more positive target, and deposited on the front surface of the glass divider. The beam current from the electron gun at the base end of the tube is accelerated toward the target area. Just prior to reaching the target, the electron beam is aligned parallel with the length of the tube and decelerated for a soft landing on the target. As the electron beam is scanned across the target, it neutralizes the microscopic area charges on the target that were placed there by the photocathode electron image. The scanning beam gives up some of its electrons in the neutralizing process that causes changes in the beam current to be used for developing the output signal. The electron beam has no place to go at the sealed target end of the tube. The negative electrons are attracted by the positive potential along the inside coating of the tube and are turned around to start their journey back through the tube along the same path as the forward electron beam. At the cathode end, they are attracted by the higher positive potential on the dynodes of the electron multipliers. The electron multipliers are a series of five dynodes, in this case, each having a higher positive potential than the one before it. As seen in Figure 16.3b, for each electron that lands on dynode 1, a total of three electrons, in this example, is released from dynode 1 and attracted by the more positive potential on dynode 2. The second dynode releases electrons at the 3:1 ratio that are attracted to dynode 3, and so on. A current gain of 81 is achieved in this electron multiplier ($1 \times 3 \times 3 \times 3 \times 3 = 81$).

With the lens cap in place, no electron image is deposited on the target. The electron beam current is maximum, called *dark current*, and has a value of about 0.06 microampere (μA). When the target is fully illuminated, the neutralizing action reduces the beam current to about 0.0475 μA. The difference between these two values, 12.5 μA, may seem small, but when multiplied by 81 and passed

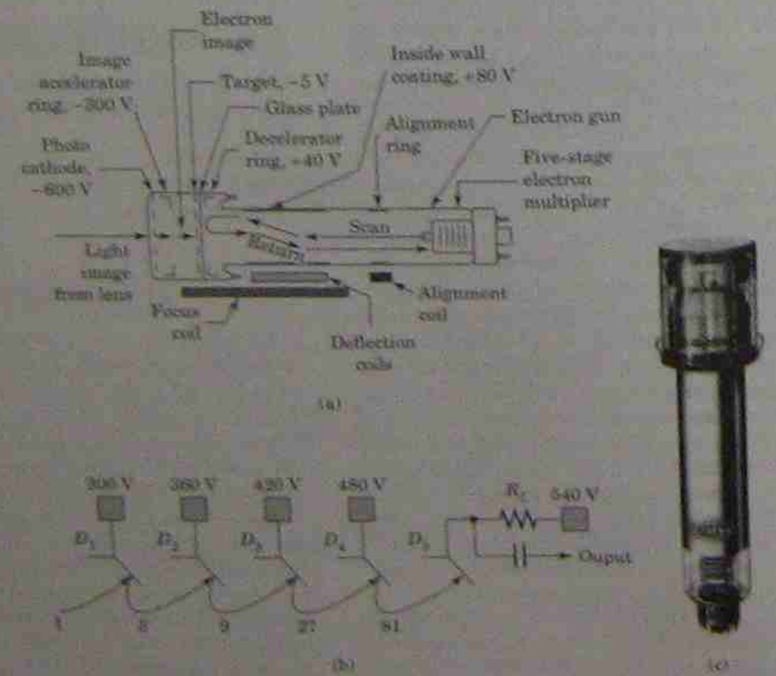


FIGURE 16.3
Image orthocon: (a) internal construction, (b) 5 dynode photo-multiplier (c) external illustration.
(Part (c) courtesy Thomson Consumer Electronics, Inc.)

through a 500 kilohm (kΩ) load resistor, it will develop about a $\frac{1}{2}$ volt (V) p-p output signal. The only disadvantage is that achieving this high output signal voltage takes about 150 footcandles of light on the photocathode. That's about 50 lux, in today's camcorder language.

16.5.2 Vidicon Family

The vidicon camera tube was developed to replace the much larger image orthocon tube. The original tube was 1 in. by 8 in. and was reduced in stages down to $\frac{1}{2}$ in. by 4 in., without changing the principle of operation. Vidicons are lighter in weight, smaller sized, operate at much lower voltages, have 600-line resolution capabilities, and require only 1 footcandle of light for full output signal level. The output signal is only 20 millivolts (mV) p-p compared to the $\frac{1}{2}$ $V_{p\text{-}p}$ from the image orthocon.

The vidicon used selenium or antimony for the target material, which acts like a variable resistor. In Figure 16.4a, the current path from ground goes through the cathode and the vacuum of the tube, through the target resistance, out of the tube, and through the load resistance to the positive terminal of the power supply. The image light falling on the target changes the resistance of the target between 2 and 20 megohms (MΩ), with bright light representing the smaller resistance. Therefore, any change in target resistance caused a change in beam current and output voltage. A dark current of 0.02 μA through a 50-kΩ load developed 1 mV at minimum signal. Maximum bright current of about 0.4 μA represents about 20 mV of signal, or about $(20 - 1)$ 19 $mV_{p\text{-}p}$ output signal, with black as the positive peak of the signal.

The plumbicon and epicon are two variations of the vidicon camera tube. The tube construction and operation are identical to the vidicon except that the target materials are different.

The plumbicon uses a thin layer of tin oxide (SnO_2) on the glass inside surface, covered with a layer of lead monoxide (PbO), and then a layer of doped lead monoxide (doped PbO) forming a PIN diode. The diode conduction changes the beam current for each microscopic point on the target surface in accordance with the light intensity on that point at that time. The change in beam current through the load resistor represents the output signal voltage. The dark current of the plumbicon averages about 4 nanoamperes (nA), and the white current of about 0.3 μA is achieved with 0.8 footcandle of light on the target. The doped lead monoxide layer can be modified to be more sensitive to red, green, or blue light for color cameras that use the three-tube system, as described in Chapter 8.

The epicon target layers are made to look like light-sensitive silicon diodes and operate like all other vidicons in every other respect.

16.5.3 Charged-coupled Devices

The basic concept and operation of charged-coupled devices (CCDs) are simple and straightforward. They are self-scanning and work on the principles of a series of vertical shift registers plus one horizontal shift register. They use the pixel format and are the first real contribution of digital electronics into the world of analog electronics. Figure 16.5

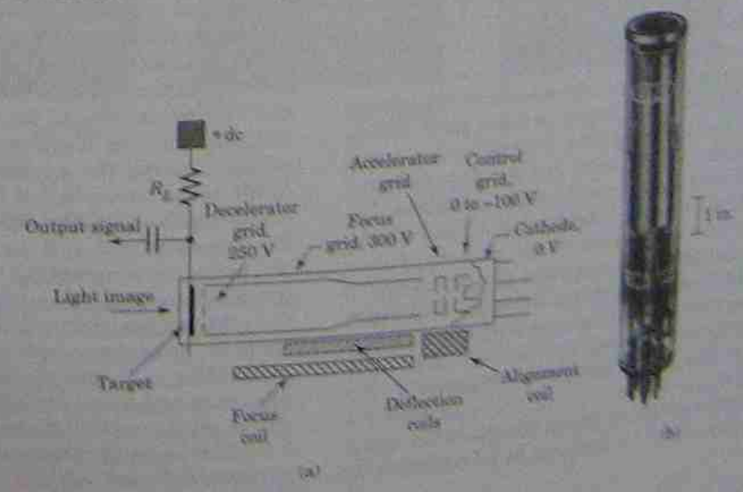
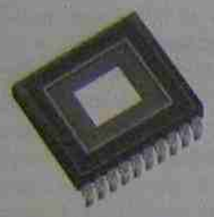
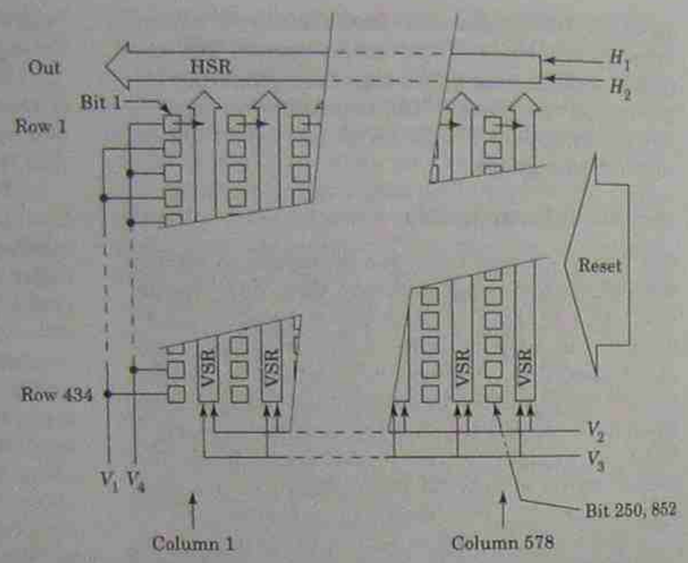


FIGURE 16.4
Vidicon tube: (a) internal construction; (b) external illustration. (Part (b) courtesy Thomson Consumer Electronics, Inc.)

FIGURE 16.5
Charged-coupled device (CCD): (a) photo, 1 in.^{2}; (b) internal block diagram. (Courtesy Thomson Consumer Electronics, Inc.)



(a)



(b)

shows a typical internal block diagram for the MN3734F charged-coupled device. This is a 250,000-pixel array on a ½-in.^{2} surface with a 4 : 3 aspect ratio of 578 × 434 elements.

Light falling on the photodiode area, noted as squares in Figure 16.5, accumulates a charge dependent on the light intensity over each specific area. During the vertical blanking time and at a field rate, V_3 or V_4 downloads the charges from the diodes into the respective vertical shift registers. In this example, V_4 controls the *odd*-numbered rows, corresponding to the odd-numbered scan lines in the NTSC system. V_3 is inhibited at this time. V_2 and V_3 clock out the (434/2) 217 bits of data from all 578 vertical shift registers, one line at a time. The transfer of data from the vertical shift registers to the horizontal shift registers takes place during the horizontal blanking time. During the horizontal scan time, H_1 and H_2 clock out the data from the horizontal shift register to the video amplifiers. The next vertical blanking time inhibits V_4 and sets V_3 to download the even-numbered packets of data into the vertical shift registers as the second field of video. The reset pulse is applied to all shift registers to remove any residual charges, allowing each shift register to start with a clean slate. The downloading of the shift registers are triggered by the sync pulses.

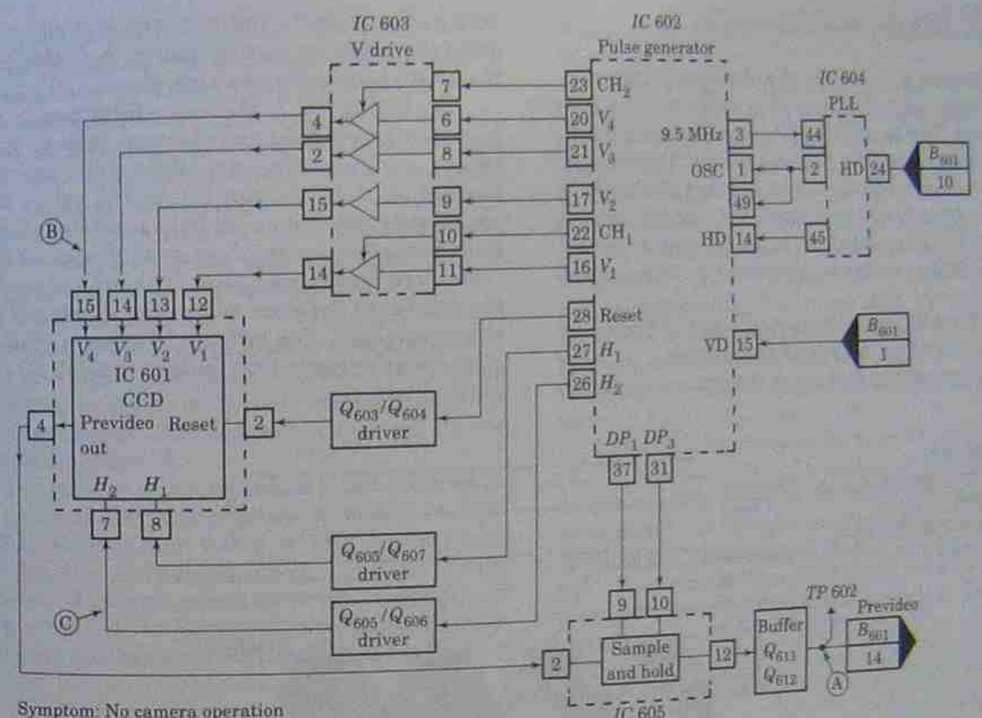
In the scanning cycle, we started at the upper-right corner of the CRT screen and finished at the lower-left corner of the screen. The CCD energy packets must be sequenced to leave in the same order. Bit 1 is the first packet to exit the horizontal shift register, and bit 250,852 is the last to leave.

Figure 16.6 is a typical CCD drive circuit. It should be noted that, historically, CCDs are extremely rugged and rarely fail. Be advised to check all the drive signals first before replacing the CCD. The CCDs are shipped with a protective cover over the light-sensitive element array. This cover should remain in place until the last possible moment, and then do not touch the array itself, as skin oils are harmful to the array surface.

The pulse generator *IC*602 has two input signals, the horizontal sync pulse to pin 24 of the PLL and the vertical sync to pin 15. The pulse generator will stop working if *either* of these two signals is missing, giving the appearance of a failed CCD. *IC*604 is the phase-locked loop that is part of the 9.535-megahertz (MHz) oscillator in *IC*602. Check the signals at pins 1, 3, 14, and 49 to ensure that the oscillator is operating. The exact frequency of the oscillator depends on the number of pixels in the array and should be of less concern at this time than the presence or absence of the signal. The 9.535 MHz is divided by 606 to get the horizontal frequency and then multiplied by 2 and divided by 525 to get the vertical frequency.

The pulse generator operates at TTL levels, typically 0 V and +5 V, which are not suitable to drive the CCD. These output signals are converted to +13, +1, and −7 V by the driver amplifier circuits. The voltage from CH_1 inhibits V_1, and the voltage from CH_2 inhibits V_4. When viewed on the oscilloscope, all input signal waveforms can be easily identified and the video output signal is the standard waveform. Wave B in Figure 16.6 shows V_4 as a positive spiked voltage of 6.4 V. The wave at V_3 is identical to the wave at V_4, while waves V_1 and V_2 are negative spiked voltages of the same magnitude and frequency.

Check the B+ voltage first, then the horizontal and vertical input signals, and then the seven driving voltages. Only when the driving signals are found to be correct and there is no output signal should the CCD be replaced.



Symptom: No camera operation
A. Check signal at *TP* 602
B. Check signal at *IC* 601, pins 12 to 15
C. Check signal at *IC* 601, pins 7 to 8

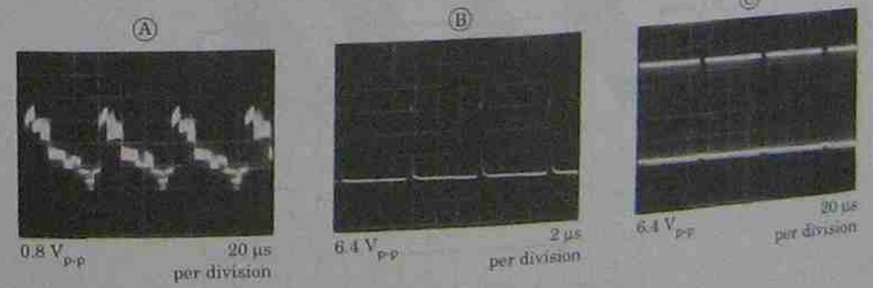


FIGURE 16.6
CCD driving circuits.
(Courtesy Thomson Consumer Electronics, Inc.)

16.6 COLOR FILTERS

In Chapter 8 we looked at a three-color tube camera with dichroic mirrors that developed the color signals. This system is still in use for most studio cameras, but not for field equipment. The cameras were too big and bulky to be handled efficiently. A filter system was developed for vidicon camera tubes and later fitted to the CCDs that allowed a single image sensor to generate a color video signal.

Strip filters at 60° angles from the horizontal and matched to the size of the scanning lines (or pixels) are placed in front of the camera target, as seen in Figure 16.7. Alternate strips of cyan, clear, and yellow are the most common, but other selections have been shown to work also.

In Figure 16.7, the cyan filter passes only blue and green light information through to the target surface. The red light information is blocked out by the cyan filter. The yellow filter passes only red and green light and blocks out the blue light. The transparent area passes all three colors, red, green and blue. The area covered by the overlap of the cyan and yellow filters will pass only green light. The red and blue are blocked out. Note that the green light passes through all areas of the filters.

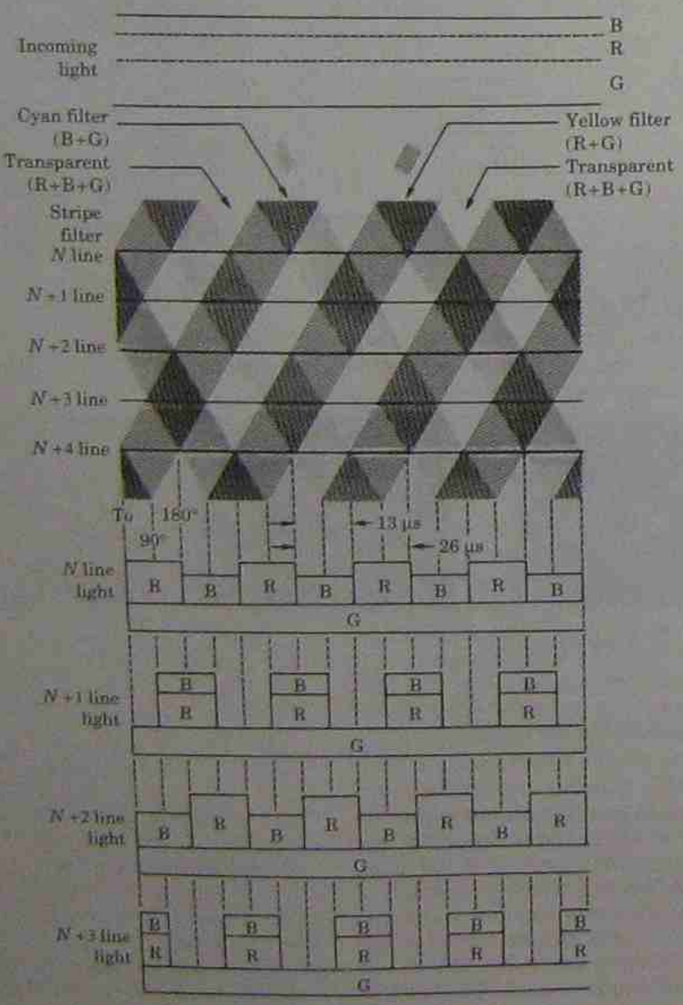


FIGURE 16.7
Light characteristics of strip filters. (Courtesy Thomson Consumer Electronics, Inc.)

Development of the color signals can be explained by examination of the light passing through the strip filters on a line by line sequence. As line N is scanned across the target area, the light by the target is alternately red and blue. The target area behind the yellow filter receives only red and green light; therefore, the output signal contains only these two colors. The target area behind the cyan filter receives only green and blue light. The sequence is repeated for the full line.

When scanning the $N + 1$ line, the first full strip is transparent and all three colors appear in the output signal. The beam next scans the overlap section where green is the only color to appear in the output signal. The sequence is repeated for the full balance of line $N + 1$.

As line $N + 2$ is scanned, the light received by the target is 180° out of phase from line N. In a similar fashion, line $N + 3$ is 180° out of phase from line $N + 1$. Therefore, line $N + 3$ starts with all colors and then scans the overlap section where green is the only output signal. The sequence is repeated for the remainder of line $N + 3$. Line $N + 4$ is a duplicate of line N, where the sequence starts all over again.

Comparing the four lines generated in this discussion, it can be seen that each subsequent line is delayed from the previous line by one-half the width of the strip filter. The red light on line $N + 1$ is received at a delayed equivalent of 90°, or one-half the width of the strip filter. The red light on line $N + 2$ is delayed by another one-half strip width from line $N + 1$, and a full strip width from line N, representing 180° phase shift. The red light on line $N + 3$ is delayed 90° from line $N + 2$ and 180° from line $N + 1$. The sequence is repeated from line to line as the target is scanned, causing a 90° shift from line to line.

The signals shown in the diagram for lines N, $N + 1$, $N + 2$, and $N + 3$ represent the light falling on the target to generate the target current, which is applied to the output preamplifier circuit. The preamplifier output signal is then used to develop the Y-luminance signal and the R − Y and B − Y color difference signals for the chroma, as was described in Chapter 8.

17 Video Tape Recording

17.1 INTRODUCTION

The tape used for magnetic recording had to be flexible, strong, stretch proof under tension, and moisture resistant. Mylar became the material of choice. A thin layer of magnetically hard powered iron-oxide, which holds its magnetism for long periods of time, is spray painted onto one side of the tape. The oxide surface is then polished to a smooth finish. Audio cassettes use 0.001-, 0.002-, and 0.003-in. tape thicknesses for 90, 60, and 30 minutes of recording time. The thinner tapes play longer but are more fragile.

The speed at which the tape travels through the machine affects the highest frequency of recording as well as the playing time. Dictation recorders use a tape speed of 0.9375 (15/16) in./sec, audio cassette recorders use 1.875 (1⅞) in./sec, reel to reel audio decks use selectable 3¾, 7½, or 15 in./sec tape speeds, while professional sound recording studios still use 30 in./sec reel to reel decks.

17.2 RECORD HEADS

A coil of wire wrapped around a metal bar will become a solenoid when a current is passed through the wire. The ends of the bar will have oppositely polarized magnetic fields called the north and south poles. Bending the bar into a horseshoe shape establishes a magnetic field in the space between the ends of the horseshoe, as seen in Figure 17.1a. Heads made from laminated layers of mu-metal or permalloy will reduce the eddy-current losses in the core material. Solid-block record heads are a mix of ferric oxide with such materials as manganese, zinc, magnesium, or nickel. These heads are all magnetically soft, which means that they can be rapidly magnetized and demagnetized.

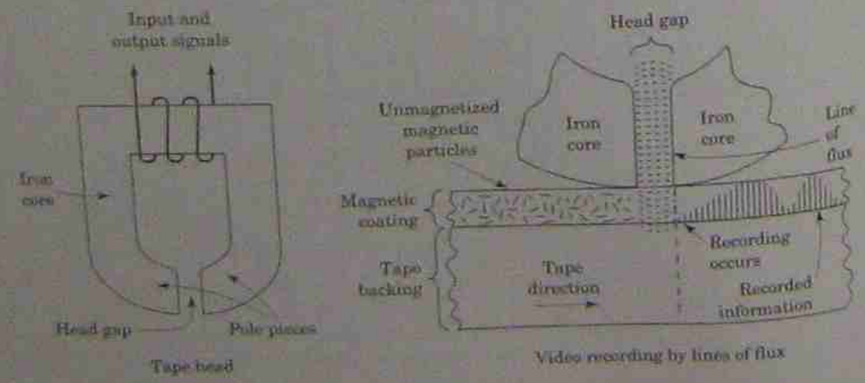


FIGURE 17.1
Tape recording head construction and operating principle. (Courtesy Thomson Consumer Electronics, Inc.)

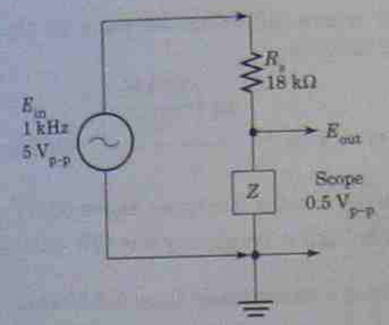


FIGURE 17.2
Test circuit for checking tape head impedance.

Audio record heads usually have 500 ohms (Ω) of impedance, while playback heads have 2000 Ω of impedance. A combination record–playback head is generally 1000 Ω, as are video record heads. Use the same method to test tape heads as was used for testing crystals. That is, connect a resistor in series with the head and apply a signal generator across both elements. Measure the voltage across the tape head and use the rearranged voltage-divider equation to find head impedance, as follows:

$$\text{head impedance } (Z) = \frac{R_s E_s}{E_{in} - E_s}\ \Omega \quad (17.1)$$

where R_s is the series resistance.

The example in Figure 17.2 uses equation 17.1 to find the head impedance as

$$Z = \frac{(18\ \text{k}\Omega)(0.5\ \text{V})}{5\ \text{V}} - 0.5\ \text{V} = \frac{9\ \text{k}\Omega}{4.5} = 2\ \text{k}\Omega$$

Never use an ohmmeter to measure the resistance of the tape head because the dc voltage from the meter will permanently magnetize the head. Head demagnetizers with instructions are available from most parts distributors, as are head cleaning solvents. Rubbing alcohol and cotton swabs can substitute for commercial head cleaners when available.

Figure 17.3 illustrates how the tape becomes magnetized when an ac signal is applied to the tape head. The size of the iron oxide granules has been greatly exaggerated in order to best show this condition. An ac current is set up in the head due to the ac voltage applied across the head. The induced magnetic field in the head core material polarizes

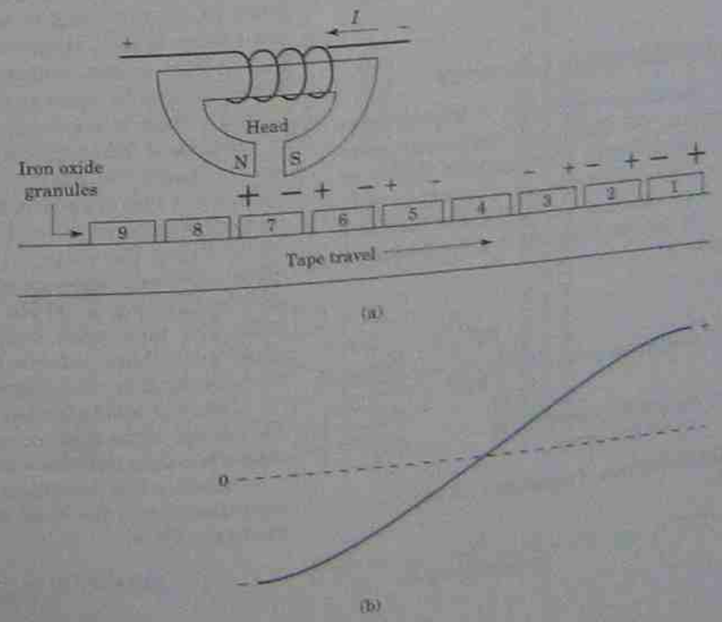


FIGURE 17.3
Recording a sine wave on tape: (a) shows strong positive at 1, zero at 4, and strong negative at 7; (b) the resulting signal.

the pole pieces, which make contact with the tape. The direction of tape travel in Figure 17.3a is from left to right. Granules 1 through 7 have already been magnetized, while granules 8 and 9 have randomly scattered magnetization.

The illustration process in Figure 17.3a begins with granule 1 that has been strongly magnetized as it passed under the head gap. Granule 2 is polarized in the same direction as it passed under the head gap, but shows a lesser strength than granule 1. Granule 3 has been magnetized by a still weaker field as it passed under the head gap, but is polarized the same as 1 and 2. Granule 4 passes under the head gap when there is no magnetic difference across the gap and is therefore not magnetized. Granule 5 is lightly magnetized with minus on the right, equal but opposite to granule 3. Granules 6 and 7 are magnetized by progressively stronger fields with minus to the right as they pass under the head gap.

The half-cycle wave in Figure 17.3b can be used to represent three different aspects. Most importantly, it represents the polarity and strength of the magnetic forces imprinted onto the tape. It is also an exact replica of the ac signal voltage that is applied to the tape head in order to develop this specific recording. It would also be the amplitude and polarity of the magnetic recording from the tape head when granules 1 through 7 are played back.

17.2.1 Gap Size versus Frequency

The audio frequency range is 20 to 20,000 hertz (Hz) or 9.96 octaves. The video frequencies cover the range from 30 Hz to 4.2 megahertz (MHz), or 17.1 octaves. Remember that an octave change in frequency is two times or one-half of the reference frequency. The octave change for a given frequency range is found by

$$\text{number of octaves } (N) = \frac{\log\left(\frac{f_h}{f_l}\right)}{\log 2} \qquad (17.2)$$

where f_h = highest frequency
f_l = lowest frequency

Useful derivatives of equation 17.2 are

$$f_h = f_l(2^N) \quad \text{and} \quad f_l = \frac{f_h}{\text{antilog}\,(N \log 2)}$$

The octave difference between 20 Hz and 20 kilohertz (kHz) is

$$\text{number of octaves} = \frac{\log\left(\frac{20\ \text{kHz}}{20}\right)}{} = 9.966 \text{ octaves}$$

When you want 9 octaves above 50 Hz,

$$\text{frequency high} = \text{frequency low } (2^9) = 25{,}600 \text{ Hz}$$

Sixteen octaves lower than 5.4 MHz is

$$\text{frequency low} = \frac{5.4\ \text{MHz}}{\text{antilog}\,(16 \times \log 2)} = 82.4 \text{ Hz}$$

Figure 17.4a compares the space occupied on the tape for one cycle of signal to the size of the gap at several frequencies. In the top wave, only a small part of the wave appears across the gap, and the change in voltage is small regardless of which part of the wave is examined. The center wave shows a maximum positive peak of the wave at one edge of the gap and the maximum negative peak at the other edge of the gap, yielding maximum voltage across the gap. The bottom wave shows the same part of the wave at both edges of the gap for a voltage difference of zero, or zero output voltage.

Figure 17.4b compares the head voltage to frequency graph for a fixed head gap. It shows that when the gap is equal to one wave length the output voltage is zero. Higher frequencies will have repeated zero nodes, making this range unusable. When the gap is equal to one half-wavelength, the output voltage is maximum and drops off at a rate of −6 decibels (dB) per octave for all frequencies below this point. For example, when the head output voltage is 1 volt (V) p-p at 20 kHz, the output at 20 Hz for 9.96 octaves at −6 dB/octave is about 1 millivolt (mV) p-p. For video, a 17.1-octave change at −6 dB/octave would mean an output voltage of 7.44 microvolts (μV) p-p at 30 Hz for 1 $V_{p\text{-}p}$ output at 4.2 MHz. The tape noise, head noise, and amplifier noise would bury the low-frequency signal under the noise for this video signal condition.

The gap size is further related to frequency by the velocity of the tape movement. Faster movement means less time that the wave is across the gap.

Time is the reciprocal of frequency, so if the tape time across the head decreases, the frequency increases. Then

$$\text{gap size } (g) = \frac{\text{velocity}}{2(\text{frequency})} \qquad (17.3)$$

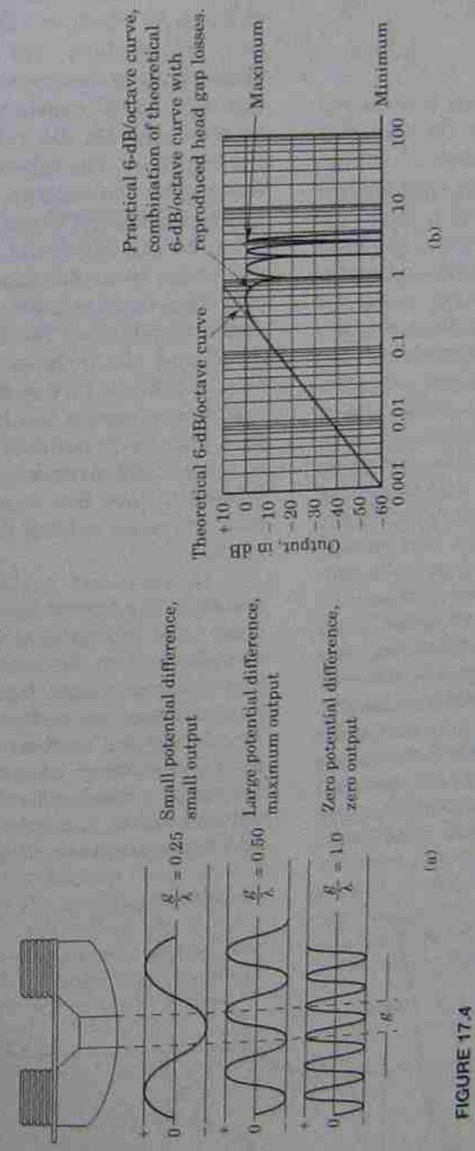


FIGURE 17.4
Tape head response: (a) signal wavelength compared to gap size; (b) head frequency response as a ratio of gap size to signal wavelength.
(Courtesy Thomson Consumer Electronics, Inc.)

where gap size is in inches, tape velocity is in inches/second, and frequency is the highest to be recorded.

Derivatives of equation 16.3 are

$$V = 2fg \quad \text{and} \quad f = \frac{V}{2g}$$

17.2.2 Bias Voltages

The reluctance of the head material opposes any change in the magnetic field around the head. Figure 17.5a shows that the applied force (H) will induce a magnetic field (B) around the head to saturation. This initial curve is labeled 1. When the polarity of the applied force is reversed, the head demagnetizes to zero and then magnetizes to saturation in the other direction, but not along the same path. It follows the odd path. Reversing the polarity a second time causes the magnetic field to follow the even path. Magnetizing and demagnetizing the head along different paths cause crossover distortion in the output signal, as seen in Figure 17.5b. To overcome this distortion caused by the hysteresis loop, a high-frequency sine wave called the *bias voltage* is added to the audio signal. The amplitude of the bias voltage should be at least two times the largest audio voltage to be recorded, and the frequency should be any odd harmonic of the highest audio frequency to be recorded (5× is typical). The effects are seen in Figure 17.6b, where the bias signal is distorted but not the audio signal. The simplified block diagram in Figure 17.6a shows the bias and audio signals added together and applied to the record head. The bias voltage is also used for the *erase* voltage (E). The high-pass filter allowed the bias voltage to feed through to the record head in the record mode but prevented the audio voltage from reaching the erase head.

17.2.3 Tape Transports

Figure 17.7 illustrates the components of an ideal audio tape transport. After the tape is threaded onto the machine and turned on, the semihard pressure roller moves into position and pinches the tape against the capstan cylinder. The speed of the capstan controls the velocity of the tape through the transport. The takeup reel is driven at a speed faster than the capstan can supply the tape, so a forward pressure is maintained to keep the tape from spilling out of the reel. The tension roller is the brake lever for the supply reel, which must provide a reverse tension so that the supply reel does not spill tape. The forward pull of the capstan drive and the reverse drag of the supply reel should provide just enough pressure to keep the tape firmly against the face of the tape heads. It is good practice to position the heads so that the tape forms a slight wrap around the face of the heads. When the tape has straight-line travel, pressure pads are used to keep the tape firmly against the heads.

In the record mode, the tape will need to be erased before laying down a fresh recording, so the erase head is first in line from the supply reel. In the playback mode, the erase voltage is disabled and the erase head has no function. The record head is placed before the playback head when separate heads are used so that you can monitor the fresh recording in progress. Using a single record–playback head voids this possibility. In compact recorders, a single head holds the erase coil and the common record–playback coil.

FIGURE 17.5
(a) The hysteresis (B–H) curve and (b) the effects on the applied signal.

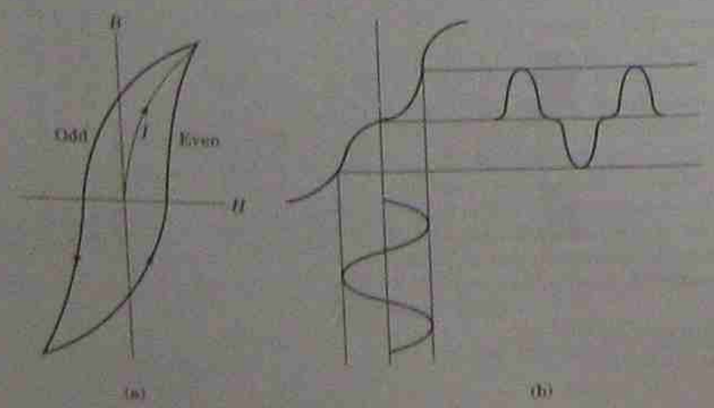
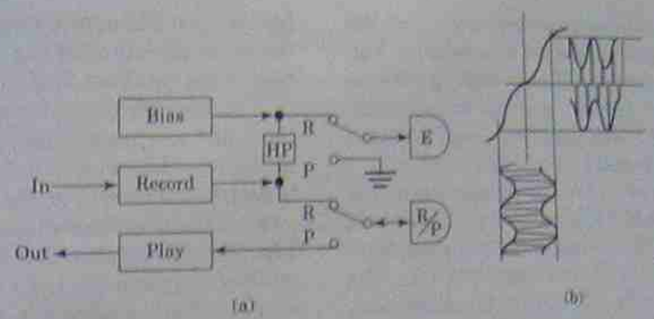


FIGURE 17.6
Control of the hysteresis effect (b) by adding a high-frequency bias voltage (a).



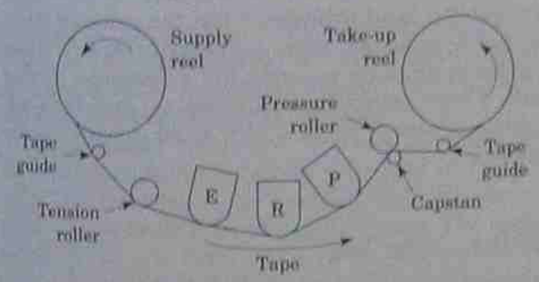


FIGURE 17.7
The ideal audio tape transport.

17.2.4 Head Alignment

A professionally prepared test tape is played on the unit to correctly position the playback head first. Test tapes are available for each of the standard tape speeds. A test frequency is announced on the tape, followed by a 1-minute sine-wave signal at that frequency. This procedure is followed for all the frequencies in the testing sequence. Figure 17.8b identifies the **zenith** adjustment, which is set for maximum output signal at any of the mid-frequencies. The **azimuth** positioning is adjusted for maximum output at only the highest frequency at this tape speed. Notice that the zenith and azimuth adjustments also affect the **elevation** positioning. On a combination record–play head, setting the playback head also sets the record head positioning. On tape decks that use separate record-playback heads, after the playback head is adjusted, feed in a sine-wave signal at the highest frequency to be recorded, and in the record mode, monitor the playback signal while you adjust the position of the record head for maximum output signal. Use an old tape for setting the erase head positioning. Set the recorder in the record mode with no input signal, and monitor the output signal of the playback section. Adjust the erase head for minimum output noise from the tape. Video cassette recorders (VCRs) use all these same principles and a few more, but in a different way.

17.3 HELICAL SCANNING

In 1955, the British Broadcasting Company (BBC) aired a 30-minute video program from tape that required a 5-foot-diameter tape reel. About the same time, a slant track helical recording system was introduced that placed the record heads on a revolving head cylinder. Moving the head and the tape at the same time provided the higher head to tape velocity that was needed to reduce the size of the tape reels. Each rotation of the head cylinder recorded one full field of video information on a slanted track across the tape. The path starts during the vertical blanking time, records 262.5 lines of horizontal video, and ends during the next vertical blanking pulse.

FIGURE 17.8
Tape heads showing (a) makeup of the head while (b), (c), and (d) identify the conditions for zenith, azimuth, and elevation adjustments.

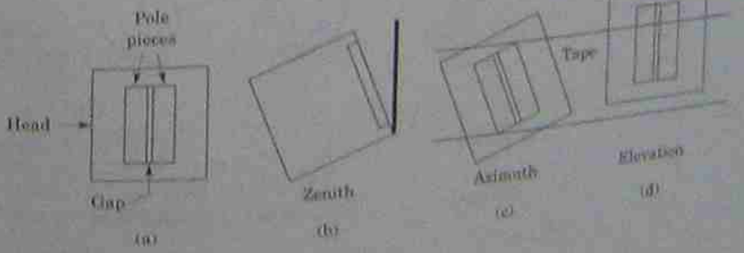


Figure 17.9 illustrates several ways that the tape may be wrapped around the tape cylinder. Figure 17.9a and b show a **full** wrap that is used on reel-to-reel tape decks when you can put a loop in the tape. One full revolution of one head provided the slant track of recorded video information.

Figure 17.9c and d are the **omega** wrap that came out of automatic loading efforts. There was still a tiny section of tape where the one video head was not in contact with the tape, but this was timed to coincide with the vertical blanking time, and no video information was lost. Notice that both the full and omega wrap systems require the tape reels to be at different elevations, which does not lend itself to cassette loading.

Figure 17.9e and f identify the **half+** wrap, which allows the tape to arrive and depart from the head cylinder at the same elevation. This is most conducive to cassette loading. It requires that the head cylinder be slanted at about 6° and was further improved by adding a second video head to the cylinder. Wrapping the tape slightly greater than 180° allowed head *B* to enter onto the tape just before head *A* departed from the tape. The overlap of recording was again timed with the vertical blanking interval so that each slanted track of video started with the vertical blanking (and sync) pulse, recorded 262.5 horizontal lines of video, and ended with the next vertical blanking pulse. One full field of video was recorded, and no information was lost.

Note that all the systems in Figure 17.9 have the head cylinder spinning in the same direction as the tape travel. With some thought, you can conclude that, if the head cylinder rotated in the opposite direction from the tape travel, a greater head-to-tape velocity could be achieved with better high-frequency response. In the next section you will see that the way in which the luminance signal is formatted does not demand this improved high-frequency performance and, by rotating the head in the same direction as the tape travel, reduces the tape usage by about 30%.

Almost all the video tape recorders today use the half+ wrap and tape-to-head direction as noted in Figure 17.9e and f. It has become an unspoken industry standard. For the tape to change pitch or yaw requires a cone-shaped tape guide. All three tape feeds in Figure 17.9 have cone-shaped guides as they approach the head cylinder, whether shown or not. These guides are precision made and are used for the elevation adjustment of the tape around the head cylinder, since the cylinder itself cannot be adjusted. Many manufacturers lock these guides in place by securing the adjustment screws with a hard paint. They will rarely if ever need adjustment except when a new head cylinder is installed.

17.3.1 Tape Track

Two basic systems emerged from the head cylinder development. They were the **beta** and the **home video system** (VHS). Both systems are similar, but not interchangeable. Over the years, the VHS system has gained the greatest popularity and is the only system discussed in this text.

A standard VHS tape pattern is shown in Figure 17.10 in the record mode as viewed from the oxide side of the tape. The tape movement is from right to left across the page and has already passed the erase head. The tape, as it moves around the video head cylinder, gets successive tracks of video recorded from heads *A* and *B*. Figure 17.10 shows the diagonal video tracks starting at the bottom and ending at the top edge of the tape. Head *B* has just entered onto the tape as head *A* is leaving the tape. At the instant shown in Figure 17.10, both heads are recording the same vertical blanking and

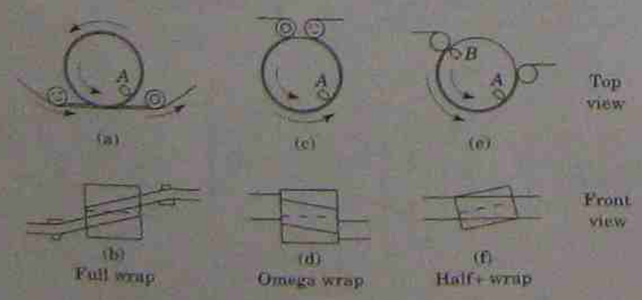


FIGURE 17.9
Common methods for wrapping the tape around the revolving video head cylinder.

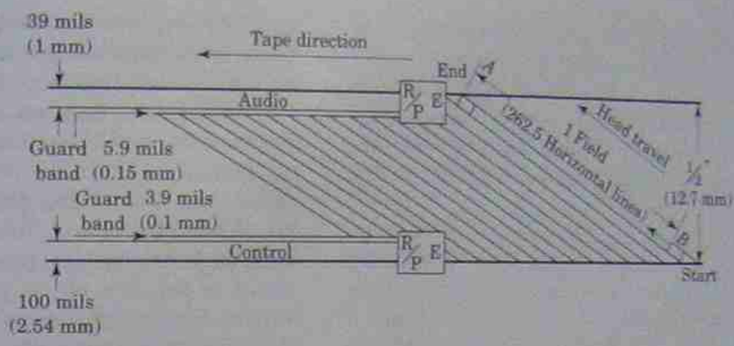


FIGURE 17.10
Diagram of how the video, audio, and control tracks are placed on ½-in. wide video tape.

sync pulse. Each cylinder head records one field of video, so one revolution of the head cylinder records one frame. At 30 frames per second, the video head cylinder spins at 1800 rpm (see Table 17.1).

The audio track and the control track are recorded longitudinally along the edges of the tape after the video has been recorded. This is achieved by a single head with four pole pieces. The audio erase poles are first, followed by the audio R/P poles at the top edge of the tape. The tape must be cleaned to provide the guard band between the video and audio recordings as the fresh audio track is laid down.

Figure 17.10 also shows the control track with its guard band at the bottom edge of the tape. The control track is recorded in exactly the same way as the audio track, in that the erase function occurs first, followed by the control information recording. Keep in mind that the erase operation is only active during the record mode and is disabled during the playback sequence.

In the record mode, the tape is transported through the machine at a specific speed (see Table 17.1), and the head cylinder revolves to record first one video head information and then the other video head information, which is repeated continually for as long as the mode is selected. The audio and control track data are recorded along with the video in a fairly normal manner. The only timing requirement in the record mode is the position of the video head with respect to the vertical blanking and sync pulse as described earlier. The speed of the cylinder head motor is adjusted until the video head makes contact with the tape at 6.5 horizontal time periods before the leading edge of the vertical sync pulse.

However, in the playback mode, we need to ensure that the tape speed, the head cylinder

Table 17.1
Tape format

	VHS	VHS-C	8 mm
Cylinder diameter	2.44 in. 62 mm	1.63 in. 41.33 mm	1.575 in. 40 mm
Cylinder circumference	7.67 in. 195 mm	5.11 in. 130 mm	4.95 in. 126 mm.
Cylinder speed	1800 rpm	2700 rpm	1800 rpm
Tape speed (SP)*	1.315 in./sec 3.34 cm/sec	1.315 in./sec 3.34 cm/sec	0.565 in./sec 1.435 cm/sec
Tape wrap	195°	270°	221°
Head Gap 1 and 3* (SP)	2.76 mils 70 μm	1.2 mils 30 μm	1.0 mils 25 μm
Azimuth (head tilt)	+6°	+6°	+10°

SP: standard play (2 hr)
*LP: long play (4 hr); tape speed = 0.65 in./sec
*EP: extended play (6 hr); tape speed = 0.43 in./sec
LP and EP heads 2 and 4. Gap width = 1.2 mils.

speed, and the position of the video head on the tape are an exact duplicate of the sequence that was present in the record mode. Head *A* must playback from track *A*, and head *B* must playback from track *B*. The video head cannot enter onto the tape overlapping part of track *A* and part of track *B*. The timing must be precise.

A toothed gear on the lower end of the capstan motor and another on the lower end of the cylinder head motor act as a pulse generator as the teeth of the gear pass by a pickup coil. A metal vane attached to the head assembly generates a pulse to announce the position of the video head as it passes another pickup coil. The coil output signals will be called the CAP PG (pulse generator) for the capstan motor speed, the CYL FG (frequency generator) when referring to the head cylinder motor speed, and the CYL PG (pulse generator) when talking about the video head positioning. These pulses, plus the vertical blanking and sync pulse, are all ruled by frequency. Then, by comparing the four frequencies through a series of phase-locked loops, two different dc voltages are developed to control the speed of the head cylinder motor and the speed of the capstan motor individually.

A pulse voltage is developed from the four frequencies and is added to the tape via the control head to denote the time that video head *A* makes contact with the tape, to later be used as the playback reference pulse position.

In the playback mode, the control track data are read into the motor control system as the **tracking** sequence. This sets the capstan motor speed and the head cylinder motor speed individually until a match is achieved by which head *A* makes contact with the tape at the same time that a control track pulse occurs.

The square-wave voltage that drives the ac capstan and head motors is pulse width modulated. At 50% modulation, that is, the pulse is high for 50% of the time and low for 50% of the time; the motors will run at the design speed. Increasing the percent of modulation causes the motor to run faster, and decreasing the percent of modulation slows down the motor. The pulse repetition rate (or frequency) does not change; only the time high compared to the time of one cycle changes as the percent of modulation is varied.

Originally, there was a guard band of 0.8 mils (20 μm) between the video recording tracks to avoid crosstalk from track to track. Later developments tilted the record heads in opposite directions by 0.4° and eliminated the guard bands so that the long play and the extended play features could be added. This created two problems. (1) The color subcarrier from adjacent tracks would heterodyne to cause a faint but noticeable beat pattern in the picture. A system to change the phase of the color subcarrier oscillator by 90° on each successive video track cancelled this effect. (2) The horizontal sync pulses overlapped from one video track to the next when the guard band was eliminated. A method of frequency interleaving of the video signal on successive tracks does not cancel this effect, but optically removes it from the viewed picture.

17.3.2 VCR Cassette Loading

The majority of problems found in VCRs involve the tape deck mechanism and the status-sensing devices that control its operation. When the cassette is placed in the loading door, switch *A* in Figure 17.11 is closed and starts the loading motor that draws the cassette into the loading elevator. The front flap of the cassette is opened as the elevator

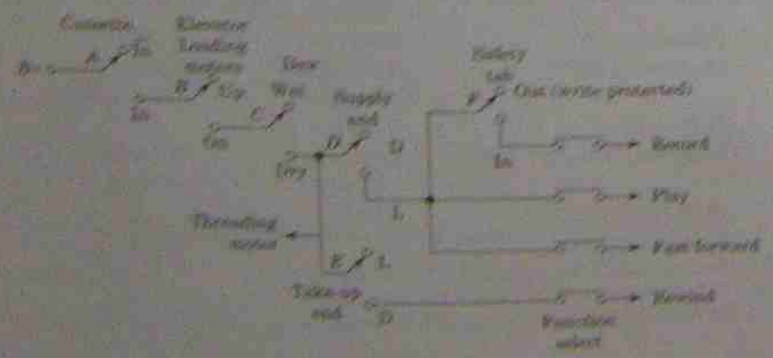


FIGURE 17.11
Tape deck functional status control switches.

lowers the cassette into position. Some recorders require that the power switch be turned on before the cassette can be loaded, while newer VCRs turn on the power when the cassette is inserted (not shown in Figure 17.11). Switch *B* is closed when the elevator is down and locked. At this point, the physical position of the cassette is as shown in Figure 17.12a. The tape guide cams *A*, *B*, and *C* and the capstan drive shaft must all be on the inside of the tape loop.

Several sensory devices are brought into play at this time. Too much humidity will cause the tape to stick together and jam the tape transport. The dew sensor is switch *C* in Figure 17.11. The resistance of the dew sensor increases as the humidity goes up. It is part of a voltage divider in the compare circuit and raises the sensor voltage to change the compare output status to shut down the tape transport. All operations except eject are inhibited under high-humidity conditions, because switch *C* is held open.

A clear leader and trailer are added to the ends of the tape. Two phototransistors are stationed at the outside of the tape path by the supply reel and takeup reel that will turn on when exposed to infrared light. An infrared LED is placed at the center of the transport, which will activate either phototransistor when the clear tape passes light to the sensors. These are designated as switches *D* and *E* in Figure 17.11. When the leader is exposed (takeup reel sensor active), the recorder will not rewind. When the trailer is uncovered (supply reel sensor active), the recorder will reject commands to play, record, and fast-forward. See Figure 17.13 for the relationship of these devices.

To play or FF, plus switches *A*, *B*, *C*, and *D* in Figure 17.11 must be closed, opposite from the positions shown in the figure. To record, the same switches must be closed, and the safety tab switch (*F*) must also be closed.

On the rear of the cassette housing, there is a plastic tab that activates the safety switch. When the tab is in place, you may record on the tape. When the tab is removed, the tape is *write protected* and you cannot record. However, placing a piece of electrical tape across the tab space will again permit recording.

To rewind, switches *A*, *B*, *C*, and *E* must be closed. Switches *A* and *B* may be physical microswitches, whereas switches *C*, *D*, *E*, and *F* are digital AND gates inside the microprocessor.

Figure 17.12 shows the cassette in place for the conditions of (a) before loading and (b) after loading. As stated earlier, the tape guides *A*, *B*, and *C*, and the capstan drive cylinder must all be inside the tape loop when the cassette is set in place. In beta machines, the tape is immediately extracted from the cassette and wrapped around the head cylinder, where it remains until the eject command

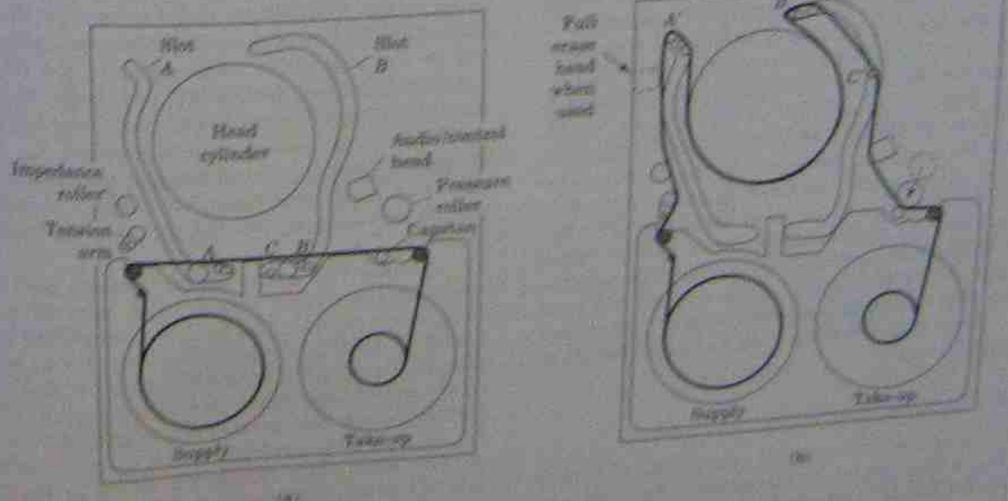


FIGURE 17.12
Video cassette recorder tape deck. Cassette in place (a) before loading and (b) after loading.

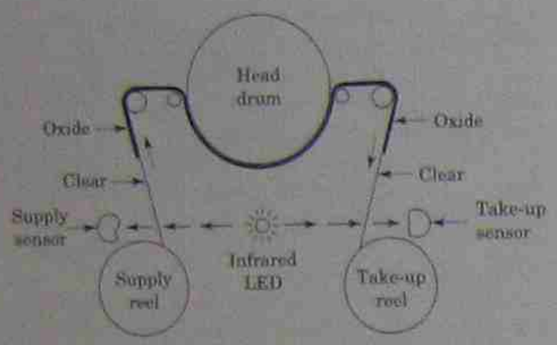


FIGURE 17.13
Infrared LED and sensors to detect end of tape (both ends).

is given. In VHS transports, the tape remains inside the cassette until an operational command is given. Only then is the tape extracted and wrapped around the head cylinder. Each time a stop command is ordered, the tape retracts into the cassette and waits for the next functional command.

Moving the tape out of the cassette, as in Figure 17.12b, starts by moving cam *A* from its rest position to the other end of the slot, at *A'*. In this position, the tape moves the tension arm out and reduces the brake band pressure on the supply flywheel. It moves around the impedance roller and past the full erase head (when used) and around the tape guide at *A'*. Machines with flying erase heads (covered later) do not have a full erase head.

At the same time, cam *B* leaves the rest position and moves upward through slot *B*. Halfway along its travel, cam *C* is coupled onto the takeup loading ring and follows cam *B* up through slot *B*. Cam *B* reaches the end of its travel at *B'*, and cam *C* stops at midpoint position *C'*. The tape is now wrapped 270° around the head cylinder, with cam *C* holding the tape away from the head cylinder and against the audio control head. The pressure roller moves into position, holding the tape against the capstan drive cylinder. Cam *A* is moved by a supply ring assembly, and cams *B* and *C* are moved by a takeup ring assembly, both on the underside of the tape transport.

17.4 BLOCK DIAGRAM

Look carefully at the upper-left corner of Figure 17.14 as this section is examined. The VCR contains the full RF section of a television receiver, in that it gets its input signal from the antenna. It must be able to select any of the program channels within its design limits and lower each channel frequency down to the IF frequency. It has a video IF section, a video detector, and an AGC section. It has a sound section that separates the sound channel and demodulates the FM signal to recover the audio signal, just like a television receiver. You may have observed that all the special signal treatment, FM stereo, color television, closed captioning, and now video tape recording take place at the lower frequencies.

In the case of camcorders, Figure 17.14 will omit the RF sections, but will include (in dashed lines) the camera pickup device that is fed into the recorder at the same place that the detected video is entered. A view finder with a 0.6-in.-diagonal CRT is part of the video output circuit to display the camera signal and the playback picture via switch S_{2a}.

Normal television viewing takes place when the TV–VCR switch is in the TV position, as seen in Figure 17.14. The VCR is turned off and the antenna is connected directly to the television receiver.

When the VCR is turned on with switch S_1 in the VCR position, and the receiver is set to channel 3 or 4, whichever is used in your area; the channels are selected by changing the tuner in the VCR section. We will use channel 45 in the following example.

Channel 45 comes in through the antenna, selected by the VCR tuner, and is lowered to the standard video IF frequencies. The detected output signal is the composite video that is fed into the luminance record circuits (*IC* 203, lower half) and the chroma record circuits (*IC* 204, lower half). It is connected to the record contact of switch S_{2a}, where the video signal is passed through the sound adder and then amplitude modulated onto Channel 3–4 picture carrier signal for the signal to the television receiver.

Channel 45 sound comes through part of the video IF amplifiers and is then separated from the picture signal. The sound is amplified by the sound IF amplifiers and is FM detected to become the audio signal. The audio signal is fed to the audio record amplifiers and to the record (R) contact of switch S_{2b}. Switch S_{2b} is ganged to switch S_{2a} so that both sections are in the same position at the time. The recovered audio is then frequency modulated onto a 4.5-MHz carrier and added to the video, which are then both applied to the channel 3–4 amplitude modulator. The output of the channel 3–4 modulator is connected

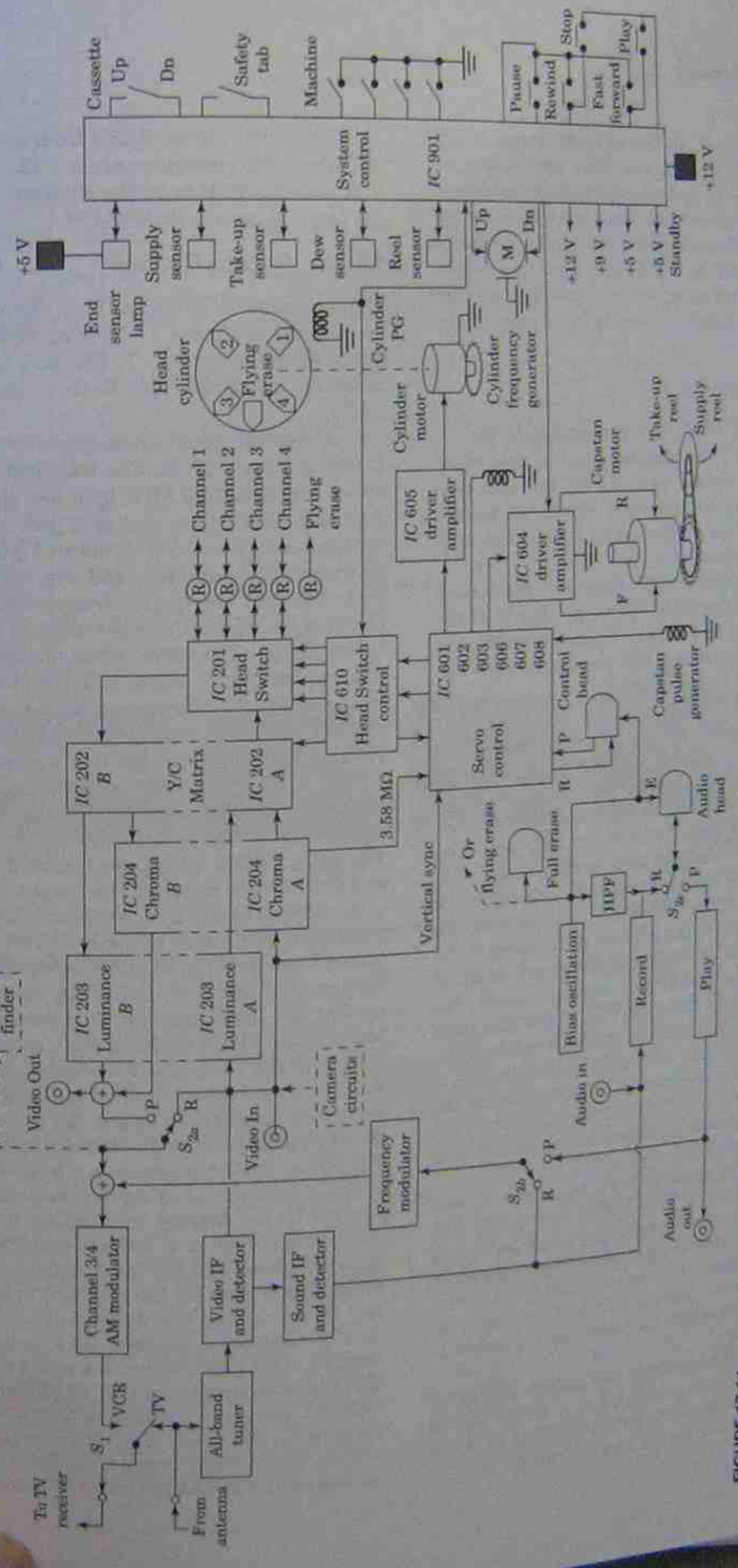


FIGURE 17.14
Typical block diagram for a video tape recorder.

through switch S_1 to the antenna input of the viewing television receiver. This section has received channel 45 and demodulated the video and audio, as is done in the standard television receiver. It has then frequency modulated the audio signal and added it to the video signal for amplitude modulation onto the channel 3–4 picture carrier signal before delivering it to your television receiver.

17.4.1 System Control

The function of *IC*901 (system control) at the far right of Figure 17.14 was discussed in part when the loading procedure was covered. Its main purpose is to supply the operating voltages to specific circuits depending on the status of the tape deck and selected functions.

The supply reel sensor lamp and the takeup reel sensor lamp establish when the tape is at the end of its travel and may be driven forward or in reverse. The dew sensor lets you know when the humidity is safe for operation.

The cylinder pulse generator (PG) is used to compare the frequency of the driving voltage for the capstan motor to the speed of the motor itself as sensed from the capstan pulse generator (FG).

There are two reel speed sensors feeding *IC* 901, although Figure 17.14 shows only one. The sensors have a reflective plate located under each reel deck that is serrated into eight segments. An infrared LED and a light-sensitive transistor can then count the speed of each reel. If the speed of the takeup reel falls below 1 Hz in the record mode or below 3 Hz in the fast forward or rewind mode, the control system will place the VCR in the stop position to prevent tape spill in the VCR mechanism. The supply sensor is similar in operation and is also used to count tape usage. The frequency of the supply reel and the frequency of the takeup reel are compared to a memory pattern in the control chip to read out to a tape counter.

The loading motor gets its instructions from the system control *IC* 901 to move the cassette elevator up or down during the loading and unloading operation. The cassette up–down, the safety switch, and the mechanical switches were part of the coverage in Figure 17.11, but you will need to check your schematic to see which switches are applicable to your product.

The function controls are shown in Figure 17.14 as mechanical switches, but in all late-model VCRs they are electronic switches driven by a microprocessor and/or remote-control transmitter.

The entire circuit works from a +12-V dc supply, which will then dispense a +12-, +9-, and +5-V dc standby voltage to the circuits as selected by the function control switches.

17.4.2 Record Circuits

The composite video signal from the video detector (or camera) in Figure 17.14 is applied to the luminance processor circuit *IC* 203 and to the chroma processor circuit *IC* 204. Each is examined separately.

A typical luminance processing circuit is shown in Figure 17.15. The frequency of the luminance is limited to 3 MHz by a low-pass filter, and then the sync pulses are clamped to a reference voltage level. The video signal in Figure 17.15 will be frequency modulated, and you may recall from basic FM that the higher frequencies are preemphasized to reduce the noise content of the modulating signal. Therefore, after clamping the sync tips, the luminance signal is preemphasized, giving more gain to the higher frequencies. Preemphasizing causes the fast rise time signals to have a large positive overshoot and the fast decay time signals to have a large negative overshoot. These will appear as spike voltages above and below the desired signal level, as seen in Figure 17.15, waveform D. The spike voltage peaks are removed by the white and dark clipper circuits. The output of the clippers is dc coupled to the frequency-modulating, voltage-controlled oscillator. You may recall from phase-locked loops that the dc error voltage controlled the frequency of the VCO. It has the same effect here, in that the instantaneous changing signal of the video looks like a dc level that controls the frequency of the VCO. The FM carrier rest frequency, with no video signal applied is 3.9 MHz for VHS and 100% modulation, causes the carrier to deviate by ±500 kHz for a modulated envelope from 3.4 to 4.4 MHz. This represents a modulation index of 0.33 (i.e., the changing carrier frequency of 1 MHz divided by the highest modulating frequency of 3 MHz) and is typical of narrowband FM having one upper sideband and one lower sideband. The modulating phase is set for the sync tips to lower the carrier frequency and the white peaks to increase the carrier frequency, as seen in Figure 17.16. The number of octaves between 3.4 and 4.4 MHz is only 0.372 octaves (from equation 17.2) and, at −6 decibels (dB) per octave, results in only a −2.23-dB difference in amplitude over this frequency range. This is considerably better than the −102.5 dB discussed earlier for the full video frequency range of 4

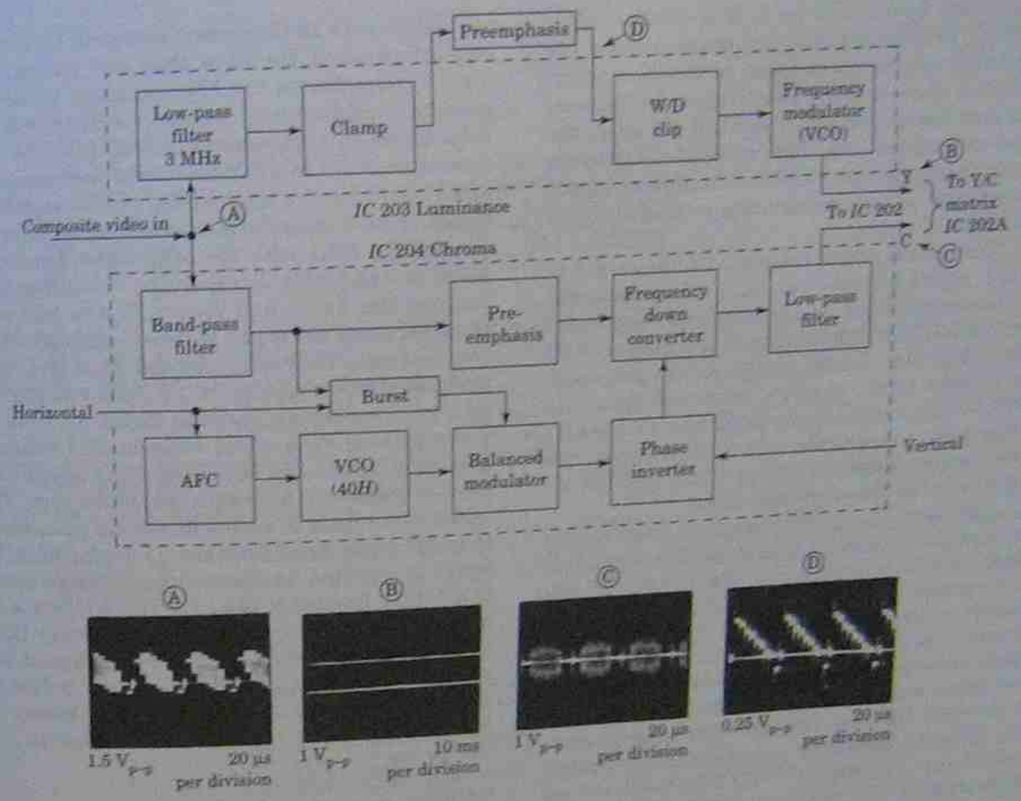


FIGURE 17.15
Record processing circuits for the luminance and chrominance signal. (Courtesy Thomson Consumer Electronics, Inc.)

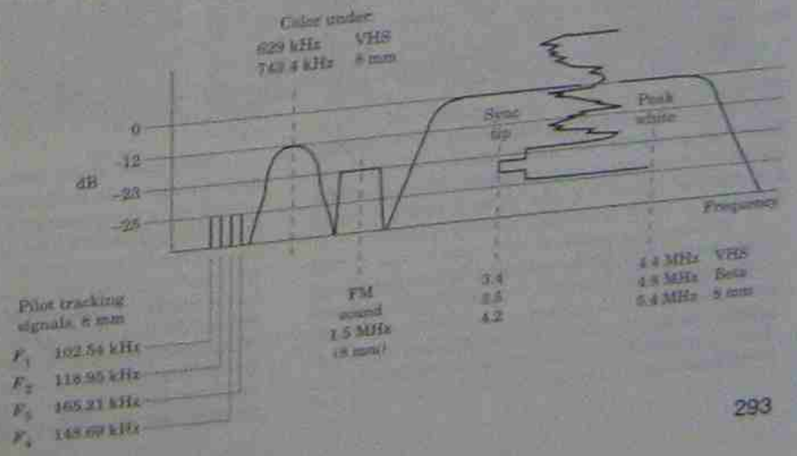


FIGURE 17.16
Spectrum of frequencies versus amplitude for the signals recorded on video tape.

MHz. There is no need for a bias voltage when recording the luminance signal because there are only small amplitude changes in the frequency-modulated wave. Any crossover distortion that may occur is in the carrier signal and will not affect the frequency deviation that represents the luminance signal. The frequency-modulated luminance signal is now added to the chromanance processed signal at *IC* 202, *Y/C* matrix.

The full composite video signal is also fed to *IC* 204, where a band-pass filter allows only the amplitude-modulated double-sideband suppressed carrier (DSSC) chroma signal over the range of 3.08 to 4.08 MHz to be treated by the chroma processor. The chroma signal is down converted from the 3.579545-MHz carrier center frequency to 629-kHz carrier center frequency in order to fit the spectrum of frequencies, shown in Figure 17.16, and not interfere with the FM luminance signal.

Any form of frequency changer is acceptable in this application. A mixer and an oscillator or a balanced modulator with an oscillator are the two most common converter circuits. Either circuit will produce a sum and difference set of sidebands that contains the DSSC characteristics of the chroma signal. Many systems use a 4.209-MHz oscillator to heterodyne with the 3.579545-MHz color subcarrier to generate the new 629-kHz color under signal. The difference frequency is used for this operation, and the sum frequency of 7.789 MHz is filtered out of the system. The resulting chroma output signal looks exactly like those discussed in Chapter 8, except that the side frequencies will extend around the new lower carrier frequency of 629.37 kHz, rather than the 3.579545-MHz frequency as before. The waveform is shown in Figure 17.15 at wave C, but you will not be able to see the difference on your oscilloscope waveforms.

The phase inverter is responsible for the phase change of the chroma signal that cancels the crosstalk on the recorded tape, as mentioned earlier. This is done by changing the phase of the 4.209-MHz carrier by 90° for every horizontal line, but only during alternate vertical fields. The horizontal and vertical pulses into the chroma record circuits take care of this processing without your notice.

The chroma signal is now sent to the *IC*202 adder, where it is joined with the luminance signal and applied to the record heads. The frequency-modulated luminance signal serves as the bias voltage for the amplitude-modulated chroma signal, so there is no need for a bias oscillator, except for the erase function.

Figure 17.16 (frequency spectrum) has recording information for more than one system. The VHS system places the FM luminance in the frequency band between 3.4 and 4.4 MHz with the color under chroma signal at 629.37 kHz. The beta system uses 3.5 to 4.8 MHz for the luminance and 629.37 kHz for the color under chroma signal. An 8-mm system modulates the luminance between 4.2 and 5.8 MHz with the color under signal centered at 743.4 kHz. Because the 8-mm tape is so narrow, the audio and control tracks cannot be recorded along the edges, as was done for the other two systems. They are replaced by a frequency-modulated audio carrier at 1.5 MHz and the four pilot tracking signals found in Figure 17.16. In the 8-mm system, F_1 is added when head *A* makes its first pass across the tape, and F_2 is added when head *B* makes its first pass across the tape. F_3 is added when head A makes its second pass, and F_4 is added when head *B* makes its second pass. The series is repeated for the recording. Notice that F_3 is a higher frequency than F_4. There is now a frequency difference of 16 kHz (approximately 1*H*) or 45 kHz (approximately 3*H*) between adjacent pilot signals recording tracks that the servo system can decode on playback to adjust the motor speeds and head placement for correct head tracking on playback.

17.4.3 Head Switching

The original two head recorders did not switch the record–play heads in the record mode. The input signal was applied to both heads continuously. The head that was in contact with the tape laid down the recorded message, while the head that was away from the tape caused no ill effects. However, in the playback mode, the head that was away from the tape would add noise to the low-level playback signal if it were not removed from the circuit.

Two more video record–play heads were later added to provide better *pause* pictures and better record–play recording at slower than the standard play (SP) speeds. The second pair of heads (2 and 4) are narrower than heads 1 and 3 so that they do not overlap record tracks at the slower moving tape speed set for long play (LP) and extended play (EP). See Table 17.1. This system required the ability to switch video heads in both the record and play modes. Figure 17.17 shows the circuit that switches heads in both modes. The record signal is applied through the record amplifier to all four heads. The four-phase logic circuit grounds the other side of the two heads selected. For example, heads 1 and 3 are grounded while heads 2 and 4 remain ungrounded. Only the two heads that can conduct current have a magnetic field across the head gap. The four-phase logic circuit is controlled by the selection of SP, LP, or EP tape speeds in the record mode and by the control track in the playback mode. This selection, once made, remains fixed until a new command is issued by the operator or control track.

In the playback mode, the four-phase logic circuit receives its information from the control track

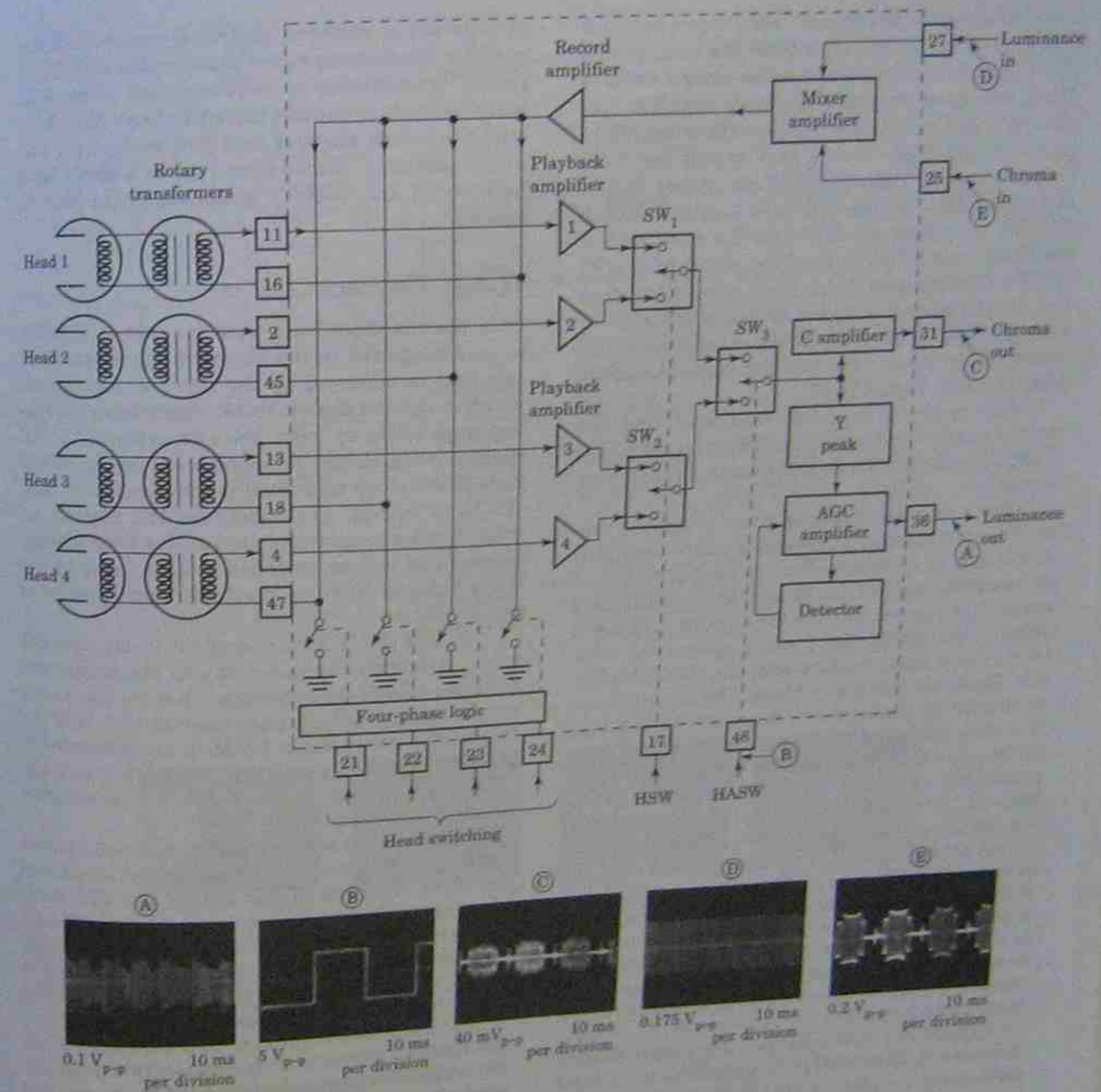


FIGURE 17.17
Video head switching circuit.
(Courtesy Thomson Consumer Electronics, Inc.)

only and activates the pair of heads appropriate for that tape speed. At the same time, the head switch (HSW) input receives data from the control track to direct SW_1 to select either playback amplifier output 1 or 2 and switch SW_2 to select the output from playback amplifiers 3 or 4 that match the four-phase logic data. This setup will not change until a new command is issued. The head amplifier switch (HASW) input lines get data from the servo control circuit for switch SW_3 to read the signal from SW_1 or SW_2, depending on which head is on the tape at that time. The control signal to SW_3 alternates for each half-cycle of head cylinder revolution as directed by the head cylinder pulse generator (PG), waveform B in Figure 17.17.

The playback signal is separated into the chroma and luminance output signals by the *C* and *Y* amplifier circuits for distribution to the playback circuits.

Some thought should be given to making contact from a stationary PC board to a tape head that is spinning at 1800 rpm. One method is to embed an insulated ring into the shaft of the cylinder head motor that connects to the tape heads and use a dimpled leaf spring that presses against the insulated ring to make contact with the stationary circuit. These are called **slip rings.** The slip rings can be cleaned by placing a few drops of cleaning fluid on a clean piece of writing paper; then slide the paper between the leaf spring and the slip ring with a gentle back and forth motion. Do not try to re-form bent or twisted leaf springs. It is better and cheaper to replace the entire leaf spring assembly.

A second method is to wind an insulated coil around the shaft of the motor and connect the ends of the coil to the tape heads. A second coil is placed around (but not touching) the shaft as the primary of a *rotary* transformer. You need one rotary transformer for each head on the head drum assembly. These are noted in Figure 17.14 by the letter R in a circle for each head.

The *flying* erase head becomes a fifth head on the head drum assembly and eliminates the need for a full erase head on the tape transport. The flying erase head is wide enough to erase two full tracks of video information on each pass over the tape. The audio and control track heads are still required to clear a path for their own signals to be recorded. The flying erase head cleans the tape just a millisecond before the new video recording is made, leaving little or no room for dust or electrical impulses to contaminate the tape. The advantages are cleaner recordings and an insignificant length of tape saved between recording segments. Some possible disadvantages are that another slip ring or rotary transformer is required, and it becomes more difficult to replace the erase head. Most VCR manufacturers suggest that you replace the full drum assembly, rather than replace a single head because of the tedious head alignment that is needed.

17.4.4 Playback Circuits

Only the one video head that has contact with the tape is connected to the playback amplifiers. Head selection is managed by the servo control circuit, which compares the playback signal from the control track to the cylinder pulse generator (CYL PG) signal. When these two signals are synchronized, the correct video tape head is connected to *IC* 201, the head switch, to *IC* 202, the *Y/C* matrix. All other heads are open circuited at this time. The opposite head will be switched in as it lands on the video tape, so only one playback head is active at any given time.

IC 202 (*Y/C* matrix) functions in the playback mode in exactly the same way as the matrix circuits for television receivers. That is, the signal passes through a high-pass filter so that only the frequencies above about 1.5 MHz are forwarded to the luminance FM recovery circuits. The same signal is fed in parallel to a low-pass filter to separate the chroma signals.

Figure 17.18 shows the FM luminance signal entering *IC* 203, where a double limiter suppresses the lower sideband of the signal. The FM luminance signal is then demodulated, filtered, and de-emphasized before being checked for dropout lines. The de-emphasizing and timing components are unique to each circuit design and become the external parts of the common chip.

The luminance signal is then fed back into *IC* 203 and the dropout compensator (DOC). At the same time, the frequency-modulated luminance signal is internally connected to the dropout detector (DOD) and an envelope detector. The dropout compensator monitors the dropout detector and the envelope detector for any dropouts from the FM envelope and inserts a stored line of luminance if either of the detectors is active. When the dropout of the FM envelope lasts longer than one line, the dropout compensator keeps inserting the same line for up to three lines. The 1-*H* (horizontal) delay circuit supplies the stored line from memory of the luminance signal for the dropout compensator.

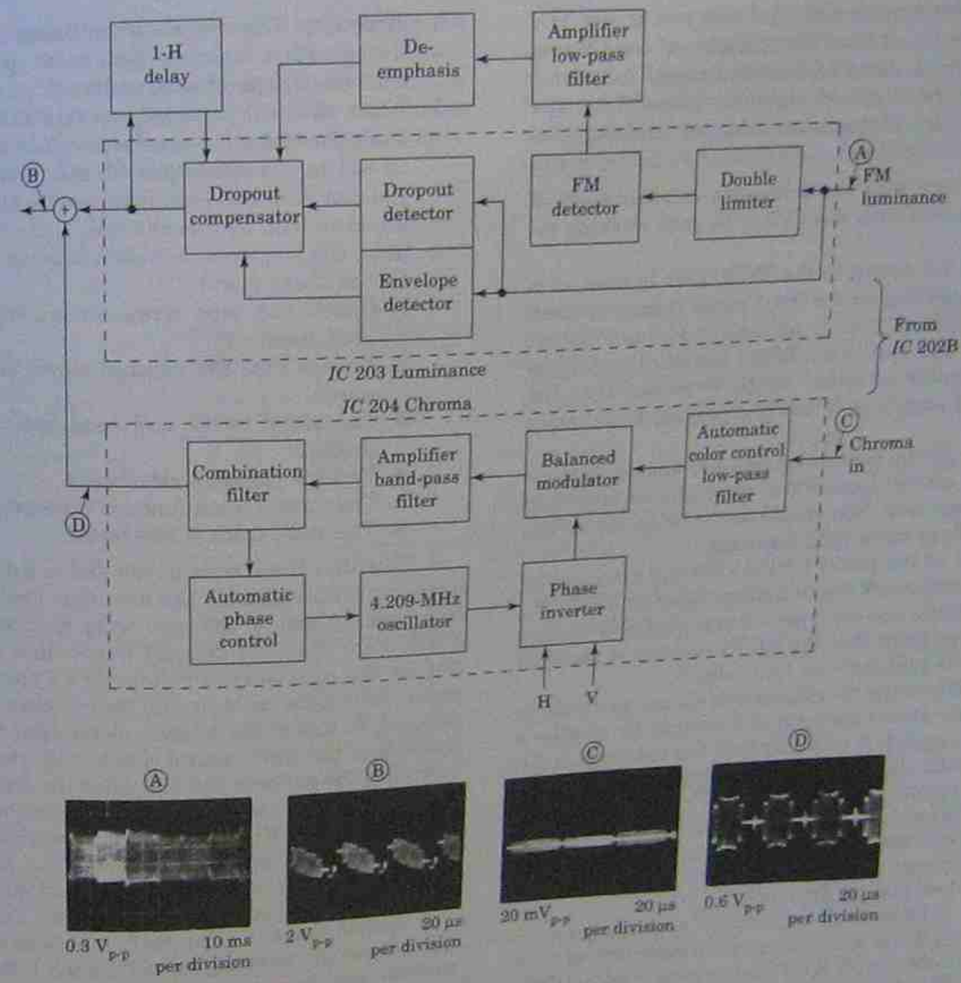


FIGURE 17.18
Playback signal processing.
(Courtesy Thomson Consumer Electronics, Inc.)

The chrominance portion of the playback signal from the head switching circuits at 629.37 kHz is fed into *IC* 204 in Figure 17.18, where it is applied to an automatic color control (ACC) and a low-pass filter. From here, the chroma signal goes to a balanced modulator for up conversion to 3.579545 MHz.

A carrier oscillator signal at 4.209 MHz is also fed into the balanced modulator along with the 629.37-kHz color signal for the up conversion of the chroma signal. The output from the balanced modulator is the sum and difference frequencies of the two input signals. The difference frequency is 3.58 MHz to be passed on to the combining circuit, and the sum frequency is 4.838 MHz. The upper sideband of 3.58 MHz and the lower sideband of 4.838 MHz are about $\frac{1}{2}$ MHz apart and require a sharp cutoff filter to separate the two signals. The COMB filter does this job nicely.

17.5 TROUBLESHOOTING VCRs

You may have guessed that there is more than one way to troubleshoot a system. With some experience, you will start to develop your own testing sequence. This is good, because it shows that you un-

derstand the system and that you can think. The outline given here tests the operation of the RF section first, then some of the mechanical functions, and then the playback section, followed by the record section. The synchronizing (or tracking) section is examined last.

1. Make sure that the television receiver used in conjunction with the VCR is in good working order.
2. Check for power to the VCR. This is seen as a clock reading on the front panel indicator when the VCR is turned off and a status readout when the unit is on. When the front panel has no display in either mode, it means that the power supply is defective and must be repaired first.
3. Turn on the companion receiver and set it to receive either channel 3 or 4, whichever is unused in your area. You should see snow on the screen and hear static in the speaker.
4. Turn on the power for the VCR and manually or remotely work the channel selector for the VCR.
   a. When you can view several channels clearly, you know that the full RF sections of the VCR are working well. Go to step 5.
   b. When the viewing screen clears up (little or no snow) but you are unable to receive a channel, it tells you that the transmitter circuit is working, including the TV–VCR switch.
   c. When the TV–VCR switch is activated back and forth with no difference on the viewing screen, the TV–VCR switch or its control section may be defective.
   d. If steps b and c indicate a working system and you are still unable to view several channels, the VCR receiver section is not working. That is, the tuner, video IF, and detector may be in trouble.
5. The first mechanical test is to see if the VCR will accept a cassette. With the power on, load a cassette into the loading door.
   a. When the VCR will not accept a cassette, the elevator up–down switch or motor or control chip is not operating. Check Figure 17.11 for these switch functions. *Note:* You will need to remove the top and bottom covers and then blindfold the two reel end sensor transistors. This is done by placing a piece of masking tape over the flat surface of the transistor. Letting ambient light into the working section will activate the sensors and tell the control chip that tape cannot be moved in either direction. The switches and motor can be tested with a voltmeter with power applied or with an ohmmeter with power off.
   b. When the recorder accepts a tape and downloads the cassette, test the play function. Use an old tape prerecorded for these tests that you can afford to lose. Six separate functions are examined by this one test. If any function fails, the sequence is halted because the defect has been found.
      1. Check the tape wrap around the head drum assembly.
      2. Ensure that the capstan moves tape forward.
      3. The video heads and head switching is checked.
      4. Test the playback electronics.
      5. The control track function is tested.
      6. The audio track is also tested.

Note that these tests do not define a defective component; they identify the area that needs to be examined. In test 1, the tape wrap mechanism is driven from the head cylinder motor. It is easy to test for the lack of drive voltage or an open drive motor. When the motor runs, the problem is mechanical. In test 2, the capstan motor drive voltage comes from the servo control chip to help you to decide when the motor is bad and when the drive voltage is missing. Tests 3 and 4 can be combined into one observation. When the circuit is working, the results will be a picture display on the receiver viewing screen. Remember that step 4A has verified that the transmit section is all right. You have now verified that the video heads and head switching sections are working, as well as the luminance and chroma processors, the adder, and switch S_{2a} in the playback mode.

Failure of the control track of test 5 will be identified by a video display that has no vertical or horizontal sync. In many video tape recorders, the loss of sync also causes loss of the color operation, which can be checked later. When the cylinder frequency generator (FG), the capstan pulse generator (PG) signals, and the playback signals from the control head are all found to be OK, the servo control section may be defective. The most common fault in this section is dirt on the head surface. Clean the heads with rubbing alcohol and cotton swabs.

The audio signals are easily traced with an oscilloscope in the playback mode. The high-frequency bias signal is only used in the record mode and is filtered out in the playback mode.

The record circuits are tested by checking the signal at the video detector output and then through the record circuits *IC* 202A, *IC* 203A, and *IC* 204A with an oscilloscope. The tape heads, the head switching section, and the servo control have all been tested in the playback mode.

When the video recorder is part of a camcorder, the playback screen is the view finder, shown in dashed lines on Figure 17.19, and is tested with an oscilloscope by signal tracing. The pickup device may be a vidicon tube in older products or a CCD in later models. See Section 16.5.3.

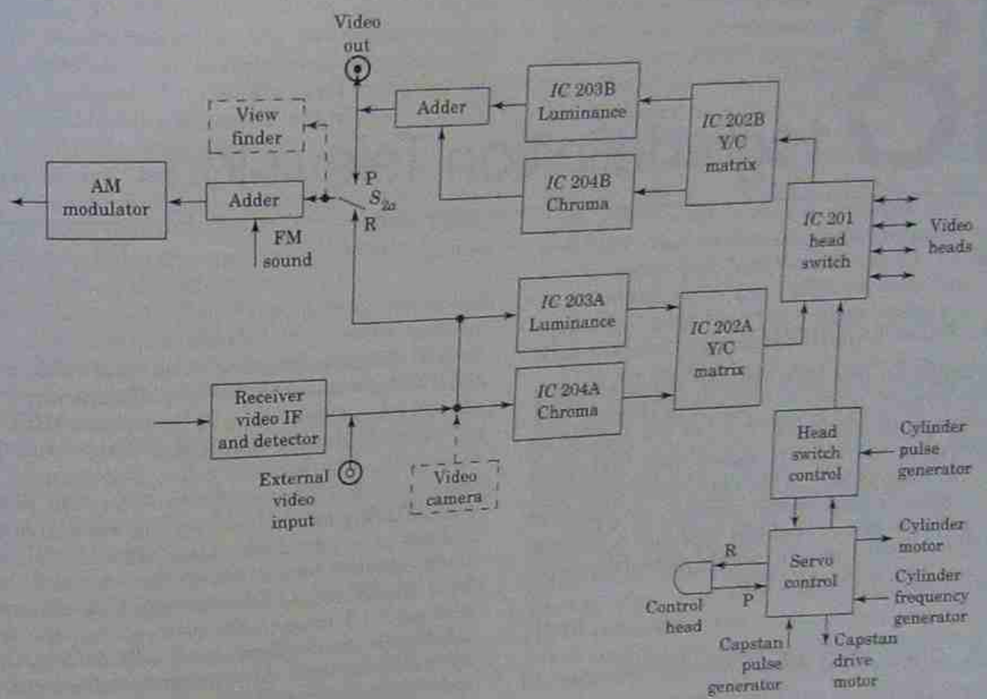


FIGURE 17.19
Block diagram for testing the video record and playback circuits.

18 High-definition Television

18.1 INTRODUCTION

High-definition television (HDTV) is not a reality for the general public yet, but it is coming, and sooner than we may think! You will not want to be caught short when you encounter your first exposure. So, what exactly is high definition television? It is a movement to greatly improve the quality of the television picture and add digital data communication packets that will require major changes in the system as we know it today.

18.2 EXPECTED IMPROVEMENTS

The current NTSC system uses 525 horizontal scan lines. HDTV will more than double this number to between 1050 to 1920 scan lines, changing the horizontal frequency.

The 60-hertz (Hz) vertical rate will change to a 24, 30, and 60 frames per second progressive scan with a pixel format of 1280 × 720 (number of picture elements per line times the number of active lines) and 24 and 30 frames per second progressive scan with a pixel format of 1920 × 1080. The system is also capable of 60 frames per second interlaced scan with a pixel format of 1920 × 1080.

The video bandwidth, which has been limited to 4.2 megahertz (MHz), will be increased to 30 MHz under the new system. Then, from equation 5.1, the lines of horizontal resolution can be found to be the square root of 2, times the time for one cycle of the horizontal frequency (26 microseconds from 31,500 Hz), times the video bandwidth, and is equal to 1104 lines of resolution. Comparing this to the 310 lines of resolution in the present NTSC system, this is about a 3.56 times better horizontal resolution. The picture, color, five-channel surround sound (Dolby AC-3), and the data packets will all be digitalized, making this resolution comparison only a crude estimate. The 30-MHz combined signal will be compressed into a 4-MHz bandwidth using a Reed–Solomon frequency compressor with an 8 : 1 compression ratio so that the entire intelligence modulated signal will fit into the 6-MHz channel bandwidth currently being used. The video information will be an eight-level vestigial sideband, suppressed carrier terrestrial transmission called 8-VSB, and the higher data rate cable system is a 16 level VSB, which will allow the cable operators to transmit two full HDTV signals on a single 6-MHz cable channel.

The aspect ratio, now set at 4 : 3, will be increased to a wider picture having a ratio of 16 : 9. This means that for an equal height under both systems the HDTV screen will be 33.3% wider than the current screen size.

18.3 HDTV TIMETABLE

Early in 1987, broadcasters petitioned the FCC to open investigations on advanced television standards. The invitation went out for anyone to submit proposals for the improved systems. The Advisory Committee on Advanced Television Services (ACATS) was commissioned. An event calendar was drafted that would target the sequence of dates for each phase of the new program, as follows:

Step 1. By September 1988, 23 proposals were submitted. Six systems had working hardware that was tested.

Step 2. Early 1990: The FCC decided to allow transmission on the currently unused channels for a simulcast approach, first proposed by Zenith, and broadcasters would be assigned a second channel for HDTV transmission.

Step 3. Spring 1990: General Instrument announced an all-digital system and was soon followed by M.I.T., Phillips–Thomson–Sarnoff, and Zenith–AT&T groups with all digital systems.

Step 4. Early 1993: The FCC advisory committee recommends HDTV transmission systems. Five months of field testing begin.

Step 5. Late 1993: FCC selects national HDTV standards.

Step 6. 1994–1995: TV stations apply for HDTV licenses.

Step 7. 1996–1998: Stations build HDTV facilities.

Step 8. 1999–2002: Stations develop HDTV programs and begin simulcasts for sending the same programs to conventional sets in the NTSC format and the HDTV sets with the new standards.

Step 9. 2008: All TV transmissions in the United States are converted to the high-definition standards. The NTSC system, which has been the standard since 1941, is phased out completely. All broadcasters will return the presently used channels back to the FCC for reassignment to other services.

Let's first examine how these changes will affect the general public and then how they will affect the service industry.

18.4 EFFECTS ON THE GENERAL PUBLIC

The planned calendar may often differ greatly from the actual performance of the events because of unforeseen obstacles. For instance, the 5 months of field testing planned for 1993 (step 4) were then scheduled for March 1995, with hopes of a demonstration system in place at the 1996 Summer Olympics in Atlanta, Georgia.

Step 7 will require the approximately 1500 TV stations in the United States to each invest between $12 million and $15 million in new transmitting equipment (at today's prices), suggesting a total expenditure of $18 billion.

Step 8 directs the television stations to develop HDTV programs and simultaneously broadcast them in both types of signal formats while the general public purchases new receivers that will accept the new HDTV standards. The estimated cost of a HDTV receiver is $1000 to $2000 *more* than the top-priced large screen sets available today.

Combining steps 7 and 8, the television station management and the advertisers will be reluctant to invest $12 million or more to be on the air with HDTV until there is an audience with HDTV receivers to help defray the costs. The public will be unwilling to buy HDTV receivers at the higher prices until there are sufficient programs. This could take more than the 8 years (steps 8 to steps 9) as planned in the outline.

Every large project must have a sequence of events calendar in order to ensure that the cart is not placed before the horse. However, the assigned dates may or may not turn out exactly as planned. This does not make the plan invalid; it only pushes the time for the events further down the scale.

How will the end of the NTSC system affect consumers with a large library of video tapes and NTSC video camcorders or VCRs? First, it is planned that new VCRs and camcorders with HDTV parameters will be phased in along with the television receivers. Second, history has shown that the older NTSC receivers will be around for a reasonable number of years after the switchover has been initiated and that conversion methods will allow the NTSC tapes to be reformatted to the new HDTV system in much the same way that consumers have converted their home movies onto tapes.

18.5 EFFECTS ON THE SERVICE INDUSTRY

The new system will affect the service industry probably much less than you may at first imagine, based on the facts just presented.

18.5.1 Circuits That Should Not Change

First, let's look at some circuits that in all likelihood will not change or will change so little that they can be considered to be the same circuits.

The wide-screen color cathode ray tubes are already being developed, and since we have already studied servicing CRTs in Section 15.5.4, there should be only small differences in the procedure with the newer wide-screen CRTs. The differences will be in the shape of the screen and the angle of deflection. The CRT will still require a deflection yoke that will be driven from the vertical-deflection and the horizontal-deflection circuits. The vertical and horizontal will be able to operate over a large range of frequencies that will be synchronized by the new formatted sync pulses.

The horizontal output amplifier will still drive the flyback transformer to develop the high voltage, the focus voltage, and the scan-derived dc voltage sources. You can depend on Section 15.5.1 to service the vertical circuits and on Section 15.5.2 to service the horizontal and high-voltage circuits with almost no changes.

The low-voltage power supply circuit is unchanged and will most likely be of the switching type of supply circuits. Section 15.5.3 will still apply to servicing the low-voltage power supply circuits.

18.6 NEW SIGNAL CIRCUITS

The following is extracted directly from publications of the Digital HDTV Grand Alliance draft document.

18.6.1 System Overview

The Grand Alliance (GA) vestigial sideband (VSB) digital transmission system provides a basis for a family of transmissions suitable for data transmission over a variety of media. This family shares the pilot signal, symbol rate, interleaving, Reed–Solomon coding, and synchronizing pulses. The VSB takes two modes: a simulcast terrestrial broadcast mode and a high-data cable mode. The terrestrial broadcast mode, which transmits an advanced television (ATV) signal on currently unused taboo NTSC channels with minimum interference to or from other NTSC channels, is optimized for the maximum coverage area and supports one ATV signal in a 6-MHz channel. The higher-data-rate cable mode, which trades off some robustness for twice the data rate, supports two ATV signals in one 6-MHz channel.

The VSB transmission systems (both modes) take advantage of a pilot signal, a segment sync, and a training sequence for robust acquisition and operation. The two systems also share identical carrier, sync, clock, and clock recovery circuits, as well as phase correctors and equalizers. Additionally, both systems use the same Reed–Solomon (RS) code for forward error correction (FEC).

To maximize the coverage area, the terrestrial broadcast mode incorporates both an NTSC rejection filter (in the receiver) and trellis coding. When the NTSC rejection filter is activated in the receiver, the trellis decoder is switched in series with the filter.

The cable mode, on the other hand, works in a less severe environment than the terrestrial mode and therefore has a higher data rate in the form of more data levels (bits per symbol). No trellis coding or NTSC rejection filters are used in this mode.

VSB transmission requires only processing of the in-phase (I) channel signal, sampled at the symbol rate, which optimizes the receiver for low-cost operation. The decoder requires only one A/D converter and a real equalizer operating at the symbol rate of 10.76 MHz symbols per second. The parameters for the two VSB transmission modes are shown in Table 18.1.

18.6.2 System Information

The VSB system transmits data according to the data frame shown in Figure 18.1. The frame is organized into segments of 836 symbols each. Each segment consists of a four-symbol sync segment followed by 832 data plus FEC (forward error correction) symbols. The data contained in each 208-byte segment are a 188-byte MPEG (moving picture expert group) compatible data packet with 20 R–S (Reed–Solomon) parity bytes. The exact symbol rate is

$$\frac{4.5}{286}\ \text{MHz} \times 684 = 10.76\ \text{MHz}$$

The frequency of a segment may be calculated as

$$f_{seg} = \frac{10.76\ \text{MHz symbols/s}}{836\ \text{symbols/seg}} = 12.87\ \text{kHz symbols/s}$$

For the terrestrial broadcast mode, each segment corresponds to one R–S correction block of 208 bytes as follows:

$$208\ \text{bytes/block} \times 8\ \text{bits} \times \tfrac{1}{2}\text{trellis} = 3\ \text{bits/symbol} \times 832\ \text{symbols} = 2496\ \text{bits}$$

For the high-data-rate cable mode, each segment corresponds to two R–S correction blocks of 208 bytes, as follows:

$$2\ \text{blocks} \times 208\ \text{bytes/block} \times 8\ \text{bits} = 4\ \text{bits/symbol} \times 832\ \text{symbols} = 3328\ \text{bits}$$

As seen in Figure 18.1, each data frame begins with a first field vertical sync segment followed by 312 data segments, then the second data field vertical sync segment, and another 312 data segments.

Except for the binary data segment and data field sync, all other symbols are multilevel. For the terrestrial broadcast mode, 8-level symbols (3 bits/symbol) are transmitted, while for the higher-data-rate cable mode, 16 levels (4 bits/symbol) are used. These are called 8-VSB and 16-VSB, respectively.

The multilevel symbols combined with the data segment and field syncs are used to suppress carrier amplitude modulate a single carrier. However, before transmission the lower sideband is removed. The resulting spectrum is flat except for the band edges, where a root-raised cosine response re-

TABLE 18.1
VSB Parameters

Parameter	Terrestrial Mode	High-data-rate Cable Mode
Channel bandwidth	6 MHz	6 MHz
Excess bandwidth	11.5%	11.5%
Symbol rate	10.76 million symbols/s	10.76 million symbols/s
Bits per symbol	3	4
Trellis FEC	½ rate	None
Reed–Solomon FEC	$T = 10$ (208,188)	$T = 10$ (208,188)
Segment length	836 symbols	836 symbols
Segment sync	Four symbols per segment	Four symbols per segment
Frame sync	One per 313 segments	One per 313 segments
Payload data rate	19.3 Mb/s	38.6 Mb/s
NTSC co-channel rejection	NTSC rejection filter in receiver	N/A
Pilot power contribution	0.3 dB	0.3 dB
C/N threshold	14.9 dB	28.3 dB

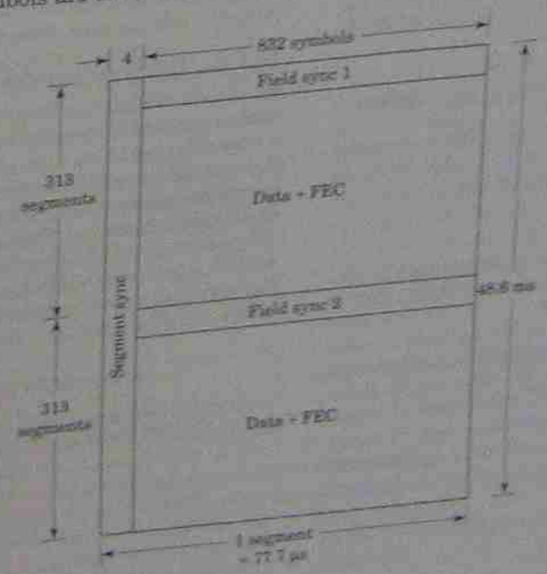


FIGURE 18.1
VSB data frame.

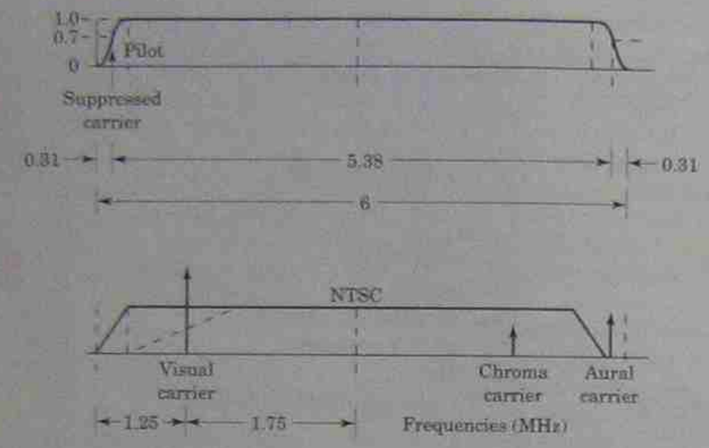


FIGURE 18.2
VSB and NTSC channel occupancy.

sults in a 620-kilohertz (kHz) transition region. The VSB transmission spectrum relative to the NTSC spectrum is shown in Figure 18.2.

A small pilot signal is added to the suppressed carrier envelope at 310 kHz above the lower band edge. This is the position of a co-channel NTSC signal and does not contribute to co-channel interference into NTSC transmissions. The pilot signal is used to achieve carrier lock.

Forward error correction in the form of R–S and trellis coding, along with one-third data field interleaving, provides a system that can endure both white noise and environmental interference. The VSB terrestrial system can operate well in signal-to-noise ratio (S/N) of 14.9 dB (3×10^{-6} BER) bit error rate.

18.7 TRANSMITTER BROADCAST MODE

A functional block diagram of the VSB terrestrial broadcast transmitter is shown in Figure 18.3 and is described in the following paragraphs.

18.7.1 Data Randomizer

A data randomizer is used on all input data to randomize the data payload (not including the sync or the R–S parity bytes). This ensures that random data are transmitted even when constant data are applied to the system, as might happen when the data input is disconnected. Random data are important for optimum reception of the transmitted signal.

The data randomizer exclusive-ORs all incoming data bytes with a 16-bit-maximum-length pseudorandom sequence (PRS) locked to the data frame. The PRS is generated in a 16-bit shift register that has nine feedback taps. Eight of the shift register's outputs are selected as the fixed randomizing byte, where each byte is used to individually exclusive-OR the corresponding input data bit.

18.7.2 Reed–Solomon Encoder

The Reed–Solomon (R–S) error protection code, known for its burst noise correction capabilities, is a very efficient block code with low parity overhead. Since it works with bytes (8 bits), any number of bit errors can occur within a byte and not affect its error-correction ability. Therefore, there is no direct proportional relationship between byte error rate and bit error rate. Only at very low error rates do the two factors converge, but the bit error rate is never smaller than the byte error rate with the

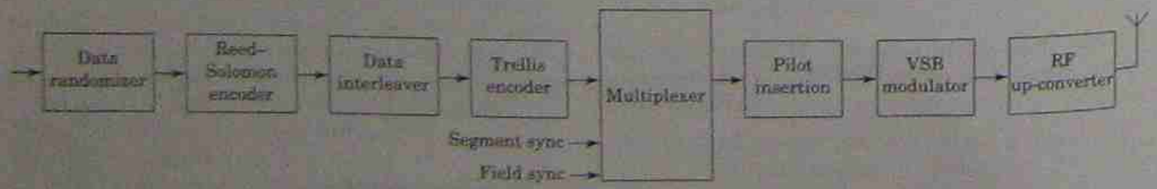


FIGURE 18.3
VSB terrestrial transmitter.

same S/N ratio. The measure of performance for block codes is its packet error rate versus signal-to-noise ratio, or signal-to-interference ratio. Since ATV data is to be transmitted in MPEG transport packets, the most common method of describing data transmission performance in signal and interference conditions is the probability of data packet errors.

The R–S code used in the VSB transmission system is a $t = 10$ (208,188) code. The data block size is 188 bytes with 20 R–S parity bytes added for error correction. A total block size of 208 bytes is transmitted per data segment. A $t = 10$ R–S code with 20 parity bytes can correct up to 10 byte errors per block.

18.7.3 Interleaver

Although the R–S code is particularly powerful in protecting against burst errors, the data are interleaved for further protection. Burst errors result from both impairment and trellis decoding mistakes, where a single error can propagate through the trellis decoder, multiply, and become a burst error. Long trellis decoders (large K) cause correspondingly longer burst errors to be created.

The goal of the interleaver is to spread to data bytes from the same R–S block over time so that a long burst of noise is necessary to encompass more than 10 data bytes and overrun the R–S error protection. Since the R–S code can correct up to 10 byte errors per block regardless of how many bit errors may occur within each byte, it is advantageous to group consecutive symbols from the trellis decoder into bytes to get the best burst error performance.

The interleaver in the VSB transmission system is an 87-data-segment (intersegment) diagonal byte interleaver. Interleaving is provided to a depth of about one-third of a data field (5.5 ms deep). Intrasegment interleaving is also performed for the benefit of the trellis coding process, to be described next.

18.7.4 Trellis Coding Modulation

The terrestrial broadcast VSB transmission system employs a two-thirds rate ($R = \frac{2}{3}$ trellis code (with one unencoded bit). That is, one input bit is encoded into two output bits using a one-half rate convolution code, while the other input bit is left unencoded. The signal waveform used with the trellis code is an eight-level (3-bit), 1-dimensional constellation, referred to as 8-VSB. To minimize the complexity of interleaving and trellis decoder hardware, as well as to minimize error propagation, a relatively simple (short) four-state trellis encoder is used. A long code that causes longer burst errors and requires more interleaving was not found to be beneficial.

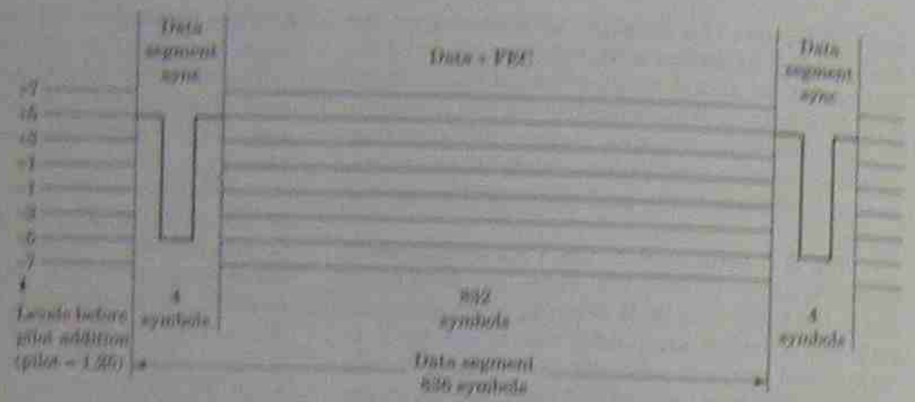
Although trellis codes produce improvements in S/N ratio threshholds against white noise, they do not perform well for impulse or burst noise. Burst noise and phase noise are caused by NTSC co-channel interference, which can cause data-dependent crosstalk. To further reduce the effects of burst errors and to simplify the trellis decoder when the NTSC rejection filter is used, trellis code interleaving is used. This uses 12 identical trellis encoders operating on interleaved data symbols. The code interleaving is accomplished by encoding symbols (0, 12, 24, 36,...) as one group, symbols (1, 13, 25, 37,...) as a second group, and symbols (2, 14, 26, 38,...) as the third group, and so on, for a total of 12 groups. The 12 groups are used since the creation of spectral nulls in the receiver requires a comb filter with delays of 12 symbols.

18.7.5 Synchronization Information

The sync information is added to the digital data signal in order to achieve packet and symbol clock acquisition and phase lock during extreme noise conditions. The encoded trellis data are passed through a multiplexer (mixer) that inserts the data segment sync (horizontal) and data frame sync (vertical).

A two-level (binary) four-symbol data sync segment signal is inserted into the eight-level digital data stream at the beginning of each data segment. The data sync segment is embedded in the random data, as seen in Figure 18.4. A complete segment consists of 836 symbols made up of 4 sync symbols and 832 data plus parity symbols. The sync is a two-level binary segment between +5 and −5 volts (V) in order to make packet and clock recovery rugged and does not cause undue interference into the co-channel NTSC signal. They also have an average value of zero so that when the dc pilot signal is added they will not alter the desired value of the pilot. The same sync pattern occurs regularly at the horizontal sync rate and is the only signal at this rate. The periodic reoccurrence of these four symbols make possible their detection at the receiver under severe noise conditions. Unlike the data, the four sync segments are not Reed–Solomon or trellis encoded, nor are they interleaved.

FIGURE 18.4
VSB data segment (horizontal).



The data are divided into data fields and data segments. Each data field starts with one complete data segment of data field sync, as seen in Figure 18.5, made up of binary (two-level) pseudorandom sequences of 511 and 63 symbol packets. The 12 symbols at the end of the field are repeated from the previous active data segment to aid the trellis decoder in the receiver during co-channel interference when the NTSC rejection filter is in the path (12-symbol subtractive comb). Binary levels provide reliable detection of the data sync under extremely adverse channel conditions.

The three groups of 63-bit PRS segments in the field sync alternate polarity from one field to the next, providing field identification information to the receiver. Therefore, there are two data field syncs that make up one data frame (48.6 ms). The average value of the field sync symbols is close to zero so that when the dc pilot is added to the transmission they will not alter the desired value of the pilot.

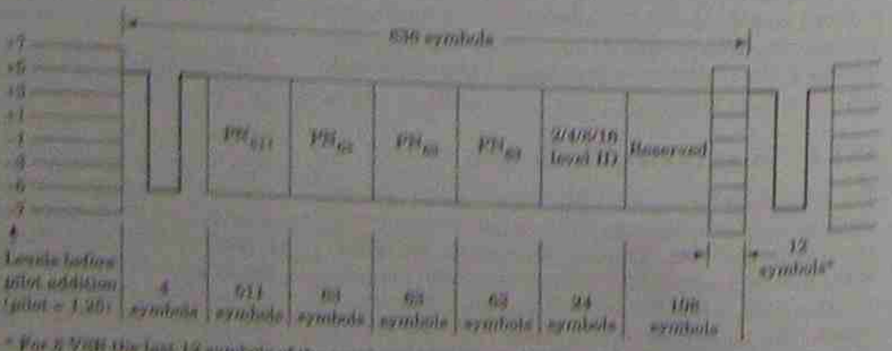
The data field sync serves five purposes: (1) It provides a means to determine the beginning of each data field. (2) It is used by the equalizer in the receiver as a training reference signal to remove intersymbol and other interferences. (3) It allows the receiver to determine when the interference rejection filter (12-symbol subtractive comb) should be used. (4) It is used for system measurements, such as S/N and channel response. (5) The phase tracker in the receiver uses the field sync to reset its circuitry and determine its loop parameters. Just like the data segment sync (horizontal), the field sync (vertical) is not Reed–Solomon or trellis encoded, nor is it interleaved.

18.7.6 Pilot Insertion

A reliable system must be able to acquire a signal and maintain lock in the presence of very heavy noise and interference. A small pilot added to the suppressed carrier RF data signal is adequate to allow for carrier recovery in the receiver during these extreme conditions.

A small (digital) dc level (1.25 V) is added to every symbol of the digital baseband data plus sync

FIGURE 18.5
VSB data field sync.



* For 8 VSB the last 12 symbols of the previous segment are duplicated in the last 12 reserved symbols of the field sync.

signal (±1, ±3, ±5, ±7 V). This has the effect of adding a small in-phase pilot to the data signal. Digital addition of the pilot (at baseband) provides a highly stable and accurate pilot. The frequency of the pilot will be the same as the suppressed carrier frequency. Since the data are guaranteed to be random over long intervals, all data states are equally probable. Using the above eight values for the random data symbols, the total average data power of the eight levels is 21. After adding the pilot, the total average signal power is 22.56. Thus the pilot represents an increased transmitter power of 0.3 decibels (dB). In the interference limited environment, the pilot is not a contributing factor. Furthermore, the pilot power has no significant effect on the ATV transmitter hardware.

18.7.7 Presequalizer Filter

A filter is available for use in over-the-air broadcasts when the high-power transmitter may have in-band ripple and roll-offs at the band edges. This linear distortion can be detected by an equalizer in the reference demodulator (ideal receiver) located at the transmitter site that is receiving a small portion of the antenna signal (as a sample). The reference demodulator equalizer tap weights can be transferred into the transmitter presequalizer for precorrection of the linear distortion. The presequalizer is an 80-tap, forward transversal filter. It operates on the *I* channel data signal and shapes the frequency spectrum of the IF signal so that it is a flat spectrum at the output of the high power transmitter that feeds the antenna.

18.7.8 VSB Modulation

The VSB modulator receives the 10.76M symbols/second eight-level trellis composite data signal (pilot plus syncs added). For minimum intersymbol interference, the data signal must be properly shaped (filtered) before it is transmitted over the 6-MHz channel. A linear phase raised cosine Nyquist filter is employed in the transmitter and receiver, as shown in Figure 18.6. The system filter response is essentially flat across the entire band, except for the transition regions at the ends of the band. Due to the vestigial sideband nature of the transmitted signal, the same skirt selectivity on both sides is not required, although it is implemented. The optimum system arrangement is to divide the roll-off equally between the transmitter and receiver filters. Therefore, root-raised cosine filters are used.

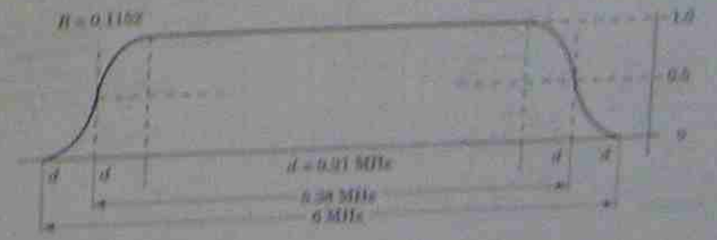
The transmitter VSB response is implemented by complex filtering of the baseband data signal, creating precision filtered and stable in-phase and quadrature-phased modulation signals. This filtering provides the Nyquist filter as well as the sin x/x compensation for the D/A converters. The orthogonal baseband signals are converted to analog and then modulated on quadrature IF carriers to create the vestigial sideband IF signal by sideband cancellation (phasing method). The nominal frequency of the IF carrier is 46.69 MHz, which is equal to the IF center frequency plus the data rate divided by 4: 44 MHz + (10.762 MHz/4) = 46.69 MHz. Additional adjacent channel suppression is performed by a linear phase, flat amplitude response SAW filter. Adjacent channel energy spillage at the IF output is at least −57 dB below the ATV signal power.

18.7.9 Upconverter and RF Carrier Frequency Offset

The VSB TV transmitters use a two-step modulation process. The first step usually is modulation of the data onto an IF carrier, which is the same frequency for all channels, followed by the translation to the desired RF channel frequency.

The frequency of the upconverter oscillator in the ATV terrestrial broadcast is typically the same as that used for the NTSC, except for the NTSC offsets. Since the VSB data signal sends repetitive synchronizing information into the VSB receiver (segment syncs), precise offset causes NTSC co-

FIGURE 18.6
Nominal VSB system channel response (linear phase raised cosine Nyquist filter).



channel carrier interference into the VSB receiver to phase alternate from sync to sync. The VSB receiver circuits average successive syncs to cancel the interference and make data sync detection more reliable.

The ATV co-channel pilot should be offset in the RF upconverter from the dominant NTSC picture carrier by an odd multiple of half the data segment rate. A 56.9 × horizontal frequency = 56.9 × 15,734.26 Hz = 895.28 kHz offset is proposed between the pilot frequency and the co-channel NTSC picture carrier frequency. To achieve this requirement, a 45.8-kHz spectrum shift of the VSB signal into the upper adjacent channel is required.

18.8 RECEIVER BROADCAST MODE

Figure 18.7 shows the receiver block diagram of the VSB terrestrial broadcast transmission system. A description of each block follows.

18.8.1 Tuner

The tuner, illustrated in Figure 18.8, receives the 6-MHz ATV signal from the antenna. It is a high-injection, double-conversion type with the first IF frequency at 920 MHz. This puts the image frequency well above 1 gigahertz (GHz), making it easy to reject by a fixed front end filter. This selection of the first IF frequency is high enough so that the input passband filter selectivity prevents the local oscillator (970 to 1723 MHz) from leaking out of the tuner front end and interfering with other UHF channels; yet it is low enough for second harmonics of the UHF channels (470 to 806 MHz) to fall above the first band-pass. Harmonics of the cable channels could possibly occur in the first IF band-pass, but are not a real problem because of the relatively flat spectrum (within 10 dB) and small signal levels (−28 dB or less) used in the cable systems.

The tuner input has a bypass filter that limits the frequency range to 50 to 810 MHz, rejecting all other nontelevision signals that may fall within the tuner's image frequency range (beyond 920 MHz). In addition, a broadband tracking filter rejects other television signals, especially those much larger in signal power than the desired signal power. This tracking filter is not narrow, nor is it critically tuned, as is the case in present-day

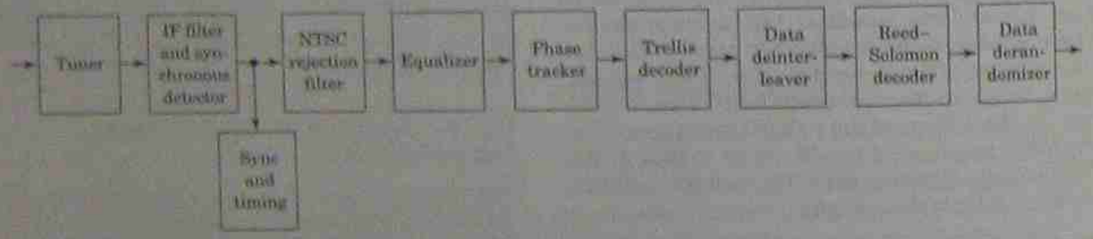


FIGURE 18.7
Terrestial VSB receiver.

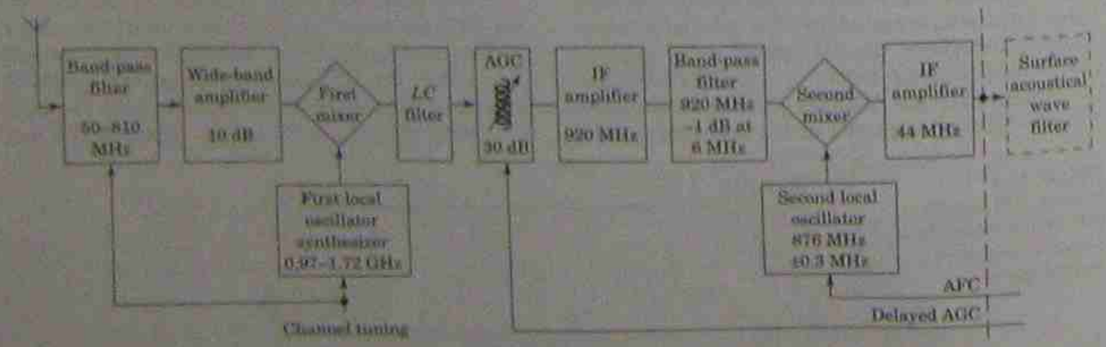


FIGURE 18.8
Tuner block diagram.

NTSC tuners that must reject image signals only 90 MHz away from the desired channel. Minimum channel tilt, if any, exists due to this tracking filter.

A 10-dB-gain, wideband RF amplifier increases the tuner signal level into the first mixer and is the dominant determining factor of receiver noise figure (7 to 9 dB over the entire VHF, UHF, and cable bands). The first mixer, a highly linear double-balanced circuit to minimize even-harmonic generation, is driven by a synthesized low-phase-noise local oscillator (LO) above the first IF frequency, (high-side injection). Both the channel tuning (first LO) and the broadband tracking filter (input band-pass filter) are controlled by a microprocessor. The tuner is capable of tuning the entire VHF and UHF broadcast bands as well as the IRC and HRC cable bands.

The mixer is followed by an LC filter in tandem with a narrow 920-MHz band-pass ceramic resonator filter. The LC filter provides selectivity against the harmonic and subharmonic spurious responses of the ceramic resonators. The 920-MHz ceramic resonator band-pass filter has a −1-dB bandwidth of about 6 MHz. A 920-MHz IF amplifier is placed between the two filters. Delayed AGC to the first IF signal amplifier is applied immediately following the first LC filter. The 30-dB range of the AGC circuit protects the remaining active circuits from large signal overload.

The second mixer is driven by the second local oscillator (LO_2), which is an 876-MHz voltage-controlled SAW oscillator. It is controlled by the frequency and phase-locked-loop (F-PLL) synchronous detector. The second mixer, whose output is the desired 44-MHz second IF frequency, drives a constant-gain 44-MHz amplifier. The output of the tuner feeds the IF SAW filter and synchronous detector circuitry.

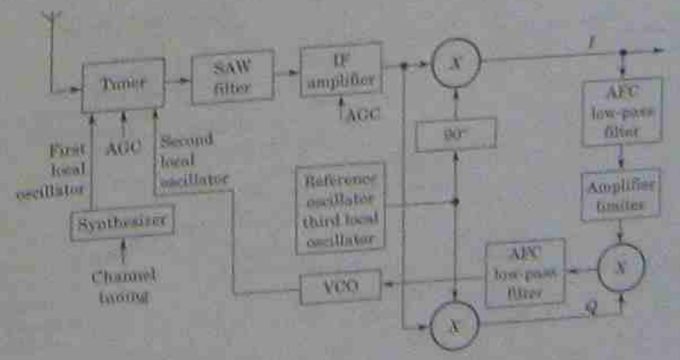
The tuner is made out of standard consumer electronic components and is housed in a stamped metal enclosure.

18.8.2 Channel Filtering and VSB Carrier Recovery

Carrier recovery is performed by the F-PLL circuit shown in Figure 18.9. The first local oscillator is synthesized by a PLL and controlled by a microprocessor. The third local oscillator is a fixed reference oscillator. Any frequency drift or deviation from normal has to be compensated for in the second local oscillator (VCO). Control of the second oscillator comes from the F-PLL synchronous detector, which contains both the frequency loop and the phase-locked loop in one unit. The frequency loop provides a wide-frequency pull-in range of ±100 kHz, while the phase-locked loop has a narrow bandwidth of less than 2 kHz.

During frequency acquisition, the frequency loop uses both the in-phase (I) and the quadrature-phase (Q) pilot signals. All other data-processing circuits in the receiver use only the I channel pilot signal. Prior to phase lock, as is the condition after a channel change, the automatic frequency control (AFC) low-pass filter acts on the beat signal created by the frequency difference between the VCO and the incoming pilot signal. The high-frequency data (as well as the noise and interference) are mostly rejected by the AFC filter, leaving only the pilot beat frequency. After limiting the pilot beat signal to a constant-amplitude (±1 V) square wave and

FIGURE 18.9
Tuner IF F-PLL.



using it to multiply the quadrature signal, a traditional bipolar S-curve APC characteristic is obtained, similar in effect to the S curve found in many FM detectors. The polarity of the curve depends on whether the VCO frequency is above or below the incoming IF signal frequency. Filtered and integrated by the automatic phase control (APC), low-pass filter, this dc signal adjusts the tuner's second local oscillator to reduce the difference frequency.

When the frequency difference comes close to zero, the APC loop takes over and phase locks the incoming IF signal to the third local oscillator. This is the normal phase-locked-loop circuit, with the exception that it is biphase stable. However, the correct phase polarity is determined by forcing the polarity of the pilot to be equal to the known transmitted positive polarity. Once locked, the detected pilot signal is constant, the limiter output feeding the third multiplier is at a constant +1 V, and only the phase-locked loop is active (frequency loop automatically disabled). The APC low-bass filter is wide enough to reliably allow ±100-kHz frequency pull-in, yet narrow enough to consistently reject all strong white noise (including data) and NTSC channel signals. The PLL has a bandwidth that is narrow enough to reject all amplitude- and phase-modulated interference generated by the data, yet is wide enough to track out any phase noise on the signal (and hence on the pilot) out to about 2 kHz. Tracking out low-frequency phase noise as well as low-frequency FM components allows the phase tracking loop to be more efficient.

18.8.3 Segment Sync and Symbol Clock Recovery

The repetitive data segment syncs are detected from among the synchronously detected random data by a narrow-bandwidth filter. From the data segment syncs, a properly phased 10.76-MHz symbol clock is created along with a coherent AGC control signal. Figure 18.10 is a block diagram of this circuit.

The 10.76 MHz symbol/s *I*-channel composite baseband data signal (sync plus data) from the synchronous detector is converted from analog to digital for digital processing. Traditional analog data eyes can be viewed after synchronous detection. However, after conversion to a digital signal, the data eyes cannot be seen due to the sampling process. A PLL is used to derive a clean 10.76-MHz symbol clock for the receiver.

With the PLL free running, the data segment sync detector containing a four-symbol sync correlator looks for the two-level syncs occurring at the specified repetition rate. The repetitive segment sync is detected while the random data are not, enabling the PLL to lock onto the sampled sync from the A/D converter and achieve data symbol clock synchronization. Upon reaching a predefined level of confidence (using a confidence counter) that the segment sync has found, subsequent receiver loops are enabled. Data segment sync detection and clock recovery both work reliably at signal-to-noise ratios of 0 dB or less and in the presence of heavy interference.

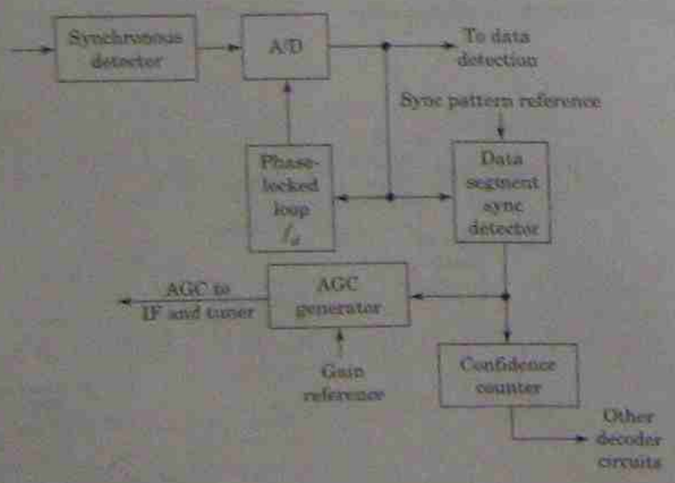


FIGURE 18.10
Segment sync and symbol clock recovery with AGC generation.

18.8.4 Coherent and Noncoherent AGC

Prior to carrier and clock synchronization, noncoherent automatic gain control (AGC) is performed whenever any signal (locked or unlocked, noise or interference) overruns the A/D converter. The IF and RF gains are reduced accordingly, with the appropriate AGC delay applied.

When the data segment syncs are detected, coherent AGC occurs using the measured segment sync amplitudes. The amplitude of the bipolar syncs, relative to the discrete levels of the random data, is determined in the transmitter. Once the syncs are detected in the receiver, they are compared to the reference value with the integrated difference error. The integrater output then controls the IF and delayed RF gains, forcing them to whatever values provide the correct sync amplitudes.

18.8.5 Data Field Synchronization

Data field synchronization, shown in Figure 18.11, is achieved by comparing each received data segment from the A/D converter (after rejection filtering to minimize co-channel interference) to an ideal field 1 and field 2 reference signal in the receiver. Oversampling of the field sync is not necessary since a precision data segment and symbol clock have already been created by the clock recovery circuit. Therefore, the field sync recovery circuit knows exactly where a valid field sync correlation should occur within each data segment and only needs to perform a symbol-to-symbol difference test. Upon reaching a predetermined level of confidence (from a confidence counter) that field syncs have been detected, the data field sync signals become available for use by the segment circuits. The polarity of the three alternating, 63-bit, pseuderandom field sync signal sequences determines whether field 1 or field 2 is detected.

This procedure makes field sync detection robust even in heavy noise, interference, or ghost conditions. Field sync recovery can occur at S/N ratios of 0 dB or less, even in the presence of heavy interference.

18.8.6 Interference Rejection Filter

The interference properties of the VSB transmission system are based on the principal components of the NTSC co-channel interfering signal within the 6-MHz TV channel and the periodic nulls of the VSB receiver baseband comb filter.

Figure 18.12a shows the location and approximate magnitude of the three principal NTSC components: (1) the visual carrier (*V*) located 1.25 MHz from the lower band edge, (2) the chrominance subcarrier (*C*) located 3.579545 MHz higher than the visual carrier frequency, and (3) the aural carrier (*A*) located 4.5 MHz higher than the visual carrier frequency.

The NTSC interference rejection filter (comb) is a one-tap linear feed-forward filter, as shown in Figure 18.13. Figure 18.12b shows the frequency response of the comb filter, which provides periodic spectral nulls spaced 56.9 times the horizontal scan frequency at 896.83 kHz apart. There are seven nulls within the 6-MHz channel. The NTSC visual carrier falls close to the second null from the lower band edge. The sixth null from the lower band edge is correctly placed for the chrominance subcarrier, and the seventh null from the lower band edge is near the NTSC aural carrier.

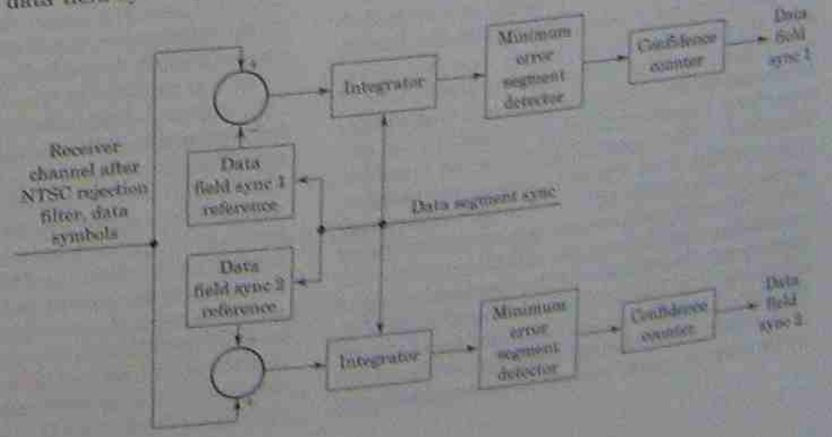


FIGURE 18.11
Data field sync recovery.

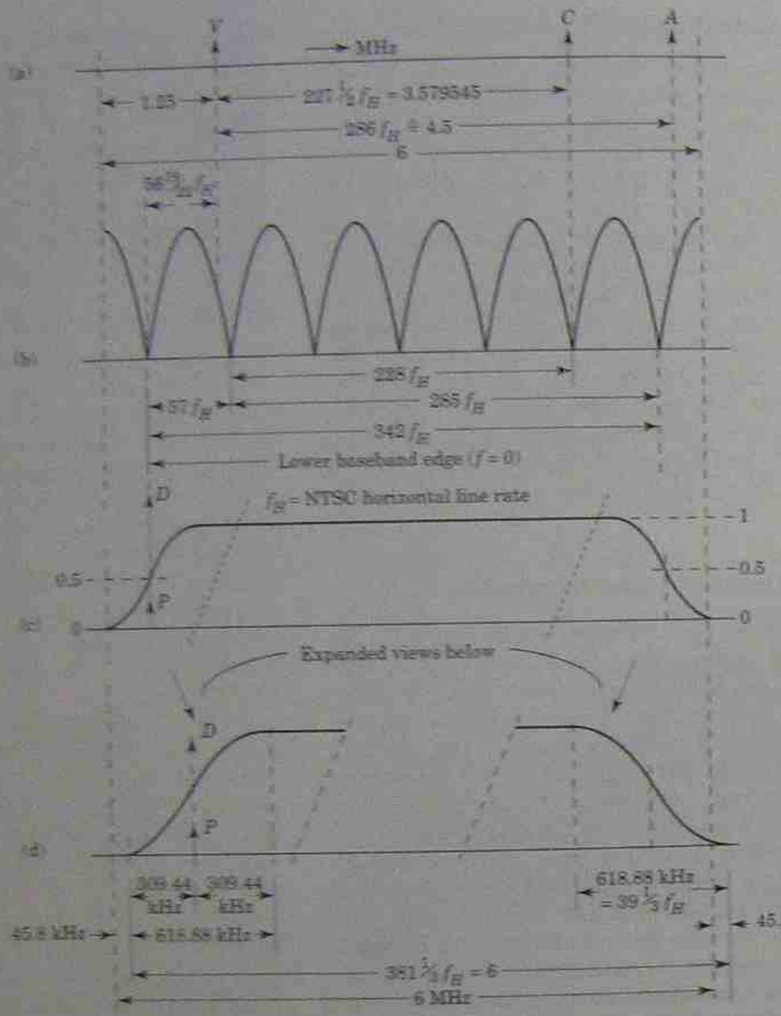


FIGURE 18.12
NTSC interference rejection filter spectrum occupancy.

Comparing Figure 18.12a and b shows that the visual carrier falls 2.1 kHz below the second comb filter null.

The comb filter, while providing rejection of steady-state signals located at the null frequencies, has a finite response time of 12 symbols (1.115 μs). Thus, if the NTSC interfering signal has a sudden step in carrier level, then one cycle of the beat frequency (offset) between the ATV and NTSC carrier frequencies will pass through the comb filter at an amplitude proportional to the NTSC step size as instantaneous interference. Examples of such steps of NTSC carrier are leading and trailing edges of sync (40 IRE units). If the desired-to-undesired signal power ratio is large enough, data slicing errors will occur. However, interleaving will spread the interference and make it easier for the Reed–Solomon code to correct them (R–S can correct up to 10 byte errors per segment).

Although the comb filter reduces the NTSC interference, the data are also modified. The 7 data eyes (8 levels) are converted to 14 data eyes (15 levels). Such a process is called *partial response*. The modified data signal can be properly decoded by the trellis decoder. Note, because of the time sampling, that only the maximum data eye value is seen after the A/D converter. The details for the band edges for the overall channel are shown in Figure 18.12c and d. Figure 18.12c shows that the frequency relationship (56$\frac{1}{3}$ times the horizontal frequency between the NTSC visual carrier and the ATV carrier) requires a shift in the ATV spectrum with respect to the nominal channel. The shift equals +45.8 kHz or about +0.76%. This is slightly higher than currently applied channel offsets and reaches into the upper adjacent channel at a level of about −40 dB. If that is another ATV channel, then the nominal situation is restored. If it is an NTSC channel, the shift is below the Nyquist slope (RF equivalent) of an NTSC receiver where there is high attenuation and is slightly above its customary lower adjacent sound trap. No adverse effects have been found nor are any foreseen.

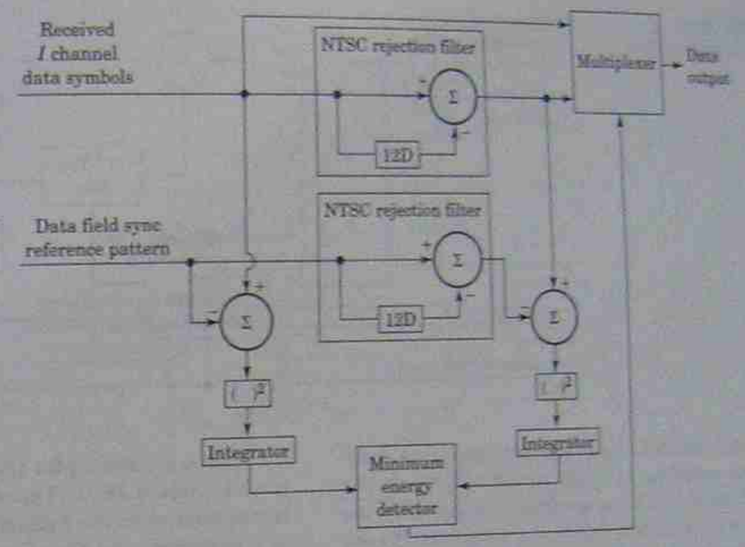


FIGURE 18.13
NTSC interference detection

NTSC interference can be detected by the circuit shown in Figure 18.13, where the signal-to-interference plus noise ratio of the binary data field sync is measured at the input and output of the comb filter and these are compared to each other. This is accomplished by creating an error signal at each rejection filter port and by comparing the received signal with a stored reference of the field sync. The errors are squared and integrated. After a predetermined level of confidence is achieved, the path with the largest S/N ratio is switched in and then out of the system automatically.

There is a reason for not leaving the rejection comb filter switched in all the time. The comb filter, which provides the needed co-channel interference benefits, degrades the white noise performance by 3 dB. This is due to the fact that the filter output is the subtraction of two full-gain paths, and since white noise is uncorrelated from symbol to symbol, the noise power doubles. If little or no NTSC interference is present, the comb filter is automatically switched out of the data path.

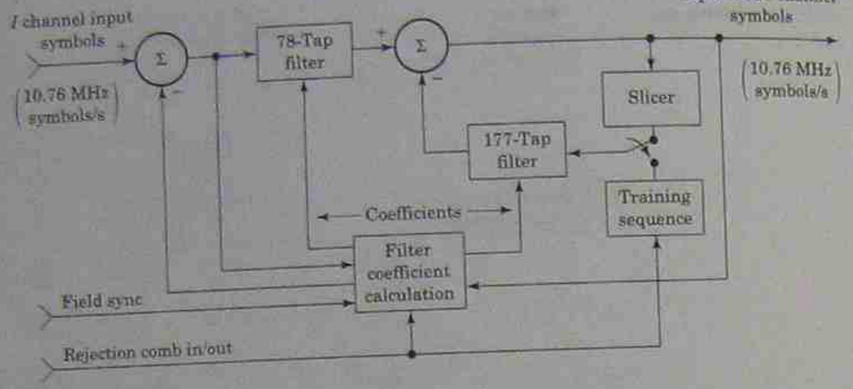
18.8.7 Channel Equalizer

The equalizer–ghost canceler is used to compensate for the linear channel distortions, such as tilt and ghosts. The distortion can come from the transmission channel or from imperfect components within the receiver. The equalizer delivered for testing uses a *least mean square* (LMS) algorithm and adapts to the binary data field as well as to the random data. A block diagram of the equalizer used in this system is shown in Figure 18.14.

The advantage for adapting to an unknown training signal embedded within the random data signal is the guarantee of the tap convergence, especially under extreme noise, ghost, and interference conditions. All the various loops within the receiver (carrier, clock, AGC, segment sync, frame sync) are independent of subsequent loops, including the equalizer. An optimum method is to use a two-step process: equalization first on a binary training sequence to open the data eyes, and then equalization on the random data for high-speed tracking of moving ghosts (airplane flutter).

The equalizer filter consists of two parts, a 78-tap feed-forward transversal filter followed by a 177-tap decision feedback section. The long decision feedback provides more accurate ghost canceling to reduce noise enhancement than that found in long feed-forward equalizers. The equalizer operates at

FIGURE 18.14
VSB equalizer system.



10.76-MHz symbol rate (T-sample equalizer). Symbol rate sampling is made possible because the symbol clock has been accurately phased by the clock recovery circuit *before* the equalizer. To aid convergence, the equalizer also includes an extra adder, which is used to add or subtract a dc value to compensate for dc errors that can be caused by circuit offset nonlinearities or shifts in the pilot due to ghosts.

18.8.8 Phase Tracking Loop

The phase tracking loop is an additional decision feedback loop that further tracks out phase noise that has not been removed by the IF PLL operating on the pilot signal. Thus the phase noise is tracked out by not just one loop, but two series loops. Because the system is already frequency locked to the pilot by the IF PLL (independent of the data), the phase tracking loop bandwidth is maximized for phase tracking by using a first-order loop. Higher-order loops, which are needed for frequency tracking, do not perform phase tracking as well as first-order loops. Therefore, they are not used in the VSB systems.

A block diagram for the phase tracking loop is given in Figure 18.15. The output of the real equalizer operating on the I signal is first gain controlled by a multiplier and then fed into a filter that re-creates an approximation of the Q signal. This is possible because of the VSB transmission method, where the I and Q components are related by a filter function called a *Hilbert transform*.

These I and Q signals are then fed into a derotator (complex multiplier), which is used to remove the phase noise. The amount of derotation is controlled by the decision feedback of the data taken from the output of the derotator. Since the phase tracker is operating on the 10.76 MHz symbol/s data, the bandwidth of the phase tracking loop is fairly large, approximately 60 kHz. The gain multiplier is also controlled by the decision feedback.

18.8.9 Trellis Decoder

To help protect the trellis decoder against short burst interference, such as impulse noise or NTSC co-channel interference, 12-symbol-code interleaving is employed in the transmitter. As shown in Figure 18.16, the receiver uses 12 trellis decoders

FIGURE 18.15
Phase tracking loop.

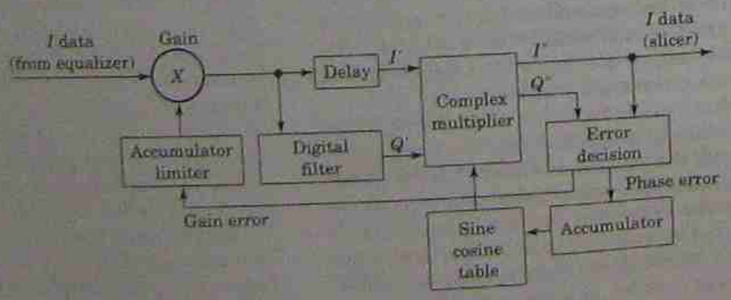
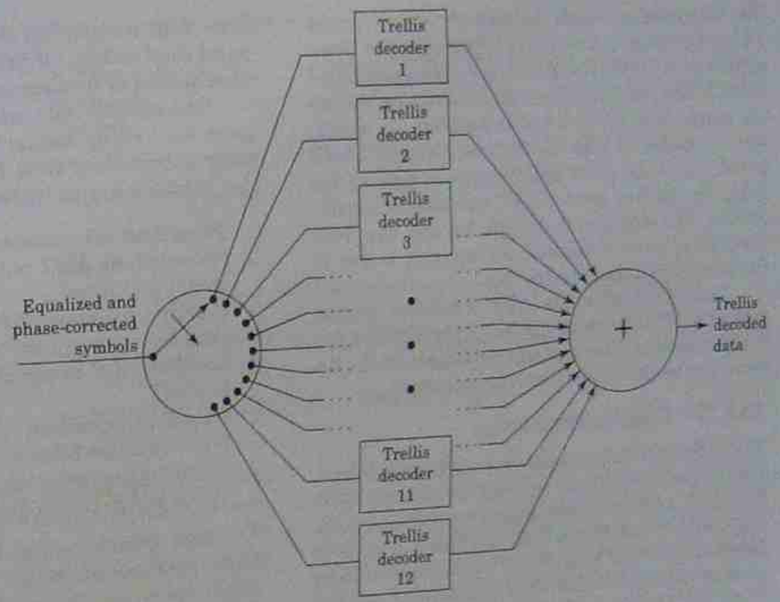


FIGURE 18.16
Trellis code deinterleaver.

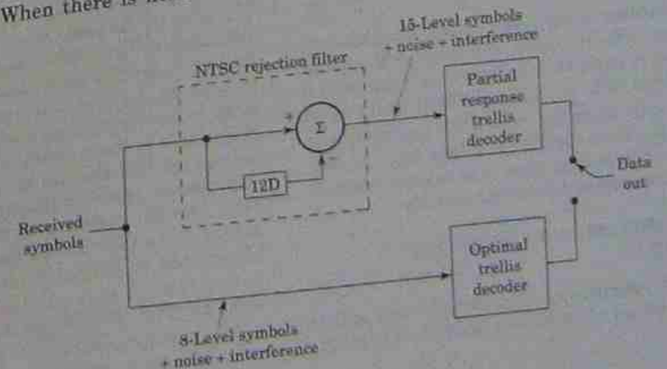


in parallel, where each trellis decoder sees every twelfth symbol. This code interleaver has all the same noise benefits of a 12-symbol interleaver, but also minimizes the resulting code expansion (and hardware) when the NTSC rejection comb filter is active.

The trellis decoder performs the task of slicing and convolutional decoding. It has two modes, one when the NTSC rejection filter is used to minimize co-channel and the other when it is not used. This is illustrated in Figure 18.17. The insertion of the NTSC rejection filter is determined automatically (before the equalizer), with this information passed to the trellis decoder. When there is little or no NTSC co-channel interference, the NTSC rejection filter is not used, and an optimal trellis decoder is used to decode the four-state trellis encoded data.

In the presence of significant NTSC co-channel interference, when the NTSC rejection filter (12-symbol forward subtractive comb) is employed, a trellis decoder optimized for this partial response channel is used. This optimal code requires eight states. This is necessary since the NTSC rejection filter, which has memory, represents another state machine seen at the input of the trellis decoder. To minimize the expansion of trellis states, two measures are taken: (1) special design of the trellis code and (2) 12-to-1 interleaving of the trellis encoding.

FIGURE 18.17
Trellis decoding with and without NTSC rejection filter.



The interleaving, which corresponds exactly to the 12-symbol delay in use in the NTSC rejection filter, causes each trellis decoder to see only one symbol delay NTSC rejection filter. By minimizing the delay stages seen by each trellis decoder, the expansion of states is also minimized. Only a 3.5-dB penalty in white noise performance is paid as the price for having good NTSC co-channel performance. The additional 0.5 dB beyond the 3-dB comb filter noise threshold degradation is due to the 12-symbol differential coding.

Note that after the ATV transition period, when the NTSC is no longer being transmitted, the NTSC rejection filter and the eight-state trellis decoder can be eliminated from the receivers.

18.8.10 Data Deinterleaving

The deinterleaver performs the exact inverse function of the transmitter interleaver. Its one-third data field depth and intersegment dispersion properties allow noise bursts lasting about 170 μs to be handled. Even strong NTSC co-channel signals passing through the NTSC rejection filter and creating short bursts due to the NTSC vertical edges, are reliably handled due to the interleaving and R–S coding process. Intrasegment interleaving is also performed, which resembles the trellis data from the twelve trellis decoders in its original form.

18.8.11 Reed–Solomon Decoders

The trellis decoder byte data are sent to the (208, 188) t = 10 R–S decoder, where it uses the 20 parity bytes to perform the byte-error correction by the R–S decoder. Any burst errors created by impulse noise, NTSC co-channel interference, or trellis decoding errors are greatly reduced by the combination of the interleaving and R–S error correction.

18.8.12 Data Derandomizing

The derandomizer accepts the error-corrected data bytes from the R–S decoder and applies the same pseudorandom segment randomizing code to the data. The PRS code is generated identically as in the transmitter, using the same PRS generator and feedback taps. Since the PRS is locked into the reliably recovered data field sync, it is exactly synchronized with the data and performs reliably.

18.8.13 Receiver Loop Acquisition Sequencing

The receiver incorporates a *universal reset*, which initiates a number of *confidence counters* and *confidence flags* involved in the lock-up process. A universal reset occurs, for example, when tuning to another station or turning on the receiver.

The various loops within the VSB receiver acquire the lock-up sequentially, with earlier loops being independent from later loops. The order of loop acquisition is as follows:

- Tuner first LO synchronizer acquisition
- Noncoherent AGC reduces unlocked signal to within A/D range
- Carrier acquisition (F-PLL)
- Data segment sync and clock acquisition
- Coherent AGC of signal (IF and RF gains properly set)
- Data field acquisition
- NTSC rejection filter insertion decision made
- Equalizer completes tap adjustment algorithm
- Trellis and R–S data decoding begins

Most of the loops mentioned above have confidence counters associated with them to ensure proper operation. However, the buildup and letdown of confidence is not designed to be equal. The confidence counters build up confidence rapidly for quick acquisition times, but lose confidence slowly to maintain operation in noisy environments. The VSB receiver will work in S/N conditions of 0 dB or less as well as in severe interference conditions.

18.9 HIGH-SPEED CABLE MODE CONDITIONS

The high-data-rate cable mode trades off transmission robustness (28.3-dB S/N threshold) for system data rate (43 Mbits/s). Most parts of the cable mode VSB system are identical or similar to the terrestrial system. A pilot, data segment sync, and data field sync are all used to provide robust operation. The pilot in the cable mode also adds 0.3 dB to the data power. The symbol, segment, and field signals and rates are the same, allowing either receiver to lock up on the other's transmitted signal. Also, the data frame definitions are identical. The primary difference is the number of transmitted levels (8 versus 16) and the use of trellis coding and NTSC interference rejection filtering in the terrestrial system. The RF spectrum of the cable modem transmitter looks identical to the terrestrial system, as illustrated in Figure 18.18. The peak to average power ratio is very similar between the two VSB systems. The 16-VSB has a slightly higher peak to average power ratio due to its 16-level random code. The error probability of 16-VSB is about 28.3

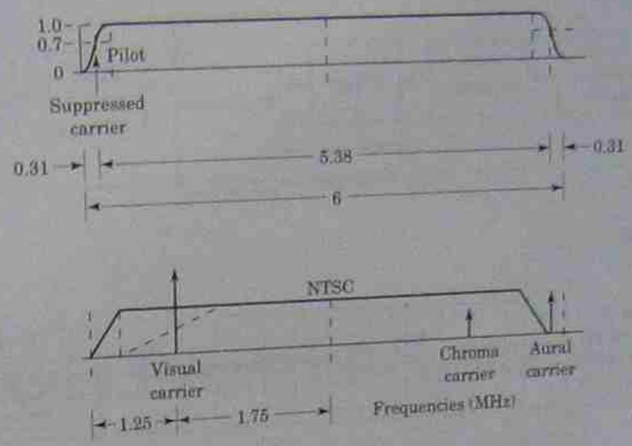


FIGURE 18.18
Sixteen-VSB and NTSC channel occupancy.

dB (3×10^{-6} BER), with forward error correction provided by the Reed–Solomon decoder. Figure 18.19 shows a typical data segment, where the number of data levels is less than 16 due to the double data rate.

Figure 18.20 shows the block diagram of the transmitter. It is identical to the terrestrial VSB system except that the trellis coding is replaced with a mapper, which converts data to multilevel symbols. This conversion is performed by the trellis coding in the terrestrial VSB system. The receiver, shown in Figure 18.21, is identical to the VSB terrestrial receiver except that the trellis decoder is replaced with a slicer, which translates the multilevel symbols into data. Also note that no NTSC interference rejection filter is required in the cable mode, since strong co-channel signals are not present on cable. The lack of trellis coding and NTSC co-channel interference rejection results in a cost savings in the cable modem.

Factors contributing to low-cost receivers are the following:

- Simple carrier recovery (F-PLL) using small pilot
- Standard-technology IF SAW filters
- High immunity to phase noise (phase tracker) for inexpensive tuners

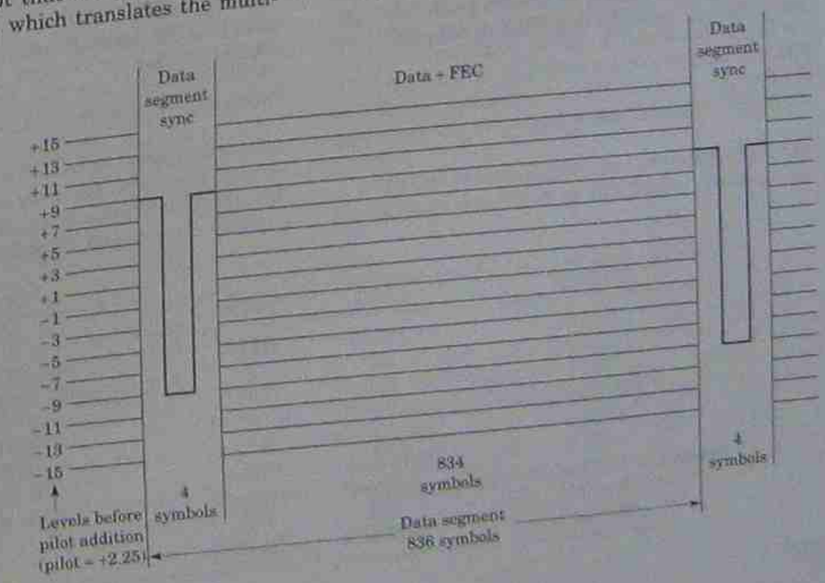


FIGURE 18.19
Sixteen-VSB data segment for high-speed data mode.

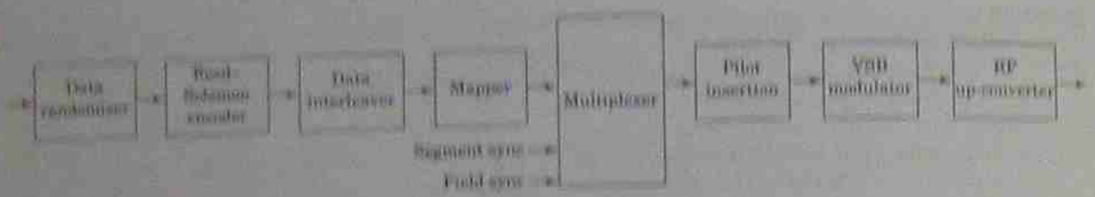


FIGURE 18.20
Sixteen-VSB transmitter.

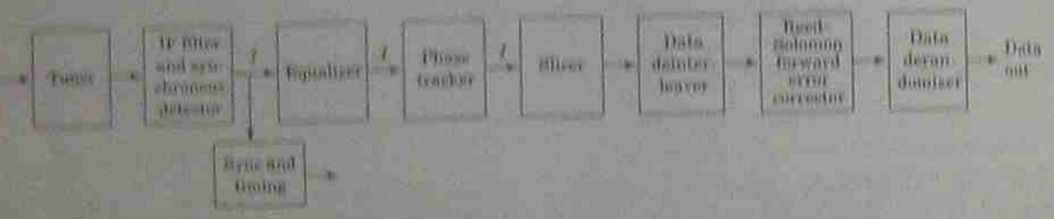


FIGURE 18.21
Sixteen-VSB receiver.

- Symbol spaced sampling for all data-processing circuits
- Single A/D converter (*I* channel only)
- Simple clock recovery using data segment syncs
- Real time sampled adaptive equalizer operating at 10.76 MHz

Keep in mind that this system is not yet a reality and that some aspects of this outline could change slightly before it becomes a published standard. Second, only the engineering personnel who work on HDTV prototypes have ever seen a working model. Therefore, a large number of questions cannot be answered at this time. Also, the NTSC system will be around for several decades yet and should not be abandoned too readily. The intent of this chapter is to give you insight into future systems; to be forewarned is to be forearmed.

Although 16-level cable system products are primarily digital, there is no mention at this time as to how the personal computer industry will handle the changeover.

A World Television Systems

In the late 1930s, the idea of broadcast television was born. The electronic industry realized that a common broadcasting system was necessary that followed standard guidelines. Many companies in the industry pooled their engineering personnel to form the National Television Systems Committee (NTSC) to work out the specifications for compatibility. The standards for monochrome television were drafted and accepted by the Federal Communications Commission (FCC).

The outbreak of World War II put a stop to all television research with a full-time focus on radar. Although no television systems were under design, a great deal of technical skill was developed during this phase. After the war, these skills were applied to the development of television.

About 1953, the NTSC added compatible color standards to the other television broadcast specifications as two-quadrature multiplexed DSSC-AM signals on a 3.579545-MHz suppressed carrier.

About 31 countries have adopted the NTSC standards for broadcast, called the North American network. See Table A-1 for some of these data.

The phase alternate line (PAL) system was developed in Europe in an attempt to improve on the NTSC system, which had some minor drawbacks. The PAL system is similar to the NTSC system but changes the color burst phase by ±45° with each horizontal scan line. At the receiver, the reconstructed subcarrier is shifted forward by +45° for one color demodulator, where the R − Y signal will cancel the R − Y signal. In the second demodulator, the subcarrier is phase shifted by −45°, and at the second demodulator, the R − Y signal will cancel the B − Y signal. This says that one horizontal scan line will display the red color difference signal, and the next scan line will display the blue color difference signal.

The sequential color and memory (SECAM) system was developed in the 1960s, transmitting

TABLE A-1

	NTSC	PAL	SECAM
ac line frequency	60 Hz	50 Hz	50 Hz
Interlaced frames/second	30	25	25
Lines/frame	525	625	625
Scan frequency	15,750 Hz	15,625 Hz	15,625 Hz
Video BW	4.2 MHz	5 to 6 MHz	6 MHz
Channel BW	6 MHz	7 to 8 MHz	8 MHz
Picture phase	Negative	Negative	Negative (positive in France)
Sound	FM	FM	FM (AM in France)
Color	3.58 MHz	4.43 MHz	4.43 MHz

the quadrature-modulated DSSC-AM color signal on a 4.43-MHz suppressed subcarrier with the color signal shifted by 180° on alternate horizontal scan lines.

The NTSC system is based on the 60-Hz power line frequency, while both the PAL and SECAM systems are based on the European power line frequency of 50 Hz. This small difference has kept the systems from merging into a single world system.

B Voltage Amplifiers versus Power Amplifiers

Comparing the two circuits in Figure B.1, you can see that the voltage-divider-based biasing network R_1 and R_2 is the same for both circuits and places the base voltage at about 2.18 V dc. Assuming a constant 0.6-V dc drop across the base–emitter junction will set the emitter voltage in both cases at about 1.58 V dc.

In Figure B.1a, the emitter current is about (1.58/790) = 2 mA. The same 2 mA of current will flow through the collector resistor and drop about 11.2 V dc across the resistor, placing the collector at about 12.8 V dc. The power dissipated by the collector load is EI = 22.4 mW.

In Figure B.1b, the emitter current is about (1.58/32) = 50 mA. The same 50 mA of current will flow through the collector resistor and drop about 11.2 V dc across the resistor, placing the collector at about 12.8 V dc. The power dissipated by the collector load is EI = 560 mW.

Both circuits have a gain of about 7 (R_c/R_e), and each will produce about a 20-$V_{p\text{-}p}$ output signal.

The key to determining a voltage amplifier from a power amplifier without calculations is to look at the value of the collector load. A large value passes a small current and identifies a voltage amplifier. A small-value load passes higher currents and identifies a power amplifier.

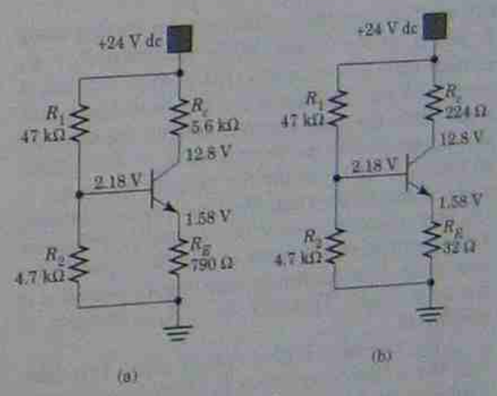


FIGURE B.1
Determining the difference between a voltage amplifier and power amplifier.

C Transistor Biasing and Class of Operation

Circuit C.1a identifies voltage divider biasing using R_1 and R_2 as the divider. When the sum of $R_1 + R_2$ is high (200 kΩ or more), the divider current is small and may be only a few orders of magnitude larger than the base current, making the base circuit barely stable. As the sum of $R_1 + R_2$ is made smaller (50 kΩ), the divider current increases to many times larger than the base current, causing the base current to have much smaller influence. The circuit becomes more stable. Voltage-divider bias is the most commonly used circuit because it is the most stable. Typically, $R_1 + R_2$ is between 10 and 50 kΩ.

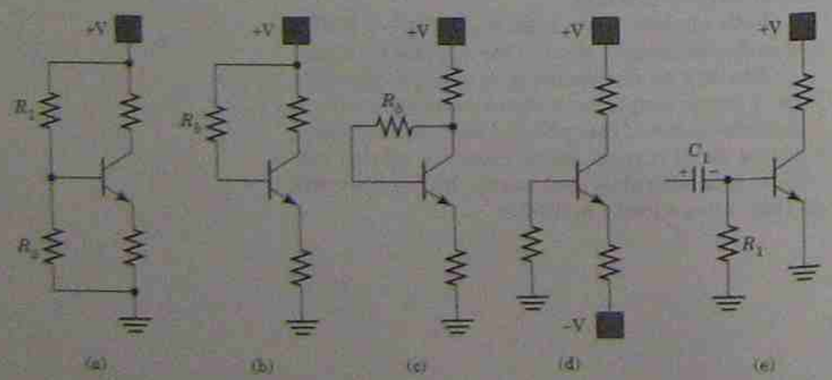
The circuit in Figure C.1b is called *base biasing*. The voltage drop across R_b, due to the base current, sets the base dc voltage. R_b is typically 500 kΩ or larger. Base biasing is very unstable due to its dependence on the level of base current.

Figure C.1c shows *collector feedback bias*; it uses the collector dc voltage as the source of the base bias voltage. Any change in base voltage due to an input signal causes the collector dc voltage to change in the opposite direction and stabilizes the base voltage. Collector feedback bias is better than base bias, but poorer than voltage-divider bias.

Figure C.1d shows *emitter bias*. This circuit is as stable as voltage-divider bias, but requires two power supplies.

There is no dc voltage connected to the base circuit in Figure C.1e, and with no input signal, the base is at 0 V dc. This arrangement is called *signal bias* or *self-bias*, because the base dc voltage depends on the peak value of the input signal. On the positive peak signal, capacitor C_1 will charge to the peak of the input signal through the base–emitter junction with the polarity shown in the figure. On

FIGURE C.1
Biasing arrangements.



the negative peak, the base–emitter diode is reverse biased and the capacitor discharges through the resistor R at a much slower rate than the charge time, maintaining a negative potential on the base. Signal bias is found in all class C amplifiers. The dc base voltage is $-(V_{pk} + 0.6\ V)$.

CLASS OF OPERATION

Using the circuit of Figure B.1 and voltage-divider biasing, the ratio of R_1 to R_2 will help to determine the class of operation. When R_1 is less than 10 times larger than R_2, the amplifier is generally in class A. When R_2 becomes 40 or more times larger than R_1, the amplifier is in one of the intermediate modes between class A and class B, such as AB1. The ratio of R_1 to R_2 must increase to about 100 to 1 before full class B operation is realized. However, class B is most often used in push–pull amplifiers.

Self- or signal bias *always* identifies class C operation.

Index

Absorption trap, 209
Additive and subtractive mixing, 96–97
Advisory Committee on Advanced Television Services (ACATS), 300
AFC. *See* Automatic frequency control
AFT (automatic fine tuning), 161–62
AGC. *See* Automatic gain control
Alignment
  record head, 285
  tuner, 197–98
  video IF amplifier, 218–19
AM (amplitude modulation), 1
Amplifier circuits, video
  described, 71–72
  op-amp, 70
  output amplifiers, 72–73
Amplifiers, cascode
  RF, 192–93
  video, 74–75
Amplifiers, color output, 256–57
Amplifiers, luminance, 164, 170–71
  troubleshooting, 230–32
Amplifiers, output power
  circuits, 72–73
  damper diode for, 44
  horizontal, 42–44
  vertical, 27–29
Amplifiers, RF
  cascode, 192–93
  described, 192–94
  sensitivity of, 194–95
Amplifiers, video
  block diagram, basic, 68–69
  block diagram, monochrome monitor, 112
  cascode, 74–75
  circuits, 70–73
  common-base, 70
  common-collector, 70
  common-emitter, 70
  dc restoration, 75–76, 167–68
  functions of, 112
  gain versus frequency, 70–71
  IF, 160–61, 168, 170, 206, 208–12, 215–19, 258–59
  introduction to, 68
  luminance, 164, 170–71, 230–32
  op-amp circuits, 70
  output power, 27–29, 42–44
  review of basic amplifiers, 69–70
  schematic diagram, monochrome monitor, 113, 115–18
  signal levels, 69
  testing of, 76, 215–16
Amplifiers, video IF
  alignment of, 218–19
  coupling circuits, 209–10
  crystal filters, 210–11
  introduction to, 160–61, 168, 170, 206
  large-scale integrated circuits, 216–18
  SAW (surface acoustical wave) filters, 211–12
  schematic diagram, 206, 208–12
  testing of, 215–16
  traps (notch filters), 208–9
  troubleshooting, 258–59
Amplifiers, voltage versus power, 321
Amplitude control, 51
Amplitude modulation (AM), 1
Anode (plate), 3
Antennas
  described, 147
  driven arrays, 150
  folded dipole, 148–49
  gain and, 149
  half-wave dipole, 148
  heights for, 153–54
  Marconi, 151
  parabolic reflectors (dish antennas), 151–52
  parasitic arrays, 149–50
  reciprocity theorem, 147
  stacked, 150–51
  wavelength, 147–48
  wave propagation and, 152–53

Aquadag, 6
Arrays
  driven, 150
  parasitic, 149–50
Aspect ratio, 2
Atmosphere layers, 152–53
Automatic fine tuning (AFT), 161–62
Automatic frequency control (AFC)
  circuit operation, 38–40
  circuits, described, 38
  described, 37–38
Automatic gain control (AGC)
  chroma (color killer threshold circuit), 232, 255
  coherent and noncoherent, 311
  forward, 214
  HDTV, 311
  introduction to, 163–64
  keyed (gated), 213–15
  reverse, 214
  troubleshooting, 258–59
Azimuth positioning, 285

Back back porch, 57
Back porch, 55
Balun transformers, 178, 180
Bandwidth
  FM, 139
  gain-bandwidth product, 70–71
Barkhausen oscillations, 37
Bar pattern, color. *See* Color bar pattern
Base biasing, 322
Bias/biasing
  base, 322
  collector feedback, 322
  emitter, 322
  signal (self-), 322–23
  voltage-divider, 322
Bias controls, 9
Bias voltages, 284
Black and white video signal, 64
Blacker than black, 54
Blanking interval, 29
Blanking pulses
  horizontal, 54
  vertical, 57
Block diagram
  amplifier, 68–69
  color monitor, 118–23
  horizontal deflection, complete, high-voltage, 34–36
  horizontal deflection, partial, 34
  monochrome monitor, 111–13
  receiver, television, 156, 158–60
  UHF tuner, 184–86
  VCR, 290, 292, 294–97
  vertical deflection, 25–26
Blue beam, 7
Blue bias control, 9
Boosted $B+$ (bootstrap) voltage, 37
Breezeway, 57
Bridge T circuit, 209
Brightness
  master, 9
  troubleshooting, 229
Brightness range control, 223
Brightness signal, 64
Broadcast mode, HDTV
  receiver, 308–16
  transmitter, 304–8
Burst, color, 56–57
Buzz, sync (intercarrier), 171–72

Cable band frequencies, 186
Cable measurements, physical, 145–46
Cable mode conditions, high-speed, 316–18
Cameras, color
  chrominance signal, 105–6
  color area size, 103
  color difference signals, 100, 102
  described, 98
  dichroic mirrors and camera tubes, 98–99
  functions, summary of, 107–8
  I and Q signals, 102–3
  luminance signal, 99–100
  quadrature balanced modulation, 103–5
Canceling systems, noise, 87
Carrier frequency offset, RF, 307–8
Carrier modulation, RF, 135–36
Cascode amplifiers. *See* Amplifiers, cascode
Cassette loading, 288–90
Cathode, 3
Cathode ray tube (CRT) principles
  aspect ratio, 2
  bias controls, 9
  color, described, 7–9
  color purity, described, 9
  electron gun assemblies, 10
  frame rate (frames per second), 2, 15
  introduction to, 1
  numbering systems for, 10–11
  as pentode, 5
  picture size, 2–3
  safe handling of CRTs, 222
  structure of CRTs, 6–7
  television system, 1–2
  vacuum tube operation, 3–9
Cathode ray tube troubleshooting
  described, 247–49
  dynamic convergence, 249, 250
  gray scale adjustments, 250
  purity adjustments, 249–50
CCDs (charged-coupled devices), 275–77
Channel equalizer, 313–14
Channel filtering, 309–10
Channels, troubleshooting all, 227–28
Characteristic impedance, 145
Charged-coupled devices (CCDs), 275–77
Chassis ground, 221
Chassis layout, television
  color section, 170
  described, 168
  high-voltage sections, 170
  horizontal sections, 170
  low-voltage section, 170
  sound section, 170
  synchronization section, 171
  tuner, 168

Chassis layout, television *continued*
vertical section, 170
video IF amplifiers, 168, 170
Chroma automatic gain control (color killer threshold circuit), 232, 255
Chromaticity, 95–96
Chrominance signal, 105–6
CIE (International Commission on Illumination) primary colors, 96
Class of operation, 323
Closed captioning (CC or Q)
described, 61
framing code for, 61
reception of, 62
Coding. *See* Decoders/decoding; Encoders/encoding
Coil, peaking, 72–73
Collector feedback bias, 322
Color(s)
additive and subtractive mixing, 96–97
area size, 103
blacker than black, 54
burst, 56–57
camera, 98–100, 102–8
colorplex frequency spectrum, 106–7
compatibility, 98
CRT, principles of, 7–9
demodulation of, 164–67
difference signals, 100, 102
dynamic convergence, 249, 250
gray scale adjustments, 250
introduction to, 94
light, 94–96
primary, 96–97
purity of, 9, 249–50
R-G-B values, standard, 97–98
saturated, 96
subcarrier, 56–57
troubleshooting, 226, 232–33, 235, 249–50, 253–57
Color bar pattern, 61
NTSC color bar test pattern, 98–99, 102, 106, 123, 126, 233, 255
Color cameras. *See* Cameras, color
Color filters, 278–79
Color killer threshold circuit (chroma automatic gain control), 232, 255
Color lock, 227
Color monitors. *See under* Monitors, video
Color output amplifiers, 256–57
Colorplex composite video signal, 106
Colorplex frequency spectrum, 106–7
Color section, television receiver, 170
Common-base amplifiers, 70
Common-collector amplifiers, 70
Common-emitter amplifiers, 70
Compatibility, color, 98
Complement, 96–97
Composite video signal
described, 55–56
horizontal pulse timing, 56–57
negative and positive picture phase, 56
Confetti, 166, 227, 232
Confidence counters, 316
Confidence flags, 316
Contrast, 1
Control grid, 4
Convergence
correction of, 49, 51
described, 22
dynamic, 249, 250
static, 249, 250
Countdown circuits, digital. *See* Digital countdown circuits
Coupler/coupling
charged-coupled devices (CCDs), 275–77
critical, 184
direct, 209–10
mutual, 183–84
optical, 246
over- 184
resistance-capacitance (RC), 209
transformer, 210
under-, 184
video IF amplifier coupling circuits, 209–10
Cross-hatch pattern, 51
Critical coupling, 184
CRTs. *See* Cathode ray tube principles; Cathode ray tube troubleshooting
Crystal filters, 210–11
Current
dark, 274
dc restoration, 75–76, 167–68
leakage current hot tests, 222
regulated dc supplies, 118

Damper diode, 44
Damper section, 36–37
Dark current, 274
Data deinterleaving, 316
Data derandomizing, 316
Data field synchronization, 311
Data randomizer, 304
dc (direct current)
regulated supplies of, 118
restoration of, 75–76, 167–68
Decoders/decoding. *See also* Encoders/encoding
Reed–Solomon (R–S), 316
trellis, 314–16
Deflection systems. *See* Horizontal deflection systems; Vertical deflection systems
Deflection yoke
defined, 18
mechanical functions of, 20–21
waveforms of, 19–20
Deinterleaving, data, 316
Delta gun, 10
Demodulation, color, 164–67
Derandomizing, data, 316
Detectors, video
introduction to, 162–63, 212
synchronous detection, 212–13
testing of, 215–16
troubleshooting, 258–59
Deviation, frequency, 137–38
Deviation ratio, 139
Deviation sensitivity, 138
Dichroic mirrors, camera tubes and, 98–99
Differentiator output signals, 82–83

Digital countdown circuits
described, 83–84
horizontal section, 84–85
other, 85–86
troubleshooting, 90–91
vertical section, 85
Digital encoding, 200–203
Diode
damper, 44
varactor diode tuning, 186–88
Diode band switching, 186–87
Dipole antennas
folded, 148–49
half-wave, 148
Direct coupling, 209–10
Direct current. *See* dc
Direct FM, 139–40
Discontinuities, schematic symbols and, 126
Dish antennas (parabolic reflectors), 151–52
Driven arrays, 150
Dynamic convergence, 249, 250

Electromagnetic deflection
advantages and disadvantages of, 19
described, 18–19
Electron-coupled Hartley oscillator, 41–42
Electron gun
assemblies, 10
defined, 5
Electronic Communications: Modulation and Transmission (Schoenbeck), 138, 184
Electronic tuners
cable band frequencies and, 186
described, 186
diode band switching and, 186–87
low-band operation, 189–90
schematic diagrams, 188–92
superband operation, 190–91
testing of, 196–97
UHF-band operation, 191–92
varactor diode tuning, 186–88
Electrostatic deflection
advantages of, 17–18
described, 16–17
Elevation positioning, 285
Emission
secondary, 4
thermionic, 3
Emitter bias, 322
Encoders/encoding. *See also* Decoders/decoding
digital, 200–203
Reed–Solomon (R–S), 304–5
trellis coding modulation, 305
Equalizer, channel, 313–14
Equalizing pulses, 57–58
Erase head, flying, 296

FCC (Federal Communications Commission) regulations
closed captioning and, 62
color system and, 98
equalizing pulses and, 58
HDTV and, 301

Field
data field synchronization, 311
one, 14
second, 15
Filters/filtering
channel, 309–10
color, 278–79
crystal, 210–11
interference rejection, 311–13
notch (traps), 208–9
preequalizer, 307
SAW (surface acoustical wave), 211–12
Flyback action, 35
Flying erase head, 296
FM (frequency modulation), 1
bandwidth of, 139
described, 137
deviation ratio, 139
deviation sensitivity, 138
direct, 139–40
frequency deviation, 137–38
indirect (phase modulation), 140–41
modulation index, 138–39
percent of modulation, 138
Focus voltage, 37
Folded dipole antennas, 148–49
Foldover, vertical, 29
Forbidden zone, 133
Forward automatic gain control, 214
Frame, 15
Frame rate (frames per second), 2, 15
Frequency
gain versus, 70–71
gap size versus, 282, 284
Frequency control, automatic. *See* Automatic frequency control
Frequency deviation, 137–38
Frequency modulation. *See* FM
Frequency ranges
cable band, 186
described, 133
forbidden zone, 133
hyperband, 186
intermediate carrier, 156
low-band, 189–90
midband, 186
superband, 186, 190–91
UHF band, 135, 191–92
VHF band, 133, 135
Frequency spectrum, colorplex, 106–7
Frequency synthesis, 83
Frequency troubleshooting, horizontal, 47
Front porch, 55
Full wrap, 286

Gain
antenna, 149
frequency versus, 70–71
Gain-bandwidth product, 70–71
Gain control, 28
Gap, spark, 116
Gap size, frequency versus, 282, 284
Gated (keyed) automatic gain control, 213–15

Gates, noise, 87–88
Getter, 4
Ghost, 235
Good raster condition, 223, 225–26
Gray scale adjustments, 250
Green beam, 7
Green bias control, 9
Grid
  control, 4
  screen, 4
  suppressor, 4
Ground
  chassis, 221
  hot, 240–41
  phantom, 20
Ground waves, 153

Half+ wrap, 286
Half-wave dipole antennas, 148
Hammerhead pattern, 90
Hartley oscillator, electron-coupled, 41–42
HDTV. *See* High-definition television
Head switching, VCR, 294–96
Helical scanning
  cassette loading, 288–90
  described, 285–86
  tape track, 286–88
High-definition television (HDTV)
  automatic gain control, coherent and noncoherent, 311
  carrier recovery, VSB, 309–10
  channel equalizer, 313–14
  channel filtering, 309–10
  circuits that should not change, 301–2
  data deinterleaving, 316
  data derandomizing, 316
  data field synchronization, 311
  data randomizer, 304
  effects on general public, 301
  effects on service industry, 301–2
  expected improvements, 300
  high-speed cable mode conditions, 316–18
  interference rejection filter, 311–13
  interleaver, 305
  introduction to, 300
  modulation, VSB, 307
  new signal circuits, 302–4
  NTSC system and, 300–318
  phase tracking loop, 314
  pilot insertion, 306–7
  preequalizer filter, 307
  receiver broadcast mode, 308–16
  receiver loop acquisition sequencing, 316
  Reed–Solomon (R–S) decoders, 316
  Reed–Solomon (R–S) encoder, 304–5
  RF carrier frequency offset, 307–8
  segment synchronization, 310
  symbol clock recovery, 310
  synchronization information, 305–6
  system information, 302–4
  system overview, 302
  timetable, 300–301
  transmitter broadcast mode, 304–8
  trellis coding modulation, 305
  trellis decoder, 314–16
  tuner, 308–9
  upconverter, 307–8
  VSB system, 302–5, 307–8, 316–17
High-speed cable mode conditions, 316–18
High-voltage block diagram, 34–36
High-voltage measurements, 222
High-voltage section, horizontal deflection
  described, 44
  troubleshooting, 239–44
  voltage multipliers, 44–45
  x-radiation, 45–46
High-voltage sections, television receiver, 170
Hilbert transform, 314
Hold control, vertical, 25
Hook, 86
Horizontal blanking pulses, 54
Horizontal deflection systems
  automatic frequency control (AFC), 37–40
  block diagram, complete, high-voltage, 34–36
  block diagram, partial, 34
  boosted B+ (bootstrap) voltage, 37
  convergence, correction of, 49, 51
  damper section, 36–37
  focus voltage, 37
  high-voltage section, 44–46, 239–44
  introduction to, 34
  monitor, 113, 117–18
  multivibrator, 40–42
  oscillators, 40–42
  output power amplifiers, 42–44
  pincushioning, correction of, 48–49
  troubleshooting, 46–48, 239–44
  x-radiation, 45–46
Horizontal pulse timing, 56–57
Horizontal scanning, 14–15
Horizontal sections, television receiver, 170
Horizontal synchronizing pulse, 55
Horizontal timing, 15–16
Hot ground, 240–41
Hue, 96
Hue control, 166
Hyperband frequencies, 186

IEEE (Institute of Electronic and Electrical Engineers), 59
IF amplifiers, video. *See* Amplifiers, video IF
Image orthocon, 274–75
Impedance, characteristic, 145
Infrared LEDs, 200
In-line gun assembly, 10
Institute of Electronic and Electrical Engineers (IEEE), 59
Institute of Radio Engineers (IRE), 59
In sync condition, 82
Integrator output signals, vertical, 81–82
Interference rejection filter, 311–13
Interlace scanning, 15
Interleaver, 305
Intermediate-frequency carrier, 156
International Commission on Illumination (CIE) primary colors, 96
Inverse square law, 45

Inverters, noise, 88–89
Ion, 7
Ion trap, 7
IRE (Institute of Radio Engineers), 59
IRE units, 59–60
I signals
Isolation transformers, 221–22

Johnson (thermal or white) noise, 87, 195

Keyed (gated) automatic gain control, 213–15
Keystone raster condition, 46

Large-scale integrated circuits
  troubleshooting, 262–63, 266, 268–70
  video IF amplifier, 216–18
LCDs (liquid-crystal displays), 273
Leakage current hot tests, 222
LEDs. *See* Light-emitting diodes
Light
  chromaticity, 95–96
  described, 94–95
  white, 1
Light-emitting diodes (LEDs)
  described, 272–73
  infrared, 200
Light exchangers
  color filters, 278–79
  introduction to, 271
  light-emitting diodes (LEDs), 200, 272–73
  liquid-crystal displays (LCDs), 273
  pickup devices, 273–77
  projection systems, 271–72
Linearity control, vertical, 28
Line of video (analog), one, 54
Line pairing, 59
Lines of resolution, 64–65
Liquid-crystal displays (LCDs), 273
Loop acquisition sequencing, receiver, 316
Low-band frequencies, 189–90
Low-voltage power supplies, 113, 118
Low-voltage section, television receiver, 170
  troubleshooting, 244–47
Lumen, 64
Luminance amplifiers. *See* Amplifiers, luminance
Luminance signal, 64, 99–100
  troubleshooting, 252–53

Magenta, 96
Marconi, Guglielmo, 151
Marconi antennas, 151
Master brightness, 9
Maxwell, James C., 95, 96, 98
Mechanical tuners
  described, 177
  testing of, 195–96
  turret, 181, 183
  wafer switch, 177–78, 180–81
Mesophase, 273
Midband frequencies, 186
Miller effect, 72
Mirrors, camera tubes and dichroic, 98–99
Modulation
  amplitude (AM), 1
  percent of, 138
  picture phase, modulated, 136–37
  quadrature balanced, 103–5
  RF carrier, 135–36
  trellis coding, 305
  VSB, 307
  Z-axis, 62–63
Modulation, frequency. *See* FM
Modulation index, 138–39
Monitors, video
  color block diagram, 118–23
  color schematic diagram, 123, 126
  color video signal, 120–22
  introduction to, 111
  low-voltage power supplies, 113, 118
  monochrome block diagram, 111–13
  monochrome schematic diagram, 113, 115–18
  monochrome video signal, 119–20
  troubleshooting, 129–30
Monochrome monitors. *See under* Monitors, video
Monochrome TV standards, NTSC, 319
Monochrome video signal, 64
MOSFET, 193
Multiburst signal, 60
Multichannel television sound (MTS) (stereo), 141–42
Multipliers, voltage, 44–45
Multivibrator, horizontal deflection, 40–42
Mutual coupling, 183–84

Narrow raster condition, 47
National Television Systems Committee standards. *See* NTSC standards
Negative picture phase, 56
Negative resistance, 4
Neutralization, 184
Newton, Sir Isaac, 94–96
Noise, characteristics of
  canceling systems, 87
  described, 86–87
  gates, 87–88
  inverters, 88–89
Noise, thermal (white or Johnson), 87, 195
Nonstandard systems, scanning and, 22
No raster, normal sound condition, 223
No raster, no sound, no ON condition, 223
No raster condition, 47–48, 223
Notch filters (traps), 208–9
NTSC (National Television Systems Committee) standards
  color bar test pattern, 98–99, 102, 106, 123, 126, 233, 255
  details of, 319–20
  HDTV and, 300–318
  horizontal timing, 16
  monochrome TV, 319
  RF transmission, 133, 135, 136
  vertical timing, 16
  video signal, 56, 59–60, 97, 98, 105, 319–20
Numbering systems, CRT, 10–11

Omega wrap, 286
One field, 14
One line of video (analog), 54
Op-amp circuits, 70
Operation, class of, 323
Optical coupler, 246
Orthocon, image, 274–75
Oscillations
  Barkhausen, 37
  parasitic, 184
Oscillators
  Hartley, electron-coupled, 41–42
  horizontal, 40–42
  vertical, 26–27
  voltage-controlled (VCOs), 84–85, 91
Out of sync condition, 82
Output amplifiers, 256–57
Output power amplifiers. *See* Amplifiers, output power
Output signals, synchronization
  described, 81
  differentiator, 82–83
  vertical integrator, 81–82
Overcoupling, 184
Overtone crystals, 211

Pairing, line, 59
PAL (phase alternate line) system, 319–20
Parabolic reflectors (dish antennas), 151–52
Parabolic waveform, 51
Parallel resonant circuit, 209
Parasitic arrays, 149–50
Parasitic oscillations, 184
Partial response, 312
Peaking coil, 72–73
Pentode
  CRT as, 5
  defined, 4
Percent of modulation, 138
Phantom ground, 20
Phase alternate line (PAL) system, 319–20
Phase control, 84
Phase modulation (indirect FM), 140–41
Phase splitter, 80
Phase tracking loop, 314
Phosphorescent, 6
PHOTOFACTS® service folder, 236
Photon, 6
Pickup devices
  charged-coupled devices (CCDs), 275–77
  described, 273–74
  image orthocon, 274–75
  vidicon family, 275
Picture phase
  modulated, 136–37
  negative, 56
  positive, 56
Picture size, 2–3
Picture tube. *See* Cathode ray tube principles; Cathode ray tube troubleshooting
Pilot insertion, 306–7
Pincushioning
  correction of, 48–49
  described, 21–22
Pixel, 272
Plate (anode), 3
Playback circuits, VCR, 296–97
Porch
  back, 55
  back back, 57
  front, 55
Positive picture phase, 56
Power amplifiers, voltage amplifiers versus, 321
Power supplies
  low-voltage, 113, 118
  regulated dc, 118
  switching, 246
Precision static toroid (PST), 22
Preequalizer filter, 307
Primary colors, 96–97
Processor, 217
Projection systems, 271–72
Pulse timing, horizontal, 56–57
Purity, color, 9
  adjustments, 249–50

Q signals, 102–3
Quadrature balanced modulation, 103–5
Quality, troubleshooting
  described, 228
  picture synchronization, 89–91, 229–30
  raster brightness, 229
  raster size, 228–29

Radiation, x-, 45–46
Radio frequency transmission. *See* RF transmission
Randomizer, data, 304
Raster
  defined, 16
  scanning and, 16
  size of, 2, 228–29
  standard white, 9
Raster troubleshooting
  brightness, 229
  described, 46
  good raster, 223, 225–26
  keystone raster, 46
  narrow raster, 47
  no raster, 47–48, 223
  no raster, normal sound, 223
  no raster, no sound, no ON, 223
  raster with good picture, good sound, 226
  raster with good picture, no sound, 226
  raster with heavy snow, no picture, no sound, 225–26
  raster with no picture, good sound, 226
  raster with no picture, no sound, no snow, 225
  size, 228–29
Receiver broadcast mode, HDTV, 308–16
Receiver loop acquisition sequencing, HDTV, 316
Receivers, split sound, 171–72
Receivers, television, introduction to
  automatic fine tuning (AFT), 161–62
  automatic gain control (AGC), 163–64
  block diagram, 156, 158–60

  chassis layout, 168, 170–71
  color demodulation, 164–67
  dc restoration, 167–68
  introduction to, 156
  luminance, 164, 170–71
  split sound receivers, 171–72
  video amplifiers, 160–61, 164, 168, 170–71
  video detectors, 162–63
  video IF amplifier, 160–61, 168, 170
Receivers, television, troubleshooting
  cathode ray tubes, 247–50
  comparing similar effects, 236
  introduction to, 221
  outline for, 222–23, 225–28
  quality, 228–33, 235–36
  RF circuits, 235–36, 259–60
  safety, 221–22
  schematic, 236, 238–63, 266, 268–70
  sound circuits, 260–62
Reciprocity theorem, antennas and, 147
Record circuits, VCR, 292, 294
Record heads, VCR, 280–82, 284–85
  alignment of, 285
  bias voltages, 284
  described, 280–82
  gap size versus frequency, 282, 284
  head switching, 294–96
  tape transports, 284
Red beam, 7
Red bias control, 9
Reed–Solomon (R–S) decoders, 316
Reed–Solomon (R–S) encoder, 304–5
Reflectors, parabolic (dish antennas), 151–52
Refracted path, 153
Regulated dc supplies, 118
Remote control
  described, 198–200
  digital encoding, 200–203
  infrared LEDs, 200
Reset, universal, 316
Resistance, negative, 4
Resistance-capacitance (RC) coupling, 209
Resolution, lines of, 64–65
Response, partial response, 312
Restoration, dc, 75–76, 167–68
Retrace, 15–16
Reverse automatic gain control, 214
RF (radio frequency) amplifiers. *See* Amplifiers, RF
RF circuits, troubleshooting, 235–36, 259–60
RF transmission
  carrier frequency offset, 307–8
  carrier modulation, 135–36
  direct FM, 139–40
  FM sound, 137–39
  frequency ranges, 133, 135
  indirect FM (phase modulation), 140–41
  introduction to, 133
  modulated picture phase, 136–37
  multichannel television sound (MTS) (stereo), 141–42
R-G-B and *I* inputs, 122–23
R-G-B values, standard, 97–98
Rings, slip, 296
Rotary transformers, 296

Safety
  basic precautions, 221
  CRTs, handling, 222
  high-voltage measurements, 222
  isolation transformers, 221–22
  leakage current hot tests, 222
SAP (second audio program) channel, 142
Saturated color, 96
SAW (surface acoustical wave) filters, 211–12
Sawtooth waveform, 16, 19–20, 51
Scanning principles
  deflection yoke, mechanical functions of, 20–21
  deflection yoke, waveforms of, 19–20
  electromagnetic deflection, advantages and disadvantages of, 19
  electromagnetic deflection, described, 18–19
  electrostatic deflection, advantages of, 17–18
  electrostatic deflection, described, 16–17
  horizontal, 14–15
  horizontal timing, 15–16
  interlace, 15
  introduction to, 14
  nonstandard systems and, 22
  pincushioning, 21–22
  raster and, 16
  vertical timing, 16
Schematic diagrams
  color monitor, 123, 126
  discontinuities and schematic symbols, 126
  electronic tuner, 188–92
  horizontal, 239–44
  monochrome monitor, 113, 115–18
  vertical, 29, 31, 238–39
  video IF amplifier, 206, 208–12
Schematic troubleshooting
  automatic gain control, 258–59
  cathode ray tubes, 247–50
  color circuit, 253–57
  described, 236, 238
  high-voltage, 239–44
  horizontal deflection, 239–44
  large-scale integrated circuits, 262–63, 266, 268–70
  low-voltage, 244–47
  luminance, 252–53
  RF circuits, 259–60
  sound circuits, 260–62
  synchronization circuits, 250–52
  vertical deflection, 238–39
  video detectors, 258–59
  video IF amplifiers, 258–59
Schmidt projection tube, 271
Schoenbeck, Robert J., 138, 184
Scoping the video wave, 63–64
Screen grid, 4
SECAM (sequential color and memory) system, 319–20
Secondary emission, 4
Second audio program (SAP) channel, 142
Second field, 15
Segment synchronization, HDTV, 310
Self- (signal) bias, 322–23
Sensitivity
  deviation, 138
  of RF amplifiers, 194–95

Separators, synchronization, 83, 112–13, 116–17
Sequential color and memory (SECAM) system, 319–20
Series resonant circuit, 209
Serrations, vertical, 58
Shadow mask, 7–8
Signal(s), video
  chrominance signal, 105–6
  closed caption reception, 62
  color, 120–22
  color difference signals, 100, 102
  colorplex composite, 106
  composite, 55–57
  horizontal blanking pulses, 54
  horizontal synchronizing pulse, 55
  I, 102–3
  IRE units, 59–60
  introduction to, 54
  levels of, for amplifier, 69
  line pairing, 59
  lines of resolution, 64–65
  luminance signal, 64, 99–100, 252–53
  monochrome, 119–20
  NTSC standards, 56, 59–60, 97, 98, 105, 319–20
  one line of video (analog), 54
  Q, 102–3
  scoping the video wave, 63–64
  synchronization output, 81–83
  tracing of, 123, 126
  vertical blanking pulses, 57
  vertical interval test signals (VITS), 60–61
  vertical synchronizing pulse, 57–58
  Z-axis modulation, 62–63
Signal (self-) bias, 322–23
Sine squared, 61
Sky waves, 153
Slip rings, 296
Soft tube, 229
Sound circuits, troubleshooting, 260–62
Sound receivers, split, 171–72
Sound section, television receiver, 170
Space waves, 153
Spark gap, 116
Split sound receivers, 171–72
Splitter, phase, 80
Square-wave waveform, 20
Stacked antennas, 150–51
Staggered tuning, 210
Stairstep pattern, 61
Standing wave ratio, 146–47
Static convergence, 249, 250
Stereo (multichannel television sound, or MTS), 141–42
Subbers, tuner, 177
Subbrightness control, 223
Subcarrier, color, 56–57
Subtractive and additive mixing, 96–97
Superband frequencies, 186, 190–91
Superheterodyne, 156
Suppressor grid, 4
Surface acoustical wave (SAW) filters, 211–12
Sychronization, HDTV
  data field, 311
  general information on, 305–6
  segment, 310
Symbol clock recovery, 310
Synchronization circuits
  digital countdown circuits, 83–86, 90–91
  in sync condition, 82
  introduction to, 80
  introductory circuit, 80
  noise, characteristics of, 86–89
  out of sync condition, 82
  output signals, 81–83
  requirements, 80–81
  separators, 83, 112–13, 116–17
Synchronization circuit troubleshooting
  described, 89, 250–52
  digital countdown circuits, 90–91
  loss of picture, 226
  picture rolls vertically, 89–90, 229–30
  picture tears horizontally, 90
  total loss of synchronization, 90
Synchronization section, television receiver, 171
Synchronizing pulse
  horizontal, 55
  vertical, 57–58
Synchronous detection, 212–13
Synthesis, frequency, 83
System control, VCR, 292

Tape recording, video. *See* Videocassette recorders
Tape track, VCR, 286–88
Tape transports, VCR, 284
Television, high-definition. *See* High-definition television
Television receivers, introduction to. *See* Receivers, television, introduction to
Television receivers, troubleshooting. *See* Receivers, television, troubleshooting
Television system, introduction to, 1–2
Television tuners. *See* Tuners, television
Testing. *See also* Troubleshooting
  of tuners, 195–97
  of video amplifiers, 76, 215–16
  of video detectors, 215–16
  of video IF amplifiers, 215–16
Test pattern, NTSC color bar, 98–99, 102, 106, 123, 126, 233, 255
Tetrode, 4
Thermal (white or Johnson) noise, 87, 195
Thermionic emission, 3
Tilt control, 51
Timing
  horizontal, 15–16
  vertical, 16
Tint control, 166
Trace, 15–16
Tracing, signal, 123, 126
Tracking loop, phase, 314
Tracking sequence, 288
Transformer coupling, 210
Transformers
  balun, 178, 180
  isolation, 221–22
  rotary, 296
Transmission, RF. *See* RF transmission
Transmission lines
  cable measurements, physical, 145–46

  introduction to, 145
  standing wave ratio, 146–47
Transmitter broadcast mode, HDTV, 304–8
Trapezoidal waveform, 20
Traps (notch filters), 208–9
Traps, ion, 7
Trellis coding modulation, 305
Trellis decoder, 314–16
Trinitron assembly, 10
Triode, 4
Troubleshooting. *See also* Testing
  basic equipment for, 236, 238
  cathode ray tubes, 247–50
  color, 226, 232–33, 235, 249–50, 253–57
  high-voltage, 239–44
  horizontal circuits, 46–48, 239–44
  horizontal frequency, 47
  low-voltage, 244–47
  monitors, video, 129–30
  raster, 46–48, 223, 225–26, 228–29
  receiver, television, 221–23, 225–33, 235–36, 238–63, 266, 268–70
  synchronization, 89–91, 226, 229–30, 250–52
  VCRs, 197–99
  vertical circuits, 31, 238–39
Tuners, television
  alignment of, 197–98
  described, 168
  electronic, 186–92, 196–97
  HDTV, 308–9
  introduction to, 177
  mechanical, 177–78, 180–81, 183, 195–96
  mutual coupling and, 183–84
  neutralization and, 184
  testing of, 195–97
  turret, 181, 183
  types of, 177
  UHF, 159–60, 184–86, 191–92
  VHF, 156, 158–59
  wafer switch, 177–78, 180–81
Tuner subbers, 177
Tuning, staggered, 210
Turret tuners, 181, 183

UHF channels, 135
UHF tuners
  block diagram, 184–86
  electronic operation, 191–92
  introduction to, 159–60
Undercoupling, 184
U.S. Department of Health, Education, and Welfare (HEW) radiation-exposure limits, 45
Universal reset, 316
Upconverter, 307–8

Vacuum tube operation, 3–9
Varactor diode tuning, 186–88
VCOs. *See* Voltage-controlled oscillators
VCRs. *See* Videocassette recorders
Vertical blanking pulses, 57
Vertical block diagram, 25–26
Vertical deflection systems
  block diagram, 25–26
  introduction to, 25
  monitor, 113, 117
  oscillators, 26–27
  output power amplifiers, 27–29
  schematic diagrams, 29, 31, 238–39
  troubleshooting, 31, 238–39
Vertical foldover, 29
Vertical hold control, 25
Vertical integrator output signals, 81–82
Vertical interval reference (VIR), 61
Vertical interval test signals (VITS)
  closed captioning, 61–62
  color bar pattern, 61
  described, 60
  multiburst, 60
  sine squared, 61
  stairstep pattern, 61
  vertical interval reference (VIR), 61
Vertical linearity control, 28
Vertical section, television receiver, 170
Vertical serrations, 58
Vertical synchronizing pulse
  described, 57
  equalizing pulses, 57–58
  serrations, 58
Vertical timing, 16
Vestigial sideband transmission (VSB), 107, 135
  carrier recovery, 309–10
  HDTV and, 302–5, 307–8, 316–17
  modulator, 307
VHF band, 133, 135
VHF tuner, 156, 158–59
Video amplifier circuits. *See* Amplifier circuits, video
Video amplifiers. *See* Amplifiers, video
Videocassette recorders (VCRs)
  block diagram, 290, 292, 294–97
  cassette loading, 288–90
  head switching, 294–96
  helical scanning, 285–90
  introduction to, 280
  playback circuits, VCR, 296–97
  record circuits, 292, 294
  record heads, 280–82, 284–85, 294–96
  system control, 292
  tape track, 286–88
  troubleshooting, 297–99
Video detectors. *See* Detectors, video
Video monitors. *See* Monitors, video
Video signals. *See* Signal(s), video
Vidicon family, 275
VIR (vertical interval reference), 61
VITS. *See* Vertical interval test signals
Voltage(s)
  bias, 284
  boosted *B*+ (bootstrap), 37
  focus, 37
Voltage, high
  block diagram, 34–36
  horizontal deflection, 44–46
  television receiver sections, 170
Voltage, low
  power supplies, 113, 118
  television receiver section, 170

Voltage amplifiers, power amplifiers versus, 321
Voltage-controlled oscillators (VCOs)
  described, 84–85
  troubleshooting, 91
Voltage-divider bias, 322
Voltage multipliers, 44–45
Volume control, 28
VSB. *See* Vestigial sideband transmission

Wafer switch tuners, 177–78, 180–81
Waveforms
  deflection yoke, 19–20
  parabolic, 51
  sawtooth, 16, 19–20, 51
  scoping the video wave, 63–64
  square-wave, 20
  trapezoidal, 20
Wavelength, antennas and, 147–48
Wave propagation, antennas and
  atmosphere layers, 152–53
  described, 152
  ground waves, 153
  sky waves, 153
  space waves, 153
White light, 1
White (thermal or Johnson) noise, 87, 195
White raster, standard, 9
World television systems, 319–20
Worldwide Type Designation System (WTDS), 10–11
Wrapping, tape, 286

x-radiation, 45–46

Y-signal, 64

Z-axis modulation, 62–63
Zenith adjustment, 285

No phones
No food
No drink

CHASSIS SCHEMATIC — SIGNAL CIRCUIT

FW3000 SOUND

SOUND PROCESSOR OUTPUT

CHROMA

U3001
CHROMA PROCESSOR

AFT

IF

AGC DELAY

PW3000
KINE SOCKET

PW3000
LUMINANCE

Valuables unattended

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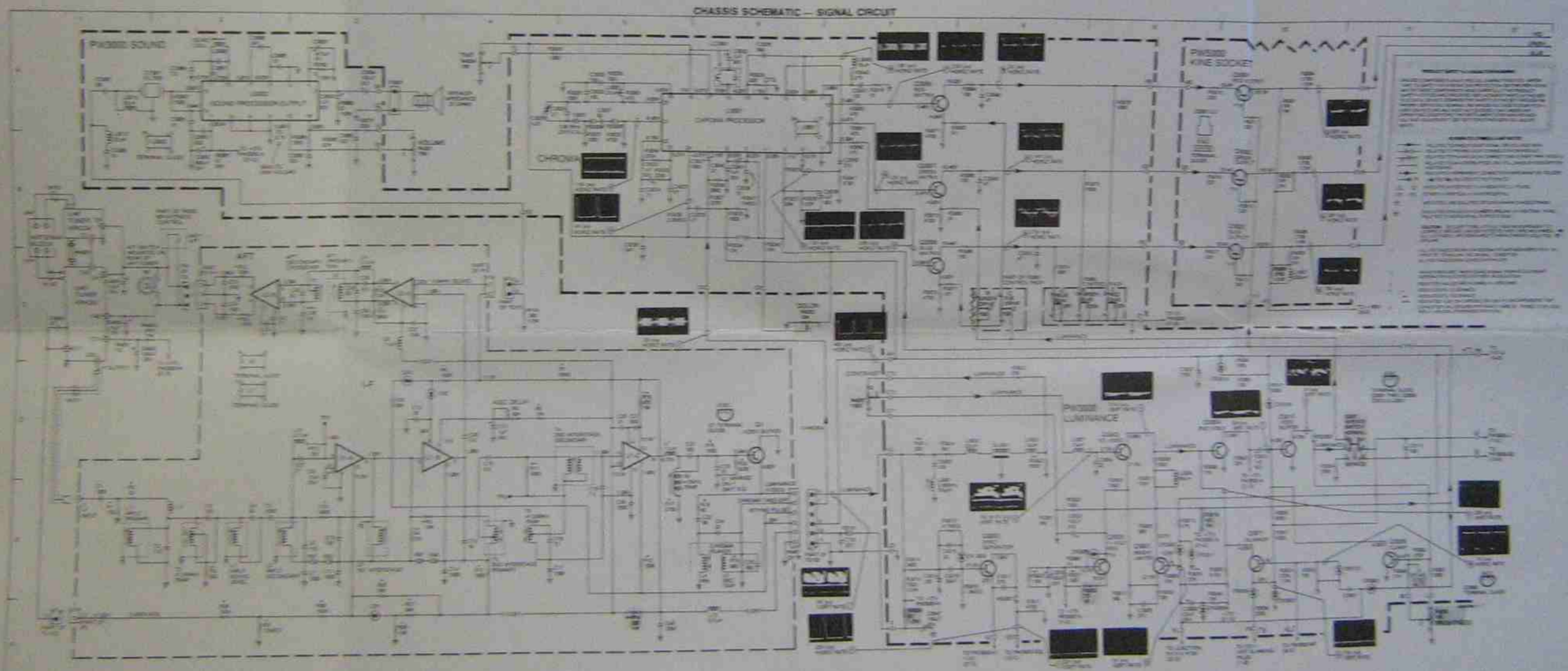

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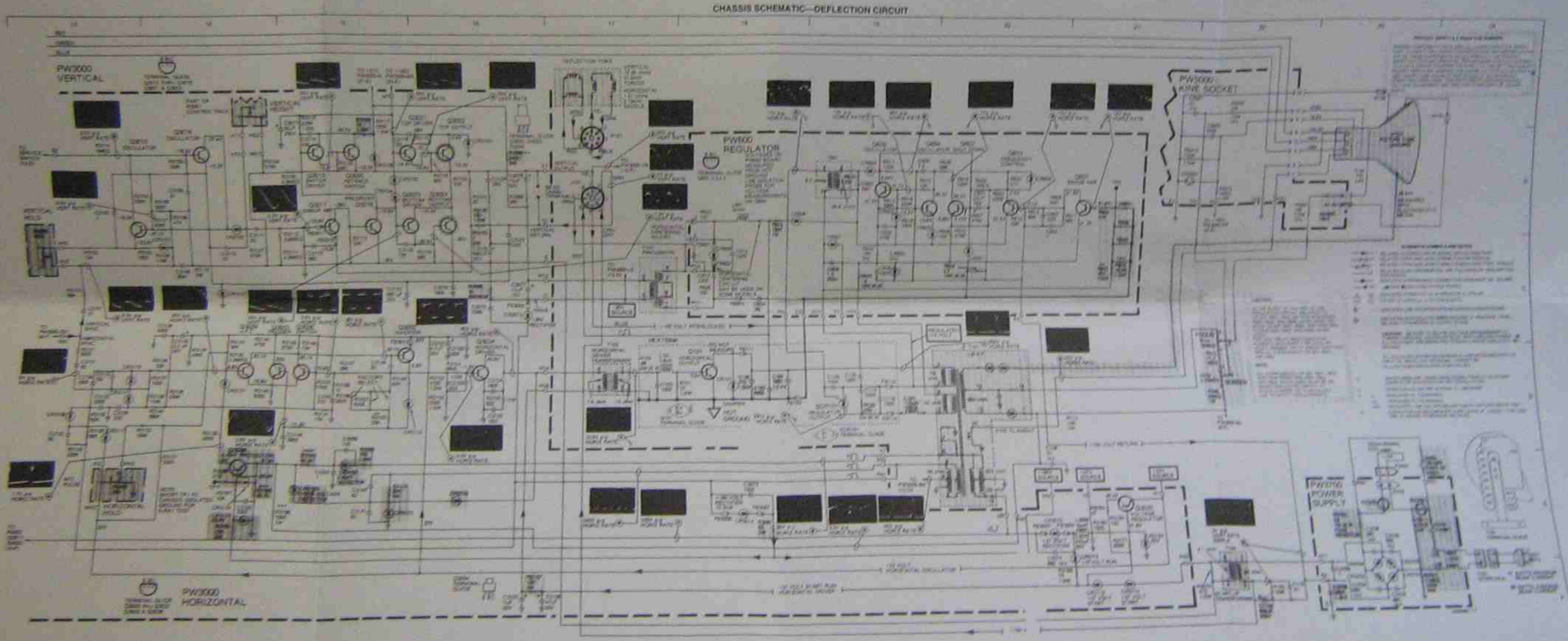

ELECTRONIC VIDEO SYSTEMS

DIAGNOSTICS AND MAINTENANCE

by Robert J. Schoenbeck

Intended for courses in television, VCR repair, or for advanced offerings in analog communications, this book provides readers with a practical introduction to video systems, beginning with the most obvious difference between radio and television and proceeding through computer monitors, VCRs, camcorders, cable TV, and high-definition television (HDTV). Robert Schoenbeck thoroughly identifies the components of each system, then explains how each component contributes to the system's overall operation. Through this building-block presentation, readers learn current solid-state and LSI circuitry, as well as how to apply this basic knowledge to the circuits and systems they will encounter in the future. Coverage reflects NTSC standards and compares them to systems such as PAL and SECAM to give readers the background needed to understand all of the various global systems now in use.

Outstanding features of this innovative book include:

- A picture guide to television troubleshooting that graphically illustrates the kinds of problems that television can develop.
- A troubleshooting flowchart that identifies what the technician should test for first.
- A detailed block diagram identifying what circuits to test.
- A picture/sound guide that illustrates what the problems look and sound like.
- Comprehensive coverage of each component in a single chapter that first defines what is required of the component, then explores how it is accomplished in a current product, and finally explains why the component is used.
- Discussion of computer monitors alongside television receivers to more clearly identify their similarities and differences.

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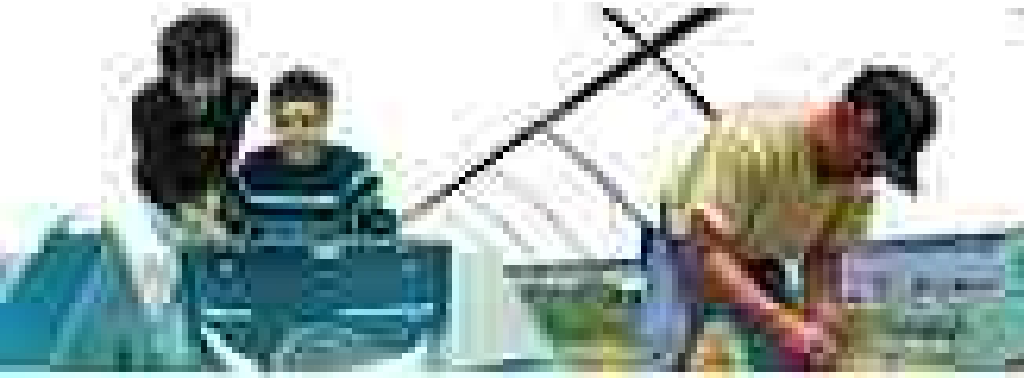



















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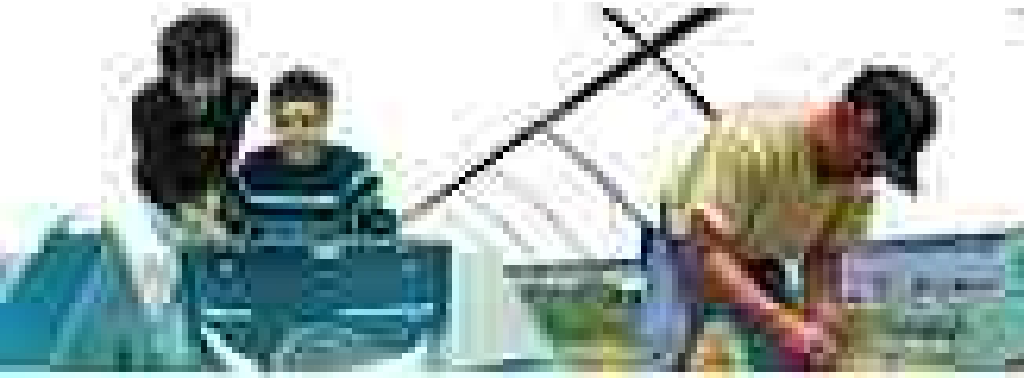



















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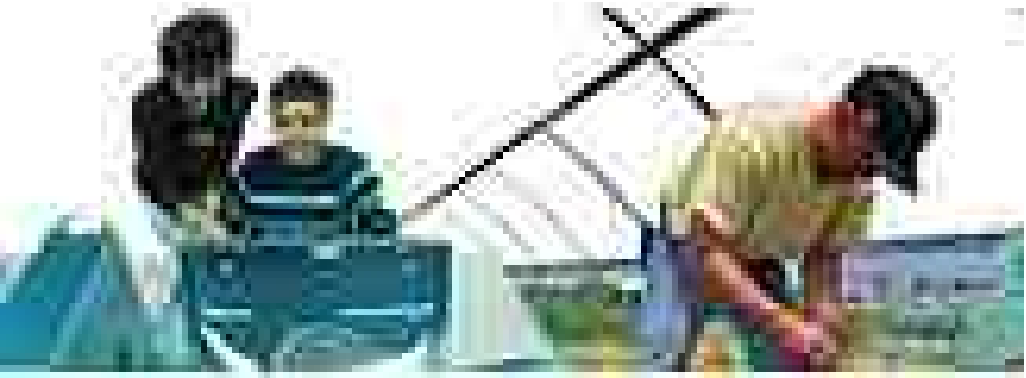
















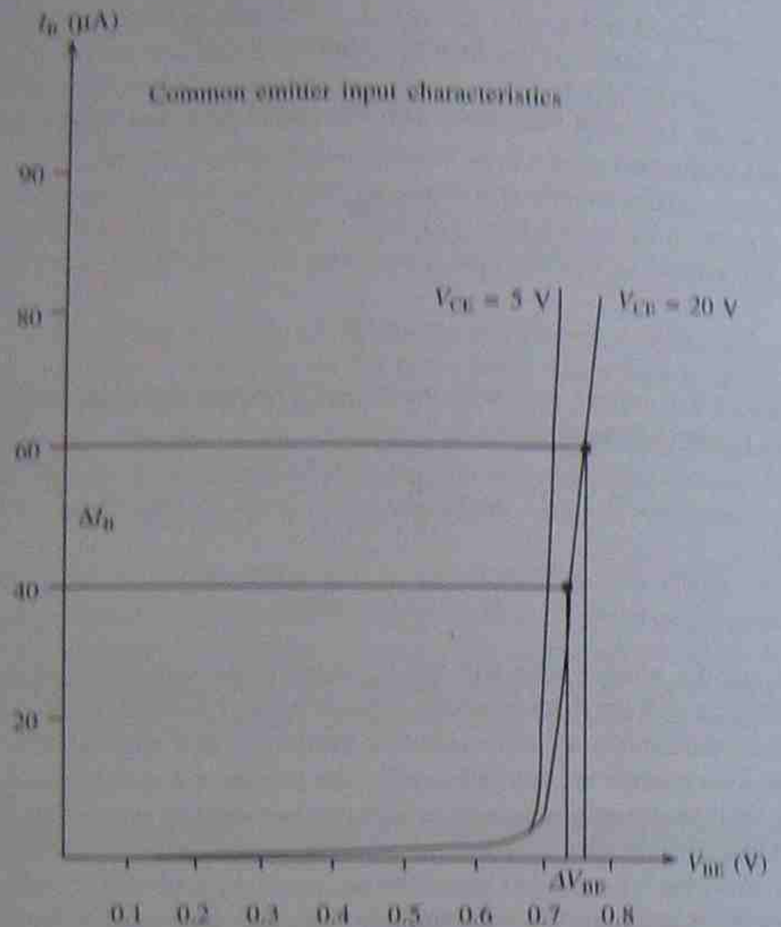


Fig. 5.3

supply voltage V_{CC}. The leakage current (I_{CEO}) is the only current flowing and it is very small.

The saturation condition occurs when the emitter junction is forward-biased and there is enough base current to produce a maximum collector current. Under these conditions the saturation current is calculated by using Ohm's law and using the collector load resistor (R_C) and the supply voltage V_{CC}:

$$I_{C(sat)} = \frac{V_{CC}}{R_C} \tag{5.7}$$

Consider Fig. 5.5, in which a base bias current of 60 μA has been selected. Using this characteristic shows a change of V_{CE} and I_C when solid projection is used. This gives

$$h_{OE} = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{2 \times 10^3}{0.24} = 8.3 \text{ k}\Omega$$

The current gain can be found for a fixed value of V_{CE}. In Fig. 5.5, $V_{CE} = 8.5$ V and the projection gives

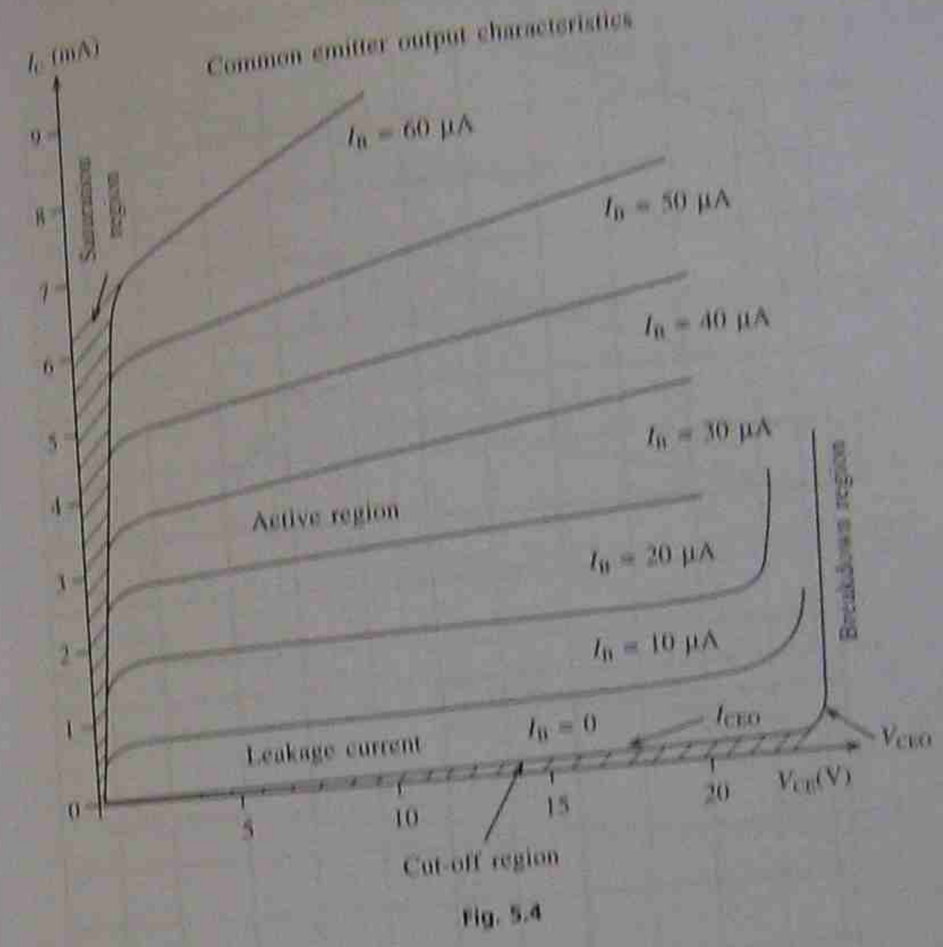


Fig. 5.4

$$h_{FE} = \frac{\Delta I}{\Delta I_B} = \frac{1 \times 10^6}{2 \times 10^4} = 50$$

Occasionally the mutual conductance (g_m) is required, and this is given by

$$g_m = \frac{I_C}{V_{BE}} = \frac{h_{FE}}{h_{IE}} = \frac{50}{36\,250} = 1.4 \text{ mA/V}$$

5.3 Transistor bias

Up to this point the active device has been considered, namely the transistor. The characteristics under these conditions are used as static curves. However, the ultimate use of the device is in an amplifier circuit and for this purpose the transistor has to be properly set up to accept and amplify the input a.c. signals without distortion. Under these conditions the characteristics are used as dynamic curves.

Figure 5.6 shows three conditions under which an amplifier may function, but of course it is the linear condition which is required as this condition is free of distortion. Mention has already been made of saturation and cut-off with respect to the output

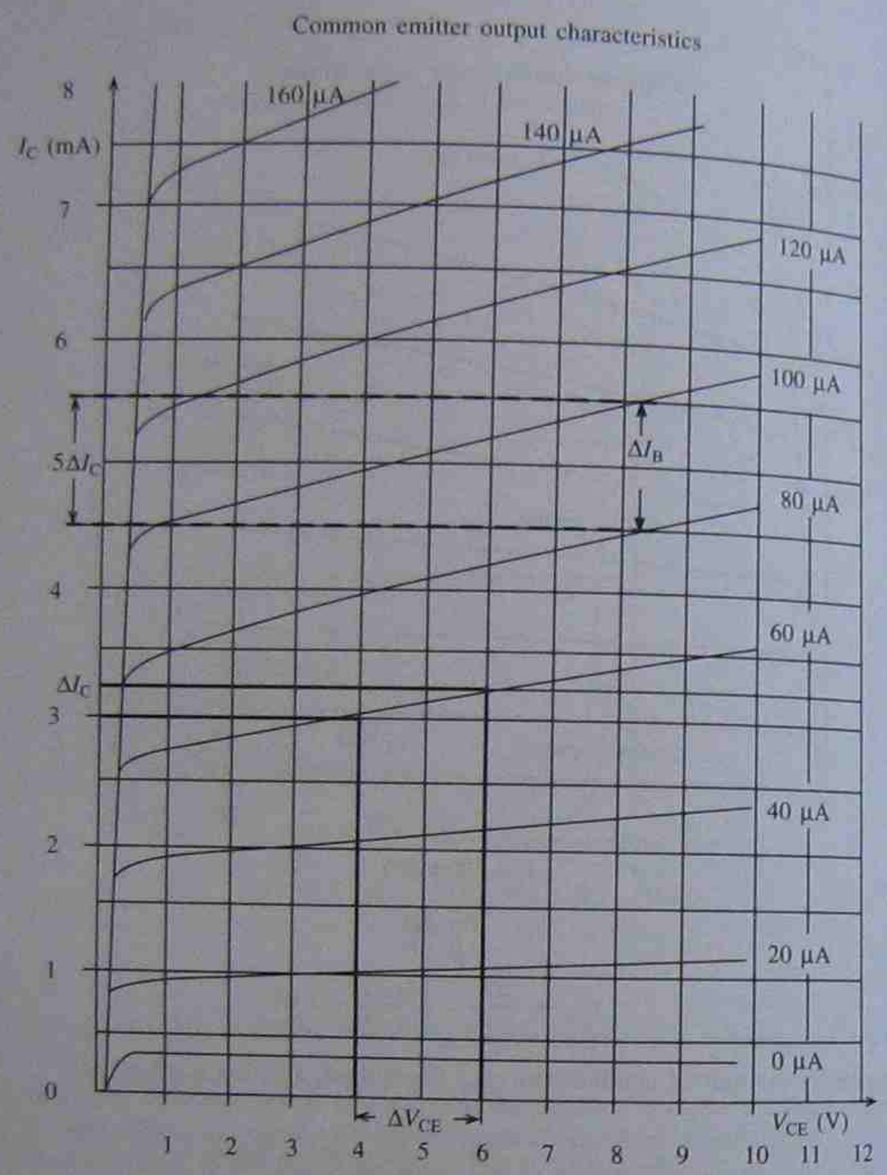


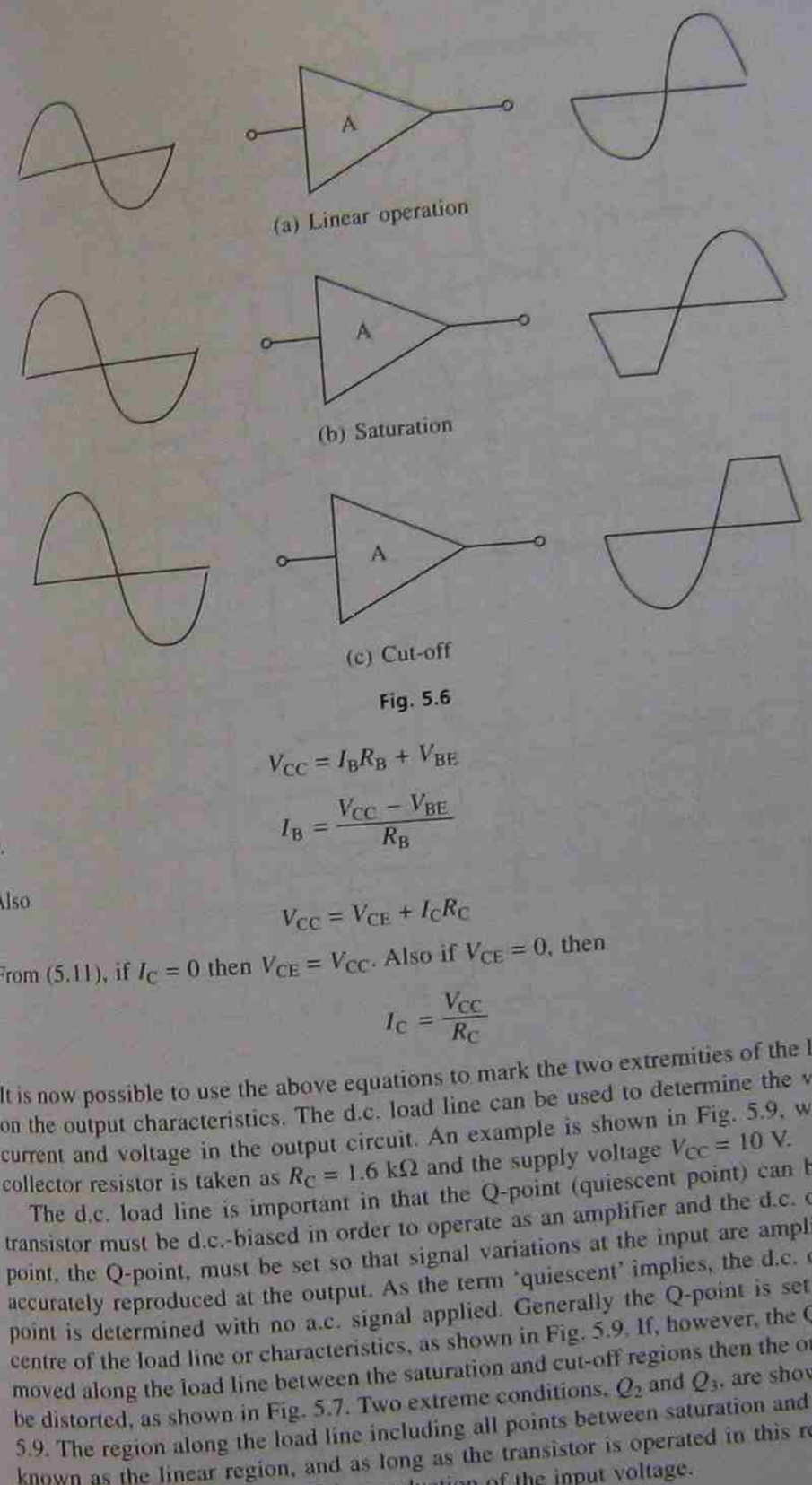
Fig. 5.5

characteristics. We can now see the effects on the output signal if these regions are entered, and this may occur if the input voltage swing is too large. Figure 5.7 shows the effects of saturation and cut-off on an output a.c. waveform using dynamic characteristics. In order to avoid this distortion the transistor has to be properly biased and the use of a load line is helpful in understanding this.

Consider firstly a simple common emitter amplifier, as shown in Fig. 5.8. We obtain

$$I_C = h_{FE}I_B + (I_{CEO}) \tag{5.8}$$

$$I_E = I_B + I_C = I_B + h_{FE}I_B$$
$$= (h_{FE} + 1)I_B \tag{5.9}$$



(a) Linear operation

(b) Saturation

(c) Cut-off

Fig. 5.6

$$V_{CC} = I_B R_B + V_{BE}$$

$$\therefore \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{5.10}$$

Also

$$V_{CC} = V_{CE} + I_C R_C \tag{5.11}$$

From (5.11), if $I_C = 0$ then $V_{CE} = V_{CC}$. Also if $V_{CE} = 0$, then

$$I_C = \frac{V_{CC}}{R_C} \tag{5.12}$$

It is now possible to use the above equations to mark the two extremities of the load line on the output characteristics. The d.c. load line can be used to determine the values of current and voltage in the output circuit. An example is shown in Fig. 5.9, where the collector resistor is taken as $R_C = 1.6\ \text{k}\Omega$ and the supply voltage $V_{CC} = 10$ V.

The d.c. load line is important in that the Q-point (quiescent point) can be set. A transistor must be d.c.-biased in order to operate as an amplifier and the d.c. operating point, the Q-point, must be set so that signal variations at the input are amplified and accurately reproduced at the output. As the term 'quiescent' implies, the d.c. operating point is determined with no a.c. signal applied. Generally the Q-point is set near the centre of the load line or characteristics, as shown in Fig. 5.9. If, however, the Q-point is moved along the load line between the saturation and cut-off regions then the output will be distorted, as shown in Fig. 5.7. Two extreme conditions, Q_2 and Q_3, are shown in Fig. 5.9. The region along the load line including all points between saturation and cut-off is known as the linear region, and as long as the transistor is operated in this region, the output voltage will be a faithful reproduction of the input voltage.

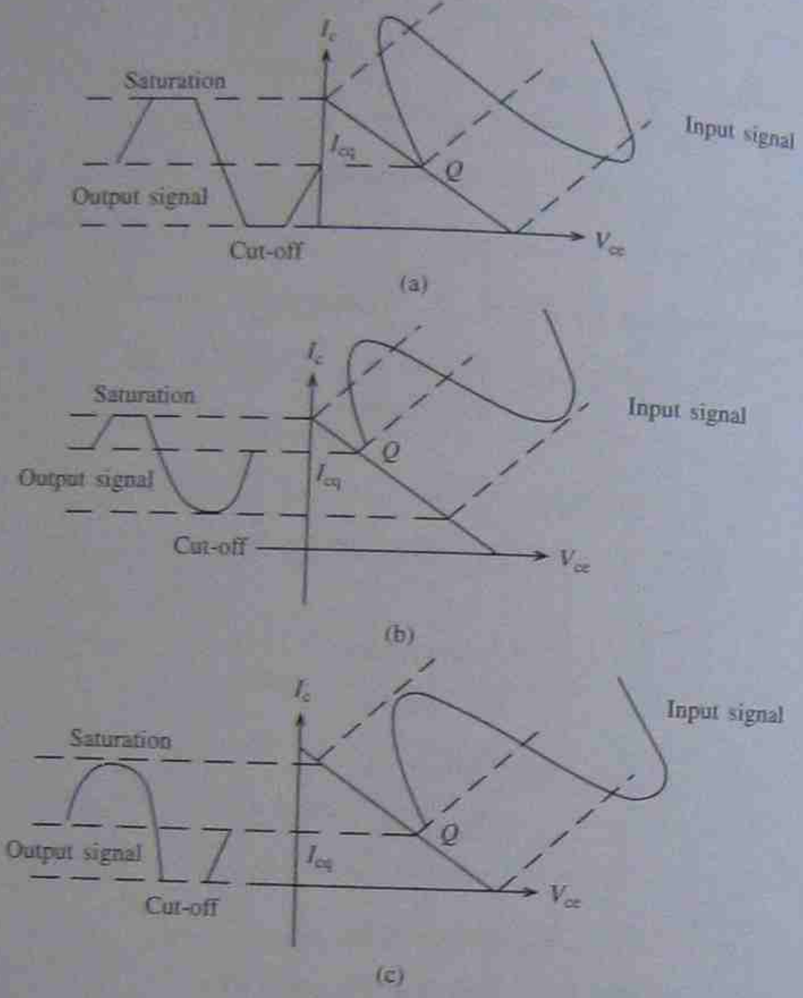


Fig. 5.7

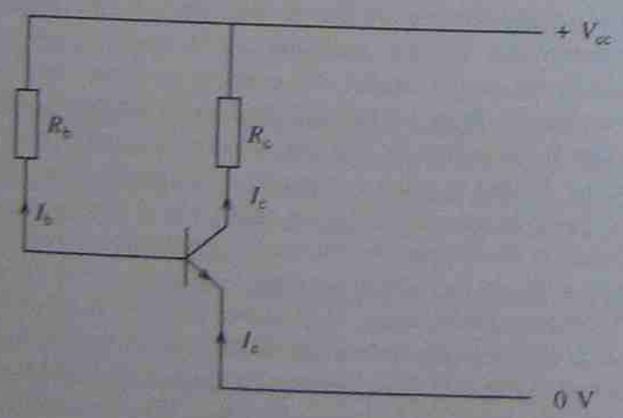


Fig. 5.8

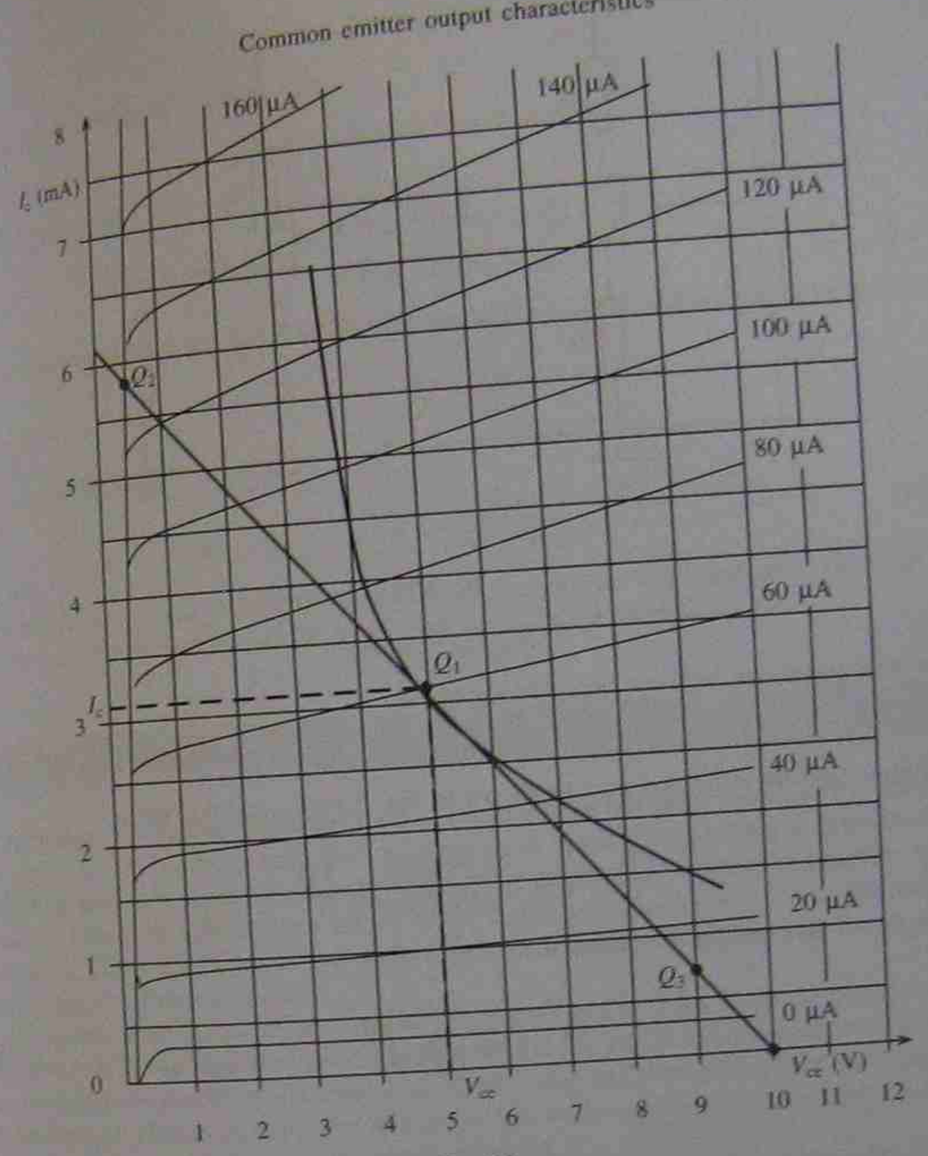


Fig. 5.9

Note that when I_B increases, I_C increases and V_{CE} decreases. Also when I_B decreases, I_C decreases and V_{CE} increases. Hence as the base bias voltage is adjusted the d.c. operating point moves along the load line and the parameters can be selected accordingly.

Voltage divider bias

Figure 5.8 uses what is called base bias, but in practice voltage divider bias is used as it provides better Q-point stability and can be used with a single supply. A typical circuit configuration is shown in Fig. 5.10. An analysis of this circuit must include the input resistance at the base which can be shown to be

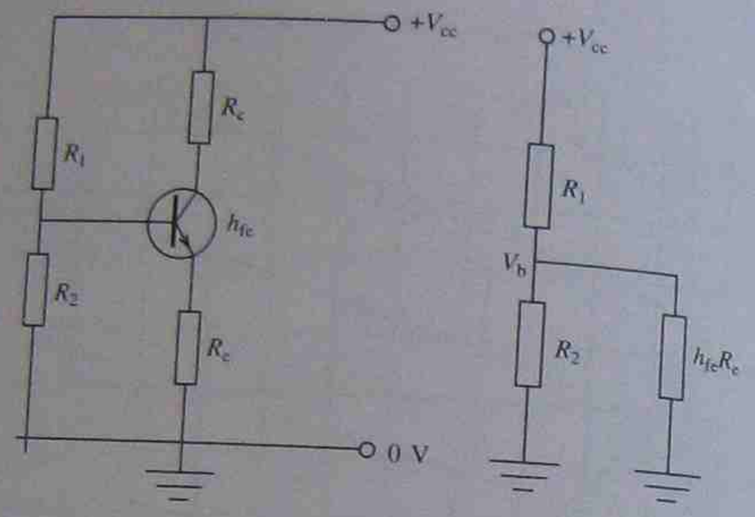


Fig. 5.10

$$R_{in(base)} \equiv h_{FE}R_E$$

The total resistance between base and ground is

$$R_2 \parallel h_{FE}R_E$$

A voltage divider is formed now as shown in Fig. 5.10(b), and this gives

$$V_B = \left(\frac{R_2 \parallel h_{FE}R_E}{R_1 + (R_2 \parallel h_{FE}R_E}\right) V_{CC} \qquad (5.13)$$

If $h_{FE}R_E >> R_2$ then this simplifies to

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC} \qquad (5.14)$$

Also

$$V_E = V_B - V_{BE}$$

and

$$I_E = \frac{V_E}{R_E}$$

and since

$$I_C \equiv I_E$$

then

$$I_C = \frac{V_B - V_{BE}}{R_E} \qquad (5.15)$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E$$

Also, using Kirchhoff's voltage law,

$$V_{CC} - I_C R_C - I_E R_E - V_{CE} = 0$$

and since $I_C \equiv I_E$,

$$V_{CE} \equiv V_{CC} - I_C R_C - I_C R_E$$
$$\equiv V_{CC} - I_C(R_C + R_E) \qquad (5.16)$$

Note that when drawing a d.c. load line the saturation current will no longer be given by

$$I_C = \frac{V_{CC}}{R_C}$$

but instead becomes

$$I_C = \frac{V_{CC}}{R_E + R_C} \qquad (5.17)$$

The cut-off point will remain the same when drawing the d.c. load line. This will be shown in the next section, which deals with small signal amplifiers.

5.4 Small signal voltage amplifiers

The biasing of a transistor is purely a d.c. operation, as has been shown in the previous sections. Also it has been seen that the purpose of biasing is to obtain a Q-point about which an input a.c. signal can cause variations in current and voltage. In practice, when dealing with such applications where small signal voltages have to be amplified, the variations about the Q-point are small. Amplifiers used in such applications are called small signal voltage amplifiers.

A typical small signal voltage amplifier is shown in Fig. 5.11. In this circuit the main difference is the inclusion of the capacitors C_1 and C_2, which are included to couple the a.c. signal to the amplifier while blocking the d.c. bias on the transistor from the input and output stages. Hence the capacitor effectively blocks d.c. and appears as a short circuit to a.c. signals, provided the correct value is selected.

Note also that the emitter resistor R_E is included in order to stabilize the bias conditions due to any temperature increases which would cause the collector current to increase. This is called **thermal runaway.** However, the inclusion of this resistor also lowers the a.c. gain of the amplifier. Hence there is a problem in that the emitter resistor is required for stability, but it reduces the a.c. gain. One solution to this is to connect a capacitor (the emitter bypass capacitor) in parallel with R_E as shown. This presents an open circuit to d.c., thus maintaining the effect of R_E for bias purposes, but a short circuit to a.c., thus shorting out R_E for a.c. purposes. This mode of operation is sometimes referred to as a single ended input. When operated in this mode one input is grounded and the signal voltage is applied to the other input. For the common emitter amplifier this causes an inverted signal at the output. Figure 5.12 may help to clarify the operation of this amplifier.

Figure 5.12 shows both the a.c. and the d.c. load lines, together with the expressions necessary to determine the cut-off and saturation points. These have been derived in

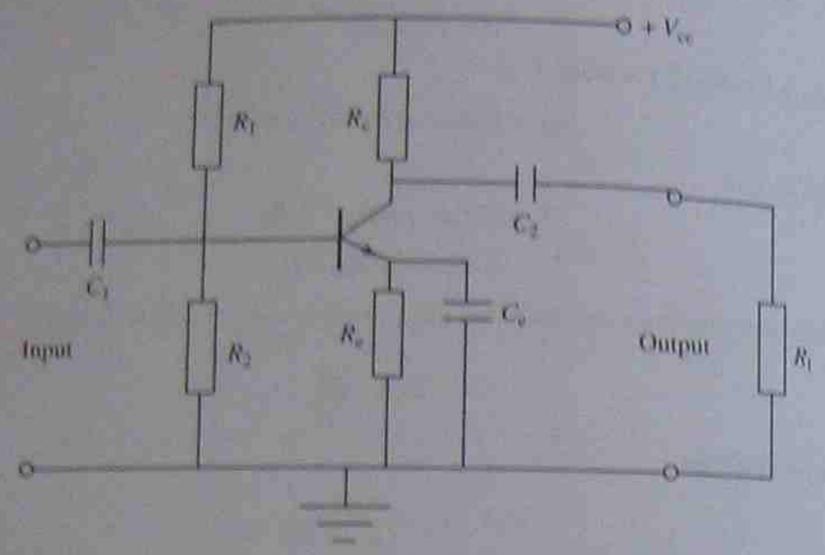


Fig. 5.11

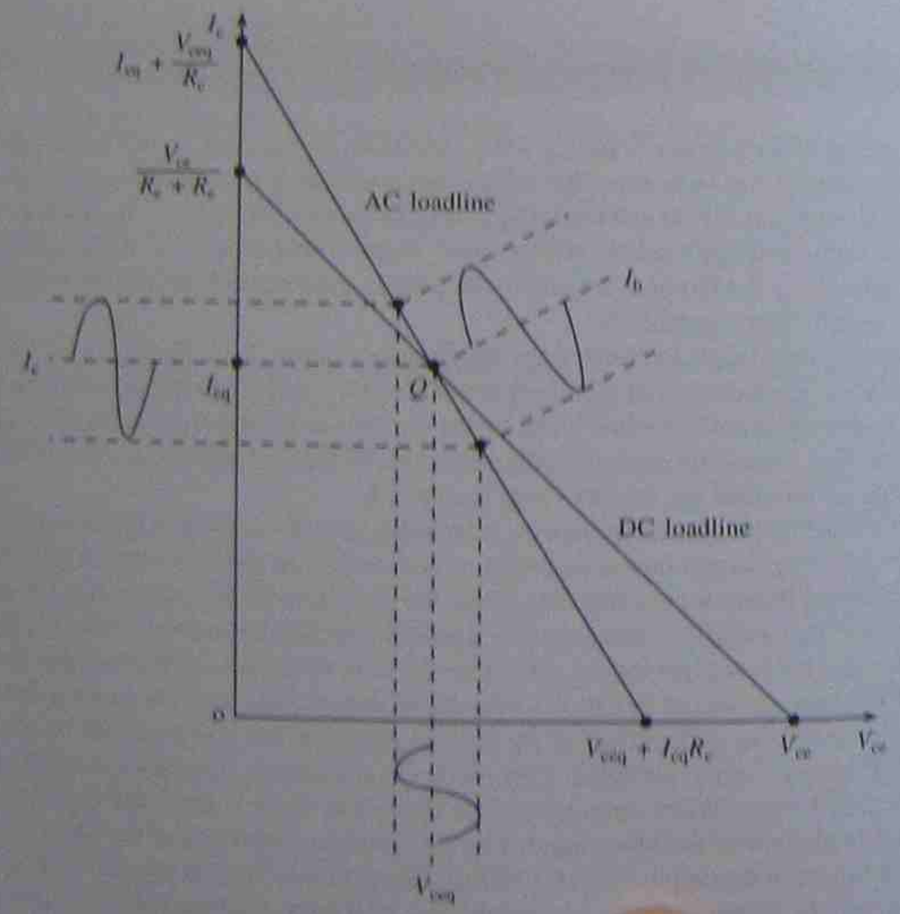


Fig. 5.12

previous sections. Also note that the collector current lies within the linear region of the amplifier; as has already been mentioned, this is necessary for an undistorted output. This is known as class A bias and indicates that the amplifier operates for the full 360° of the input voltage. However, there are two other common types of bias, and these are shown in Fig. 5.13.

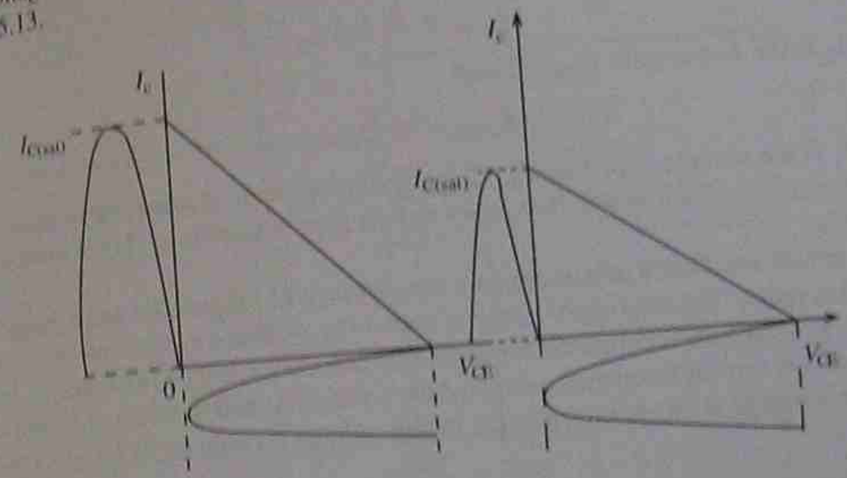


Fig. 5.13

Figure 5.13(a) shows what happens to the output signal when an amplifier is biased at cut-off. It operates in the linear region for 180° of the input cycle and is in cut-off for the other 180°. This is known as class B bias and is used regularly in power amplifiers. A variation of this is the class AB biased power amplifier which is biased to conduct for slightly more than 180°.

Figure 5.13(b) shows the result of biasing so that conduction occurs for less than 180°. Because the output is severely distorted class C amplifiers are limited to such applications as tuned amplifiers and oscillators.

5.5 The use of the decibel

Associated with power amplifiers and voltage amplifiers is the frequency response of the amplifier. This deals with gain, roll-off, bandwidth and other parameters. However, it is

customary to use the decibel to determine the gain or attenuation of an amplifier rather than a magnitude gain such as 100 or 500.

The decibel is related to the logarithmic response of the ear to the intensity of sound and is defined as the ratio of one power to another or one voltage to another. Two expressions are generally used:

$$A_{p(dB)} = 10 \log A_p \tag{5.18}$$

where A_p is the power gain P_{out}/P_{in}, and

$$A_{v(dB)} = 20 \log A_v \tag{5.19}$$

where A_v is the voltage gain V_{out}/V_{in}. If the voltage gain A_v is greater than unity the dB gain is positive, and if it is less than unity the dB gain is negative. This is usually called attenuation.

Most amplifiers show a maximum gain over a range of frequencies and a reduced gain outside this range. The maximum range is called the midband range, and the frequency where the gain falls off is called the critical frequency. As described in Chapter 3, in terms of decibels this critical frequency occurs at the 3 dB point and in terms of power we say the power is halved at this point while the output voltage is taken as 70.7% of its midband range.

5.6 Types of power amplifier

Now that the fundamentals of the small signal amplifier have been discussed, we will look at the power amplifier. In many respects this is like the voltage amplifier, except for the large signal swings and larger power dissipation which are not present in the small signal voltage amplifier. There are three popular types of power amplifier frequently used in power applications: the class A (single-ended) amplifier; the class B push-pull (transformer) amplifier; and the class B complementary pair push-pull amplifier. Each of these types will be considered in turn.

Class A (single-ended) amplifier

A single-ended power amplifier uses a single transistor with the usual biasing arrangement as for a voltage amplifier, but there the similarity ends. A typical circuit is shown in Fig. 5.14. Unlike the small signal voltage amplifier this circuit has to drive a current operated load, and this requires large collector current swings to operate the matching transformer and loudspeaker. A voltage amplifier would use a high resistive load but here the load is the low resistance primary of a transformer, the transformer being used to match the high collector resistance of the transistor.

When dealing with power amplifiers it is necessary to know the operating conditions as well as the power rating of the active device. Figure 5.15 shows a set of output characteristics together with the power dissipation curve and a.c. and d.c. load lines. The power curve shows the operational region inside which the device will operate within its rated power value. This area is marked *ABCD*. Often a heat sink has to be attached to the device to achieve the rated value.

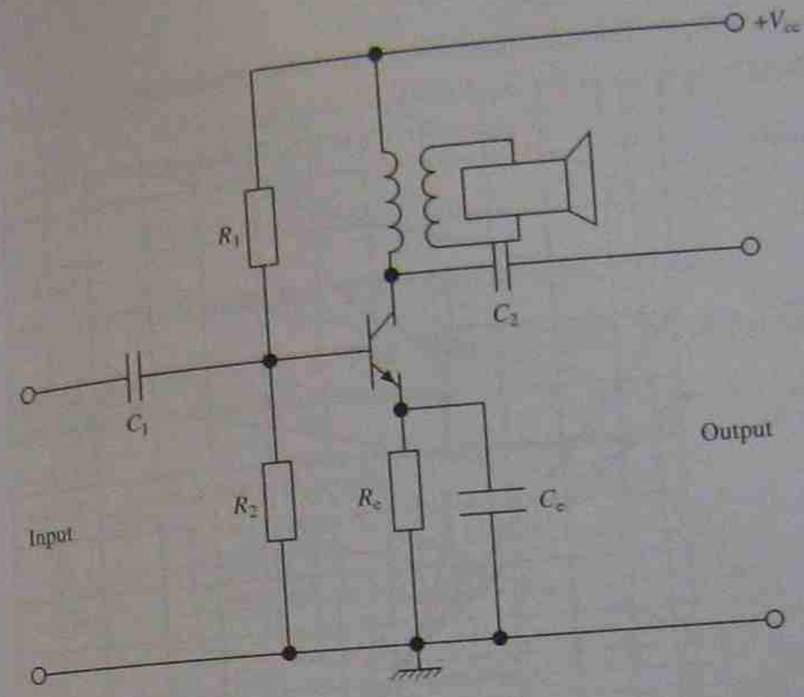


Fig. 5.14

The d.c. load line is determined by knowing the values of the collector resistance (R_C) and emitter resistance (R_E). The slope of the d.c. load line is then given as

$$\text{Slope} = \frac{1}{R_C + R_E} \tag{5.20}$$

The value of R_E is generally between 500 Ω and 1000 Ω. The d.c. load line is drawn for the d.c. operating conditions of the device without the load attached. The a.c. load line takes the load (R_L) into consideration so that

$$R_T = \frac{R_C R_L}{R_C + R_L} \tag{2.21}$$

In summary, the d.c. load line is used to set up the quiescent conditions without an input signal, while the a.c. load line sets up the amplifier for input signal conditions.

While graphical solutions are seldom used in problem-solving, it is instructive to consider the meaning of characteristics under d.c. and a.c. operating conditions. The d.c. power in this case is the product of the supply voltage and the d.c. component of the collector current, i.e.

$$P_{DC} = V_{CC} I_C \tag{5.22}$$

Because of losses due to transformer resistance, emitter resistance and collector dissipation, the output a.c. power delivered to the load is less than the d.c. power. Also since the main power loss is in the collector,

$$P_{DC} = P_{AC} + P_C \tag{5.23}$$

The following points should be observed from Fig. 5.15:

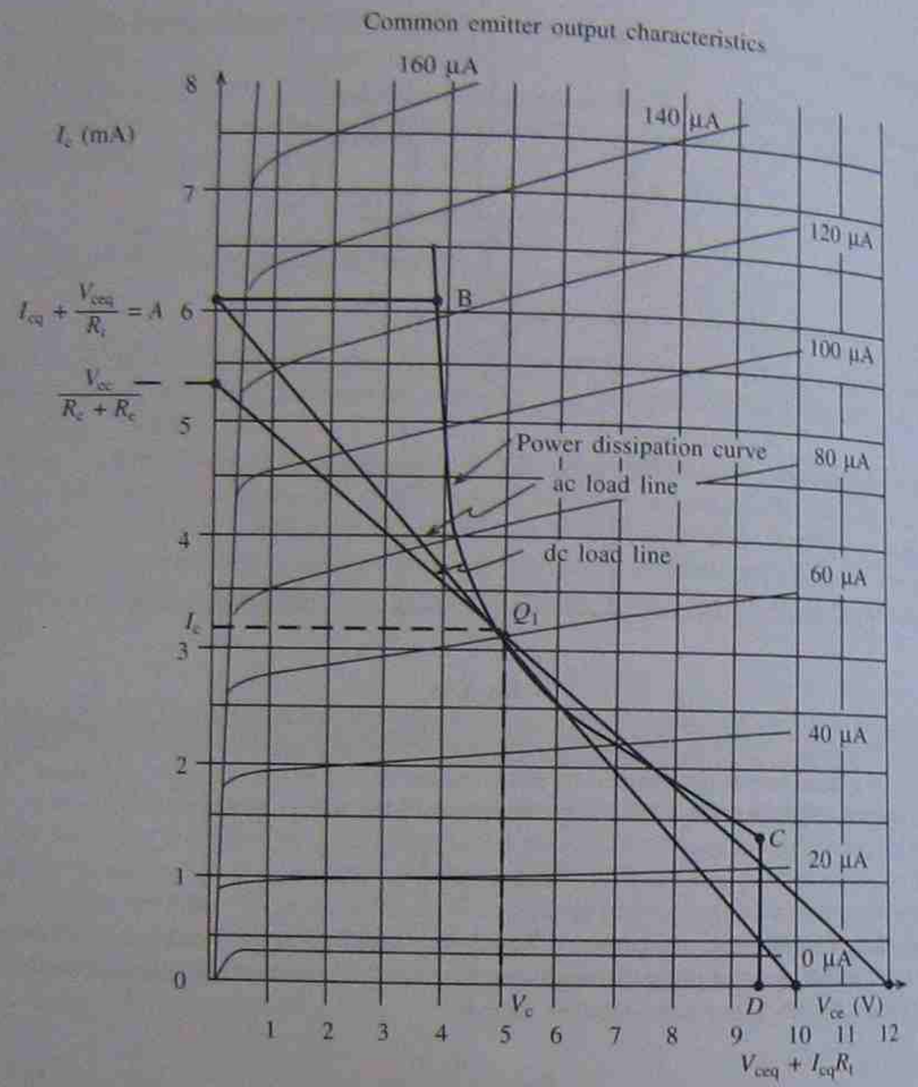


Fig. 5.15

(a) The a.c. load line sets the maximum limits of the current and voltage swings at the output.

(b) The quiescent point sets the d.c. operating conditions for the device and should be chosen to give an undistorted output. If this is not chosen properly, flattening of the waveform could occur.

(c) The intersection of the d.c. and a.c. load lines determines the Q-point, and this is normally achieved by the bias resistors.

(d) When no signal is applied, the quiescent voltage equals the supply voltage.

(e) When no signal is applied, the quiescent current is half the maximum collector current.

(f) The power dissipation curve sets the limits to how much power may be dissipated in the collector of the transistor.

(g) The corresponding base current can be determined for each collector current.

(h) The turns ratio of the transformer (n) transforms the actual load of loudspeakers (R_2) into the optimum load (R_1) of the transistor, i.e.

$$n = \sqrt{\frac{R_1}{R_2}}$$

(i) Maximum collector dissipation occurs when no signal is applied.

Figure 5.16 shows the effect of an input signal. The resultant swings of the collector current and voltage are given as peak-to-peak.

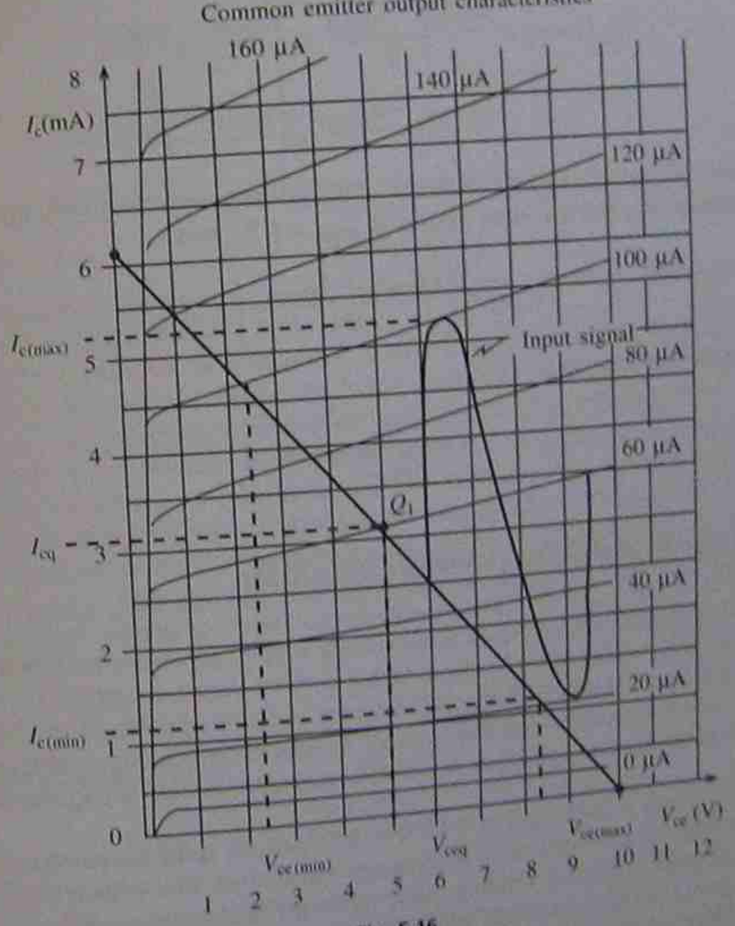


Fig. 5.16

In the above characteristics the current and voltage swing between cut-off and saturation. The efficiency of the stage will be 50% under these conditions but the distortion will be severe so in practice the actual swings are reduced. This results in an efficiency of about 25%. It is for this reason that this type of circuit is not often used.

Practical analysis of class A single-ended parameters

The application of an a.c. signal to a power amplifier causes large current (I_c) and voltage (V_{ce}) swings. The collector current swings between $I_{c(max)}$ and $I_{c(min)}$, while the collector-emitter voltage swings between $V_{ce(max)}$ and $V_{ce(min)}$. The average current and the average voltage are given by

$$\frac{V_{ce(max)} - V_{ce(min)}}{2} \text{ and } \frac{I_{c(max)} - I_{c(min)}}{2} \tag{5.24}$$

The output power in the load is generally given in r.m.s. values, and if the matching transformer is assumed to be 100% efficient then the output power ($P_{ac(rms)}$) is given by

$$P_{ac(rms)} = \frac{I_{c(max)} - I_{c(min)}}{2\sqrt{2}} \times \frac{V_{c(max)} - V_{c(min)}}{2\sqrt{2}}$$

$$= \frac{(I_{c(max)} - I_{c(min)})\,(V_{c(max)} - V_{c(min)})}{8} \tag{5.25}$$

An alternative expression given in terms of the primary resistance (R_1), the secondary load resistance (R_2) and the turns ratio is $P_{ac(rms)} = I^2 R_1$; hence

$$P_{ac(rms)} = \left[\frac{(I_{c(max)} - I_{c(min)})}{8}\right] n^2 R_2 \tag{5.26}$$

The collector efficiency is given by

$$\eta = \frac{P_{dc}}{P_{ac(rms)}} \times 100 \tag{5.27}$$

Class B push-pull (transformer) amplifier

Only class A amplification gives a distortionless output. By using push-pull circuits, however, class B amplification can be obtained with no output distortion. Furthermore, higher efficiencies are achieved. An added bonus is the elimination of even harmonic distortion which drives the collector current beyond its maximum permitted swing. The result of this is that an output power almost double that of a single transistor is produced.

A typical circuit is shown in Fig. 5.17. The driver circuit splits the phase of the input signal into two signals which are in antiphase to one another. This is done by taking the driver transformer secondary winding centre tap to the earth or common line. When no signal is present the only current flowing in the transistors is the quiescent current. This quiescent current does not produce any d.c. magnetization of the output transformer core because the magnetic forces effectively cancel. The output transformer can therefore be made smaller.

When a signal is applied the antiphase base currents will produce antiphase collector currents. These collector currents effectively add in the output transformer and the a.c. power is fed via the secondary to R_L. The signal currents do not pass through the power

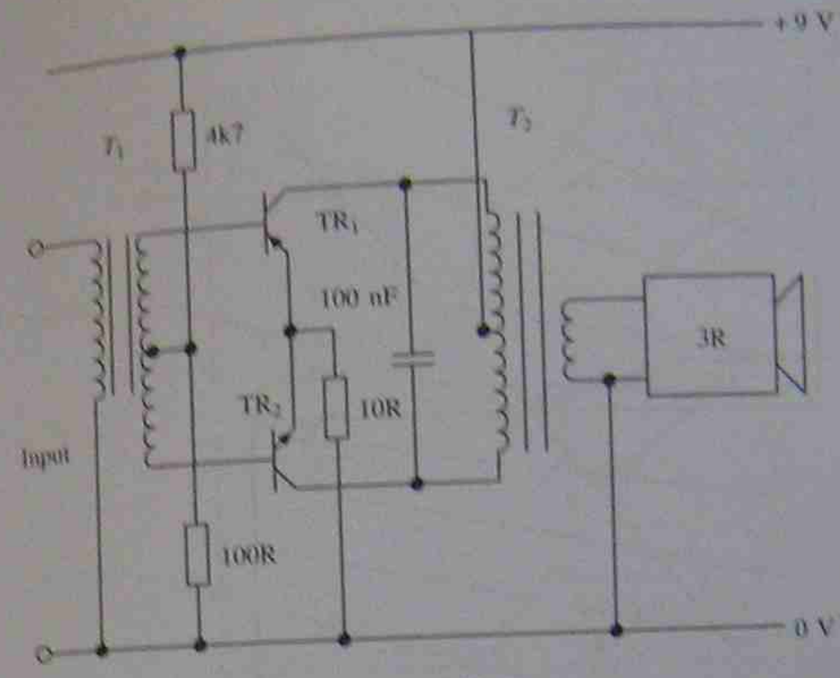


Fig. 5.17

supply or bias components. If the supply is derived from a.c. mains there is no tendency for mains hum to be introduced in this stage.

The operation of this type of amplifier is more clearly seen in Fig. 5.18, which shows the two sets of output characteristics for both transistors combined to form the composite characteristic. The point V_{cc} represents the operating point of both transistors and hence the two a.c. load lines coincide for transistors T_1 and T_2. At point 1 on the input signal for T_1 the collector current is maximum and this is represented by D on the common characteristics. At point 2 the transistor is at cut-off point A and no collector current flows in either transistor. At point 3 the collector current of T_2 is maximum and the collector-emitter voltage is zero. This is point E. If all the variations of collector current and collector-emitter voltage were plotted the composite curve shown in Fig 5.18 would be produced.

Crossover distortion

Push-pull power amplifiers are subject to distortion as shown in Fig. 5.19(a). The mutual characteristics are shown in Fig. 5.19(b), in which the non-linear input characteristics cause distortion as one transistor turns on and another turns off. This effect may be reduced by introducing class AB biasing. Such biasing causes both the output transistors to conduct a small collector current when no signal is fed to the amplifier. Normally 0.6 V is provided by means of two resistors or two diodes. However, diodes are generally preferable because of temperature changes. This means that the potential difference across them will vary in the same way as the base–emitter voltage of the output transistors. One particular configuration is shown in Fig. 5.20, which shows the application of two diodes in the biasing circuit, preventing crossover distortion.

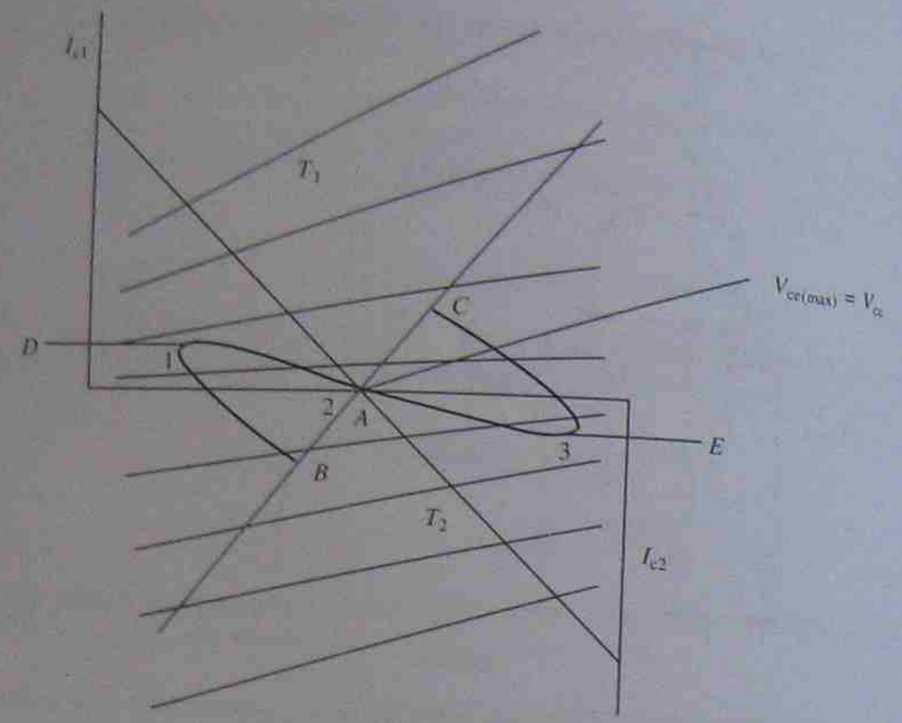


Fig. 5.18

Class B complementary pair push-pull

This type of power amplifier performs in exactly the same way as the transformer type except that two different transistors are now used, i.e. npn and pnp, which complement each other to give a faithful reproduction of the input voltage. A typical practical circuit is shown in Fig. 5.20. Once again each transistor only handles 180° of the input signal, and when there is no input signal both the transistors are switched off. Hence there is no current drawn by the system at the output which once again increases the efficiency of the system. As before, if the input swings positive T_1 will switch on and current will flow through R_L. When the input swings negative T_1 is off while T_2 is switched on, thus causing a current once again through R_L. T_1 thus pushes the current through R_L, while T_2 pulls the current through R_L.

Several practical points should be noted about this circuit:

(a) Figure 5.18 showed that the supply voltage indicated at the crossover point of the characteristic was V_{cc}. This is not the case with the complementary circuit, where the supply voltage is equal to half the maximum collector-emitter voltage of the transistors used. Otherwise the characteristics are identical for this configuration. In Figure 5.20 the two 10 Ω resistors set the bias conditions so that the junction is at half the supply voltage ($V_{cc}/2$).

(b) Diodes are used rather than bias resistors because they are manufactured from silicon and hence have similar temperature characteristics to the transistors. Also if they are mounted on the same heat sink they will undergo similar temperature and voltage changes.

(c) Complementary pair transistors are available in matched pairs in order to ensure they have identical characteristics.

(d) The use of the diodes provides class AB biasing.

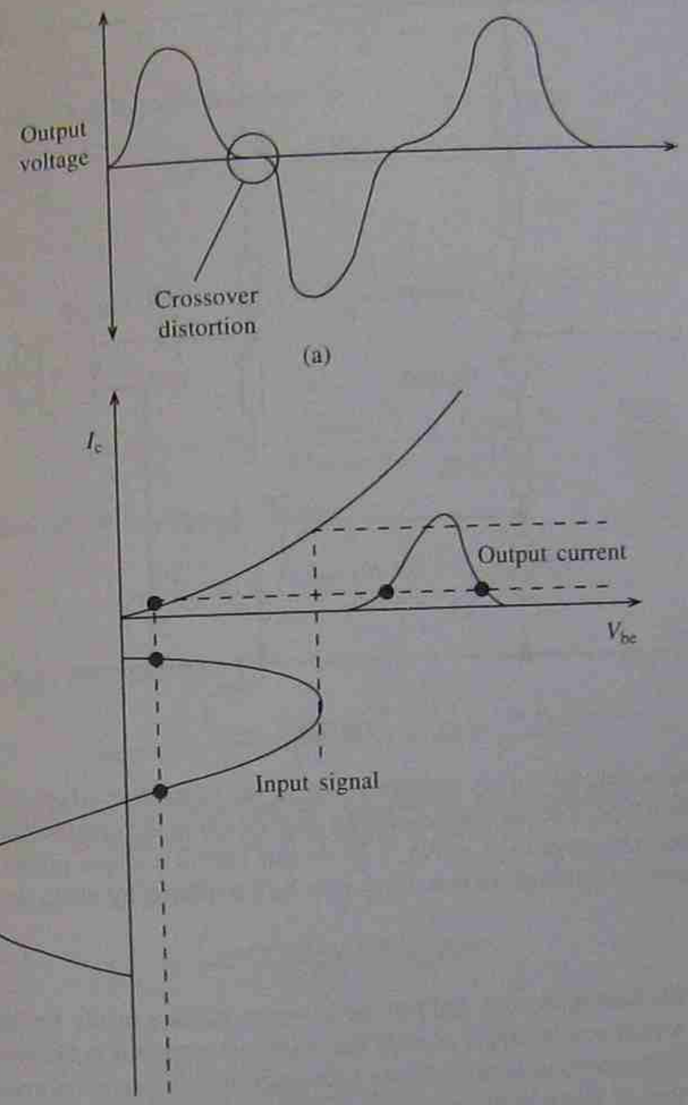


Fig. 5.19

Practical analysis of class B push-pull parameters

Both the push-pull transformer transforms and complementary pair types follow the same

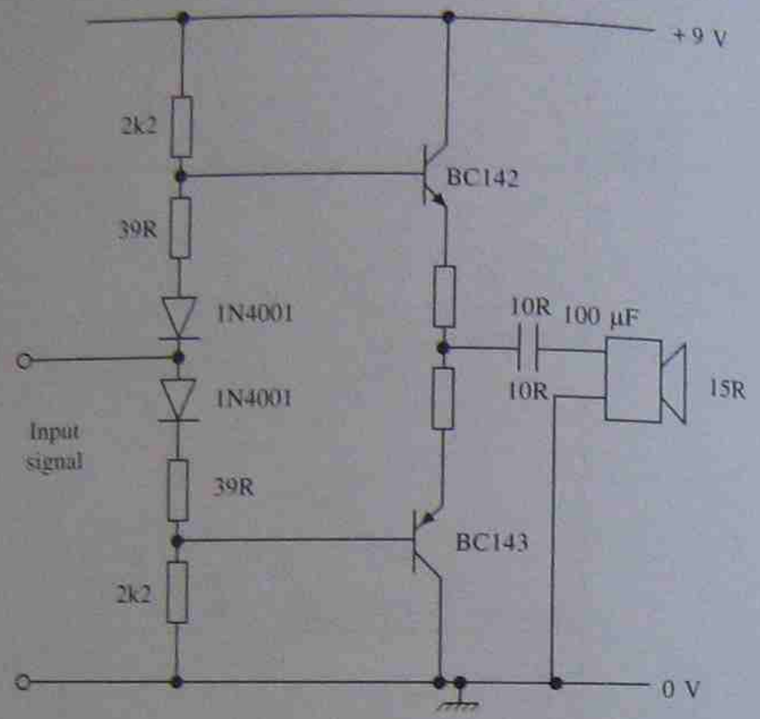


Fig. 5.20

analysis, except that the supply voltage is V_{cc} in the transformer type and $V_{cc}/2$ for the complementary type. The parameters will be derived using the complementary symmetry circuit similar to the type used in Fig. 5.20. In this circuit a single power supply is used and the capacitor C (100 µF in this case) may be calculated by using the expression

$$f = \frac{1}{2\pi C R_l} \tag{5.28}$$

where R_l is the load resistance and f is the lower frequency of the frequency response. Note that if a dual power supply is used the coupling capacitor is not necessary.

The collector current in each transistor takes the form of a series of rectified pulses. A Fourier analysis of this waveform will give an instantaneous value of

$$i_c = \frac{I_{c(max)}}{\pi} + \frac{I_{c(max)}}{2\pi}\sin\omega t - \frac{2I_{c(max)}}{3\pi}\cos 2\omega t \tag{5.29}$$

The first term in this expansion represents a d.c. component and the second term is the fundamental frequency component. Harmonics can be ignored as these are mostly reduced to a small percentage or eliminated entirely.

The fundamental r.m.s. a.c. power produced by each transistor to a load is

$$P_{ac(rms)} = \left(\frac{I_{c(max)}}{2\sqrt{2}}\right)^2 R_l \tag{5.30}$$

Note that R_l is the load into which the transistor feeds. Therefore total power delivered by both transistors is

$$P_{ac(rms)} = \frac{I_{c(max)}^2 R_l}{4} \tag{5.31}$$

Also the d.c. power taken by each transistor is

$$\frac{I_{c(max)} V_{cc}}{2} \tag{5.32}$$

Hence total power is

$$P_{dc} = \frac{I_{c(max)} V_{cc}}{\pi} \tag{5.33}$$

So the efficiency is given by

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{I_{c(max)}^2 R_l}{4 I_{c(max)} V_{cc}} = \frac{I_{c(max)} R_l}{4V_{cc}} \tag{5.34}$$

The same solution can be achieved by using

$$P_{ac(rms)} = \left[\frac{I_{c(max)} - I_{c(min)}\,(V_{cc}/2 - V_{ce(min)})}{2\sqrt{2}}\right] \times 2$$

As $I_{c(min)}$ and $I_{ce(min)}$ are small then

$$P_{ac(rms)} = \frac{I_{c(max)} \times V_{cc} \times 2}{8} = \frac{I_{c(max)} \times V_{cc}}{4} \tag{5.35}$$

One final consideration when selecting an integrated circuit or transistor for an application is its power rating. The total collector dissipation is given as

$$P_c = P_{dc} - P_{ac}$$

$$= \frac{I_{c(max)} V_{cc}}{\pi} - \frac{I_{c(max)} V_{ce(max)}}{2}$$

Since

$$I_{c(max)} = \frac{V_{ce(max)}}{R_L}$$

$$P_d = \frac{V_{cc} V_{ce(max)}}{\pi R_l} - \frac{V_{ce(max)}^2}{2R_l} \tag{5.36}$$

Differentiate (5.36) to determine the maximum dissipation:

$$\frac{dP_d}{dV_{ce(max)}} = \frac{V_{cc}}{\pi R_L} - \frac{2V_{ce(max)}}{2R_l}$$

Therefore

$$V_{ce(max)} = \frac{V_{cc}}{\pi} \tag{5.37}$$

Substituting (5.37) into (5.36) gives

$$P_{dc(max)} = \frac{V_{cc}^2}{\pi^2 R_l} = \frac{V_{cc}^2}{2\pi^2 R_l} = \frac{V_{cc}^2}{2\pi^2 R_l}$$

Since the maximum power occurs when $V_{ce(max)} = V_{cc}/2$ for complementary symmetry, and this occurs at $P_{ac(max)} = V_{cc}^2/8R_l$, then

$$P_{c(max)} = \frac{4P_{ac(max)}}{\pi^2} = 0.4P_{ac(max)} \tag{5.38}$$

This is the total power dissipation for both transistors used in a push-pull arrangement.

Example 5.1
The supply voltage of a complementary amplifier is 30 V and the output feeds into a load of 12 Ω. Determine:

(a) the maximum collector current if an efficiency of 60% is required;

(b) the maximum rated values of the transistors used.

Solution
(a)

$$\eta = \frac{I_{c(max)} R_l}{4V_{cc}}$$

$$\therefore \quad I_{c(max)} = \frac{4V_{cc}\,N}{R_l} = \frac{4 \times 30 \times 0.6}{12\pi} = 1.91 \text{ A}$$

(b)

$$P_{c(max)} = \frac{4P_{ac(max)}}{\pi^2}$$

$$P_{ac(max)} = \frac{V_{cc}^2}{8R_l} = \frac{900}{96}$$

$$\therefore \quad P_{c(max)} = \frac{4 \times 900}{96\pi^2} = 3.80 \text{ W}$$

Hence each transistor rated at 1.90 W.

Example 5.2
A class B push-pull transformer power amplifier has an output configuration as shown in Fig. 5.21. The output transformer is centre tapped such that the turns ratio is $N_1 : N_2 : N_3 = 5 : 5 : 2$. Determine:

(a) the maximum collector current produced in the primary by both transistors if the a.c. power delivered to the primary is 12.5 W;

(b) the value of supply voltage required under these conditions;

(c) the efficiency of the amplifier.

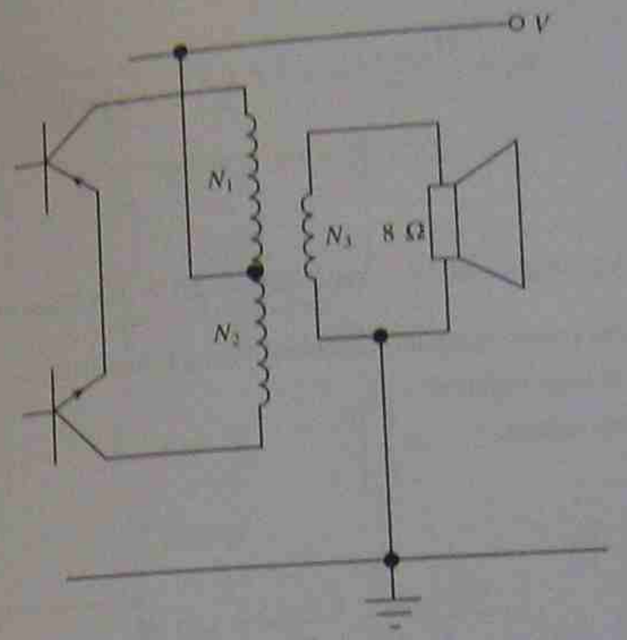


Fig. 5.21

Solution
(a) Since the turns ratio is 5 : 5 : 2, the load into which the transistors feed in the secondary is

$$\frac{N_1}{N_3} = \frac{N_2}{N_3} = \frac{5}{2} = \sqrt{\frac{R_l}{8}}$$

$$\therefore \quad R_l = \frac{25}{4} \times 5 = 50$$

Since, for transformer push-pull,

$$P_{ac(rms)} = \frac{I_{c(max)}^2 R_l}{4}$$

$$I_c = \sqrt{\frac{4 \times 12.5}{50}} = 1 \text{ A}$$

(b)

$$P_{ac(rms)} = \frac{I_{(max)} V_{cc}}{2}$$

$$\therefore \quad V_{cc} = \frac{2P_{ac(rms)}}{I_{(max)}} = \frac{2 \times 12.5}{1} = 25 \text{ V}$$

(c)

$$\eta = \frac{P_{ac(rms)}}{P_{dc}} \times 100$$

$$P_{dc} = \frac{2I_{c(max)}V_{cc}}{\pi} = \frac{2 \times 1 \times 25}{\pi} = 15.9 \text{ W}$$

$$\therefore \quad \eta = 12.5 \times \frac{\pi}{50} \times 100 = 78.5\%$$

Example 5.3

A complementary push-pull amplifier has to deliver 2.5 W into a load of 8 Ω. Determine:

(a) the maximum power dissipation required for each transistor;

(b) the supply voltage required;

(c) the peak load current.

Solution

(a)

$$\frac{4P_{o(max)}}{\pi^2} = \frac{4 \times 2.5}{\pi^2} = 1.01 \text{ W}$$

(b) Since

$$P_{o(max)} = \frac{V_{cc}^2}{2\pi^2 R_l}$$

$$V_{cc} = \sqrt{P_{o(max)} 2\pi^2 R_l} = \sqrt{\frac{10}{\pi^2} \times 2\pi^2 \times 8} = \sqrt{160} = 12.65 \text{ V}$$

(c)

$$P_{ac(max)} = \frac{V_l^2}{R_l}$$

$$\therefore \quad V_l = \sqrt{P_{ac(max)} R_l} = \sqrt{2.5 \times 8} = 4.5 \text{ V}$$

$$\therefore \quad V_{(max)} = \sqrt{2} \times \sqrt{20} = \sqrt{40} = 6.32 \text{ V}$$

∴ Peak load current is

$$I_{(max)} = \frac{V_{(max)}}{R_l} = \frac{6.32}{8} = 0.79 \text{ A}$$

Example 5.4

The complementary push-pull audio amplifier shown in Fig. 5.22 has to provide 5 W into a load of 4 Ω. The 3 dB bandwidth of the amplifier has to be flat between 80 Hz and 18 kHz. The data for the two transistors are as follows: $I_{C(max)} = 4$ A, $P_{(max)} = 36$ W, $h_{fe} = 40$ and $V_{CE(max)} = 45$ V. Determine:

(a) the value of C_1;

(b) the value of V_{CC};

(c) the value of base current;

(d) the values of R_3 and R_5.

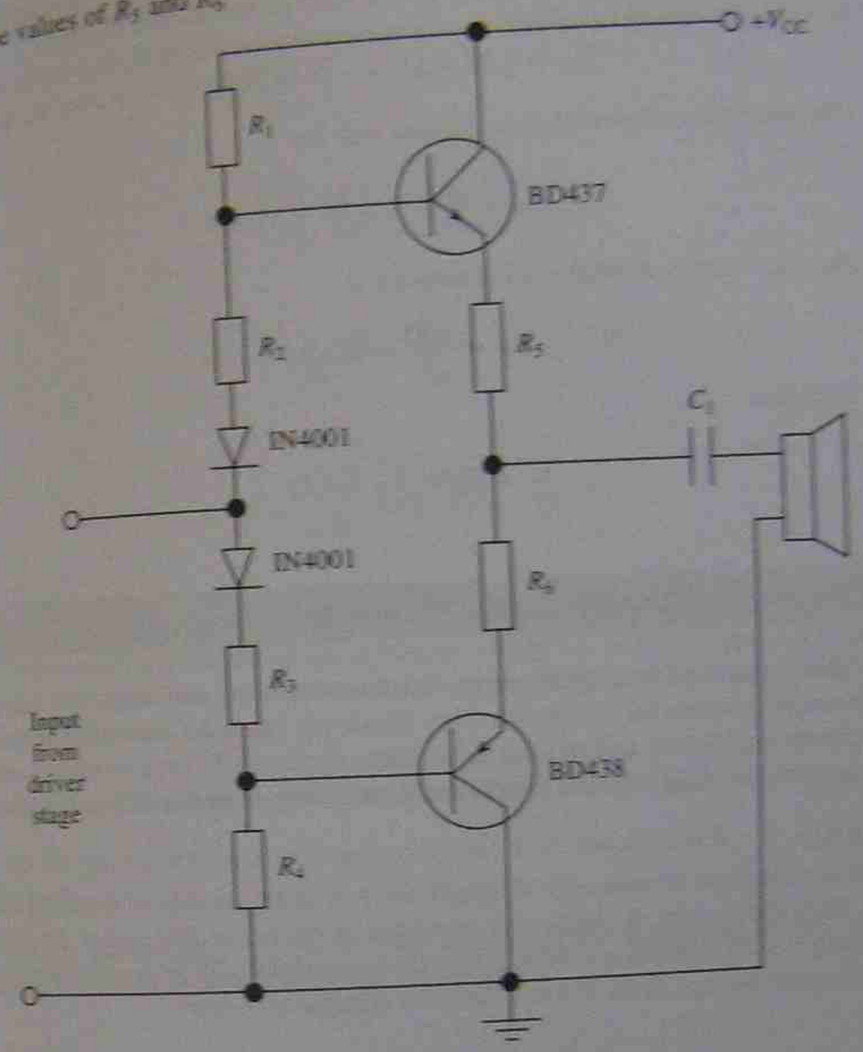


Fig. 5.22

Solution

(a)

$$f = \frac{1}{2\pi R_L C_1}$$

$$\therefore \quad C_1 = \frac{1}{2\pi f R_L} = \frac{1}{2\pi \times 80 \times 4} = 497.4 \text{ μF}$$

Select a 500 μF capacitor.

(b) The specification is for 5 W into a 4 Ω load.

$$\therefore \quad V_L = \sqrt{P_{AC(max)} \times R_L} = \sqrt{5 \times 4} = 4.47 \text{ V}$$

$$\therefore \quad V_{max} = \sqrt{2} \times \sqrt{20} = 6.32 \text{ V}$$

Also $I_{C(max)} = 6.32/4 = 1.58$ A for each transistor. According to Fig. 5.18, the quiescent voltage is half the supply voltage. Also from the data sheets (not included here) at saturation $V_{CE} = 3.2$ V. If 0.5 V is taken as the drop across R_3 and R_6, then

$$V_{CC} = 6.32 + 3.7 + \frac{V_{CC}}{2} = 20 \text{ V}$$

(c) The maximum allowable base current will be

$$I_{B(max)} = \frac{I_{C(max)}}{h_{FE}} = \frac{1.58}{40} = 39 \text{ mA}$$

(d) The d.c. current through each transistor is

$$I_{DC} = \frac{1.58}{\pi} = 0.5 \text{ A}$$

Therefore

$$R_3 = R_6 = \frac{0.5}{0.5} = 1 \Omega$$

5.7 Calculating power and efficiency

Any machine is required to convert energy into a usable form, and the power amplifier is no exception. In this case the d.c. power from the supply has to be converted to a.c. power to drive an external device, and this has to be done efficiently. Several examples are given below which should clarify the use of different configurations under different applications.

Example 5.5
An amplifier has to work with a 35 V supply and has to be capable of drawing a current of 2.5 A from the supply. A single npn transistor is biased so that under the quiescent conditions $I_C = 1.75$ A and $V_{CE} = 30$ V. Under these conditions 35 W is applied to the load when the output voltage is 18 V r.m.s. Select a suitable transistor.

Solution
From the information given we obtain

$$P_{DC} = 2.5 \times 35 = 87.5 \text{ W}$$

$$P_{AC} = 35 \text{ W}$$

$$P_{CQ} = P_{DC} - P_{AC} = 87.5 - 35 = 52.5 \text{ W}$$

$$I_{rms} = \frac{P_{AC}}{V_{rms}} = \frac{35}{18} = 1.95 \text{ A}$$

Any transistor with ratings higher than these requirements will be suitable – for example, a TIP41 with $P_{tot} = P_{C(max)} = 65$ W, $I_{CQ} = 6$ A and $V_{CEQ} = 40$ V.

Example 5.6
A single-ended transistor power amplifier takes a mean collector current of 1 A from a 12 V supply and delivers an a.c. power of 2.4 W to a transformer-coupled load. Calculate:

(a) the collector efficiency;

(b) the collector dissipation if all other losses are ignored;

(c) the turns ratio of the transformer if the output resistance of the transistor is 1.3 kΩ and the load resistance is 12 Ω.

Solution
(a)

$$P_{dc} = 12 \times 1 = 12 \text{ W}$$

(b)

$$\eta = \frac{2.4 \times 100}{12} = \frac{P_{ac}}{P_{dc}} \times 100 = 20\%$$

(c)

$$n = \sqrt{\frac{R_1}{R_2}} = \sqrt{\frac{1200}{12}} = 10:1$$

Example 5.7
A transformer push-pull amplifier has a supply voltage of 20 V. It supplies a load having a resistance of 10 Ω. The total number of turns in the primary winding is 100 and the secondary winding has 50 turns.

(a) Find the maximum power that can be delivered to the load.

(b) Find the power dissipated in each transistor when maximum power is delivered to the load.

(c) Find the power delivered to the load and the power dissipated in each transistor when transistor power dissipation is maximum.

Solution
(a) The turns ratio between each half of the primary and secondary is

$$\frac{N_1}{N_2} = 50:50$$

Hence the peak values of primary and secondary voltages are equal, as are the peak values of primary and secondary currents.

$$V_{peak} = V_{CC} = 20 \text{ V}$$

$$I_{peak} = \frac{V_{CC}}{R_1} \frac{20}{10} = 2 \text{ A}$$

Hence

$$P_{AC} = \frac{V_{peak} \times I_{peak}}{2} = \frac{20 \times 2}{2} = 20 \text{ W}$$

(b)

$$P_D = P_{DC} - P_{AC} = \frac{2I_{peak} \times I_{peak} \times V_{CC}}{\pi} - \frac{V_{peak} \times I_{peak}}{2}$$

$$= \frac{2 \times 2 \times 20}{\pi} - 20 = 5.46 \text{ W}$$

Each transistor will therefore take 2.73 W of power.

(c) Transistor power dissipation is a maximum when

$$V_{peak} = 0.636V_{CC} = 0.636 \times 20 = 12.72 \text{ V}$$

Then

$$I_{peak} = \frac{12.72}{10} = 1.272 \text{ A}$$

and

$$P_{ac} = \frac{V_{peak} \times I_{peak}}{2} = \frac{12.72 \times 1.272}{2} = 8.09 \text{ W}$$

$$P_d = \frac{2 \times I_{peak} \times V_{CC}}{\pi} - \frac{V_{peak} \times I_{peak}}{2}$$

$$= \frac{2(1.272 \times 20)}{\pi} - 8.09 = 8.09 \text{ W}$$

Hence the maximum power in each transistor is 4.05 W.

Example 5.8

In a class A transformer power amplifier, the collector current alternates between 5 mA and 115 mA and its quiescent value is 60 mA. A load of 12 Ω is connected to the secondary, and when this is referred to the primary winding it becomes 325 Ω. If the supply voltage is 25 V estimate:

(a) the transformer turns ratio;

(b) the average power output;

(c) the minimum power rating of the transistor;

(d) the efficiency of the stage.

Solution

(a) The turns ratio is given by

$$\frac{N_1}{N_2} = \frac{325}{12} = 27 : 1$$

(b)

$$P_{ac} = I_c^2 R_{eff} = \frac{(115 - 5)^2}{(2 \times 2 \times 10^3)^2} \times 325 = 0.246 \text{ W}$$

(c)

$$P_{dc} = \frac{25 \times 60}{10^3} = 1.5 \text{ W}$$

$$P_c = P_{dc} - P_{ac} = 1.5 - 0.492 = 1.008 \text{ W}$$

(d)

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{0.492}{1.5} \times 100 = 32.8\%$$

Example 5.9

A complementary pair class B push-pull amplifier has a supply voltage of 45 V and the transistors are biased so that they are sinusoidally driven to provide a current which is 80% of the maximum value. Calculate:

(a) the output power supplied to a speaker having a resistance of 15 Ω;

(b) the collector efficiency;

(c) the power rating of the transistors.

Solution

(a) The output power is given by

$$\frac{V_{CC} \times I_{C(max)}}{4} = \frac{V_{CC}^2}{8R_L}$$

Hence

$$I_{C(max)} = \frac{V_{CC}}{2R_L} = \frac{45}{30} = 1.5 \text{ A}$$

Biasing gives 80% swing, so

$$I_{C(max)} = 0.8 \times 1.5 = 1.2 \text{ A}$$

Hence output power is

$$\frac{V_{CC} \times I_{C(max)}}{4} = \frac{45 \times 1.2}{4} = 13.5 \text{ W}$$

(b)

$$P_{dc} = \frac{I_{C(max)} V_{CC}}{\pi} = \frac{1.2 \times 45}{\pi} = 17.2 \text{ W}$$

$$\eta = \frac{13.5}{17.2} \times 100 = 78.5\%$$

(c) The maximum output power is given by

$$P_{(max)} = \frac{V_{CC}^2}{8R_L} = \frac{(45)^2}{8 \times 15} = 16.9 \text{ W}$$

The maximum collector power dissipation is given approximately by $0.4P_{max}$:

$$P_{C(max)} = 0.4 \times 16.9 = 6.8 \text{ W}$$

Therefore power rating of each transistor is 3.4 W.

Example 5.10
An amplifier has to work with a 38 V supply and draw a current of 2 A from the d.c. supply. A single npn transistor is biased so that under quiescent conditions $I_C = 1.64$ A, $V_{CE} = 25$ V. This delivers 35 W into its load when the output voltage is 20 V r.m.s. Select a suitable transistor.

Solution
The steps involved in this type of practical problem are given below

$$P_{dc} = I_C \times V_{CC} = 2 \times 38 = 76 \text{ W}.$$

$$P_{ac} = 35 \text{ W}$$

The quiescent power is given by

$$P_{CQ} = I_{CQ} \times V_{CQ} = P_{dc} - P_{ac} = 41 \text{ W}$$

So

$$I_{C(max)} = \frac{P_{ac}}{V_{o(rms)}} = \frac{35}{20} = 1.75 \text{ A}$$

Hence any transistor with ratings higher than these requirements will be suitable. A TIP41 is a suitable choice as it has the following characteristics:

$$P_{tot} = P_{C(max)} = 65 \text{ W}$$

$$I_{CQ} = 6 \text{ A}$$

$$V_{CEQ} = 40 \text{ V}$$

$$P_{CQ} = 1.64 \times 25 = 41 \text{ W}$$

5.8 Integrated circuit power amplifiers

Modern chip technology has promoted the fabrication of almost every discrete circuit on to a silicon substrate, and power amplifiers are no exception. All the circuits so far discussed can be etched on to a chip, except inductors and to a certain extent pnp transistors. Where there is a high current and power demand, discrete components still have the edge, and it is possibly this reason which restricts the availability and choice of integrated circuit power amplifiers. There are many power amplifiers on the market but it is a matter of deciding the requirements and parameters, then selecting the most suitable chip.

The integrated circuits discussed in this section are the LM380 (National Semiconductor), TBA820 (SGS–Thomson), TDA2030 (SGS–Thomson) and TDA2006 (SGS–Thomson). Details of characteristics and applications of the TDA 2006 will be found at the end of this chapter; those of the others can be found in appropriate manufacturers' data sheets.

LM380

This is a 14-pin dual in-line package that requires very few external components to make a 2.5 W power amplifier feeding into an 8 Ω load. Typical parameters for this integrated circuit are:

Fixed loop gain	50 (34 dB)
Supply voltage range	8–22 V
Quiescent current	7 mA
Input sensitivity	150 mV r.m.s.
Input resistance	150 kΩ
Load resistance	8 Ω
Bandwidth	100 kHz
Maximum current	1.3 A

The pinout diagram is shown in Fig. 5.23.

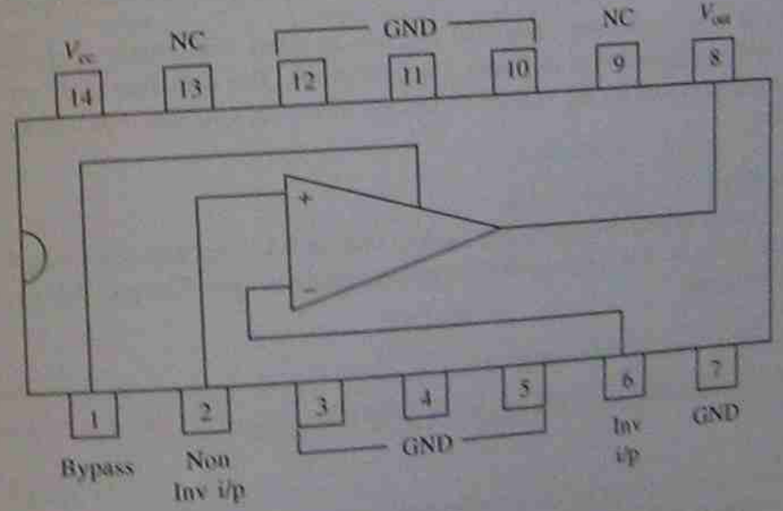


Fig. 5.23

The following points should be noted concerning the connection of this chip:

1. The output signal is automatically centred at half the supply voltage.
2. Pins 3, 4, 5, 10, 11 and 12 should be connected to ground and a heat sink connected directly to the pins for cooling.
3. The amplifier is suitable for low-power audio applications, but when used with a battery the current drain can be excessive.
4. In most applications it is advisable to add a 2.7 Ω resistor and a 0.1 μF polyester

capacitor in series from pin 8 to ground. A 4.7 μF capacitor connected from pin 1 to ground is also recommended.

5. The power-handling capabilities can be increased if a bridge system is used. It is then possible to feed into a 5 W load.

TBA 820M

This is an 8-pin amplifier capable of delivering 2 W into an 8 Ω load, 1.6 W into a 4 Ω load or 1.2 W into an 8 Ω load. A bootstrap circuit is included in order to increase the gain of the amplifier, and high ripple rejection from the power supply is a major feature. This is achieved by including a 47 μF capacitor when required.

Frequency compensation is provided by pin 1. The value of C_B (from the data sheets) is selected with R_f, the gain setting resistor, by using the C_B/R_f graph. Selection of these components will also affect the frequency response, as can be seen from the electrical characteristics.

TDA2006

This chip is identical to the TDA2030 and can be used with single or double power supplies and in single-ended or bridge configurations. The data sheets are set out in a similar manner to those for the TDA2030, and the following example indicates a particular application.

Example 5.11

Design an audio amplifier suitable for feeding into an 8 Ω load and delivering 8 W. The bandwidth has to be 20 kHz and a double power supply is used. The gain has to be set at 30 dB. Determine:

(a) suitable values for components;

(b) the expected efficiency if a supply of ± 12 V is used.

Solution

(a) Suitable values can be achieved from the data sheet applications graph. As the bandwidth has to be 20 kHz and a bandwidth gain of 30 dB is required, the value of C_8 is 250 pF. Also

$$C_8 = \frac{1}{2\pi BWR_1}$$

$$\therefore \quad R_1 = \frac{1}{2\pi BWC_8} = \frac{10^{12}}{2\pi \times 2 \times 10^4 \times 250} = 31.9\ \text{k}\Omega$$

This will give the larger gain of 30 dB.

(b) From the data sheets and for a load of 8 Ω and $V = \pm 12$ V, the power dissipation (P_c) is approximately 4.6 W.

$$P_{dc} = P_c + P_{ac} = 4.8 + 8 = 12.8\ \text{W}$$

$$\therefore \quad \eta = \frac{8}{12.8} \times 100 = 62.5\%$$

Note that decreasing the supply voltage would increase the efficiency while decreasing P_{ac} and P_c. Sensitivity will also decrease.

5.9 Radio frequency power amplifiers

These amplifiers normally function under class C bias conditions and are required as conventional amplifiers to boost the final power from the transmitter to the aerial tuning unit and antenna. They are also used as frequency amplifier stages in situations where the carrier frequency is insufficiently high. Two applications where this type of amplifier is used are given in Figs 5.24 and 5.25.

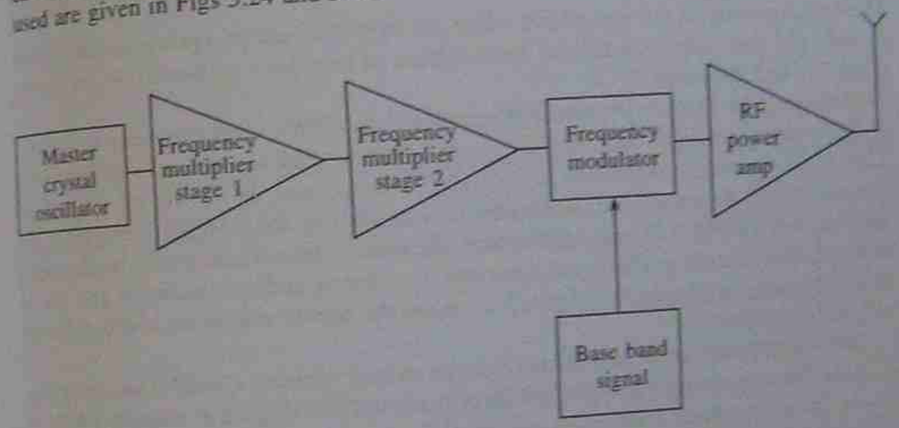


Fig. 5.24

Figure 5.24 shows a simplified block diagram of an FM receiver with frequency multiplication and radio frequency power boosting. The frequency multiplication is necessary

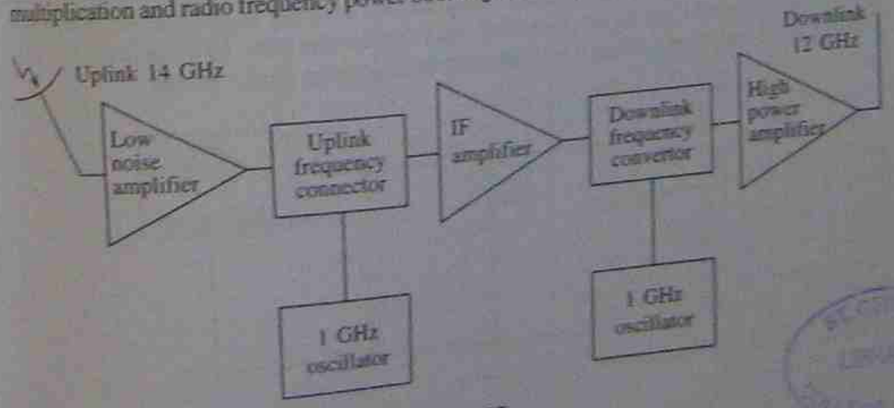


Fig. 5.25

because there is a limit to how thin the crystal in the oscillator can be cut: the thinner the crystal, the higher the frequency. Hence several stages of frequency multiplication are required operating with class C classic bias and having their loads tuned to some harmonic of the crystal oscillator.

Figure 5.25 shows a satellite transponder used for an uplink/downlink of 14/12 GHz. A high-power amplifier is required to accommodate the spectral power used over several channels. The amplifier used here is a microwave type and is highly specialized.

Radio frequency power amplifiers are numerous, and the topic is beyond the scope of this text. However, it is informative to look at one particular versatile chip, the MAX2430 manufactured by Maxim Integrated Products. The data sheets for this chip can be obtained from the manufacturer.

5.10 Power amplifier measurements

There are a number of test procedures which can be carried out on a power amplifier, but perhaps the most important are the measurement of frequency response, output power efficiency and distortion.

Measuring the frequency response for a power amplifier is similar to other amplifiers in that a signal generator and oscilloscope or voltmeter can be used, as shown in Fig. 5.26. A two-channel oscilloscope is generally preferred and, as shown, all instrument grounds should be commoned. Integrated circuits such as the LM380, a response for which is shown in Fig. 5.27, may have several unconnected pins. These should be grounded to avoid signal coupling. The signal generator is set for an undistorted output and swept through a range of frequencies. Figure 5.27 shows the half-power points, the bandwidth and mid-band gain.

The output power can be determined for a given load by using a similar set-up to Fig. 5.26. In this measurement an audio oscillator is set at a test frequency, usually 1 kHz or lower. The input voltage is increased until some distortion is seen in the output waveform. The voltage is then measured by means of a voltmeter and the r.m.s. power calculated. Generally this will be done for a fixed resistance such as the 8 Ω speaker in Fig. 5.27. The output power can also be measured by means of an audio power meter, but these can be expensive and are not necessary in most applications. In order to measure the efficiency the d.c. input power has to be calculated, and this can be done by measuring the d.c. current from the supply when it is delivering its maximum output power.

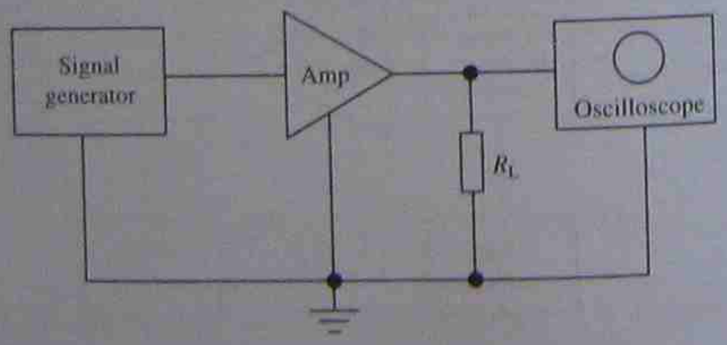
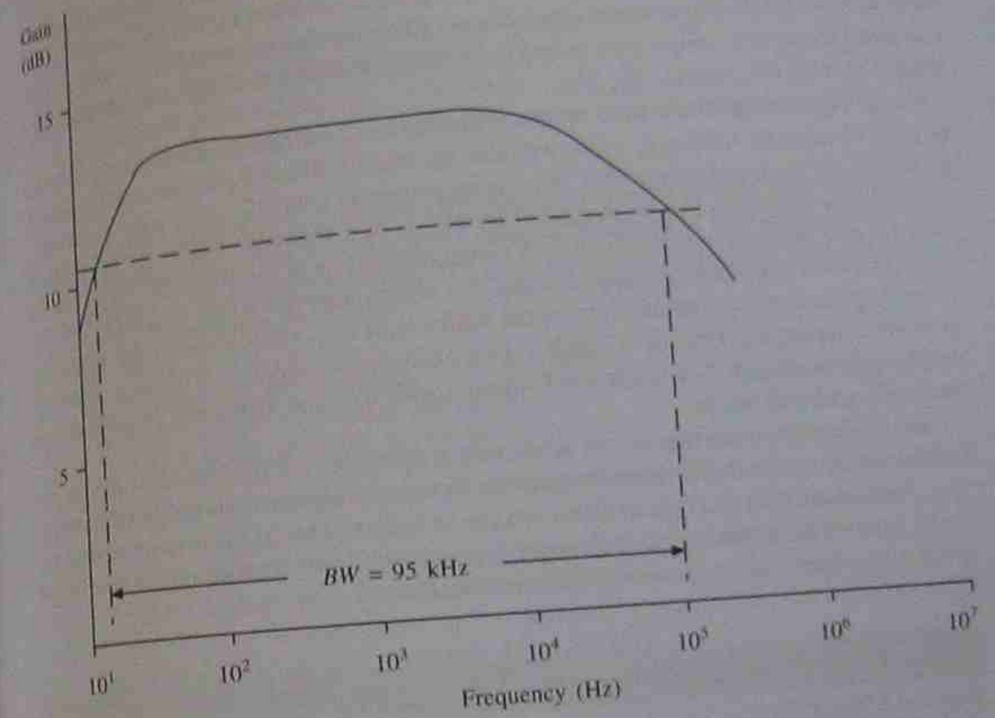
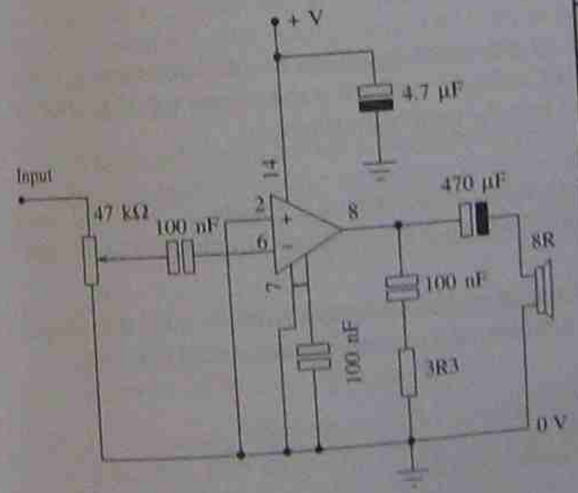


Fig. 5.26





f(Hz)	V_i(V)	V_o(V)	V_i/V_o	dB
0.3		1	3.3	10.5
20	0.3	1.1	3.6	11.3
40	0.3	1.38	4.6	13.2
50	0.3	1.4	4.7	13.3
60	0.3	1.4	4.7	13.4
80	0.3	1.4	4.7	13.4
100	0.3	1.4	4.7	13.4
200	0.3	1.4	4.7	13.4
300	0.3	1.4	4.7	13.4
400	0.3	1.4	4.7	13.4
500	0.3	1.4	4.7	13.4
1000	0.3	1.4	4.7	13.4
3000	0.3	1.4	4.7	13.4
10000	0.3	1.4	4.7	13.4
15000	0.27	1.2	4.6	13.1
20000	0.27	1.19	4.4	13
30000	0.27	1.18	4.2	12.9
50000	0.05	0.2	3.54	11
100000	0.05	0.15	3	9.54

Fig. 5.27

The final test considered here is for harmonic and intermodulation distortion, which is generally expressed as a percentage or so many decibels down on the fundamental (f_1). BJTs and FETs all show some non-linearity in their characteristics, and this causes unwanted frequency components to appear at the output. Generally they are harmonically related to the fundamental ($2f_1$, $3f_1$).

Large signal amplifiers, such as power amplifiers, can have their distorted outputs reduced by negative feedback, which will alter the input and output resistance of the circuit as well as the gain and bandwidth, but a compromise is generally built into the design.

Harmonic distortion can be measured by means of a specturm analyser or distortion meter. A new innovation is the Tektronix power measurement oscilloscope which can be used for power measurement applications, but which also has a bar graph facility for measuring harmonics. Another convenient addition to the oscilloscope is the spectrum analyser adaptor by Thurlby Thander. This instrument operates with any standard oscilloscope having an X-Y mode and features a wide dynamic range and variable centre frequency and scan width.

Intermodulation distortion occurs when new frequencies are introduced at the output which contain sum and difference frequencies from input signals such as $2f_1 + 2f_2$ or $f_3 + 2f_2$. A measurement of this type of distortion can be achieved by applying two frequencies to the input of an amplifier and then observing any additional components at the output using a spectrum analyser or intermodulation analyser.

5.11 Further problems

1. An amplifier has a dc. input power of 4 W and an efficiency of 28%. Calculate its collector dissipation.
   Answer: 2.88 W
2. When a signal is applied to a single-ended amplifier its collector current varies from 28 mA to 225 mA and its collector voltage varies from 1.8 V to 14.8 V. Calculate the a.c. power output and the collector efficiency.
   Answer: 325 mW, 31.13%
3. A complementary symmetry pair audio amplifier has a supply of 30 V and feeds into a load of 16 Ω. Calculate the maximum possible power delivered to the load.
   Answer: 7.03 W
4. Under operating conditions an amplifier draws 800 mA from its 10 V d.c. supply. If 6 W of audio output power is delivered to a loudspeaker, calculate:
   (a) the d.c. power;
   (b) the collector power dissipation;
   (c) the efficiency of the amplifier.
   Assume a single-ended type of audio amplifier.
   Answer: 8 W, 2 W, 75%
5. A class C transistor tuned power amplifier operates from a 30 V collector supply. If the collector dissipation of the transistor is 1.2 W and the mean collector current is 0.1 A, determine:
   (a) the a.c. output power;
   (b) the collector efficiency of the amplifier.
   Answer: 1.8 W, 60%

6. A transducer class C amplifier tuned to 500 kHz uses a coil of inductance 3.5 μH. The effective Q of the circuit is 25. A mean current of 0.12 A is taken from the 50 V collector supply and the collector voltage has a peak value of 47 V. Calculate:
   (a) the efficiency of the amplifier;
   (b) the collector dissipation;
   (c) the peak amplitude of the 500 kHz component of collector current pulses.
   Answer: 66.7%, 2 W, 1711 mA
7. In a class A transformer-coupled amplifier, the collector current alternates between 3 mA and 100 mA and its quiescent value is 58 mA. The load is 12 Ω and, when referred to the primary winding, 315 Ω. If the supply voltage is 20 V, estimate:
   (a) the transformer turns ratio;
   (b) the a.c. power output;
   (c) the minimum power rating of the transistor;
   (d) the d.c. power supplied to the circuit.
   Answer: 5, 0.465 W, 0.695 W, 1.6 W
8. A complementary push-pull amplifier has a supply voltage of 20 V and delivers power to a 10 Ω load. Determine.
   (a) the power delivered to the load under maximum signal conditions;
   (b) the efficiency under maximum signal conditions;
   (c) the value of the capacitor which couples the signal to the load if the amplifier has to be used at signal frequencies down to 20 Hz.
   Answer: 5 W, 78.5% 795 μF
9. A single-ended power amplifier has a supply voltage $V_{CC} = 20$ V and a collector resistance of $R_C = 1$ Ω. Determine:
   (a) the maximum power dissipation rating that the transistor should have;
   (b) the value of R_C which should be used to ensure safe operation if an increase of temperature reduces the maximum rating found in (a) by half.
   Answer: 0.1 W, 2 kW
10. A push-pull amplifier has a supply voltage $V_{CC} = 20$ V and supplies a load of 10 Ω. The primary/secondary turns ratio is 100 : 50. Determine:
    (a) the maximum power that can be delivered to the load;
    (b) the power dissipated in each transistor when maximum power is delivered to the load;
    (c) the power delivered to the load and the power dissipated in each transistor when the transistor power dissipated is maximum.
    Answer: 20 W, 2.73 W, 4.05 W)
11. Design an audio power amplifier using a TDA2030 chip which has to deliver 14 W/ 8 Ω. The gain has to be 30 dB and the pass band from 20 Hz to 30 kHz. (See Example 5.12.)
12. Design an audio amplifier using a TBA820M chip which has to deliver a maximum of 1 W into an 8 Ω load when the bandwidth is from 20 Hz to 25 kHz. (See Example 5.11.)
13. A 24 W audio amplifier has to be built to feed into a load of 8 Ω. Select a chip which might satisfy this requirement and suggest what practical considerations should be

applied to the circuit if short-circuit protection and thermal shut down have to be applied. The voltage gain has to be 30 dB and the bandwidth from 20 Hz to 25 kHz.

14. Design an RF power amplifier suitable for a cellular phone operating at 915 MHz. State all the practical considerations when fabricating the printed circuit board.
15. An LM380 has to deliver 2 W to an 8 Ω load. The voltage gain has to be set at 33 dB. Explain the function of each component and what dimensions the heatsink should be.

Data sheets

SGS-THOMSON MICROELECTRONICS

TBA820M

1.2W AUDIO AMPLIFIER

DESCRIPTION

The TBA820M is a monolithic integrated audio amplifier in a 8 lead dual in-line plastic package. It is intended for use as low frequency class B power amplifier with wide range of supply voltage: 3 to 16V, in portable radios, cassette recorders and players etc. Main features are: minimum working supply voltage of 3V, low quiescent current, low number of external components, good ripple rejection, no cross-over distortion, low power dissipation.

Output power: P_o = 2W at 12V/8Ω, 1.6W at 9V/4Ω and 1.2W at 9V/8Ω.



Minidip

ORDERING NUMBER: TBA820M

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply voltage	16	V
I_o	Output peak current	1.5	A
P_{tot}	Power dissipation at T_{amb} = 60°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

TEST AND APPLICATION CIRCUITS

Figure 1. Circuit diagram with load connected to the supply voltage

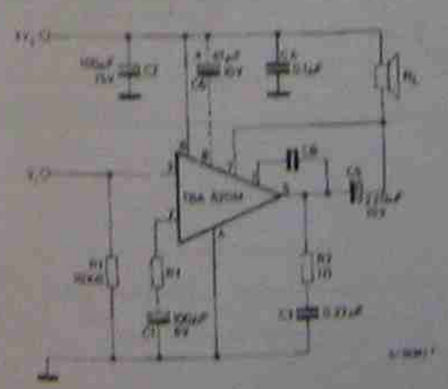
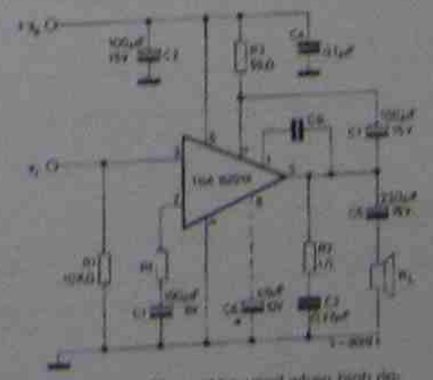


Figure 2. Circuit diagram with load connected to ground



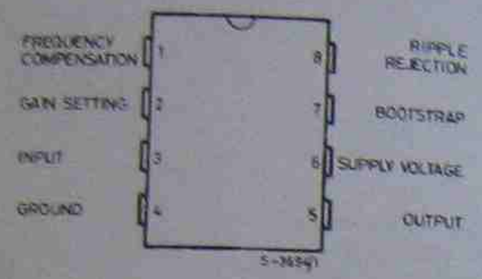
* Capacitor C6 must be used when high ripple rejection is requested.

June 1988

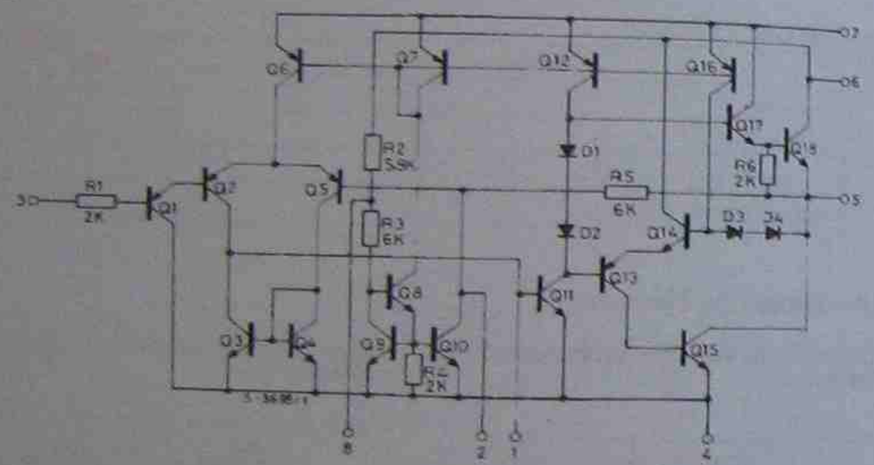
This is known as STMicroelectronics

TBA820M

PIN CONNECTION (top view)



SCHEMATIC DIAGRAM



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	100	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuits V_S = 9V, T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_S	Supply voltage			3		16	V
V_o	Quiescent output voltage (pin 5)			4	4.5	5	V
I_d	Quiescent drain current				4	12	mA
I_b	Bias current (pin 3)				0.1		µA
P_o	Output power	d = 10% f = 1 kHz R_f = 120Ω V_S = 12V V_S = 9V V_S = 9V V_S = 6V V_S = 3.5V	R_L = 8Ω R_L = 4Ω R_L = 8Ω R_L = 4Ω R_L = 4Ω	0.9	2 1.6 1.2 0.75 0.25		W W W W W
R_i	Input resistance (pin 3)	f = 1 kHz			5		MΩ
B	Frequency response (-3 dB)	R_L = 8Ω C_S = 1000 µF R_f = 120Ω	C_B = 680 pF	25 to 7,000			Hz
			C_B = 220 pF	25 to 20,000			
d	Distortion	P_o = 500 mW R_L = 8Ω f = 1 kHz	R_f = 33Ω		0.8		%
			R_f = 120Ω		0.4		
G_v	Voltage gain (open loop)	f = 1 kHz	R_L = 8Ω		75		dB
G_v	Voltage gain (closed loop)	R_L = 8Ω	R_f = 33Ω		45		dB
		f = 1 kHz	R_f = 120Ω		34		
e_N	Input noise voltage (*)				3		µV
i_N	Input noise current (*)				0.4		nA
$\frac{S+N}{N}$	Signal to noise ratio (*)	P_o = 1.2W R_L = 8Ω G_v = 34 dB	R1 = 10KΩ		80		dB
			R1 = 50 kΩ		70		
SVR	Supply voltage rejection (test circuit of fig. 2)	R_L = 8Ω $f_{(ripple)}$ = 100 Hz C6 = 47 µF R_f = 120Ω			42		dB

(*) B = 22 Hz to 22 KHz

Figure 3. Output power vs. supply voltage

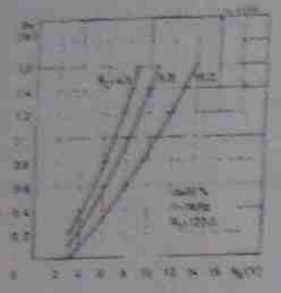


Figure 4. Harmonic distortion vs. output power

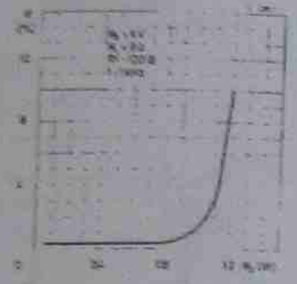


Figure 5. Power dissipation and efficiency vs. output power

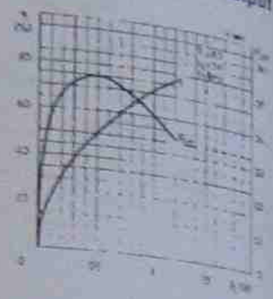


Figure 6. Maximum power dissipation (sine wave operation)

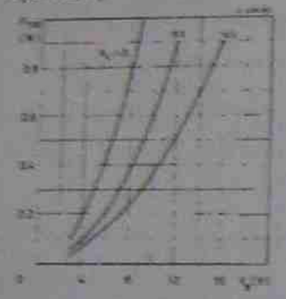


Figure 7. Suggested value of C_B vs. R_i

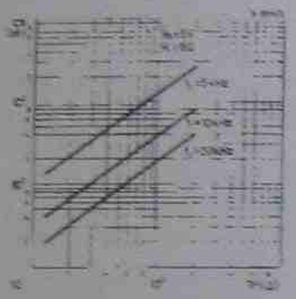


Figure 8. Frequency response

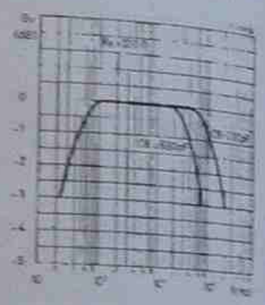


Figure 9. Harmonic distortion vs. frequency

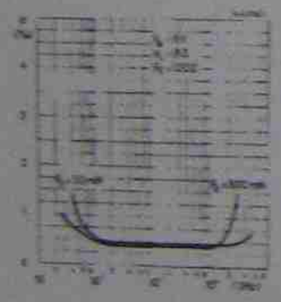


Figure 10. Supply voltage rejection (Fig. 2 circuit)

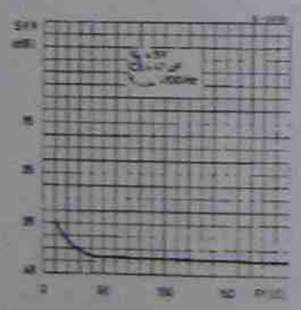
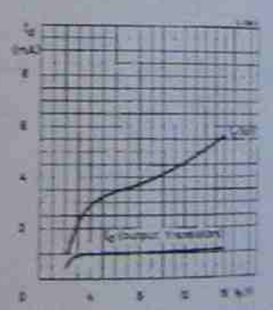
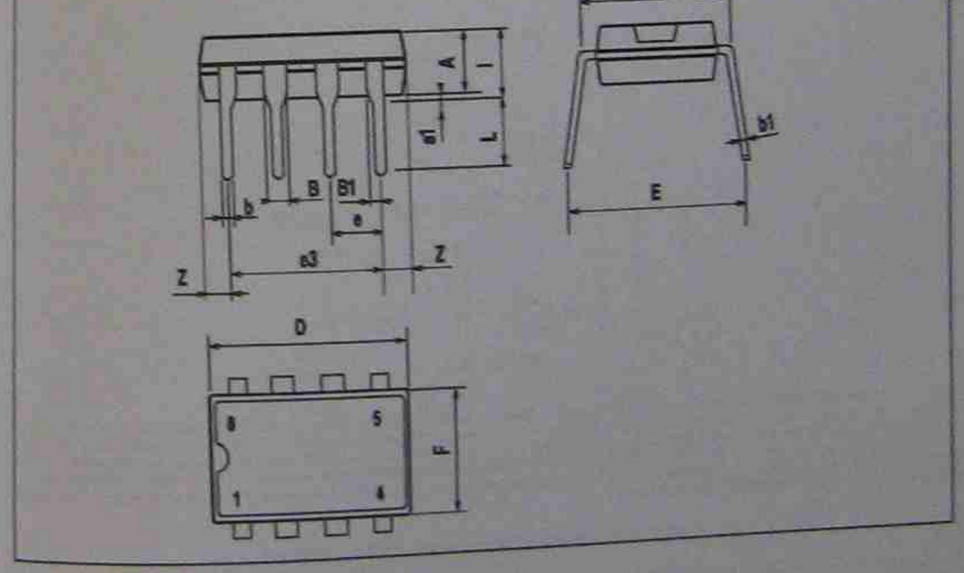


Figure 11. Quiescent current vs. supply voltage



MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



TBA820M

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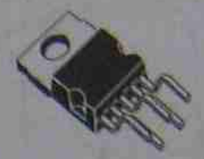
SGS-THOMSON* MICROELECTRONICS

TDA2006

12W AUDIO AMPLIFIER

DESCRIPTION

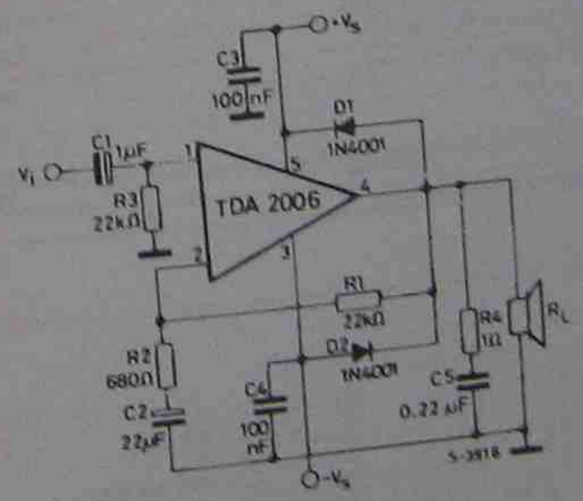
The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ±12V, d = 10 % typically it provides 12W output power on a 4Ω load and 8W on a 8Ω . The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.



PENTAWATT

ORDERING NUMBERS : TDA2006V
TDA2006H

TYPICAL APPLICATION CIRCUIT



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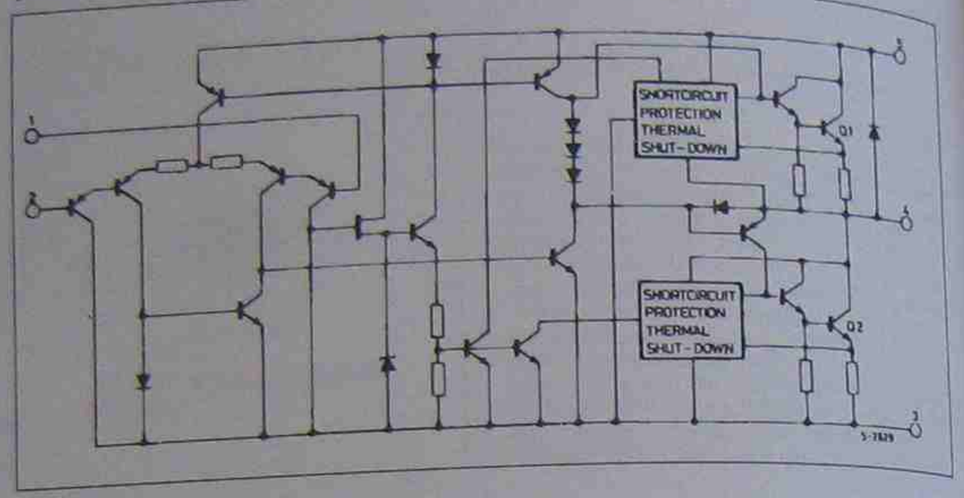
May 1995

*Now known as STMicroelectronics

TDA2006

SCHEMATIC DIAGRAM



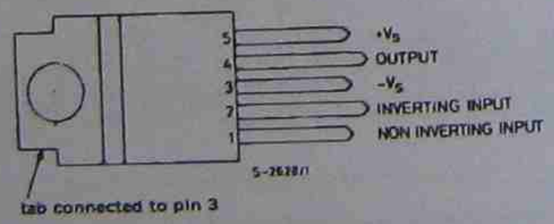
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 12	V
I_o	Output Peak Current (internaly limited)	3	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN CONNECTION



ELECTRICAL CHARACTERISTICS

(refer to the test circuit ; V_S = ± 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 15	V
I_d	Quiescent Drain Current	V_s = ± 15V		40	80	mA
I_b	Input Bias Current	V_s = ± 15V		0.2	3	µA
V_{os}	Input Offset Voltage	V_s = ± 15V		± 8		mV
I_{os}	Input Offset Current	V_s = ± 15V		± 80		nA
V_{os}	Output Offset Voltage	V_s = ± 15V		± 10	± 100	mV
P_o	Output Power	d = 10%, f = 1kHz R_L = 4Ω R_L = 8Ω	6	12 8		W
d	Distortion	P_o = 0.1 to 8W, R_L = 4Ω, f = 1kHz P_o = 0.1 to 4W, R_L = 8Ω, f = 1kHz		0.2 0.1		% %
V_i	Input Sensitivity	P_o = 10W, R_L = 4Ω, f = 1kHz P_o = 6W, R_L = 8Ω, f = 1kHz		200 220		mV mV
B	Frequency Response (– 3dB)	P_o = 8W, R_L = 4Ω	20Hz to 100kHz			
R_i	Input Resistance (pin 1)	f = 1kHz	0.5	5		MΩ
G_v	Voltage Gain (open loop)	f = 1kHz		75		dB
G_v	Voltage Gain (closed loop)	f = 1kHz	29.5	30	30.5	dB
e_N	Input Noise Voltage	B (– 3dB) = 22Hz to 22kHz, R_L = 4Ω		3	10	µV
i_N	Input Noise Current	B (– 3dB) = 22Hz to 22kHz, R_L = 4Ω		80	200	pA
SVR	Supply Voltage Rejection	R_L = 4Ω; R_g = 22kΩ, f_{ripple} = 100Hz (*)	40	50		dB
I_d	Drain Current	P_o = 12W, R_L = 4Ω P_o = 8W, R_L = 8Ω		850 500		mA mA
T_j	Thermal Shutdown Junction Temperature				145	°C

(*) Referring to Figure 15, single supply.

Figure 1 : Output Power versus Supply Voltage

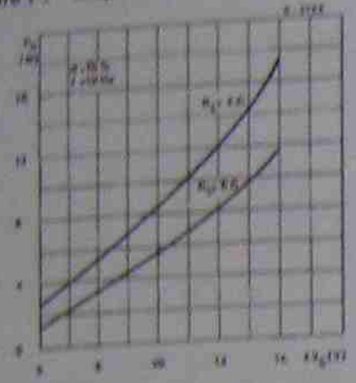


Figure 2 : Distortion versus Output Power

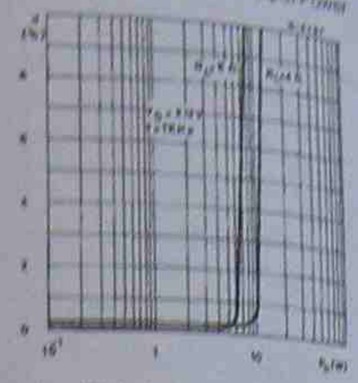


Figure 3 : Distortion versus Frequency

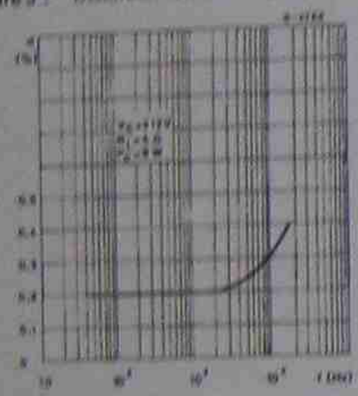


Figure 4 : Distortion versus Frequency

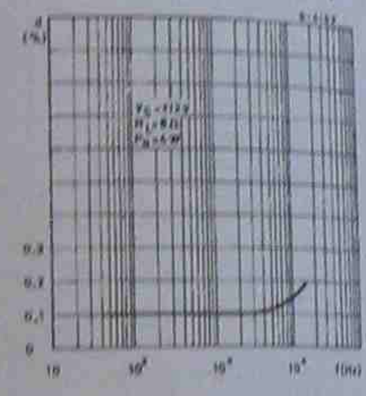


Figure 5 : Sensitivity versus Output Power

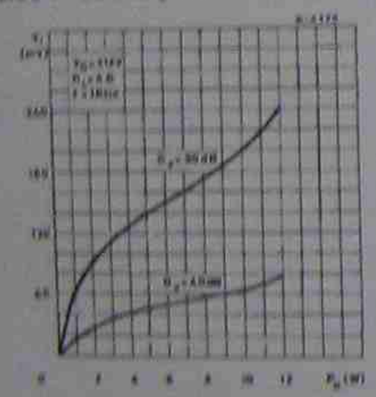


Figure 6 : Sensitivity versus Output Power

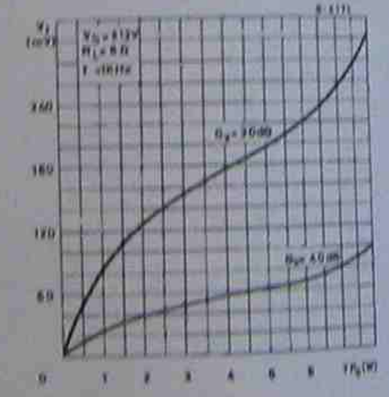


Figure 7 : Frequency Response with different values of the rolloff Capacitor C8 (see Figure 13)

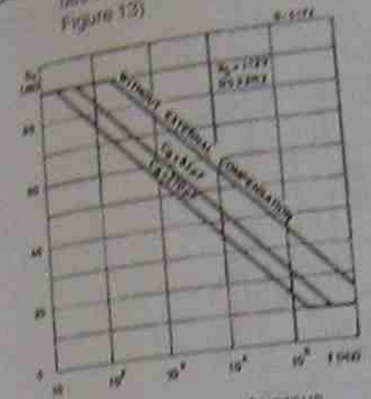


Figure 8 : Value of C8 versus Voltage Gain for different Bandwidths (see Figure 13)

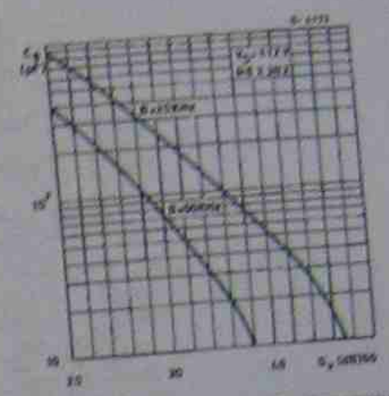


Figure 9 : Quiescent Current versus Supply Voltage

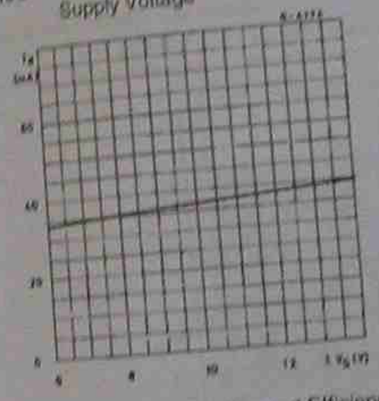


Figure 10 : Supply Voltage Rejection versus Voltage Gain

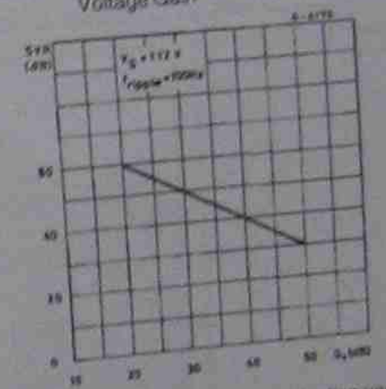


Figure 11 : Power Dissipation and Efficiency versus Output Power

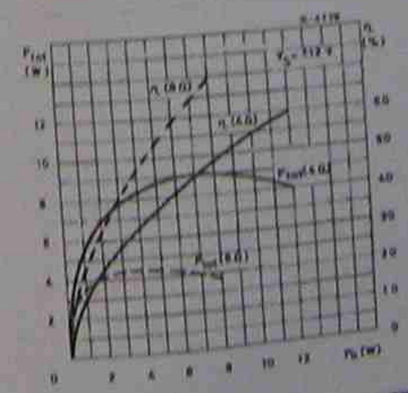


Figure 12 : Maximum Power Dissipation versus Supply Voltage (sine wave operation)

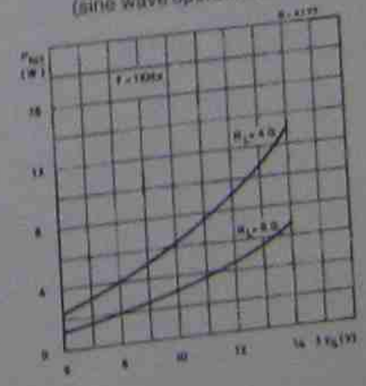


Figure 13 : Application Circuit with Spilt Power Supply

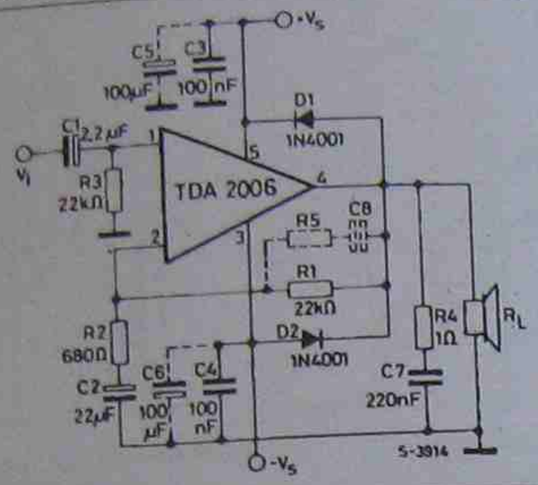


Figure 14 : P.C. Board and Components Layout of the Circuit of Figure 13 (1:1 scale)

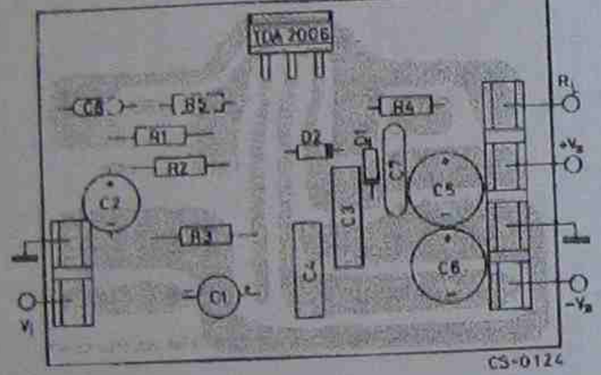


Figure 15 : Application Circuit with Single Power Supply

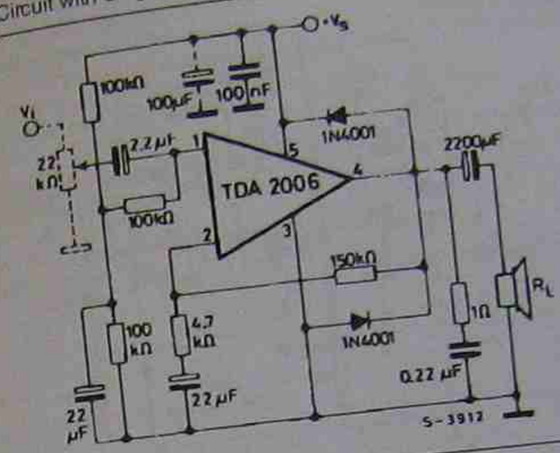


Figure 16 : P.C. Board and Components Layout of the Circuit of Figure 15 (1:1 scale)

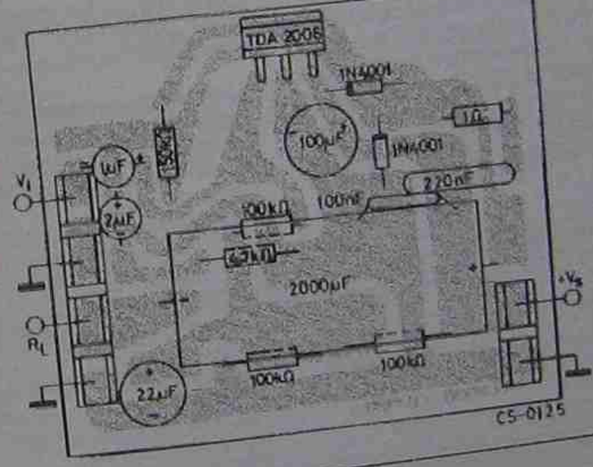
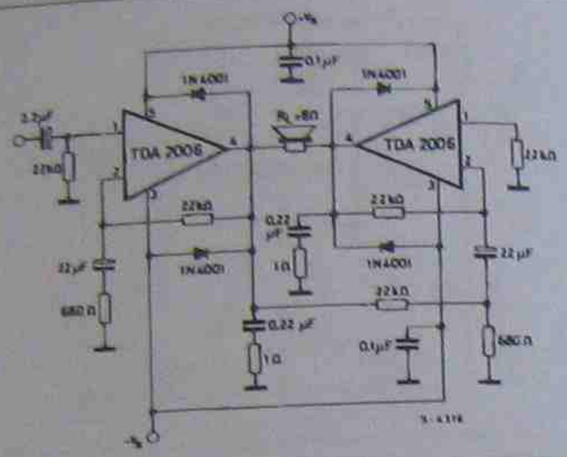


Figure 17 : Bridge Amplifier Configuration with Split Power Supply (P_O = 24W, V_S = ± 12V)



PRACTICAL CONSIDERATIONS

Printed Circuit Board

The layout shown in Figure 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly Suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application Suggestion

The recommended values of the components are the ones shown on application circuits of Figure 13. Different values can be used. The table 1 can help the designers.

Table 1

Component	Recommanded Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value
R_1	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)
R_2	680 Ω	Closed Loop Gain Setting	Decrease of Gain (*)	Increase of Gain
R_3	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance
R_4	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads	
R_5	$3R_2$	Upper Frequency Cut-off	Poor High Frequencies Attenuation	Danger of Oscillation
C_1	2.2 µF	Input DC Decoupling		Increase of Low Frequencies Cut-off
C_2	22 µF	Inverting Input DC Decoupling		Increase of Low Frequencies Cut-off
C_3C_4	0.1 µF	Supply Voltage by Pass		Danger of Oscillation
C_5C_6	100 µF	Supply Voltage by Pass		Danger of Oscillation
C_7	0.22 µF	Frequency Stability		Danger of Oscillation
C_8	$\frac{1}{2\pi BR_1}$	Upper Frequency Cut-off	Lower Bandwidth	Larger Bandwidth
D_1D_2	1N4001	To Protect the Device Against Output Voltage Spikes.		

(*) Closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Figure 18 shows that the maximum output current is a function of the collector emitter voltage ; hence the output transistors work within their safe operating area (Figure 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) an overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; Figure 22 shows the dissipable power as a function of ambient temperature for different thermal resistances.

Figure 18 : Maximum Output Current versus Voltage $V_{CE\,(sat)}$ accross each Output Transistor

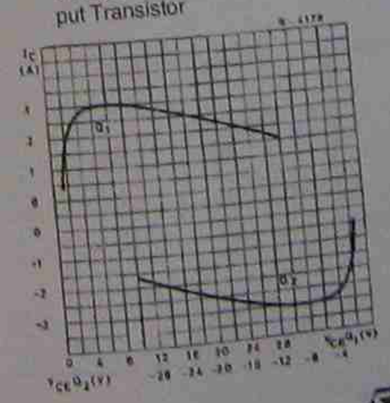


Figure 19 : Safe Operating Area and Collector Characteristics of the Protected Power Transistor

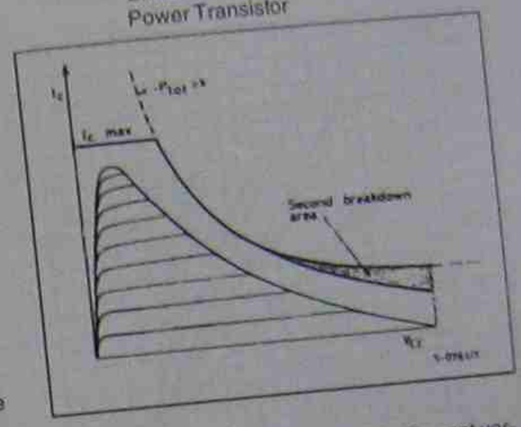


Figure 20 : Output Power and Drain Current versus Case Temperature (R_L = 4Ω)

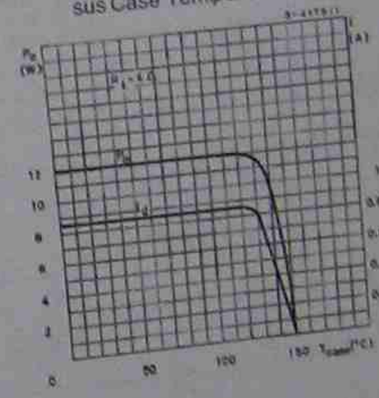


Figure 21 : Output Power and Drain Current versus Case Temperature (R_L = 8Ω)

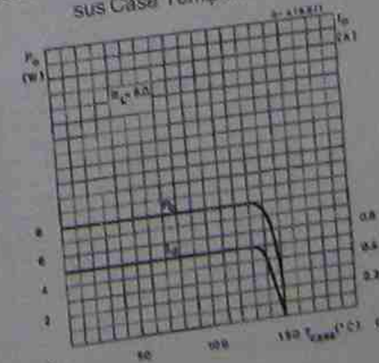
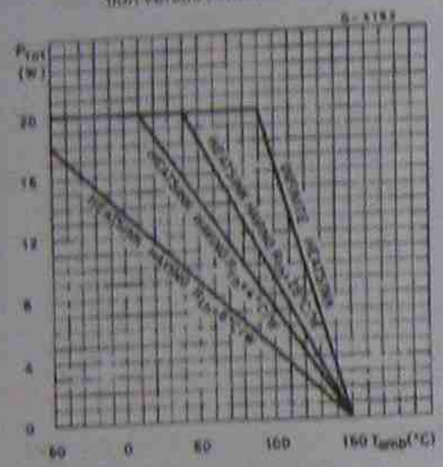


Figure 22 : Maximum Allowable Power Dissipation versus Ambient Temperature

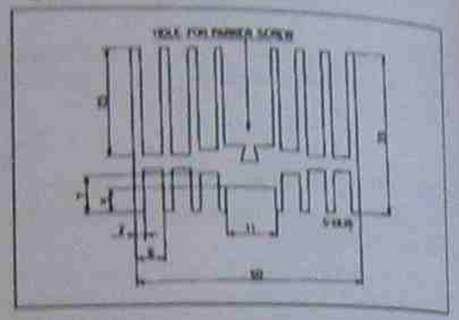


DIMENSION SUGGESTION

The following table shows the length of the heatsink in Figure 23 for several values of P_{tot} and R_{th}

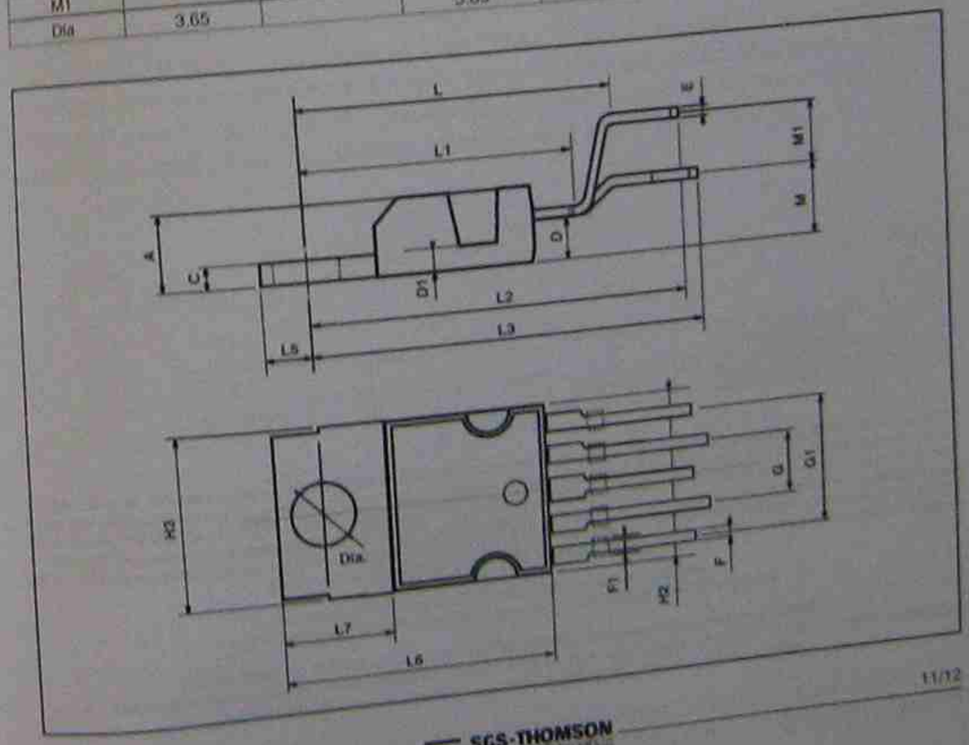
P_{tot} (W)	12	8	6
Lenght of Heatsink (mm)	60	40	30
R_{th} of Heatsink (°C/W)	4.2	6.2	8.3

Figure 23 : Example of Heatsink



PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152



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6

Phase-locked loops and synthesizers

6.1 Introduction

Figure 6.1 shows a receiver suitable for detecting signals from fast moving objects where the signal-to-noise ratio is low. The phase detector, amplifier and voltage-controlled oscillator (VCO) form a phase-locked loop (PLL) which is capable of locking on to an incoming carrier and maintaining this lock when the tracking varies. This system is really a feedback loop forming part of a closed-loop control system, and the overall gain is simply the product of all the separate gains for each block in the system.

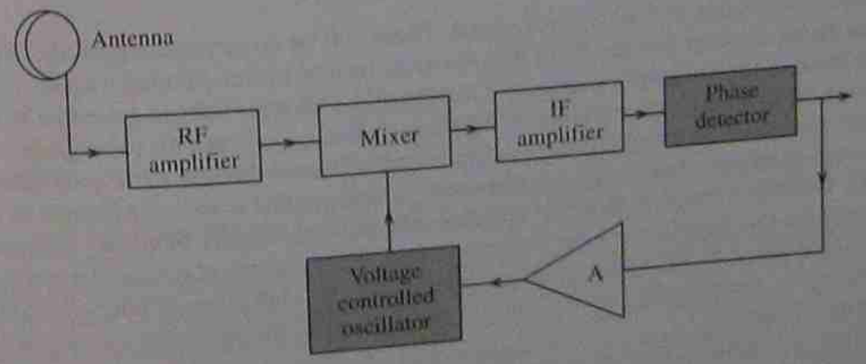


Fig. 6.1

There are many applications for this type of system such as synchronous detection of AM signals, FM modulation, frequency multiplication, automatic frequency control of the television horizontal amplifier and frequency shift keying decoders.

6.2 Operational considerations

A PLL is a form of servo system which consists of a phase detector, low-pass filter and VCO. The phase detector compares the phase of the VCO with the incoming reference signal, giving an output proportional to the difference in phase. This is then filtered to remove unwanted high-frequency components, and the output from the low-pass filter is used to control the frequency of the VCO, locking it to the incoming signal.

It should be noted that phase is the integral of frequency, and there is only a difference in frequency between two signals when the phase is changing between them. When the VCO signal is locked to an incoming reference a steady d.c. error voltage is applied to the VCO, and this is proportional to a constant phase difference between the two signals. Hence there is no actual phase change and the frequency of the VCO must be exactly the same as the reference.

Consider Fig. 6.2. This is a fundamental PLL block diagram which can be assembled discretely or on an integrated chip. It shows what is called a filter tracking circuit.

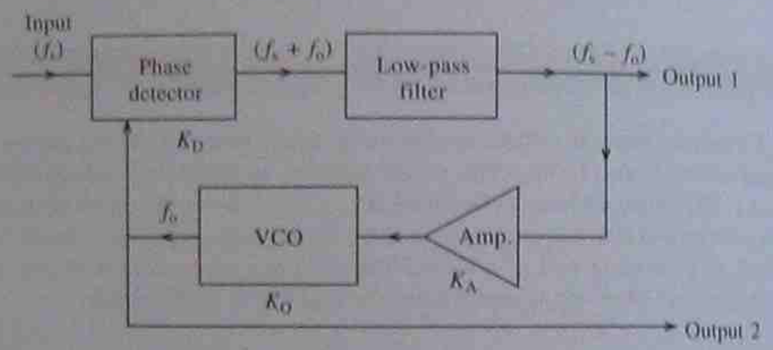


Fig. 6.2

Consider the circuit with no applied signal. There will be no error voltage at the output of the phase detector, and the VCO will run at its natural or free-running frequency (f_o). If an input is applied with a frequency f_s there will be an error voltage generated by the phase detector which is proportional to the phase difference between the two signals. This output consists of sum and difference signals and is filtered through a low-pass filter to leave the difference frequency, which is amplified and applied to the control point on the VCO. The error voltage is such that it reduces the phase, hence the frequency difference between the two signals. Once the loop has locked, the frequency of the oscillator will be exactly the same as that of the reference, but this will be a net phase difference which is necessary to generate the required error voltage to keep the oscillator running at the reference frequency.

When no signal is applied to the PLL it will have no error voltage applied to the oscillator. If a signal is applied and swept towards the oscillator frequency, the phase detector will generate the sum and difference frequencies. If the difference frequency which produces the error voltage falls outside the pass band of the low-pass filter no correction will be applied to the oscillator, but as the reference is swept nearer the oscillator frequency there comes a point where it does fall within the pass band and causes the loop to lock. Therefore, what is called the **capture range** of the loop can be

defined as the frequency range over which it can gain acquisition. This range depends largely on the characteristics of the first-order low-pass filter. Once the PLL has achieved capture, it can maintain lock with the input signal over a wider frequency range called the **lock range.**

6.3 Phase-locked loop elements

The four elements of the fundamental block diagram (Fig. 6.2) will now be discussed individually.

Phase detector

The phase detector is really a d.c. coupled mixer with two a.c. input signals. When the signals have the same frequency they are locked and a phase difference results in a d.c. voltage (V_D) appearing at the output of the filter.

The mixer performs a mathematical multiplication. If the two frequencies are given as f_o and f_s then the instantaneous voltages are given by

$$v_s = V_s \sin(\omega_s t + \theta_s)$$

$$v_o = V_o \sin(\omega_o t + \theta_o)$$

where v_s is the instantaneous signal voltage, ω_s is the signal frequency in radians, V_s is the maximum signal voltage, and where v_o is the instantaneous VCO output, ω_o is the oscillator frequency in radians and V_o is the maximum oscillator voltage; thus the output of the detector is given by

$$v = V_o V_s [\sin(\omega_s t + \theta_s) \sin(\omega_o t + \theta_o)]$$

Applying the identity

$$\sin A \sin B = \frac{1}{2}[\cos(A - B) - \cos(A + B)]$$

we obtain

$$v = \frac{V_s V_o}{2} \cos 2\pi(f_s - f_o + \theta_s - \theta_o)t - \frac{V_s V_o}{2} \cos 2\pi(f_s + f_o + \theta_s + \theta_o)t$$

Hence the output from the detector consists of the sum and difference frequencies. In reality the VCO usually has a square wave output which varies between $+V_o$ and zero. This causes several harmonics to be produced as well as the components mentioned above. However, the low-pass first-order filter response is such that all unwanted frequencies are out with its pass band and only the difference frequency is passed. The output from the filter is therefore given by (6.1)

$$v = \frac{V_s V_o}{2} \cos[(2\pi f_s - 2\pi f_o) + (\theta_s - \theta_o)]$$

When $f_s = f_o$ (6.1) becomes

$$v = \frac{V_s V_o}{2} \cos(\theta_s - \theta_o) \tag{6.2}$$

If $(V_s V_o)/2 = K_D$ (the phase detector gain factor) and $\theta_e = \theta_s - \theta_o$ where θ_e is the static phase error, then

$$v = K_D \cos \theta_e \tag{6.3}$$

When $\theta_e = 90°$ the error voltage is zero; hence it is customary to express (6.2) as

$$v = K_D \sin \theta_e \tag{6.4}$$

so that the static phase error is then shown as the variation from a quadrature relationship. If the static phase error is small, as it generally is in practice, then (6.4) becomes

$$v = K_D \theta_e \tag{6.5}$$

Figure 6.3 shows how the d.c. correction voltage due to θ_e is derived between the VCO and input signal. This can be achieved practically by connecting an oscilloscope at the output of the phase detector. Figure 6.3(a) shows the two signals out of phase by 90°. When this is the case a zero d.c. voltage output results. If the phase shift is greater than 90° as in Fig. 6.3(b), a small negative d.c. output is produced. Finally, if the signals are in phase then a small positive d.c. output voltage is produced, as is shown in Fig. 6.3(c). It should be appreciated, however, that small changes of θ_e are considered in practice. From these diagrams the average d.c. value of the unfiltered output is proportional to the phase difference between f_s and f_o. Only the d.c. component is present at the output of the filter.

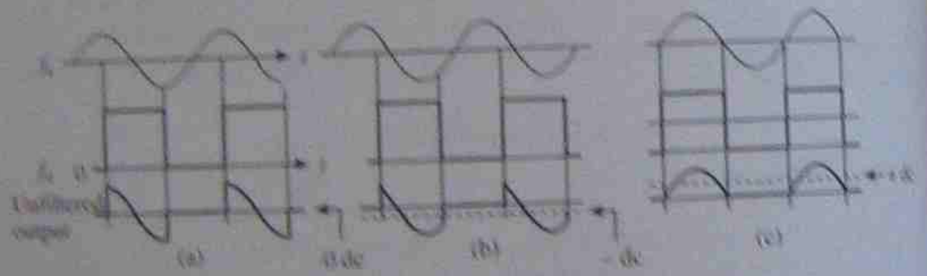


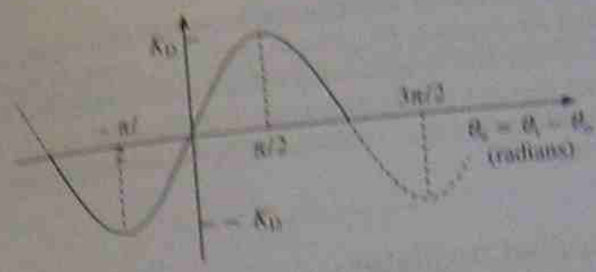
Fig. 6.3

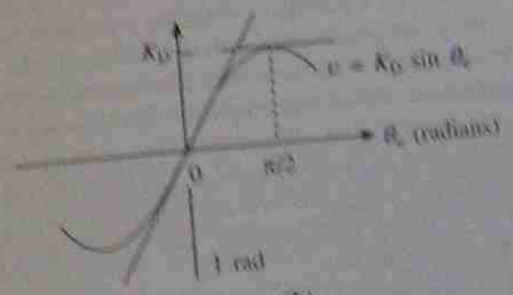
Equation (6.4) showed the phase detector gain factor (K_D). This factor is generally given in volts per radian and is derived from the fact that the phase detector characteristic is a sinusoidal output with period 2π radians. Tracking is limited between $\pm\pi/2$ otherwise positive feedback would be applied to the loop, with resultant instability. This is shown in Fig. 6.4(a). The slope of the characteristic is given by the derivative of expression (6.4) with $\theta_e = 0$.

$$\frac{d}{d\theta_e} K_D \sin \theta_e \bigg|_{\theta_e = 0} = K_D \cos 0 = K_D$$

as indicated in Fig. 6.4(b). This figure shows the response when the VCO output is a sine wave, while Fig. 6.4(c) shows the response when the VCO output is square.

There is one further point which should be understood before leaving the PLL. Once





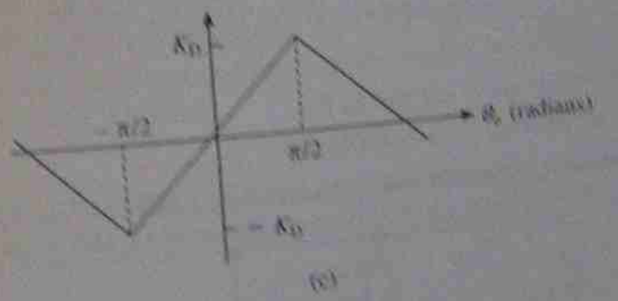


Fig. 6.4

acquisition has been gained the loop will remain locked over the lock range. There are two main factors which affect this. First, the range over which the VCO can swing will be limited, and if the reference goes beyond this then the lock will be lost. Second, the output of the phase detector is sensitive to both phase and amplitude in most cases. Hence if the signal amplitude decreases, the phase difference between the two signals must increase to compensate for this. Therefore at low signal levels the effective lock range is reduced and the phase errors will be larger. Conversely, a large signal will permit use of the full oscillator swing and give smaller phase errors.

Amplifier

The amplifier is a d.c. amplifier which amplifies the phase detector output. It can be a

transistor type, or an operational amplifier can be used in its inverting and non-inverting modes. The gain of the amplifier (K_v) can be altered by means of external resistors if a discrete system is used or else by connecting a single resistor externally for chip operation. This will be shown later in a practical example. It is important that the bandwidth of the d.c. amplifier should be very high compared with the loop bandwidth or there will be instability in the loop.

Voltage-controlled oscillator

This element functions virtually as a voltage-to-frequency convertor in which the output frequency is a direct result of the phase error voltage. Generally the VCO incorporates two varactor diodes fabricated into a multivibrator configuration. When a constant d.c. correction voltage is applied the VCO will output its free-running frequency which is determined by an external *RC* network. When this free-running frequency is plotted against the phase error voltage the conversion gain (K_o) of the VCO can be obtained. This conversion gain is defined as the change of free-running frequency to the applied input error voltage. It should be a linear characteristic, and operation is generally centred around the midpoint of the characteristic.

The LM566 is a general-purpose VCO, the data sheets for which are given at the end of the chapter. A typical configuration for this chip is shown in Fig. 6.5. In this configuration the chip operates as a function generator. If this integrated circuit is used the following points should be noted:

(a) R_1 should lie between 2 kΩ and 20 kΩ.

(b) V_c should lie between (+V) and 0.75 (+V).

(c) The free-running frequency should be less than 1 MHz.

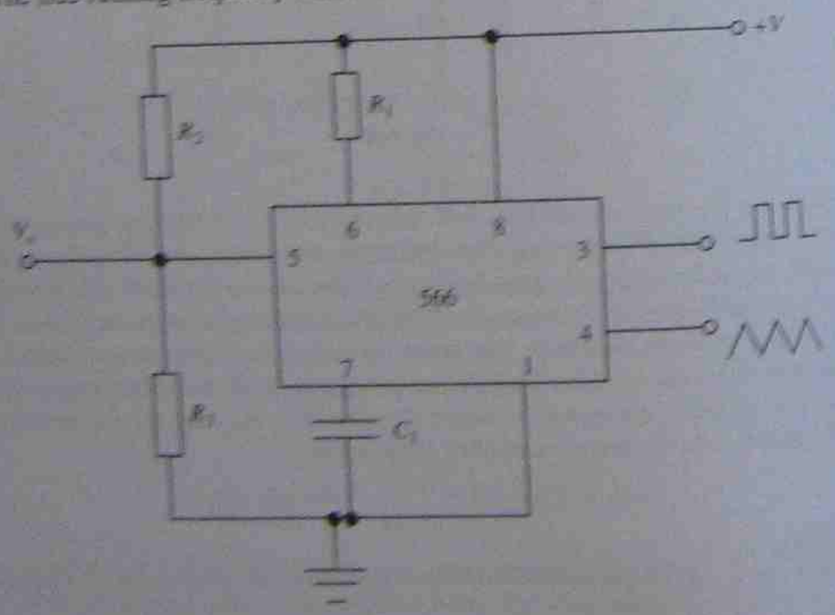


Fig. 6.5

(d) The supply voltage should lie between 10 V and 24 V.

(e) R_2 and R_3 set the modulating voltage at a fixed level by use of a voltage divider network.

(f) The free-running frequency is given by

$$f_o = \frac{2}{R_1 C_1} \frac{(+V) - V_c}{(+V)} \tag{6.6}$$

This chip has been introduced to show how the VCO may be used for a separate function. The conversion gain is given in the data sheets.

Filter

The function of the low-pass filter is to pass the difference frequency while suppressing any noise or interference. However, it also improves the frequency response; this can be done by using either a lag compensation or lead-lag compensation filter.

All the PLL elements are d.c. coupled except for the phase detector input and the VCO output. Also the bandwidth of a phase detector can be very high which means the *RC* output time constant of the phase detector limits the frequency response. This is the filter which passes the difference frequency. Also the VCO frequency response is mainly responsible for limiting the loop bandwidth. For a PLL which has no compensation built into it, the overall uncompensated loop gain is determined by the product of the individual element responses. This is given by

$$K_L = 2\pi K_D K_A K_O \tag{6.7}$$

where K_L is the overall loop gain, K_A is the amplifier gain and K_O is the VCO loop gain. It can also be shown that for an uncompensated PLL the bandwidth is given by

$$K_L = BW \tag{6.8}$$

6.4 Compensation

For many applications the uncompensated loop is too slow, and if there is a sudden change in input frequency the output waveform will be rounded instead of square. The loop response can be improved by introducing some form of loop compensation in the form of a phase delay network.

These compensation networks are generally of three types, referred to as **phase lag**, **phase lead** or **lead-lag** circuits, and the amount of compensation is best shown in the form of a **Bode plot**. An explanation of these terms will be given initially before their application to compensation is examined.

The Bode plot

It is convenient and generally accepted in practice to plot the logarithmic value of frequency

response rather than the raw frequency itself. This is because a greater range of frequencies can then be plotted on suitable graph paper without losing the resolution of the response curve. Log-linear or log-log graph paper may be conveniently used. Figure 6.8 uses log-linear or semilog paper, with the frequency plotted horizontally and the gain (dB) plotted vertically. Log-linear graph paper is also used to plot the phase shift between the input and output responses.

A typical single pole transfer function is given by

$$A_H = \frac{A_M}{1 + j\left(\frac{f}{f_H}\right)} \tag{6.9}$$

Taking logs of both sides of (6.9) gives

$$20 \log_{10} |A_H| = 20 \log_{10} |A_M| - 20 \log_{10} \sqrt{1 + \left(\frac{f}{f_H}\right)^2} \tag{6.10}$$

where A_H represents the high frequency gain and A_M represents the midband gain of the circuit.

If (6.10) is plotted on semilog graph paper then a response similar to that shown in Fig. 6.6(a) will be obtained. This figure shows the response which would be obtained if f_H was plotted against A_H (shown as a dotted line), and also the straight-line approximation known as the Bode plot. It consists of an idealized plot of two straight lines which represent the midband gain and the high-frequency gain. Obviously there will be a slight error here, but it gives a good representation of the expected response without a lengthy plotting procedure.

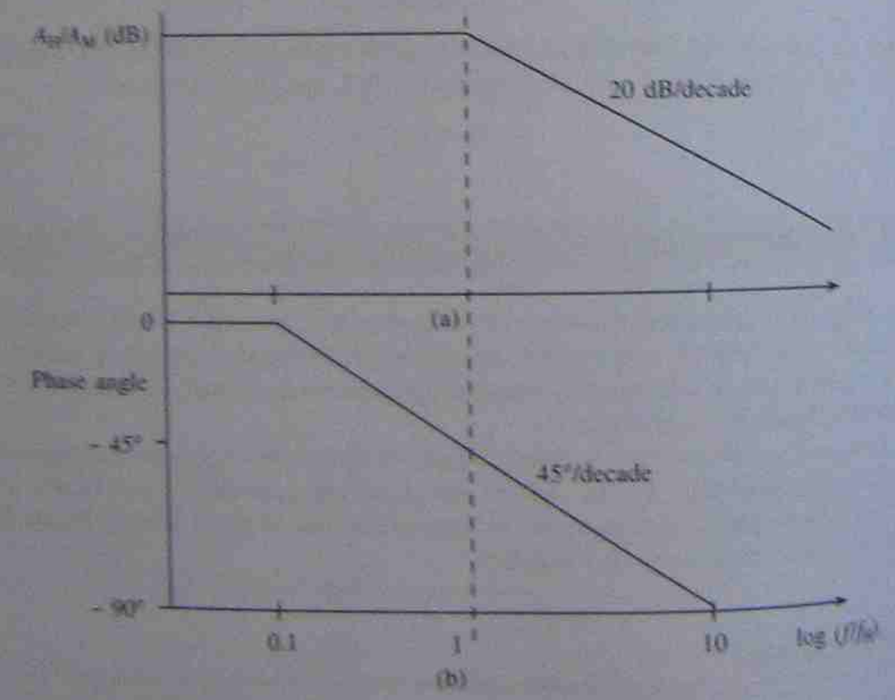


Fig. 6.6

Note that the response rolls off at 20 dB/decade after the cut-off frequency (f). This is characteristic of a single-pole transfer function. A two-pole function would have a roll-off of 40 dB/decade. This type of response has already been discussed in Chapter 3.

A phase/frequency plot is also shown in Fig. 6.6(b). This is also a straight-line approximation, and as can be seen, for frequencies below 0.1 f_H the phase is assumed to be zero. For frequencies above 10 f_H the phase is assumed to be $-90°$. This plot is assumed to be a straight line between these two points, passing through $-45°$ at $f = f_H$. The slope is therefore 45°/decade. For a two-pole function it would be 90°/decade.

Delay networks

These networks were encountered in our discussion of passive low and high-pass filter networks. The basic types used in compensation networks are shown in Fig. 6.7.

A lead network is an R_1C_1 circuit in which the output voltage across R_1 leads the input voltage, while a lag network is an R_2C_2 network in which the output voltage across C_2 lags the input voltage. The lead-lag network is a combination of these two. At lower frequencies the lead circuit (R_1C_1) dominates due to the high reactance of C_1. As the frequency increases X_{C1} decreases, thus allowing the output voltage to increase. At a particular frequency the response of the lag circuit (R_2C_2) takes over and the decreasing value of X_{C2} causes the output voltage to decrease. Hence the lead-lag network has a particular frequency at which the phase shift through the circuit is zero degrees and the attenuation falls. Below a particular frequency the lead circuit causes the output to lead the input, and above a particular frequency the lag circuit causes the output to lag the input. This principle is used for frequency compensation.

Compensation analysis

If a first-order filter similar to that shown in Fig. 6.7(b) is added to the system then a second-order system is produced because the VCO acts as an integrator.

The transfer function of this filter for a sinusoidal input is given by

$$\begin{aligned} F(j\omega) &= \frac{V_o(j\omega_c)}{V_i(j\omega_c)} \\ &= \frac{1}{j\omega_c C_2} \Big/ \left(R_2 + \frac{1}{j\omega_c C_2}\right) \\ &= \frac{1}{1 + j\omega_c C_2 R_2} \end{aligned} \tag{6.11}$$

At the 3 dB or corner frequency the magnitude of the filter transfer function is

$$|F(j\omega_c)| = \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + \omega_c^2 C_2^2 R_2^2}}$$

Hence

$$f_c = \frac{1}{2\pi R_2 C_2} \tag{6.12}$$

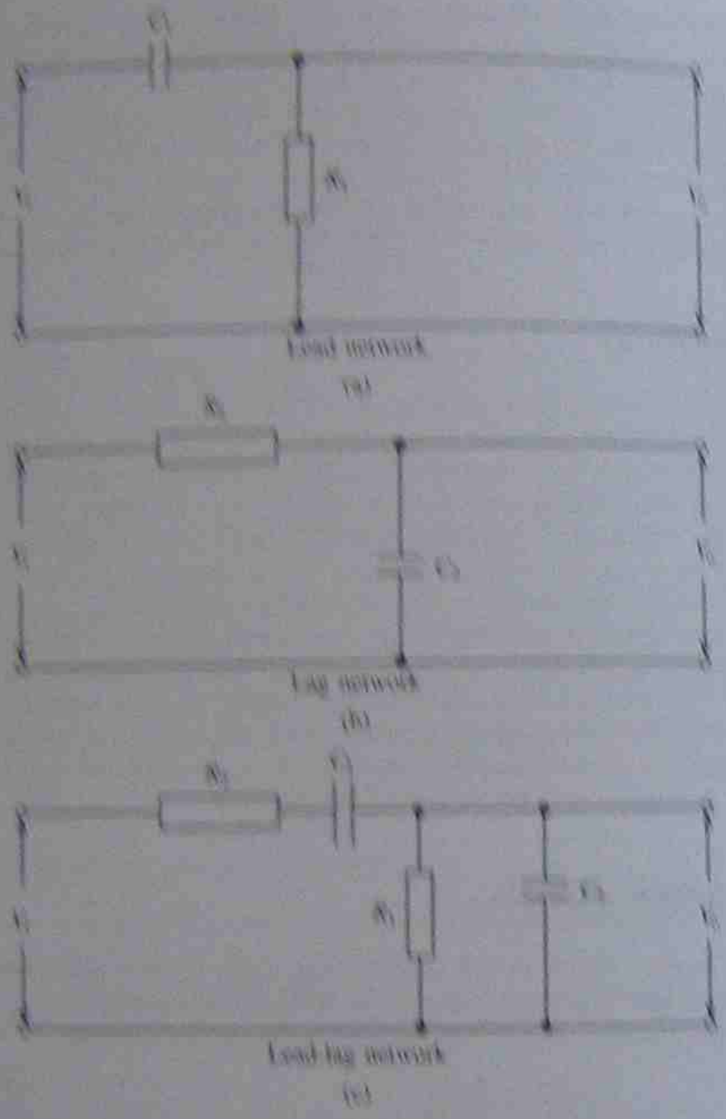


Fig. 8.7

This compensation is generally shown in the form of a Bode plot similar to that of Fig. 8.8. This plot shows how the output voltage remains constant at 0 dB up to the cut-off frequency (f_1) and here thereafter attenuation occurs at 20 dB/decade.

Lead-lag compensation is also used, and a variation on the circuit of Fig. 8.7(c) is shown in Fig. 8.9. The filter transfer function for this filter is given by

$$F(j\omega_0) = \left(R_2 + \frac{1}{j\omega_0 C}\right) \Big/ \left(R_1 + R_2 + \frac{1}{j\omega_0 C}\right)$$

$$= 1 + \frac{1}{j\omega_0 C R_2} \Big/ (1 + j\omega_0 C (R_1 + R_2))$$

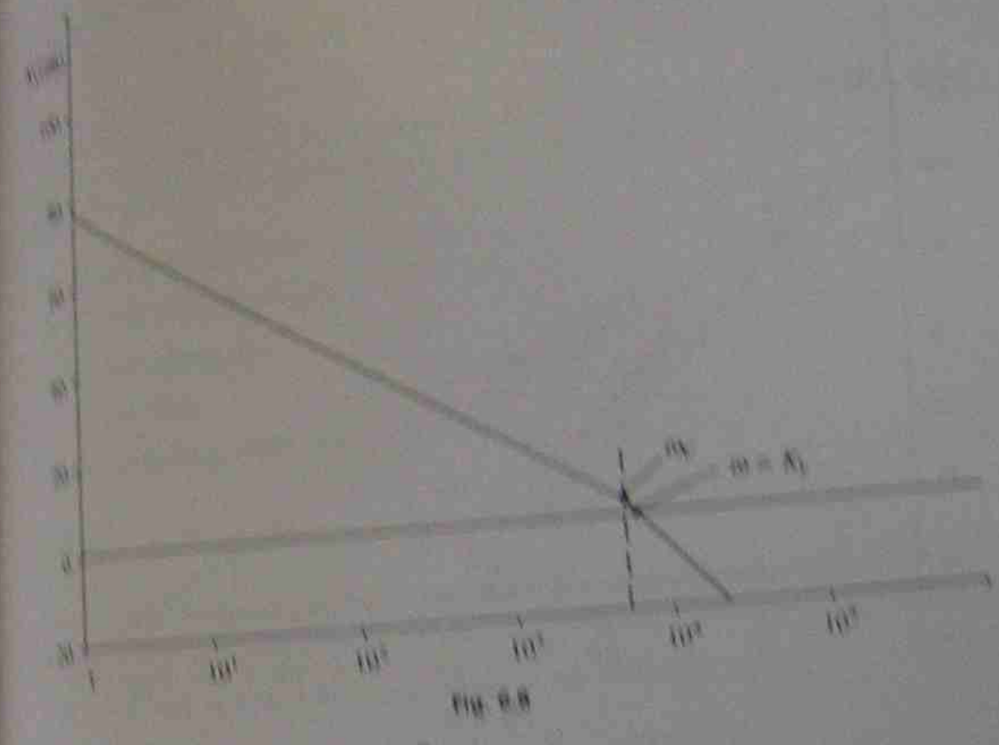


Fig. 8.8

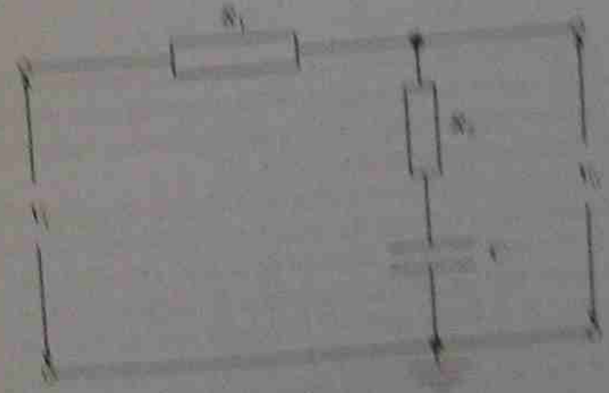


Fig. 8.9

Two cut-off frequencies are indicated here at the 3 dB points:

$$\omega_1 = \frac{1}{CR_2} \qquad (8.13)$$

and

$$\omega_2 = \frac{1}{C(R_1 + R_2)} \qquad (8.14)$$

Once again this is shown on the Bode plot of Fig. 8.10. In this case the output voltage is attenuated at the rate of 20 dB/decade until the second cut-off frequency (ω_2). The output voltage then remains constant.

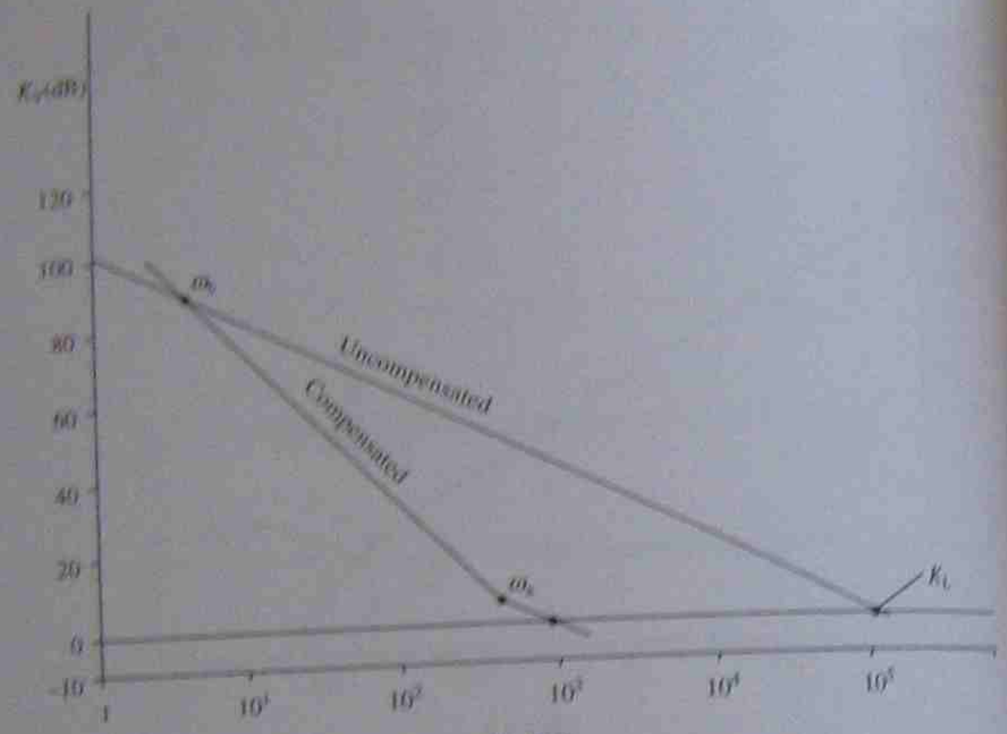


Fig. 6.10

The advantage of lead-lag compensation is that all the parameters (K_L, damping factor and bandwidth) can be varied independently. This is not the case with lag compensation, and it would be a distinct disadvantage in such applications as demodulators where these parameters have to be independently controlled.

Obviously the filter bandwidth can be varied according to the design of the compensating filter. There are advantages in making the pass band small. The narrower the filter pass band, the less likely the loop is to be affected by noise. Also if the RC time constant is long, the loop can store the signal frequency if it is temporarily lost. If, however, the signal frequency is lost it is more difficult to regain lock as the capture range will be reduced. Generally a compromise has to be found. The low-pass filter does not alter the lock frequency but it does alter the tracking rate. If tracking is required at high frequencies, the cut-off frequency should be high, but not too high, in order to avoid noise interference.

Example 6.1
A PLL has the following component gains: $K_D = 0.4$ V/rad, $K_A = 5$ and $K_O = 25$ kHz/V. Determine the loop gain.

Solution

$$K_L = 2\pi K_D K_A K_O = 2\pi \times 0.4 \times 5 \times 25 = 314 \times 10^3 \text{ Hz/rad}$$

$$K_L(\text{dB}) = 20 \log 314 \times 10^3 = 109.9 \text{ dB}$$

Note that this answer can also be expressed in kilohertz per radian:

$$K_L = K_D K_A K_O = 0.4 \times 5 \times 25 = 50 \text{ kHz/rad}$$

Example 6.2
A PLL has parameters $K_A = 5$, $K_O = -35$ kHz/V, $K_D = 0.3$ V/rad and $f_o = 220$ kHz. If the input signal (f_s) is 180 kHz and the loop is locked, determine:

(a) the loop gain in kHz/rad;

(b) the VCO output frequency;

(c) the static phase error;

(d) the lock range;

(e) the maximum possible value of v.

Solution

(a)

$$K_L = K_O K_D K_A = -35 \times 0.3 \times 5 = -52.3 \text{ kHz/rad}$$

(b) When the loop is locked, $f_s = f_o = 220$ kHz.

(c) As the loop is locked the input voltage to the VCO must be

$$V_i = \frac{180 - 220}{-35} = \frac{-40}{-35} = 1.143 \text{ V}$$

(This is a d.c. voltage, of course.) Since $K_A = 5$,

$$v = \frac{V_i}{K_A} = \frac{1.143}{5} = 0.229 \text{ V}$$

Also

$$\theta_e = \frac{v}{K_D} \text{ from expression (6.5)}$$

$$= \frac{0.229}{0.3} = 0.763 \text{ rad}$$

(d) It has already been seen from (c) that V_i is required to keep the system in lock, so the phase comparator must produce a voltage of

$$v = \frac{V_i}{K_A} = \frac{\Delta f}{K_O K_A} \tag{6.15}$$

where Δf is the lock range. Also $\theta_e = v/K_D$, hence

$$v = K_D \theta_e \tag{6.16}$$

Substituting (6.13) into (6.14) gives

$$\theta_e K_D = \frac{\Delta f}{K_O K_A}$$

$$\therefore \quad \theta_e = \frac{\Delta f}{K_L} \tag{6.17}$$

Figure 6.4(b) shows the VCO characteristics for a sinusoidal input. v will reach a maximum at $\theta_e = \pi/2$. Hence the total lock range is $\pm\pi/2$ or π radians. This is the maximum static phase error $\theta_{e(max)}$. Hence from expression (6.17)

$$\Delta f = \theta_e K_L = \pi \times 52.5 = 165 \text{ kHz}$$

(e) v is maximum when $\theta_e = \pi/2$ so

$$v = K_D \theta_e = 0.3 \times \frac{\pi}{2} = 0.47 \text{ V}$$

Example 6.3

A PLL is compensated by means of a lead-lag compensation network. If $\omega_s = 350$ rad and $\omega_n = 5$ rad, determine the values of the filter components. Assume the output resistance (R_o) of the phase comparator is 35 kΩ.

Solution

Select $C = 0.1$ μF. From (6.13),

$$\omega_n = \frac{1}{R_2 C}$$

$$\therefore \quad R_2 = \frac{1}{\omega_n C} = \frac{10^6}{350 \times 0.1} = 28.57 \text{ k}\Omega$$

From (6.12),

$$\omega_n = \frac{1}{C(R_1 + R_2)}$$

$$\therefore \quad R_1 = \frac{1 - \omega_n C R_2}{C\omega_n} = \frac{1 - 5 \times 0.1 \times 10^{-6} \times 28.57 \times 10^3}{0.1 \times 10^{-6} \times 5} = 1.97 \text{ M}\Omega$$

Since $R_o = 35$ kΩ the value of the external resistor R_1 should be 1.97 MΩ.

Example 6.4

Figure 6.11 shows the characteristics of a PLL. The low-pass filter consists of an RC network having a cut-off frequency of 40 kHz, and the characteristics for each stage are shown in the annotated diagram. Determine:

(a) K_D, K_V, K_O and K_L;

(b) the values of R and C for the filter;

(c) the value of V_i, v and θ_e under lock conditions;

(d) the lock range.

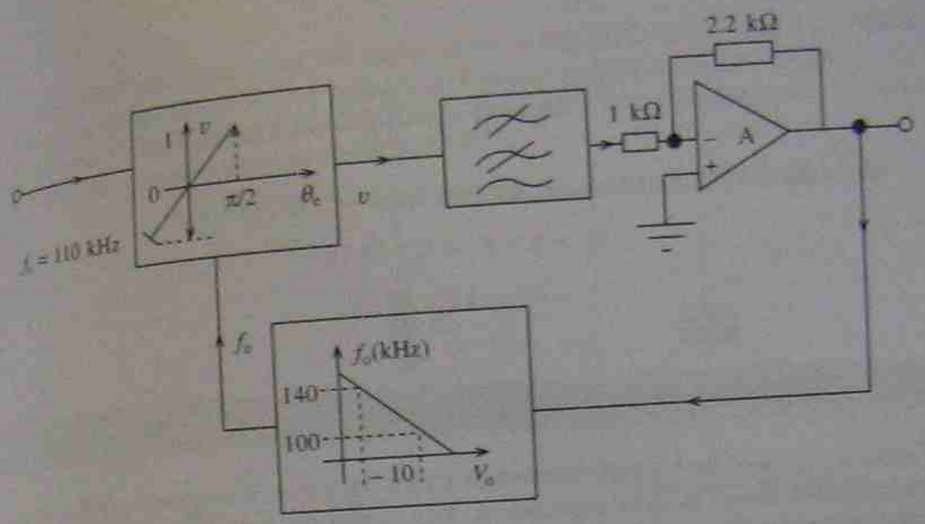


Fig. 6.11

Solution

(a) From the characteristics

$$K_D = 1 \text{ V} \Big/ \frac{\pi}{2} = 0.64 \text{ V/rad}$$

$$K_A = \frac{2.2}{1} = 2.2$$

For K_O it is assumed from the characteristics that the output voltage (V_O) is linear between 100 kHz and 140 kHz.

$$K_O = \frac{100 - 140}{(1 - (-1))} = -20 \text{ kHz/V}$$

Hence $K_L = K_A K_D K_O = -2.2 \times 0.64 \times -20 = 28.16$ kHz/rad

(b) This is a first-order RC filter, hence

$$f_c = \frac{1}{2\pi RC}$$

Select $C = 0.01$ μF

$$\therefore \quad R = \frac{1}{2\pi f_c C} = \frac{10^6}{2\pi \times 40 \times 10^3 \times 0.01} = 398 \ \Omega$$

(c)

$$V_i = \frac{f_s - f_o}{K_O}$$

From the characteristics the free-running frequency is 120 kHz. So

$$V_i = \frac{110 - 120}{-20} = 0.5 \text{ V}$$

$$v = \frac{V_i}{K_A} = \frac{0.5}{-2.2} = -0.227 \text{ V}$$

Also

$$\theta_e = \frac{v}{K_D} = \frac{-0.227}{0.64} = -0.355 \text{ rad}$$

(d) As for the previous example the lock range is $\pm \pi/2$ or π rad.

$$\therefore \quad f_L = \pi \times K_L = \pi \times 28.16$$
$$= 88.46 \text{ kHz}$$

6.5 Integrated phase-locked loops

Figure 6.2 showed the various elements of a PLL. However, it is normal practice to use an integrated circuit in most applications. Two commonly used PLL chips are the 565 manufactured by National Semiconductor and the 4046 manufactured by SGS-Thomson Microelectronics. Details of these integrated circuits are given in the data sheets, and these should be consulted when studying the worked examples considered later. Initially the following points should be noted when using the data sheets for the 565.

(a) The loop gain is given as $K_O K_D$, but this is for $K_A = 1$. Typically a value of 1.4 is used, and when this is the case the loop gain is given as $K_O K_D K_A$. From the data sheets

$$K_O K_D = \frac{33.6 f_o}{V_c} \tag{6.18}$$

but

$$K_O K_D K_A = \frac{50 f_o}{V_c} \tag{6.19}$$

(b) Where formulae are stated as $\pm$ values it is easier to keep parameter values in this form. For example, if a lock range (f_L) of $\pm$ 600 Hz is used in a problem in conjunction with a free-running frequency of 1200 Hz, then

$$f_L \pm \frac{8 f_o}{V_C} \tag{6.20}$$

and f_L = 1200 Hz while f_o = 1200 Hz. This accommodates a swing of 600 Hz on either side of the free-running frequency.

(c) The capture range for a simple lag filter is given by

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}} \tag{6.21}$$

where $\tau = 3.6 \times 10^3 C_1$. For a lag-lead filter

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau_1 + \tau_2}} \tag{6.22}$$

where $\tau_1 + \tau_2 = (R_1 + R_2)C_1$.

(d) A typical configuration for this chip is given in Fig. 6.12. In this circuit the 680 Ω resistors are included to ensure that both input terminals receive equal bias conditions. R_O should have a value between 2 kΩ and 20 kΩ, and finally the loop gain can be reduced by connecting a resistor between pins 6 and 7.

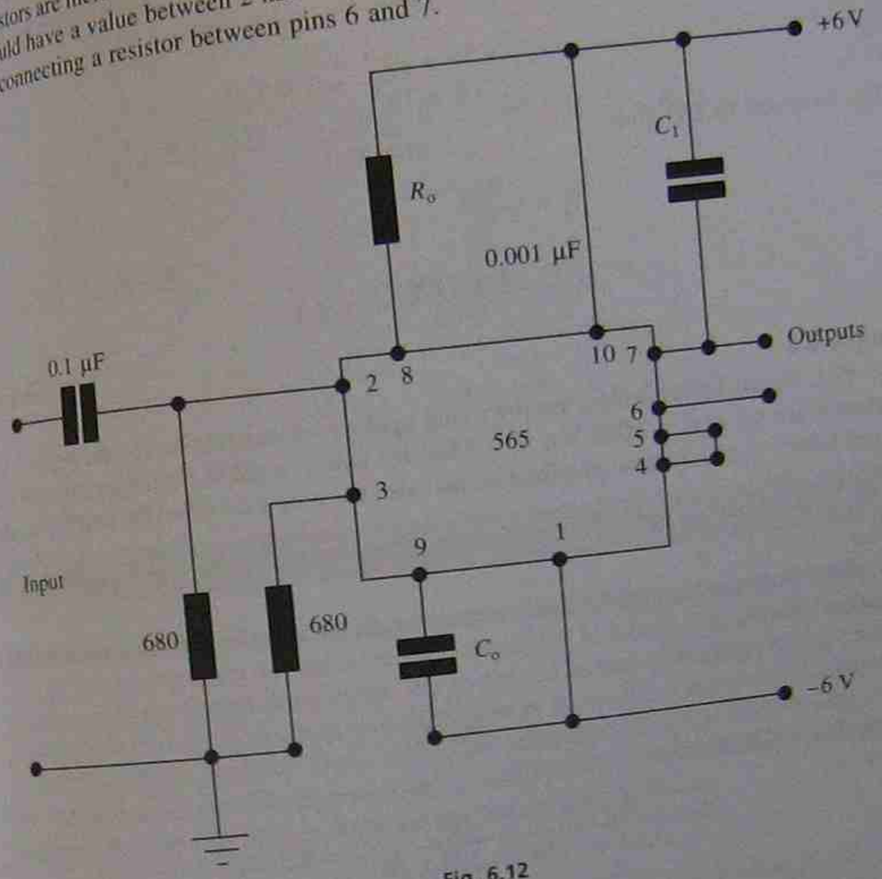


Fig. 6.12

Example 6.5

A 565 PLL is designed for use in a wide closed-loop bandwidth application. If f_o = 1100 Hz, f_L = ±700 Hz and f_C = 400 Hz, calculate R_O, C_O, C_1 and suitable values for the power supply.

Solution

$$f_o = \frac{0.3}{R_O C_O}$$

Selecting C_O = 100 nF,

$$R_O = \frac{0.3}{f_o C_O} = \frac{0.3 \times 10^9}{1100 \times 100} = 2.73 \text{ k}\Omega$$

Also

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$$

$$\therefore \quad \tau = \frac{2\pi f_L}{(2\pi f_C)^2} = \frac{2\pi \times 1400}{(2\pi \times 400)^2} = 1.39 \times 10^{-3} \text{ s}$$

Now $\tau = 3.6 \times 10^3 \times C_1$

$$\therefore \quad C_1 = \frac{1.39 \times 10^{-3}}{3.6 \times 10^3} = 0.387 \ \mu\text{F}$$

Using equation (6.18) gives

$$f_L = \pm \frac{8 f_O}{V_C}$$

$$V_C = \pm \frac{8 \times 1100}{1400} = +6.3 \text{ V}$$

Example 6.6
A 565 PLL has to be used for a narrow-band application in order to reduce noise. The parameters are set at $f_o = 1000$ Hz, $f_L = \pm 500$ Hz and $f_C = \pm 200$ Hz. Determine all the required values to satisfy this specification and also the loop gain when the amplifier gain is unity.

Solution
The configuration used in Fig. 6.12 is used once again but a lag-lead filter is used for this application. Since

$$f_o = \frac{0.3}{R_O C_O}$$

selecting $C_O = 120$ nF gives

$$R_O = \frac{0.3}{f_o C_O} = \frac{0.3}{10^3 \times 120 \times 10^{-9}} = 2.5 \text{ k}\Omega$$

Also

$$f_L = \pm \frac{8 f_o}{V_C}$$

Hence

$$V_C = \pm \frac{8 f_o}{f_L} = \pm \frac{8 \times 10^3}{10^3} = \pm 8 \text{ V}$$

$$f_C = \mp \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau_1 + \tau_2}}$$

$$\tau = \tau_1 + \tau_2 = \frac{2\pi f_L}{(2\pi f_C)^2} = \frac{2\pi \times 10^3}{(2\pi \times 400)^2} = 9.95 \times 10^{-4} \text{ s}$$

So

$$R_1 C_1 + R_2 C_1 = \tau_1 + \tau_2 = \tau$$

$$\therefore \quad 9.95 \times 10^{-4} = R_1 C_1 + R_2 C_1$$

$R_1 = 3.6$ kΩ; selecting $C_1 = 100$ nF gives

$$9.95 = 3.6 \times 10^3 \times 100 \times 10^{-9} + R_2 \times 100 \times 10^{-9}$$

Hence

$$R_2 = \frac{9.95 \times 10^{-4} - 3.6 \times 10^3 \times 100 \times 10^{-9}}{100 \times 10^{-9}} = 63.5 \text{ k}\Omega$$

$C_2 = 0.1 C_1$; hence

$$C_2 = 10 \text{ nF}$$

For $K_A = 1$,

$$K_O K_D K_A = \frac{33.6 f_o}{V_C} = \frac{33.6 \times 10^3}{16} = 2.1 \text{ kHz/rad}$$

6.6 Phase-locked loop design using the HCC4046B

This chip is a monolithic integrated circuit using a 16-pin package. It is a CMOS micropower PLL device having extra on-board facilities which the 565 does not have. These facilities, together with the circuit description, are explained in the data sheets at the end of the chapter. The functional diagram in the data sheets shows the component connections for the VCO and filter sections. These values are calculated using the same equations as for the 565 and a design information sheet is also provided. The following examples will demonstrate how this PLL is designed for certain specifications.

Example 6.7
An HCC4046B CMOS PLL has to be used with the following parameters: $f_L = \pm 400$ kHz, $f_C = \pm 200$ kHz and $f_o = 500$ kHz. Design a PLL having no offset using comparator 1. Also select a suitable power supply.

Solution

$$f_o = \frac{0.3}{C_1 R_1}$$

(note that the symbols on the data sheet are used). Select $C_1 = 50$ pF. Hence

$$R_1 = \frac{0.3 \times 10^{12}}{5 \times 10^5 \times 50} = 12 \text{ k}\Omega$$

$$f_C = \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$$

where $\tau = R_2 C_2$.

$$\therefore \quad \tau = \frac{2\pi f_L}{(2\pi f_C)^2}$$

$$= \frac{2\pi \times 8 \times 10^5}{(2\pi \times 4 \times 10^5)^2} = 796 \text{ nS}$$

Select $C_2 = 10$ nF. Then

$$\tau = R_3 C_2$$

so

$$R_3 = \frac{\tau}{C_2} = \frac{796 \times 10^{-9}}{10 \times 10^{-9}} = 79.6\ \Omega$$

A suitable value for V_{DD} is 10 V. The schematic diagram is shown in Fig. 6.13.

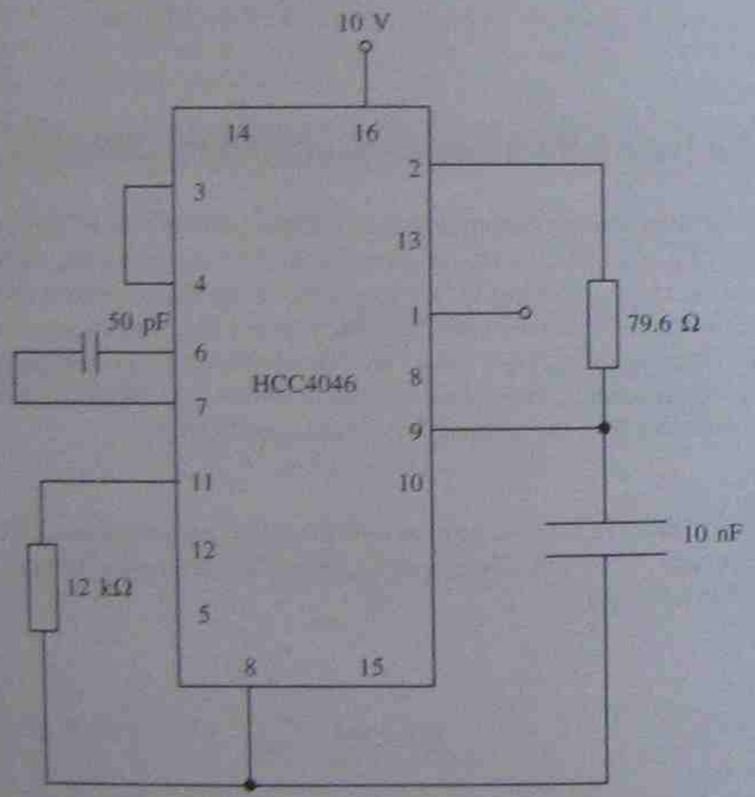


Fig. 6.13

Example 6.8

An HCC4046B chip has to be configured to the following specification: $f_o = 100$ kHz, $f_L = \pm 300$ kHz and $f_C = \pm 300$ kHz. The power supply has to be 15 V and the VCO has to be operated with a variable offset. Calculate all components and draw a schematic diagram which would be suitable for this specification and capable of monitoring the locked condition.

Solution

$$f_o = \frac{0.3}{R_1 C_1}$$

Select $R_1 = 47$ kΩ. Then

$$C_1 = \frac{0.3}{R_1 f_o} = \frac{0.3 \times 10^{12}}{47 \times 10^3 \times 100 \times 10^3} = 63.8 \text{ pF}$$

$$f_C = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$$

$$\therefore \quad \tau = \frac{2\pi f_L}{(2\pi f_C)^2} = \frac{2\pi \times 600 \times 10^3}{(2\pi \times 600 \times 10^3)^2} = 0.2653\ \mu\text{S}$$

Select $R_3 = 10$ kΩ

$$C_2 = \frac{\tau}{R_3} = \frac{0.2653 \times 10^{-6}}{10^4} = 26.53 \text{ pF}$$

As $f_L = f_C$, comparator 2 has to be used in this design. Also, in order to operate a variable-frequency offset R_2 should be variable between 5 kΩ and 1 MΩ, hence a 1 MΩ potentiometer should be connected to pin 12. The final design is shown in Fig. 6.14. Note that some trimming of the components may be required.

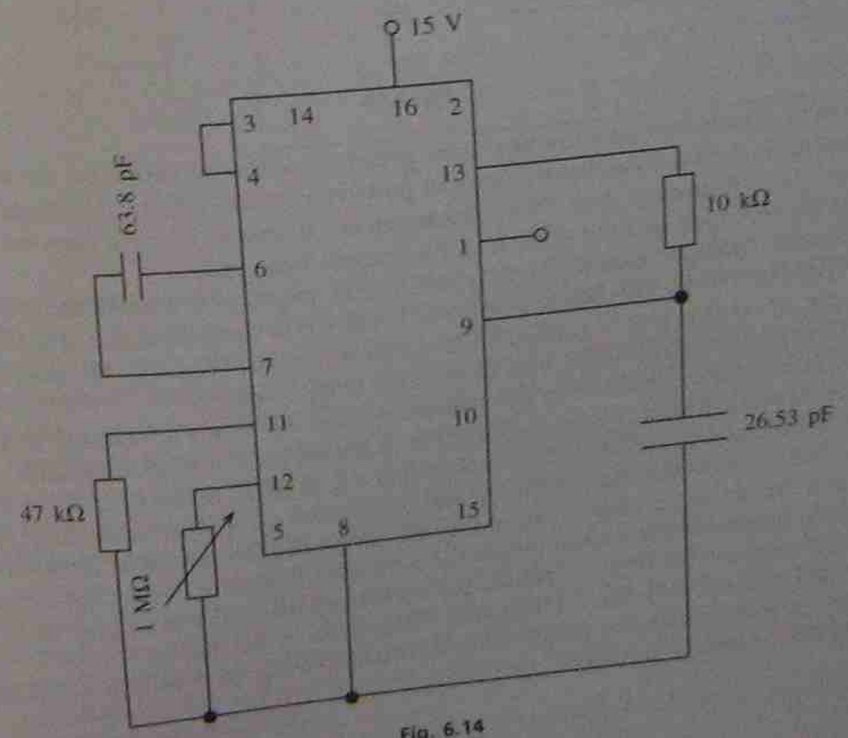


Fig. 6.14

6.7 Frequency synthesis

Frequency synthesis is a method of producing a range of frequencies with crystal-controlled stability. Synthesizers are used in test equipment, communication equipment and television and radio channel selection.

A communications receiver is shown in Fig. 6.15. This receiver uses a principle known as **heterodyning** in which two frequencies are mixed together in a demodulator to produce a single frequency known as the intermediate frequency. Each time the receiver is tuned to a particular channel or carrier, conversion takes place to a low or intermediate frequency. In order to achieve this the local oscillator is usually tuned to a frequency above that of the receiver RF signal. The difference frequency is selected while all other frequencies are suppressed. The difference frequency is then passed on to the IF amplifier.

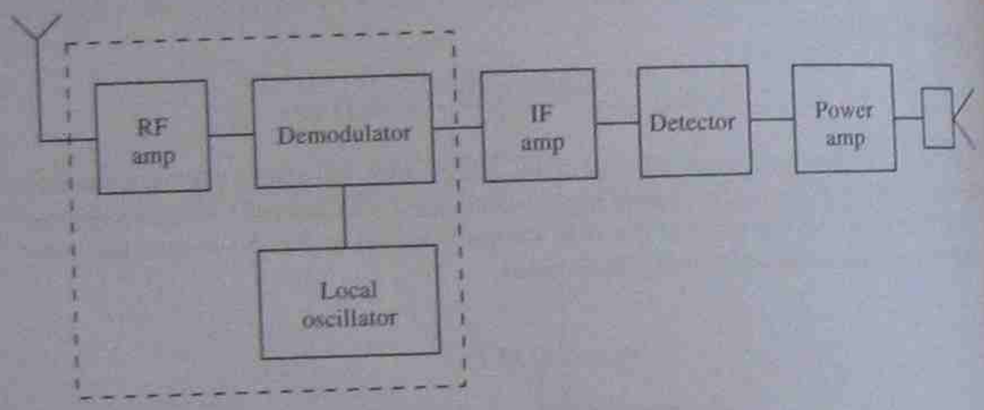


Fig. 6.15

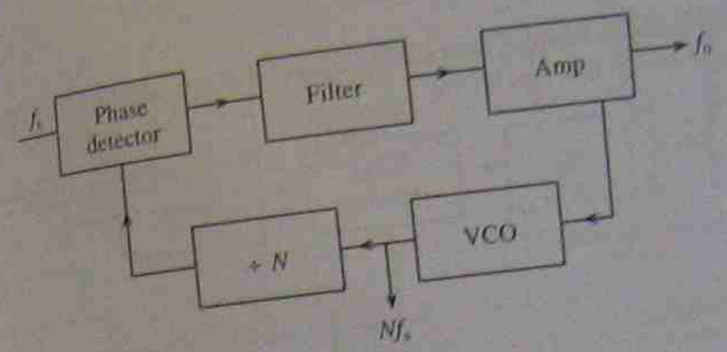
Modern digital receivers use the same principle described above but the use of a synthesizer in the local oscillator stage can provide a system which is highly stable and has very little frequency drift. The synthesizer is variable in discrete steps but uses a crystal for very high stability at each of the discrete frequencies.

Frequency multiplication is generally involved in frequency **synthesis**, and this can be achieved in two ways. The first is to lock the oscillator to some harmonic of the input or reference signal (f_s). This is generally the simplest method, but it has the disadvantage that the range becomes smaller with an increase in harmonics.

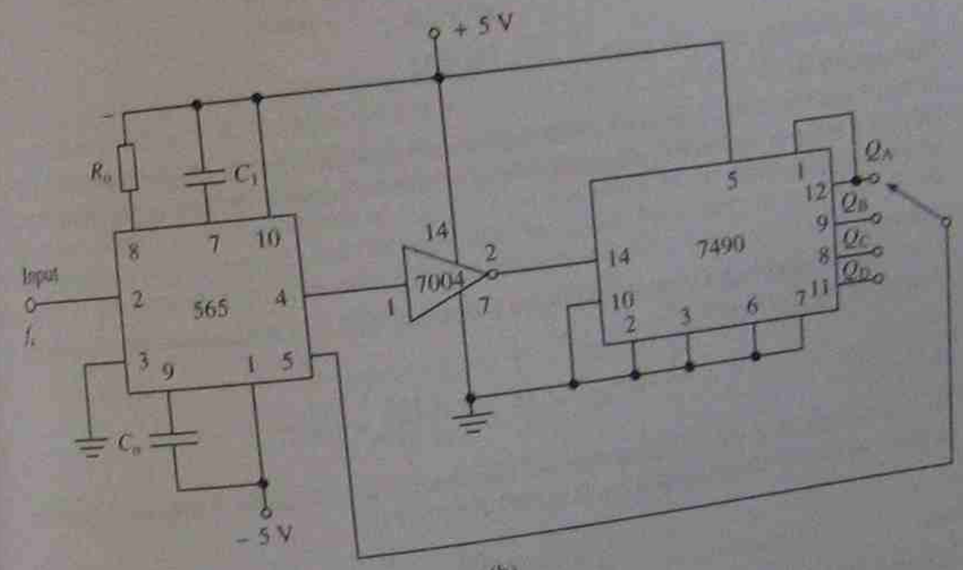
The most frequent method is the indirect method in which a PLL and frequency division network is used. This is shown in Fig. 6.16: the general block diagram is shown in Fig. 6.16(a) and a practical system is shown in Fig. 6.16(b). In this case the VCO runs at some harmonic of the input signal (f_s) and comparison takes place at this input signal. The filter has to be carefully designed as the phase detector produces both sum and difference frequencies and when locked the difference frequency is d.c., but the sum is twice the fundamental. If this is not adequately filtered there will be a ripple on the d.c. error voltage which will cause a frequency modulation on the output.

Figure 6.16 compares two frequencies and produces a d.c. error voltage which causes the two frequencies to be locked. This gives

$$f_s = \frac{f_o}{N} \tag{6.23}$$



(a)



(b)

Fig. 6.16

and using a programmable divider will enable N to be varied. This type of divider is different from a presettable or fixed-modulus divider in that its moduli are programmed for the particular input channels which may be required.

The presettable divider is the basic building block which can be used to construct a divider which has any modulus. Practically all presettable dividers are constructed by using four JK flip-flops, and they may be connected in such a way that they function as decade counters or in the count-up or count-down mode. A flip-flop is a bistable device, that is, it has two stable states, namely, a high (1) state and a low (0) state. The output of a flip-flop indicates which bit it is storing.

A practical circuit is shown in Fig. 6.16(b). In this case a decade counter has been used. The output signal from the 565 is passed through an inverter to the decade counter. The output is taken from pin 12 and so the output from the PLL is twice the free-running frequency of the VCO. The VCO can only be varied over a limited range depending on its linear characteristic, and so it may be necessary to change the VCO frequency by varying the timing capacitor C_1.

The circuit shown in Fig. 6.16 can only generate multiples of f_s and if it is necessary

to produce frequencies below f_s then a fixed-modulus divider can be used to divide down. This is shown in Fig. 6.17.

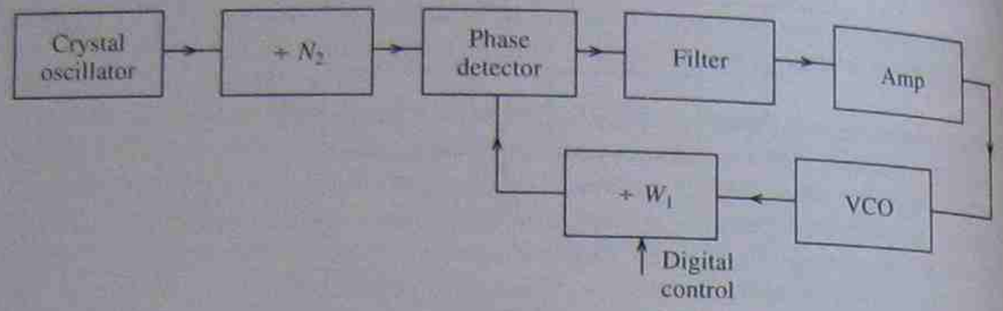


Fig. 6.17

Example 6.9

A radio station using 5 kHz channel separation broadcasts in the range 600–1200 kHz. Design a simple indirect synthesizer which would be suitable for this application if a 5 MHz crystal is used.

Solution

Since the channel separation is 5 kHz, each channel will be a multiple of this frequency. Hence taking $f_s = 5$ kHz,

$$N_1 = \frac{f_o}{f_s} = \frac{5 \times 10^6}{5 \times 10^3} = 1000$$

N_2 can be specified by assuming that the frequency will change by 5 kHz each time N_1 is incremented or decremented by 1: at 600 Hz

$$N = \frac{f_o}{f_s} = \frac{600}{5} = 120$$

and at 1200 kHz

$$N = \frac{f_o}{f_s} = \frac{1200}{5} = 240$$

A suitable system design might be as shown in Fig. 6.18. Note that the loop gain for a PLL is given by equation (6.7), and this will be changed by the frequency divider network to give

$$K_L = \frac{2\pi K_D K_A K_O}{N} \tag{6.24}$$

The loop gain is therefore reduced so that the other stages must have higher gain. This should be remedied by using linear amplifiers.

Prescaling

Because of the limitation of programmable dividers at much higher frequencies, it is not

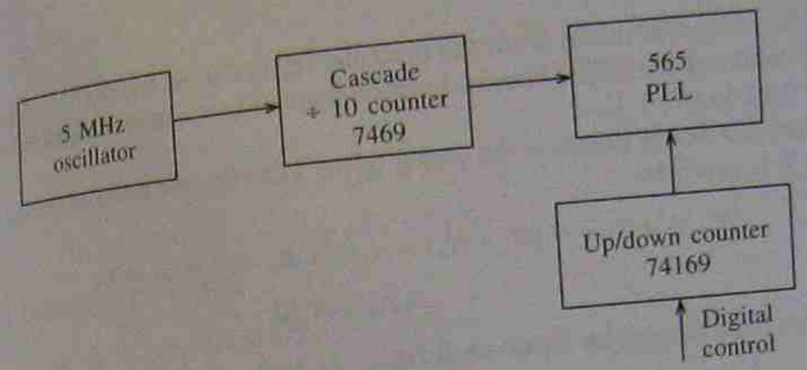


Fig. 6.18

possible to use the simple synthesizer design so far considered. The problem may be partially solved if a fixed-modulus divider is placed before N_1 in Fig. 6.15, but this means that the frequency can only be changed by a minimum amount depending on the value of the new fixed-modulus divider. A method currently used is the inclusion of a two-modulus prescaler similar to the one shown in Fig. 6.19. In this diagram the counter N_1 performs the same function as before, but the prescaler can divide by either N_3 or $(N_3 + 1)$. N_4 switches the prescaler between two different moduli and $N_1 > N_4$.

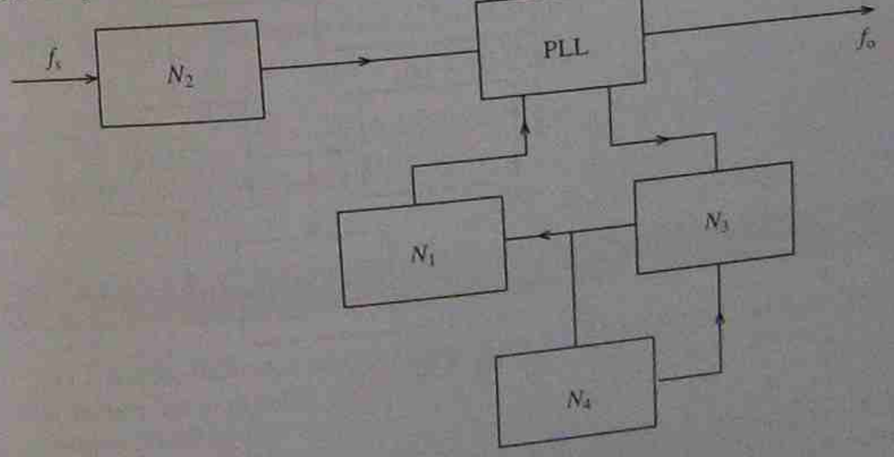


Fig. 6.19

Consider initially the prescaler set to the $(N_3 + 1)$ position and the N_4 counter reset. When the N_4 counter has received the appropriate number of transitions from the VCO the prescaler changes state to N_3. Hence the prescaler will divide by N_3 until the N_4 counter changes state again. Initially the prescaler is set to divide by $(N_3 + 1)$, hence this is the number of transitions required from the VCO to apply one count to the N_4 counter. This counter reaches zero after $N_4(N_3 + 1)$ transitions from pin 4 of the 565. Also the same pulses that go to the N_4 counter are also routed to the N_1 counter. When the N_4 counter reaches zero, the N_1 counter has reached $(N_1 - N_4)$. This value has to be greater than zero and this is why $N_1 > N_4$. The prescaler now switches to its other position and the next N_3 input from the VCO produces one transition from the prescaler output; this is repeated until the N_1 counter reaches zero. This counter begins with a count of $(N_1 + N_4)$ it must

receive $(N_1 - N_4)$ transitions from the prescaler. Hence there are $N_3(N_1 - N_4)$ changes from the output of the VCO. Finally, both counters reset (N_1 and N_4) and the prescaler switches back to $(N_4 + 1)$.

The total number of pulses at the output of the VCO for one pulse at the input of the 565 (pin 5) is given by

$$N_4(N_3 + 1) + N_3(N_1 - N_4) = N_4N_3 + N_4 + N_1N_3 - N_4N_3$$
$$= N_4 + N_1N_3 \tag{6.25}$$

Since f_o has been divided by equation (6.24),

$$f_o = (N_4 + N_1N_3)f_s \tag{6.26}$$

Example 6.10

A frequency synthesizer with the design shown in Fig. 6.20 has a prescaler ratio of 15 : 16. Determine the output frequency (f_o).

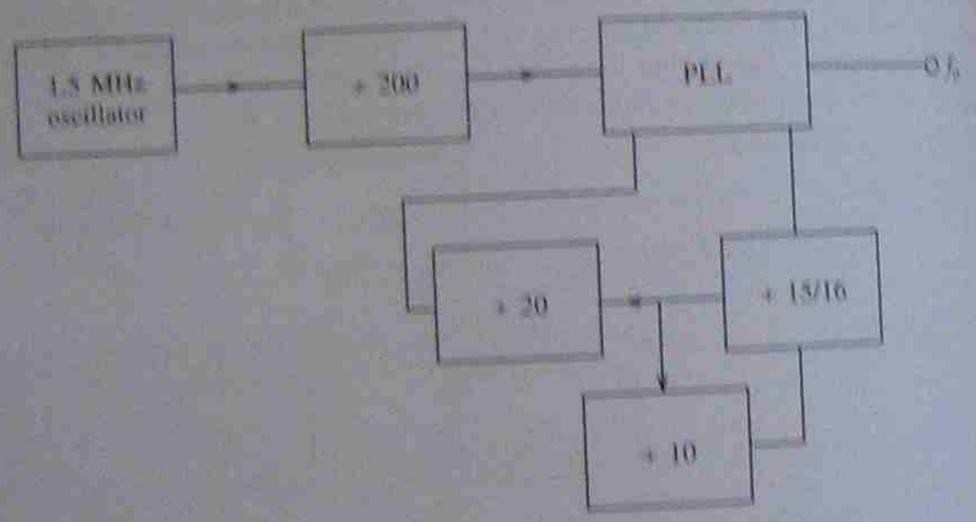


Fig. 6.20

Solution

$$f_o = (N_4 + N_1N_3)f_s$$
$$= (10 + 20 \times 15)\ \frac{1.5 \times 10^6}{200}$$
$$= \frac{310 \times 1.5 \times 10^6}{200}$$
$$= 2.325 \text{ MHz}$$

Example 6.11

A synthesizer uses a two-modulus prescaler with a ratio of 10 : 11. If the input signal to the PLL has to be 5 kHz and the output range has to be 500–900 kHz, determine suitable

Solution

For a two-modulus system assume N_1 is constant and N_4 is incremented by $(N_4 + 1)$. Initially,

$$f_{o1} = (N_4 + N_1N_3)f_s$$
$$= (N_4 + N_1N_3)5$$

If N_4 is incremented by 1, then

$$f_{o2} = (N_4 + 1 + N_1N_3)5$$
$$f_{o2} - f_{o1} = (N_4 + 1 + N_1N_3)5 - (N_4 + N_1N_3)5$$
$$= 5 \text{ kHz}$$

Hence the step size is the same as if no prescaler was used. The resolution is unchanged, and since the incoming signal is 400 kHz, $N_2 = 80$ for $f_s = 5$ kHz. For 500 kHz

$$f_o = (N_4 + N_1N_3)f_s$$
$$500 = (N_4 + N_1 \times 10)5$$
$$100 = N_4 + 10 \times N_1$$
$$N_4 = 100 - 10 \times N_1$$

As $N_1 > N_4$ select $N_1 = 9.5$, hence $N_4 = 5$. For 900 kHz

$$900 = (N_4 + 10 \times N_1)5$$
$$180 = (N_4 + 10 \times N_1)$$

As $N_1 > N_4$ select $N_1 = 19.5$, hence $N_4 = 15$.

6.8 Further problems

1. A PLL has the following element gains: $K_D = 0.4$ V/rad, $K_A = 4$ and $K_O = 30$ kHz/V. Determine the loop gain.
   Answer: 36 kHz/rad

2. A PLL has the following parameters: $K_A = 3$, $K_O = 45$ kHz/V, $K_D = 0.45$ V/rad and $f_o = 365$ kHz. If the input signal is 220 kHz and the loop is locked, determine:
   (a) the loop gain in kHz/rad;
   (b) the VCO output frequency;
   (c) the static phase error;
   (d) the lock range;
   (e) the maximum possible value of v_c.
   Answer: 60.75 kHz/rad, 365 kHz, 402 rad, 1113.1 kHz, 0.47 V

3. A PLL has to be compensated by using a lead-lag compensation network. If $\omega_0 = 260$ rad/s and $\omega_N = 10$ rad/s, determine the value of the filter components. Assume the output resistance (R_o) of the phase comparator is 20 kΩ and select $C = 0.22$ μF.
   Answer: $R_2 = 17.48$ kΩ, $R_1 = 417.1$ kΩ

4. A PLL is compensated by means of a lead-lag compensation network. If $\omega_h = 210$ rad/s and $\omega_l = 6$ rad/s, determine the values of the filter components assuming the phase comparator output resistance is 15 kΩ and the value of C is 47 nF. Also determine the component values if a phase lag compensation network was used with the same value of C.
Answer: $R_1 = 4.134$ MΩ, $R_2 = 101.32$ kΩ, $R_1 = 101.37$ kΩ

5. Figure 6.21 shows the characteristics of a PLL. The low-pass filter consists of an RC phase lag network having a cut-off frequency of 30 kHz and $C = 0.15$ μF. Determine:
(a) K_D, K_V, K_O, K_L;
(b) the values of R and C for the filter;
(c) the value of V_o, v and θ_e under lock conditions;
(d) the lock range.
Answer: 0.64 V/rad, 1.46, −15 kHz/V, 14 kHz/rad, 35 Ω, 0.667 V, −0.457 V, 0.713 rad, 44 kHz

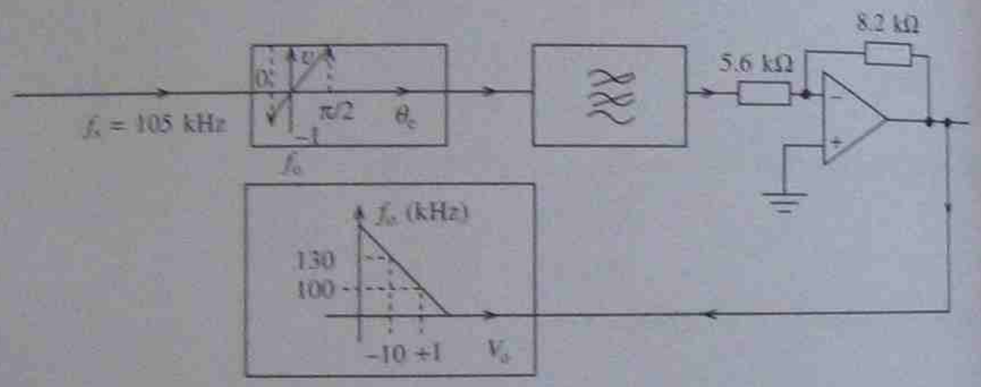


Fig. 6.21

6. Determine typical values for a 565 PLL wide-bandwidth application if $f_o = 1$ kHz, $f_L = \pm 800$ Hz, and $f_C = \pm 300$ Hz. Select $C_O = 250$ nF.
Answer: $R_1 = 101.37$ kΩ, $R_o = 1.2$ kΩ, $C_1 = 0.39$ μF, $V_C = \pm 5$ V, $R_2 = 17.6$ kΩ

7. A 565 PLL is used as a narrow-band application in order to correct for jitter in a data communication system. The parameters are $f_o = 1.2$ kHz, $f_L = \pm 600$ Hz and $f_C = \pm 500$ Hz. Calculate the values of the required components and also the loop gain when the amplifier gain is unity. Use a 150 nF capacitor for C_O and 9 nF for C_1.
Answer: $R_O = 1.67$ kΩ, $V_C = \pm 8$ V, $R_2 = 17.6$ kΩ, 2.52 kHz/rad

8. Design a circuit incorporating an HCC4046B CMOS PLL, to be used with the following parameters: $f_L = \pm 300$ kHz, $f_C = \pm 100$ kHz, and $f_o = 400$ kHz. Select $C_1 = 2$ nF and $C_2 = 4.7$ nF.
Answer: $R_1 = 375$ Ω, $R_3 = 508.5$ Ω, $V_{DD} = 10$ V

9. Design an indirect synthesizer which could be used in an FM broadcast system operating at 98–110 MHz. The channel separation is 1 MHz and a 20 MHz crystal is used.
Answer: $N_1 = 20$, $N_2 = 98$

10. Figure 6.22 shows a synthesizer which uses a two-modulus prescaler with a ratio of 8 : 9. Determine the output frequency and explain the operation of this type of synthesizer.
Answer: 14.9 MHz

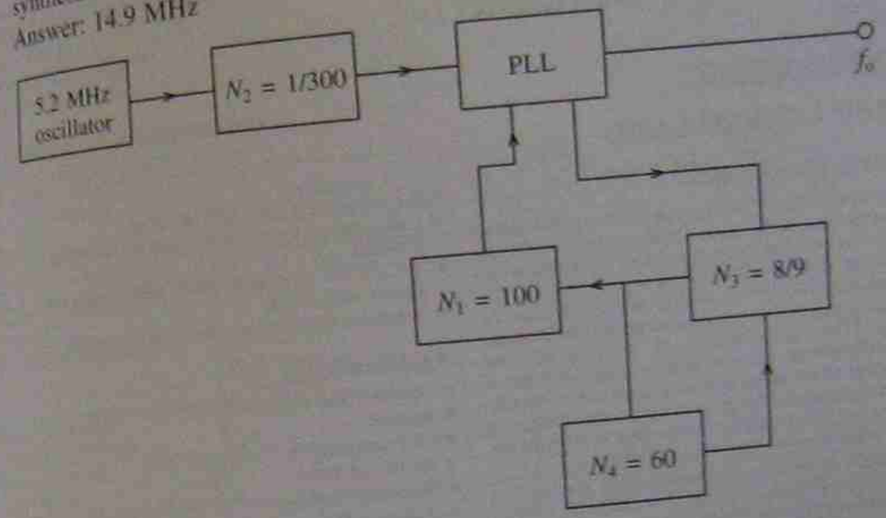


Fig. 6.22

11. A musical synthesizer uses a two-modulus prescaler with a ratio of 10 : 11. If the input signal to the PLL has to be 2.2 kHz and the output range is from 100 Hz to 22 kHz, determine appropriate counters for this application.

12. Explain how a PLL may be tested for free-running frequency, lock range and capture range. Give reasons why a spectrum analyser should not be used in this application.

Data sheets

National Semiconductor

May 1999

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

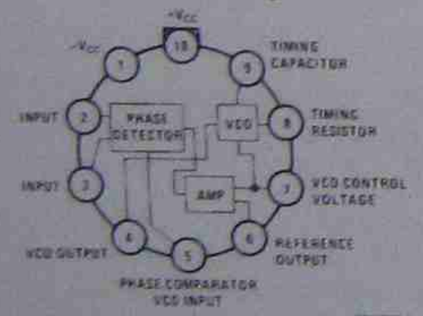
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

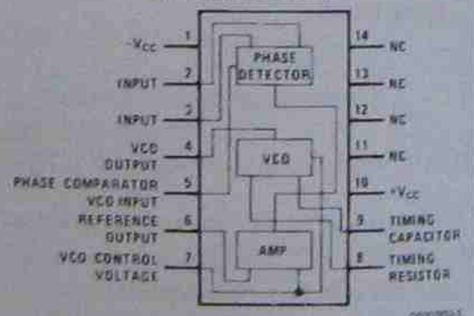
Connection Diagrams

Metal Can Package



Order Number LM565H
See NS Package Number H10C

Dual-In-Line Package



Order Number LM565CN
See NS Package Number N14A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 2)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

AC Test Circuit, T_A = 25°C, V_{CC} = ±6V

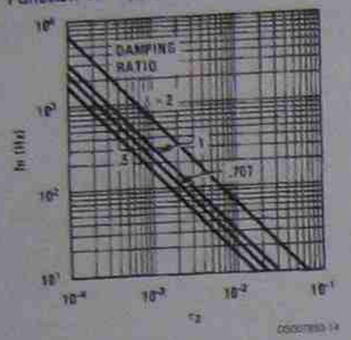
Parameter	Conditions	LM565 Min	LM565 Typ	LM565 Max	LM565C Min	LM565C Typ	LM565C Max	Units
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	−4V < V_2, V_3 < 0V	7	10			5		kΩ
VCO Maximum Operating Frequency	C_o = 2.7 pF	300	500		250	500		kHz
VCO Free-Running Frequency	C_o = 1.5 nF R_o = 20 kΩ f_o = 10 kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	f_o = 10 kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		µV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			0.68			0.68		V/radian

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

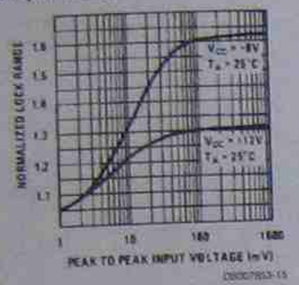
Note 2: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

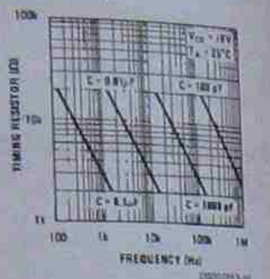
Power Supply Current as a Function of Supply Voltage



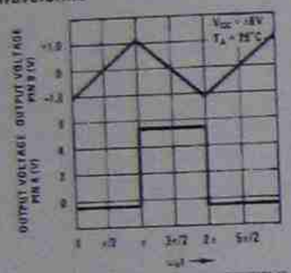
Lock Range as a Function of Input Voltage



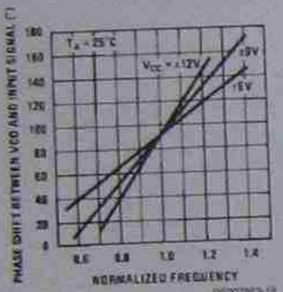
VCO Frequency



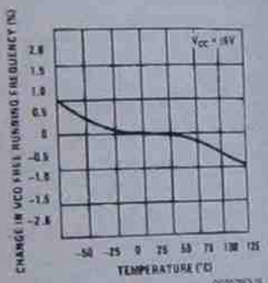
Oscillator Output Waveforms



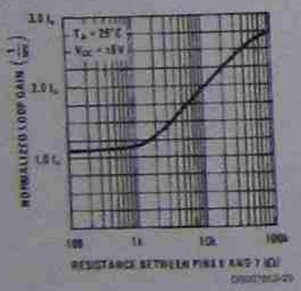
Phase Shift vs Frequency



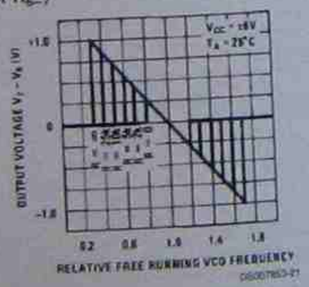
VCO Frequency as a Function of Temperature



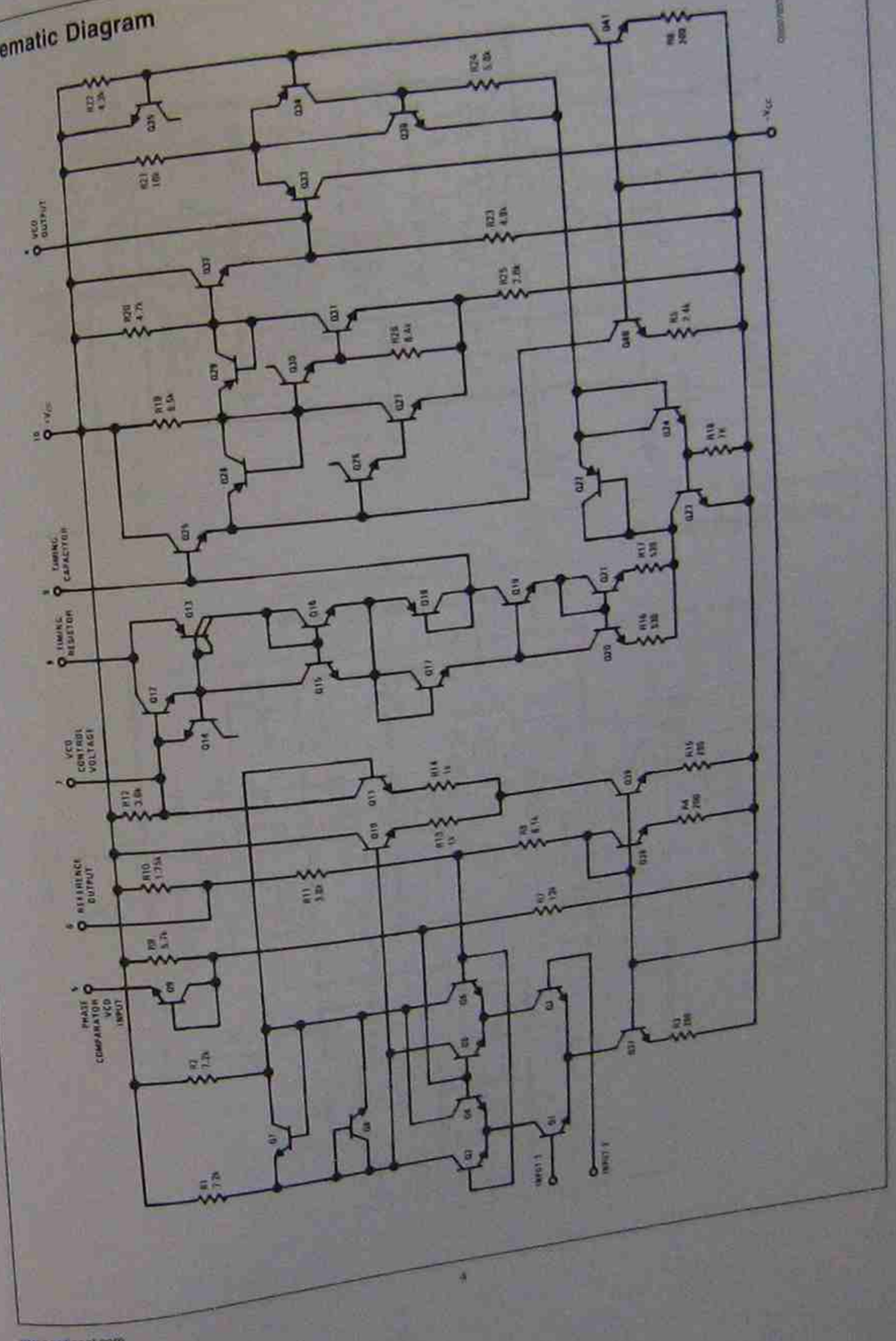
Loop Gain vs Load Resistance



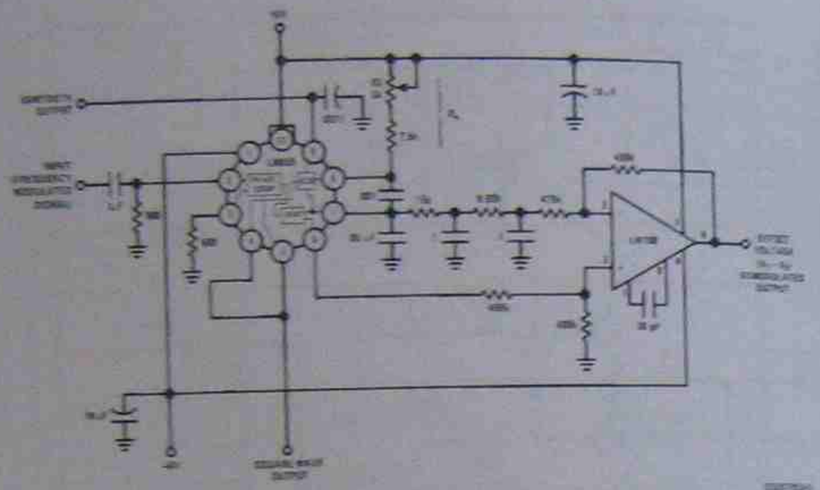
Hold in Range as a Function of R_{5-7}



Schematic Diagram



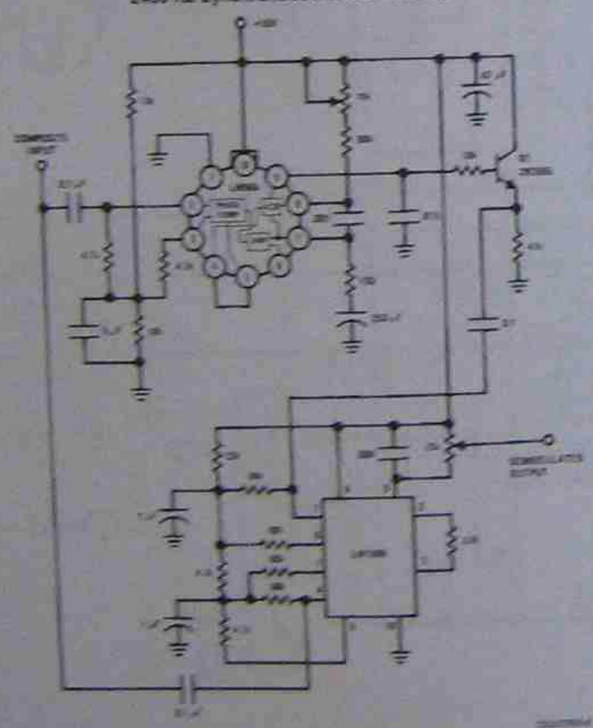
AC Test Circuit



Note 5: open for output offset voltage ($V_O - V_{OS}$) measurement.

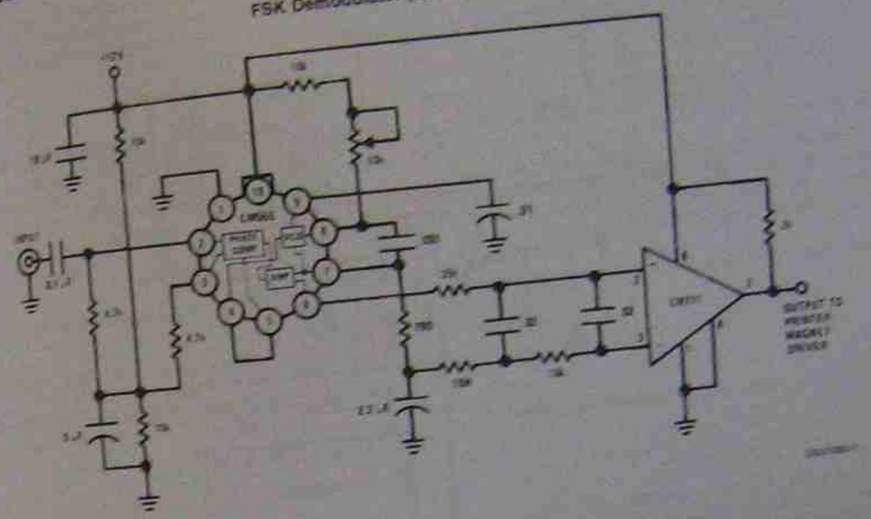
Typical Applications

2400 Hz Synchronous AM Demodulator

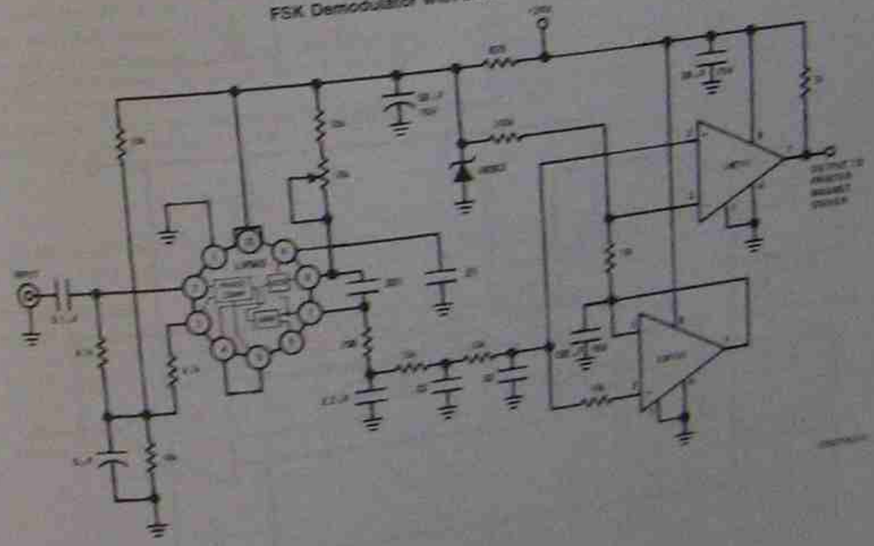


Typical Applications (Continued)

FSK Demodulator (2025–2225 cps)

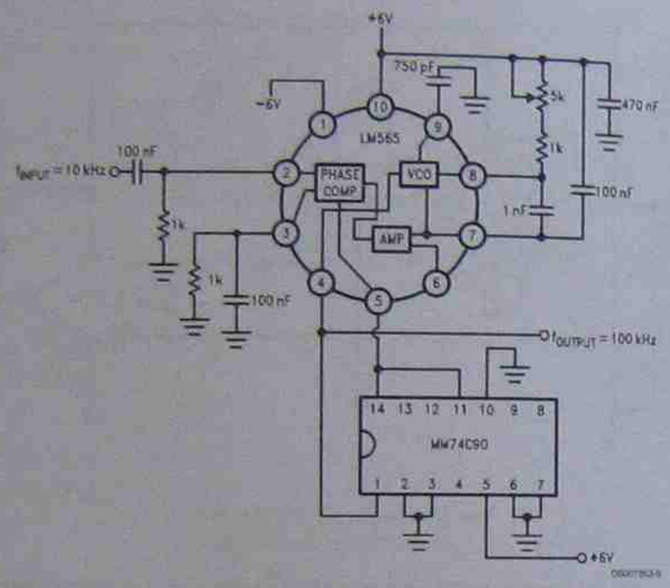


FSK Demodulator with DC Restoration

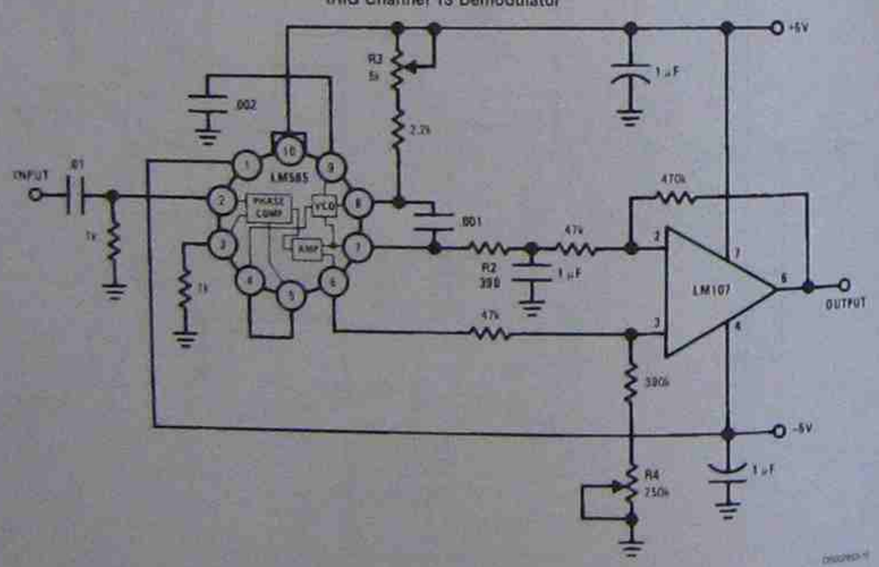


Typical Applications (Continued)

Frequency Multiplier (x10)



IRIG Channel 13 Demodulator



Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \approx \frac{0.3}{R_0 C_0}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo easy, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

K_o = oscillator sensitivity $\left(\frac{\text{radians/sec}}{\text{volt}}\right)$

K_D = phase detector sensitivity $\left(\frac{\text{volts}}{\text{radian}}\right)$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_C}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm \frac{8\, f_o}{V_C}$$

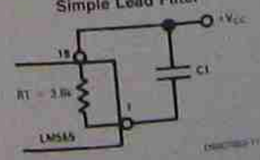
f_o = free running frequency of VCO

V_c = total supply voltage to the circuit

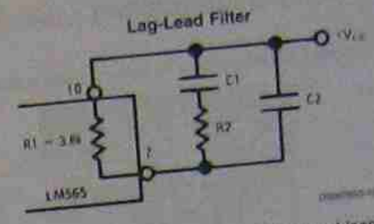
THE LOOP FILTER

In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lead Filter



Lag-Lead Filter



A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2}\sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

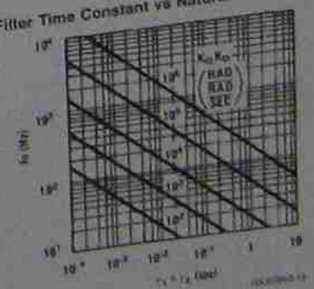
$$\tau_1 + \tau_2 = (R_1 + R_2) C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi \tau_2 f_n$$

These two equations are plotted for convenience.

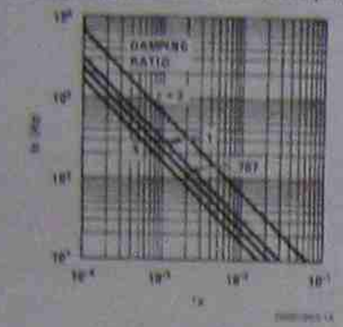
Filter Time Constant vs Natural Frequency



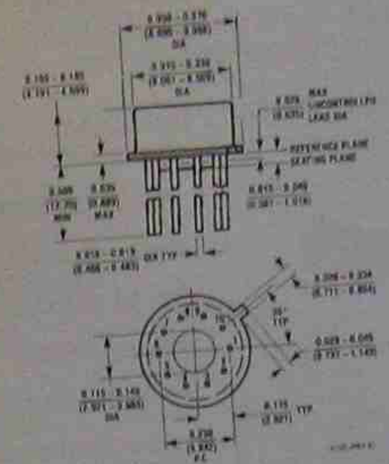
Applications Information (Continued)

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\ C_1$.

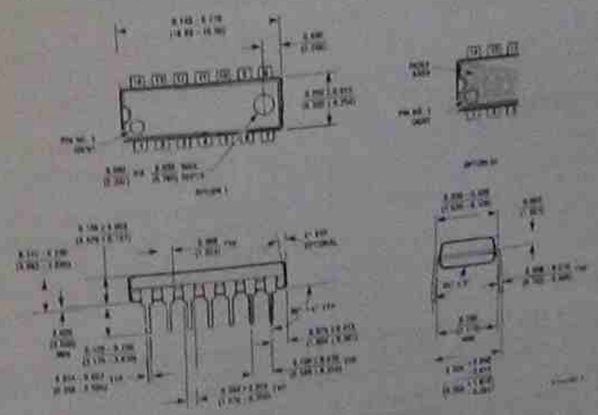
Damping Time Constant vs Natural Frequency



Physical Dimensions inches (millimeters) unless otherwise noted



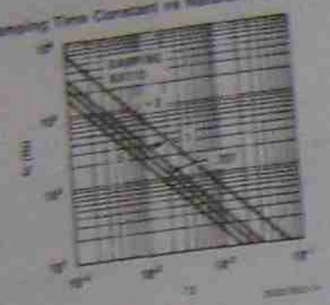
Metal Can Package (H)
Order Number LM565H
NS Package Number H10C



Dual-In-Line Package (N)
Order Number LM565CN
NS Package Number N14A

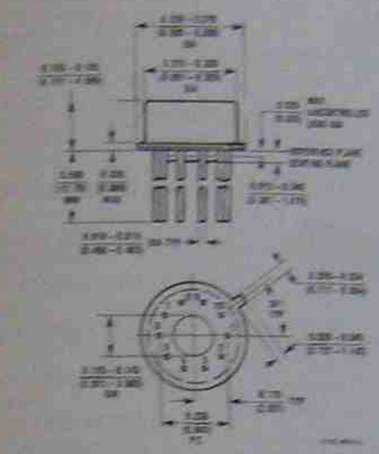
Applications Information (Continued)

Damping Time Constant vs Natural Frequency

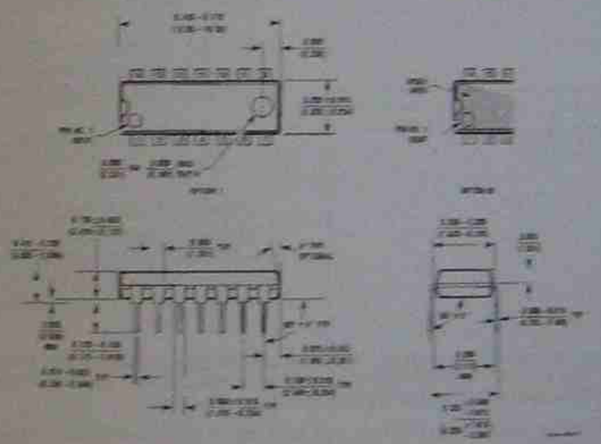


Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of ripple. In general $C_2 \leq 0.1\ C_1$.

Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
Order Number LM565H
NS Package Number H10C



Dual-In-Line Package (N)
Order Number LM565CN
NS Package Number N14A

Notes

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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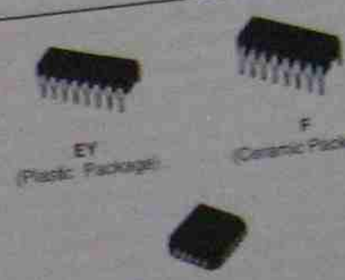
SGS-THOMSON* MICROELECTRONICS

HCC/HCF4046B

MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- VERY LOW POWER CONSUMPTION : 100µW (TYP.) AT VCO f_o = 10kHz, V_{DD} = 5V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT V_{DD} = 10V
- LOW FREQUENCY DRIFT : 0.06%/°C (typ.) AT V_{DD} = 10V
- CHOICE OF TWO PHASE COMPARATORS :
  1) EXCLUSIVE - OR NETWORK
  2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY : 1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



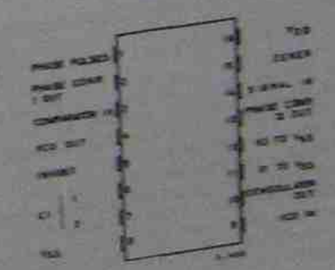
EY (Plastic Package)

F (Ceramic Package)

C1 (Chip Carrier)

ORDER CODES :
HCC4046BF HCF4046BEY
HCF4043BC1

PIN CONNECTIONS



DESCRIPTION

The **HCC4046B** (extended temperature range) and **HCF4046B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package. The **HCC/HCF4046B** COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

June 1989

*Now known as STMicroelectronics

1/12

VCO Section

The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{10}\ \Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (Rs) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CD/MOS frequency dividers such as the **HCC/HCF4024B**, **HCC/HCF4018B**, **HCC/HCF4020B**, **HCC/HCF4022B**, **HCC/HCF4029B** and **HBC/HBF4059A**. One or more **HCC/HCF4018B** (Presettable Divide-by-N Counter) or **HCC/HCF4029B** (Presettable Up/Down Counter) or **HBC/HBF4059A** (Programmable Divide-by-"N" Counter), together with the **HCC/HCF4046B** (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CD/MOS logic levels (logic "0" ≤ 30 % ($V_{DD} - V_{SS}$), logic "1" ≥ 70 % ($V_{DD} - V_{SS}$)). For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_c$). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CD/MOS phase-locked-loop employing phase-comparator I in locked condition of f_0 are shown in fig. (b). Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3-state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time and both the n- and p-drivers OFF (3-state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal rises after the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage of the low-pass filter connected to this comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating lock condition. Thus, for phase comparator I, a phase difference exists between signal and comparator

input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a CD/MOS PLL employing phase comparator II in a locked condition.

Figure a : Phase-Comparator I Characteristics at Low-Pass Filter Output.

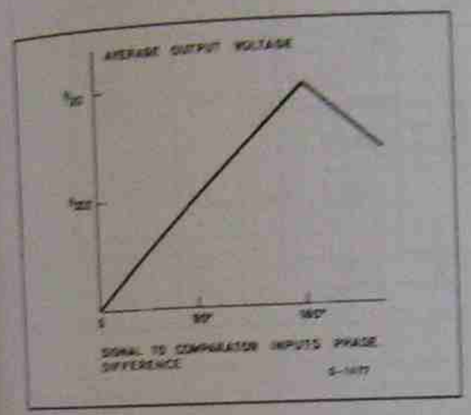


Figure b : Typical Waveforms for COS/MOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of f_0.

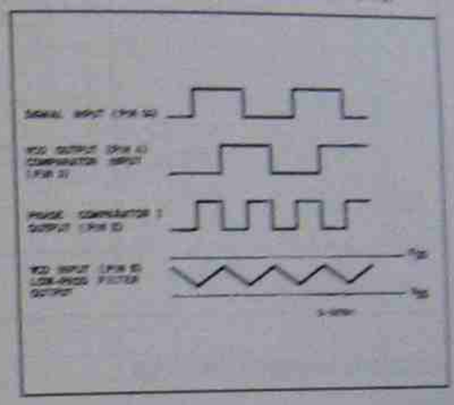
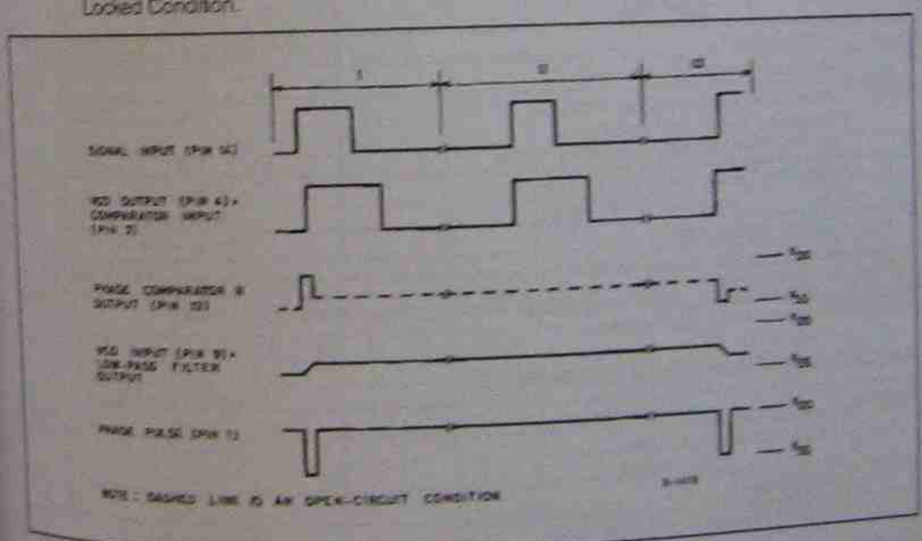
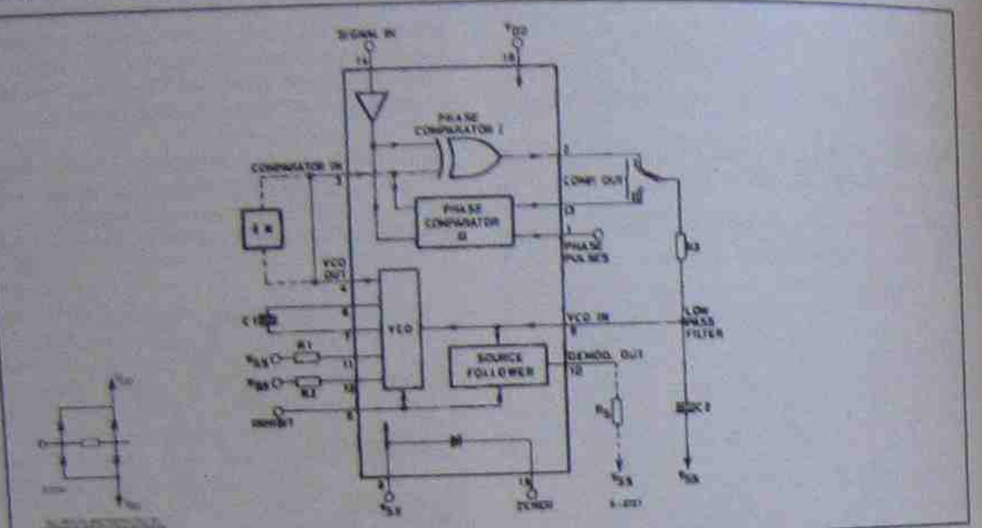


Figure c : Typical Waveforms For COS/MOS Phase-locked Loop Employing Phase Comparator II in Locked Condition.



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}*	Supply Voltage : **HCC** Types **HCF** Types	− 0.5 to + 20 − 0.5 to + 18	V V
V_I	Input Voltage	− 0.5 to V_{DD} + 0.5	V
I_I	DC Input Current (any one input)	± 10	mA
P_{tot}	Total Power Dissipation (per package) Dissipation per Output Transistor for T_{op} = Full Package-temperature Range	200 100	mW mW
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C
T_{stg}	Storage Temperature	− 65 to + 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

* All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature : **HCC** Types **HCF** Types	− 55 to + 125 − 40 to + 85	°C °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions V_I (V)	Test Conditions V_O (V)	Test Conditions $\|I_O\|$ (μA)	Test Conditions V_{DD} (V)	Value T_{Low}* Min.	Value T_{Low}* Max.	Value 25°C Min.	Value 25°C Typ.	Value 25°C Max.	Value T_{High}* Min.	Value T_{High}* Max.	Unit
VCO SECTION														
V_{OH}	Output High Voltage		0/ 5		< 1	5	4.95		4.95	5		4.95		V
			0/10		< 1	10	9.95		9.95	10		9.95		
			0/15		< 1	15	14.95		14.95	15		14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	− 2		− 1.6	− 3.2		− 1.15		mA
			0/ 5	4.6		5	− 0.64		− 0.51	− 1		− 0.36		
			0/10	9.5		10	− 1.6		− 1.3	− 2.6		− 0.9		
			0/15	13.5		15	− 4.2		− 3.4	− 6.8		− 2.4		
		HCF Types	0/ 5	2.5		5	− 1.53		− 1.36	− 3.2		− 1.1		
			0/ 5	4.6		5	− 0.52		− 0.44	− 1		− 0.36		
			0/10	9.5		10	− 1.3		− 1.1	− 2.6		− 0.9		
			0/15	13.5		15	− 3.6		− 3.0	− 6.8		− 2.4		
I_{OL}	Output Sink Current	HCC Types	0/ 5	0.4		5	0.64		0.51	1		0.36		
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18		Any Input	18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		± 10^{-5}	± 0.3		± 1	
PHASE COMPARATOR SECTION														
I_{DD}	Total Device Current Pin 14 = Open Pin 5 = V_{DD}		0/ 5			5		0.1		0.05	0.1		0.1	mA
			0/10			10		0.5		0.25	0.5		0.5	
			0/15			15		1.5		0.75	1.5		1.5	
			0/20			20		4		2	4		4	
	Pin 14 = V_{SS} or V_{DD} Pin 5 = V_{DD}	HCC Types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
I_{OH}	Output Drive Current	HCC Types	0/ 5	2.5		5	− 2		− 1.6	− 3.2		− 1.15		mA
			0/ 5	4.6		5	− 0.64		− 0.51	− 1		− 0.36		
			0/10	9.5		10	− 1.6		− 1.3	− 2.6		− 0.9		
			0/15	13.5		15	− 4.2		− 3.4	− 6.8		− 2.4		
		HCF Types	0/ 5	2.5		5	− 1.53		− 1.36	− 3.2		− 1.1		
			0/ 5	4.6		5	− 0.52		− 0.44	− 1		− 0.36		
			0/10	9.5		10	− 1.3		− 1.1	− 2.6		− 0.9		
			0/15	13.5		15	− 3.6		− 3.0	− 6.8		− 2.4		

* T_{Low} = − 55°C for **HCC** device : − 40°C for **HCF** device.
* T_{High} = + 125°C for **HCC** device : + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter		Test Conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Value T_{Low}* Min.	Max.	25°C Min.	Typ.	Max.	T_{High}* Min.	Max.	Unit
I_{OL}	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{IH}, I_{IL}	Input Leakage Current (except pin 14)	HCC Types	0/18	Any Input		18		± 0.1		$± 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$± 10^{-5}$	± 0.3		± 1	
I_{OUT}	3-state Leakage Current	HCC Types	0/18	0/18		18		± 0.4		$± 10^{-4}$	± 0.4		± 12	μA
		HCF Types	0/15	0/15		15		± 1.0		$± 10^{-4}$	± 1.0		± 7.5	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{Low} = −55°C for HCC device: −40°C for HCF device.
* T_{High} = + 125°C for HCC device: +85°C for HCF device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V min. with V_{DD} = 15V.

ELECTRICAL CARACTERISTICS (T_{amb} = 25 °C)

Symbol	Parameter	Test Conditions	V_{DD} (V)	Value Min.	Typ.	Max.	Unit
VCO SECTION							
P_D	Operating Power Dissipation	f_O = 10 KHz R1 = 10 MΩ R2 = ∞ $V_{COIN} = \frac{V_{DD}}{2}$	5		70	140	μW
			10		800	1600	
			15		3000	6000	
f_{max}	Maximum Frequency	R1 = 10 KΩ C1 = 50 pF R2 = ∞ $V_{COIN} = V_{DD}$	5	0.3	0.6		MHz
			10	0.6	1.2		
			15	0.8	1.6		
		R1 = 5 KΩ n C1 = 50 pF R2 = ∞ $V_{COIN} = V_{DD}$	5	0.5	0.8		
			10	1	1.4		
			15	1.4	2.4		
	Center Frequency (f_O) and Frequency Range f_{max} - f_{min}	Programmable with external components R1, R2 and C1					
	Linearity	V_{COIN}=2.5V ± 0.3 R1=10 KΩ	5		1.7		%
		V_{COIN}=5V ± 1 R1=100 KΩ	10		0.5		
		V_{COIN}=5V ± 0.5 R1=400 KΩ	10		4		
		V_{COIN}=7.5V ± 1.5 R1=100 KΩ	15		0.5		
		V_{COIN}=7.5V ± 5 R1=1 MΩ	15		7		
	Temperature Frequency Stability (no frequency offset) f_{min} = 0		5		±0.12		%/°C
			10		±0.04		
			15		±0.015		
	Temperature Frequency Stability (frequency offset) f_{min} ≠ 0		5		±0.09		
			10		±0.07		
			15		±0.03		
Vco	Output Duty Cycle		5, 10, 15		50		%
t_{THL} t_{TLH}	VCO Output Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
	Source Follower Output (demodulated Output): Offset Voltage V_{COIN} - V_{DEM}	R_S > 10 KΩ	5, 10, 15		1.8	2.5	V
	Source Follower Output (demodulated Output): Linearity	R_{SH}=100 KΩ V_{COIN}=2.5(0.3)V	5		0.8		%
		R_{SH}=300 KΩ V_{COIN}=5(1.5)V	10		0.7		
		R_{SH}=500 KΩ V_{COIN}=7.5(1.5)V	15		0.9		
V_Z	Zener Diode Voltage	I_Z = 50 μA		4.45	5.5	7.5	V
R_Z	Zener Dynamic Resistance	I_Z = 1 mA			40		Ω
PHASE COMPARATOR SECTION							
R14	Pin 14 (signal in) Input Resistance		5	1	2		MΩ
			10	0.2	0.4		
			15	0.1	0.2		
	A.C. Coupled Signal Input Voltage Sensitivity * (peak to peak)	f_{in} = 100 KHz sine wave	5	150	360		mV
			10	330	660		
			15	900	1800		

ELECTRICAL CHARACTERISTICS (continued)

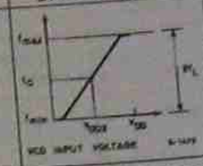
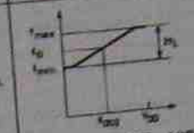
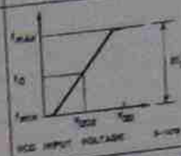
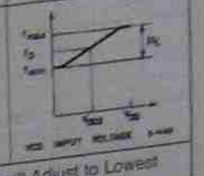
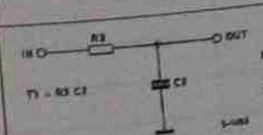
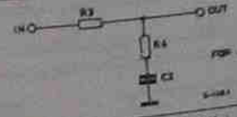
Symbol	Parameter	Test Conditions		Value			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
PHASE COMPARATOR SECTION (cont'd)							
T_{PHL}	Propagation Delay Time High to Low Level Pins 14 to 13		5	225	450		ns
			10	100	200		
			15	65	130		
T_{PLH}	Propagation Delay Time Low to High, Level		5		350	700	ns
			10		150	300	
			15		100	200	
T_{PHZ}	Propagation Delay Time 3-state High Level to High Impedance Pins 14 to 13		5		225	450	ns
			10		100	200	
			15		65	130	
T_{PLZ}	Low Level to High Impedance		5		285	570	ns
			10		130	260	
			15		95	190	
t_r, t_f	Input Rise or Fall Time Comparetor Pin 3		5			50	µs
			10			1	
			15			0.3	
	Signal Pin 14		5			500	µs
			10			20	
			15			2.5	
T_{THL}, T_{TLH}	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	

* For sine wave the frequency must be greater than 10KHz for Phase Comparator II.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the **HCC/HCF 4046B** in a Phase-Locked-Loop system. The selected external components must be within the following ranges :

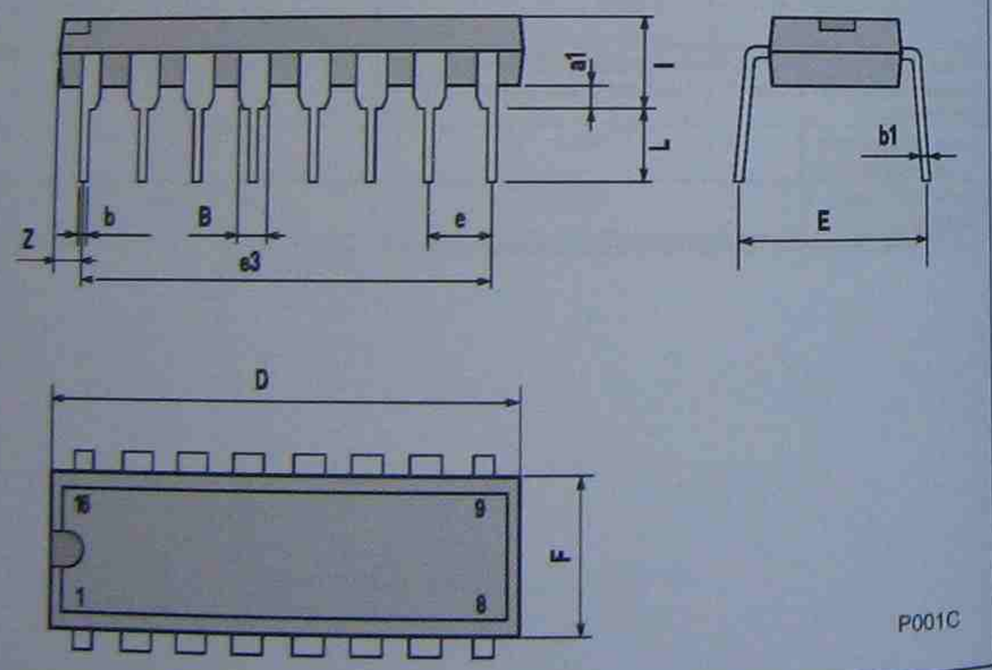
$5k\Omega \leq R1, R2, R_S \leq 1M\Omega$ $\quad C1 \geq 100pF$ at $V_{DD} \geq 5V$ $\quad C1 \geq 50pF$ at $V_{DD} \geq 10V$

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL System will Adjust to centre frequency f_o		VCO in PLL System will Adjust to Lowest Operating Frequency f_{min}	
Frequency Lock Range, 2 f_L	2 f_L = full VCO frequency range 2 $f_L = f_{max} - f_{min}$			
Frequency Capture Range, 2 f_C			$f_C = f_L$	
Loop Filter Component Selection				
Phase Angle Between Signal and Comparator	90° at Centre Frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

* G.S. Moschytz "miniaturized RC filters using phase Lockedloop" BSTJ, may 1965

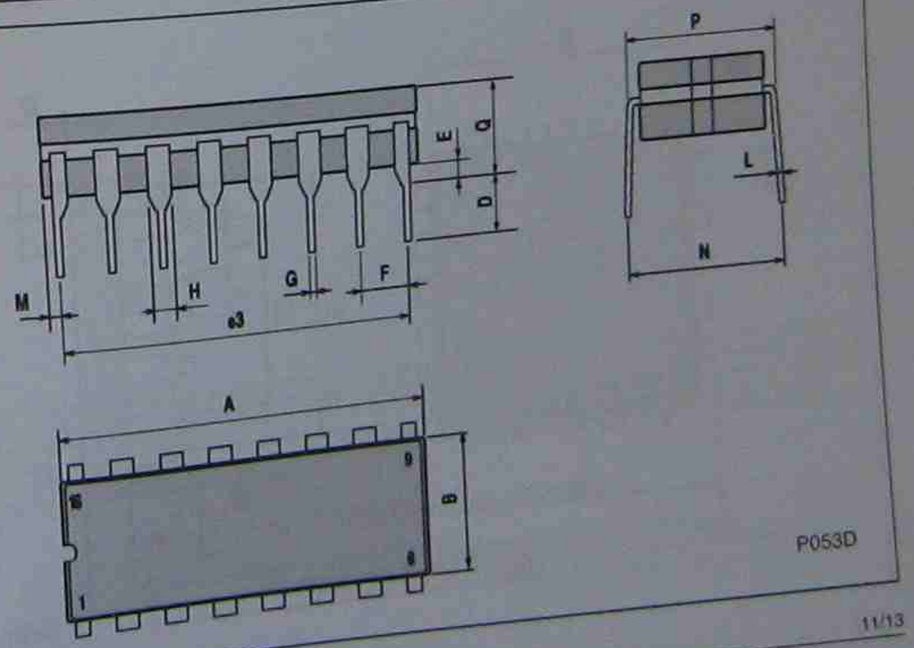
Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



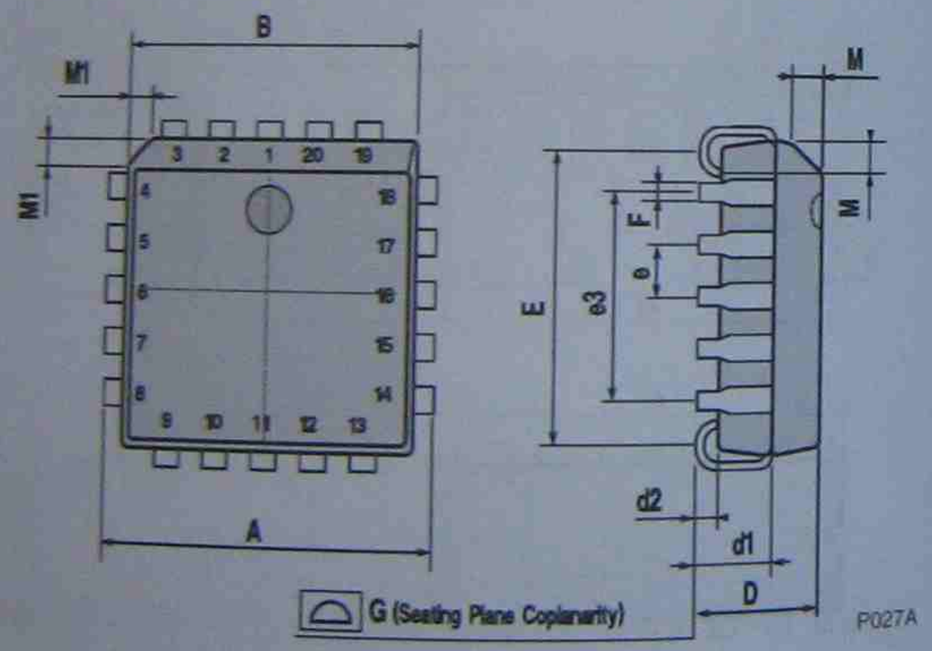
Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.69		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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7

Microwave devices and components

7.1 Introduction

A transmission line is a system of conductors which connects two points by means of electromagnetic energy which travels along the system. A system may include wires which carry 240 V/50 Hz mains supplies to consumers, or it may consist of lines which feed thousands of watts to a transmitting antenna. There are various kinds of transmission lines in use – the twisted pair, twin lead and coaxial, to mention a few. Twin-wire lines are often used for carrying radio frequency power to transmitters, while coaxial cables are commonly employed for low-power applications such as coupling receivers to their antennas.

Consider Fig. 7.1 in which a transmission line is connected between a generator and a load. In this circuit a section of transmission line is used and takes on the characteristics of a T-network. The components shown are not lumped components connected into the transmission line as such, but inherent parameters which manifest themselves when energy is propagated along the transmission line.

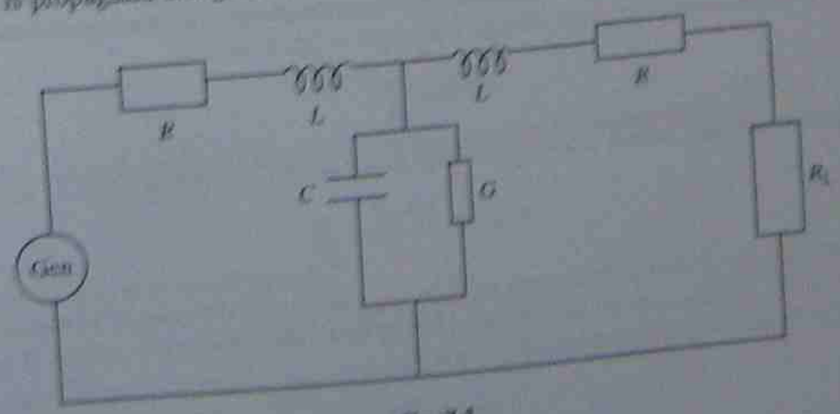


Fig. 7.1

The wave which moves along the transmission line is known as a travelling wave; as it moves from generator to load the capacitance of the line is charged up and the moving charges cause magnetic energy to be stored. Because of this the line does not appear as an open circuit to the generator but presents a finite value of impedance known as the characteristic impedance (Z_o) which is connected across the generator terminals. Each type of transmission line has its own characteristic impedance regardless of the length of the line; a symmetrical T-network like that in Fig. 7.1 is terminated in its characteristic impedance, equal to the network's characteristic impedance. This is irrespective of how many T-networks are connected. Obviously the loss in the line is due to the resistance (R) and the conductance (G).

From Fig. 7.1 there are four parameters connected with such a line: the resistance (R) which is dependent upon the dimensions of the line and its resistivity; the inductance (L) caused by the circular magnetic field around the conductors and dependent on the conductors' separation, radii and permeability; the capacitance due to the electric field between the conductors, also dependent on the dimensions of the conductors and the permittivity; and finally, the conductance due to the insulation of the line which allows some current to leak from one conductor to another. All these constants are referred to as the primary constants.

7.2 Phase delay and propagation velocity

If the losses are assumed to be small, R and G can be removed from Fig. 7.1, so that it simply becomes an LC low-pass filter network. As with any conductor, a current passes through the inductance of this conductor and charges up C. This takes time, and this time will increase as more and more sections of line are added (its length is increased). There will therefore be a phase difference between the generator voltage and the voltage at any point along the line.

The phase delay parameter (β) is given by

$$\beta = \omega\sqrt{LC} \text{ (rad/m)} \tag{7.1}$$

where L and C are the inductance and capacitance per metre of the line. Also as the wavelength (λ) on the line is the distance between two points with the same phase (360° or 2 π radians apart), the phase change per metre is $2\pi/\lambda$. Hence

$$\lambda = \frac{2\pi}{\beta} \tag{7.2}$$

The **phase velocity**, which is always strictly less than the velocity of light, is given by

$$V_p = f\lambda = \frac{2\pi f}{\beta} = \frac{\omega}{\beta} \tag{7.3a}$$

Another velocity, known as the **group velocity** (v_g), deals with the velocity of transferring energy along the line. As the line contains inductance and capacitance, energy is stored along its length and is transferred at velocity

$$V_g = \frac{d\omega}{d\beta} \tag{7.3b}$$

This velocity is normally associated with the group movement of several waveforms which have different phase velocities and is generally applied to pulses which consist of numerous frequencies having different phase relationships. Phase and group velocities are important in microwave devices.

7.3 The propagation constant and secondary constants

As current flows in a transmission line its value decreases because of attenuation in the line. If I_1 is the initial current at the generator and I_2 is the current (say) 1 km along the line towards the load, then the attenuation, which is a logarithmic decay, is given by

$$\frac{I_1}{I_2} = e^{\gamma}$$

The propagation coefficient γ is a complex quantity given by $\gamma = \alpha + j\beta$, where α is known as the attenuation constant and β is the phase-shift coefficient. If n sections of transmission line are connected then

$$\frac{I_G}{I_L} = e^{n\gamma} \tag{7.4}$$

where I_G is the current at the generator end and I_L is the current at the load end. Hence

$$\frac{I_G}{I_L} = e^{n(\alpha+j\beta)} = e^{n\alpha}\angle n\beta$$

from which

$$I_L = I_G e^{-n\gamma} = I_G e^{-n\alpha}\angle -n\beta \tag{7.5}$$

The receiving end voltage is similarly given by

$$V_L = V_G e^{-n\alpha}\ \angle -n\beta \tag{7.6}$$

Note that Z_o, γ, α and β are known as the secondary constants and impedance and they may be expressed in terms of the primary constants. A full analysis of the following expressions may be found in other texts. The characteristic impedance is given by

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{7.7}$$

Note that this is for a lossy line; for a lossless line the expression becomes

$$Z_o = \sqrt{\frac{L}{C}} \tag{7.8}$$

Also the propagation coefficient is

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{7.9}$$

Once again this is for a lossy line; for a lossless line this equation is

$$\gamma = j\omega\sqrt{LC} \tag{7.10}$$

The characteristic impedance of the line may also be given by

$$Z_0 = \sqrt{Z_{oc} Z_{sc}} \qquad (7.11)$$

where Z_{oc} and Z_{sc} are the open-circuit and short-circuit impedance of the line, respectively. This is a practical method of obtaining the characteristic impedance as Z_{oc} and Z_{sc} can both be easily measured.

7.4 Transmission line distortion

The waveform at the receiving end of a transmission line may be distorted for many reasons, but the most common problems are the following:

(a) The terminating impedance is not the same as the characteristic impedance. As the characteristic impedance varies with frequency for a lossy line (equation (7.7)), the terminating impedance may not change with frequency in the same way. If the characteristic impedance is to remain the same for the complete frequency operating range, the condition $LG = CR$ must be achieved.

(b) The attenuation (and thus the propagation coefficient) of a line varies with frequency (equation (7.9)), thus different frequencies are attenuated by different amounts. This is avoided if $LG = CR$ and when this is the case,

$$\alpha = \sqrt{RG} \qquad (7.12)$$

and

$$\beta = \omega\sqrt{LC}$$

Hence the attenuation coefficient is independent of frequency.

(c) The velocity of propagation varies with frequency. Once again if $LG = CR$ then the velocity of propagation is given by

$$v = \frac{1}{\sqrt{LC}} \qquad (7.14)$$

which is independent of frequency, as will be the time delay.

If the above conditions are applied, i.e. $LG = CR$, then distortion will be kept at a minimum. However, in practice $R/L \gg G/C$. Also the inductance is usually low and the capacitance is large. For the condition $LG = CR$ to be achieved either L or G has to be increased since C and R cannot really be altered. Also if G is increased the attenuation and power losses will increase. Thus L is generally altered, and when this occurs **loading** is said to take place. In practice, this is achieved either by inserting inductance at intervals along the line or by wrapping the conductors with high-permeability sheaths.

7.5 Wave reflection and the reflection coefficient

It has already been mentioned that for a lossless line equation (7.1) applies. If the line is increased in length the inductance increases, and the capacitance increases because the capacitance area is greater. So overall the LC ratio remains the same.

When the load and generator impedances are both equal to the characteristic impedance of the line, maximum energy is absorbed by the load. However, when a line is not terminated in its own impedance the load absorbs only a portion of the energy, reflecting the remainder back along the line. Standing waves of voltage and current are set up, their amplitude depending on the extent of the mismatch. The standing waves are smaller in amplitude than the generator signal because the resistance absorbs a portion of the energy, sending the remainder back as reflected waves.

It is instructive at this point to explain what is meant by a standing wave. A wave travelling along a transmission line consists of electric and magnetic components, and energy is stored in the magnetic field of the line inductance ($\frac{1}{2}LI^2$) and the electric field of the line capacitance ($\frac{1}{2}CV^2$). This energy is interchanged between the magnetic and electric fields and causes the transmission of the electromagnetic energy along the line.

When a wave reaches an open-circuited termination the magnetic field collapses since the current is zero. The energy is not lost but is converted into electrical energy adding to that already caused by the existing electric field. Hence the voltage at the termination doubles, and this increased voltage causes the reflected wave which moves back along the line in the reverse direction.

The same reasoning can be applied to a short-circuited termination. In this case the electric field collapses at the termination and its energy changes to magnetic energy. This results in a doubling of the current.

Extreme resistance loading conditions are shown in Fig. 7.2. In Fig. 7.2(a) the line is terminated in an open circuit and, regardless of the length of line, the current and voltage conditions at the termination end are the same. In an open circuit the current is a minimum and so the impedance and voltage are maximum. In Fig. 7.2(b) the line termination is a short circuit resulting in maximum current, while the impedance and voltage are minimum.

Figures 7.3(a) and 7.3(b) show terminations in pure capacitance and pure inductance, respectively. In Fig. 7.3(a) all of the energy is reflected because a capacitor does not absorb energy. The relative phases of the waves shift according to the reactance and the line impedance. It is assumed in this case that the capacitive reactance equals the characteristic impedance simulating a phase condition of 45°.

At the termination end of the line the current and voltage arrive in phase, but due to the current through Z_c and Z_0 in series, the current leads by 45° while the voltage lags by 45°. So although current and voltage arrive in phase they are reflected 90° out of phase, as shown by the standing waves.

The voltage standing wave is a minimum at a point 2.0 from the termination end when $X_c = Z_0$. When X_c is greater the arrangement acts more like an open circuit and the minimum voltage point moves further away from the termination end. When X_c is less than Z_0 it is more like a short circuit, and the voltage minimum is closer to the end.

In Fig. 7.3(b) the line is terminated in its inductance and the waveforms occur when $X_c = Z_0$. Conditions are similar to the capacitance case, except that the phase shifts occur in the opposite direction. The shift is again 45° but the waveforms at the termination end

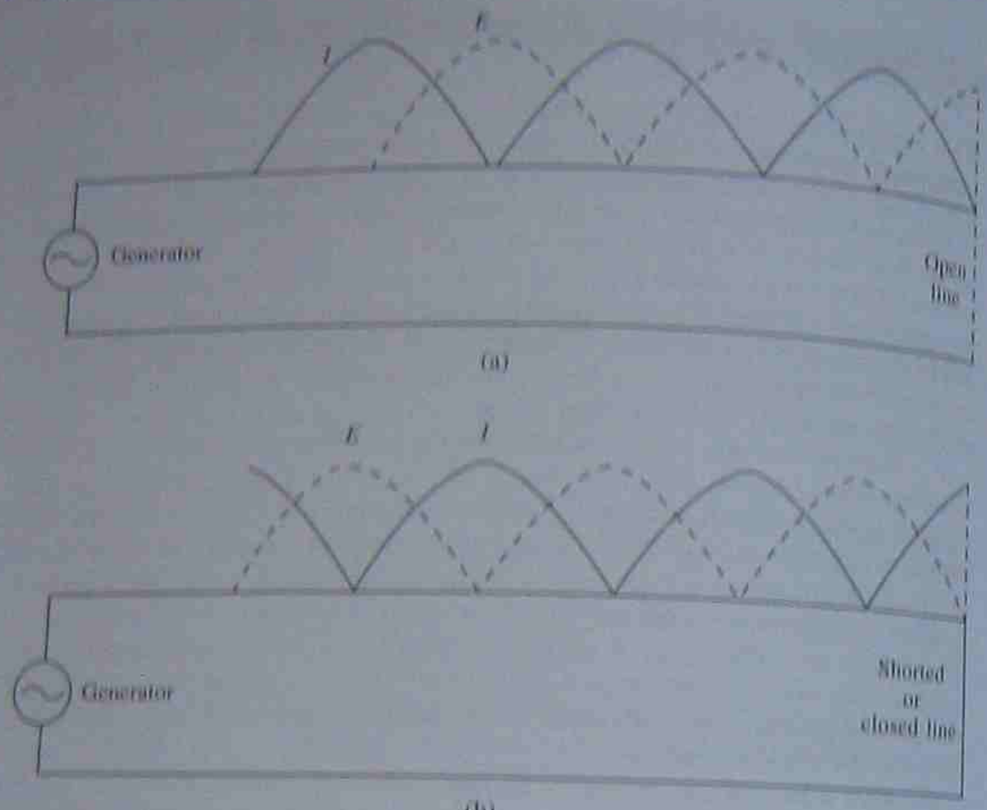


Fig. 7.2

are reversed. The current minimum now occurs at $\lambda/8$ from the end, whereas in Fig. 7.3(a) the voltage minimum occurred at this point.

If X_L is increased the condition is more similar to an open circuit and the current minimum moves toward the termination end, while a decrease in X_L moves the waves in the opposite direction.

A variety of conditions may be obtained using either an open-circuited or short-circuited transmission line cut to the desired length. This can simulate such conditions as series and parallel resonance and pure capacitance and inductance.

The reflection coefficient is an indication of amplitudes of the incident and reflected currents (I_i, I_r) and voltages (V_i, V_r). It is given in several forms, and once again the analysis of these formulae can be found in most common texts dealing with transmission lines. One form is

$$\frac{I_r}{I_i} = \frac{Z_0 - Z_L}{Z_0 + Z_L} = \rho \tag{7.15}$$

Another form relates the voltages and currents

$$\frac{V_r}{V_i} = -\frac{I_r}{I_i} = \rho \tag{7.16}$$

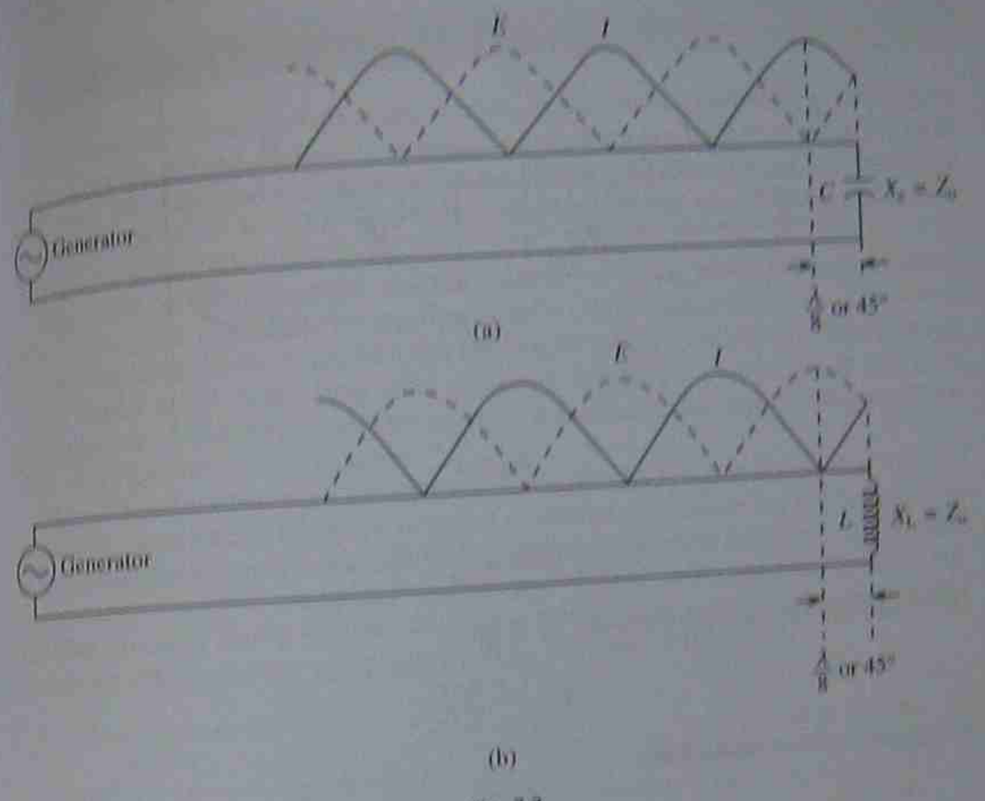


Fig. 7.3

Thus the ratio of the reflected to the incident voltage has the same magnitude as the current ratio, but opposite sign.

7.6 Standing wave ratio

Standing waves have already been mentioned, together with their formation due to load termination. Figure 7.4 shows the result of producing standing waves on a transmission line. Remember that standing waves are produced when two waves having the same frequency and amplitude and travelling in opposite directions are superimposed. The figure shows that standing waves produce points of minimum and maximum disturbance called nodes and antinodes, and this applies to voltage or current waves.

Associated with standing waves is the **standing wave ratio** which indicates the amount of reflected energy relative to the incident energy which is absorbed at the termination. Several forms of this are derived below. At a voltage maximum

$$V_{max} = V_i + V_r$$

while at a minimum

$$V_{min} = V_i - V_r$$

Hence

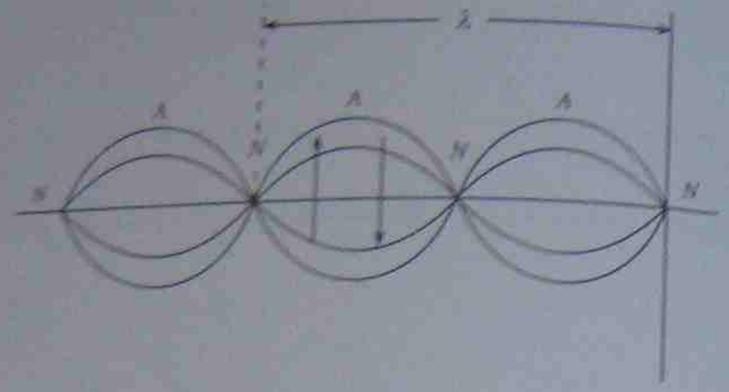


Fig. 7.4

$$S = \frac{V_{max}}{V_{min}} = \frac{V_i + V_r}{V_i - V_r}$$

Dividing numerator and denominator by V_i gives

$$S = \frac{1 + V_r/V_i}{1 - V_r/V_i}$$

It has already been stated that

$$\left|\frac{V_r}{V_i}\right| = |\rho|$$

hence

$$S = \frac{1 + |\rho|}{1 - |\rho|} \tag{7.17}$$

Also the power absorbed in the termination and the power reflected are given respectively by

$$P_i = I_i^2 Z_0 \text{ and } P_r = I_r^2 Z_0$$

Hence

$$\frac{P_r}{P_i} = \frac{I_r^2 Z_0}{I_i^2 Z_0} = \frac{I_r^2}{I_i^2}$$

Since

$$\frac{I_r}{I_i} = \frac{S-1}{S+1}$$

then

$$\frac{P_r}{P_i} = \left(\frac{S-1}{S+1}\right)^2 \tag{7.18}$$

7.7 Fundamental waveguide characteristics

The principles and parameters discussed in previous sections are applicable to waveguides and microwave devices. However, generally waveguides are used over short distances and losses are minimized. If a dielectric waveguide is used then primary and secondary coefficients such as R, G and α have to be considered. In this text air-filled rectangular waveguides will be discussed.

The part of the electromagnetic spectrum referred to as the microwave region loosely includes the range 1–300 GHz for practical purposes. Microwaves can be used for almost any of the applications for which the lower frequencies are used, but some of the advantages of the shorter waves make them more applicable for certain purposes. The two main advantages of microwaves are that the energy can be focused into narrow beams and that large signal bandwidths are possible.

These microwave bands are especially advantageous for relay sevices such as are used in satellite transmission, telephone relay, oil platform transmission and the broadcasting of commercial radio and television. However, special components and devices are required for operation at microwave frequencies, and one of these, a circulator, is shown in Fig. 7.5. The circulator allows the same microwave antenna to be coupled to the receiver and transmitter. This and other components will be discussed in this chapter.

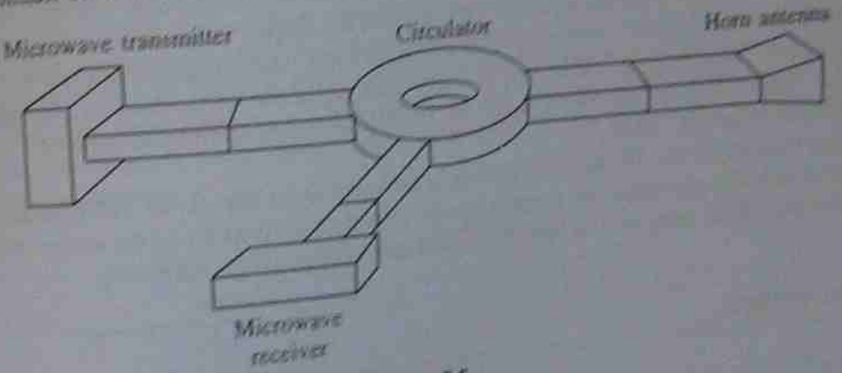


Fig. 7.5

The purpose of this chapter is to give a basic idea of the various microwave generators and devices which are used in the industry, but initially a knowledge of microwave transmission is necessary.

Transmission modes

Electromagnetic fields are formed as voltage and current waves travel down a transmission line. As propagation frequency increases a portion of the associated wavelength becomes comparable to the geometry of the transmission line dimensions. As the frequency increases, different types of propagation modes appear. The principal mode is the one which can carry energy at all frequencies. Higher modes are those that propagate only above a definite frequency range, and the point at which these frequencies start to propagate is called the cut-off frequency for that particular mode. An analogy is shown in Fig. 7.6.



Fig. 7.6

Figure 7.6(a) shows particles moving down a tube. In this case the particles have similar cross-sectional dimensions to the tube, and if the particles are given a constant velocity then a certain propagation will exist. This is analogous to single-mode propagation. If the diameter of the tube is increased or the particle size decreased, then the particles would propagate down the tube in different modes as shown in Fig. 7.6(b). This is analogous to high-order modes. If the particle size is further decreased the number of modes or propagation patterns increases. Hence certain patterns will occur when a definite change in size occurs either in the tube dimensions or in the propagating frequency.

A two-wire transmission line exhibits electric and magnetic fields as current flows along it. Both these fields are perpendicular to one another and also to the direction of propagation. Hence in the principal mode these waves are called transverse electromagnetic (TEM) waves.

If the frequency of transmission is increased so that the wavelength becomes similar to the cross-sectional dimensions of the transmission line higher-order modes can propagate. These higher-order modes will have at least one of their field components showing in the propagation direction, i.e. either the H-wave (magnetic mode) or the E-wave (electric mode). Depending on the mode involved it will be called transverse electric (TE) or transverse magnetic (TM).

The velocity of the TE and TM modes is different from that of the TEM mode. Two types of velocity are involved, namely group velocity (the velocity of the entire moving group) and phase velocity (including all path movements of the particles).

Skin effect

This effect occurs due to conductor losses mainly caused by the series resistance of the conductor. As frequency increases, skin effect becomes more critical and the current flows on the surface of the conductor rather than inside the conductor. Microwave guides are therefore used as hollow pipes with the inner surface coated with a conductive material. Because current penetration due to the skin effect is shallow, the currents have to follow the surface irregularities, thus increasing the length and consequently the losses. This is the reason why microwave components are highly polished in order to erase all surface markings.

The rectangular waveguide

When James Clerk Maxwell developed the theory of electromagnetic waves he imposed certain boundary conditions which are present when electric and magnetic fields travel through one material bounded by another.

Consider Fig. 7.7, in which a wave is guided along a tube. Under the principle of total internal reflection $\theta_i = \theta_r$ and the wave is continually reflected along the metal guide. A phase reversal occurs at each reflection, and for the electric field there is a change of permittivity (ε) at the boundary, while for the magnetic field there is a change in permeability (μ).

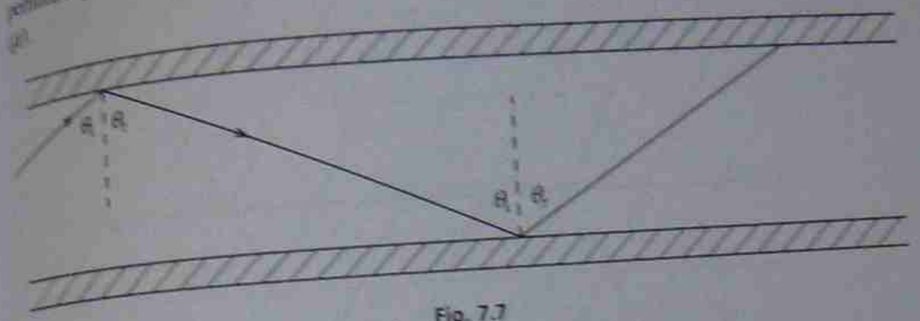


Fig. 7.7

An electric field which is parallel to a conductor will be short-circuited, and for this reason electric lines of force must always be at an angle to the guide walls. The magnetic field creates surface currents in the guide walls. This is the skin effect which determines the waveguide loss, and so it is essential that the propagation occurs through the guide rather than along the walls. This is achieved by using various modes which were explained earlier. For a rectangular guide the mode is described as TE_{mn}, where m and n refer to the dimensions shown in Fig. 7.8. Note that m indicates the number of half-wave variations of the electric field along a, while n indicates the number of half-wave variations of electric and magnetic field along b. If a dimension is less than half a wavelength no propagation occurs.

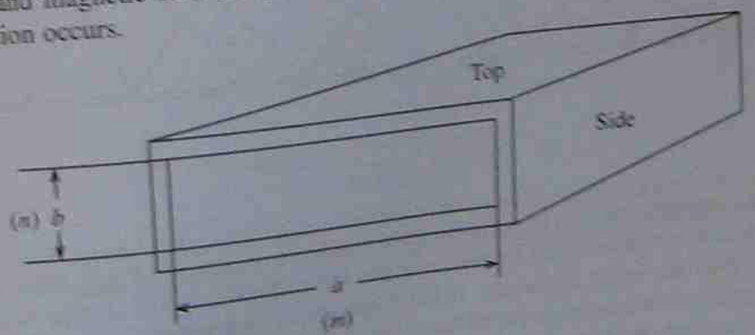


Fig. 7.8

Cut-off conditions

Each mode has a cut-off frequency below which it will not propagate. Single-mode propagation can be achieved by using only the mode with the lowest cut-off frequency. This is the dominant mode, and the waveguide will function at frequencies between its cut-off frequency and that of the mode with the next lowest cut-off frequency.

The concept of the parallel plate waveguide is helpful in understanding how the wave is guided along a waveguide. Figure 7.9 shows a plane wave being reflected from a plane conducting sheet. The angle of incidence $\theta_i = \theta_r$ and the lines denote positions of equal

phase. The propagation direction of the wave is perpendicular to the equal-phase lines. If a second sheet is added at *AA* as shown in Fig. 7.9 then a single ray along the guide would be propagated without loss as shown in Fig. 7.10.

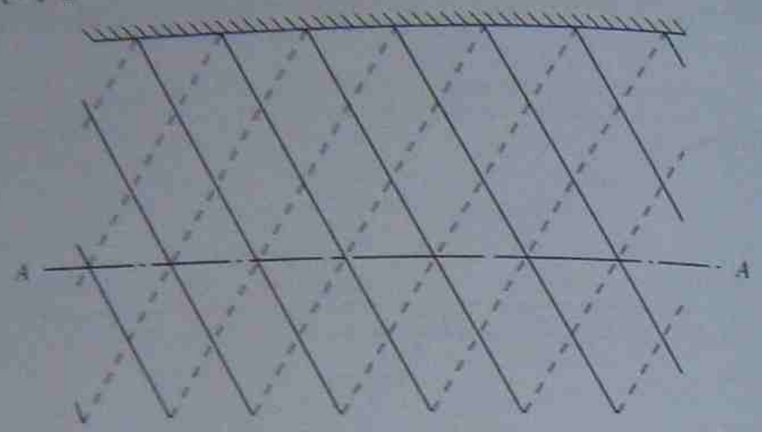
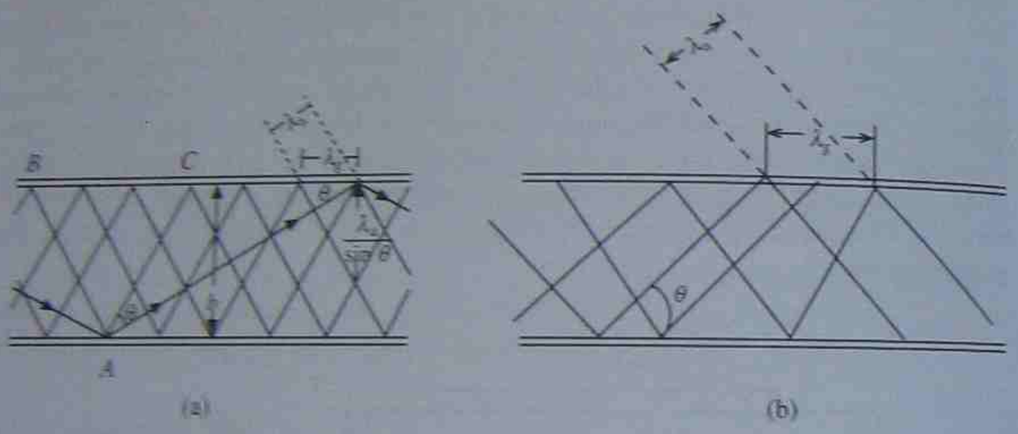


Fig. 7.9



(a) (b)

Fig. 7.10

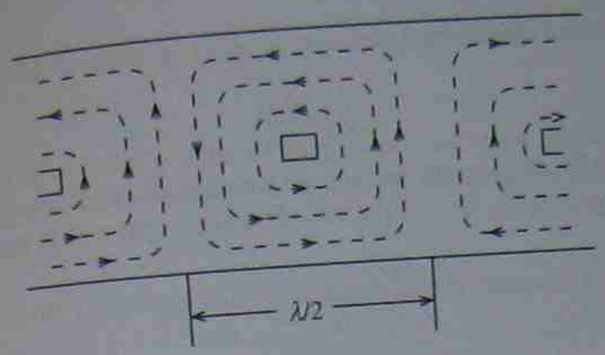
If the frequency which is being propagated is reduced as shown in Fig. 7.10(b) then the wavelength is increased. This would cause the angle of reflection to change in order to accommodate the lower frequency. If the frequency is progressively reduced, the half-wavelength becomes equal to the distance between the reflecting walls of the guide and the wave reflects backwards and forwards without progressing along the guide. This occurs at what is called the **cut-off frequency**. No propagation occurs below this frequency.

Figure 7.10 only shows a single propagation path, and it illustrates the simplest mode which is TE_{10}. The fields for this type of propagation are shown in Fig. 7.11.

For a rectangular waveguide the cut-off frequency is given by

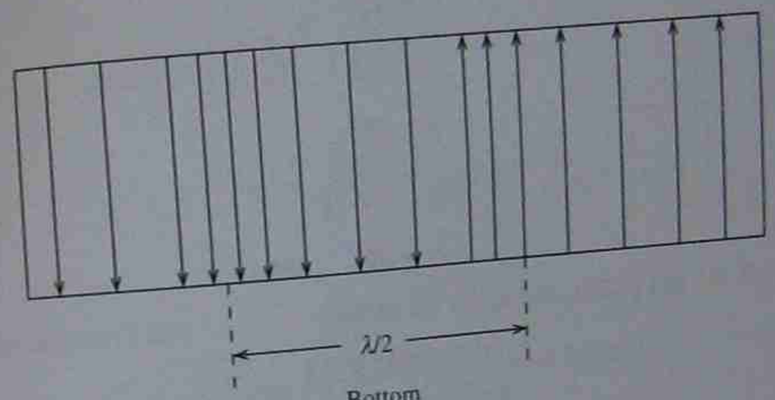
$$f_{c\mathrm{TE}nm} = \frac{c}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \tag{7.19}$$

where m and n are subscripts of a particular TE and TM mode. Hence, for the simplest mode, we have



Top
(magnetic field)

(a)



Bottom
(electric field)

(b)

Fig. 7.11

$$\lambda_{c\mathrm{TE}10} = \frac{2}{\sqrt{(1/a)^2 + (0/b)^2}} \tag{7.20}$$

This solution depends on the fact that there should be a whole number of half-wavelengths between the plates. If λ_a is the wavelength in air or free space, then the condition would be

$$b = \frac{n\lambda_a}{2\sin\theta} \tag{7.21}$$

where n is an integer.

Note that the wavelength in the direction of propagation is called the waveguide wavelength (λ_g) and is given by

$$\lambda_g = \frac{\lambda}{\cos\theta} \tag{7.22}$$

Hence

$$\cos\theta = \frac{\lambda}{\lambda_g}$$

If the spacing between the plates is

$$b = \frac{n\lambda_g}{2} \tag{7.23}$$

then $\theta = 90°$ (equation (7.21)), the waveguide wavelength is infinite from (7.22). Hence the wave will not propagate. This is the cut-off wavelength and is given by (7.23).

Since

$$\lambda_g = \frac{c}{f}$$

we can rewrite (7.23) as

$$b = \frac{nc}{2f_c}$$

and

$$f_c = \frac{nc}{2b}$$

hence

$$\lambda_c = 2b \tag{7.24}$$

Combining (7.21) and (7.22), and using the identity

$$\sin^2\theta + \cos^2\theta = 1$$

gives

$$\frac{\lambda_c^2}{(2b)^2} + \frac{\lambda_0^2}{\lambda_g^2} = 1$$

($n = 1$ in this mode). Also, from (7.24),

$$\frac{\lambda_c^2}{\lambda_1^2} + \frac{\lambda_0^2}{\lambda_g^2} = 1 \tag{7.25}$$

hence

$$\frac{1}{\lambda_g^2} = \frac{1}{\lambda_0^2} - \frac{1}{\lambda_c^2} \tag{7.26}$$

This equation can also be expressed as

$$\lambda_g = \frac{\lambda_0}{\sqrt{1 - (n\lambda_0/2b)^2}} \tag{7.27}$$

by using (7.24) and assuming $n = 1$.

The following points should be noted regarding waveguide design:

(i) The attenuation loss is greater as b is made smaller.

(ii) The dimension of b determines the voltage breakdown characteristics and hence the maximum power capacity.

(iii) a and b should be made as large as possible for large power applications.

(iv) In practice $a = 2b$.

(v) Dimensions are normally selected so that only one mode of propagation is possible and thus the size of the waveguide is related to the frequency band.

Example 7.1

Determine the cut-off frequency and wavelength of a rectangular waveguide in the TE_{11} mode if $a = 8.1$ cm and $b = 4.3$ cm.

Solution

From (7.19),

$$f_{cTE11} = \frac{c}{2}\sqrt{\left(\frac{1}{a}\right)^2 + \left(\frac{1}{b}\right)^2}$$

$$= \frac{3 \times 10^8}{2}\sqrt{\left(\frac{1}{8.1 \times 10^{-2}}\right)^2 + \left(\frac{1}{4.3 \times 10^{-2}}\right)^2}$$

$$= 8.9 \text{ GHz}$$

and, similarly to (7.20),

$$\lambda_{cTE11} = \frac{2}{\sqrt{\left(\frac{1}{a}\right)^2 + \left(\frac{1}{b}\right)^2}} = 3.4 \text{ cm}$$

Example 7.2

A rectangular waveguide functions in the TE_{10} mode with a free space frequency of 3.2 GHz. If the guide dimensions are given as $a = 6.2$ cm and $b = 3.3$ cm, determine:

(a) the cut-off frequency and wavelength;

(b) the guide wavelength.

Solution

(a)

$$f_{cTE10} = 1.5 \times 10^8\sqrt{\frac{1}{6.2 \times 10^{-2}}} = 2.4 \text{ GHz}$$

$$\lambda_{cTE10} = \frac{2}{\sqrt{\frac{1}{6.2 \times 10^{-2}}}} = 12.4 \text{ cm}$$

(b)

$$\frac{1}{\lambda_g^2} = \frac{1}{\lambda_0^2} - \frac{1}{\lambda_c^2}$$

Since

$$\lambda_0 = \frac{c}{f_0} = \frac{3 \times 10^8}{3.2 \times 10^9} = 0.094 \text{ m}$$

we have

$$\frac{1}{\lambda_g^2} = \frac{1}{(0.094)^2} - \frac{1}{(0.124)^2}$$

$$\lambda_g = 14.32 \text{ cm}$$

Example 7.3

A waveguide is of British Standards size 12 and has the following specifications: a = 17.215 cm, b = 8.315 cm and f_c = 3.15247 GHz. Its recommended operating range is 3.95–5.85 GHz. If it has to function in the TE_{21} mode, calculate the guide wavelength for its operating range.

Solution

We will use equation (7.27):

$$\lambda_g = \frac{\lambda_0}{\sqrt{1 - (n\lambda_0/2b)^2}}$$

For f_0 = 3.95 GHz,

$$\lambda_0 = \frac{c}{f_0} = \frac{3 \times 10^8}{3.95 \times 10^9} = 0.0759 \text{ m}$$

$$\therefore \quad \lambda_g = \frac{0.0759}{\sqrt{1 - (0.0759/(2 \times 0.08315))^2}} = 8.5 \text{ cm}$$

For f_0 = 5.85 GHz,

$$\lambda_0 = \frac{3 \times 10^8}{5.85 \times 10^9} = 0.05 \text{ m}$$

$$\therefore \quad \lambda_g = \frac{0.05}{\sqrt{1 - (0.05/(2 \times 0.17215))^2}} = 5.4 \text{ cm}$$

7.8 Microwave passive components

The basic theory of microwaves and their transmission along waveguides has been discussed previously. In order to couple or direct this energy special components are used which operate generally in the TE_{10} dominant mode for rectangular waveguides. This text will only deal with rectangular waveguides, although other geometries exist. The components discussed here are: the directional coupler, waveguide junctions, cavity resonators, probes, and circulators and isolators.

The directional coupler

The directional coupler is a device which, when installed in a waveguide, will respond to a wave travelling in one direction but will be unaffected by a wave travelling in the opposite direction. Directional couplers are four-port devices and the power ratios between the ports are defined by the **coupling factor**, **directivity** and **insertion loss**.

Consider the four-port directional coupler in Fig 7.12. In this case power entering port 1 gives an output at ports 2 and 3 but no output at port 4. This coupler can be inserted in two ways: forward and reverse. Note the following parameters. The coupling factor is given by

$$C_f = \frac{\text{Power in port 3}}{\text{Power in port 1}} \text{ (dB)} \tag{7.28}$$

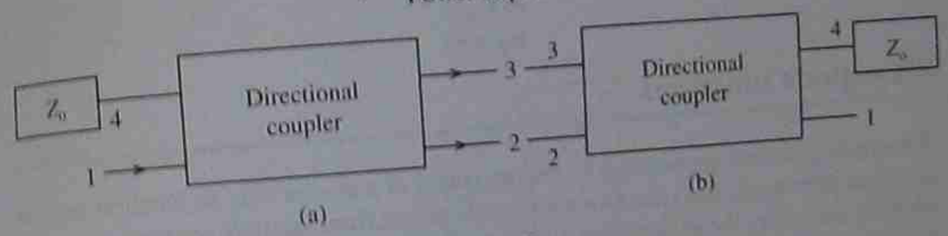


Fig. 7.12

The directivity is given by

$$D = \frac{\text{Power in port 4}}{\text{Power in port 3}} \text{ (dB)} \tag{7.29}$$

The insertion loss is the amount by which the signal in the main guide is attenuated and may be given by

$$I = \frac{\text{Power in port 4}}{\text{Power in port 1}} \text{ (dB)} \tag{7.30}$$

Note that the directivity is defined as the ratio of the power appearing at port 4 when the coupler is in the forward direction to the power appearing at port 3 when the coupler is in the reverse direction and port 4 is terminated in its characteristic impedance (Z_0).

One of the most common directional couplers is the two-hole interference directional coupler shown in Fig. 7.13. This coupler will only work when the holes are a quarter of a wavelength apart. If higher frequencies are required the number of holes is increased. Figure 7.13(a) shows the physical structure, while Fig. 7.13(b) shows how the signal is propagated through the holes. At each hole the signal splits into two components, one travelling in the forward and one in the reverse direction. The waves which travel from input port 1 to output port 3 move the same wavelength distance, and are in phase and add constructively; the two waves travelling from input port 1 to the load move along a path which differs by half a wavelength, and hence destructive interference takes place.

The holes are separated by half a guide wavelength, as shown in Fig. 7.13(a). In this case only two holes are shown, but more may be included to provide greater coupling between guides.

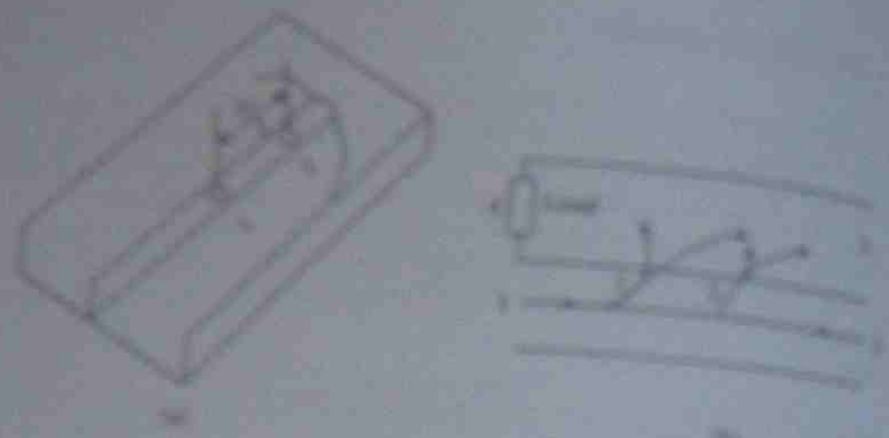


Fig. 7.12

Waveguide junctions

Waveguide junctions are required to remove power in a similar way to junction device to unlock the work. They are also used to mix power from multiple sources. However, anything that alters the geometry of a waveguide will have an effect on the circuits and magnetic fields and may change the characteristic impedance of the guide.

If the guide normally works in the TE_{10} mode with E-field and H-field patterns as shown in Fig. 7.13, then bend couplings, similar to those in Fig. 7.14, should be used.



E-plane bend

H-plane bend

Fig. 7.14

One of the most common junctions is the T junction shown in Fig. 7.15. This is an E-field T junction. A signal applied to port 1 appears at ports 2 and 3, both these signals being out of phase. In practice, the T junction requires some form of matching between the ports, this can be done by using a tuning device such as a boss screw which is inserted into the guide section. It can be adjusted for capacitance, mesh resistance of inductive loading.

If E-field and H-field T junctions are combined, the hybrid T junction is formed (see Fig. 7.16). A wave entering port 1 excites signal waves of opposite phase in 2 and 3. A signal at 4 produces equal signals of opposite phase in 2 and 3. Because of the geometry of the device a signal in 1 will not excite any dominant mode wave in 4. Hence there is no direct coupling between 1 and 4.

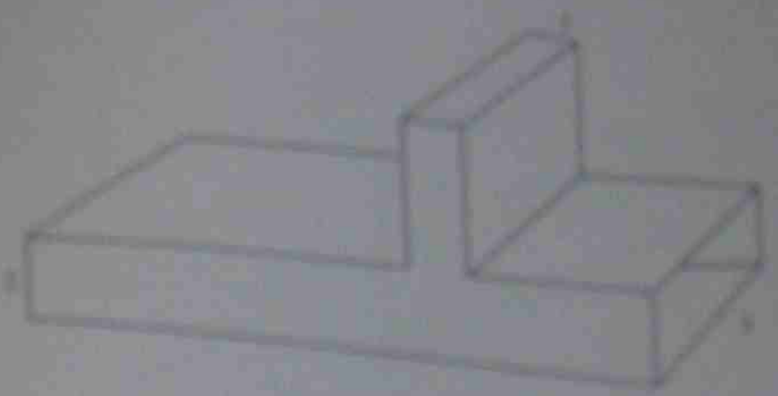


Fig. 7.15

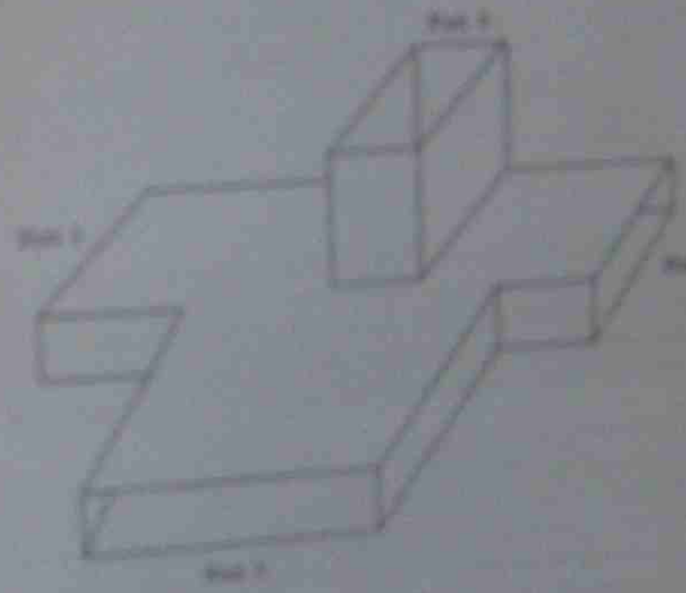


Fig. 7.16

If the E and H branches of the junction are matched, the other two arms are matched and there is no transmission between 2 and 3. Therefore a signal entering 2 will be equally divided between arms 1 and 4, while a signal entering 3 is equally divided between 4 and 1. The converse is also true.

Figure 7.17 shows the coupling between a local oscillator and a mixer. This configuration allows the signal at 4 to be combined with the local oscillator signal at 1. The combined signals then appear at 2 and 3.

Cavity resonators

The proportion of the cavity resonator is shown in Fig. 7.18. The concrete wall circuit is shown in Fig. 7.19(a). Increasing the resonant frequency means that C and L must be

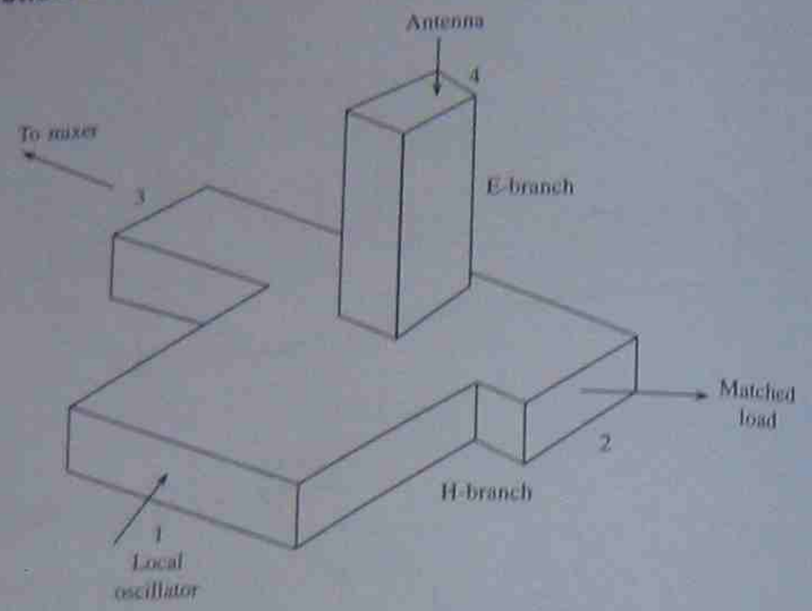


Fig 7.17

reduced until two small plates and a single-turn inductance comprise the *LC* circuit as in Fig. 7.18(b). To reduce the inductance further, several one-turn inductors are placed around the edge of the capacitor plates as shown in Fig 7.18(c). Continuing this process, it can be imagined that the two small capacitor plates are completely enclosed by several inductor bands until essentially a box is formed, known as a **cavity resonator**.

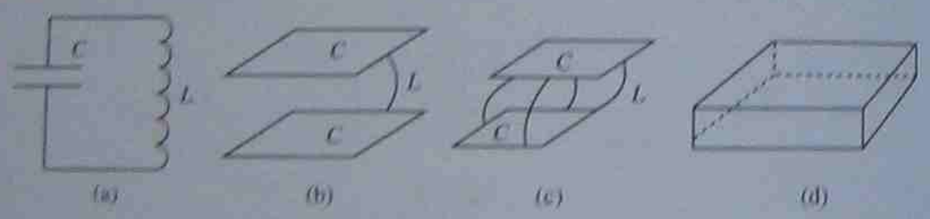


Fig 7.18

Cavity resonators therefore have a natural frequency which depends on the dimensions of the 'box'. At some determined frequency there will be a high-amplitude electric field between the plates of the capacitor and a high current up and down the sides of the box. At some instant the energy is stored in the electric field, while at the next instant it is transferred to the magnetic field.

In order to understand the fields in resonators a three-dimensional effect is necessary, and it is common to use rectangular coordinates as in Fig. 7.19. Here the energy has been introduced at point *A* and standing waves E_y, H_z and H_x have been developed as a result of incident and reflected components of the wave. Here E_y is the electric component and H_z and H_x are magnetic components 90° out of phase with each other and also 90° out of phase with the E_y field.

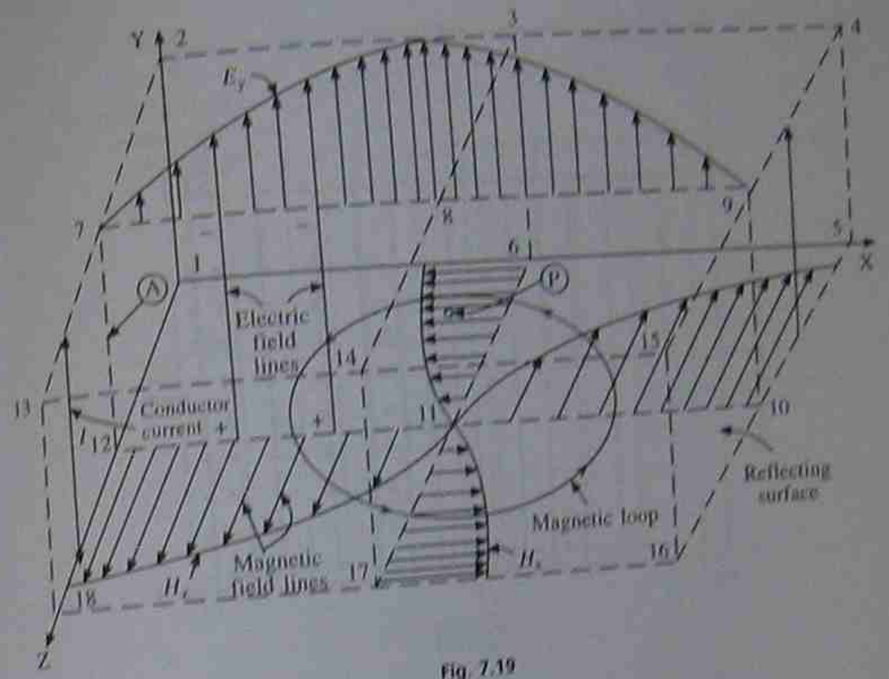


Fig. 7.19

To follow the details of the action more clearly, the corners and centre points of the edges of the three-dimensional enclosure have been numbered in order to identify the location of different two-dimensional areas or planes, e.g. the top plate is indicated by plane 2, 3, 4, 9, 15, 14, 13 and 7.

Figure 7.19 has been redrawn with the electric field distribution as shown with the appropriate polarity. In both Figs. 7.20 and 7.21 only an instantaneous condition of an action in which the magnetic and electric fields are constantly changing is represented, therefore a conduction current does exist mainly on the sides of the box. At the instant indicated in Fig. 7.16 the lower plate is positive and the upper plate is negative, but a half-cycle later their polarities will reverse and these reversals will repeat during each succeeding cycle. As the conduction current tends to equalize the charges on the top and bottom plates it will be alternating as indicated by the double-headed arrows between points 7–12 and 9–10.

The magnetic fields H_z and H_x of Fig. 7.19 can be analysed best by reference to the essential information of plane 1, 5, 16, 18 which is redrawn in Fig. 7.21. Here the non-uniform distribution of the magnetic field is shown by curves H_z and H_x, drawn over the tops of the solid line magnetic fields to represent the variation of the strength of the field from centre point 11 to the corresponding sides of the cavity. If it is assumed further that the extended dashed magnetic field lines are a continuation of the solid lines, a magnetic loop is formed. The intensity of the magnetic loops is greatest near the sides of the cavity and decreases toward the centre until at point 11 the magnetic field is zero.

As explained for Fig. 7.19, the electric and magnetic fields are 90° out of phase, therefore with zero magnetic field at point 11 the electric field must be maximum. This is shown in Fig. 7.22, where the conditions of point 11 extend upward through point *P* of

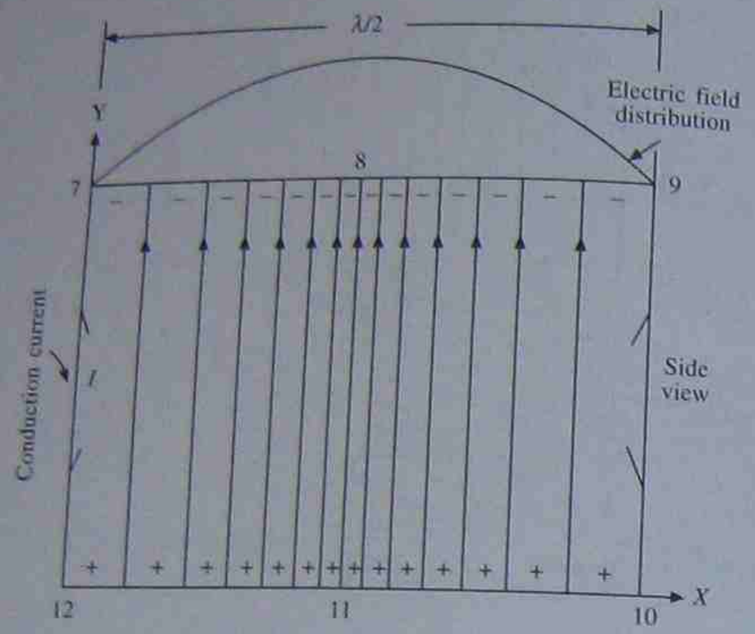


Fig. 7.20

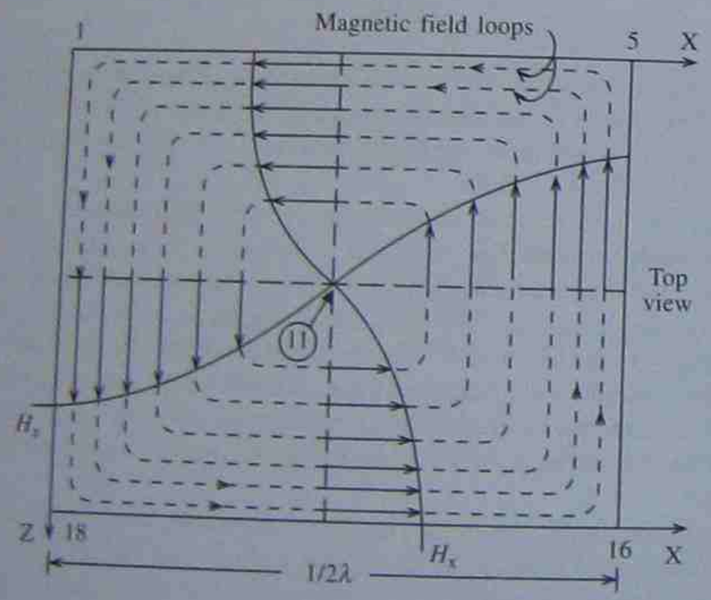


Fig. 7.21

Fig. 7.19 to point 8. Therefore at point P there is zero magnetic field and maximum electric field.

Looking in from the end of Fig. 7.19, the plane bounded by points 14, 8, 3, 6, 11 and 17 appears as shown in Fig. 7.22 with point P at its centre. To show more clearly the direction of magnetic density distribution, solid dots represent vectors out of the plane of the paper and small circles represent vectors into the paper, as indicated by the upper sketch of Fig. 7.23.

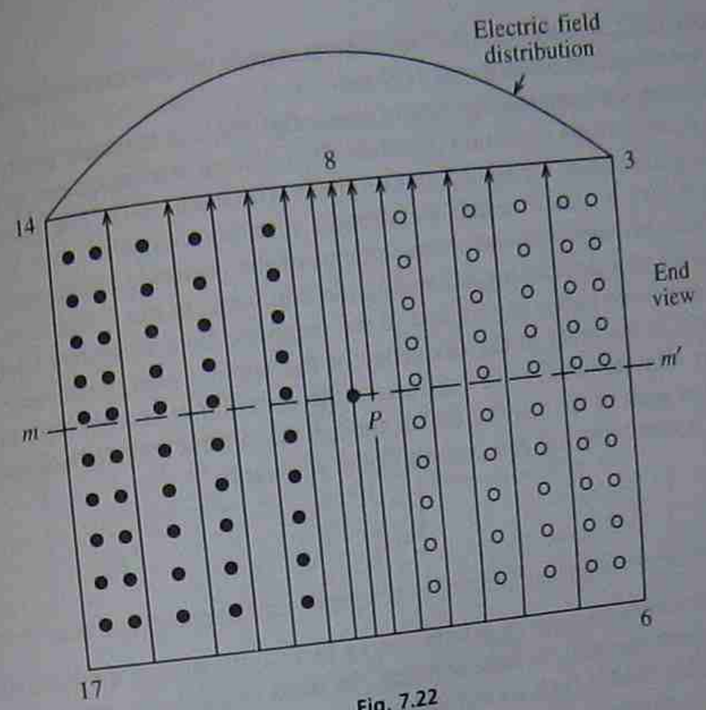


Fig. 7.22

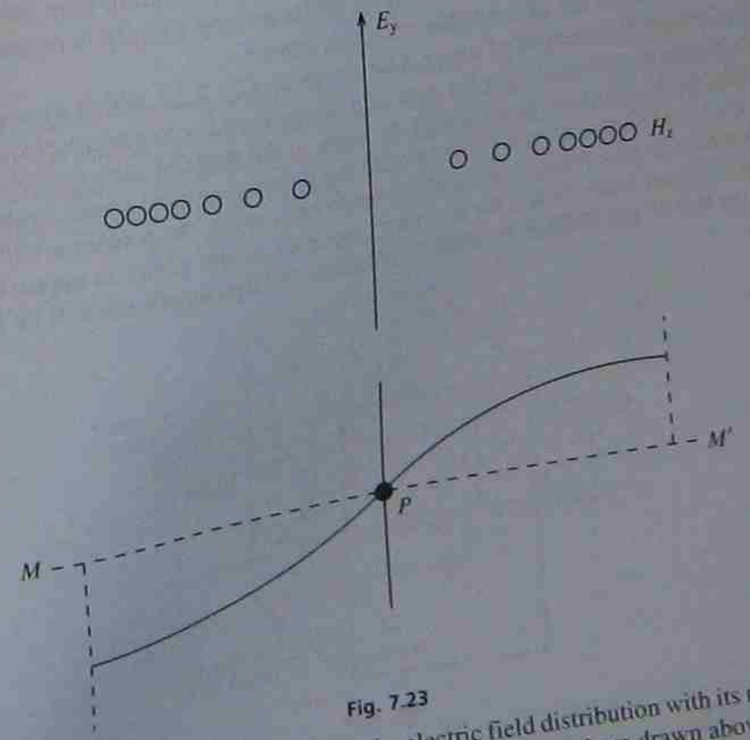


Fig. 7.23

As in Fig. 7.22, the arrowed lines show the electric field distribution with its maximum value in the plane of line 8 and point P, with the electric waveform drawn above line 14, 8, 3 of Fig. 7.22. The magnetic field distribution across section MM' is shown by the

curve of Fig. 7.23, but notice that P is still the region of zero magnetic field and a point of maximum electric field strength.

Summarizing the important points of these figures, the resonant cavity of Fig. 7.19 shows the instantaneous condition of established electric and magnetic fields with their maximum and minimum values 90° out of phase with each other. The dimensions of the rectangle are such to permit a half-wavelength standing magnetic wave in the X and Z directions in accordance with the characteristics of the initiating electromagnetic energy, and at the same time developing a standing electric wave in the Y direction. The energy is in the electric field at one instant and in the magnetic field an instant later, oscillating from one field to the other at the frequency of the applied energy. Because of the skin effect at very high frequencies of oscillation, the conduction current does not penetrate deeply into the sides of the box but acts as though the current travels back and forth over the surfaces between the top and bottom of the resonator.

Probes

In order to extract energy from or deliver energy to a cavity special methods of coupling are required. Such methods include shooting electrons through the resonator at a point where the electric field is high, or introducing a small conducting loop into the area at a point where the magnetic field is strong. A probe or loop usually is connected to a co-axial cable with the aid of a suitable matching device.

The first method mentioned above is illustrated in Fig. 7.24, which shows a simplified cavity resonator with holes in the near and opposite sides to permit electrons to pass through. As the electrons pass through the holes in the walls of the cavity it is necessary that their transit time be small compared to the duration of a resonator cycle. However, if the electrons pass through in bunches, one to each cycle, the resonator will be excited by the electron beam. When the resonant frequency of the cavity is approximately the same as that of the electron bunches, oscillations of large amplitude will be generated.

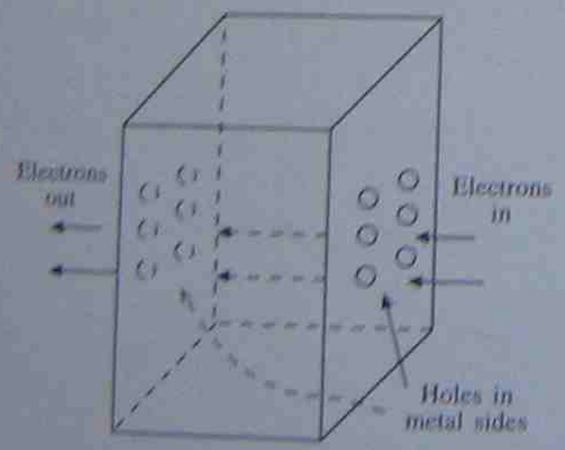


Fig. 7.24

The second method of excitation is illustrated in Fig. 7.25, which shows a small probe placed in the central area of the cavity resonator. The probe is the extended inner conductor

of a co-axial cable and should be placed to coincide with the electric field vector. From the explanations given previously, it is known that the greatest strength of the electric field is found near the centre of the resonator, therefore the exciting probe should be placed in the region of point P in Fig. 7.19.

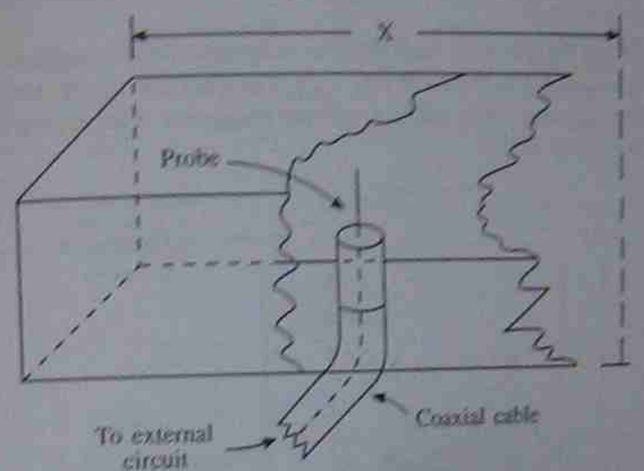


Fig. 7.25

The third method of cavity excitation is that shown in Fig. 7.26, where a loop of arbitrary shape is placed within the cavity in such a position as to envelop the greatest magnitude of magnetic flux lines. The plane of the loop must be at right angles to the magnetic field, as shown at point A in Fig. 7.19.

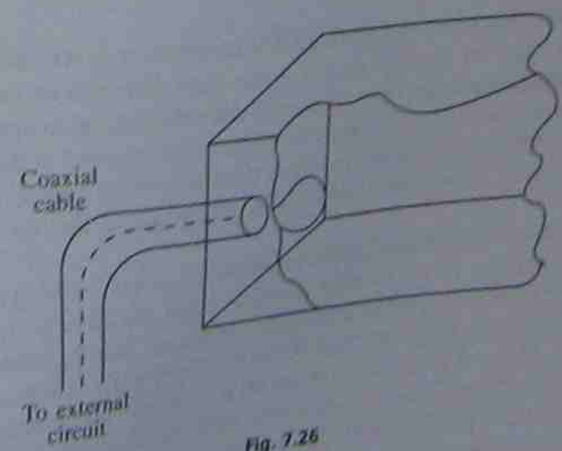


Fig. 7.26

Generally the method of output coupling to the cavity resonator is the same as the methods of injection, and so points of maximum electric and magnetic field strength are chosen for best effects.

Circulators and isolators

An isolator is a device that has the ability to pass a signal in only one direction while the other direction exhibits high attenuation. A typical type of isolator is the ferrite isolator; for the purpose of understanding its operation an explanation of Faraday rotation is helpful.

Any electron has natural spin, and if a d.c. magnetic field is applied to a spinning electron it starts to precess as shown in Fig. 7.27. The direction of precession depends on the polarity of the magnetic field, and its rotational frequency is dependent on the strength of the applied magnetic field.

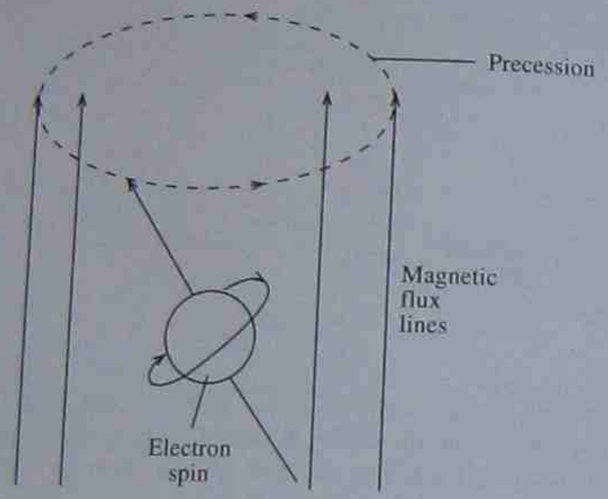


Fig. 7.27

When a circularly polarized wave meets precessing electrons, it is found that interaction only takes place when the wave rotation is in the same direction as the electron spin. Since linear polarization consists of two equal circular polarizations in opposite directions then when the linear polarized wave travels through a ferrite material in the same direction as an applied magnetic field these two circularly polarized waves interact differently with the spinning electron. Hence their phase shifts are not equal and the polarization is rotated.

Figure 7.28 is the functional diagram of a Faraday rotation isolator using these principles. This shows transmission in the forward direction; when the electric field lines of the microwave are at right angles to the attenuation vanes there is little attenuation, but this will increase as the angle decreases from 90° to 0°. The specific action in the isolator is seen in Fig. 7.29. Figure 7.29(a) shows the incident wave with no attenuation, while Fig. 7.29(b) shows the reflected wave which suffers up to 30 dB of attenuation because the vane of waveguide 2 is at 45° to that of waveguide 1.

A circulator allows the separation of signals and once again involves the operation of ferrites. The most frequently used type is the three-port circulator which is shown in Fig. 7.30. Effectively this device consists of three isolators in which power entering 1 is received at 2 only, while power entering 2 is received at 3 only, and power entering at 3 is received at 1 only.

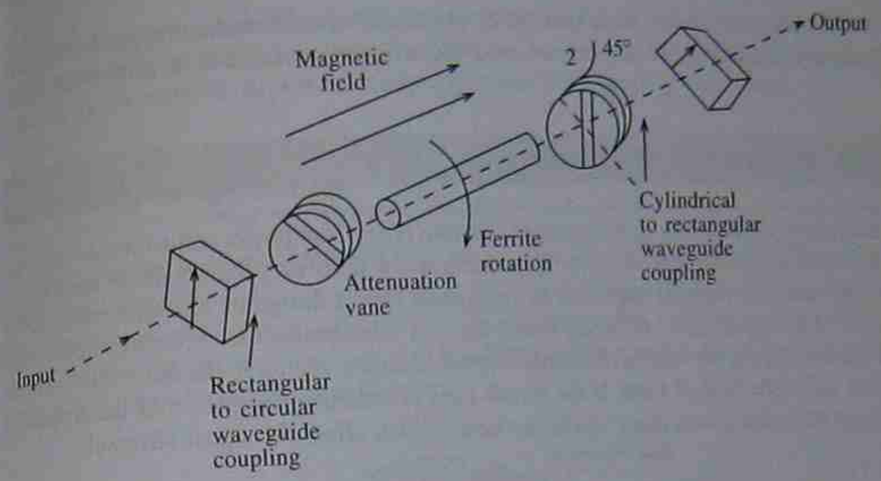


Fig. 7.28

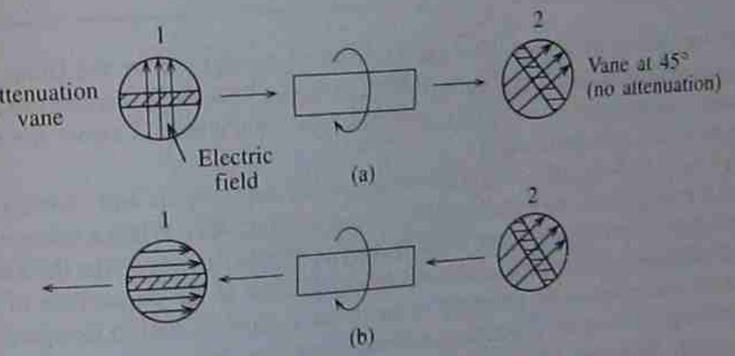


Fig. 7.29

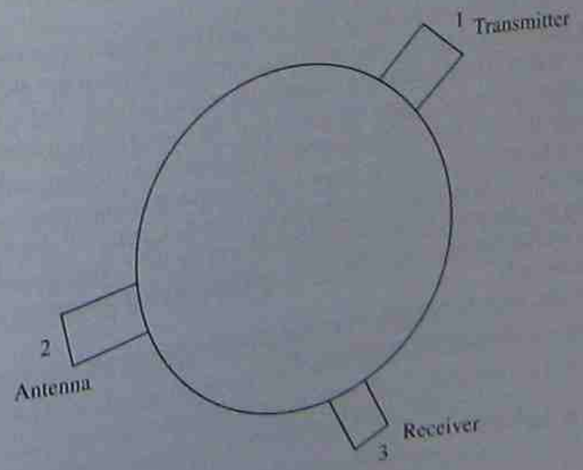


Fig. 7.30

Circulators can have more than three ports and operate without using ferrites, but generally a maximum of four ports are used with a ferrite construction for greater efficiency.

7.9 Microwave active devices

Microwave devices may be categorized into two types: low-power solid-state devices and high-power vacuum-tube devices. Communications involving the gigahertz bandwidths cannot use conventional transistor or integrated circuit design as silicon devices suffer from stray capacitance between leads and the semiconductor elements themselves. Furthermore, the movement of charge carriers from one region to the other takes a finite time called the **transit time**. If the transit time is similar to the period of the frequency being transmitted then phase shifts can occur which affect the signal adversely.

Solid-state devices

Two devices which overcome the major problem of transit time are the Gunn diode and the impact avalanche and transit time (IMPATT) diode. Both these devices use a negative resistance characteristic, i.e. over a portion of the characteristic curve the resistance decreases as the voltage increases.

The Gunn diode is used for oscillator and mixer applications and consists of a thin slice of n-type gallium arsenide between two metal conductors. When a voltage is placed across the slice oscillations occur, the frequency of which depends on the thickness of the slice. Furthermore, the period of the oscillations is equal to the transit time of electrons across the slice. Hence the geometry of the device is fundamental to its operation.

It also operates on several modes, and this allows the diode to be tuned when placed in a cavity. However, like all negative resistance devices, it requires a circulator to separate the input from the output signals.

The IMPATT diode utilizes the delay time required for an avalanche condition and the transit time to produce a negative resistance characteristic. It has a p-n junction and may be a four-layer device. The thickness of the intrinsic region is fabricated so that the transit time of an electron across this region is equal to half the period of the operating frequency.

The diode operates with reverse bias just below the breakdown region, and the fluctuation of the operating frequency, which is superimposed upon this bias, causes breakdown to occur once per cycle. When the junction breaks down, a burst of electrons enters the intrinsic region and appears at the other side half a cycle later. The resultant oscillations are dependent on the dimensions of the diode and the resonant frequency of the cavity in which it is immersed.

IMPATT diodes have higher efficiency and greater power levels than Gunn diodes, but they are noisier because of the avalanche effect.

Microwave tubes

When greater power is required more complex devices must be used. Also the process of miniaturization imposes problems at higher frequencies due to higher power dissipation. Because of these restrictions alternative designs have been developed, among them multicavity magnetrons, klystrons, reflex klystrons and travelling wave tubes.

Multicavity magnetrons

In order to understand the operation of a magnetron, Fig. 7.31 shows the effect of an electric and magnetic field interaction on an electron's motion. The dot in the centre of the figure is the cross-section of a filament in a cylinder. The cylinder is positive with respect to the filament, and the small dots inside the cylinder represent the magnetic flux lines in the same direction as the filament.

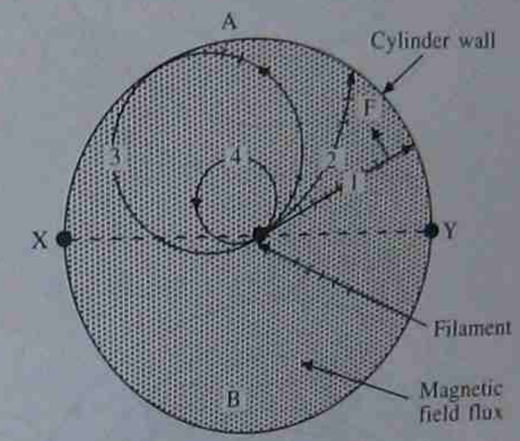


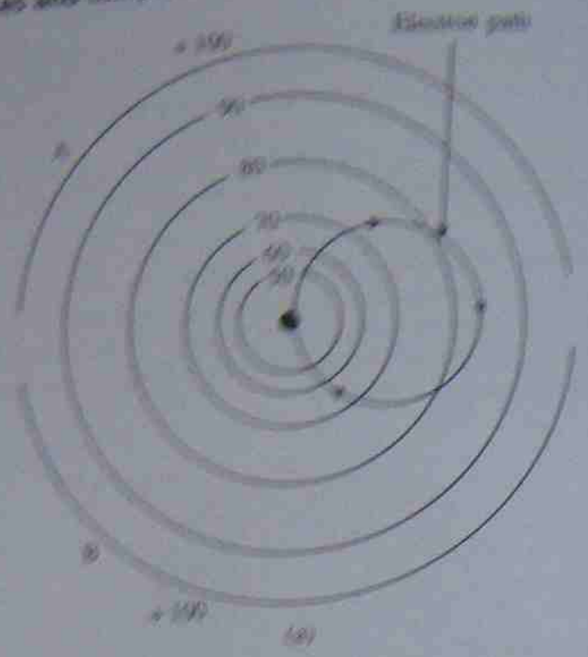
Fig. 7.31

When there are no magnetic lines present the electrons move from the filament to the cylinder wall as shown in path 1. When a weak magnetic flux is applied, the electrons cross the flux lines and, because of the interaction, the electrons travel in a circular path as seen in path 2. If the magnetic flux is increased it is possible to cause the electron stream to follow path 3 and just graze the cylinder wall before returning to the filament. Path 4 shows the movement of electrons under the influence of a stronger field.

Hence if the filament is a hot cathode and the cylinder is the anode, forming a diode, then the electrons can move in curved paths depending on the strength of the magnetic field. For path 2 the average diode current remains constant but for path 3 the diode current suddenly drops to zero or cut-off. Any further increase of magnetic flux merely reduces the excursion of the electrons from the filament source after cut-off has been reached.

A practical magnetron is made with a split anode as shown in the cross-sectional view of Fig. 7.32. If both anodes are positive by the same amount, their force distributes evenly between the anodes and the cathode. An electron in Fig. 7.32(a) will experience the same attractive force at any position on the equipotential lines. The path of an electron is shown for the cut-off condition.

If the voltage on one anode is increased while the voltage on the other is decreased, the equipotentials are distorted as shown in Fig. 7.32(b). At cut-off the electron is attracted.



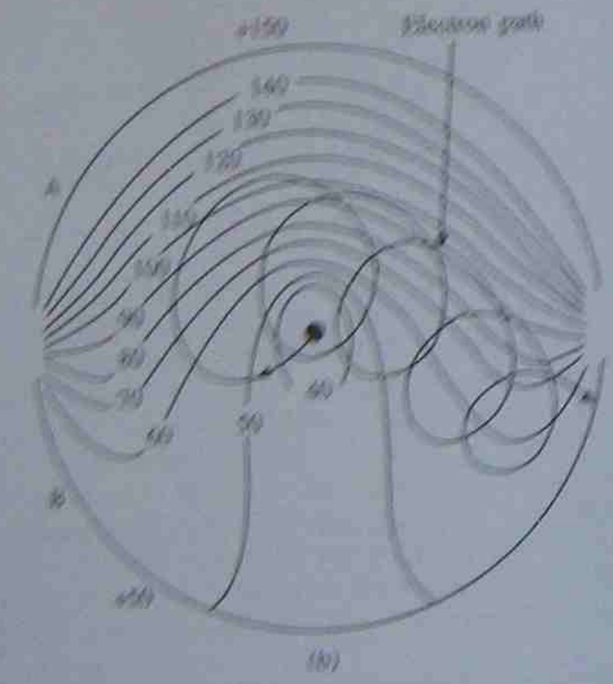


Fig. 7.32

at first, to the anode with the highest potential. But the magnetic field curves it away from this direction. As its path continues it is once again attracted to the same anode, but the attraction is not as great as before because the anode potential is now less. Hence the electron takes a spiral path, its energy decreasing all the time until it approaches the anode with the lower potential. This potential is enough to attract the electron to the

anode with the lower voltage. More electrons arriving at the lower-voltage anode cause the negative resistance effect which was mentioned earlier. This effect is shared by both anodes so an alternating voltage appears across them, and hence the positive feedback produces oscillations by altering anode potentials.

The problem of transit time is overcome by adding end plates to the split anode and causing the electrons to spiral around the cathode, as shown in Fig. 7.33. Hence the path of the electrons can be adjusted either by varying the anode voltage, the magnetic field or both, the electrons can spiral for the full length of the cathode. There is a mutual action between the anode and an electron. As the electron approaches the anode, the magnetic field curves the electron path away from the anode. The electron was travelling towards the anode and because of this it loses energy.

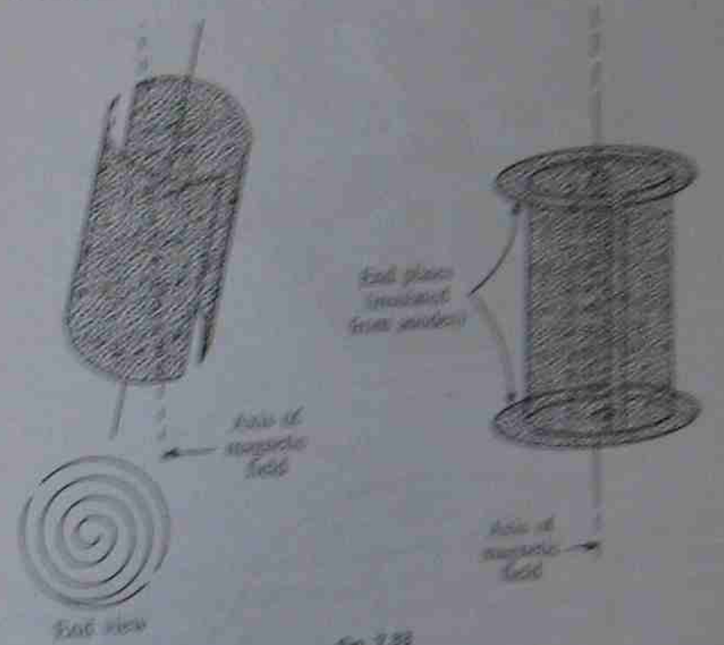


Fig. 7.33

Because the electron travels through the field near the anode, the field for that moment is less by one electron charge. The electron repels one electron charge from the anode to the supply, but as soon as the electron is no longer near the anode, this electron, repelled towards the supply, can return. This back-and-forth motion of the repelled electrons on the anode is the a.c. component of the field superimposed on the d.c. field.

The electric and magnetic fields must be so adjusted that the electrons always find a retarding field, one in which they can give up energy. The d.c. component and the magnetic field are so adjusted that the electrons can add energy to the a.c. component of the electric field each time around. Thus the transit time of the electron is one complete cycle of the induced field. This is known as the transit time operation of the magnetron.

It should be noted that so long as the fields are present it does not matter if the anode is split or integral. However, to achieve the fields some resonant circuits must be built into the anode and the simplest way to do this is to build cavities into the anode. The resonant time between cavities is the time of one cycle.

The structure of a multicavity magnetron, using the principles discussed in the previous section, is shown in Fig. 7.34. In the multicavity magnetron, the cavities are set in oscillation by the rotating electrons in the space between cathode and anode. When the electron path is favourable to adding electron energy to the field, the oscillations are sustained. Other electron paths take energy away from the field. The magnetron operating conditions must be adjusted so that more energy is added to the field than taken away. Maximum output occurs when the added energy reinforces the cavity oscillations.

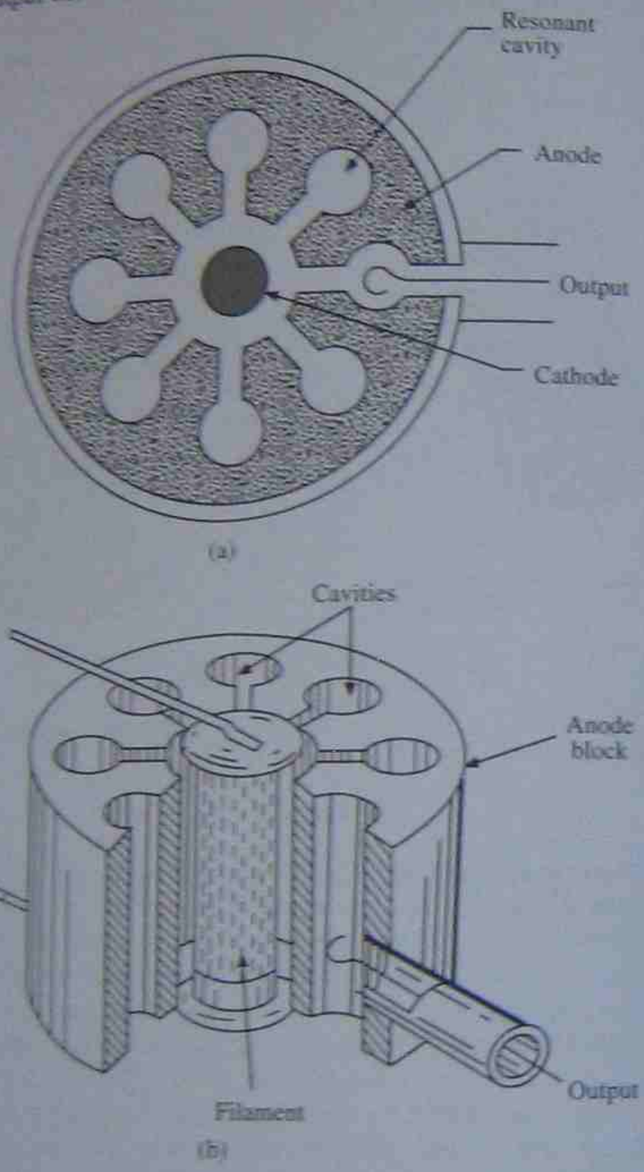


Fig. 7.34

The best time for the electrons to arrive is when there is maximum voltage across the opening in the cavity. The opposite sides of the opening are then at opposite polarities and the electrons approach from the positive side of the opening, as shown in Fig. 7.35. Side

B is negative and contains more electrons than A, so the electrons of the oncoming stream repel those at B, giving them added push to travel to side A around the inner surface of the cavity. In this way the oscillations of the cavity are reinforced.

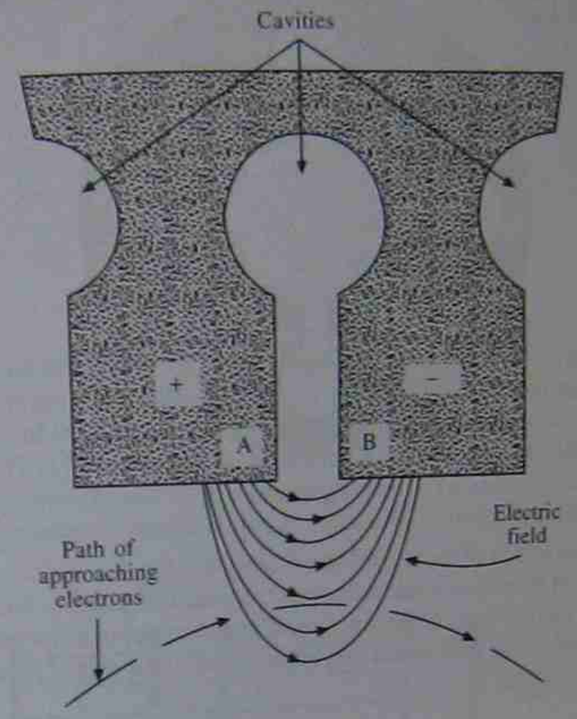


Fig. 7.35

After passing a number of cavities the stream of electrons is slowed down and is attracted by the anode block. The cathode, however, is continually emitting electrons and some of them arrive at the gap at a time when the oscillations are not aided. These electrons, instead of being slowed down, are speeded up by passing the cavity fields. This results in greater action between the electrons and the magnetron magnetic field, and the electrons curve back towards the cathode. Thus, when all the operating constants are correctly adjusted, the electrons which do not aid oscillations are carried off and the magnetron can operate efficiently at high output.

Magnetrons have various modes of operation, each of which gives a different operating frequency. The cavity resonators represent a series of tuned resonant circuits, each coupled to the other. Some phase difference usually exists across the faces of the cavities and, at a given field strength and anode voltage, a phase difference of 360° exists around all of the cavities.

Maximum efficiency may occur for a particular mode. For example, if the phase difference between the oscillations in successive cavities is 180° and there are eight cavities then there are four separate groups of electrons each aiding oscillations. However, when a number of resonant circuits are used, there is a slight tendency for the frequency of each to vary slightly from the other. To prevent this, the coupling between the in-phase cavities is increased by strapping. Figure 7.36 shows the anode straps connected to

alternate anode segments. This keeps the anode voltages in phase and stabilises the frequency.

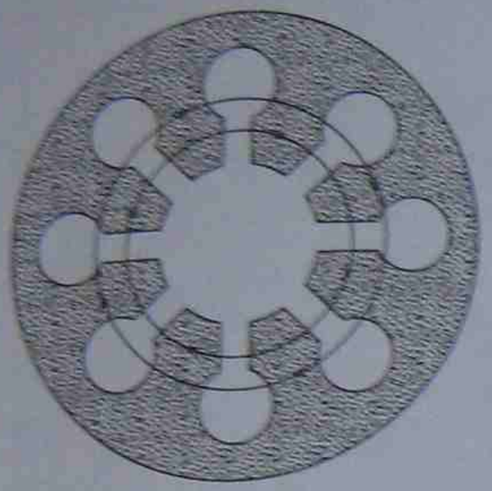


Fig. 7.36

One main disadvantage of the magnetrons described is that it is hard to modulate them by any of the usual modulation methods. Also the transit time sets a limit to the upper frequency which can be used. However, very high-power applications such as modern radar would be impossible without the magnetron, which is capable of producing 10 MW or more of pulsed power.

Klystrons

The problem of transit time can be overcome by use of a klystron. Originally this type of microwave tube was developed as a low-power device, but the power-handling capacity of modern tubes is high. Klystron tubes are superior to magnetrons in that they can function as an oscillator, amplifier or detector.

The klystron uses a process known as **velocity modulation** in which the velocity of the electron stream is varied as it moves through the tube. Figure 7.37 illustrates the basic method of producing this type of modulation. The arrangement consists of an electron beam of constant velocity directed towards two grid meshes. These grids extend out into the electron stream, and a source of RF voltage is connected across the grids.

As the electrons pass through the grids they are affected by the field set up between them by the RF generator. An electron that leaves grid 1 just before that grid goes positive is drawn back to it when the grid becomes positive. At the same time the electron is repelled by grid 2, thus causing it to slow down. An electron that leaves grid 1 when it is just going negative is repelled by grid 1 and attracted by grid 2. This electron is speeded up. Electrons that pass through the grids when the grids are at zero potential are neither speeded up nor slowed down, and they join the slowed-down electrons. The speeded-up ones catch up with those that go through unaffected, and in this way bunches of electrons are formed.

Figure 7.38 shows an industrial velocity-modulated klystron tube. A stream of electrons

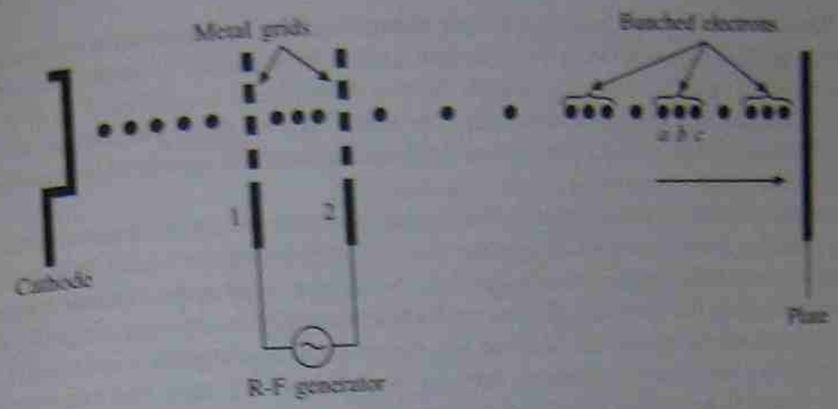


Fig. 7.37

emitted by the cathode is focused into a sharp beam by the action of G_1 which is connected to a suitable voltage. This electron beam is accelerated toward G_2 and G_3 by the high positive voltage of the voltage source V_1 (usually over 1 kV). G_2 and G_3 then act as the grids in Fig. 7.37 to bunch the electrons in their travel towards the collector plate. Since the distance between G_2 and G_3 is short, the change in velocity of the electrons is very slight, but this change is usable if an a.c. voltage V_2 is superimposed on the high d.c. voltage V_1.

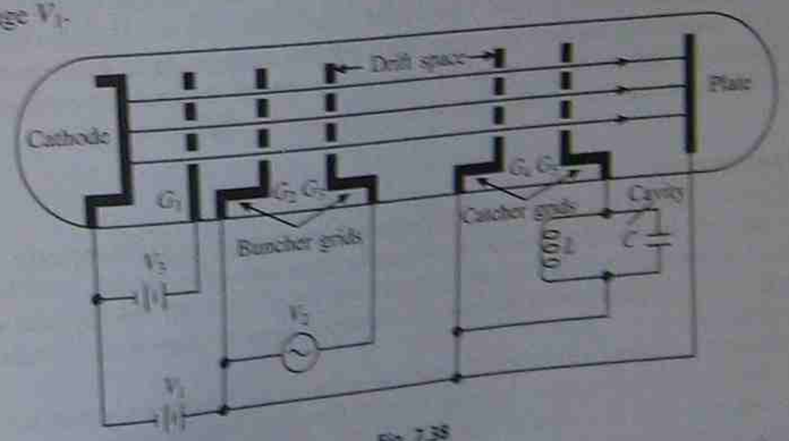


Fig. 7.38

In general, just as many electrons enter the buncher grids as leave, and since the electrons spend only a short time between the grids, there is no resultant current in the grids. Thus, the transit time of the electrons has a negligible effect on the operation.

To be of greater use the electrons are converted into a **density-modulated beam** from which energy can be extracted. There are several conversion methods. In the drift-tube process the electrons pass through a tube that is long compared to the grid spacing. This tube contains no electric or magnetic fields. The electrons accelerated by the buncher grids eventually catch up with those ahead and form bunches as they continue their path through the tube. Referring to the lettered bunch of Fig. 7.37, this means that electron *a* was accelerated, *b* was unaffected and *c* was decelerated to form a density-modulated beam.

The drift tube or space should not be long enough to allow the electrons to be separated by the repelling action between them. In their path to the collector plate these electrons reach grids G_1 and G_2 placed at a suitable distance from G_1 and G_2. In Fig. 7.38 grids G_1 and G_2 connect to a tuned resonant cavity. The electrons form dense bunches, as before, which move through grids G_1 and G_2, and if this current could be measured it would look as if it consisted of a pulsating d.c.

In order to understand the amplification process, consider a bunch of electrons between the grids, i.e. a strong current. To produce this strong current there would have to be a large potential difference between the grids. As the current flows in the external resonant cavity, this potential decreases. If it reverses while the bunch is between the grids, this will tend to reverse the current. To avoid this, the potential on the grids is reversed at an instant when there are few electrons between them. The bunch must last between the grids G_1 and G_2 not so long as half a cycle. Energy is extracted during this half cycle and very little is put back during the next half cycle.

Amplification has taken place because in the buncher grids the electrons are affected very little, but in the drift space this effect is given time to grow and the bunching becomes much more pronounced. Therefore the second set of grids is greatly energized by the bunched electron stream and the RF field is produced on the second set of grids, which are called the **catcher grids**. To operate effectively, the cavity must be tuned correctly and the catcher grids should not be spaced too far from G_1 and G_2.

To change an amplifier circuit into an oscillator, it is necessary to feed back a voltage of proper phase from output to input. This is done in the klystron by connecting a suitable length of transmission line from the output resonator (the catcher) to an input resonator (the buncher). The klystron is tuned by varying the size of the resonant cavities, by changing the spacing between the cavities or by varying the applied voltage.

Reflex klystrons

This type of klystron is a single-cavity klystron and functions as an oscillator only. It is a low-noise device and is used in low power applications below frequencies of 30 GHz. Its basic structure is shown in the cross-sectional diagram of Fig. 7.40. This klystron uses a single cavity wrapped around the tube and the output signal is taken from the tube by a coupling loop.

Following the electron path from the cathode to the cavity, the reflex klystron is very much like the two-cavity type, however, beyond the cavity there is a long drift space at the end of which is a repeller plate. When this plate is negative the electrons are repelled, which slows them down and repels them back to the buncher grids, thus causing oscillations.

When an RF voltage exists in the single-cavity resonator, the positive voltage at the cavity attracts the electrons and either accelerates or retards them, depending on the RF cycle. After having the buncher field the electrons travel towards the plate, are slowed down, stopped and then restricted by the buncher. This return action is intensified because the plate is negative, repelling the beam, and the buncher is positive, attracting it. The electrons, which received their initial acceleration from the accelerator grid, eventually return to this positive grid after passing through the buncher grids on their return path.

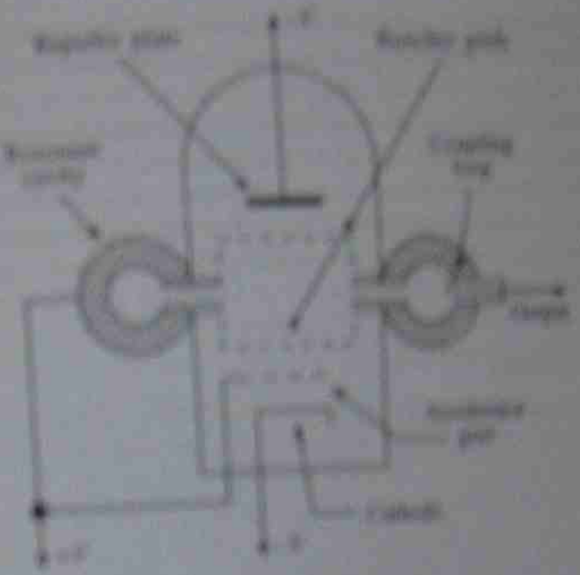


Fig. 7.39

The bunching operation is shown in Fig. 7.41. The lower one-wave voltage represents the voltage at the buncher grids. And the paths of three electrons that pass through the buncher grids at different instants in the RF cycle are shown at the centre of the diagram.

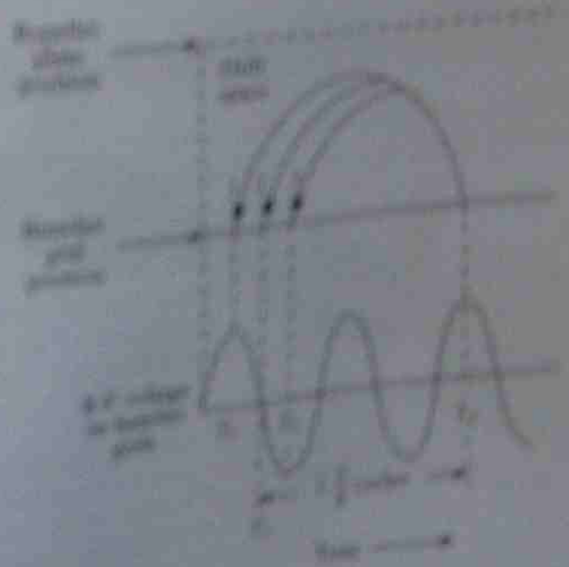


Fig. 7.40

Electron 1 passes through the buncher grids at time T_1, and the positive swing of voltage accelerates it through a large portion of the drift space towards the repeller plate. Electron 2 leaves later, when the RF voltage is zero, so its velocity is not affected. As a result it does not travel as far into the drift space as electron 1.

Electron 3 is decelerated by the buncher because the RF signal is in its maximum negative position, although the voltage is still positive. Electron 3 travels a much shorter distance into the drift space than the other two electrons. When proper adjustments are made, all three electrons arrive at the buncher at time T_4, when the voltage is at a positive peak. This satisfies the two conditions for oscillation where the feedback signal arrives in phase and with the correct amount of energy, i.e. regenerative feedback.

Figure 7.40 shows feedback occurring $1^3/_4$ cycles later if T_2 is taken as the average of T_1, T_2 and T_3. The bunches can spend the period of $^3/_4$, $1^3/_4$ and $2^3/_4$ cycles making the round trip and still maintain oscillations.

Travelling–wave tubes

For very wide-band applications the klystron's operation is a compromise between gain and bandwidth. If the gain is reduced enough to give the required bandwidth, the noise generated within the klystron may decrease the signal-to-noise ratio. Also, in the klystron tube the coupling between the electron beam and the field is limited due to the narrowness of the resonator gaps. Hence the transfer of signal energy is less efficient.

In order to overcome these deficiencies the travelling-wave tube was designed. The construction of this tube is shown in Fig. 7.41. The structure consists of an electron gun which produces a collimated beam of electrons. The electrons are accelerated along the tube towards the collector, which has a high positive potential. The slender section of the tube contains a helix of wire which is rigidly mounted on insulating supports in the long glass tube.

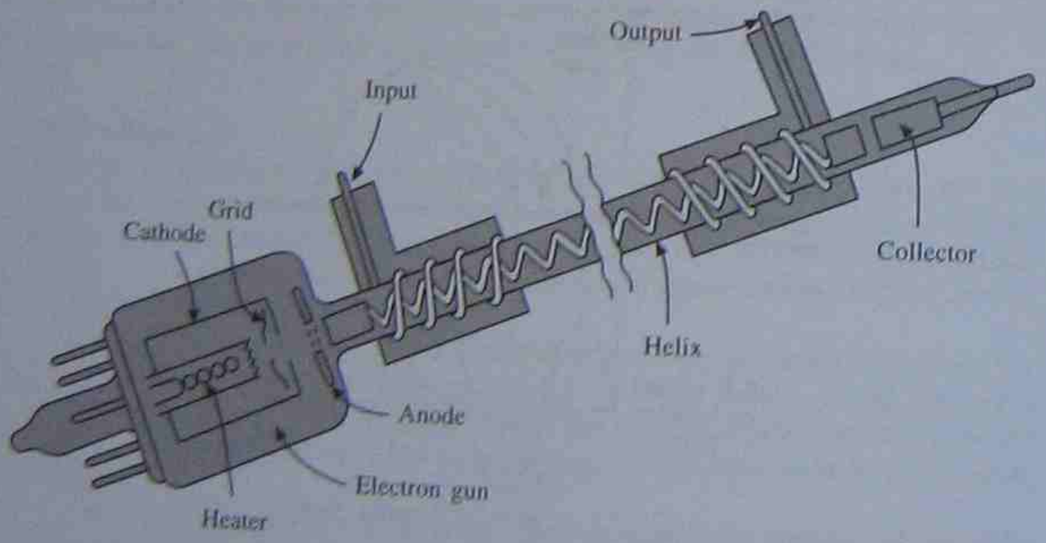


Fig. 7.41

The electron beam travels through the helix to the collector. Outside the helix there are two short spirals wound on the glass at each end of the helix, and these serve as the input and output connections. Outside the tube is a focusing magnet which serves to collimate the electrons.

The helix has inductance and capacitance which are effective in slowing down any wave travelling in it, and hence it functions as a delay line. This avoids one of the problems of the klystron, where the interaction between the field and the electrons is very short. In the travelling-wave tube the interaction can take place through the entire length of the tube.

With a beam of electrons travelling down the helix, a wave is injected on the end of the helix. This wave travels in the same direction as the electrons. By varying the collector voltage, we adjust the speed of the electrons so that the electrons tend to move slightly faster than the wave. Where the wave has a positive maximum it tries to attract the electrons and hence speeds them up. If the wave has a negative maximum it retards the electrons. Hence bunching occurs as in the klystrons. However as the electrons were travelling slightly faster than the wave in the first place, more energy is given up in the retarding than is extracted in the speeding up. This produces considerable gains up to 60 dB for frequencies of 100 GHz or more.

By proper matching and by using directional attenuators which will soak up the backward wave as it occurs, it is possible to avoid backward waves in amplifiers. When operating as an oscillator the backward reflection is permitted. The reflected wave then will travel forward in the right phase, be amplified, and so on, until the circuit reaches its peak amplitude of oscillation. This is termed a **backward-wave oscillator**.

The collector voltage or the voltage applied to the helix controls the speed of the electrons. Thus, when the travelling-wave tube is used as an oscillator, the collector or helix voltage can be used to control the oscillator frequency. Also the tube can be pulse-modulated, which is essential for certain applications.

7.10 Further problems

1. Calculate the cut-off frequency of the following modes in a rectangular waveguide which has the inside dimensions 4 cm by 4 cm for the following modes: TE_{10}, TM_{11}, TE_{01}, TM_{21} and TE_{22}
   Answer: 3.75, 5.3, 3.75, 8.4 and 10.6 GHz

2. A waveguide is used for operation at 10 GHz. If it has dimensions 2.3 cm by 1 cm, calculate the frequency range over which the dominant mode can propogate and explain why the recommended range of operation is in the X-band range of 8.2–12.5 GHz.

3. Calculate the size of a quarter-wavelength section of waveguide which is needed to match a junction between rectangular waveguides having dimensions 2.1 cm by 1.2 cm and 3.8 cm by 1.2 cm. Also determine the frequency at which higher-order modes would cause energy loss.
   Answer: 2.3 cm by 1 cm, 7.8 GHz

4. Determine the cut-off frequency and wavelength of a rectangular waveguide in the T_{21} mode if $a = 3$ cm and $b = 1$ cm.
   Answer: 18 GHz, 1.38 cm

5. A rectangular waveguide functions in the T_{10} mode with a free space frequency of 5.5 GHz. If the guide dimensions are $a = 5$ cm and $b = 2$ cm, determine
   (a) the cut-off frequency and wavelength;

Appendix B

Analysis of gain off resonance

Consider the circuit in Fig. B.1, where R_i is the resistance of the source. At resonance, from (4.6),

$$A_{V_0} = \text{Im}\, R_i \Omega \tag{B.1}$$

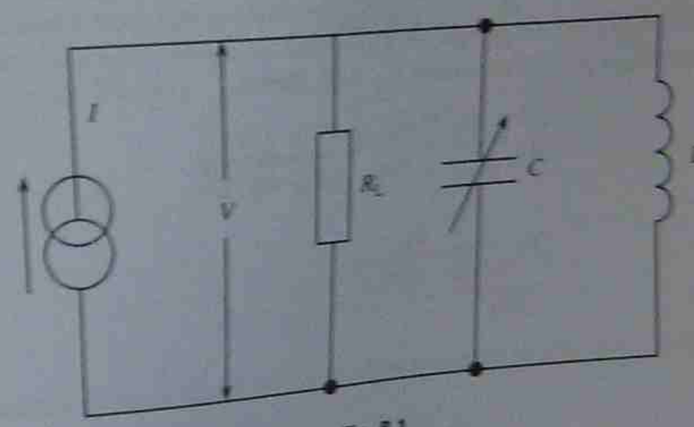


Fig. B.1

Also, from the circuit, the total current is given by

$$I = \frac{V}{R_i} + \frac{V}{i/j\omega C} + \frac{V}{j\omega L}$$

$$= V\left[\frac{1}{R_i} + j\left(\omega C - \frac{i}{\omega L}\right)\right] = \frac{V}{Y} \tag{B.2}$$

$$Z = \frac{1}{Y} = \frac{1}{1/R_i + j[\omega C - (1/\omega L)]} \tag{B.3}$$

From (B.2),

Rearranging gives

$$Z = \frac{R_i}{1 + j\omega C R_i [1 - (1/\omega^2 LC)]}$$

$$= \frac{R_i}{1 + jQ[1 - (\omega_o/\omega)\,2]}$$

Let $D = (\omega - \omega_o)/\omega_o$. Then

$$\left(\frac{\omega_o}{\omega}\right)^2 = \left(\frac{1}{1+D}\right)^2$$

Expanding this by the binomial theorem gives

$$\left(\frac{1}{1+D}\right)^2 = 1 - 2D + 3D^2 - 4D^2$$

All higher components can be ignored as D will generally be small. This gives

$$Z = \frac{R_i}{1 + jQ[1 - 1 + 2D]}$$

$$\frac{Z}{R_i} = \frac{1}{1 + j2QD} \qquad \text{(B.4)}$$

$$\therefore \quad \frac{Z}{R_i} = \frac{1}{\sqrt{1 + 4Q^2D^2}}$$

At resonance $V_{o1} = IR_i$. Off resonance $V_{o2} = IZ$. Hence

$$\frac{IZ}{IR_C} = \frac{V_{o2}}{V_{o1}} = \frac{A_V}{A_{V0}} = \frac{1}{\sqrt{1 + 4Q^2D^2}}$$

$$\therefore \quad A_V = \frac{A_{V0}}{\sqrt{1 + 4Q^2D^2}} \qquad \text{(B.5)}$$

Appendix C

Circuit analysis for a tuned primary amplifier

This analysis uses the equivalent T-network and a knowledge of two-port networks which may be obtained from any standard text.

Consider the circuit in Fig. 4.11(b), where R_{11} and R_{22} are the primary and secondary load resistances. We have

$$V_{11} - j\omega L_1 I_1 - j\omega M I_2$$

$$O = j\omega M I_1 - (R_{22} + j\omega L_2)\, I_2$$

Hence

$$Z_{11} = \frac{V_{11}}{I_1} = j\omega L_1 + \frac{\omega^2 M^2}{R_{22} + j\omega L_2} \qquad \text{(C.1)}$$

The secondary is untuned and will have a low reactance so that $\omega L_2 << R_{22}$. Hence

$$Z_{11} = j\omega L_1 + \frac{\omega^2 M^2}{R_{22}} \qquad \text{(C.2)}$$

This expression represents a series circuit consisting of L_1 and $R_s = (\omega^2 M^2)/R_{22}$. This is shown in Fig. 4.11(c). Using expression (4.3) will give the equivalent parallel resistance at port 1,1:

$$R_{P1} = \frac{\omega^2 L_1^2}{R_s} = \frac{\omega^2 L_1^2}{\omega^2 M^2 / R_{22}} \qquad \text{(C.3)}$$

The equivalent resistance (R_{P2}) appearing at the input is given by

$$R_{P2} = \frac{R_{11} R_{P1}}{R_{11} + R_{P1}} = \frac{R_{11}}{(1 + M^2/L_1^2)(R_{11}/R_{22})} \qquad \text{(C.4)}$$

Also $V = IZ = j\omega L_1 I_1$ since $\omega L_1 >> R_s$ (see (C.2)).

From the second hoop in Fig. 4.11(b),

$$V_{be2} = R_{22}I_2 = j\omega MI_1$$

Also since $I = g_m V_{be}$, the voltage gain at resonance,

$$A_{Vo} = \frac{V_{be2}}{V_{be1}} = \frac{g_m R_{11}(M/L_1)}{(1 + M^2/L_1^2)(R_{11}/R_{22})} \tag{C.5}$$

The effective Q factor (Q_{e1}) is given by

$$Q_{e1} = \frac{R_{p2}}{\omega L_1} \tag{C.6}$$

Hence,

$$Q_{e1} = \frac{R_{11}/\omega L_1}{(1 + M^2/L_1^2)(R_{11}/R_{22})} \tag{C.7}$$

As M actually controls the Q factor, the bandwidth is also affected by M. It is therefore possible to maximize the gain or bandwidth by selecting M. This is achieved by differentiating (C.7) and setting it to zero (maximum turning point in mathematical terms). When this is done the optimum value of M which will give maximum gain is found to be

$$\omega_o M = \omega_o L_1 \sqrt{\frac{R_{22}}{R_{11}}} \tag{C.8}$$

Using this optimum value reduces (C.7) to

$$Q_{e1} = \frac{Q_1}{2} \tag{C.9}$$

where Q_1 is the effective Q factor of the primary circuit ($R_{p2}/\omega L_1$). It can be seen that when the inductivity-coupled circuit is adjusted for maximum gain it will have twice the bandwidth of the tuned primary only ($BW = f_o/Q_{e1}$).

Appendix D

Circuit analysis for a tuned secondary

From Fig. 4.13 the loop equations are formed:

$$V_{11} = j\omega L_1 I_1 - j\omega M I_2$$

$$O = \left[R_2 + j\left(\omega L_2 - \frac{1}{\omega C_2}\right)\right] I_2 - j\omega M I_1$$

At resonance $\omega_o L_2 = 1/\omega_o L_2$ for the secondary tuned circuit,

$$\therefore \qquad I_2 = \frac{j\omega M I_1}{R_2} \tag{D.1}$$

Hence

$$Z_{11} = \frac{V_{11}}{I_1} = j\omega_o L_1 + \frac{\omega_o^2 M^2}{R_2}$$

and using current division between r_{ds} and Z_{11} gives

$$I_1 = I \frac{r_{ds}}{r_{ds} + j\omega L_1 + \omega_o^2 M^2/R_2}$$

As $r_{ds} >> \omega_o L_1$,

$$I_1 = I \frac{1}{1 + \omega_o^2 M^2/r_{ds} R_2}$$

Using (D.1) gives

$$V_{gs2} = \frac{-jI_2}{\omega C_1} - g_m V_{gs1} \frac{\omega_o M}{\omega_o C_2 R_2} \left(\frac{1}{1 + \omega_o^2 M^2/r_{ds} R_2}\right)$$

Resonance gives

$$\frac{1}{\omega_o C_2} = \omega_o L_2$$

so gain is given by

$$A_{V0} = \frac{V_{gs2}}{V_{gs1}} = g_m \omega_o M_1 \frac{Q_2}{1 + \omega_o^2 M^2 / r_{ds} R_2} \tag{D.2}$$

where $Q_2 = \omega_o L_2 / R_2$. As with primary tuning, the effective Q factor is given by

$$Q_{e2} = \frac{Q_2}{1 + \omega_o^2 M^2 / r_{ds} R_2} \tag{D.3}$$

If (D.2) is differentiated and set to zero the optimum value for M can be determined from

$$\omega_o M = \sqrt{r_{ds} R_2} \tag{D.4}$$

The bandwidth will therefore be given by

$$BW = \frac{f_o}{Q_{e2}} = \frac{2 f_o}{Q_2}$$

This is twice the bandwidth of the resonant circuit.

Appendix E

Circuit analysis for double tuning

In the equivalent circuits shown in Figs. 4.14(a) and 4.14(b), the following points should be noted:

(i) The series and parallel resistances are combined to give:

$$R_{11} = \frac{\omega_o^2 L_1^2}{r_1} + R_1$$

$$R_{22} = \frac{\omega_o^2 L_2^2}{r_2} + R_2$$

(ii) The Norton generator is replaced by a Thevenin generator.

(iii)
$$Q_1 = Q_2 = \frac{\omega_o L_1}{R_{11}} = \frac{\omega_o L_2}{R_{22}}$$

(iv)
$$V_o = -\frac{\mathrm{j}}{\omega_o C_2} I_2$$

Using $I_2 = Y_T V_{11}$, then

$$I_2 = \frac{\mathrm{j} g_m}{\omega C_1} Y_T V_1$$

and the gain is given by

$$\frac{V_0}{V_1} = -\frac{\mathrm{j}}{\omega_o C_2} \frac{\mathrm{j} g_m}{\omega_o C_1} Y_T = g_m \omega_o^2 L_1 L_2 Y_T \tag{E.1}$$

At resonance the admittance Y_T may be assembled from the z parameters

$$Z_f = j\omega_o M = \mathrm{j}\omega_o k \sqrt{L_1 L_2}$$

$$Z_i = R_{11} + \mathrm{j}\left(\omega L_1 - \frac{1}{\omega C_1}\right) \equiv \frac{\omega_o L_1}{Q} (1 + \mathrm{j}2QD)$$

Note that

$$\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} = 1 + D - (1 - D) = 2D$$

and if D is small then

$$\frac{1}{1 + D} \equiv 1 - D$$

When $Z_L \equiv -j/\omega_o C_2$ the following can be deduced:

$$Z_o + Z_L = R_{22} = j\left(\omega L_2 - \frac{1}{\omega C_2}\right) \equiv \frac{\omega_o L_2}{Q}(1 + j2QD)$$

hence

$$Y_T = \frac{1}{z_f - z_i\,(z_o + z_L)/z_f} = \frac{kQ^2}{\omega_o\sqrt{L_1 L_2}\,[4QD - j(1 + k^2Q^2 - 4Q^2D^2]} \quad \text{(E.2)}$$

From (E.1) and (E.2) the gain at resonance becomes

$$A_V = \frac{g_m\omega_o k\sqrt{L_1 L_2}\;Q^2}{4QD - j(1 + k^2Q^2 - 4Q^2D^2)}$$

which in magnitude terms becomes

$$A_V = g_m\omega_o\sqrt{L_1 L_2}\;Q\frac{kQ}{\sqrt{(1 + k^2Q^2 - 4Q^2D^2)^2 + 16Q^2D^2}} \quad \text{(E.3)}$$

The frequency deviation D at which the gain is maximum occurs by maximizing (E.3). This gives

$$D(4Q^2D^2 + 1 - k^2Q^2) = 0 \quad \text{(E.4)}$$

Two peaks occur from this quadratic:

$$f_1 = f_o\left(1 - \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right) \quad \text{(E.5)}$$

$$f_2 = f_o\left(1 + \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right) \quad \text{(E.6)}$$

Note that when $k^2Q^2 = 1$, critical coupling occurs and

$$k = k_c = \frac{1}{Q} \quad \text{(E.7)}$$

The double peaked response is shown in Fig. E.1. Note from this diagram that the two peaks coincide when $D = 0$ and for coupling values greater than $1/Q$ the response shows a double peak and is overcoupled.

The magnitude of the gain at a peak (A_p) is given as

$$A_p = \frac{g_m\omega_o\sqrt{L_1 L_2}\,kQ}{\quad} \quad \text{(E.8)}$$

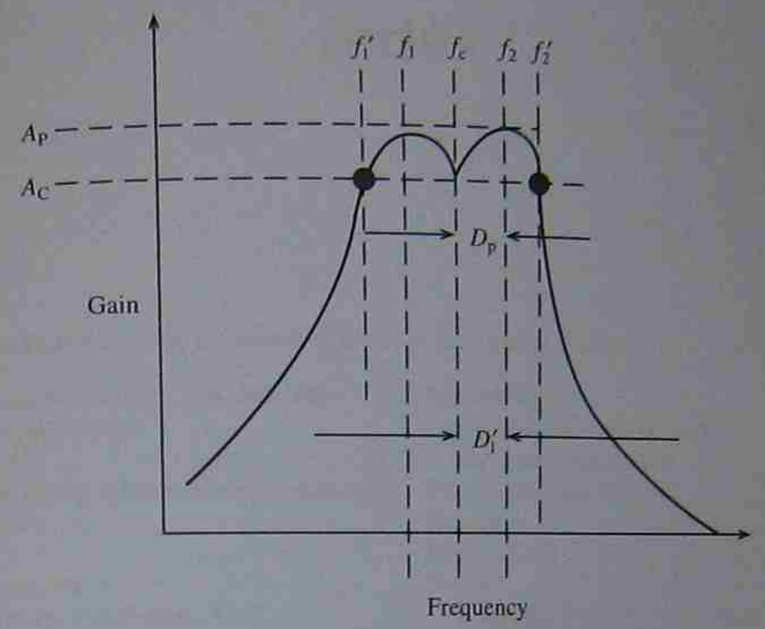


Fig. E.1

When $D = 0$

$$A_c = A_p\frac{2kQ}{1 + k^2Q^2} \quad \text{(E.9)}$$

The magnitude of the dip in Fig. E.1 is dependent on transformer design. The ripple ratio G may be given by

$$G = \frac{A_p}{A_c} = \frac{1 + k^2Q^2}{2kQ}$$

hence

$$kQ = G - \sqrt{G^2 - 1} \quad \text{(E.10)}$$

Note $kQ > 1$ and the value of (E.10) gives a value of kQ for a given ripple.

The bandwidth between the frequencies at which the gain drops to A_c is the practical bandwidth generally used:

$$2D' = \sqrt{2}\,(f_2 - f_1) \quad \text{(E.11)}$$

The 3 dB bandwidth is established between the D' frequencies when $G = \sqrt{2}$ so that $kQ = 2.414$

$$BW = f_2' = f_1' = \frac{3.1f_o}{Q} \quad \text{(E.12)}$$

Also

It can be seen from this that the double tuned circuit can substantially increase the bandwidth while retaining steep roll-off.

Index

Numbers in **bold** face refer to figures; numbers in *italics* refer to tables

Active filters, 98–101, **99**, **100**, **101**, **102**
  buffering effect, 98
  tuning, 98
Advantages, double sideband modulation (d.s.b.), 58, **59**
AM:
  techniques, 58–9
  wave, power distribution, 55–8
Amplifiers:
  ceramic tuned, 184–8, **186**, **187**, **188**
  crystal tuned, 184–8, **186**, **187**, **188**
  double tuning, 181–4, **182**
  gain, 164–6
  integrated tuned, 188–91, **190**, **192**
  loading, 166–9, **166**, **168**
  operational, 2–3
  PLL, 279–80
  saturation, 3
  single-stage, 168–9, **168**
    tuned, 196
  testing, 192, **192**, **193**, **194**
  transformer-coupled, 173, **173**
  tuned primary, 173–7, **174**, **175**, 198
  tuned secondary, 177–81, **178**, **179**, 199
  unstable, 3
  voltage, **2**
Amplifying devices, 4
Amplitude modulation, 51, 53–9, **54**, **55**, **58**, *see also* AM
Analogue modulation, 53–9
Antenna:
  input impedance, 55
  resistance, 55–6
  systems, half-wavelength, 52
Armstrong oscillators, 23–4, **23**

Backward-wave oscillator, 367
Balanced modulator, 60–1, **61**
  FSK 74
Bandpass filters, 120–4, **121**, **122**, **124**
  buffering, 121
Bandwidth:
  and Carson's rule, 66–9, **67**
  and gains, **163**, 164–6
Barkhausen criterion, 5
Baseband, 53
Baud rate, 75
Bessel:
  functions, 64–7
  graphs, **369**
  table, *370*
Binary phase shift keying, *see* BPSK
Bipolar junction transfer (BJT), 6
Block diagram, television receiver, 51–3, **51**
Bode plot, 281–3, **282**, 284
BPSK, 76–8, **77**
  demodulation, 77–8, **77**
Buffering:
  active filters, 98
  bandpass filters, 121
Butterworth:
  first-order filter, 115, **115**
  polynomials, *108*
  responses, 100, **101**, 107, **107**

Capacitors:
  ceramic, 133
  electrolytic, 133
  polyester, 133
  polystyrene, 132
  selection, filters, 132–3
  silvered mica, 132
  tantalum, 133
Capture range, 276–7, 290
Carrier:
  amplitude, 65
  signals, QPSK, 78, **79**
Carson's rule, and bandwidth, 66–9, **67**
Cascading, second-order filters, 106
Catcher grids, 364
Cavity resonators, 347–52, **348**, **349**, **350**, **351**
  progression, **348**

Ceramic:
capacitors, 133
filter 185
tuned amplifiers, 184–8, **186**, **187**, **188**
Channel:
separation, 52
signals, integrator, 96
Chebyshev:
polynomials, *108*
responses, 100, **101**, 107, **107**, 111
Circuit analysis:
double tuning, 377–9
tuned primary amplifier, 373–4
tuned secondary amplifier, 375–6
Circuits, inductance-capacitance (LC), 3, 4
Circulators, microwaves, 354–6, **354**, **355**
Clapp oscillators, 21–3, **21**
frequency division multiplexing 21–2
Class A:
power amplifier, 246–7
(single-ended) amplifier, 230–4, **231**
power rating, 230–1, **232**
practical analysis, 234
Class B:
complementary pair push-pull, 236–44, **236**, **238**, **243**, 247–8
practical analysis, 237–44
push-pull amplifier, 234–5, **235**, **236**
Closed-loop:
gain, 4, 9
voltage, 6
Collector:
currents, 234, 238
dissipation, 233
Colpitts oscillator, 13–17, **14**, **15**, 28, **29**, 69, 70
advantage of, 20
crystal-controlled, 30–1
design, 14–16, **15**
input resistance, 14
split capacitance, 13–14
transistor, 16–17
Communication systems, **1**
Compensation analysis, 283–90, **284**, **285**, **286**
Complementary:
amplifier, 240
symmetry circuit, 238
Components:
filters, 132–3
selection, frequency stability, 28
Continuous winding, 169
Coupling factor, 345
Critical coupling, tuned primary, 176
Crossover, distortion, 235, **237**, **238**
Crosstalk, 51
Crystal:
choice of, 29, 30
controlled Colpitts oscillator, 30–1
cuts, 25
dimensions, 185
oscillators, 24–5, **24**
crystal cuts, 25
overloading, 25
package capacitance, **24**, 25
parallel mode, 24
series mode, 24
types of, 25–6, **26**
piezo-electric, 3, 4
resonance frequencies, 185
selectivity, 185
stability, 4
tuned, amplifiers, 184–8, **186**, **187**, **188**
Cut-off:
frequency, 98, 339–44, **340**, **341**
rectangular waveguide, 340–1
and roll-off rate, 99–100, **99**, **100**
and saturation, 220–2, **221**, 233, **224**, 227

Data sheets:
modulation systems, 83–94
oscillators, 35–49
Decibel, 229–30
Delay networks, PLL, 283
Demodulators, 60–1, **61**
FM, 71–3, **71**, **72**, **73**
ouputs, **78**, 80
phase comparator, 71
phase-locked loop, 71, **71**
ratio detector, 72–3, **72**, **73**
Demultiplexer, 95
Denormalization, 108
Density-modulated beam, 363
Depth of modulation, 54–5, **54**, 56–7
Design:
Colpitts oscillator, 14–16, **15**
first-order filters, 104–6, **105**, **106**
Hartley oscillator, 20
Destination, 1
Deviation ratio, 65
maximum permissible value, 69
zero, 67
Dibit code, QPSK, 78–9
Differentially encoded dibit (DED), 78–9
Digital modulation, 73–80, **74**, **75**, **77**, **79**
Dimensions, crystal, 185
Directional coupler, 345–6, **345**, **346**
coupling factor, 345
directivity, 345
insertion loss, 345
Directivity, 345
Distortion, 221
crossover, 235, **237**, **238**
power amplifiers, 254
transmission line, 332
Double sideband modulation (d.s.b.), 58
advantages, 58, **59**
Double sideband suppressed carrier modulation (d.s.b.s.c.), 58
Double tuning:
amplifiers, 181–4, **182**
circuit, 72
transformer, 199
Dynamic impedance, tuned circuits, 164

Efficiency, 239
and power, 224–8
Electrolytic capacitors, 133
Emitter amplifier, 212–3, **224**
Error voltage, 276
Extremities, load lines, 223

Feedback network, 3
Filter response, 133–6
Filters, 95–160
active, 98–101, **99**, **100**, **101**, **102**
bandpass, 120–4, **121**, **122**, **124**
capacitor selection, 132–3
cascading, 97
components for, 132–3
first-order, 101–6, **102**, **104**, **105**, **106**
and frequencies, 96
high-pass, 97, **97**
low-pass, 97, **97**, 101–4, **102**, **104**
notch, 127–32, **128**, **129**, **130**, **131**, **132**
order of, 99, **100**
passive, 97, **97**
Q factor, 130
resistor selection, 132
response, 98, **99**
second-order, 106–9, **107**, **108**
selectivity, 130
switched capacitor, 124–6, **125**, **126**
transfer function, 110–12, **111**
First-order filters, 101–6, **102**, **104**, **105**, **106**
Butterworth, 115, **115**
design, 104–6, **105**, **106**
high-pass, 103, **104**
Fixed frequency, twin-T, 11, **13**
Free-running frequency, IM566, 280–1
Frequency:
components, modulation, 54
division multiplexing, Clapp oscillators, 21–2
and filters, 96
fixed, 11, **13**
intermediate, 2
modulation, 51, 61–9, **62**, **63**, **65**, **66**, **67**
natural, 3–4
resonant, 3–4
response, power amplifiers, 252
shift keying, *see* FSK
signal generators, 136
stability:
component selection, 28
loading effects, 28
oscillators, 26–31
power supply coupling, 28
temperature variations, 28
synthesis, PLL, 296–301, **296**, **297**, **298**, **299**, **300**
Frequency-determining network, 3, **3**
Frequency-modulated transmitter, 161, **161**
FSK, 73–6, **74**, **75**
balanced modulator, 74
frequencies used in, 74
waveform, 75

Gain off response, 371–2
Gain resonance, tuned secondary, 177–8
Gains:
amplifiers, 164–6
and bandwidth, **163**, 164–6
Group velocity, 330–1
Guard band separation, 96
Guide dimensions, waveguide characteristics, 342–3

h-parameters, 218–19
Half-power points, 164
Half-wavelength, antenna systems, 52
Harmonic reduction, 96
Harris CA3028A, 188–91, **190**
Harris HA721031–3, **32**
Hartley oscillator, 18–20, **18**, **19**, 69
design, 20
split inductance, 18
HCC4046B, PLL, 293–5, **294**, **295**
Heat sink, 230
Heterodyning, 296

High-pass filters, 97, **97**
  first-order, *103*, **104**
  second-order, *113–19*, **114**, **115**, **116**, **117**, **118**, **119**
Hybrid parameters, *see h-parameters*

Identical components, 113
IF 2:
  amplifier, 161–2
Impedance, 187
In phase signal feedback, 3
Inductance-capacitance (LC) circuits, 3, 4
Information signal, 1
Input resistance, Colpitts oscillator, 14
Insertion loss, 345
Integrated circuit:
  oscillators, 31–3, **32**
  power amplifiers, 248–51
Integrator, channel signals, 96
Intermediate frequency, *see* IF
Intermodulation distortion, 51
Isolators:
  Faraday rotation, 354, **355**
  microwaves, 354–6, **354**, **355**

JK flip-flops, 297

Klystrons, 362–6, **363**, **365**
  reflex, 364–7, **365**
  travelling-wave tubes, 366–7, **366**
  velocity modulation, 362–3, **363**

LC oscillators, 13–24, **14**, **15**, **18**, **21**, **23**
Lead-lag:
  circuits, 281
  compensation, 284, **285**
Lead-lag compensation, advantages of, 286
LM380, 249–50, **249**
  pinout diagram, **249**
LM566, 280–1, **280**
  free-running frequency, 280–1
Load lines, 223
  a.c., 232
  d.c., 223, 227, 231
  extremities, 223
Loading, 332
  amplifiers, 166–9, **166**, **168**
  effects, frequency stability, 28
Lock range, PLL, 288–90
Loop phase shift, 4, **5**
Loop-gain, 4
  closed, 4

PLL, 286–7, 290
Low-level signal, 2
Low-pass:
  filter, 97, **97**, 101–4, **102**, **104**, 281
    phase lag, 97
    third-order, 119–120, 123
  second-order, 106–9

Maximum permissible value, deviation ratio, 69
Measurements, power amplifiers, 252–4, **252**
MF100, switched capacitor filters, 126–7, *137–9*
Microwaves, 329–68
  active devices, 356–67
  circulators, 354–6, **354**, **355**
  isolators, 354–6, **354**, **355**
  multicavity magnetrons, 357–67, **357**, **358**, **359**, **360**, **361**, **362**, **363**, **365**
  passive components, 344–56
  phase delay, 330–1
  probes, 352–3, **352**, **353**
  propagation velocity, 330–1
  rectangular waveguide, 338–9, **339**
  reflection coefficient, 333–5, **334**
  solid-state devices, 356
  transmission modes, 337–8, **338**
  tubes, 356–7
  wave reflection, 333–5, **334**
  waveguide characteristics, 337–44, **337**, **338**, **339**, **340**, **341**
Mixer, 277
Modulation:
  depth of, 54–5, **54**, 56–7
  digital, 73–80, **74**, **75**, **77**, **79**
  double sideband, 58
  factor, 54–5, **54**
  frequency components, 54
  index, 63
  noise reduction, 67
  peak angular frequency shift, 62
  requirements for, 51
  signal, 53, **54**
  spectrum diagram, **67**
  systems, 51–94
    data sheets, 83–94
Modulators:
  balanced, 60–1, **61**
  FM, 69–71, **70**
  Philips MC 149660, **60**, **61**
  reactance, 69
  tuning range, 70–1, **70**
Motorola MC1350, 188–91, 199

Multicavity magnetrons, 357–67, **357**, **358**, **359**, **360**, **361**, **362**, **363**, **365**
  disadvantages, 362
  structure, 360, **360**
  transit time, 359
Mutual conductance, 167

Natural frequency, 3–4
Noise:
  filtering, 96
  reduction, modulation, 67
Normalization, 109
  tables:
    second-order filters, *109*
    using, 112–13
Notch:
  filters, 11, 127–32, **128**, **129**, **130**, **131**, **132**
    state variable, 129–32, **130**, **131**, **132**
    twin-T network, 128–9, **128**, **129**
  oscillators, 12–13, **13**

Op-amp version:
  phase-shift oscillator, 7, **7**
  Wien bridge oscillator, 9
Open-circuited termination, 333
Operational:
  amplifier, 2–3
  considerations, PLL 276–7, **276**
Oscillation, principles, 2–3
Oscillators, 1–49
  Armstrong, 23–4, **23**
  Clapp, 21–3, **21**
  Colpitts, 13–17, **14**, **15**
  crystal, 24–5, **24**
  data sheets, 35–49
  frequency stability, 26–31
  Hartley, 18–20, **18**, **19**
  integrated circuit, 31–3, **32**
  LC, 13–24, **14**, **15**, **18**, **21**, **23**
  local, 1–2
  notch, 12–13, **13**
  phase–shift, 6–7, **6**, **7**
  RC, 5–13, **6**, **7**, **8**, **9**, **10**
  receiver, 1–2
  requirements, 3–5, **3**
  structure, 3–5, **3**
  twin-T, 11–13, **12**, **13**
  variable, 8
  voltage, 277
  Wien bridge, 8–11, **8**, **9**
Oscillatory frequency, 6
Oscilloscope, and signal generators, 133–6
Output power, power amplifiers, 252
Output waveform, 9

Package capacitance, crystal oscillators, **24**, 25
Parallel mode, crystal oscillators, 24
Parallel plate waveguide, 339–40, **340**
Pass bands, 98, **99**
Passive components, microwaves, 344–56
Passive filters, 97, **97**
Peak angular frequency shift, modulation, 62
Phase:
  comparator, demodulators, 71
  delay, microwaves, 330–1
  detector, 277–9, **278**, **279**
    gain factor, 278
  lag, 281
    low-pass filters, 97
  shift, 8
  velocity, 330
Phase-locked loops, *see* PLL
Phase-shift:
  coefficient, 331
  oscillators, 6–7, **6**, **7**
    op-amp version, 7, **7**
Philips MC 149660, **60**, **61**
Pierce oscillator, 26, **27**
Piezo-electric crystals, 3, 4
PLL, 75–6, **75**, 275–328
  565, 291–3
  amplifiers, 279–80
  block diagram, **276**
  compensation, 281–90, 283–90, **284**, **285**, **286**
  delay networks, 283
  demodulators, 71, **71**
  elements, 277–81
  free running frequency, 76
  frequency synthesis, 296–301, **296**, **297**, **298**, **299**, **300**
  HCC4046B, 293–5, **294**, **295**
  integrated, 290–3
  lock range, 288–90
  loop gain, 286–7, 290
  operational considerations, 276–7, **276**
  output, **75**
  prescaling, 298–300
Polyester capacitors, 133
Polystyrene capacitors, 132
Power:
  amplifiers, 217–74
    applications, 217–**17**
    distortion, 254
    frequency response, 252

Power (continued)
measurements, 252–4, **252**
output power, 252
transistor characteristics, 218–21, **218**, **220**, **221**
dissipation, 239–40
curve, 232
distribution, AM wave, 55–8
and efficiency, 224–8
rating, class A (single-ended) amplifier, 230–1, **232**
supply coupling, frequency stability, 28
Practical analysis, class B complementary pair push-pull, 237–44
Prescaling:
PLL, 298–300
ratio, 300–1
two-modulus, 299, **299**
Principles, oscillation, 2–3
Probes, 352–3, **352**, **353**
Propagation:
constant, 331–2
secondary constants, 331–2
velocity, 332
microwaves, 330–1
Public address system, 217

Q factor, 166, 174, 178
filters, 130
tuned circuits, 163–4, **163**
Q-point, 223, 232
QPSK, 76, 78–80, **79**, **80**
advantages, 78
carrier signals, 78, **79**
dibit code, 78–9
Quadrature phase shift keying, *see* QPSK
Quiescent point, *see Q*-point

Radiation resistance, 55–6
Radio frequency, *see* RF
Ratio detector, demodulators, 72–3, **72**, **73**
RC oscillators, 5–13, **6**, **7**, **8**, **9**, **10**
Reactance modulators, 69
Receiver block, 1
Rectangular waveguide, 338–9, **339**
cut-off frequency, 340–1
Reflection coefficient, microwaves, 333–5, **334**
Reflex klystrons, 364–7, **365**
bunching operation, 365, **365**
Requirements, oscillators, 3–5, **3**
Resistance–capacitance, circuits, 3, 4
Resistor selection, filters, 132
Resonance frequencies, 3–4
crystal, 185
Responses:
Butterworth, 107, **107**
Chebyshev, 107, **107**, **114**
RF, power amplifiers, 161–2, 251–2, **251**
Roll-off rate, 98
and cut-off frequency, 99–100, **99**, **100**

Sallen-Key circuit, 107–8, **107**, 111, **111**, **114**
Saturation:
amplifier, 3
and cut-off, 220–2, **221**, **224**, 227, 233
Second-order filters 106–9, **107**, **108**
cascading, 106
high-pass, 113–19, **114**, **115**, **116**, **117**, **118**, **119**
low-pass 106–9
normalization tables, *109*
Secondary constants, propagation, 331–2
Selectivity:
crystal, 185
filters, 130
Series mode, crystal oscillators, 24
Short-circuited termination, 333
Signal:
feedback, in phase, 3
generators:
frequency, 136
and oscilloscope, 133–6
low-level, 2
Silvered mica, capacitors, 132
Single sideband suppressed carrier modulation (s.s.b.s.c.), 58, **59**
Single-ended transistor amplifier, 244–5
Single-stage, amplifiers, 168–9, **168**, 196
Skin effect, 338
Small signal voltage amplifiers, 227–9, **228**, **229**
Solid-state devices, microwaves, 356
Spectrum:
analyser, 192
diagram, modulation, **67**
Split:
capacitance, Colpitts oscillators, 13–14
inductance, Hartley oscillator, 18
Stability, crystals, 4
Standing wave, 333
ratio, 335–6, **336**
State variable, notch filters, 129–32, **130**, **131**, **132**
Stop bands, 98, **99**
Structure, oscillators, 3–5, **3**
Sweep frequency, 136, **136**
Switched capacitor filters, 124–6, **125**, **126**
MF100, 126–7, *127–9*
monolithic, 126–7

T-junctions, 346, **347**
E-field, 346
H-field, 346
T-network, **329**, 330
Tantalum capacitors, 133
Tapping, tuning coils, 169–72, **170**, **172**
TBA 820M, 250
TDA2006, 250–1
Tektronix power measurement oscilloscope, 254
Television receiver, block diagram, 51–3, **51**
Temperature variations, frequency stability, 28
Termination, 333–4, **335**
open-circuited, 333
short-circuited, 333
Thermal runaway, 227
Third-order, low-pass filter, 119–20, 123
Time-constant network, 4
Time-division multiplexing (TDM), 95, **95**
Total power, 239
Transformer-coupled amplifiers, 173, **173**
Transistor:
bias, 221–7, **222**, **223**, **224**, **225**, **226**
characteristics, 219–21, **220**, **221**
power amplifiers, 218–21, **218**, **220**, **221**
Colpitts oscillator, 16–17
Transmission:
lines, 329–30, **329**
distortion, 332
medium, 1
Transmitter block, 1
Transverse electric mode, 338
Transverse magnetic mode, 338
Travelling waves, 330
Travelling-wave tubes, klystrons, 366–7, **366**
Tubes:
microwaves, 356–7
miniaturization, 357
Tuned:
amplifiers, 161–215
primary, 173–7, **174**, **175**
circuit analysis, 373–4
critical coupling, 176
secondary, 177–81, **178**, **179**
circuit analysis, 375–6
gain resonance, 177–8
circuits, 162–3, **162**
dynamic impedance, 164
Q factor, 163–4, **163**
Tuning:
active filters, 98
coils, tapping, 169–72, **170**, **172**
range, modulators, 70–1, **70**
Turns ratio, 233, 241, 246
Twin-T, 11–13, **12**, **13**
fixed frequency, 11, **13**
notch filters, 128–9, **128**, **129**
problems with 11

Unstable amplifier, 3

Varactor, 69–70
Variable oscillators, 8
VCO, 71, 275–328
as an integrator, 283
d.c. correction voltage, 278
LM566, 280–1, **280**
Velocity:
modulation, klystrons, 362–3, **363**
propogation, 332
Voltage:
amplifier, **2**
divider bias, 225–7, **226**
Voltage-controlled oscillator, *see* VCO

Wave reflection, microwaves, 333–5, **334**
Waveguide characteristics, 337–44, **337**, **338**, **339**, **340**, **341**
attenuation loss, 342–3
guide dimensions, 342–3
parallel plate, 339–40, **340**
rectangular, 338–9, **339**
wavelength, 341–2
Waveguide junctions, 346–7, **346**, **347**, **348**
T-junctions, 346, **347**
Wayne-Kerr bridge, 11
Wien bridge, 8–11, **8**, **9**
oscillator, 26, **27**, 29–30, **30**
op-amp version, 9

Zeners, 10