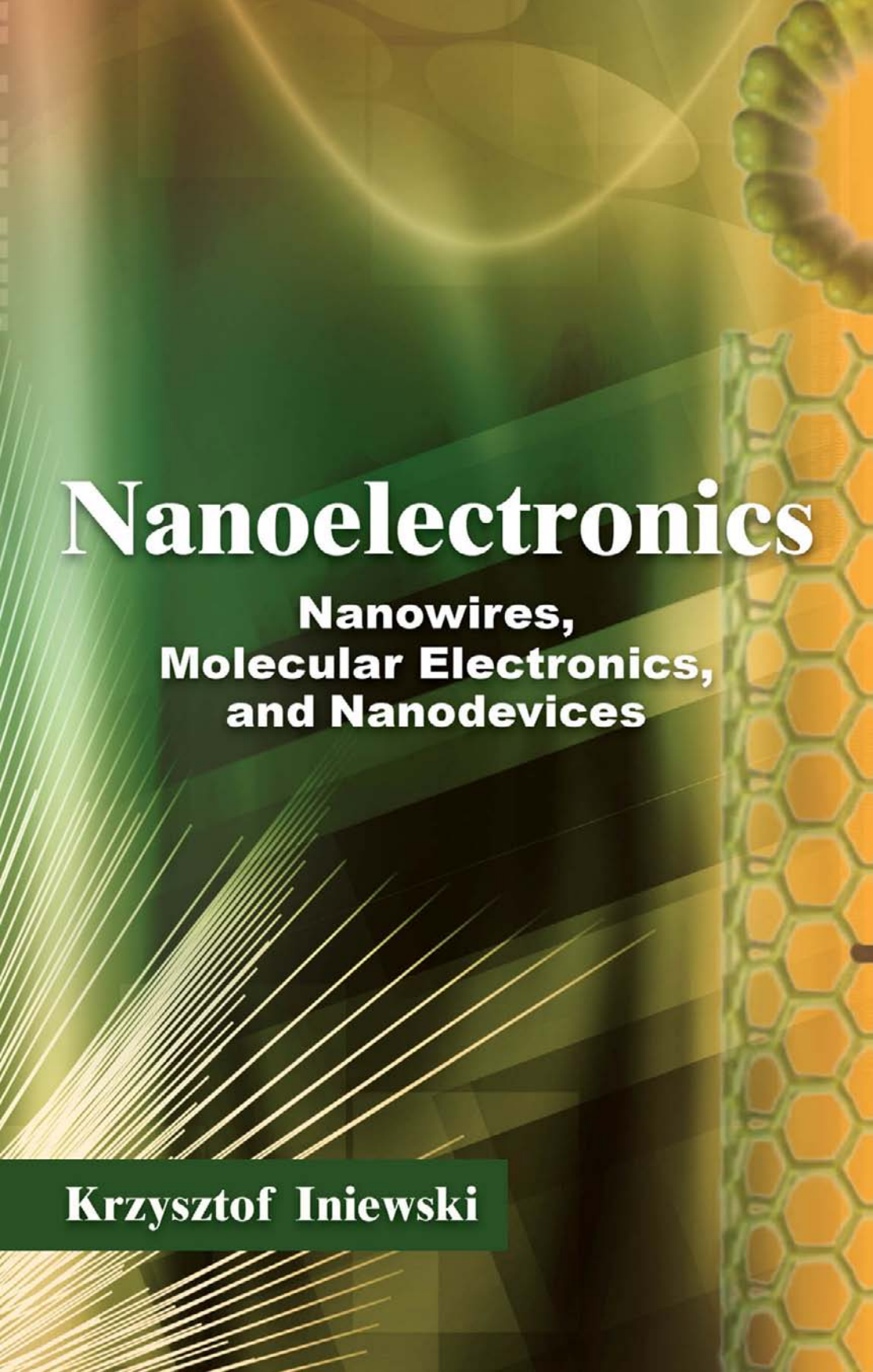

Nanoelectronics
Nanowires,
Molecular Electronics,
and Nanodevices
Krzysztof Iniewski

Nanoelectronics

About the Editor

Dr. Krzysztof (Kris) Iniewski is managing R&D developments at Redlen Technologies, Inc., a startup company in British Columbia. He is also Executive Director of CMOS Emerging Technologies, Inc. (www.cmoset.com). His research interests are in hardware design for biomedical and networking applications. From 2004 to 2006, he was an associate professor in the Electrical Engineering and Computer Engineering Department of the University of Alberta, where he conducted research on low-power wireless circuits and systems. During his tenure in Edmonton, he published *Wireless Technologies: Circuits, Systems and Devices*.

From 1995 to 2003, he was with PMC-Sierra and held various technical and management positions. He led development of a number of VLSI chips used in optical networks during his tenure there. From 1990 to 1994, prior to joining PMC-Sierra, he was an assistant professor at the University of Toronto's Electrical Engineering and Computer Engineering department. Dr. Iniewski has published more than 100 research papers in international journals and conferences. He holds 18 international patents granted in the United States, Canada, France, Germany, and Japan. He received his Ph.D. in electronics (honors) from the Warsaw University of Technology (Warsaw, Poland) in 1988. Together with Carl McCrosky and Dan Minoli, he is an author of *Data Networks—VLSI and Optical Fibre*, 2008. He recently edited *Medical Imaging Electronics*, 2009; *VLSI Circuits for Biomedical Applications*, 2008; *Circuits at Nanoscale: Communications, Imaging and Sensing*, 2008; and *Next Generation Networks*, 2010. Kris can be reached at kris.iniewski@gmail.com.

Nanoelectronics

Nanowires, Molecular Electronics, and Nanodevices

Edited by

Krzysztof Iniewski

New York Chicago San Francisco
Lisbon London Madrid Mexico City
Milan New Delhi San Juan
Seoul Singapore Sydney Toronto

The McGraw-Hill Companies

ISBN: 978-0-07-166449-3

MHID: 0-07-166449-1

The material in this eBook also appears in the print version of this title: ISBN: 978-0-07-166448-6, MHID: 0-07-166448-3.

Contents

This page intentionally left blank

List of Authors

Chuan Cai *Department of Mechanical Engineering, Louisiana State University, Baton Rouge, LA* (CHAP. 11)

Sandro Carrara *EPFL—Swiss Federal Institute of Technology, Lausanne, Switzerland* (CHAP. 9)

Gael F. Close *IBM Research Laboratory, Zurich, Switzerland* (CHAP. 3)

Stephen R. Diegelmann *Johns Hopkins University, Baltimore, MD* (CHAP. 10)

Zhiyong Fan *University of California at Berkeley, Berkeley, CA* (CHAP. 4)

Luigi Fortuna *Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi, Università degli Studi di Catania, Italy* (CHAP. 5)

Mattia Frasca *Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi, Università degli Studi di Catania, Italy* (CHAP. 5)

Bonnie L. Gray *Engineering Science, Simon Fraser University, Burnaby, BC, Canada* (CHAP. 8)

Dongsheng Guan *Department of Mechanical Engineering, Louisiana State University, Baton Rouge, LA* (CHAP. 11)

Johnny Chung Yin Ho *University of California at Berkeley, Berkeley, CA* (CHAP. 4)

Qiaojian Huang *University of Illinois at Chicago, Chicago, IL* (CHAP. 1)

Ali Javey *University of California at Berkeley, Berkeley, CA* (CHAP. 4)

Ajit Khosla *Engineering Science, Simon Fraser University, Burnaby, BC, Canada* (CHAP. 8)

Manuela La Rosa *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Carmen M. Lilley *Department of Mechanical and Industrial Engineering, University of Illinois at Chicago, Chicago, IL* (CHAP. 1)

Aihua Liu *Qingdao Institute of Bioenergy and Bioprocess Technology, Chinese Academy of Sciences, China* (CHAP. 6)

John D. W. Madden *Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada* (CHAP. 13)

Nunzia Malagnino *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Alessandro Marcellino *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Tissaphern Mirfakhrai *Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada* (CHAP. 13)

Kabir Mirpuri *Intel Corp., Chandler, AZ* (CHAP. 2)

James E. Morris *Department of Electrical & Computer Engineering, Portland State University, Portland, OR* (CHAP. 16)

Ali Kashefian Naieni *Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada* (CHAP. 12)

Donata Nicolosi *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Alireza Nojeh *Department of Electrical and Computer Engineering, University of British Columbia, Vancouver, BC, Canada* (CHAP. 12)

Luigi Occhipinti *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Fabrizio Porro *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Giovanni Sicurella *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

David W. Steuerman *University of Victoria, Victoria, BC, Canada* (CHAP. 7)

Jerzy Szpunar *Department of Mining and Materials Engineering, Montreal, QC, Canada* (CHAP. 2)

John D. Tovar *Johns Hopkins University, Baltimore, MD* (CHAP. 10)

Jonathan Tucker *Keithley Instruments, Inc., Cleveland, OH* (CHAP. 14)

Elena Umana *Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi, Università degli Studi di Catania, Italy* (CHAP. 5)

Raffaele Vecchione *Technology R&D, ST Microelectronics, Italy* (CHAP. 5)

Steven H. Voldman *IEEE Fellow, Vermont* (CHAP. 15)

Brian D. Wall *Johns Hopkins University, Baltimore, MD* (CHAP. 10)

Erich C. Walter *3M Display and Graphics Business Laboratory, 3M Center, St. Paul, MN* (CHAP. 7)

Ying Wang *Department of Mechanical Engineering, Louisiana State University, Baton Rouge, LA* (CHAP. 11)

Horst Wendrock *IFW-Dresden, Dresden, Germany* (CHAP. 2)

This page intentionally left blank

Preface

Nanoelectronics is an emerging, enabling, and multidisciplinary field with a wide range of potential applications. Although no single definition of nanoelectronics exists, it is commonly understood as an ability to control matter on a nanometer scale for the construction of new materials with novel properties (physical, chemical, and biological) and functions (e.g., quantum effects). In recent years, new nanomaterials and device structures have attracted an enormous amount of attention because of their fascinating properties and potential as building blocks for electronics, optoelectronics, and sensor applications.

Over the years, there have been many proposals for new electronic switching elements that could replace traditional CMOS transistors. They include various quantum devices (such as single-electron transistors and quantum dots), some of which are described in this book. Although this replacement improves the intrinsic device speed, it does not solve a key problem with the wires that connect devices. In most integrated circuits, a significant consideration is the ability of the devices to drive the wires. For this reason, we have devoted Part I of the book to the topic of nanowires.

Chapter 1 provides a general introduction to electrical properties, and Chapter 2 deals with copper interconnect lines and related electromigration problems. Futuristic interconnects based on carbon nanotubes are described in Chapter 3. Finally, Chapter 4 presents innovative ways of producing nanowire integrated circuitry.

A second important thrust in nanoelectronics is related to molecules. Scientists are beginning to understand cell engineering, and various molecular devices have been proposed. One should keep in mind that classical computing with these devices is not efficient; they are simply too slow and unreliable. However, they can be very good for creating materials and sensing signals from the environment, and they can possibly modify living tissue so that it acts

differently. For these reasons, Part II of the book is devoted to molecular electronics.

Chapter 5 introduces the exciting technology of printed organic electronics. Chapter 6 describes nanostructure-enabled chemical sensing, whereas Chapter 7 deals with the analysis of complex organic structures. Chapter 8 describes applications of nanoparticle-doped polymers, and Chapter 9 characterizes single-electron organic devices. Part II of the book closes with a chapter on developments toward the synthesis of supermolecular bioelectronic nanostructures.

Finally, Part III of the book deals with various phenomena related to nanodevices. Chapter 11 provides an introduction to nanostructured electrode materials for advanced battery concepts. Chapters 12 and 13 are devoted to various aspects of carbon nanotubes. Measurements at the nanoscale are treated in Chapter 14 and ESD protection for nanodevices in Chapter 15. The book closes with the topic of nanopackaging, a frequently omitted but critical topic in making nanodevices a reality.

I hope the reader enjoys reading this book as much as I enjoyed putting it together. Nanoelectronics is full of exciting potential, and I am sure we have seen only a small part of what it can accomplish.

Krzysztof (Kris) Iniewski
Vancouver, BC

Nanoelectronics

This page intentionally left blank

PART

Nanowires

This page intentionally left blank

CHAPTER 1

Electrical Properties of Metallic Nanowires for Nanoelectronic Applications

Carmen M. Lilley and Qiaojian Huang

Many researchers have focused on metallic nanowire (NW) materials, such as Cu, Ag, and Au nanowires, as basic material building blocks for nanoelectronics. This chapter was written with the intention of providing an overview of electrical properties of metallic nanowire materials useful to researchers and engineers. Researchers may find the information useful in designing nanoscale electrical systems before they fabricate devices. The chapter is divided so that we begin with an overview of basic electrical properties, such as electrical resistivity and thermal coefficients of resistivity. In addition, we discuss parameters that influence the electrical properties at the nanoscale, such as size and surface effects. Finally, this chapter concludes with a discussion on the failure properties of metallic nanowires, such as failure from Joule heating and electromigration, so that the reliability of material system components can be considered in the design of nanoscale electrical systems.

1.1 Introduction

Nanowires have a wide range of applications in electronic systems, for example as interconnect wires in field-effect transistors,[1] resonators,[2–5] nanomagnets,[6–8] and spintronic systems.[9,10] Nanowires are also critical components used in the design of nanoelectromechanical systems (NEMSs), where they have applications as interconnects in circuits and sensors to detect chemical or biological agents.

A considerable challenge is the successful integration of these types of nanotechnology into larger scale systems with multiple platforms of integration, so that the nanosystems can interact with the macroscale world. Microscale electrical systems are a logical choice as the first platform for integration of nanosystems, because they are the closest to the nanosystem length scale among current manufactured electronic products. This makes microsystems the best candidate as a platform for integration and a link for controlled interaction with the macroscale world. The successful integration of nanosystems into microscale electronics depends on stable material properties that are reliable for at least a 10-year life cycle (with greater than a trillion cycles of operation).[11] However, most nanoscale systems fabricated to date are prone to material instabilities (for example, oxidation of surfaces or agglomeration of quantum dots or carbon nanofibers) that negatively affect their usefulness.

There has been much research in the area of modeling and characterization of surface properties and crystalline structure of metallic nanowires and how these properties influence their electrical properties. Within the nanoscale domain, for instance, there has been considerable research on the size dependence of electrical resistivity. For example, as a nanowire's critical dimension decreases from hundreds to tens of nanometers, their electrical resistivity will increase because of size and surface effects. As the critical dimensions decrease further, to dimensions smaller than 1 nm, their electron transport properties will exhibit a unique shift to quantized behavior that can only be modeled by quantum mechanics. To date, however, there is limited research on the long-term stability of these properties. It should be noted that the surface and structural properties of nanomaterials may lead to unexpected material failures, which are a significant obstacle to the reliability of these material systems.

Some of the most common metallic nanowire materials used by researchers are face-centered cubic (FCC) metals such as copper (Cu), silver (Ag), and gold (Au) synthesized by bottom-up and top-down approaches. For a monolithic nanowire, the electrical and failure properties of the nanowire will vary with size and surface properties. Therefore, this chapter gives an overview of electrical properties of Cu, Ag, and Au nanowire materials with critical dimensions of a 10- to 100-nm size scale. The influence of size and surface on the material properties is also discussed. The aim of this chapter is to provide the reader with practical information on material property considerations of metallic nanowires when planning to design a nanoelectronic system. In addition, by providing information on failure properties, scientists and engineers will be able to incorporate reliability of material components into their design processes. It is expected that scientists and engineers will find this information

useful for the practical design and fabrication of nanoelectronic systems.

1.1.1 Size and Surface Effects on Electrical Properties of Nanowires

Figure 1.1 illustrates the percentage of surface atoms with respect to bulk atoms for an FCC close-packed nanoparticle of Cu with diameters ranging from 0.25 to 50.9 nm.[12] As can be seen, the ratio of surface atoms to bulk atoms becomes increasingly large as the particles become smaller. There has been much focus on how surface influences the material properties of nanoscale structures, where some of these surface effects may lead to changes in the electrical[13,14] or mechanical[15–18] properties of NWs. For example, apparent variations in measured elastic modulus for NWs have been attributed to a combination of effects from surface stress and surface elasticity; see for example Refs. 15, 16, and 18. In addition, size has been found to influence the electrical resistivity of nanowires. For example, it is now well known that nanowires with dimensions below 10 nm can exhibit quantized resistivity behavior; and this behavior has been studied extensively using molecular dynamic simulation methods. For nanowire sizes larger than 10 nm, electron surface scattering and electron grain boundary scattering have been shown to cause a nonlinear change in the electrical resistivity. For these larger nanowire diameters, the well-established kinetic theory (commonly referred to as the Fuchs-Sondheimer theory) has been used to model the effects from electron surface scattering, and Mayadas-Schatzkes theory has been used to model the effects from electron grain boundary scattering.

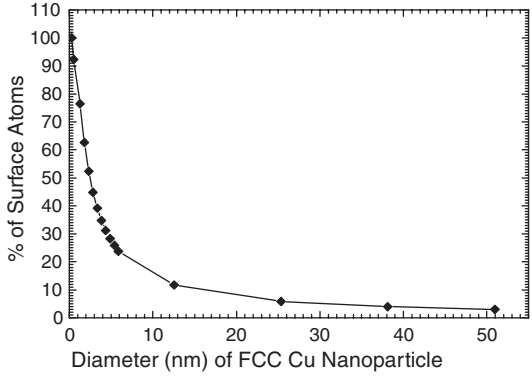


Figure 1.1 Graph of the percentage of surface atoms with respect to bulk atoms for FCC close-packed Cu nanoparticles.

In Section 1.2, we present a review of these theoretical models for size and surface effects on the electrical resistivity of a nanowire.

1.1.2 Stability of Nanomaterial Properties—Surface Matters

Adsorption of surface contaminants is another type of surface effect that may cause changes in material properties at the nanoscale. For example, variations in tensile strength of Au NWs were attributed to the presence of carbon (C), oxygen (O), and nitrogen (N).[17] Similarly, exposure to air or other sources of contaminants may affect the measured resistance and long-term reliability of metal NWs.[14,19] For example, researchers have found that the aging mechanisms for permalloys, such as those of nickel (Ni) and iron (Fe), were a result of oxidation and diffusion of this oxygen into the bulk NW material. This oxidation and the subsequent diffusion of oxygen cause the electrical resistivity of the nanowire to increase. Consequently, it was found that capping the nanowire surface, such as with a thin surface film of gold (15 nm), prevented surface oxidation and thus also the increase in electrical resistance.[19] However, Au has very high mobility and can readily contaminate silicon-on-insulator (SOI) devices at the wafer level.[20] Therefore, it is unlikely that Au would be used to fabricate nanoscale electronics that would be integrated into microelectronics in a commercial fabrication setting. As previously mentioned, there is limited published research on the stability of nanoscale material properties. However, researchers should take note: surface contaminants may affect their design of nanoscale electronic systems, and they may find it useful to identify the surface composition of the nanomaterials as a way to identify whether surface contaminants have any significant impact on their designs.

As discussed previously, the relative ratio of surface atoms to bulk (or volume) atoms in nanoscale systems increases dramatically as the nanostructures decrease in size. This may also influence material diffusion at the surface, because there are more atoms positioned at the surface, and these surface atoms may be detached more easily from their equilibrium positions. This would result in materials having surface diffusion at lower temperatures as compared to bulk temperatures.[21] This lower diffusion temperature (or enhanced diffusivity) has an important impact on the stability of a nanowire. For example, Karabacak et al. recently published a premelting temperature of 673 to 773 K for copper nanorod arrays with a diameter of approximately 100 nm.[21] This premelting temperature range is lower than the bulk melting temperature and is believed to be a result of the nanowire size. Other researchers have also found that although the current-to-failure density increases as wires become smaller, the mean temperature to failure may actually decrease as compared to the bulk

melting temperatures.[21,22] A decrease in the temperature for material diffusivity therefore may affect the material lifetime where they may fail from such effects as electromigration.

1.2 Electrical Resistivity of Metallic Nanowires

1.2.1 Electron Surface Scattering

As previously mentioned, size effects on electrical resistivity for metallic nanowires have been modeled by various researchers using two well-established theories, Fuchs-Sondheimer for electron surface scattering, and Mayadas-Schatzkes for grain boundary scattering. This section provides a brief overview of these theories, and their application to experimental results is discussed in the following section. Fuchs-Sondheimer theory is also called kinetic theory and is a well-established theory to model nonlinear changes in electrical resistivity for thin films.[23,24] Chambers applied this theory to model the electrical resistance of wires.[25] Herein, we will present the analysis for a trapezoidal nanowire system using Chambers's approach, because this more general geometry can be applied to model square, rectangular, trapezoidal, and triangular nanowires (all of which can result from various nanofabrication methods). The variable p is used to characterize the probability of elastic electron reflection at the surface where $p = 1$ for a total elastic reflection and $p = 0$ for a purely diffuse scattering and is called the electron surface scattering coefficient. For purely specular scattering ($p = 0$), the theoretical resistivity can be expressed as

$$\frac{\rho_o}{\rho_{FS}}(p=0,\lambda) = \frac{3}{4\pi s}\int_s ds \int_0^{2\pi} d\phi \int_0^{\pi} d\theta \sin\theta \cos^2\theta \left[1 - \exp\left(\frac{-L_{OP}}{\lambda}\right)\right] \tag{1.1}$$

where ρ_o is the bulk resistivity of the material, λ is the electron mean free path of the material, s is the cross-sectional surface area of the wire, point O is on the surface of a cross-sectional area of the wire, and P is a point located on the wire surface. The vector **OP** connects point O to point P and has the length L_{OP}. The vector **OP′** is the projection of the vector **OP** onto surface s. The angle ϕ is the radial angle for **OP′**, and θ is the azimuthal angle of vector **OP**. Equation (1.1) is integrated over all points on the surface s. In essence, the mean free path for electrons is reduced due to electron surface scattering on the wire surface which causes an increase in resistivity for the wire as compared to the bulk material.

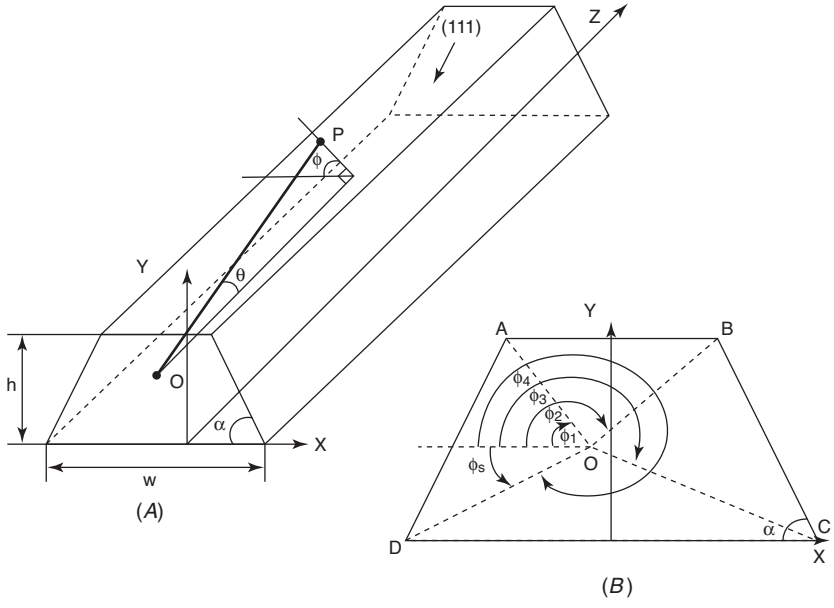


FIGURE 1.2 Illustration of a wire with a trapezoidal cross-section.

The equation for the electrical resistivity of a trapezoidal wire is given in Eq. (1.2). To derive this equation from Eq. (1.1), we first consider a point O in the cross section and electrons passing through it in the direction of **OP**, where P is on the top wire surface, as shown in Fig. 1.2. The integration of Eq. (1.1) is over all locations throughout the wire cross section s, with L_{OP} being the distance from the location of point O in the cross section to the point P on the wire surface in the direction of the azimuthal angle θ and the radial angle ϕ. From this calculation, the resultant electron mean free path in the wire is reduced to $\lambda[1 - \exp(\frac{-L_{OP}}{\lambda})]$ because of electron scattering on the wire surface.[25] In Fig. 1.2, the dimensions $2a$, $2b$, and h are the top width, bottom width, and height for the trapezoidal wire, respectively. The bottom angle of the trapezoid wire is given by

$$\alpha = \arctan\left(\frac{h}{b-a}\right) \tag{1.2}$$

The cross-section area of the trapezoid wire is written as

$$s = \frac{(2a+2b)h}{2} = (a+b)h \tag{1.3}$$

By examining the in-plane cross section of trapezoid ABCD (the surface s) and the projection of **OP (OP')** from the electron traveling path,

the path length L_{OP} for an electron scattering at point P on the wire top surface (P′ on the segment AB) can be written as

$$L_{OP\_AB} = \frac{L_{OP'}}{\sin\theta} = \frac{h-y}{\sin\theta\sin\phi} \tag{1.4a}$$

Similarly, the path length for an electron scattering at point P on the wire for P′ on segment BC can be written as

$$L_{OP\_BC} = \frac{L_{OP'}}{\sin\theta} = \frac{(b+x-y/\tan\alpha)\sin\alpha}{\sin\theta\sin(\phi-\alpha)} \tag{1.4b}$$

The path length for an electron scattering at point P on the wire for P′ on segment CD can be written as

$$L_{OP\_CD} = \frac{L_{OP'}}{\sin\theta} = \frac{-y}{\sin\theta\sin\phi} \tag{1.4c}$$

Finally, the path length for an electron scattering at point P on the wire for P′ on segment DA can be written as

$$L_{OP\_DA} = \frac{L_{OP'}}{\sin\theta} = \frac{(b-x-y/\tan\alpha)\sin\alpha}{\sin\theta\sin(\phi+\alpha)} \tag{1.4d}$$

As shown in the same figure, the integral limits for the radial angles ϕ are determined from the geometry as

$$\phi_1 = \begin{cases} \arctan\left(\dfrac{h-y}{a-x}\right) & (\text{for } x < a) \\ \dfrac{\pi}{2} + \arctan\left(\dfrac{x-a}{h-y}\right) & (\text{for } a \le x < b) \end{cases} \tag{1.5a}$$

$$\phi_2 = \frac{\pi}{2} + \arctan\left(\frac{a+x}{h-y}\right) \tag{1.5b}$$

$$\phi_3 = \frac{3\pi}{2} - \arctan\left(\frac{b+x}{y}\right) \tag{1.5c}$$

$$\phi_4 = \frac{3\pi}{2} + \arctan\left(\frac{b-x}{y}\right) \tag{1.5d}$$

$$\phi_5 = -\frac{\pi}{2} + \arctan\left(\frac{b-x}{y}\right) \tag{1.5e}$$

The limits of integration for radial angle ϕ are $[\phi_1, \phi_2]$, $[\phi_2, \phi_3]$, $[\phi_3, \phi_4]$, and $[\phi_5, \phi_1]$ for the traveling paths of LOP_AB, LOP_BC, LOP_CD, and LOP_DA, respectively. Substituting Eq. (1.5) into Eq. (1.1), the solution of a trapezoid wire resistivity is

$$\frac{\rho_0}{\rho_{FS}}(p=0,\lambda) = \frac{3}{2\pi(a+b)h}\int_0^a dx\int_0^h dy\int_{\arctan(\frac{h-y}{a-x})}^{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(h-y)}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_0^a dx\int_0^h dy\int_{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})}^{\frac{3\pi}{2}-\arctan(\frac{b+x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(b+x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi-\alpha)}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_0^a dx\int_0^h dy\int_{\frac{3\pi}{2}-\arctan(\frac{b+x}{y})}^{\frac{3\pi}{2}+\arctan(\frac{b-x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{y}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_0^a dx\int_0^h dy\int_{-\frac{\pi}{2}+\arctan(\frac{b-x}{y})}^{\arctan(\frac{h-y}{a-x})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(b-x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi+\alpha)}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_a^b dx\int_0^{(b-x)\tan\alpha} dy\int_{\frac{\pi}{2}+\arctan(\frac{x-a}{h-y})}^{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(h-y)}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_a^b dx\int_0^{(b-x)\tan\alpha} dy\int_{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})}^{\frac{3\pi}{2}-\arctan(\frac{b+x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(b+x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi-\alpha)}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_a^b dx\int_0^{(b-x)\tan\alpha} dy\int_{\frac{3\pi}{2}-\arctan(\frac{b+x}{y})}^{\frac{3\pi}{2}+\arctan(\frac{b-x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{y}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{2\pi(a+b)h}\int_a^b dx\int_0^{(b-x)\tan\alpha} dy\int_{-\frac{\pi}{2}+\arctan(\frac{b-x}{y})}^{\frac{\pi}{2}+\arctan(\frac{x-a}{h-y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(b-x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi+\alpha)}\right]\right\} \tag{1.6}$$

The last four terms of Eq. (1.6) drop away when $a = b$ for the case of wires with a rectangular cross section (where $\alpha = 90^\circ$). In this case, the first four terms in Eq. (1.6) can be simplified to

$$\frac{\rho_0}{\rho_{FS}}(p=0,\lambda) = \frac{3}{4\pi ah}\int_0^a dx\int_0^h dy\int_{\arctan(\frac{h-y}{a-x})}^{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(h-y)}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{4\pi ah}\int_0^a dx\int_0^h dy\int_{\frac{\pi}{2}+\arctan(\frac{a+x}{h-y})}^{\frac{3\pi}{2}-\arctan(\frac{a+x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{(a+x)}{\lambda\sin\theta\cos\phi}\right]\right\}$$

$$+\frac{3}{4\pi ah}\int_0^a dx\int_0^h dy\int_{\frac{3\pi}{2}-\arctan(\frac{a+x}{y})}^{\frac{3\pi}{2}+\arctan(\frac{a-x}{y})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{y}{\lambda\sin\theta\sin\phi}\right]\right\}$$

$$+\frac{3}{4\pi ah}\int_0^a dx\int_0^h dy\int_{-\frac{\pi}{2}+\arctan(\frac{a-x}{y})}^{\arctan(\frac{h-y}{a-x})} d\phi$$

$$\int_0^\pi d\theta\sin\theta\cos^2\theta\left\{1-\exp\left[\frac{-(a-x)}{\lambda\sin\theta\cos\phi}\right]\right\} \tag{1.7}$$

Because of symmetry of the cross section, the equation for resistivity of a rectangular nanowire with electron surface scattering effects is[26,27]

$$\frac{\rho_0}{\rho_{FS}}(p=0,\lambda) = \frac{6}{4\pi wh}\int_0^w dx \int_0^h dy \int_{-\arctan(x/y)}^{\arctan[(w-x)/y]} d\phi \int_0^{\pi} d\theta \sin\theta\cos^2\theta \left[1-\exp\left(\frac{-y}{\lambda\cos\phi\sin\theta}\right)\right] + \frac{6}{4\pi wh}\int_0^w dx \int_0^h dy \int_{-\arctan[y/(w-x)]}^{\arctan[(h-y)/(w-x)]} d\phi \int_0^{\pi} d\theta \sin\theta\cos^2\theta \left[1-\exp\left(\frac{-(w-x)}{\lambda\cos\phi\sin\theta}\right)\right] \tag{1.8}$$

The theoretical equation for a square nanowire can be obtained by letting $w = h$ in the integral equation. For the case of triangular cross-sectional wires, the first four terms in Eq. (1.6) cancel because $a = 0$. The fifth integral term in Eq. (1.6) is also equal to zero because the integral limits for ϕ are same. Therefore, the solution of the electrical resistivity for a triangular cross-section wire is

$$\frac{\rho_0}{\rho_{FS}}(p=0,\lambda) = \frac{3}{2\pi bh}\int_0^b dx \int_0^{(b-x)\tan\alpha} dy \int_{\frac{\pi}{2}+\arctan\left(\frac{a+x}{h-y}\right)}^{\frac{3\pi}{2}-\arctan\left(\frac{b+x}{y}\right)} d\phi \int_0^{\pi} d\theta \sin\theta\cos^2\theta \left\{1-\exp\left[\frac{-(b+x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi-\alpha)}\right]\right\} + \frac{3}{2\pi bh}\int_0^b dx \int_0^{(b-x)\tan\alpha} dy \int_{\frac{3\pi}{2}-\arctan\left(\frac{b+x}{y}\right)}^{\frac{3\pi}{2}+\arctan\left(\frac{b-x}{y}\right)} d\phi \int_0^{\pi} d\theta \sin\theta\cos^2\theta \left\{1-\exp\left[\frac{y}{\lambda\sin\theta\sin\phi}\right]\right\} + \frac{3}{2\pi bh}\int_0^b dx \int_0^{(b-x)\tan\alpha} dy \int_{-\frac{\pi}{2}+\arctan\left(\frac{b-x}{y}\right)}^{\frac{\pi}{2}+\arctan\left(\frac{x-a}{h-y}\right)} d\phi \int_0^{\pi} d\theta \sin\theta\cos^2\theta \left\{1-\exp\left[\frac{-(b-x-y/\tan\alpha)\sin\alpha}{\lambda\sin\theta\sin(\phi+\alpha)}\right]\right\} \tag{1.9}$$

Finally, for a circular cross-section, the equation for resistivity with electron surface scattering effects is[25]

$$\frac{\rho_0}{\rho_{FS}}(p=0,\lambda)=\left(1-\frac{3}{2\pi a^2}\right)\int_0^a r\,dr\int_0^{2\pi} d\phi \int_0^{\pi} d\theta\,\sin\theta\cos^2\theta\exp\left[\frac{-(a-r)}{l\sin\theta}\right] \tag{1.10}$$

All of the foregoing equations are purely diffuse electron surface scattering. For the case of partially diffusive scattering ($p \neq 0$), the exact solution for the resistivity requires summing over all possible multiple scattering paths. The resistivity is determined with the following series of expansions:[25–28]

$$\frac{\rho_0}{\rho_{FS}}(p,\lambda)=(1-p^2)\sum_{k=1}^{\infty}\left[kp^{k-1}\cdot\frac{\rho_0}{\rho}\left(p=0,\frac{\lambda}{k}\right)\right] \tag{1.11}$$

Note that the series solution is obtained when the specularly scattered electrons travel equal distances between successive scattering events.[25] For trapezoidal wires, the requirement of equal path lengths between successive specular scattering events is not completely satisfied. Therefore, Eq. (1.11) is an approximate solution to model the resistivity for trapezoidal and rectangular wires when it is a partially diffuse scattering. For rectangular wires, the equation for resistivity with surface scattering effects for $p \neq 0$ can be approximated using Sondheimer's approach[24]:

$$\rho_{FS}=\rho_0\left[1+\frac{3}{8}\lambda_0(1-p)\left(\frac{1}{t}+\frac{1}{w}\right)\right] \tag{1.12}$$

where t and w are the thickness and the width of a nanowire, respectively. The error for Eq. (1.12) is estimated to be approximately 5 percent or less for larger nanowires (dimensions larger than 200 nm) as compared to the exact solution calculated with Eq. (1.6).[28,29]

1.2.2 Grain Boundary Scattering

Mayadas-Shatzkes (MS) developed a model resistivity in grain boundary scattering of conduction electrons.[30] The probability for the electrons to be reflected at the grain boundary is denoted by the reflection coefficient R. Because the reflected electrons reduce the electrical current, grain boundary scattering results in a higher resistivity. The effect

of grain boundary scattering on the resistivity has the form

$$\rho_{MS} = \frac{\rho_0}{1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)} \tag{1.13}$$

where $\alpha = \frac{\lambda_o}{d}\frac{R}{1-R}$ and d is the mean grain size.

At the nanoscale, both surface and grain boundary scattering contribute to the electrical resistivity of interconnects. Following Matthiessen's rule, the combined model for the size dependent resistivity of a rectangular wire can be approximated with[28]

$$\rho = \rho_0 \left[\frac{3}{8}\lambda_0 (1-p)\left(\frac{1}{t} + \frac{1}{w}\right) + \frac{1}{1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)} \right] \tag{1.14}$$

These equations represent a summary of the theoretical models commonly used to study the size effects on the electrical resistivity of metallic nanowires. In the following section, we present a summary of electrical resistivity properties, including measured p and R values, for commonly used materials for nanowire interconnects, namely, Cu, Ag, and Au.

1.2.3 Electrical Resistivity of Cu, Ag, and Au Metallic Nanowires

Figures 1.3 and 1.4 illustrate the change in electrical resistivity for square Cu, Ag, and Au nanowires with dimensions ranging from 10 nm to 250 nm. These graphs were calculated by calculating Eq. (1.6) (the exact solution using Chamber's method) and Eq. (1.12) (the approximate solution using Sondheimer's method). The material parameters for the metals are (i) Cu: $\lambda_o = 40$ nm,[28] $\rho_o = 1.712$ $\mu\Omega$-cm[31]; (ii) Ag: $\lambda_o = 51$ nm,[32] $\rho_o = 1.629$ $\mu\Omega$-cm[31]; and (iii) Au: $\lambda_o = 38$ nm,[33] $\rho_o = 2.255$ $\mu\Omega$-cm.[31] As can be seen in these graphs, the overall electrical resistivity increases as the nanowire dimensions decrease, and the overall electrical resistivity decreases as p increases. The numerical results indicate that the approximate solution has an error of 3 percent. As can also be seen, Cu has the lowest resistivity for the three materials. Although Ag had the lowest bulk resistivity, because of its electron mean free path, it has a larger theoretical resistivity than Cu. The Au nanowires have the greatest theoretical resistivity among the three metals.

Many researchers have measured the overall electrical resistivity of nanowires from which they have obtained electron surface

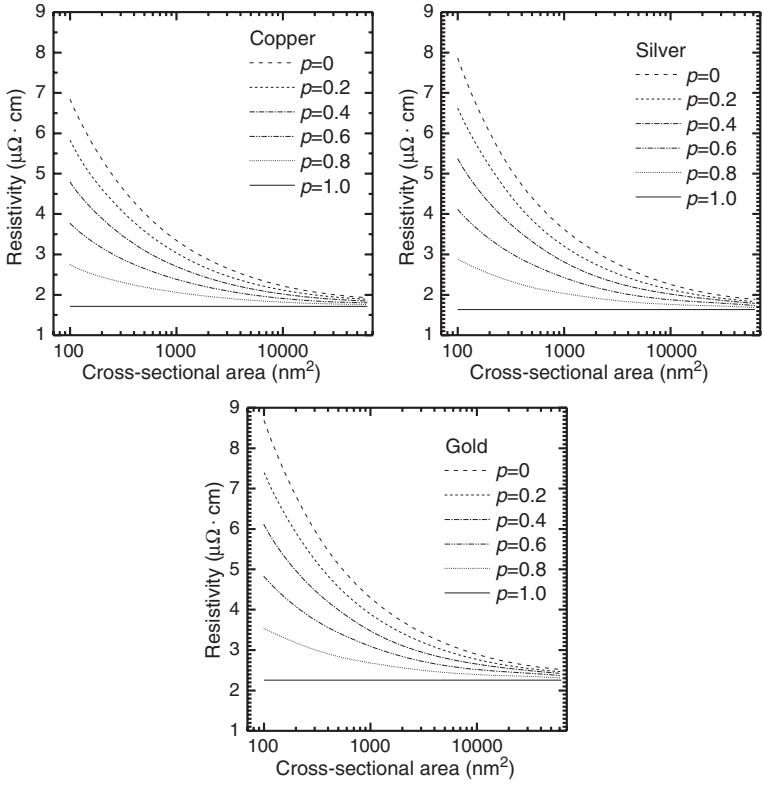


Figure 1.3 Wire resistivity as a function of the cross-sectional area for copper, silver, and gold square nanowires: calculated with approximate solution.

scattering and grain boundary reflectivity coefficients. For example, Fig. 1.5 shows the electrical resistivity measurements for rectangular Cu nanowires.[22] These wires were fabricated with e-beam lithography and metal evaporation. Three curves are shown, one for electron surface scattering (–), grain boundary scattering (. . .), and the combined resistivity) (—). The measured resistivity increases as the nanowires decrease in width. For these systems, the obtained p and R values were 0.50 and 0.34, respectively.

A summary of published literature values for the electrical resistivity properties is presented in Table 1.1. The summary includes results for experimentally measured electrical resistivity (ρ), electron surface scattering coefficients (p), and grain boundary reflectivity values (R) of Cu, Ag, and Au nanowires synthesized by various methods and with varying dimensions. As can be seen, the experimentally measured values for p and R vary significantly for nanowires. Because

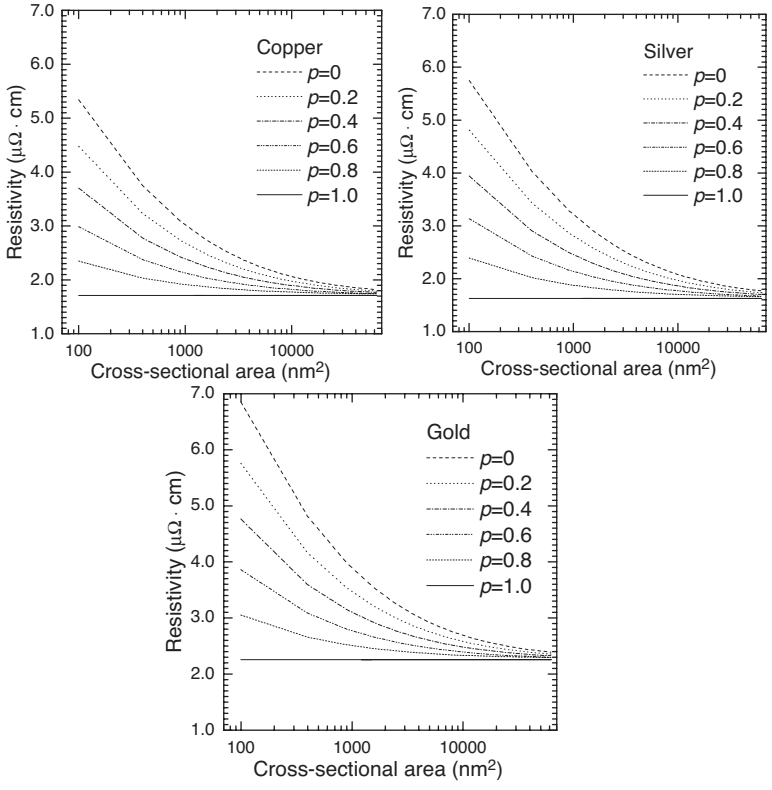


Figure 1.4 Wire resistivity as a function of the cross-sectional area for copper, silver, and gold square nanowires calculated with the FS model. The material parameters for the calculations are (i) Cu: $\lambda_o = 40$ nm, $\rho_o = 1.712\,\mu\Omega$-cm; (ii) Ag: $\lambda_o = 51$ nm, $\rho_o = 1.629\,\mu\Omega$-cm; and (iii) Au: $\lambda_o = 38$ nm, $\rho_o = 2.255\,\mu\Omega$-cm.

there is wide variability in fabrication methods and dimensions of the nanowires, the variation in results suggest that it would be prudent for researchers to measure the resistivity of a sample set of nanowires as part of the standard process monitoring when fabricating nanoelectronics.

1.3 Failure Properties of Metallic Nanowires

1.3.1 Failure of Nanowires from Joule Heating

Published research on the width dependence of the temperature coefficient of resistance (α_R) for metallic nanowires is not widely available.

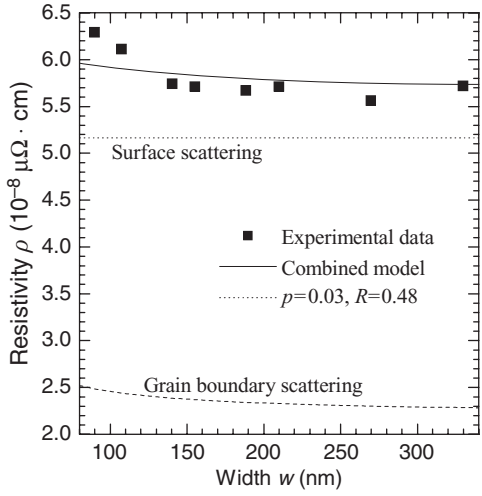


Figure 1.5 The measured resistivity of Cu nanowires versus the wire width at room temperature (closed squares) compared with the combined model (solid curve), FS model (dashed curve), and MS model (dotted curve). (Note: $l = 2.04\,\mu$m and $t = 50$ nm.)

This material parameter is important because nanoscale interconnects experience current densities much larger than microscale interconnects. As a result, the subsequent Joule heating can cause a significant increase in the nanowire resistance, which results in a positive feedback where an increase in resistance leads to an increase in heating. The result is that material diffusion can occur from the Joule heating. This material diffusion would cause local discontinuities in the uniformity of the nanowire geometries. These geometric discontinuities can cause localized hot spots in the nanowire, which may also further accelerate material diffusion. Therefore, an accurate determination of α_R is important to model the temperature profile in a nanowire in order to design nanoelectronic systems.

A summary of experimentally measured values for α_R is given in Table 1.2. As can be seen, the general trend for Cu and Au nanowires is that α_R decreases as the nanowire dimensions decrease. This is not true in the case of Ag. However, we were not able to find additional published results for Ag to make any observation on size effects as the nanowires decrease in size. The reason for the apparently reduced α_R in Cu (or Au) nanowires is not well understood. Two possible explanations have been previously proposed: heating from the SEM electron beam during measurements of thermal properties, and a strain effect due to the mismatch in the coefficients of thermal expansion α_{TE}.[39] For example, the α_{TE} for Cu is 17×10^{-6} K^{-1} at 300 K (see Ref. 31) and for a SiN substrate underneath the Cu nanowire, the α_{TE} is 4.5×10^{-6} K^{-1}

	Resistivity ($\mu\Omega$-cm)	P^*	R^{**}	Dimensions	Synthesis Technique	Comments	Ref.
Cu	5.5–6.4	0.5	0.34	w = 90–330 nm, t = 50 nm	E-beam evaporation	4-point	22
	2.45–4.6	0.4–0.6	0.5	w = 40–800 nm, t = 230 nm	Electrochemical	$I = 10\ \mu$A	27, 34
	2.4–4.7	0.0	—	w = 43–810 nm, t = 230 nm	—	Autoprober	34
	2.3–3.2	—	0.57–0.62	w = 95–305 nm, t = 130 nm	Electroplating	4-point	35
	1.9–3.1	0.0	0.12–0.21	w = 80–2,000 nm, t = 250 nm	Electrochemical	$I < 500\ \mu$A	29
Ag	1.95–3.67	0	0.3	w = 50–1,000 nm, t = 300 nm	Electroplating	4-point	26
	2.00–4.11	0.5	—	d = 15–200 nm	Electrochemical	$I < 100\ \mu$A	36
Au	6.8–11.0	0.5	0.9	w = 20–60 nm, t = 40 nm	Evaporation	4-point	37
	3.7–5.4	0–0.5	0.45	d = 80–300 nm	Electrochemical	2-point	38

p^*: Electron surface reflection coefficient
R^{**}: Electron grain boundary reflection coefficient

Table 1.1 Electrical Resistivity of Cu, Ag, and Au Nanowires Measured at Room Temperature

	TCR ($\times 10^{-3}K^{-1}$)	Geometries or Dimensions	Synthesis Technique	Experimental Method	Reference
Cu	3.9, 4.1, 4.3	Bulk	—	—	31, 34, 42
	3.82	Film of 330-nm thickness on SiN/Si substrate	Sputtered	Four-point probe direct current technique	45, 46
	3.55	Film of 330-nm thickness on SiN/Si substrate	E-beam evaporation		
	3.6	Nanowires, $l = 200\,\mu$m, $t = 230$ nm, and $w = 310$–810 nm	Standard electrochemical deposition	Measured using an autoprober	34, 47
	3.2	Nanowires, $l = 200\,\mu$m, $t = 230$ nm, and $w = 110$ nm			
	2.9	Nanowires, $l = 200\,\mu$m, $t = 230$ nm, and $w = 88$ nm			
	2.5	Nanowires, $l = 200\,\mu$m, $t = 230$ nm, and $w = 44$ nm			
	1.34–1.54	Nanowires, $l = 2.04\,\mu$m, $t = 50$ nm, $w = 90$–330 nm	E-beam evaporation	Four-point probe measurement in UHV condition	22
Ag	3.8	Bulk	—	—	42
	4.3	Nanowires with diameters of 15, 30, 100, and 200 nm	Electrochemical deposition	Two-point measurement using a lock-in amplifier	36
Au	3.4, 3.9	Bulk	—	—	31, 42
	3.0–3.4	Film of $t = 10$–20 nm	Thermal evaporation	DC electrical sheet resistance measurement by four-probe van der Pauw method	48
	2.0	Wires of $l = 10\,\mu$m, $w = 1\,\mu$m, and $t = 36$ nm	Thermal evaporation	Four-point measurement	49
	1.10–1.34	Nanowires, $l = 2.1\,\mu$m, $t = 50$ nm, $w = 64$, 95, and 145 nm	E-beam evaporation	Four-point probe measurement in UHV condition	50

Table 1.2 Temperature Coefficient of Resistance for Cu, Ag, and Au

at 300 K.[40] In our own research, we have measured the temperature-dependent resistivity of Cu nanowires for various wire widths in order to calculate the corresponding temperature coefficient of resistance, α_R.[22] We found that heating from the electron beam for Cu nanowires was negligible because the change in temperature as a result of the electron beam was much smaller than the mean temperature of the wire. When the thermal strain was studied, it was found that the strain in a nanowire due to a thermal mismatch at the nanowire and substrate interface is the same for all samples because the nanowires were tested at the same temperatures.[41] As a result, thermal strains are not believed to cause the width dependence of α_R. It should be noted that the strains on the edges of the nanowires may also partially relax, which results in an inhomogenous strain distribution in the nanowires. However, this effect would cause increasing α_R values for smaller wire widths,[42] which is opposite to the trend observed experimentally. Another cause for the reduced temperature coefficient of resistance for smaller wires may be surface diffuse scattering.[42,43] Because the ratio of surface area to volume increases as the wire width decreases, the influence of surface diffuse scattering becomes a significant effect and would decrease the value for α_R. However, these research findings are not conclusive, and further research is needed to fully understand how size and surface may influence α_R.

Similarly, researchers have also found that the mean temperature at current density to failure, calculated with α_R, is lower than the bulk melting temperature of the material. Conversely, the current density to failure increases as the cross-sectional area decreases for a nanowire. This increase in failure current density has been attributed to the large surface-to-volume ratio, which allows improved heat transfer from the nanowire to the local environment.[34,44] Other researchers have found that heat transfer from the nanowire to the substrate is the cause for this increase in failure current density as size decreases. However, the average temperatures of the Cu nanowires before failure have been found to be lower than the melting temperature (1356 K) for the bulk metal.[31] Researchers have hypothesized that there may be two causes for enhanced surface diffusion (i.e., lower failure temperatures). One may be a result of "hot spots" within the wire, that is, localized points of higher resistance than the surrounding materials due to impurities or defects. These hot spots locally have greater Joule heating and thus localized higher temperatures, which in turn increase the resistivity, thus forming a feedback for increased Joule heating that accelerates diffusion locally. A second cause for the enhanced surface diffusion may be due to surface effects. For example, Karabacak et al. recently published premelting temperature of 673 to 773 K for copper nanorod arrays with a diameter of approximately 100 nm. This premelting temperature range is lower than the bulk melting temperature and is

believed to be a result of the nanowire size. The smaller size of the nanowires allows a large percentage of the Cu atoms to be positioned at the surface of a nanowire, and these surface atoms are more responsive to diffusion. Therefore, the surface atoms may detach more readily from their equilibrium positions and start to diffuse at a lower temperature.[21]

In summary, the nature of a decrease in α_R as nanowire sizes decrease may be due to electron surface diffuse scattering. The size of a nanowire appears to influence the current density to failure by increasing the failure point as the size decreases. However, the mean temperature at failure appears to be lower than the bulk melting temperature and may be a result of surface effects. As with the resistivity of nanowire, there is a size dependence to α_R that needs further research. If this material property is important to a researcher, then it is recommended that α_R be characterized for more accurate identification of material properties. It should also be noted that α_R is necessary to measure the activation energy for electromigration failure in a wire. In the following section, we present a summary of activation energies for Cu, Ag, and Au nanowires and how these energies are used to predict a material lifetime.

1.3.2 Electromigration of Cu, Ag, and Au Nanowires

Electromigration is a major type of failure mechanism in electronic devices that affects the reliability assessment of very large-scale integrated (VLSI) microelectronic devices.[51] Electromigration is a material diffusion that results from momentum transfer from the moving electrons, called "electron wind," to atoms in a wire when an electrical current is present.[52] The material atoms will move in the direction of the electron flow once activation energy is achieved. As a result, metal ions will accumulate at individual grain boundaries forming hillocks and voids where atoms vacate a region at a greater rate than the arrival of atoms. Voids in the metallic nanowires will locally increase the current density, and therefore increase the local Joule heating and the electrical resistance. The higher temperature and current density will accelerate the atomic diffusion and eventually result in a rapid increase in resistance before failure. Furthermore, electromigration may also affect the reliability of electronic devices as the hillocks may short-connect adjacent wires.[53] Determining the activation energy for electromigration failure is a critical concern to modeling the stability of electrical resistivity for a nanowire.

The failure criterion to determine mean time to failure $\bar{t}_f$, which is also used to determine the activation energy for electromigration, is typically defined as a 10 percent[54] or 20 percent[55] relative increase in resistance. Black developed an empirical model to estimate the mean

	Activation Energy (eV)	Diffusion Pathways	Geometry or Dimensions	Synthesis Technique	Experimental Conditions	Reference
Cu	2.1	Lattice	—	—	—	59
	1.2	Grain boundary				
	0.7	Surface				
	1.2	Grain boundary	Nanowires of $l = 500$ μm, $w = 100$ and 150 nm, and $t = 200$ nm	Electrochemical plating	$J = 1.5$–3.7×10^{10} A·m^{-2}, $T = 300$°C	60
	0.94, 1.06	Surface or grain boundary	Nanowires of $l = 2.04$ μm, $w = 90$ and 141 nm, and $t = 50$ nm	E-beam evaporation	Ultrahigh vacuum, $J = 8.5$–10.9×10^{11} A·m^{-2}, $T = 107$–161°C	61
	0.81	Surface	$w = 0.25$–1.0 μm	E-beam evaporation	Vacuum, $J = 2.5 \times 10^{10}$ A·m^{-2}, $T = 375$°C	62
	0.28	Surface	$l = 3{,}000$ μm, $t = 425$ nm, $w = 1$ μm	Chemical vapor deposition	$J = 2.7$–3.3×10^{11} A·m^{-2}, $T = 300$°C	63
Ag	0.95	Grain boundary	Film of $t = 170$ nm	Chemical vapor deposition	$J = 0.68 \times 10^{10}$ A·m^{-2}, $T = 225$°C	64
	0.3	Surface	Film of $t = 170$ nm	Chemical vapor deposition	$J = 0.68 \times 10^{10}$ A·m^{-2}, $T = 150$–215°C	64
Au	0.98	—	Film of $t = 170$ nm	Chemical vapor deposition	$J = 0.63 \times 10^{10}$ A·m^{-2}, $T = 260$–380°C	64
	0.8	Grain boundary	Film of $t = 52.5$ and 500 nm	E-beam evaporation	$J = 1.8$–2.5×10^{10} A·m^{-2}, $T = 120$–425°C	65, 66
	0.675	—	$l = 800$ μm, $t = 1.4$ μm, $w = 3$ μm	—	$J = 0.2$–6×10^{10} A·m^{-2}, $T = 160$–300°C	54
	0.59	Surface or interface	$l = 450$ μm, $t = 1$ μm, $w = 2$ μm	Electrochemical plating	Ambient, $J = 2.0 \times 10^{10}$ A·m^{-2}, $T = 341$–391°C	67
	0.5	Surface	Nanowires of $l = 2.1$ μm, $w = 95$ nm, and $t = 50$ nm	E-beam evaporation	Ultrahigh vacuum, $J = 1.16$–1.37×10^{12} A·m^{-2}, $T = 98$–222°C	50

TABLE 1.3 Activation Energies for Cu, Ag, and Au

time to failure $\bar{t}_f$ of a wire, where Black's law is expressed as[56]

$$\bar{t}_f = \frac{A}{J^n} \cdot \exp\left(\frac{E_a}{K_B \cdot T}\right) \tag{1.15}$$

Here, A is a constant based on the cross-sectional area of the wire, J is the current density, E_a is the activation energy, k_B is the Boltzmann constant, and T is the mean temperature of the wire in kelvins. The current exponent, n, can range in value from 1 to 3; however, it is typically set to $n = 2$.[57] Determining the activation energy for electromigration failure is critical for predicting the lifetime because $\bar{t}_f$ is dependent on the activation energy exponentially.

Three diffusion pathways—lattice, grain boundary, and surface/interface—are possible for a material during electromigration. The activation energies will vary depending on the diffusion pathways. Lattice diffusion is the slowest pathway and has the largest activation energy. Grain boundary diffusion has a lower E_a value, whereas surfaces are the most rapid diffusion pathways with the lowest activation energy. The activation energy for electromigration failure will depend on the dominant diffusion pathway, which depends on such factors as the material, wire dimensions, crystalline structure, and surface properties. As can be seen in Table 1.3, the activation energies vary greatly for all three metals. In general, the measured electromigration activation energies have been found to range between the grain boundary and surface diffusion activation energies. Because the fabrication process will influence the crystalline or grain structure of metallic nanowires, there is generally a wide range of reported activation energies for nanowires. For example, the reported values for E_a of Cu wires range from 0.5 eV to 2 eV.[58] Researchers may find that a conservative estimation to predict a nanowire's lifetime with electromigration may be approximated by using surface diffusion activation energies when they are using metallic nanowires. However, as mentioned previously, measured activation energies vary significantly and direct measurement of the activation energies may be necessary for designing successful nanoelectronics.

1.4 Summary

We have presented a comprehensive review of electrical properties of metal nanowires that scientist and engineers may find useful for their design needs of nanoelectronics. As can be seen, the properties of nanowires change significantly at the nanoscale as compared to the bulk properties. A significant difference is that their resistivity in general is larger than the bulk resistivity and increases as the sizes decrease. The temperature coefficient of resistance at the nanoscale

is in general lower than the bulk value and is an advantage to reduce Joule heating as the current densities in the nanowires ($>10^8$ A/m^2) are generally much larger than wires at the microscale (on the order of $10^6 A/m^2$). The lower melting temperatures for current density to failure imply that there may be enhanced surface diffusion at the nanoscale that may affect the long-term stability of the nanowires and, as a result, the reliability of the nanoscale design. Finally, a review of electromigration studies for metallic nanowires also indicates that surface diffusion may become a significant diffusion pathway for nanowires. In this case, researchers may find that a conservative estimate of the nanowire lifetime may be made using surface diffusion activation energies with Black's law.

References

1. J. Song, W. Dongmok, M. C. McAlpine, R. S. Friedman, W. Yue, and C. M. Lieber, "Scalable interconnection and integration of nanowire devices without registration," *Nano Letters,* vol. 4, pp. 915-919, 2004.
2. S. Perisanu, P. Vincent, A. Ayari, M. Choueib, S. T. Purcell, M. Bechelany, and D. Cornu, "High Q factor for mechanical resonances of batch-fabricated SiC nanowires," *Applied Physics Letters,* vol. 90, 43113, 2007.
3. Z. L. Wang, G. Rui Ping, P. Zheng Wei, and D. Zu Rong, "Nano-scale mechanics of nanotubes, nanowires, and nanobelts," *Advanced Engineering Materials,* vol. 3, pp. 657-661, 2001.
4. A. Shik, H. E. Ruda, and I. G. Currie, "Electromechanical and electro-optical properties of nanowires," *Journal of Applied Physics,* vol. 98, 94306, 2005.
5. A. Husain, J. Hone, H. W. C. Postma, X. M. H. Huang, T. Drake, M. Barbic, A. Scherer, and M. L. Roukes, "Nanowire-based very-high-frequency electromechanical resonator," *Applied Physics Letters,* vol. 83, pp. 1240-1242, 2003.
6. R. Moradian and A. Fathalian, "Ferromagnetic semiconductor single-wall carbon nanotubes," *Nanotechnology,* vol. 17, pp. 1835-1842, 2006.
7. X. Ma, Y. Cai, N. Lun, and S. Wen, "Ferromagnetic Metal Nanoclusters Encapsulated in Carbon Nanotubes," *Nanotube-based Devices*, vol. 772, pp. 87-92, 2003.
8. E. Borowiak-Palen, E. Mendoza, A. Bachmatiuk, M. H. Rummeli, T. Gemming, J. Nogues, V. Skumryev, R. J. Kalenczuk, T. Pichler, and S. R. P. Silva, "Iron filled single-wall carbon nanotubes, a novel ferromagnetic medium," *Chemical Physics Letters,* vol. 421, pp. 129-133, 2006.
9. Y.-L. Mao, X.-H. Yan, and Y. Xiao, "First-principles study of transition-metal-dope single walled carbon nanotubes," *Nanotechnology,* vol. 16, pp. 3092-3096, 2005.
10. M. Weissmann, G. Garcia, M. Kiwi, and R. Ramirez, "Theoretical study of carbon-coated iron nanowires," *Physical Review B,* vol. 70, 2004.
11. Y. C. Lee, B. A. Parviz, J. A. Chiou, and S. C. Chen, "Packaging for microelectromechanical and nanoelectromechanical systems," *IEEE Transactions on Advanced Packaging,* vol. 26, pp. 217-226, 2003.
12. C. P. Poole, Jr., and Frank Owen, *Introduction to Nanotechnology*, Wiley, New York, 2003.
13. T. Hanrath and B. A. Korgel, "Influence of surface states on electron transport through intrinsic Ge nanowires," *Journal of Physical Chemistry B,* vol. 109, pp. 5518-5524, 2005.
14. C. M. Lilley and H. Qiaojian, "Surface contamination effects on resistance of gold nanowires," *Applied Physics Letters,* vol. 89, 203114, 2006.

15. S. Cuenot, C. Frétigny, S. Demoustier-Champagne, and B. Nysten, "Surface tension effect on the mechanical properties of nanomaterials measured by atomic force microscopy," *Physical Review B,* vol. 69, 2004.
16. G. Y. Jing, H. L. Duan, X. M. Sun, Z. S. Zhang, J. Xu., Y. D. Li, J. X. Wang, and D. P. Yu, "Surface effects on elastic properties of silver nanowires: Contact atomic-force microscopy," *Physical Review B,* vol. 73, 2006.
17. F. D. Novaes, Antonio J. R. da Silva, E. Z. da Silva, and A. Fazzio, "Effect of impurities in the large Au-Au distances in gold nanowires," *Physical Review Letters,* vol. 90, 036101, 2003.
18. J. He and C. M. Lilley, "Surface effect on the elastic behavior of static bending nanowires," *Nano Letters,* vol. 8, pp. 1798-1802, 2008.
19. T. Last, S. Hacia, S. F. Fischer, and U. Kunze, "Aging phenomena in single nanopatterned permalloy wires," *Physica B: Condensed Matter,* vol. 384, pp. 9-11, 2006.
20. E. R. Weber, "Understanding defects in semiconductors as key to advancing device technology," *Physica B,* vol. 340-342, pp. 1-14, 2003.
21. T. Karabacak, J. S. DeLuca, P. I. Wang, G. A. Ten Eyck, D. Ye, G. C. Wang, and T. M. Lu, "Low temperature melting of copper nanorod arrays," *Journal of Applied Physics,* vol. 99, 064304, 2006.
22. Q. Huang, C. M. Lilley, M. Bode, and R. Divan, "Surface and size effects on the electrical properties of Cu nanowires," *Journal of Applied Physics,* vol. 104, 023709, 2008.
23. K. Fuchs, "The conductivity of thin metallic films according to the electron theory of metals," *Proceedings of the Cambridge Philosophical Society,* vol. 34, pp. 100-108, 1938.
24. E. H. Sondheimer, "The mean free path of electrons in metals," *Advances in Physics,* vol. 1, pp. 1-42, 1952.
25. R. G. Chambers, "The conductivity of thin wires in a magnetic field," *Proceedings of the Royal Society of London. Series A, Mathematical and Physical Sciences,* vol. 202, pp. 378-394, 1950.
26. D. Josell, C. Burkhard, Y. Li, Y. W. Cheng, R. R. Keller, C. A. Witt, D. R. Kelley, J. E. Bonevich, B. C. Baker, and T. P. Moffat, "Electrical properties of superfilled sub-micrometer silver metallizations," *Journal of Applied Physics,* vol. 96, pp. 759-768, 2004.
27. W. Steinhogl, G. Schindler, G. Steinlesberger, and M. Engelhardt, "Size-dependent resistivity of metallic wires in the mesoscopic range," *Physical Review B,* vol. 66, 075414, 2002.
28. W. Steinhoegl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, "Scaling laws for the resistivity increase of sub-100 nm interconnects," in *IEEE International Conference on Simulation of Semiconductor Processes and Devices*, September 2003, pp. 27-30.
29. S. Maitrejean, R. Gers, T. Mourier, A. Toffoli, and G. Passemard, "Experimental measurements of electron scattering parameters in Cu narrow lines," *Microelectronic Engineering,* vol. 83, pp. 2396-2401, 2006.
30. A. F. Mayadas and M. Shatzkes, "Electrical-resistivity model for polycrystalline films: the case of arbitrary reflection at external surfaces," *Physical Review B,* vol. 1, p. 1382, 1970.
31. D. R. Lide, *Handbook of Chemistry and Physics*. New York: CRC, 2005-2006.
32. X. Y. Qin, L. D. Zhang, G. S. Cheng, X. J. Liu, and D. Jin, "The low-temperature resistance and its density effects of bulk nanostructured silver," *Journal of Physics D—Applied Physics,* vol. 31, pp. 24-31, 1998.
33. W. Zhang, S. H. Brongersma, O. Richard, B. Brijs, R. Palmans, L. Froyen, and K. Maex, "Influence of the electron mean free path on the resistivity of thin metal films," *Microelectronic Engineering,* vol. 76, p. 146, 2004.
34. G. Schindler, G. Steinlesberger, M. Engelhardt, and W. Steinhogl, "Electrical characterization of copper interconnects with end-of-roadmap feature sizes," *Solid-State Electronics,* vol. 47, pp. 1233-1236, 2003.

35. W. Wu, S. H. Brongersma, M. V. Hove, and K. Maex, "Influence of surface and grain-boundary scattering on the resistivity of copper in reduced dimensions," *Applied Physics Letters,* vol. 84, pp. 2838-2840, 2004.
36. A. Bid, A. Bora, and A. K. Raychaudhuri, "Temperature dependence of the resistance of metallic nanowires of diameter >= 15 nm: Applicability of Bloch-Gruneisen theorem," *Physical Review B,* vol. 74, p. 035426, 2006.
37. C. Durkan and M. E. Welland, "Size effects in the electrical resistivity of polycrystalline nanowires," *Physical Review B,* vol. 61, pp. 14215-14218, 2000.
38. S. Karim, W. Ensinger, T. W. Cornelius, and R. Neumann, "Investigation of size effects in the electrical resistivity of single electrochemically fabricated gold nanowires," *Physica E: Low-dimensional Systems and Nanostructures,* vol. 40, p. 3173, 2008.
39. E. J. Menke, M. A. Thompson, C. Xiang, L. C. Yang, and R. M. Penner, "Lithographically patterned nanowire electrodeposition," *Nature Materials,* vol. 5, pp. 914-919, 2006.
40. A. Kwatera and A. Sawka, "Preparation of amorphous composites of silicon nitride and carbon layers on silica glass by chemical vapor deposition method," *Journal of Non-crystalline Solids,* vol. 265, pp. 120-124, 2000.
41. B. S. Verma and S. K. Sharma, "Effect of thermal strains on the temperature coefficient of resistance," *Thin Solid Films,* vol. 5, p. R44, 1970.
42. F. Warkusz, "The size effect and the temperature coefficient of resistance in thin films," *Journal of Physics D: Applied Physics,* vol. 11, pp. 689-694, 1978.
43. J. B. Thompson, "Absolute thermoelectric power and temperature coefficient of resistance of thin continuous metal films," *Thin Solid Films,* vol. 18, p. 77, 1973.
44. C. Durkan and M. E. Welland, "Analysis of failure mechanisms in electrically stressed gold nanowires," *Ultramicroscopy,* vol. 82, pp. 125-133, 2000.
45. C. Ciofi, V. Damlo, and B. Neri, "Copper interconnection lines: SARF characterization and lifetime test," in *Proceedings of the 7th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, p. 1747, 1996.
46. P. Bruschi, C. Ciofi, V. Dattilo, A. Diligenti, A. Nannini, and B. Neri, "Copper metallizations for integrated circuits: TEM analysis and electrical characterization," *Journal of Electronic Materials,* vol. 26, pp. L17-L20, 1997.
47. G. Steinlesberger, M. Engelhardt, G. Schindler, J. Kretz, W. Steinhogl, and E. Bertagnolli, "Processing technology for the investigation of sub-50 nm copper damascene interconnects," *Solid-State Electronics,* vol. 47, pp. 1237-1241, 2003.
48. L. Lecko and R. Hrach, "Electrical and optical properties of very thin gold films," *International Journal of Electronics,* vol. 77, pp. 989-991, 1994.
49. B. Stahlmecke and G. Dumpich, "Resistance behaviour and morphological changes during electromigration in gold wires," *Journal of Physics—Condensed Matter,* vol. 19, p. 046210, 2007.
50. Q. Huang, C. M. Lilley, R. Divan, and M. Bode, "Electrical failure analysis of Au nanowires," *Nanotechnology, IEEE Transactions on,* vol. 7, pp. 688-692, 2008.
51. ASTM, *Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallizations [Metric]*, ASTM International, pp. F1260M-96, 2003.
52. P. S. Ho and T. Kwok, "Electromigration in metals," *Reports on Progress in Physics,* vol. 52, pp. 301-348, 1989.
53. J. Lienig, "Invited Talk: Introduction to electromigration-aware physical design," in *Proceedings of the 2006 International Symposium on Physical Design*, San Jose, CA, 2006, pp. 39-46.
54. K. Croes, R. Dreesen, J. Manca, W. De Ceuninck, L. De Schepper, L. Tielemans, and P. Van der Wel, "High-resolution in-situ study of gold electromigration: test time reduction," *Microelectronics Reliability,* vol. 41, pp. 1439-1442, 2001.

55. C. Pennetta, E. Alfinito, L. Reggiani, F. Fantini, I. DeMunari, and A. Scorzoni, "Biased resistor network model for electromigration failure and related phenomena in metallic lines," *Physical Review B,* vol. 70, p. 174305, 2004.
56. J. R. Black, "Electromigration—a brief survey and some recent results,"*IEEE Transactions on Electron Devices,* vol. 16, p. 338, 1969.
57. J. R. Lloyd, "Black's law revisited—nucleation and growth in electromigration failure," *Microelectronics Reliability,* vol. 47, p. 1468, 2007.
58. C. K. Hu, R. Rosenberg, and K. Y. Lee, "Electromigration path in Cu thin-film lines," *Applied Physics Letters,* vol. 74, pp. 2945-2947, 1999.
59. J. R. Lloyd, J. Clemens, and R. Snede, "Copper metallization reliability," *Microelectronics Reliability,* vol. 39, p. 1595, 1999.
60. A. Roy, R. Kumar, C. M. Tan, T. K. S. Wong, and C. H. Tung, "Electromigration in damascene copper interconnects of line width down to 100 nm," *Semiconductor Science and Technology,* vol. 21, pp. 1369-1372, 2006.
61. Q. Huang, C. M. Lilley, and R. Divan, "An in situ investigation of electromigration in Cu nanowires," *Nanotechnology,* vol. 20, p. 075706, 2008.
62. C. K. Hu, K. Y. Lee, L. Gignac, and R. Carruthers, "Electromigration in 0.25 μm wide Cu line on W," *Thin Solid Films,* vol. 308-309, p. 443, 1997.
63. L. Arnaud, R. Gonella, G. Tartavel, J. Torres, C. Gounelle, Y. Gobil, and Y. Morand, "Electromigration failure modes in damascene copper interconnects," *Microelectronics and Reliability,* vol. 38, pp. 1029-1034, 1998.
64. R. E. Hummel and H. J. Geier, "Activation energy for electrotransport in thin silver and gold films," *Thin Solid Films,* vol. 25, p. 335, 1975.
65. K. L. Tai and M. Ohring, "Grain-boundary electromigration in thin films II. Tracer measurements in pure Au," *Journal of Applied Physics,* vol. 48, pp. 36-45, 1977.
66. B. J. Klein, "Electromigration in thin gold films," *Journal of Physics F: Metal Physics,* vol. 3, pp. 691-696, 1973.
67. S. Kilgore, C. Gaw, H. Henry, D. Hill, and D. Schroder, "Electromigration of Electroplated Gold Interconnects," *Materials Research Society Symposium Proceedings,* vol. 863, p. B8.30, 2005.

This page intentionally left blank

CHAPTER 2

Texture and Microstructure Dependence of Electromigration Defect Nucleation in Damascene Cu Interconnect Lines Studied In Situ by EBSD

Kabir Mirpuri, Jerzy Szpunar, and Horst Wendrock

2.1 Introduction

The *integrated circuit* (IC) chip is one of the wonders of the world: one of the most sophisticated and smallest composite structures humans have ever created. Interestingly enough, there is a movement to *decrease* the features of the chip in order to realize more efficient and faster processing. The rate at which the component feature size is decreasing is closely aligned with the roadmap that was laid down by the Semiconductor Industry Association (SIA) in 1994. Termed the *National Technology Roadmap for Semiconductors* (NTRS), its fundamental guiding principle is basically the maintenance of Moore's law, which predicts that the degree of shrinkage on chips should double every 2 years. Decreasing component size is often characterized in IC technology by the minimum line width. This is usually defined as the

smallest lateral feature size that is printed on the wafer surface during the fabrication process.

It is now generally accepted that the overall circuit performance will be dictated by the efficiency with which the devices are connected rather than by the speed of the individual devices. The wiring material used to connect various devices on the electronic chip is termed the *interconnect*. Thus, interconnects are the means of transportation of information within a microelectronic circuit. The three main interconnect materials used in the semiconductor industry belong to the high-conductivity metal family, for example, Al, Al-Cu alloy, Cu, and Cu-Ag alloy. The process of incorporation of metal in the electronic chip is termed *metallization*. The semiconductor industry has made a gradual transition over the years from Al- to Cu-based metallization because of the realization of some basic advantages such as the higher conductivity of Cu compared to Al, which leads to faster signal propagation in the chip. This enables the chip to function faster with increased efficiency.

2.1.1 Transition from Al to Cu as Interconnect Material of Choice

Several challenges were encountered in incorporating Cu over Al. The first and foremost was the fabrication of Cu using the traditional *reactive ion etching* (RIE) method because of the lower reactivity between the Cu and Cl plasma. Second, where Al could easily be deposited by *physical vapor deposition* (PVD), it was found increasingly difficult to get the Cu deposited by PVD in narrow features. These problems were overcome by adopting a new process called the *Damascene process* and using electroplating as the means of depositing the major portion of the Cu. The term *Damascene* originates from one of the ancient arts of the Middle East involving inlaying metal in ceramic or wood for decoration. Figure 2.1 compares the fabrication techniques for incorporating Al and Cu in microelectronic circuits. Figure 2.1*A* shows the process steps for Al and Fig. 2.1*B* for Cu. The Al lines are fabricated by depositing a thin film of Al by magnetron sputtering. Prior to Al deposition, a thin layer of Ti or TiN is deposited that acts as a diffusion barrier and at the same time works as an antireflection coating during the lithography process. After this the Al lines are patterned by an RIE process. Contrary to this in the case of Cu, the *interlayer dielectric* (ILD) is deposited following the via plug process. Subsequent to this, trenches are defined and etched in the ILD. A thin layer of diffusion barrier such as Ta or a Ta/TaN stack is deposited by PVD. The barrier prevents the diffusion of Cu into the surrounding Si. A thin film of Cu termed the *seed layer* is deposited by PVD on the top of the diffusion barrier. As the name implies, the seed layer serves as a seed for electroplating a Cu overburden on the top of it. After Cu has

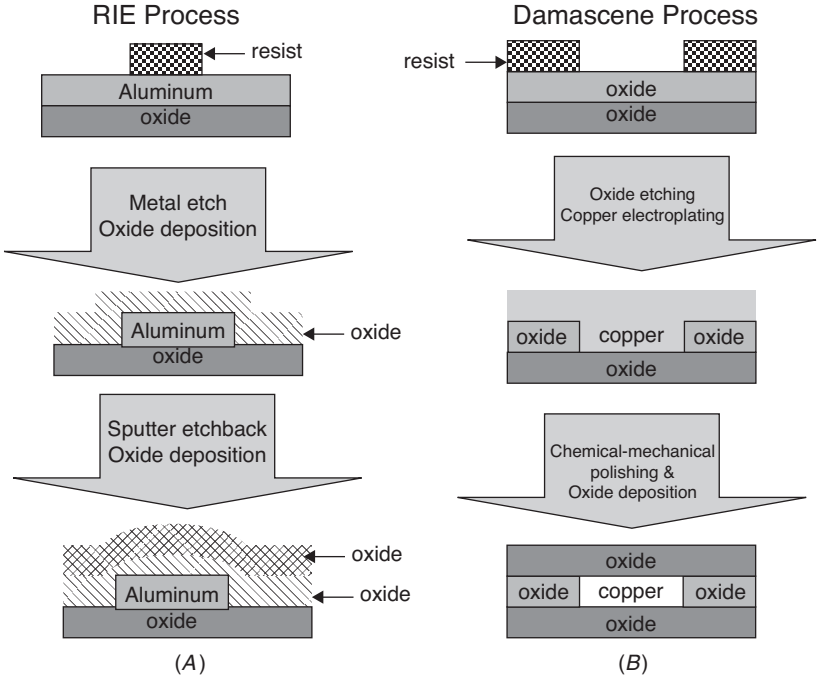


Figure 2.1 Schematic diagram comparing the process steps for Al (conventional) and Cu (inlaid) interconnect technologies.

been electroplated, the top overburden layer is removed by *chemical mechanical polishing* (CMP), leaving Cu embedded within the trench.

2.2 Electromigration

Electromigration is a phenomenon that causes migration of metal atoms in the interconnect lines when subjected to very high current densities. At very high current densities, the motion of electrons through the tiny conductor wire is equivalent to the "electron wind." The metal atom gains momentum from collisions with the conducting electrons and starts its motion along the direction of this electron wind. Figure 2.2 shows a schematic of this phenomenon, followed by real images of electromigration damage in Cu interconnect lines.

As a consequence, the migrating atoms leave behind vacancies, and the combination of these vacancies gives rise to the formation of a void at the cathode. The migrating atoms accumulate toward the anode end, forming hillocks. Both vacancies and hillocks can be seen in Fig. 2.2.

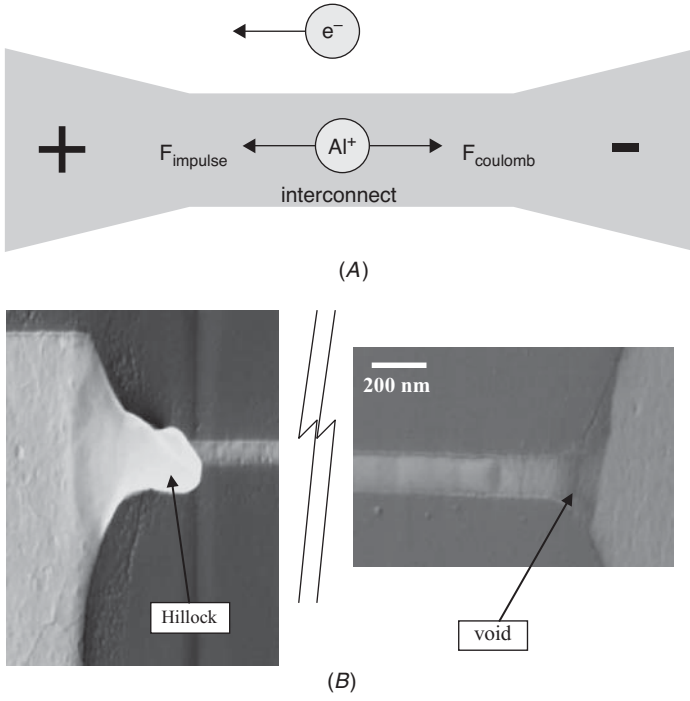


Figure 2.2 Electromigration in interconnect lines: (*A*) resulting forces on metal ions, and (*B*) scanning electron micrograph of a totally damaged Al interconnect, showing voids and hillocks in a Cu interconnect.[59]

The electromigration driving force due to momentum transfer is given by

$$F = z^* \mathrm{e} \rho j \tag{2.1}$$

where z^* is a dimensionless quantity known as the effective charge or the effective valence, e is the electronic charge, ρ is the resistivity, and j is the current density. The mass flux J, in the absence of other driving forces, is given by

$$J = \frac{DFC}{kT} = \frac{DC}{kT} z^* \mathrm{e} \rho j \tag{2.2}$$

where C is the concentration of diffusing atoms, D is the thermally activated diffusion coefficient, and kT is the average thermal energy.

However, the most interesting aspect of electromigration is that the driving force F is not the only force acting in the conductor line during electromigration. In other words, the diffusion of atoms in the lines is not entirely controlled by the electric current. There is

an additional parameter, the *chemical potential*. As a result, in general Eq. (2.2) could be expressed as

$$J = \frac{DFC}{kT} = \frac{DC}{kT}\nabla\mu \tag{2.3}$$

where $\nabla\mu$ is the gradient in the chemical potential. There are several factors that affect the chemical potential, such as the residual stress and its gradient along the interconnect line, microstructural features such as orientation of grains, the dislocation density, high angle and coincident site lattice (CSL) boundaries, and grain size. In fact, F is also one of the subsets of chemical potential. In the present chapter we focus on the influence of the grain orientations on electromigration defect nucleation. But before we delve further, let us understand the definition of *texture* and its measurement, significance, and representation for a metallic system.

2.3 Texture in Metals

The basic unit forming metals is a crystal or *grain*. A unit volume of a piece of metal contains millions of grains, making it a polycrystalline entity. The way the metal behaves and the unique properties it exhibits greatly depend on its atomic structure, the configuration of its atoms, the spacing between the planes formed by these atoms, etc. However, in addition to these inherent parameters, the properties of metal are greatly influenced by the way in which the various crystals or grains are oriented. For example, consider a cubic crystal with highlighted <100> directions (Fig. 2.3). The shaded triangular plane is the (111) plane. It is known that for metals having a *face-centered cubic* (FCC) crystal structure, the <111> direction has the highest modulus of elasticity, whereas <100> has the lowest. Thus, if most of the grains in the specimen are oriented so that the <100> direction is parallel to the direction of an externally applied uniaxial tensile load, then the force required to elastically deform the specimen will be much less compared to the case in which most of the grains are oriented with the <111> direction parallel to the load. Clearly the material will exhibit higher elastic strength in the latter case. Strength apart, several other properties of metals, such as magnetic, electrical, wear, and corrosion properties, depend strongly on the texture of the material. The degree of texture in turn strongly depends on the number of oriented grains; the greater the number of oriented grains, the greater the tendency of the material to be anisotropic.

There are several ways in which texture can be represented, ranging from pole figures and inverse pole figures to *orientation distribution functions* (ODFs) depending on the degree of complexity. All the methods correlate the orientation of three <100> axes of the crystal grain with the three principal directions of the geometrical specimen,

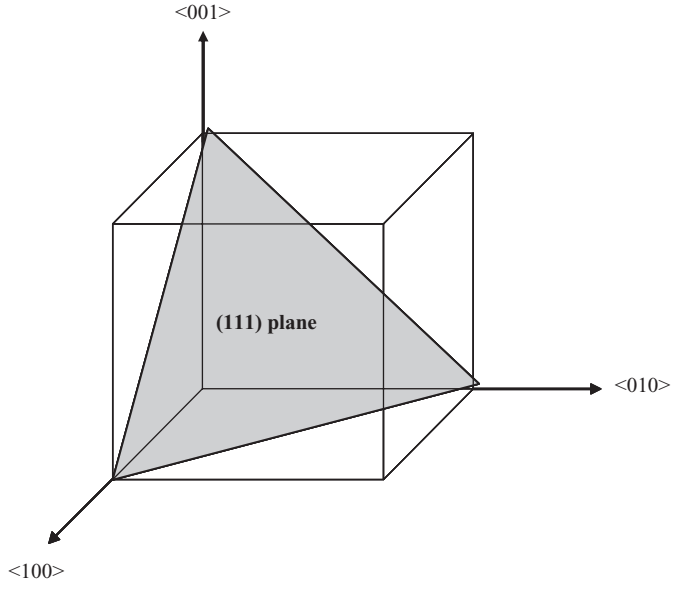


Figure 2.3 A cubic crystal with highlighted <100> directions and (111) plane.

usually normal, transverse, and longitudinal. ODFs are used to represent the entire 3D texture map of the material, whereas more general textures including fiber can be easily portrayed through the pole and inverse pole figures because of the symmetrical configuration of the FCC crystals. A detailed description of the representation methods is available.[1]

Texture can be measured using x rays and electron beam using simple diffraction techniques. X rays are better for larger samples such as rolled steel specimens because of the greater depth of penetration and good statistics. For very small specimens such as chips with patterned interconnects, electron beam analysis is a better way to go because information can be obtained through very small desired regions of interest. Currently, *orientation imaging microscopy* (OIM) is the most versatile technique to measure the local texture in the metallic systems. OIM indexes the *electron backscatter diffraction* (EBSD) patterns that emerge when an electron beam strikes the surface of a crystal grain using an attached camera in the *scanning electron microscope* (SEM) chamber. The software analyzes the patterns and, based on an established, in-built voting scheme, predicts a series of orientations that closely match that of the crystals, starting from the best match. OIM is a highly versatile technique because it can be used not only to measure the individual grain orientation, but also simultaneously to provide an idea of the nature of the grain boundary, grain size, relative dislocation density, strain, etc. A detailed description of the technique is available in several published books and literature reviews.[2,3]

2.3.1 Impact of Texture and Microstructure on the Reliability of the Interconnects

2.3.1.1 Electromigration in Al Interconnects

Electromigration was discovered in Al interconnects in the 1960s and at that time posed a serious challenge, almost threatening the progress of the IC industry. However, considerable research on texture, microstructure, and solute addition in Al led to the successful implementation of Al interconnect technology. The important role of these parameters is discussed next.

Effect of Texture and Microstructure There are three main atom diffusion pathways that dictate the electromigration failure—grain boundaries, interfaces, and bulk transport. In the case of Al, the grain boundary was recognized as the main diffusion pathway with the most detrimental contribution to electromigration failure from the grain junctions or triple points. Mass transport was also found to be affected by the orientation of the grain-boundary plane with respect to the direction of electric current flow. Soon it was recognized that a bamboo grain structure eliminated the parallel orientation of the grain boundaries to the current flow. The characteristic of the bamboo grain structure is that there is only one single grain spanning the width of the line. This slows down atom migration and leads to superior resistance against electromigration. In such bamboo-grain interconnects, the major diffusion pathway is the interface between Al and the surrounding dielectric sidewall. But because Al forms a strong adherent oxide, the interface diffusion transport does not contribute strongly to electromigration damage. Thus, the Al-dielectric interface also lost its predominance as a contributor to electromigration damage.

It was now known that with the shrinking line width, the grains became more bamboo shaped. The larger grain size (greater than the line width) was shown to have better resistance because it reduced the number of grain boundaries per unit area of the interconnect line. Experiments by d'Heurle and Ames[4] showed electromigration to be virtually absent in single crystalline films, and more recently a higher electromigration resistance in single crystalline lines has been shown by Joo et al.[5,6] Other reports also confirmed the impact of grain size on electromigration lifetime[7,8] However, one study[9] showed that apart from the larger grain size, the (111) texture of the film also contributed to higher resistance to failure. A series of experiments that followed clearly established the benefits of having (111) texture in Al interconnects.[10,11] A separate study showed a similar result for the (111)-textured bamboo grains.[12] Vaidya et al.[13] found that *mean time to failure* (MTF) increased with an increase in grain size (S) and strength of the (111) texture and with decreasing spread in the grain size distribution (σ). Thus, MTF was found to be proportional to an

empirical microstructural quantity η, given by

$$\eta = \frac{S}{\sigma^2} \log \left(\frac{I_{111}}{I_{100}} \right)^3 \tag{2.4}$$

where S is the grain size, σ is the distribution in grain size, and I represents the diffraction peak intensity from the corresponding texture components. This was the first time that a rationale was presented that took into account the effect of microstructural features.

As noted by Field and Wang,[14] materials with strong (111) texture usually have a higher number of low-angle boundaries and special boundaries. These boundaries have a lower diffusion coefficient, thus improving the electromigration resistance of the material. Thus, the improvement in electromigration resistance attributed to the (111) texture is a function of grain boundary structure and not of texture alone.

Effect of Alloying Al on Electromigration Copper is the most common alloying element added to Al to improve electromigration resistance. Studies have shown that adding higher concentrations of Cu, even beyond the solubility limits in Al (which is 0.05 wt%), drastically improved the electromigration performance. The longest lifetimes were observed with 16% Cu. Later it was shown[15] that addition of 4% Cu provided the same performance as higher amounts of Cu. Now it is a general practice in industry to add about 1 at.% of Cu. This resistance enhancement comes from two factors: first, the depletion of Cu from certain regions, and second, the formation of voids at Cu-depleted regions. The depletion of Cu, void nucleation, and then growth consumes a great deal of time and adds to the life of Al-Cu interconnects compared to pure Al, where a void would simply nucleate and grow. The excess Cu forms Al_2Cu precipitates in the Al grain boundaries. When Cu is depleted because of electromigration, these precipitates then dissolve to replenish the Cu loss in the grain boundary. The effect of addition of other elements has also been tested, and it was found that addition of Mg and Cr is more beneficial than that of Ni, Au, and Ag.[16] Experimentation with ternary and quaternary Al alloys also showed beneficial effects.[17,18] Some other schemes utilizing application of barrier and intermetallic layers in the interconnect system were also found to be advantageous.[19–25] The scheme involved depositing a 20- to 60-nm layer of the desired transition metal (Cr, Ti, Hf, or Ta) between two half-normal-thickness layers of Al-Cu. The improvement was attributed to the formation of Al transition metal compound, which effectively blocked crack growth through the film.

2.3.1.2 Electromigration in Damascene Cu Interconnects

As mentioned earlier, there were two major reasons for adoption of Cu as an interconnecting metal. The first was because of its higher

conductivity. Second, it was anticipated that because Cu had a higher melting point (1083°C) than Al (660°C), atomic diffusion should be much slower in Cu, and therefore the electromigration resistance will be superior to that in Al. However, a series of experimental investigations showed some surprising results. In some cases the Cu interconnects showed better electromigration resistance compared to Al,[26] and in other cases they behaved poorly.[27,28] These results show that there is some other fast diffusion pathway in Cu interconnects that may, at times, be responsible for poor electromigration performance.

Table 2.1 compares the activation energies for various diffusion pathways in Al, Al(Cu), and Cu interconnects. It can be seen from the table that the activation energy for the interfacial diffusion in Al alloys is higher than the grain boundary activation energy. As a consequence, the wider Al alloy lines having a polycrystalline grains will have shorter life compared to narrow lines with quasi-bamboo grain structure where interfacial diffusion will dominate. This scenario is totally the opposite in the case of Cu lines, where the activation energy for interfacial diffusion is less than the grain boundary diffusion. The reason why the dominant diffusion pathway has changed from grain boundary in Al to interface in the case of Cu interconnects is the way these two different interconnect systems are fabricated. As mentioned earlier, the damascene process provides lower cost and ease of fabrication compared to the subtractive ion etch method used for patterning Al. However, this advantage for Cu interconnect fabrication is diminished by lower activation energy for interfacial and surface diffusion. To make the matters worse, in contrast to Al, Cu has poor adherence to its oxide, which results in a lower activation energy for surface diffusion. Hence, unlike Al, the decreasing line widths in the case of Cu provide no additional advantage when it comes to electromigration. The electromigration in narrower Cu interconnects is very sensitive to the interface conditions, which are decided by the fabrication process parameters.[27] Poor electromigration performance seems to be direct evidence of poor interface conditions.

Metal	Lattice	Grain Boundary	Interface	Surface
Al	1.4	0.6	—	—
AlCu	1.2	0.7	0.9–1.0	—
Cu	2.1	1.2	0.9–1.2	0.7

Source: Ref. 27.

Table 2.1 Activation Energies (in eV) for Various Diffusion Pathways[27]

Role of Texture and Microstructure First reports of electromigration analyzed the Cu lines deposited using PVD and *chemical vapor deposition* (CVD). A series of experiments were performed by the same group of authors—Arnaud et al.[29,30] and Berger et al.[31] In one of the studies they discussed the effect of CVD-fabricated line widths on electromigration performance using both wafer- and package-level tests. The wide lines had weak (100) fiber texture, whereas the narrow lines were not textured. The higher line widths showed lower values of activation energy for electromigration combined with grain-boundary grooving indicating that diffusion through the grain boundaries was active. In the case of narrower line widths, the failure was attributed to surface diffusion at the regions where bamboo grains and grain boundaries were present. The density of void formation at the cathode increased with increasing current density in the case of wide lines. For narrow lines, the failures were more evenly distributed along the line, but void formation occurred mostly at the cathode end of the lines and was attributed to microstructure gradients.

In other experiments,[29] the same authors compared the role of fabrication methods (PVD vs. CVD) in Cu lines with the same line width and again using both wafer- and package-level tests. The PVD-deposited lines showed higher mean grain size with a random texture, whereas CVD-deposited lines showed a smaller mean grain size with weak (100) texture. The PVD samples showed better performance than the CVD samples. This was attributed to larger grain size and lower surface diffusion. Texture was shown to have negligible role in influencing the performance of the lines. Both grain-boundary and surface diffusion were shown to have occurred in the PVD and CVD samples. In yet another experiment,[31] both PVD and CVD samples were studied, but CVD samples had different line widths. Again, PVD samples showed better performance. Both higher and lower CVD line widths showed similar values of activation energy, indicating surface diffusion.

In another investigation, Gladkikh et al.[32,33] reported an explicit correlation of electromigration to microstructure. Three different kinds of microstructures were obtained by varying the processing conditions with mean grain sizes of 500, 150, and 120 nm. To study the role of surface diffusion, electromigration was carried out with and without the top Ta layer. The morphology of defects recorded after electromigration tests was different in all the three cases. In the case of lines with large grain size, the voids expanded across the conductor line, whereas for the lines with smaller grain size, global thinning of the grains was observed. In the case of films covered with Ta, no changes in the surface morphology were observed, and void formation was observed only at the sidewall, indicating that surface diffusion was absent. Clearly the interplay of grain boundary and surface diffusion was analyzed and a significant role of microstructure in influencing electromigration was demonstrated.

McCusker et al.[34] showed the surface diffusion to be active in the Cu lines which were fabricated via the RIE process. There was no silicon oxide surrounding the Cu lines. The method of deposition was sputtering. Cu lines with two different surface conditions were obtained by exploiting the gettering property of the Ta.[35] The freshly deposited Ta films gettered the residual oxygen and water vapor, enabling purer copper films to be deposited. In one case, deposition was done with Ta, and in other without Ta. The pure films with Ta failed by global thinning of the material as described by other authors,[32,33] indicating that surface diffusion was active. In the Cu lines without Ta, which were supposed to be contaminated, the shape of the voids was different for the cases where failure was fast, indicating that the failure mechanism was being influenced by something other than surface diffusion. The presence of slitlike voids was linked to a different failure mechanism where surface diffusion was suppressed. The Cu lines coated with a Ta overlayer showed an increase in time to failure due to suppressed surface diffusion. Finally, the role of surface diffusion was ascertained by letting the Cu surface be oxidized by introducing air, in which case failure was again rapid. The authors[34] attributed this to the fact that oxidation prevents uniform surface diffusion, giving fast localized failures. The authors[34] claim surface diffusion to be the healing mechanism, and that its absence leads to early failures.

The common methodology for producing Cu interconnects is electrodeposition of Cu in the damascene trenches. Several features typical of the damascene process lead to textures that are different from those observed in Al interconnects. For example, during self-annealing/annealing of Cu films, there is competition between the surface and strain energies, leading to formation of different energy-minimizing textures.[36] Additionally, Cu itself is prone to twinning because of its lower stacking fault energy. Twinning leads to the weakening of the (111) texture.[37] A series of initial experiments had shown interfacial damage to be the main contributor to failure, but later it was found that grain boundary transport also contributed to interconnect damage. Another peculiarity of self-annealing is abnormal growth of some grains in Cu films, which is driven by a combined role of impurities, surface, and strain energies.[38] As a result, the microstructure of the Cu interconnects often shows the presence of some elongated bamboo grains followed by a cluster of small grains.[39] Such a microstructure is undesirable if electromigration through grain boundaries is predominant. But it has an almost negligible role to play if surface diffusion is the active mode of mass transport. This is because on the surface, a triple point is not an effective flux divergence point. However, Lloyd[40] has shown that the presence of such clusters of grains can give rise to stress gradients along the Cu line, which in turn can influence electromigration behavior.

Two different studies[28,41] showed that the role of texture and microstructure became less significant for the damascene Cu lines when

line width decreased. Electromigration experiments[28] were carried out on Cu lines with different widths with two different underlying barrier layers of Ta and TiN. It was found that although the Cu films on TiN had smaller grain size and weaker (111) texture, they showed a longer electromigration lifetime than samples with a Ta barrier layer. This indicates the absence of grain boundary diffusion, because its presence would have led to a higher lifetime of Ta barrier samples because the grain size of the Cu lines is large. Finally, the authors hold the Cu-barrier layer interfaces responsible for the rapid Cu diffusion that led to the lower observed lifetimes in Ta barrier films.

In a detailed study, Proost et al.[42] reported electromigration results for the first time using the drift velocity experiments in damascene Cu lines. Three different line widths—0.4, 0.7, and 10 μm—with three different barrier layers—Ta, TaN, and TiN—were investigated. The 0.4-μm line widths had bamboo grain structure. The 0.7- and 10-μm line widths had more than one grain along the width of the lines, giving rise to a network of grain boundaries along the line width. It was found that the activation energy for 0.7- and 10-μm line widths for both TaN and TiN was the same even though the Cu plating chemistry was different for both the barrier layers, indicating that grain boundary diffusion was active. Interestingly, the drift velocity rate was higher for the TaN samples with weak (100) texture compared to the TiN samples with (111) texture for the same line widths, indicating that the (111) texture might be responsible for the lower drift rate; however, the authors attribute it to impurity segregation at grain boundaries in TiN samples. In the case of 0.4-μm lines, the interface diffusion was held responsible for the observed differences in drift rates because the activation energy was the same as that of polycrystalline lines. Again for the 0.4-μm lines it was Ta samples that showed the highest drift rate, indicating that the barrier-Cu interface structure decides the diffusion. Thus, an increasing number of studies show the lethal influence of Ta on Cu interconnect reliability.

One more systematic recent study[43] showed the Cu-barrier interface to be the active diffusion pathway in interconnects having widths as small as 80 nm. Though the lines showed the presence of quasi-bamboo grain structure and hence some grain boundary clusters, the authors systematically show that it is the interface diffusion that is active. The authors demonstrate that besides the primary mechanism of failure, which is interface diffusion, there is also a secondary failure mechanism that is active at the cathode end. The microstructural dependence of the secondary mechanism is unknown; it occurs by formation and annihilation of small voids. These voids can grow from preexisting voids, local stress gradients, or regions with poor adhesion to the Ta barrier layer.

The same authors in a different study[44] discussed the influence of the top passivation layer on electromigration damage. They investigated 0.25-μm lines with top layers of SiN and SiCN. With the

SiN layer, there was extensive interface damage at the periphery of Cu line. With the SiCN layer, the formation and growth of localized voids without extensive interface damage was observed. The barrier layer again was Ta. Thus, most of these studies show that Ta has a negative impact on reliability of interconnect lines.

To summarize, the role of texture in influencing the reliability of the Al and Cu interconnect lines has been clearly identified. For Al films it is well established that the (111) texture provides higher resistance to electromigration and hillock formation.[45,46] The failures were found to be occurring at regions where local variations in (111) texture were observed.[47] In the case of Al-based metallurgies, the textures are relatively uncomplicated because there are only two components, mainly (111) fiber and rarely (110) fiber.[48] As a matter of fact, there is an inherent tendency of the system to form (111) texture in the vapor-deposited Al films. However, compared to Al, in the case of Cu we find the presence of (100) along with (111) components, with the strength of (111) usually being higher.[48] In a strongly textured Cu film, a (511) component is quite often seen. The (511) component is produced by twinning in the Cu films. Multiple twinning leads to formation of still other fiber textures.[37,48,49] The (110) component is also quite often observed for electroplated Cu films compared to vapor deposits and is accompanied by a considerable random component.[48]

Unlike Al, the influence of (111) texture on the reliability of Cu films and lines is controversial. One article reports beneficial effects of a (111) texture, whereas others reports the opposite effect on electromigration reliability.[26,28] Some early reports cite the formation of voids near the regions with lower (111) strength.[50–52] The role of texture becomes even more significant in Cu, taking into account its highly anisotropic nature compared to Al. In fact, there have been reports of formation of voids at the twin boundaries in Cu films/lines.[53] TEM investigation showed that the voids formed at metastable incoherent (322) twins, and FEM calculations showed that at such grain boundaries a stress gradient follows from the anisotropic elastic constants of Cu.[53]

Like texture, the microstructure is also important in deciding the reliability of the interconnects. With the decreasing line width there is formation of bamboo or semibamboo grain structure in the interconnect lines. The formation of bamboo grain structure clearly had advantages in increasing the electromigration resistance of the Al lines.[54] This is because the bamboo grain structure leads to the alignment of grain boundary planes perpendicular to the trench sidewalls, thus offering higher resistance to the motion of electrons caused by grain-boundary scattering.[55] However, this is not as much the case for Cu lines with a bamboo grain structure, because the lower activation energy of interfacial diffusion outweighs the advantages of bamboo grain structure in Cu damascene lines.[28] In the case of Al, the CSL boundaries were shown to have higher resistance to electromigration damage.[56] However, in the case of Cu there are no reports clearly

showing the advantages of CSL boundaries, but the high-angle grain boundaries have certainly been reported as the potential failure sites.[57] There is also no clear understanding of the impact of the texture or local grain orientations on the reliability of the Cu lines.

The present investigation focuses on studying the possible impact of grain orientation on defect nucleation during electromigration in narrow damascene Cu interconnect lines. The investigation monitors damage origination in situ, as it happens, while the Cu lines are being stressed within the SEM chamber using a special apparatus. Based on analysis of the results, a failure mechanism is proposed that explicitly takes into account the effect of texture and microstructure on causing electromigration damage.

2.4 Experimental Setup

The Cu damascene lines were fabricated by electrodepositing Cu in 100-nm-deep trenches that were predeposited with a 10-nm PVD Ta/TaN barrier and PVD Cu seed. The width of the lines varied from 130 to 250 nm; the lengths were 20 and 50 μm. The lines were given a preannealing treatment at 400°C for 30 minutes to stabilize the microstructure prior to the electromigration test. Only single-level damascene Cu lines were fabricated to eliminate the additional effects of via stresses, which otherwise might interfere with the kinetics and mechanism of defect formation and interpretation of the results. The apparatus setup used to stress the lines is shown in Fig. 2.4. Figure 2.5 shows the 100 μm $\times$ 100 μm contact pad on both sides of

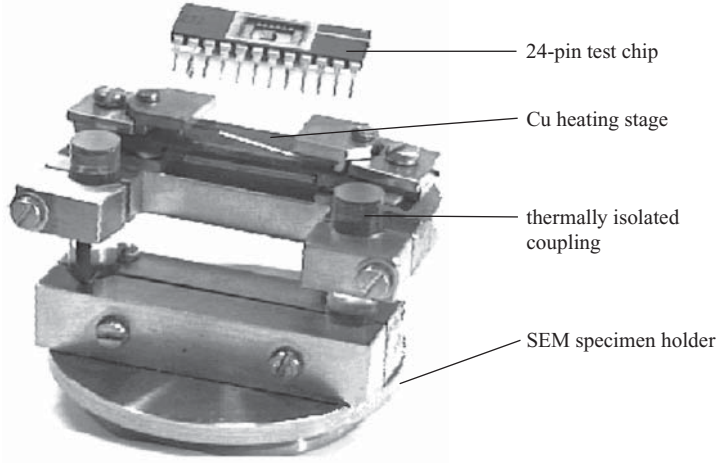


Figure 2.4 In-house designed apparatus for in situ EBSD measurements during electromigration testing of Cu damascene lines.

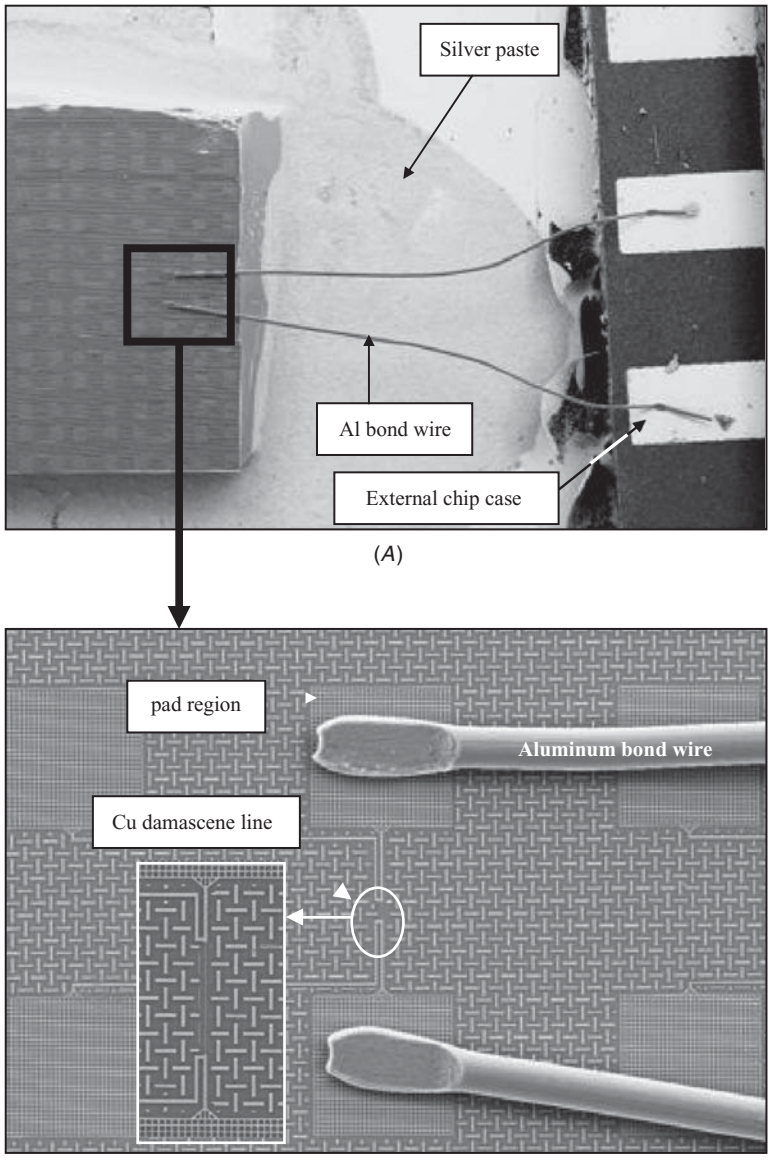


Figure 2.5 (*A*) Experimental setup for electromigration test. (*B*) Magnified view of the highlighted square region in part (*A*) showing the Cu damascene test structure layout together with Al bond wires.

the damascene Cu line. A dc current was applied to the interconnects through Al wires that were bonded to the contact pads and external chip case as shown in Fig. 2.5. A temperature of 250°C was maintained throughout the test to negate the effect of Joule heating. The chip case was mounted in an SEM stage designed in-house, making it possible to make in situ inspection as the lines were being stressed. In order to accelerate the acquisition of results, experiments were carried out at a high current density of 20 MA/cm^2 so as to get the results within a time frame of 30 to 70 hours. The EBSD scans were performed under high vacuum conditions at 20 kV, a working distance of 15 mm, and a sample tilt of 70 degrees. Scanning was performed using a hexagonal grid mode with a scan step size of 20 nm inside a field emission gun SEM (LEO Gemini 310) with orientation imaging microscopy apparatus attached. The processing of the in situ EBSD data was done using CHANNEL 5 software from HKL Technology.[58] Several different case studies were performed on Cu lines with different widths and lengths, but only representative cases are discussed here.

2.5 Case 1

Figure 2.6 shows the results for the Cu line 200 nm wide and 50 μm long. The figure shows SEM images at specific locations along the line where voids and hillocks formed during the test. The voids have been highlighted as V2 and V3; the hillocks have been highlighted as H2a, H2b, and H2c.

2.5.1 Correlating Grain Orientation to Voids

Figures 2.7 and 2.8 show that the voids V2 and V3 formed in the neighborhood of (111) grains. Figure 2.7 displays the orientation contrast maps and SEM images for V2 before and after the failure. The grains have been named from A to E and have been grayscale colored based on their orientation corresponding to that depicted in the legend. The orientation of these grains and misorientation between them is listed in Table 2.2. We can see from Fig. 2.7 that the void V2 is located in the vicinity of grains B and C. In fact, void V2 nucleated at the high-angle grain boundary between the grains A and B. The boundary has a misorientation of 33.4 degrees. The formation of void V2 resulted from the erosion of mass at the trench sidewall starting at grain B and then continuing through grain C and finally consuming the entire grain D in its stride. Grain C is of the orientation close to {111}<112> and is surrounded by Σ3 twin boundaries above and below. It is interesting to notice that the void growth continued along the (111) grain even though it is not surrounded by high-angle grain boundaries. The consumption of grain D was easy because it was a long, narrow grain between grain E and the trench sidewall, located right in the path

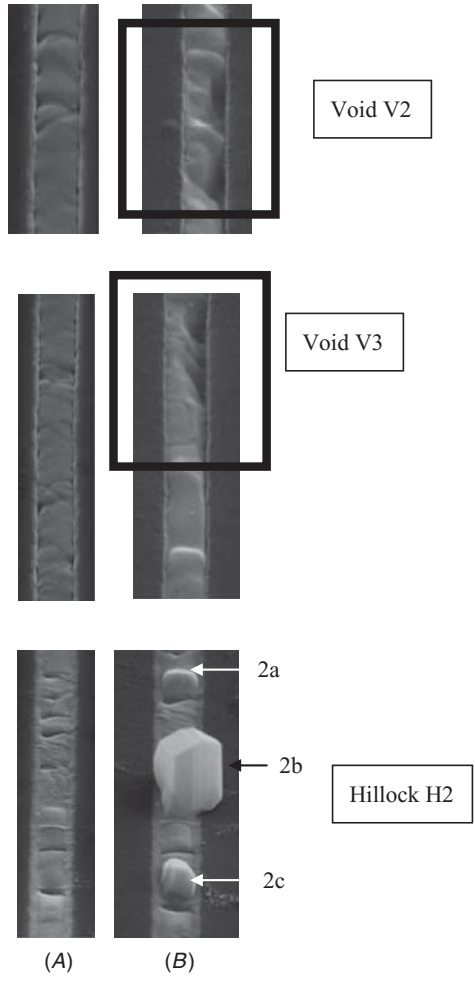


Figure 2.6 SEM images showing formation of voids and hillocks in a 200-nm-wide and 50-μm-long Cu damascene interconnect line (*A*) before and (*B*) after the electromigration test.

where erosion continued along the trench sidewall from grain B to grain C. Interestingly, the orientation of grain D is {111}<112>. Moreover, the presence of a high-angle grain boundary having a misorientation of 24 degrees between grains C and D made the elimination of grain D quite feasible because of easy diffusion along high-angle grain boundaries. The contribution of this high-angle grain boundary to the consumption of grain D is even more pronounced because it meets the trench sidewall. In short, once again a (111) grain having a high-angle grain boundary was associated with void formation (grain D). Even for the case where the (111) grain was not surrounded by a high-angle grain boundary (grain C), a void nucleated in its neighborhood.

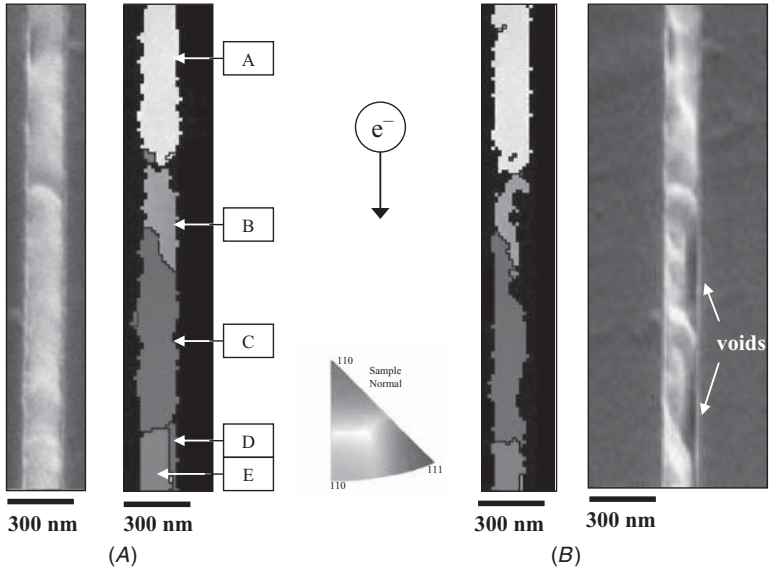


FIGURE 2.7 Orientation contrast maps (*A*) before and (*B*) after the electromigration test on a damascene Cu interconnect line 50 μm long and 200 nm wide computed at the void nucleation site. The SEM images have been depicted for purpose of comparison at a 70-degree tilt with tilt correction.

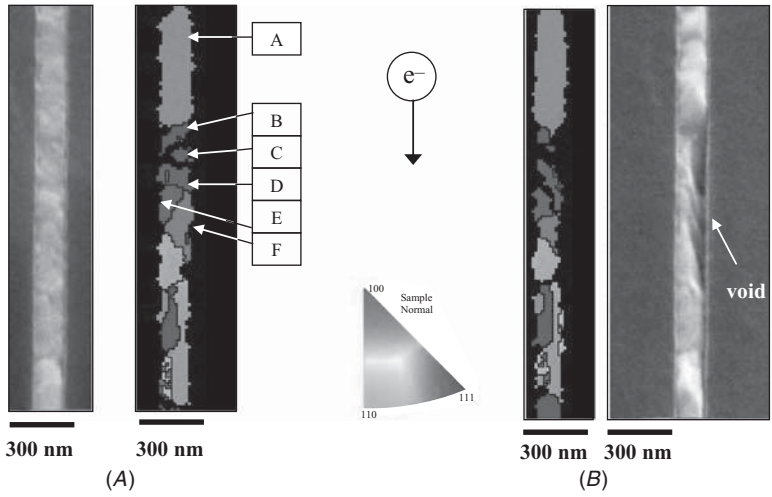


FIGURE 2.8 Orientation contrast maps (*A*) before and (*B*) after the electromigration test on a damascene Cu interconnect line 50 μm long and 200 nm wide computed at the void nucleation site V3. The SEM images have been depicted for purpose of comparison at a 70-degree tilt after applying tilt correction.

Grain1	Grain2	Misorientation (deg)/ Boundary Character
A = (417)[-211]	B = (013)[-100]	33.4
B	C = (111)[-1-23]	Σ3
C	D = (111)[2-1-1]	24
D	E = (106)[64-1]	Σ3
C	E	Σ3

Table 2.2 Orientations of the Grains Listed in Fig. 2.7 and Misorientation between Them

Figure 2.8 compares the orientation maps and SEM images associated with V3 before and after the failure. The SEM images have been displayed for comparison. When we compare the orientation maps and corresponding SEM images, we find that the nucleation of a void occurred again in the neighborhood of (111) grains. In order to highlight the role of microstructure, we have named the grains in Fig. 2.8*A* from A to F. The orientation of these grains and misorientation between them is listed in Table 2.3. We find that most of the (111) grains were surrounded by Σ3 twin boundaries with the exception of a 30-degree high-angle grain boundary between grains D and E. The misorientation between grains D and F is about 47 degrees. Thus, as with void V2, we again find that though a majority of the (111) grains around the void V3 were surrounded by Σ3 CSL boundaries, void nucleation occurred around these grains even in the absence of high-angle grain boundaries. Thus, it seems that the presence of high-angle grain boundaries is not a necessary condition for nucleation of a void; rather, the necessary condition is the association of (111) grains with void nucleation. However, if high-angle grain boundaries are present, they will further facilitate the damage nucleation.

Grain1	Grain2	Misorientation (deg)/ Boundary Character
A = (128)[6-71]	B = (111)[7-1-6]	Σ3
B	C = (111)[-615]	Σ3
C	D = (111)[1-21]	10.8
D	E = (111)[-3-14]	30
E	F = (119)[0-91]	Σ3
D	F	47.3

Table 2.3 Orientations of the Grains Listed in Fig. 2.8 and Misorientation between Them

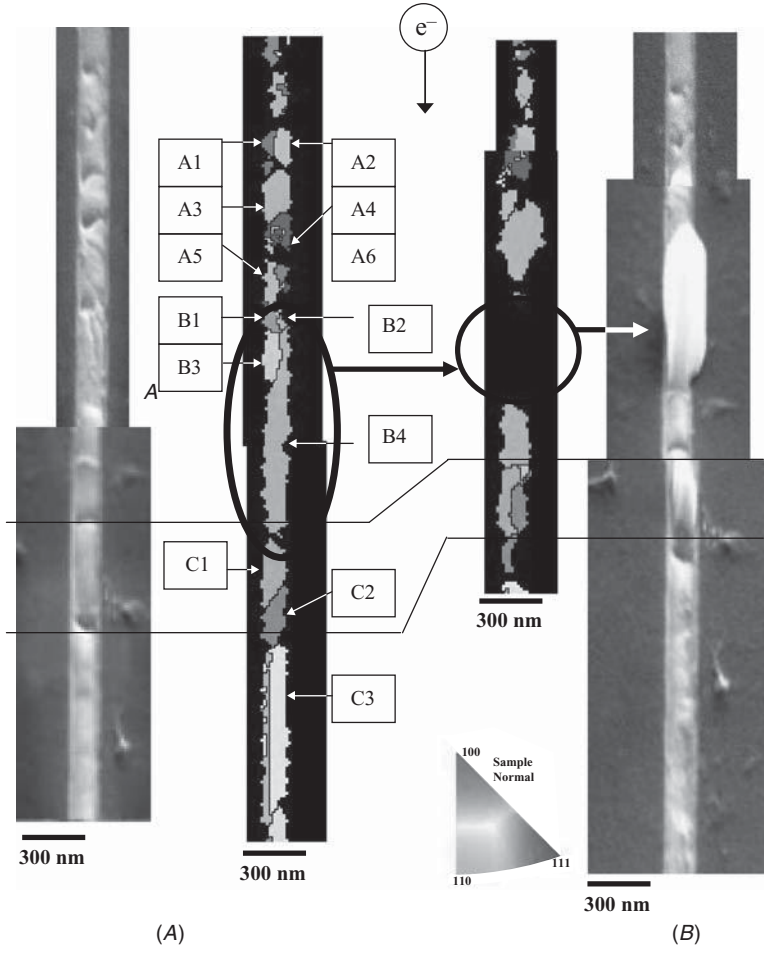


FIGURE 2.9 Orientation contrast maps (*A*) before and (*B*) after the electromigration test on a damascene Cu interconnect line 50 μm long and 200 nm wide computed at the hillock formation site H2 (Fig. 2.6*B*). The SEM images have been depicted for purpose of comparison at 70-degree tilt after applying tilt correction.

2.5.2 Correlating Grain Orientation to Hillocks

Now let us analyze the hillock depicted in Fig. 2.6 as H2. This region comprises three hillocks, H2a, H2b, and H2c. As seen in Fig. 2.6*A*, these hillocks formed in a region where the grooves were already present on the line perpendicular to trench sidewall, prior to the test. The SEM images and orientation maps are shown in Fig. 2.9. The high-angle grain boundaries have been highlighted in black in the maps. The

Hillock	Grain1	Grain2	Misorientation (deg)/Grain Boundary Character
H2A	A1 = (324)[-2-23]	A2 = (415)[26-3]	46
	A1	A3 = (123)[-33-1]	25
	A2	A3	33
	A3	A4 = (223)[3-20]	45
	A5 = (155)[-2-33]	A6 = (015)[-36-1]	Σ3
	A4	A5	39
	A4	A6	50
H2B	B1 = (114)[0-31]	B2 = (235)[10-2-3]	36.5
	B3 = (326)[23-2]	B4 = (329)[-2-11]	57
	B1	B3	Σ3
	B2	B4	Σ3
	B4	C1	50.6
H2C	C1 = (103)[30-1]	C2 = (234)[-320]	Σ3
	C2	C3 = (135)[-3-32]	38.6

Table 2.4 Orientations of the Grains listed in Fig. 2.9 and Misorientation between Them

grains have been named A, B, C, etc. Let us first analyze the largest hillock H2b.

We see that the big hillock was formed on grain B4 with orientation (113)[-2-11]. This grain is surrounded by grains B1, B2, B3, and C1. The misorientation between these grains around the hillock H2b is listed in Table 2.4. We can observe from the table that the misorientation of the boundaries between the grains B1 and B2 is 36.5 degrees and between B3 and B4 is 57 degrees. Moreover, it can be seen from Fig. 2.9*A* that these high-angle grain boundaries are oriented parallel to the direction of the electric current flow in the Cu line, making the line more susceptible to failure. The other remaining boundaries between these grains are Σ3. Again the grain B4 at bottom is surrounded by a high-angle grain boundary of misorientation 50.6 degrees. In a similar test[59] conducted on a different line 150 nm wide and 50 μm long, a thermal hillock had formed on a grain with orientation (113). Thus, once more we observe that the hillock formed on a grain with orientation (113) and again the high-angle grain boundaries were present in this region. We see from Fig. 2.9*B* that part of the grain B4, where the hillock formed after failure, remained dark because of the

surface topography of the hillock making it difficult to index. Among all three hillocks H2a, H2b, and H2c, the hillock H2a is the smallest and formed at the groove located at the high-angle grain boundary between grains A4 and A5 (Fig. 2.9*A*). The formation of hillock H2a through the groove can be clearly visualized in Fig. 2.6*B*. The grains in this region have been named A1, A2, etc., and the misorientation between these grains is listed in Table 2.4. In case of hillock H2a we find that this region is entirely surrounded by high-angle grain boundaries and only one Σ3 boundary. The presence of a high-angle grain boundary cluster again makes this region more susceptible to failure. Grain A4 is of an orientation close to {111}<110>, whereas grain A5 is of an orientation close to {110}<111>. This result shows that during electromigration, in addition to interface diffusion, diffusion through the high-angle grain boundaries is active as well. The intersection of grooved grain boundary and trench sidewall creates a local mass flux divergence and therefore acts as a potential failure site. The formation of hillock H2a also brought all the three grains A1, A2, and A3 in close proximity.

The hillock H2c formed in the region consisting of two grains of orientation C1 and C2 enclosed by the grooves at the top and bottom. As already mentioned, the misorientation between the grains B4 and C1 was 50.6 degrees, whereas that between C2 and C3 was 37.6 degrees. The grooves were located at these high-angle grain boundaries. The C1-C2 shared a common Σ3 CSL boundary. As can be seen from Fig. 2.9*B*, after failure, a part of the (111) grain slid and came to the side of C1, making the Σ3 boundary between them almost parallel to the trench length. Interestingly, the orientation of the grains did not change after formation of the hillock, indicating that the bottom interface diffusion was active and the hillock formed by mass accumulation beneath the grains C1 and C2. Thus, the formation of the smaller hillocks H2a and $H2_C$ is mainly driven by the deep pre-existing grooves/defects on the formed along the high angle grain boundaries.

2.6 Case 2

The next test was performed on a line 130 nm wide and 50 μm long. Figure 2.10*A* shows the SEM image (without tilt correction) of the entire Cu line before failure and Fig. 2.10*B* shows the image after failure. We find that contact opening occurred at the cathode end in the pad region. But besides cathodic failure, we also find that mass accumulation occurred at the anode end, again in the pad region. This type of failure is characteristic of that caused by interface diffusion as reported by other authors[43,44] because we did not observe any other site of mass flux divergence along the line except the hillock. The formation of the hillock might have been caused by grain-boundary

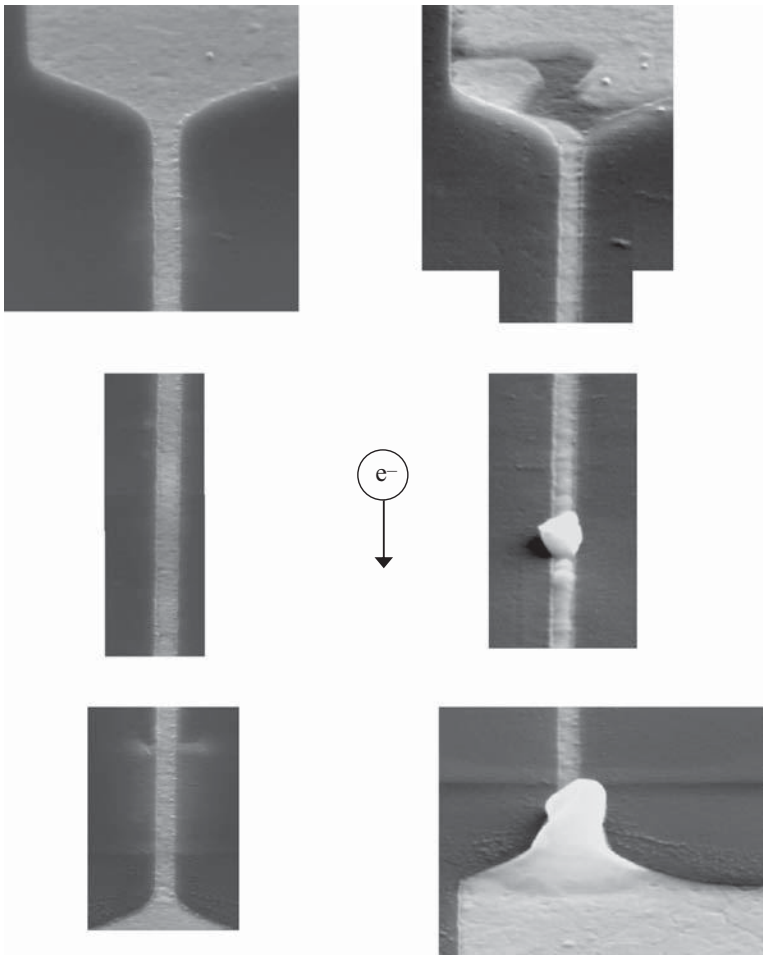


Figure 2.10 SEM images depicting 50 μm long and 130 nm wide damascene Cu interconnect lines (*A*) before and (*B*) after the electromigration failure. The images have been depicted at a 70-degree tilt in the *y* direction without tilt correction.

diffusion; however, it is also possible that bottom-interface diffusion is responsible. This can be ascertained by computing the orientation contrast maps depicted in Fig. 2.11.

Figure 2.11*A* shows the orientation map before failure and Fig. 2.11*B* shows the map after failure at the region of hillock formation. Clearly, we can see that the hillock formed on a grain with orientation (106)[68-1] (grain D). The (106) orientation is close to the (100) orientation. In order to identify the role of microstructure, we have named

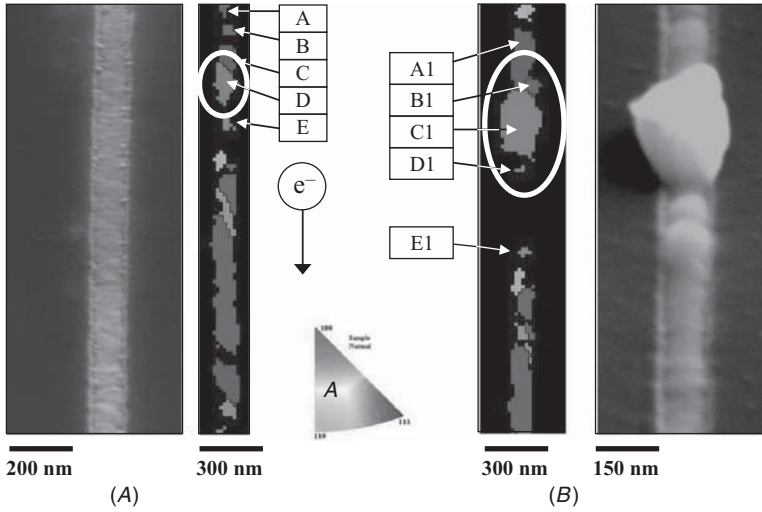


Figure 2.11 Orientation maps computed at the defect region of the hillock depicted in Fig. 2.6 (*A*) before and (*B*) after electromigration tests on a damascene Cu interconnect line 130 nm wide and 50 μm long. The SEM image has been depicted at a 70-degree tilt in the *y* direction without tilt correction.

all the grains including (100) and its immediate neighbor A, B, C, etc., whereas after failure the grains have been named A1, B1, C1, etc. The orientation of each of these grains and misorientation between them is listed in Table 2.5. We can see from Fig. 2.11*A* that grain D is surrounded by high-angle grain boundaries. The orientation of this grain

Grain1	Grain2	Misorientation (deg)/ Boundary Character
A = (223)[1-42]	B = (223)[-302]	33.8
B	C = (111)[5-4-1]	19
C	D = (106)[68-1]	55
D	E = (115)[1-10]	21.3
A1 = (111)[-2-13]	B1 = (223)[1-42]	Σ3
B1	C1 = (100)[012]	48.8
C1	D1 = (106)[68-1]	1.2
D1	E1 = (115)[1-10]	24

Table 2.5 Orientation and Misorientation of Various Grains Listed in Fig. 2.11*A* and *B*

changes after a hillock forms on it. The orientation of the same grain after failure is (100)[012] (grain C1). The change in the orientation of the grain indicates that either or both surface and grain-boundary diffusion is active in these lines. If it had been bottom interface diffusion, the grain would have simply elevated from its position without causing any orientation change.

Thus, we find orientation dependence of hillock formation with preference for (100) grains. The hillock formation occurred because of a flow of matter through either the grain boundaries or the surface.

2.7 Case 3

The third test was carried out on a Cu line that was 20 μm long and 200 nm wide. No hillock was observed, except that the portion of the Cu line in the proximity of the void bulged as a result of uniform mass accumulation. The magnified view of the void is shown in Fig. 2.12*D*. We also observe a curtain-like substance near the void. This is the impurity cloud formed along the line as a result of the carbon contamination caused by the electron beam on the specimen. The formation of the void also led to rupture of the curtain, as can be seen in Fig. 2.12*D*.

Figure 2.12*B* and *C* depicts the orientation contrast maps for the same line before and after the failure respectively. We can see from Fig. 2.12*B* and *C* that the void nucleation again occurred in the vicinity of (111) grains, and these grains once again were surrounded by high-angle grain boundaries having misorientation of 42, 58, and 29 degrees. The Cu line seems to have undergone a great deal of deformation during electromigration, the evidence of which we get from Fig. 2.12*A* and *D*. As a result of this deformation, we see the appearance of some new grains with different orientation (grain A) in Fig. 2.12*C* after the test, which were not observed in Fig. 2.12*B*. In addition, the presence of a thick impurity cloud on the surface made it difficult to obtain EBSD patterns from some regions of the Cu lines. As a consequence, these regions remained unindexed and appear dark on the orientation maps in Fig. 2.12*C*.

2.8 Failure Mechanism

In some Cu lines, the void formation occurred at the cathode end in the form of contact opening, and hillocks formed at the anode end. In some lines, we observed formation of voids but no hillocks. These two types of failure are characteristic of diffusion at a line interface with the barrier layer. The activation energy of interface diffusion is lower

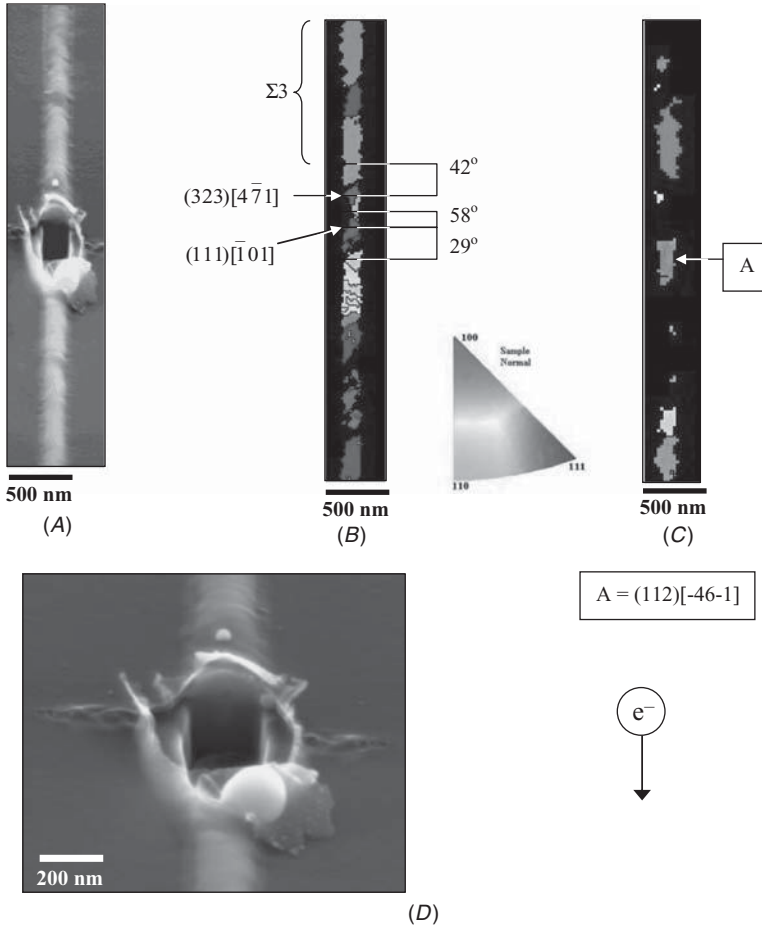


Figure 2.12 (*A*) SEM images and (*B*) orientation contrast map before and (*C*) after the electromigration test computed at the region of void for a damascene Cu interconnect line 20 μm long and 200 nm wide. (*D*) Magnified view of the void shadowed by the curtain of impurities.

than that of grain-boundary or bulk diffusion in Cu interconnects. As a consequence, the interface diffusion is most active in the damascene Cu interconnects. The chronology of events occurring during the process of electromigration can now be described in the following way. As the electromigration begins, the matter begins to flow toward the anode through the interfaces, resulting in formation of voids in the cathode region. If on its way matter encounters effective local flux divergence sites, such as grooves on grain boundaries or high-angle boundaries intersecting the trench sidewall or preexisting structural

defects such as voids, then matter starts accumulating there and could form a hillock. Thus, anything that resists or diverts the flow of matter during electromigration will lead to mass accumulation in the form of hillocks.

If there are no local mass flux divergence sites along the line, then the matter would simply flow toward the anode and be deposited in the form of hillocks. In cases where the hillocks do not form, the matter is simply deposited along the interfaces in the anode region. This gives rise to a buildup of compressive stresses in the anode region. As the electromigration progresses, there is further resistance to flow of matter toward the anode. As a result, the matter tries to flow through other paths with lower resistance, such as high-angle grain boundaries, giving rise to formation of a hillock.

Our results show that void formation occurred near (111) grains, whereas hillocks formed on grains with orientation (100) and (113), irrespective of the line width or line length. The mechanism governing the preference of selective orientations for electromigration defect formation can be explained as follows.

2.8.1 Thermal Diffusion

Before carrying out the electromigration tests the Cu lines were heated to a temperature of 250°C. Though there was no passivation layer present, the Cu lines were under compression at 250°C as the dielectric sidewall resists Cu expansion at higher temperatures. The compression will lead to straining of different grains. Because the elastic modulus of the (100) grains is the lowest, these grains in the Cu damascene lines will be under maximum strain at high temperature. Contrary to this, the (111) grains will be under minimum strain because of their high elastic modulus. At a temperature of 250°C, thermal diffusion of Cu atoms will be active. The diffusion would occur from a region where there is higher concentration of atoms per unit volume to a region with a lower concentration of atoms. The large strain of the (100) grains decreases the interplanar spacing between the (100) planes and increases the number of atoms per unit volume. As a consequence, stress-induced diffusion would begin from the (100) grains in the direction of the Cu lines as depicted by horizontal arrows in Fig. 2.13*A*. The diffusion occurring from the (111) grains of the Cu line will be minimal and hence the (111) grains will act as a sink for thermally diffused atoms. As depicted in Fig. 2.13, the active diffusion pathway will be the interfaces between the Cu and the barrier layer. At any given time there will higher mass concentration near the (100) grains since these grains will be emitting Cu atoms (Fig. 2.13*A*). There will be gradient in the mass flow with minimum concentration near the (111) grains.

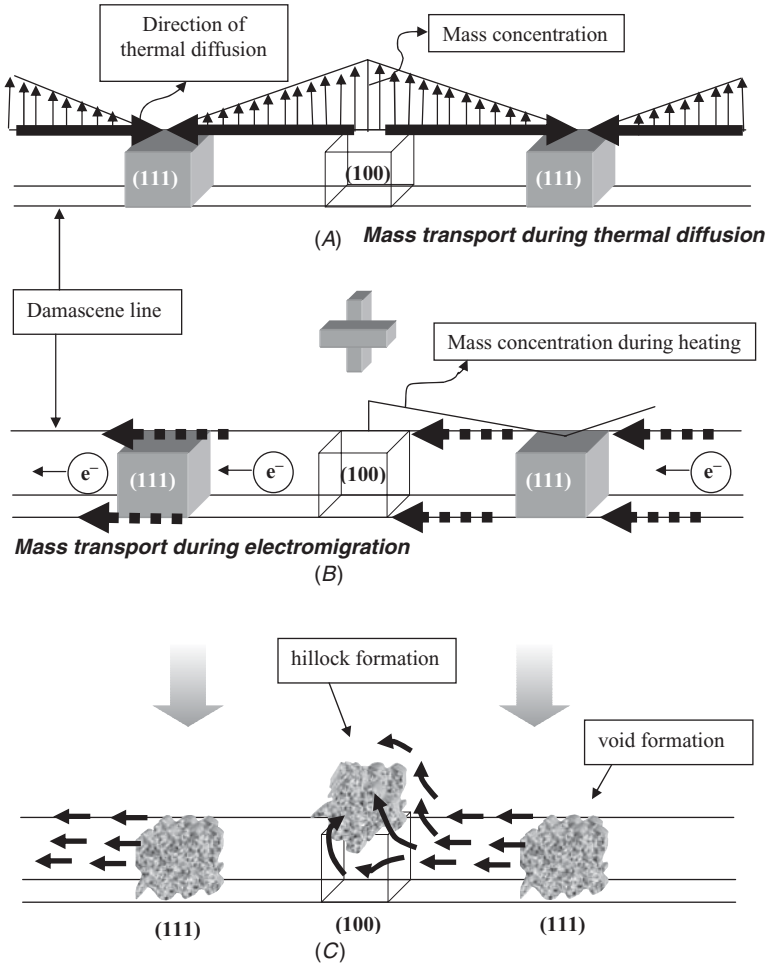


Figure 2.13 Schematic representation of (*A*) thermal diffusion of atoms occurring from (100) grains through interfaces in absence of electromigration and (*B*) diffusion of Cu atoms through interfaces during electromigration. (*C*) The thermal and electromigration diffusion add up, producing voids near (111) grains and hillocks on (100) grains.

2.8.2 Coupling of Thermal and Electromigration-Induced Mass Diffusion

During electromigration, mass transport will occur mainly through the interfaces between the Cu line and the barrier layer (Fig. 2.13*B*). The mass transport occurring as a result of thermal diffusion and electromigration will add up when the electromigration begins. Because there is already a higher concentration of mass in the interfaces

near the (100) grains, it is difficult to erode the mass from these grains during electromigration. Because the mass concentration near the (111) grains is the lowest at any given time, the mass depletion occurring due to electromigration is easiest near the (111) grains. As a consequence, the void nucleation would occur in the vicinity of (111) grains as illustrated in Fig. 2.13*C*. The most vulnerable region for void nucleation would be the intersection of a high-angle grain boundary with the trench sidewall. However, even if the (111) grain is not surrounded by high-angle grain boundaries or has twin boundaries at its border, void formation would easily occur. This is because the void will form at the interfaces of the (111) grains with the barrier layer. Evidence of mass depletion having occurred at the interface between the (111) grain and barrier layer can be clearly seen in Figs. 2.7 and 2.8. Some of these (111) grains were not surrounded by high-angle grain boundaries.

The mass will be transported during electromigration from the (111) grains in the direction of the current flow along the Cu line as shown by arrows in Fig. 2.13*B*. But there will be some resistance to flow of the matter as it approaches the (100) grains, because there is already a high concentration of matter in the interfaces near the (100) grains due to thermal diffusion. But as the electromigration progresses, more and more mass will accumulate near the (100) grains as a result of coupling of thermal diffusion and electromigration-driven mass. This will finally lead to hillock formation on (100) grains or any other orientations that are close to (100). If the (100) grain is surrounded by high-angle boundaries, there will also be diffusion of matter through the grain boundary, leading to hillock formation on (100) grains. In fact, in all cases we observe that hillock formation occurred on the grains that were surrounded by high-angle grain boundaries. The same explanation applies to hillock formation on the (113) orientation. The elastic moduli of Cu along the <113> directions also has a low value of about 100 GPa, and hence the (113) crystals will also be considerably strained at high temperature and emit Cu atoms by thermal diffusion.

Thus, our results show that all the orientations with lower elastic moduli, such as (100) and (113), especially those surrounded by high-angle grain boundaries, will be more prone to hillock formation, whereas orientations with higher elastic moduli such as (111) will have a tendency to form voids. Thus, orientations that have elastic moduli lying at the very high and low ends of the modulus spectrum seem to be detrimental for both electrical and mechanical reliability of Cu interconnects—(111), (100), and (113) orientations are just a few examples of these. Even other authors[60] have observed electromigration defects to be occurring near the (111) and (100) grains. A separate study carried out by Choi et al.[61] shows association of (111) grains with voids, though the authors do not specifically mention it.

Several other authors[62,63] have associated (111) and (100) orientations with other specific characteristics such as poor oxidation resistance. A lower degradation can be expected if the grain orientations along the damascene Cu line do not deviate much from each other—or, in other words, a very strong texture should be beneficial because it will reduce the gradients in thermal diffusion along the copper line. A random texture where there is equal possibility of finding grains with any orientation will have a detrimental effect on electromigration. In fact, some recent articles do report superior electromigration performance with strong (111) texture.[64]

References

1. H. J. Bunge, *Texture Analysis in Materials Science*, 2nd ed., Cuvillier Verlag, Gottingen, Germany, 1982.
2. V. Randle, *Microtexture Determination and Its Applications.*
3. V. Randle and O. Engler, *Introduction to Texture Analysis: Macrotexture, Microtexture, and Orientation Mapping*, 2nd ed.
4. F. d'Heurle and I. Ames, "Electromigration in single-crystal aluminum films," *Applied Physics Letters*, vol. 16, p. 80, 1970.
5. Y. C. Joo and C. V. Thompson, *Materials Reliability in Microelectronics IV, Materials Research Society Symposium*, p. 319, 1994.
6. Y. C. Joo, C. V. Thompson, S. P. Baker, and E. Arzt, "Electromigration proximity effects of two neighboring fast-diffusion segments in single-crystal aluminum lines," *Journal of Applied Physics*, vol. 85, p. 2108, 1999.
7. W. Baerg and K. Wu, *Solid State Technology*, p. 35, March 1991.
8. J. Cho and C. V. Thompson, "Grain size dependence of electromigration induced failures in narrow interconnects," *Applied Physics Letters*, vol. 54(25), p. 2577, 1989.
9. M. J. Attardo and R. Rosenberg, "Electromigration damage in aluminum film conductors," *Journal of Applied Physics*, vol. 41, p. 2381, 1970.
10. T. Muppidi, Y. Kusama, and D. P. Field, *Materials Research Society Symposium Proceedings*, vol. 721, p. 123, 2002.
11. J. K. Howard and R. F. Ross, "The effect of preferred orientation on the rate of electromigration and its implication to the cracked-stripe failure mode," *IBM Technological Reports*, vol. 22, p. 601, March 1968.
12. A. N. Campbell, R. E. Mikawa, and D. B. Knorr, "Relationship between texture and electromigration lifetime in sputtered AI-1% Si thin films," *Journal of Electronic Materials*, vol. 22, no. 6, p. 589, 1993.
13. S. Vaidya, D. B. Fraser, and A. K. Sinha, *Proceedings of the Eighteenth Annual Reliability Physics Symposium*, p. 165, 1980. IEEE.
14. D. P. Field and P. H. Wang, "Development of a preferred grain boundary structure in Al-Cu interconnects," in *Boundaries and Interfaces in Materials: David A. Smith Symposium, The Minerals, Metals and Materials Society*, p. 323, 1998.
15. F. M. d'Heurle, "The effect of copper additions on electromigration in aluminum thin films," *Metallurgical Transactions*, vol. 2, p. 683, 1971.
16. A. Gangulee and F. M. d'Heurle, "The effect of alloy additions on electromigration failure in thin aluminum films," *Applied Physics Letters*, vol. 19(3), p. 76, 1971.
17. F. M. d'Heurle and A. Gangulee, "Effects of complex alloy additions on electromigration in aluminum thin films," in *Proceedings of the International Reliability Physics Symposium*, p. 165, 1972.
18. B. Dance, *Semiconductor International*, p. 66, September 1995.
19. P. B. Ghate and J. C. Blair, "Electromigration testing of Ti: W/Al and Ti: W/Al-Cu film conductors," *Thin Solid Films*, vol. 55(113), p. 113, 1978.

20. H. H. Hoang and J. M. McDavid, "Electromigration in multilayer metallization systems," *Solid State Technology*, p. 121, October 1987.
21. N. P. Armstrong, *Quality Reliability Engineering International*, vol. 7(4), p. 281, 1991.
22. O. J. Olowwolafe, C. Lee, H. Kawasaki, C. Gelator, R. Blumental, N. D. Theordore, et al., "Effect in TiN anneal ambient on the microstructure and electromigration performance of Al-based alloys," in *Proceedings of the Materials Research Society*, p. 95, 1993.
23. T. Kikkawa, N. Endo, T. Yamazaki, and H. Watanabe, "Comparison of refractory metal and silicide capping effects on aluminum metallizations," in *Proceedings of the IEEE VLSI/ULSI Multilevel Interconnection Conference (VMIC)*, p. 463, 1989.
24. J. K. Howard, J. F. White, and P. S. Ho, "Intermetallic compounds of Al and transitions metals: Effect of electromigration in 1-2-μm-wide lines," *Journal of Applied Physics*, vol. 49(7), p. 4083, 1978.
25. A. Gangulee, P. S. Ho, and J. K. Howard, "Electromigration resistance in gold thin film conductors," U.S. Patent No. 4,166,279, 1979.
26. C. Ryu, K. W. Kwon, L. S. Loke, H. Lee, T. Nogami, V. M. Dubin, et al., "Microstructure and reliability of copper interconnects," *IEEE Transactions on Electron Devices*, vol. 40, p. 1113, 1999.
27. J. R. Lloyd, J. Clemens, and R. Snede, "Copper metallization reliability," *Microelectronics Reliability*, vol. 39, p. 1595, 1999.
28. L. Vanasupa, Y. C. Joo, P. R. Besser, and S. Pramanick, *Journal of Applied Physics*, vol. 85(5), p. 2583, 1999.
29. L. Arnaud, R. Gonella, G. Tartavel, J. Torres, C. Gounelle, Y. Gobil, and Y. Morand, "Electromigration failure modes in damascene copper interconnects," *Microelectronics Reliability*, vol. 38, p. 1029, 1998.
30. L. Arnaud, T. Berger, and G. Reimbold, "Evidence of grain-boundary versus interface diffusion in electromigration experiments in copper damascene interconnects," J*ournal of Applied Physics*, vol. 93(1), p. 192, 2003.
31. T. Berger, L. Arnaud, R. Gonella, G. Lormand, and Y. Morand, "Electromigration characterization of damascene copper interconnects using normally and highly accelerated tests," *Microelectronics Reliability*, vol. 40, p. 1311, 2000.
32. A. Gladkikh, M. Karpovski, A. Palevski, and Yu. S. Kaganovskii, "Effect of microstructure on electromigration kinetics in Cu lines," *Journal of Physics D—Applied Physics*, vol. 31(14), p. 1626, 1998.
33. A. Gladkikh, M. Karpovski, and A. Palevski, "Microstructural and surface effects on electromigration failure mechanism in Cu interconnects," *Microelectronics Reliability*, vol. 37(10-11), p. 1557, 1997.
34. N. D. McCusker, H. S. Gamble, and B. M. Armstrong, "Surface electromigration in copper interconnects," *Microelectronics Reliability*, vol. 40, p. 69, 2000.
35. N. Schwartz, *Transactions of the Tenth National Vacuum Symposium*, p. 325, 1964.
36. R. Carel, C. V. Thompson, and H. J. Frost, "Computer simulation of strain energy effects vs surface and interface energy effects on grain growth in thin films," *Acta Materialia*, vol. 44(6), p. 2479, 1996.
37. C. Lingk, M. E. Gross, and W. L. Brown, "Texture development of blanket electroplated copper films," *Journal of Applied Physics*, vol. 87(5), p. 2232, 2000.
38. S. P. Hau-Riege and C. V. Thompson, "In-situ transmission electron microscope studies of the kinetics of abnormal grain growth in electroplated copper films," *Applied Physics Letters*, vol. 76(3), p. 309.
39. K. Mirpuri and J. Szpunar, "Impact of annealing, surface/strain energy and linewidth to line spacing ratio on texture evolution in damascene Cu interconnects," *Micron*, vol. 35(7), p. 575, 2004.
40. J. R. Lloyd, "Electromigration and mechanical stress," *Microelectronic Engineering*, vol. 49, p. 51, 1999.
41. J. M. Steigerwald, S. P. Murarka, R. J. Gutmann, and D. J. Duquette, *Materials Chemistry and Physics*, vol. 41, p. 217, 1995.
42. J. Proost, T. Hirato, T. Furuhara, K. Maex, and J. -P. Celis, *Journal of Applied Physics*, vol. 87(6), p. 2792, 2000.

43. N. L. Michael, C. Kim, P. Gillespie, and R. Augur, "Electromigration failure in ultra-fine copper interconnects," *Journal of Electronic Materials*, vol. 32(10), p. 988, 2003.
44. N. L. Michael, C. Kim, Q. T. Jiang, R. Augur, and P. Gillespie, "Mechanism of electromigration failure in submicron Cu interconnects," *Journal of Electronic Materials*, vol. 31(10), p. 1004, 2002.
45. D. B. Knorr and K. P. Rodbell, *Materials Research Society Symposium Proceedings*, vol. 309, p. 345, 1993.
46. D. B. Knorr and K. P. Rodbell, *Journal of Applied Physics*, vol. 79, p. 2409, 1996.
47. J. L. Hurd, K. P. Rodbell, D. B. Knorr, and N. L. Koligman, "Local texture and electromigration in fine line microelectronic aluminum metallization," *Materials Research Society Symposium Proceedings*, vol. 343, p. 653, 1994.
48. D. B. Knorr and D. P. Tracy, "Textures of aluminum and copper thin films," *Materials Science Forum*, vol. 157-162, p. 1443, 1994.
49. R. Rosenberg, D. C. Edelstein, C. K. Hu, and K. P. Rodbell, "Copper metallization for high performance silicon technology," *Annual Reviews in Materials Science*, vol. 30, p. 229, 2000.
50. R. R. Keller and J. A. Nucci, "Effects of local crystallography on stress-induced voiding in passivated copper interconnects," *Electron Crystallography*, p. 379, 1997.
51. R. R. Keller, J. A. Nucci, and D. P. Field, "Local textures and grain boundaries in voided copper interconnects," *Journal of Electronic Materials*, vol. 26(9), p. 996, 1997.
52. J. A. Nucci, R. R. Keller, D. P. Field, and Y. Shacham-Diamand, "Grain boundary misorientation angles and stress-induced voiding in oxide passivated copper interconnects," *Applied Physics Letters*, vol. 70(10), p. 1242, 1997.
53. A. Sekiguchi, J. Koike, S. Kamiya, M. Saka, and K. Maruyama, "Void formation by thermal stress concentration at twin interfaces in Cu thin films," *Applied Physics Letters*, vol. 79/9, p. 1264, 2001.
54. O. Kraft and E. Arzt, "Current density and line width effects in electromigration: a new damage-based life time model," *Acta Materialia*, vol. 46, p. 3733, 1998.
55. A. F. Mayadas and M. Shatzkes, "Electrical-resistivity model for polycrystalline films: the case of arbitrary reflection at external surfaces," *Physical Reviews*, vol. B1, p. 1382, 1970.
56. K. T. Lee, J. A. Szpunar, and D. B. Knorr, *Materials Science Forum*, vol. 204-206, p. 423, 1996.
57. T. G. Koetter, Ph.D. thesis, Technical University of Dresden, Germany, 2002.
58. CHANNEL 5, HKL Technology, Denmark, 1990.
59. Kabir Mirpuri, "Stress, texture and electromigration in damascene Cu interconnects," PhD Thesis, McGill University, Canada, 2005.
60. S. Brongersma, E. Kerr, I. Vervoort, and K. Maex, "Limitations to copper grain growth in narrow trenches," *Proceedings of the IEEE International Interconnect Technology Conference*, p. 230, 2001.
61. Z.-S. Choi, R. Monig, and C. V. Thompson, "Effects of microstructure on the formation, shape, and motion of voids during electromigration in passivated copper interconnects," *Journal of Materials Research*, vol. 23(2), pp. 383-391, 2008.
62. A. H. Fischer, A. von Glasow, A. Huot, and R. A. Schwarzer, *Conference Proceedings, ULSI XV*, p. 137, 2000. Materials Research Society.
63. L. Carbonell, P. Ratchev, R. Caluwaerts, M. Van Hove, B. Verlinden, and K. Maex, "Dry oxidation mechanisms of copper in trenches," *Microelectronic Engineering*, vol. 64(1-4), p. 63, 2002.
64. X. Wang, X. Dong, and J. Wu, "Effects of Cr dopant on the microstructure and electromigration performance of Cu interconnects," *Applied Surface Science*, vol. 255(22), pp. 9273-9278, 2009.

CHAPTER 3

Carbon Nanotube Interconnects in CMOS Integrated Circuits

Gael Close

3.1 Introduction

The performances of integrated circuits have been steadily improved over the past few decades through miniaturization of the transistors and interconnect wires. In addition to shrinking the building blocks, new materials have been progressively introduced in the manufacture of integrated circuits to further improve their performances. Maintaining this trend of higher-performance integrated circuits into the future will increasingly require the use of materials at the nanoscale.[1] Because of their excellent electrical properties, metallic carbon nanotubes (CNTs) are promising materials for interconnect wires in future integrated circuits. Simulations have shown that the use of metallic CNT interconnects could yield more energy-efficient and faster integrated circuits. The next step is to build an experimental prototype integrated circuit using CNT interconnects operating at high speed.

The most advanced integrated circuits consist of several million (sometimes several billion) transistors, interconnected by kilometers of copper wires within a 1-cm^2 silicon chip. The number of transistors integrated on a single chip is predicted to increase even further,[2] requiring even smaller transistors and narrower copper wires in the future. However, scaling degrades the performances of interconnects in terms of delay, signal integrity, and reliability. Interconnects are therefore viewed as major limiters in the race to further miniaturization.[3]

Interconnect wires are already important factors of current integrated circuits in terms of masking levels, power, performance, and reliability. This "tyranny of interconnect"[4] requires the exploration of new materials to serve as interconnect in future silicon chips.

This chapter focuses on local wires—the ones closer to the transistors. They are aggressively shrunk from one generation to the next to keep up with the miniaturization of the transistors and sustain the density increase. These local wires are hence routed with the minimum pitch allowed in the technology. Currently, the narrowest local wires are about 50 nm wide, and they are expected to scale down with transistor size.[2] As copper wires are scaled to narrower dimensions to keep up with miniaturization of the transistors, they face two critical issues. First, their electrical resistivity degrades because of increasing electron scattering by the grain boundaries and the wire surface.[5,6] Simulations have shown that this fundamental increase of copper resistivity for the narrow wires will ultimately deteriorate the system-level performances of the chips.[7] Second, the reliability of narrow copper wires is becoming a growing concern because of the increasing current density (>2 MA/cm^2) that they need to withstand.[8] A quest for alternative interconnect materials engineered at the nanoscale has thus been initiated to solve these two problems.[9]

Because of their nanoscale size and outstanding intrinsic electronic properties, CNTs are promising materials for future nanoelectronics. Semiconducting CNTs are already being researched as the electron channel for nanotransistors.[10,11] Similarly, metallic CNTs have been proposed as effective wires[12–14] for interconnecting transistors. Metallic CNTs are attractive interconnect materials because they address, in principle, the two problems faced by copper wires. First, because of their 1D nature, electrons can travel much farther than in copper without scattering.[15] Second, they can withstand current density greatly exceeding the limit of copper.[16] Another advantage of metallic CNTs as interconnect materials is that they are scalable all the way down to the 1-nm regime.[14] As a result of these attractive attributes, CNTs are actively researched as future interconnect materials in vertical vias[17,18] and horizontal interconnects. Simulations have clearly shown the potential of CNTs as interconnect materials.[19,20]

In this chapter, we first review the copper interconnect scaling trends, justifying the needs for the exploration of new interconnect materials and establishing the motivations for CNT interconnects. We then present the fabrication of the first stand-alone integrated circuit combining silicon transistors and individual CNT interconnect wires on the same chip operating above 1 GHz. In addition to setting a milestone by operating above 1 GHz, this prototype is also a tool to investigate CNTs on a silicon-based platform at high frequencies.

3.2 Trends in Interconnect Scaling

3.2.1 Importance of Interconnects

Modern chips contain miles of copper interconnect wires arranged in up to 10 levels of metal.[2] The number of interconnect wires will grow exponentially[2] as technology advances according to Moore's law. The capacitance associated with the wiring is typically responsible for about 50 percent of the total dynamic power consumption in a low-power microprocessor.[21] The interconnect power consumption is about equally divided between relatively few global wires routing signals across the chip, and local wires, where the total power is the sum of a great number of short wires.

On top of their large impact on power, interconnects have also a major impact on speed and chip architecture. This is especially true for the long global wires whose delays scale upward relatively with gate delay as technology advances.[22] The increasing delay for communication across the chip is another incentive for moving toward multicore architectures, in which communication latency can be accommodated explicitly at the architectural level. Recently, the short local wires have also started to affect the speed, whereas their delay used to be insignificant compared to the gate delay. This is a consequence of the trend toward low-power design where transistors are sized as small as possible to minimize power, thereby magnifying the delay impact of the short wires.

All in all, as we move toward nanoelectronics, the impact of interconnects on system-level performance is increasingly pervasive, in terms of power, delay, architecture, and masking levels. As Prof. J. Meindl of Georgia Tech put it[4]: "This 'tyranny of interconnectors' will only escalate in the future, and thus the nanoelectronics that follow silicon must be interconnect-centric."

3.2.2 Scaling Trends and Challenges

To keep up with transistor miniaturization, interconnect scaling follows closely transistor scaling (see Table 3.1). The local wires ("metal 1" or "M1"), those closest to the transistors, are typically routed with the same pitch as the transistor gate pitch.

Scaling, in principle, improves transistor performance metrics. In contrast, scaling down interconnect dimensions does not improve interconnect performances, fueling the growing interconnect concern. As all the wire dimensions are scaled down by a factor $k > 1$, the resistance per length r increases as k^2, reflecting the smaller wire cross section. On the other hand, the capacitance per length c remains constant. The RC delay of a scaled local wire (whose length L is scaled

Year	2007	2010	2013	2016	2018
Node [DRAM ½ M1 Pitch (nm)]	65	45	32	22	18
Levels	11	12	13	13	14
M1 pitch (nm)	136	90	64	44	36
M1 aspect ratio	1.7	1.8	1.9	2	2
Resistivity ($\mu\Omega$-cm) M1	3.5	4.1	4.8	6	6.7
Dielectric constant k	2.9	2.6	2.4	2.1	2.0
RC delay (ps) for 1-mm M1 wire	890	2,100	4,500	10,600	17,000
Jmax (MA/cm^2) wires	1.0	1.7	2.2	3.1	3.2

Table 3.1 Interconnect Scaling Projections According to the International Technology Roadmap for Semiconductors (ITRS)[2]

down by k) is then approximately constant (= rcL^2). As the intrinsic transistor delay decreases with scaling, the local wire *RC* delay becomes increasingly dominant on a relative scale. This trend is even more severe for global interconnect wires, which do not scale in length. In addition, the interconnect reliability is also degraded as the current density increases as k.

Local and Global Wires

The complexity of the interconnect network in chips is typically addressed through a hierarchy of interconnect levels[22] as shown in Fig. 3.1. At the lower level of this hierarchy, there are the short wires connecting nearby logic gates. These local wires are routed with the tightest pitch and highest density. For a local wire, the wire capacitance rather than its resistance has the most effect on circuit behavior, because the wire resistance is dominated by the driving transistor resistance. At the other end of the interconnect hierarchy, the global wires communicate signals across the chip, and hence, their length does not scale, resulting in a larger latency relatively to the transistor delay. They are made of thicker copper to minimize resistance and are routed with larger pitch to minimize capacitance. Both the resistance and capacitance of global wires are of importance, as they typically operate in the distributed *RC* regime in which the delay grows as the square of the length (they can also operate in the *RLC*, regime where the signal propagates at the speed of light under optimal conditions).

To address the rising latency of global interconnects, there are more degrees of freedom than simply the material and the geometry making up the wire. The signaling media can be changed to speed up the link: optical and *radiofrequency* (RF) signal transmissions are indeed being

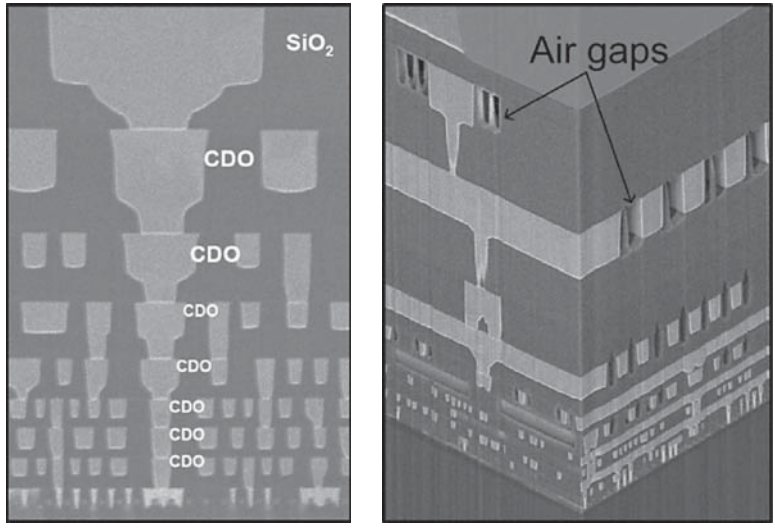


Figure 3.1 State-of-the-art copper low-*k* interconnect technologies. (*A*) Cross-section *scanning electron micrograph* (SEM) of eight of nine Cu interconnect layers in Intel 45-nm chips.[23] The wires are embedded in a low-*k* ($k = 2.8$) *carbon-doped oxide* (CDO) dielectric. The wires in the topmost Cu layer, which are not shown, are used for power distribution and are much wider than the regular wires (topmost wire pitch = 30 mm). (*B*) Bird's-eye view of the interconnect stack in an IBM prototype processor.[24] The wires are surrounded by air gaps, the ultimate low-*k* dielectric, resulting in an ultralow dielectric constant $k = 1.9$.

investigated as global interconnect scheme. For local interconnects, on the other hand, the circuit overhead of changing the signaling media cannot be tolerated. Therefore, for local interconnects, the wire material, the dielectric material, and the geometry are the only degrees of freedom to optimize the interconnect performances. That is why innovative materials are expected to have a greater impact for local interconnects than for global interconnects. Global interconnects are beyond the scope of this chapter. Instead, we focus on local interconnects.

Narrow-Width Effects

Narrow interconnect copper wires face two major problems highlighted by the ITRS.[2] First, the copper resistivity rises dramatically from its bulk value as the width of the wire is reduced in the nanoscale regime. This is due to the increased surface and grain boundary electron scattering.[5,6] An additional factor degrading the resistivity stems from the necessary presence of a diffusion barrier, also known as the liner, enclosing the copper wire to prevent diffusion of copper atoms

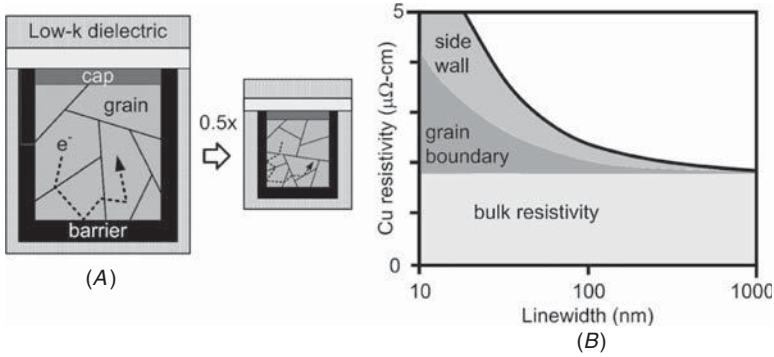


Figure 3.2 Scattering and resistivity in narrow copper lines. (*A*) Grain boundary scattering and surface scattering increase in narrow copper lines. (*B*) Both these factors contribute to an increased in resistivity in narrow copper lines.[2]

into the dielectric. The liner cannot be scaled down as aggressively as the wire width, as there is a minimum thickness required for the liner to act as an effective diffusion barrier. Therefore, the liner tends to occupy an increasing fraction of the cross section, and hence, degrades the effective resistivity because the liner are more resistive than copper. Figure 3.2 illustrates the increased scattering and resulting resistivity in narrow copper wires. Recall that scaled wires are scaled in all three dimensions by the same factor $k > 1$. That is, they become narrower with a constant aspect ratio, and they are also proportionally shortened. The resistivity increase results in a resistance per length which is increasing faster than k^2, causing the scaled wire delay to increase, although this can be compensated to some extent by the use of low-k dielectric.[25,26] This in turn mitigates the speed improvement expected from scaling.

The second problem faced by reduced-size copper wires is the increasing current density. The current density increases because the current is decreased more slowly than the wire cross section.[8] The increase in current density, coupled with the increase in resistivity and in the number of interconnect levels, cause the interconnect temperature to rise, thereby compromising the interconnect electromigration reliability.[20,27]

Impact of Narrow-Width Effects

In this section, we review the system-level impact of the narrow-width effects in copper interconnects. The rising resistivity in narrow wires affects mostly local wires. These narrow local wires are typically so short that their impact on the chip speed is inconsequential, provided that the interconnect hierarchy is optimized, even though the resistivity of the narrowest copper wires will be four times larger than that of bulk copper at the 18-nm node. This is because speed-critical signals

can always be routed with thicker wires and wider pitch using the upper levels of the interconnect hierarchy, which are hardly affected by the resistivity increase. However, to fully assess the implications of the narrow-width resistivity increase, it is necessary to include speed, power, and area into a true system-level analysis. Such analysis reveals that although the impact of narrow-width effects is only minor for high-performance chips, the impact on low-power chips is far greater.[7] For a given chip performance target (e.g., 1 GHz) and fixed number of interconnect levels (e.g., 12), a 22-nm low-power logic chip requires 30 percent larger die area to accommodate the larger wires compensating for the resistivity increase.[7] This area penalty induced by the rising resistivity is exacerbated by a 7 percent increase in power consumption.

The rising resistivity also affects the variability of interconnect delay. The exponential increase in resistivity at narrow width creates a hypersensitivity of the wire resistance with respect to the geometry. In others words, the impact of any variation in the wire width or height (e.g., line edge roughness or *chemical mechanical polishing* [CMP] nonuniformity) leads to a magnified variation in the wire resistance, and hence, in the delay. Simulations have revealed that the delay variability will double because of rising resistivity at the 32-nm node[28] compared to the 45-nm node. Multicore architectures should partly alleviate this problem thanks to their inherent short wires.[29]

3.2.3 Industry Solution

Chip makers are well aware of the problems associated with narrow copper wires. Many material innovations have been implemented recently to address them. Figure 3.3 illustrates some of these innovations.

To compensate for the resistance increase, insulating materials with lower and lower dielectric constants are being used[30] to reduce the capacitance. Thinner and higher-conductivity diffusion barriers are also being developed to minimize their adverse impact on the copper wire effective resistivity[30] Continued improvements in copper plating chemistry and annealing conditions, as well as optimization of the barrier and copper seed quality, will help "contain the finite size effects in copper lines"[31] by increasing the grain sizes and hence, reducing the impact of grain scattering. However, the scattering at the interface appears to be a more fundamental limit, which will invariably degrade the copper interconnect resistivity as its width is reduced deep in the nanoscale regime.

Metal capping of the copper lines[32] will also push the electromigration limit of copper lines even further. Electromigration might not even be an important failure mechanism in short interconnects (shorter than the *Blech length*[33]). The electromigration flow of copper atoms in the direction of the electronic current creates a stress buildup

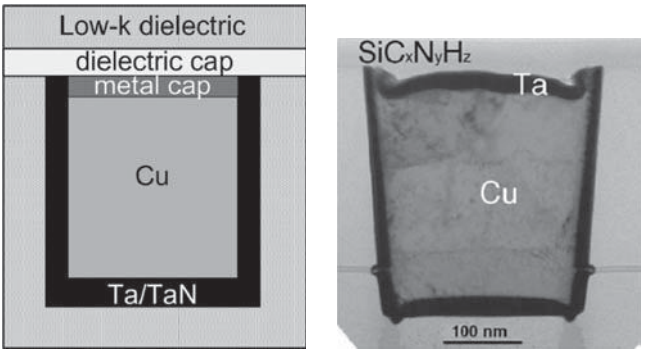


Figure 3.3 Industry solutions to interconnect challenges. To mitigate the negative effects of rising resistivity and current density, new materials are increasingly included in the back end. (*A*) Diagram of a typical modern copper wire, embedded in a low-*k* dielectric (typically, a derivative of a porous silicon oxide) and encapsulated with an ultrathin liner barrier (typically, Ta/TaN), a metal cap (typically, Ta or CoWP), and a low-*k* dielectric cap (typically, a low-*k* derivative of silicon nitride) acting as an etch-stop layer. (*B*) Corresponding cross-sectional *transmission electron micrograph* (TEM) of a copper wire capped with Ta and amorphous SiCHN.[32]

at both ends of the wire: there is an accumulation of copper atoms at one end, and conversely a shortage of copper atoms at the other end. There is then a stress gradient along the wire, which tends to move copper atoms in the direction opposite to the electromigration. In short wires, this stress gradient is strong enough to counterbalance the electromigration flow, and hence, short wires are more immune to electromigration than longer ones.

Continued scaling of copper wires using the dual damascene process[34] will continue to serve the semiconductor industry, despite the increase in resistivity in narrow copper wires in the short term. Architecture changes favoring multicores and decentralized computing units will also ease the problem,[35] but physical limits are being reached. Beyond the horizons of the ITRS road map, solutions to the fundamental issue of resistivity rise will have to be found. Hence, there is a need to explore other options in nanoscale interconnect materials, which could potentially yield lower resistivity in the nanoscale regime.[9]

3.2.4 Alternative Local Interconnect Materials beyond Copper

Just as copper wires were introduced to overcome the limitations of aluminum wires in the 1990s, there is now a pressing need to explore

alternative materials beyond copper. New nanostructured materials could potentially alleviate problems associated with narrow copper wires. Nanostructured materials offer the promise of withstanding high current density with a low resistivity at the nanoscale and are therefore promising options as interconnect materials.

Metallic single-wall or multiwall CNTs have been proposed as nanoscale interconnects.[12,13] Their quasi-1D structure limits the electron scattering, thereby yielding long electron mean free paths, and hence low resistivity, even in the nanoscale regime. The strength of the carbon-carbon bond and the single-molecule structure result in unmatched long-term current carrying capability, on the order of 10^9 A/cm^2. For example, in Ref. 16, the measured resistivity was around 5 $\mu\Omega$-cm, and current density in excess of 10^9 A/cm^2 (over a 2-week period at 250°C) were demonstrated. The ability of CNTs to withstand such high current densities means that their introduction as interconnect materials is restricted by their resistance and integration issues, but not by electromigration concerns.

The demonstrated conductivity and current capability within a nanoscale cross section makes metallic CNT a promising material for true nanoscale interconnects. Computer simulations suggest that it will become increasingly advantageous—in terms of the power/speed/crosstalk trade-off and reliability—to use CNTs for the interconnect wires in future chips, as wire cross sections keep being reduced. In the next section, we review CNT interconnects in more detail.

3.3 Carbon Nanotube Interconnects

A CNT is essentially a hollow tube of pure carbon atoms with a typical diameter around 1 nm. The carbon atoms are arranged in a honeycomb (hexagonal) lattice similar to the single-layer graphite lattice, where each carbon atom is covalently bonded with its three neighboring carbon atoms. Conceptually, one can think of a CNT as being rolled up from a strip of single-layer graphite sheet. The angle at which the CNT is rolled is known as the *chiral angle*. Depending on the chiral angle, three cases with vastly different electronic properties can be distinguished, as shown in Fig. 3.4. Zigzag CNTs are always semiconducting, with a bandgap inversely proportional to the diameter. Conversely, armchair CNTs are always metallic. In between these two extreme cases, chiral CNTs are either semiconducting (66 percent) or metallic, depending on the exact chiral angle. CNTs can also be concentrically nested within one another, just like Russian dolls. We refer to a set of nested CNTs as a *multiwall* CNT (MWCNT). Individual CNTs also have a tendency to stick to each other and form bundles of CNTs held together by van der Waals forces.

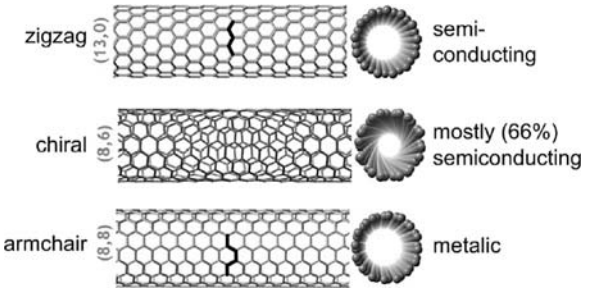


Figure 3.4 Various families of CNTs.[36] Depending on the exact angle at which a CNT is conceptually rolled from a graphene sheet, a CNT can be zigzag, armchair, or in between—that is, chiral. The electronic properties critically depend on the chiral angle. Depending on the exact chiral angle, a CNT can be either semiconducting or metallic.

Single wall CNTs (SWCNTs) were observed for the first time in 1993 independently by Iijima and Ichihashi from NEC[37] and Bethune et al. from IBM.[38] However, MWCNTs had been observed decades earlier, as early as the 1950s (see Ref. 39 for a review of the discovery of CNTs). The discovery of SWCNTs by Lijima in 1993 generated a strong renewed interest in CNTs. Since then, CNTs have been shown to exhibit a unique set of electronic, optical, mechanical, and thermal properties that are potentially useful in many applications in nanoelectronics.[11]

3.3.1 Electronic Transport in CNTs

In a CNT, each carbon atom shares three of its four valence electrons with its three nearest neighbors. The fourth electron, relevant for electronic transport, is delocalized over the full length of the CNT, hence the name "coherent quantum wire."[12]

The unique electronic transport properties of CNTs arise from their 1D structure and their regularity. The transport electrons in a CNT are confined into a 1D wire, in which only forward and backward motion along the wire are quantum-mechanically possible. This greatly reduces the scattering space as sideways scattering events are forbidden. Scattering events, giving rise to resistance, are then a relatively rare occurrence. The average distance that electrons travel between two scattering events (the mean free path) can exceed 1 μm in a CNT,[12–14] leading to ballistic transport (i.e., transport without scattering). For comparison, electrons in a regular metal such as copper scatter on average every 50 nm or so. Because of the long mean free path, exceptionally low resistivities, $r \sim 1\,\mu\Omega$ -cm (lower than that os silver), have been experimentally reported in CNTs.[15]

Counterintuitively, there is a finite nonzero resistance even when transport along a CNT is fully ballistic (without any collision). Such

a finite resistance arises from the finite density of electronic states available for transport given a certain applied voltage, and the finite speed of electrons. For an ideal 1D wire, with only N transverse modes available for electronic transport, this lower limit on the resistance, known as the quantum resistance, amounts to

$$R_{\text{quantum}} = \frac{1}{N} \times \frac{h}{2e^2} \approx \frac{1}{N} \times 13\ \text{k}\Omega \tag{3.1}$$

where h is Planck's constant, and e is the electronic charge.[40] The number of transverse modes N is roughly the number of electronic wavelengths that can fit into the conductor cross section. The quantum resistance is a fundamental limit, which applies to any conductor, not just CNTs. The quantum resistance limit is only important when the cross section of the conductor is approaching the wavelength of the electrons. For the particular case of a SWCNT at low bias voltage, there are only two transverse modes available for transport. Hence, the minimum resistance of an ideal SWCNT is 6.5 kΩ, which has been observed experimentally.[14] For MWCNTs, this lower limit is just scaled down by the number of contacted shells.

The quantum resistance appears as a contact resistance at both ends of the CNTs. The quantum contact resistance is a lower bound: if the electrical contacts at either end of the CNT are not perfect, the overall contact resistance will be higher, and this contribution is known as the contact resistance in the usual sense. Defects or scattering in the CNT will also increase the resistance. For a MWCNT, the key for obtaining a low resistance is to connect to all shells, not just to the outer shell. When this can be achieved, each shell offers two modes of conduction, and this results in a surprisingly low resistance for a single MWCNT. For example, in Ref. 15, the resistance of a single MWCNT was measured to be only about 30 Ω (the MWCNT diameter was about 100 nm, its length was about 25 μm).

Another attractive feature of CNTs for interconnect applications beyond their low resistivity is their unique ability to withstand current density exceeding 10^9 A/cm^2.[16] Such a high robustness to current (three orders of magnitude more than copper) is a consequence of the strength of the carbon-carbon bonds—one of the strongest in nature.

3.3.2 Modeling Work of CNT Interconnects

We now review the literature on modeling of CNT interconnects. These works, essentially, address the following question: what are the benefits for integrated circuits, if any, of using CNT interconnects (assuming that ideal CNTs could be assembled precisely on full-scale semiconductor wafers)? The basic assumption behind these models is that, ideally, the resistivity of CNTs is lower than that of scaled copper

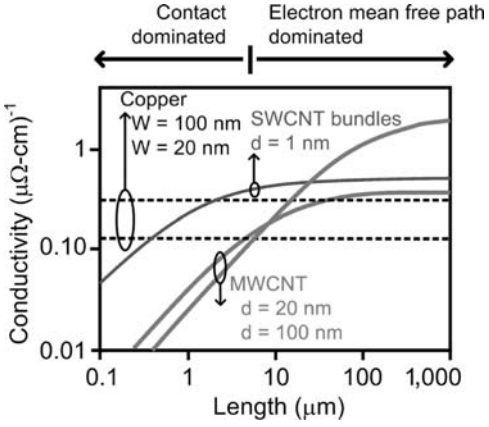


Figure 3.5 Conductivity of densely packed SWCNTs and individual MWCNTs, adapted from Ref. 41. The SWCNTs are 1 nm in diameter and have random chiral angles (such that only 33 percent of them are metallic).

wires for some wire geometries, as shown in Fig. 3.5. Figure 3.6 shows several CNT interconnect geometries that have been proposed and modeled as replacements for copper wires.[19,41–43]

For a fair comparison, the wire width should be the same. On the other hand, the height (or the aspect ratio) of the wire can be decreased. Reducing the wire height decreases the capacitance at the expense of an increase in resistance. The net result is still beneficial for short local wires, because their resistance is not as important as their capacitance.

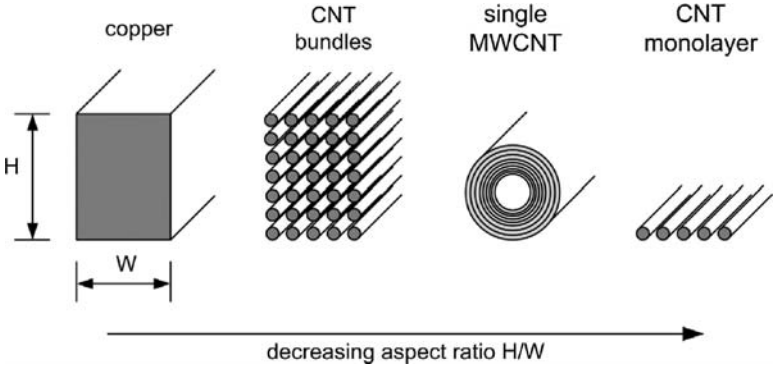


Figure 3.6 Various geometries of CNT interconnects that have been explored, through simulations, by others as replacement to copper wires, including CNT bundles (made of SWCNT or MWCNT), single MWCNT, or a CNT monolayer (most often made only of SWCNTs).

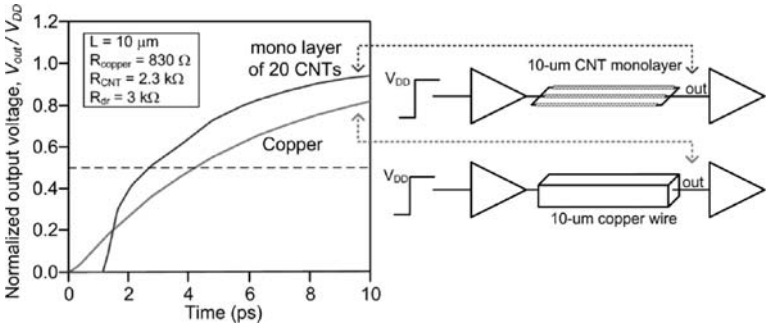


FIGURE 3.7 Step responses of 10-μm-long interconnects for a conventional copper wire and a monolayer of CNTs. A typical inverter with a 10:1 channel width-to-length ratio is assumed as the driver, corresponding to a driver resistance $R_{driver} = 3$ kΩ. The load is assumed to be a three-input NAND gate.[19]

For copper wires, the aspect ratio cannot be reduced below around 1.5 for two reasons.[19] First, it would exacerbate the already severe electromigration problem by increasing the required current density. Second, thickness variations during CMP prevent the fabrication of thin copper wires. In contrast, CNT interconnects are not affected by these two limitations and hence, can be made thinner with a lower aspect ratio, resulting in an additional degree of freedom for optimization. This is assuming that the assembly method itself does not add any other limitations.

To illustrate the benefits of reducing the interconnect height, consider the extreme case in which the interconnect wires consist of single layers of SWCNTs. In this scenario, a monolayer of metallic SWCNTs could replace a conventional copper interconnect (see Fig. 3.7). If the copper wires are replaced by monolayers of SWCNTs, the average capacitance is reduced by about 50 percent from 150 aF/mm down to 75 aF/mm, providing a significant power saving in chips in which interconnect power dominates. This is mainly due to a reduction of the sidewall capacitance, which is also beneficial for reducing crosstalk and jitter. The local interconnect delay is also improved due to the reduction in the capacitance despite the corresponding increase in resistance. This delay improvement is illustrated in Fig. 3.7, where the step responses of two 10-μm long interconnects at the 18-nm node are compared: a monolayer of SWCNTs and a conventional copper interconnect.

Similarly, interconnects made of single-sheet graphite, known as graphene, have been proposed and modeled.[44] The early conclusion is that although graphene interconnects could outperform copper in principle at narrow width (<10 nm), they are not better than monolayers of SWCNTs. This does not rule out graphene interconnects

altogether, as graphene is supposed to be easier to process and pattern. It can be grown on silicon-carbide wafers and can be patterned by conventional lithography and dry etching.

MWCNTs have also been proposed and modeled as replacements for copper wires. Both signal distribution[41] and power distribution[45] through local and global MWCNT interconnects have been considered. Both showed promise of improving interconnect performance thanks to their lower resistance.

3.3.3 Status of Experimental Work

The modeling work has provided strong and clear incentives for further investigation of CNT interconnects in integrated circuits. In this section, we review the literature on experimental work. What can be done in practice as far as integrating CNTs in circuits? In this section, we review recent advances in integrating metallic or semiconducting CNTs for interconnects or transistors, respectively. This is because the circuit integration challenges are similar for both types of CNTs. In fact, as of 2009, metallic and semiconducting CNTs cannot be reliably sorted.

Experimentally, CNTs have been shown to exhibit resistivity as low as 1 $\mu\Omega$-cm (see Ref. 15)—lower than bulk copper or even silver. The ability to pass current density as large as 10^9 A/cm^2 for extended periods of time (more than 2 weeks) at 250°C has been also experimentally verified.[16] These encouraging demonstrations strongly support the potential of CNTs as future high-performance interconnect materials. Although promising, they are mostly limited to one isolated CNT interconnect, whereas several miles of CNT interconnects would be required to wire an integrated circuit.

CNT Vias

CNT vias have also been proposed as vertical vias.[17] Again, their high conductivity and current carrying capability are desirable attributes that can be leveraged to outperform copper vias in terms of resistance and reliability. In addition, their thermal conductivity, higher than that of copper, is another advantage. It could improve the heat transfer from the chip backend down to the substrate, thereby cooling down the interconnect wires. This would improve the reliability and conductivity of the interconnects.[20] Another advantage of CNT when it comes specifically to vias is their ability to grow vertically with a large aspect ratio (nanometers wide and millimeters tall). Such tall vias would allow interconnect layers to be spaced farther apart, lowering the capacitance between subsequent interconnect layers. In terms of processing, CNT vias have been shown to offer great potential. CNTs can be readily grown in vertical forests, filling holes patterned in a dielectric by a damascene approach, and they can also be polished by conventional

chemical mechanical polishing tools. Therefore, the integration of CNT vias reuses most of the tools chip makers routinely use for fabricating copper vias. Fabrication of arrays of CNT vias with promising resistivity on full silicon wafers has even been demonstrated.[18] Despite the foregoing advantages and promises, CNT vias are outside the scope of this chapter. We focus instead on horizontal CNT interconnects.

CNT-Based Circuits

As far as CNT-based circuits are concerned, several groups have reported prototype circuits using transistors based on semiconducting SWCNT. In 2006, IBM reported the first integrated circuit based on a single semiconducting CNT.[10] Their circuit consisted of 12 CNT field-effect transistors arranged in a ring oscillator operating at 72 MHz. Analog amplifiers based on CNT field-effect transistors have also been demonstrated and used in a working 1-MHz radio receiver built on a printed circuit board (not integrated on a single chip).[46] A single CNT has also been used as a resonant antenna in a "nanotube radio."[47] In this prototype circuit, a suspended CNT was used as a resonant antenna and a demodulator by combining the mechanical and electrical properties of CNTs. The major challenge faced by integrated circuit designers when dealing with CNTs is that there is no established infrastructure as yet. High-quality CNT material is not widely available, and no CMOS foundry can integrate CNT-based devices or interconnects. The only practical approach for fabricating prototype integrated circuits with CNTs is the "do-it-yourself approach."

3.3.4 Assembling Multiwall Carbon Nanotube Interconnects

Despite the promises offered by CNTs, several major challenges need to be addressed before CNTs can fit into the semiconductor road map. One of the principal difficulties is the control of their assembly at precise locations. Ideally, one would like to obtain arrays of CNT interconnects at lithographically defined locations on a full wafer. We now review the various methods that have been developed to somewhat reliably assemble CNTs in place. One can distinguish two types of approaches: grow-in-place or grow-then-place.

Grow-in-Place Approaches

In grow-in-place approaches, metal catalyst islands are patterned by conventional lithography and liftoff. The CNTs are then directly grown in a *chemical vapor deposition* (CVD) furnace from the catalysts, ensuring precise control of the starting positions of the CNTs, acting as anchors. On the down side, the substrate has to withstand the growth temperature, which typically exceeds 500°C, or even higher for better quality CNTs. Another challenge is that the full growth process (and hence the metallic catalyst) must also be CMOS compatible.

Vertical Growth in Via Holes In this method, catalyst particles are deposited at the bottom of a trench. The CNTs are then grown by CVD at high density. If the density is high enough, the CNTs grow vertically, creating a CNT forest filling the via hole.[17] The excess CNTs can then be polished back by CMP, very much as copper vias are made.[18] This method has proved to be the most controllable and suitable for manufacturing. Leading semiconductor companies (most notably Fujitsu, and more recently IMEC) have started industrial-scale research programs to explore these CNT vias and fabricate them on full silicon wafers (e.g., Ref. 48).

Horizontal Growth between Catalytic Stripes CNTs will also grow horizontally from catalytic stripes on the substrate surface. It is possible to somewhat control their directionality by having them grow in between two parallel catalytic stripes patterned on the substrate and hence create arrays of devices.[49]

Grow-Then-Place Approaches

In grow-then-place approaches, the CNTs are synthesized on a substrate optimized for growth, and then somehow transferred to the final substrate. Usually, the transfer is accomplished via dispersion in a solvent. This is potentially attractive because solution-based methods for sorting semiconducting and metallic CNTs (to some extent) have been demonstrated using differences in their density[50] or differences in their affinity to polymer.[51]

The major difficulty in grow-then-place approaches is the precise assembly, which cannot even rely on an anchor point, unlike the grow-in-place approaches. Another concern is that the solution processing might degrade the CNTs and affect their electrical properties.

Selective Chemical Functionalization of the Substrate In this method, the substrate is selectively (through lithographic patterning) functionalized chemically. Typically, a monolayer of special molecules is selectively deposited on the patterned substrate.[52] These molecules have been engineered to act as a glue for CNTs, and therefore, the CNTs tend to assemble only on the functionalized areas.

Aligned Growth on Quartz Followed by Transfer Horizontal CNTs can also be grown on crystalline quartz with a high degree of alignment along the quartz crystal direction.[53] These aligned CNTs can then be collected on adhesive tape and transferred onto the final substrate while preserving their alignment.[54]

Self-assembling Aligned CNT Film Using Surface Tension CNT arrays can also be deposited as a aligned film using drop casting, provided that special care is applied during the solution evaporation. The alignment

arises from the surface tension forces near the receding line as the droplet evaporates.[55]

Dielectrophoresis In the dielectrophoresis approach, the CNTs are first dispersed in a solvent. Dielectrophoresis assembly then relies on electric fields to position and align the CNTs in between two electrodes.[56] As a CNT (or any other fairly conductive object, for that matter) floating in a solvent is placed in an external electric field, two opposite electric charges are induced at both ends of the CNT. These two charges, in turn, feel electrostatic forces. In a nonuniform electric field, the two electrostatic forces do not counterbalance each other, and the net force attracts the CNT toward the region of intense electric field, that is, the gap between the two electrodes. Interestingly, once one CNT has been trapped between the two electrodes by the dielectrophoretic force, the electric field pattern is disturbed (it is reduced in the gap) and no more CNT is attracted,[57] provided that the CNT concentration is below a certain threshold.

3.3.5 A Process Flow for Fabricating CNT Interconnect: Illustrative Example

As an illustrative example, consider the process flow we developed for fabricating CNT interconnect on top of commercial CMOS chip at predefined locations.[58,59] The full process flow is illustrated in Fig. 3.8. In step 1, we first pattern an array of gaps between two gold electrodes on an oxidized silicon wafer. The MWCNTs are then dispersed in

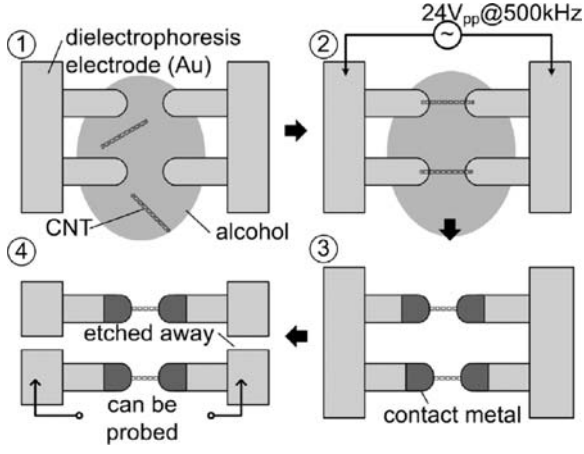


Figure 3.8 MWCNT interconnect assembly process flow. (Step 1) Patterning an array of gaps in between electrodes and deposition of the CNT solution. (Step 2) Dielectrophoresis. (Step 3) Clamping both ends of the CNTs. (Step 4) Wet etching to isolate each CNT.

ethanol by ultrasonication, and a droplet of this solution is deposited on the sample. In step 2, as a 10-V_{rms} voltage at 500 kHz is applied between the gold electrodes, individual MWCNTs assemble in the gaps due to the dielectrophoretic effect. Next, in step 3, the ends of the MWCNTs are briefly exposed to light-power oxygen plasma to reduce the contact resistance, and two metal contacts are deposited by sputtering over the ends of each MWCNT. These metal contacts clamp the MWCNTs in place and also establish electrical contacts. Finally, in step 4, the shared dielectrophoretic electrodes are etched in a gold etchant solution so as to isolate the assembled MWCNTs from one another, thereby allowing separate electrical probing of the individual MWCNTs.

The yield of the full process flow is limited by the dielectrophoresis assembly yield. We typically observed that the yield was highly dependent on the CNT solution concentration. Under the best conditions, the yield reached 25 percent for the 30-nm-diameter MWCNTs.

Figure 3.9 shows SEM images of typical arrays of MWCNT interconnects fabricated using our process flow. Typical arrays consisted of several hundreds of sites where MWCNT interconnects were assembled all at once in parallel during the same dielectrophoresis step.

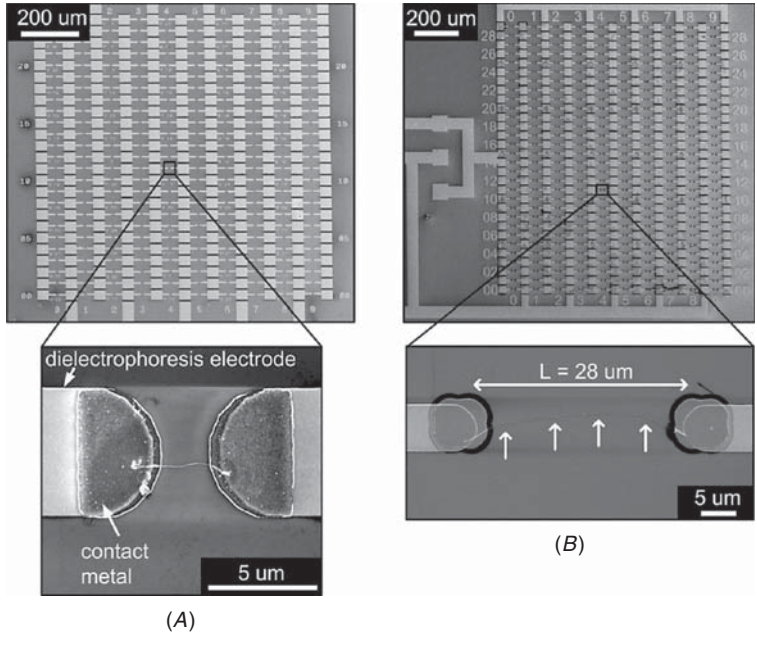


Figure 3.9 SEM images of the MWCNT interconnects. Two types of MWCNT are used. (*A*) Array of MWCNT interconnects from Helix Materials. (*B*) Array of longer and skinnier MWCNT interconnects from NanoTechLabs.

MWCNT interconnects of various lengths were assembled, ranging from 3 to 28 μm in length.

The assembly and contact method developed earlier is very general because it works equally well for different types of CNTs: single-wall, multiwall, and individual bundles that can be electrically probed selectively. Therefore, this method is ideally suited for fabricating arrays of individual MWCNTs for extensive electrical characterization. In addition, the developed method is a room-temperature process, which works on any planar substrate (oxidized silicon wafer, quartz, etc.) and can then be implemented without any adjustments on top of CMOS circuitry, as demonstrated in the next section.

3.4 CMOS Platform for Benchmarking Carbon Nanotube Interconnects

Despite the promise generated around CNT interconnects, there has been no experimental analysis of their performance in a realistic integrated circuit environment. In fact, there has been no experimental demonstration that a metallic CNT can indeed function as an interconnect wire in an electronic chip and successfully transmit gigahertz digital signals from one transistor to another.

In the context of MWCNTs as promising interconnect materials, there are two important benefits and contributions emerging from cointegration of CMOS circuitry and MWCNT interconnects. First, integrating MWCNT interconnects in a CMOS integrated circuit constitutes a proof of concept for MWCNT interconnects. Second, transmission of gigahertz digital signals is indeed possible when the MWCNT interconnects are tightly integrated with CMOS transistors on the same chip, thereby mimicking closely the scenario in which MWCNT interconnects are supposed to operate in the future for the targeted applications.

The possibility of using a MWCNT interconnect for gigahertz digital transmission is a consequence of the fact that a fully integrated test setup for a MWCNT interconnect is a low-parasitic capacitance (or equivalently high-impedance) environment. Such an environment is required to achieve high bandwidth for digital signal transmission. Consider, for example, a 10-kW MWCNT interconnect driving directly a 50-Ω instrument such as a network analyzer (see, e.g., Refs. 62 and 63). There is a large impedance mismatch leading to voltage attenuation by a factor of 200, preventing correct transmission of a digital signal through the MWCNT interconnect. A similar attenuation would take place if the MWCNT interconnect was driving a high-impedance probe via a probing pad. Assuming that the capacitance of the pad and probe combined was 150 fF (typical value), this capacitance would still significantly load the 10-kΩ MWCNT at high speed

with a reactance of around 1 kΩ at 1 GHz, leading to a 10× attenuation preventing direct digital signal transmission (without special amplifier circuitry at the receiving end). In contrast, now consider the same MWCNT in a fully integrated test bench in which the load capacitance is only a few femtofarads, say, 5 fF (reactance of around 32 kΩ at 1 GHz). In this low-parasitic capacitance environment, the MWCNT interconnect can be used to transmit gigahertz digital signals, very much as is envisioned for future integrated circuits, enhancing the proof-of-concept demonstration.

Apart from the work presented here and reported first in Ref. 64, there has been no experimental demonstration that a metallic CNT can indeed function as an interconnect wire in an electronic chip and successfully transmit gigahertz digital signals from one transistor to another. Previous attempts[60,61] to cointegrate silicon transistors and CNTs were limited to the low-frequency regime. Others[62,63] have measured the electrical properties of individual CNT interconnects in the radiofrequency regime (>1 GHz), but their functionality as interconnect wire in a working stand-alone integrated circuit has not been demonstrated.

Our platform CMOS circuit was implemented using a 0.25-μm CMOS technology from TSMC. This 0.25-μm CMOS technology was developed in the late 1990s. Despite the age of this technology, its transistors are still faster than state-of-the-art CNT interconnects. In addition, our post-CMOS optical lithography at the Stanford Nanofabrication Facility (SNF) did not allow features below 1 μm anyway. Another advantage of using a mature technology for our CMOS platform is that the established recipes for etching the passivation layer and revealing and contacting the aluminum metallization are all well understood.

3.4.1 Basic Circuit for Benchmarking CNT Interconnects

To build a CMOS integrated circuit with MWCNT interconnects, we took the following approach. We first designed a purely CMOS circuit with select interconnects intentionally missing from the layout, and had it manufactured by a CMOS foundry (TSMC). We then postprocessed the CMOS chip at SNF to implement the missing wires with MWCNT interconnects right on the chip surface at the required locations.

The basic benchmarking circuit we chose was a seven-stage ring oscillator. One interconnect wire in the oscillator loop was intentionally missing and was to be implemented with a MWCNT on the chip surface during the post-CMOS process. The MWCNT interconnect could be deselected by a multiplexer to ease testing such that every oscillator could be tested even in the absence of an MWCNT interconnect. The benchmarking power of this ring oscillator circuit arises

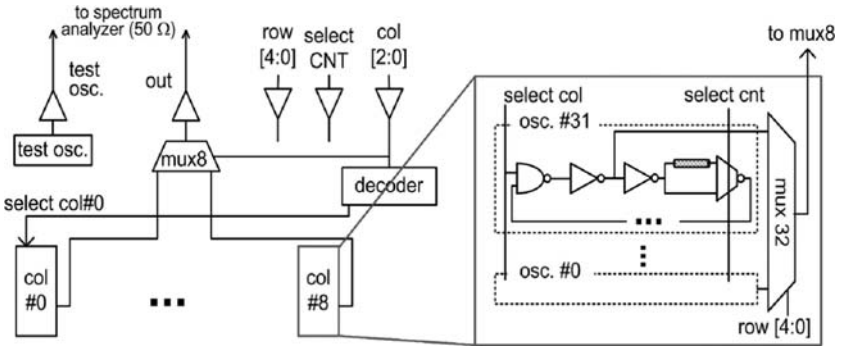


Figure 3.10 Full circuit diagram. The chip contains 256 ring oscillators arranged in an array of 8 columns by 32 rows. Each oscillator has an intentionally missing interconnect wire, to be implemented with a MWCNT. In addition, the chip contains selection circuitry (multiplexer and decoders) to selectively address one of the oscillators at a time.

from the relationship between the MWCNT interconnect resistance and the oscillation frequency. The more resistive the MWCNT is, the slower the oscillator rings. The complete CMOS platform chip consisted of an array of 256 ring oscillators and the selection circuitry to select one ring oscillator at a time, as shown in Fig. 3.10. In addition, a fully wired test oscillator was included for calibrating the test setup, with the interstage wiring in metal 1. Various buffers were included as well to guarantee that signals could be communicated at sufficiently high bandwidth (>1 GHz) despite the presence of long on-chip wires. The output buffers were sized so they could drive bonding pads, and 50-Ω off-chip cables.

3.4.2 Fabrication of CNT Interconnects above a CMOS Integrated Circuit

On delivery by TSMC, the bare 5 × 5 mm CMOS chip was glued (using epoxy) to a carrier 4-in silicon wafer. This greatly facilitated handling in the SNF clean room, while also protecting the CMOS chip from electrostatic discharge because the chip was never directly touched thereafter.

Recall that the process flow we developed on a blank silicon wafer was a room-temperature process, not specific to the substrate. As such, we were able to adapt it for the post-CMOS assembly of MWCNT interconnects with minor additions. Figure 3.11 illustrates the full post-CMOS process flow to implement the array of MWCNT interconnects on the CMOS platform chip. Growing MWCNTs directly on the CMOS chip was not possible, as it would have damaged the CMOS circuitry

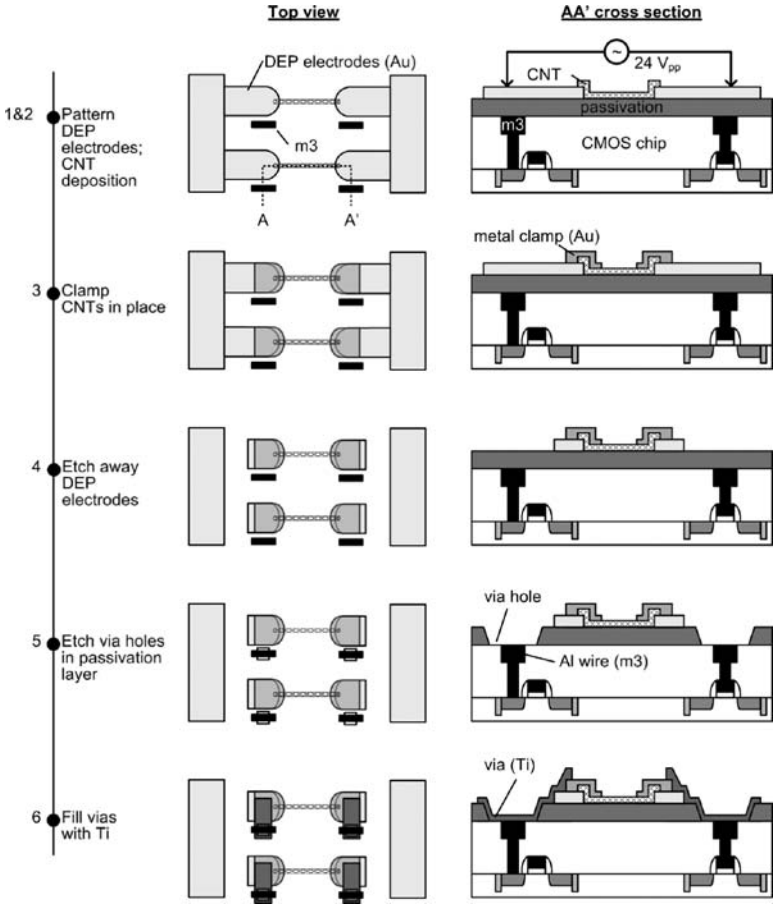


Figure 3.11 Process flow to assemble an array of MWCNT interconnects on top of the platform CMOS chip.

because of the high temperature required for MWCNT growth (typically >500°C).

Instead, we used commercially available MWCNTs. In step 1 (Fig. 3.11), we first patterned an array of gaps in between gold electrodes for dielectrophoresis (DEP). We dispersed the MWCNTs in ethanol. In step 2, we then applied an alternating voltage to assemble and precisely position the MWCNTs in the gaps between the gold electrodes using the dielectrophoretic effect. In step 3, the MWCNTs were secured in place by metal clamps deposited at both ends of the MWCNTs. In step 4, each MWCNT was isolated from its neighbors by wet etching. Next, in step 5, via holes were etched through the CMOS passivation layer to reveal the topmost aluminum metal layer of the CMOS

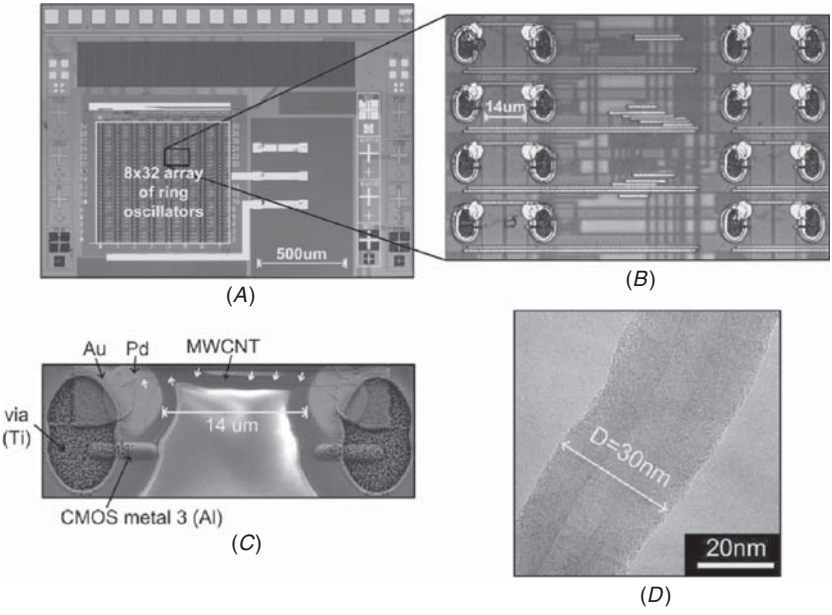


Figure 3.12 Chip micrograph after post-CMOS assembly of the MWCNT interconnects: (*A*) full chip optical image, (*B*) close-up view of a few oscillators within the array, (*C*) an individual 14-μm-long MWCNT interconnect on top of the CMOS chip, and (*D*) TEM images of another MWCNT of the same batch (commercial supplier: NanoTechLabs) with an outer diameter around 30 nm. Note that the samples for the TEM were prepared on a TEM grid (hence, not directly imaged on the CMOS chip).

chip. In step 6, the vias were finally filled with titanium, thereby establishing electrical connections between the underlying silicon CMOS transistors and the MWCNT interconnects.

Figure 3.12 shows the chip after the post-CMOS MWCNT assembly process. As the MWCNT interconnects were precisely assembled by dielectrophoresis literally right on top of the silicon transistors, the parasitic capacitances were minimized (~5 fF). This is a key aspect of this platform because it allows operation above 1 GHz for the first time.

In order to ease testing, the packaged chip was mounted onto a two-layer custom-designed printed circuit board containing the power supply network (connector, decoupling capacitors, and 2.5-V voltage regulator), the RF coaxial output connectors, a set of switches to select one of the 256 oscillators, and an IC socket to house the packaged CMOS chip. The oscillation amplitude and frequency were measured with a spectrum analyzer. The oscillators that were properly wired by a MWCNT interconnect did indeed oscillate, demonstrating the feasibility of MWCNT interconnects in a silicon environment.

The fastest oscillators oscillated at a frequency above 1 GHz, confirming that MWCNT interconnects can successfully transmit gigahertz signals. Such fast oscillation was achieved with a single carbon nanotube interconnect of relatively short length (~4 μm) and relatively large diameter (~75 nm) from Helix Materials. We also used MWCNT from NanoTechLabs with diameter around 30 nm and length up to 14 μm. These MWCNTs achieved lower-frequency oscillations. However, when normalized to their reduced cross section, they exhibited 4× lower average resistivity. In addition, these skinnier and longer MWCNTS are more representative of future interconnect requirements, as they would be suitable for local interconnects at the 22-nm node and beyond. Their electrical performance is analyzed in more detail in the next section.

3.5 On-Chip Performance Analysis of Multiwall Carbon Nanotube Interconnects

In addition to measuring the oscillation frequency, the MWCNT resistance was directly measured on the chip halfway through the process using probe tips. This is significant because it allowed us to correlate the MWCNT interconnect resistance with the oscillator period, establishing experimentally for the first time the link between the static (resistance) and dynamic (delay) behaviors of MWCNT interconnects. The measured resistances were similar to the values obtained with the same MWCNTs on blank oxidized silicon wafers, as expected. In other words, the integration with CMOS circuits did not change the average resistance of the MWCNT interconnects despite the several extra processing steps required. Typically, about 22 percent of the sites were bridged by one or two MWCNTs, while the rest of the sites were not bridged by any MWCNT. Higher concentration of MWCNTs in the alcohol solution used for the assembly would improve the yield further. However, this improvement would be at the expense of depositing sparse film of MWCNTs bridging the electrode gaps, which complicates the analysis given the uncertainty on the number of MWCNTs in each interconnect. Instead, in the rest of this analysis we consider only the sites bridged by one or two MWCNTs.

Referring to the circuit schematic in Fig. 3.10, the extra RC delay contributed by the MWCNT interconnect and its load capacitance increasingly slows down the ring oscillator as the MWCNT resistance increases. Such a slowdown is in fact the signature of the MWCNT interconnect delay. This was verified both experimentally and through transistor-level circuit simulation. The simulated range of oscillation periods, given the CMOS variability, as a function of the MWCNT resistance is plotted as dotted lines in Fig. 3.13.

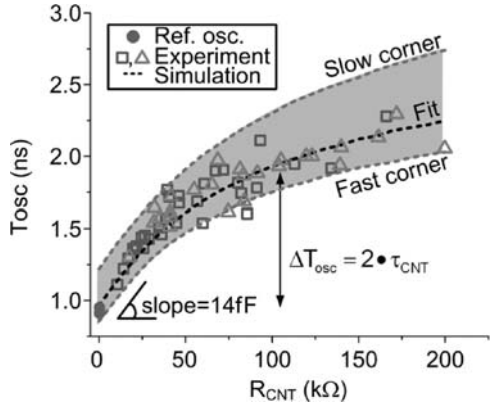


FIGURE 3.13 Oscillation period T_{osc} versus MWCNT interconnect resistance RCNT. The 57 experimental points are indicated by square or triangle symbols, respectively, for 7-μm or 14-μm long MWCNT interconnect (some interconnects are made of several MWCNTs and therefore exhibit a proportionally lower resistance). HSpice simulations are plotted as dotted lines: slow, fast, and typical CMOS process corners are shown, accounting for the CMOS delay variation. The two reference oscillators, the purely CMOS and another one with a Pd wire fabricated on the chip surface, are marked by round filled symbols.

To quantitatively extract the MWCNT interconnect delay, recall that the oscillation period of a ring oscillator is given by twice the delay around the loop, which consists of the MWCNT delay τ_{CNT} and the CMOS delay τ_{CMOS}:

$$T_{\mathrm{CNT}} = 2 \times (\tau_{\mathrm{CNT}} + \tau_{\mathrm{CMOS}}) = 2\tau_{\mathrm{CNT}} + T_{\mathrm{ref}} \tag{3.2}$$

where $T_{\mathrm{ref}} = 2\,\tau_{\mathrm{CMOS}}$ is the oscillation period of the reference oscillator fully wired with aluminum wires. Therefore, the delay τ_{CNT} of the fabricated MWCNT interconnect in a CMOS environment was extracted from the oscillation period T_{CNT} by subtracting the period T_{ref} of a purely CMOS reference oscillator (with only aluminum wires) from the period of the oscillator with one MWCNT interconnect:

$$\tau_{\mathrm{CNT}} = (T_{\mathrm{CNT}} - T_{\mathrm{ref}})/2. \tag{3.3}$$

Figure 3.13 shows the measured correlation between the MWCNT resistance RCNT and the resulting ring oscillator period T_{osc}, confirming our expectations for the first time experimentally.

Table 3.2 summarizes the performance of our best MWCNT interconnects. We observed subnanosecond delays of individual MWCNT interconnects in a CMOS environment ($\tau_{\mathrm{CNT}} = 480$ ps for the best 14-μm-long MWCNT interconnect). Despite this achievement, even

Silicon CMOS chip	
Technology	0.25-μm CMOS
Number of oscillators	256
Number of transistors	11,000
Area	2.5 mm $\times$ 1 mm
Post-CMOS assembly of the CNT interconnects	
Number of extra lithography steps	4
Carbon nanotube	Multiwall
Nanotube contact metal	Gold
In-situ benchmarking, CNT geometry: $L = 3$ μm, Diam $= 75$ nm	
Highest oscillation frequency	1.02 GHz
Minimum resistance R_{CNT}	3 kΩ
Average CNT resistivity	2,500 $\mu\Omega$-cm
In-situ benchmarking, CNT geometry: $L = 14$ μm, Diam $= 30$ nm	
Highest oscillation frequency	522 MHz
Minimum resistance R_{CNT}	109 kΩ
Minimum delay t_{CNT}	480 ps
Average CNT resistivity	640 $\mu\Omega$-cm

Table 3.2 Features of the Fabricated Hybrid Integrated Circuit and CNT Benchmarking

our very best MWCNT interconnect would not be competitive with a scaled copper wire of the same width and same length (and with a typical aspect ratio of 2), in terms of resistivity, and hence, delay. In the same setup, a scaled copper wire would have only contributed an extra 2 ps of delay in the oscillator loop, assuming a nanoscale copper resistivity of 5 $\mu\Omega$-cm.[6]

Our MWCNT had low mean free path compared to the modeling projections, severely limiting the conductivity to well below that of copper. We attributed the discrepancies with respect to the modeling to the ideal assumptions used in the model. In general, these ideal assumptions are, in order of importance, as follows: electron mean free path exceeding 1 μm, ideal contact (contributing no extra resistance beyond the ideal quantum limit of 6.5 kΩ per shell), and all shells taking part in transport.[65]

Given their low conductivity, our fabricated MWCNT interconnects operated in an unfamiliar regime for on-chip wires. Typically, local on-chip wires would affect the circuit performance solely through

their capacitance loading on the driver, and not through their resistance, which is dominated by the driver resistance. However, in this case, the resistance of our MWCNT interconnect greatly exceeded (by two orders of magnitude) the driver resistance. At the same time, the 30-nm-diameter MWCNT interconnect capacitance was overshadowed by the load capacitance corresponding to a 0.25-μm CMOS inverter. This yielded to the unfamiliar, and unrealistic, regime where only the MWCNT resistance affected the circuit performance. In fact, the measured resistivity of our MWCNT ($\sim$640 $\mu\Omega$-cm) was comparable to the resistivity of doped polysilicon, and it is a fact that polysilicon wires are only used to connect adjacent transistors within the same logic gate.

3.6 Conclusion and Outlook

After reviewing the motivations for CNT interconnects and surveying the literature (both modeling and experimental), we have presented local interconnect wires made of single MWCNTs with 30-nm diameter, geometrically suitable for the 22-nm node and beyond. We observed subnanosecond delays through these MWCNT interconnects in a CMOS environment by cointegrating the MWCNT interconnects and CMOS transistors with minimum parasitic capacitance onto a prototype digital integrated circuit. We experimentally observed the correlation between the MWCNT interconnect delay and the measured MWCNT resistance, as expected. The specific MWCNT interconnects fabricated here were still not competitive with copper wires and modeling projections. We have discussed the origins of the discrepancies. The strategy presented herein is by no means limited to the specific MWCNT materials used here. Higher quality MWCNTs, or even SWCNTs and nanowires, can be assembled the same way. Our developed platform is thus a powerful tool in nanoelectronics to evaluate various CNT- or nanowire-based interconnects in a realistic integrated circuit environment.

The key to achieving gigahertz operation with individual CNT interconnects, and more generally any individual nanoelectronic devices/structures, is to have a chain of fast circuits spanning all length scales from the nanoscale all the way up to the macroscopic test instruments (Fig. 3.14). Conventional microelectronic circuits in silicon CMOS technology are natural choices in the middle of this chain because they bridge the gap from the microscale to the macroscopic scale. Without this intermediate CMOS link, individual nanoscale devices would not be able to effectively drive any macroscopic circuits at gigahertz frequencies directly because of their low current drive compared to the macroscopic parasitic capacitances.

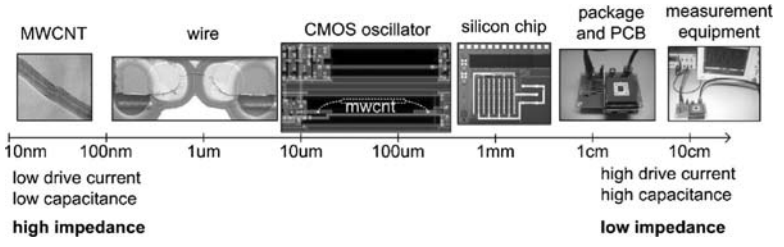


Figure 3.14 Test setup across all of the length scales from the nanoscale MWCNT all the way to the macroscopic measurement equipment. This chain of fast intermediate circuits is the key to achieve gigahertz operation despite the intrinsic impedance mismatch between the quantum world and the macroscopic world.

3.6.1 Outlook

One needs to distinguish vertical (via) from horizontal CNT interconnects. Forests of vertical CNTs suitable for vias can be readily grown selectively in via holes and polished using familiar chemical mechanical polishing tools. The technology to mass manufacture CNT-based vias on 300-mm silicon wafers has been already demonstrated by leading semiconductor companies such as Fujitsu, Infineon, and IMEC. However, it remains to be seen whether high-quality CNTs can be grown at sufficiently low temperature (~400°C) to preserve the integrity of the front-end CMOS transistors. The resulting CNT coverage density needs to be improved as well and is a topic of active research.

In contrast, the technology to mass fabricate reliably horizontal CNT interconnects does not exist today. The prototype IC presented in this chapter constitutes the most advanced published prototype circuit with horizontal CNT interconnects. Several breakthroughs have to happen before horizontal CNT interconnects can be considered as a contender for replacing copper in manufacturing. High-quality CNTs with few defects and impurities ("semiconductor grade") should be made more available. A method to synthesize predominantly metallic CNTs should also be developed. In addition, there is a need to develop a scalable process to position high-quality CNTs (or bundles of CNTs) precisely, and at tight pitches (<50 nm).

The bottom line is that horizontal CNT interconnect is a very disruptive technology. As a result, it might not be appropriate for a one-to-one replacement of copper for interconnecting silicon transistors in the near term, given the extraordinary manufacturing challenges. In the longer term, however, beyond the horizons outlined in the ITRS road map, one can envision that very dense innovative electronic devices, possibly not silicon based, will coexist in a very regular crossbar array with more conventional transistors and more conventional semiglobal copper interconnects. These dense devices, possibly

sublithographic, non-silicon-based, maybe even carbon-based, will open the door for another complementary interconnect technology. In this scenario, horizontal CNT interconnects will have a role to play in interconnecting these dense and regular arrays of devices.

Acknowledgments

This chapter was based on the doctoral work of the author at Stanford University under the expert guidance of Prof. Philip Wong. This thesis work was partially supported by the Interconnect Focus Center (IFC) of the Focus Center Research Program (FCRP) and the Intel Graduate Fellowship. Work was performed in part at the Stanford Nanofabrication Facility. We also thank TSMC for the chip fabrication, and Dr. Ann Marshall for taking the TEM pictures.

References

1. R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, "Integrated nanoelectronics for the future," *Nature Materials*, vol. 6, pp. 810-812, 2007.
2. "International technology roadmap for semiconductors," 2007. Available at http://www.itrs.net/Links/2007ITRS/Home2007.htm.
3. J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, et al., "Interconnect limits on gigascale integration (GSI) in the 21st century," *Proceedings of the IEEE*, vol. 89, pp. 305-324, 2001.
4. J. D. Meindl, "Beyond Moore's Law: the interconnect era," *Computing in Science and Engineering*, vol. 5, pp. 20-24, 2003.
5. S. M. Rossnagel and T. S. Kuan, "Alteration of Cu conductivity in the size effect regime," *Journal of Vacuum Science and Technology B*, vol. 22, p. 240, 2004.
6. W. Steinhogl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *Journal of Applied Physics*, vol. 97, p. 023706, 2005.
7. D. C. Sekar, Azad Naeemi, R. Sarvari, J. A. Davis, and J. D. Meindl, "Intsim: a CAD tool for optimization of multilevel interconnect networks," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 560-567, 2007.
8. C. Hau-Riege, "An introduction to Cu electromigration," *Microelectronics and Reliability*, vol. 44, pp. 195-205, 2004.
9. A. E. Kaloyeros, E. T. Eisenbraun, J. Welch, and R. E. Geer, "Exploiting nanotechnology for terahertz interconnects," *Semiconductor International*, vol. 26, pp. 56-59, 2003.
10. Z. Chen, J. Appenzeller, Y. Lin, J. Sippel-Oakley, A. Rinzler, J. Tang, et al., "An integrated logic circuit assembled on a single carbon nanotube," *Science*, vol. 311, p. 1735, 2006.
11. P. Avouris, Z. Chen, and V. Perebeinos, "Carbon-based electronics," *Nature Nanotechnology*, vol. 2, pp. 605-615, 2007.
12. S. J. Tans, M. H. Devoret, H. J. Dai, A. Thess, R. E. Smalley, L. J. Geerligs, et al., "Individual single-wall carbon nanotubes as quantum wires," *Nature*, vol. 386, pp. 473.7, 1997.
13. C. T. White and T. N. Todorov, "Carbon nanotubes as long ballistic conductors," *Nature*, vol. 393, pp. 240-242, 1998.
14. J. Kong, E. Yenilmez, T. Tombler, W. Kim, H. Dai, R. Laughlin, et al., "Quantum interference and ballistic transmission in nanotube electron waveguides," *Physical Review Letters*, vol. 87, p. 106801, 2001.

15. H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Physical Review Letters*, vol. 95, p. 086601, 2005.
16. B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied Physics Letters*, vol. 79, pp. 1172-1174, 2001.
17. J. Li, Q. Ye, A. Cassell, H. T. Ng, R. Stevens, J. Han, et al., "Bottom-up approach for carbon nanotube interconnects," *Applied Physics Letters*, vol. 82, pp. 2491-2493, 2003.
18. M. Nihei, T. Hyakushima, S. Sato, T. Nozue, M. Norimatsu, M. Mishima, et al., "Electrical properties of carbon nanotube via interconnects fabricated by novel damascene process," *Proceedings of the IEEE International Interconnect Technology Conference*, pp. 204-206, 2007.
19. A. Naeemi and J. D. Meindl, "Monolayer metallic nanotube interconnects: promising candidates for short local interconnects," *IEEE Electron Device Letters*, vol. 26, pp. 544-546, 2005.
20. N. Srivastava and K. Banerjee, "A comparative scaling analysis of metallic and carbon nanotube interconnections for nanometer scale VLSI technologies," *Proceedings of the International VLSI Multilevel Interconnect Conference*, pp. 393-398, 2004.
21. N. Magen, A. Kolodny, U. Weiser, and N. Shamir, "Interconnect power dissipation in a microprocessor," *Proceedings of the International Workshop on System Level Interconnect Prediction (SLIP)*, pp. 7-13, 2004.
22. R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," *Proceedings of the IEEE*, vol. 89, pp. 490-504, 2001.
23. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, et al., "A 45nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100 percent Pb-free packaging," *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, pp. 247-250, 2007.
24. S. Adee, "The ultimate dielectrics is . . . nothing," *IEEE Spectrum*, vol. 45, pp. 39-42, 2008.
25. M. Morgen, E. T. Ryan, J. H. Zhao, C. Hu, T. Cho, and P. S. Ho, "Low dielectric constant materials for ULSI interconnects," *Annual Review of Materials Science*, vol. 30, p. 645, 2000.
26. K. Maex, M. R. Baklanov, D. Shamiryan, F. Lacopi, S. H. Brongersma, and Z. S. Yanovitskaya, "Low dielectric constant materials for microelectronics," *Journal of Applied Physics*, vol. 93, p. 8793, 2003.
27. C. M. Tan, A. Roy, A. V. Vairagar, A. Krishnamoorthy, and S. G. Mhaisalkar, "Current crowding effect on copper dual damascene via bottom failure for ULSI applications," *IEEE Transactions on Device and Materials Reliability*, vol. 5, pp. 198-205, 2005.
28. H. Kitada, T. Suzuki, T. Kimura, H. Kudo, H. Ochimizu, S. Okano, et al., "The influence of the size effect of copper interconnects on RC delay variability beyond 45nm technology," *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, pp. 10-12, 2007.
29. G. Lopez, R. Murali, R. Sarvari, K. Bowman, J. Davis, and J. Meindl, "The impact of size effects and copper interconnect process variations on the maximum critical path delay of single and multi-core microprocessors," *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, pp. 40-42, 2007.
30. H. Kudo, H. Ochimizu, A. Tsukune, S. Okano, K. Naitou, M. Sakamoto, et al., "Strategies of RC delay reduction in 45 nm BEOL technology," *Proceedings of the IEEE International Interconnect Technology Conference (IITC)*, pp. 178-180, 2007.
31. C. Alers, J. Sukamto, S. Park, C. Harm, and J. Reid, "Containing the finite size effect in copper lines," *Semiconductor International*, vol. 29, pp. 38-42, 2006.
32. C.-K. Hu, D. Canaperi, S. T. Chen, L. M. Gignac, S. Kaldor, M. Krishnan, et al., "Electromigration Cu mass flow in Cu interconnections," *Thin Solid Films*, vol. 504, pp. 273-278, 2006.

33. I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *Journal of Applied Physics*, vol. 47, pp. 1203-1208, 1976.
34. J. VanOlmen, S. List, Z. Tokei, L. Carbonell, S. H. Brongersma, H. Volders, et al., "Cu resistivity scaling limits for 20nm copper damascene lines," *Proceedings of the IEEE Int. Interconnect Technology Conference (IITC)*, pp. 49-51, 2007.
35. F. Catthoor, A. Cuomo, G. Martin, P. Groeneveld, L. Rudy, K. Maex, et al., "How can system level design solve the interconnect technology scaling problem?" *Proceedings of the Design, Automation and Test in Europe Conference* pp. 332-337, Feb 2004.
36. A. Sanchez-Castillo, C. E. Roman-Velazquez, and C. Noguez, "Optical circular dichroism of single-wall carbon nanotubes," *Physical Review B*, vol. 73, p. 045401, 2006.
37. S. Iijima and T. Ichihashi, "Single-shell carbon nanotubes of 1-nm diameter," *Nature*, vol. 363, pp. 603-605, 1993.
38. D. S. Bethune, C. H. Klang, M. S. de Vries, G. Gorman, R. Savoy, J. Vazquez, et al., "Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls," *Nature*, vol. 363, pp. 605-607, 1993.
39. M. Monthioux and V. L. Kuznetsov, "Who should be given the credit for the discovery of carbon nanotubes?," *Carbon*, vol. 44, pp. 1621-1623, 2006.
40. S. Salahuddin, M. Lundstrom, and S. Datta, "Transport effects on signal propagation in quantum wires," *IEEE Transactions on Electron Devices*, vol. 52, pp. 1734-1742, 2005.
41. A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Letters*, vol. 27, pp. 338-340, 2006.
42. H. Cho, K.-H. Koo, P. Kapur, and K. C. Saraswat, "Performance comparisons between Cu/Low-k, carbon nanotube, and optics for future on-chip interconnects," *IEEE Electron Device Letters*, vol. 29, pp. 122-124, 2008.
43. S. Haruehanroengra and W. Wang, "Analyzing conductance of mixed carbon-nanotube bundles for interconnect applications," *IEEE Electron Device Letters*, vol. 28, pp. 756-759, 2007.
44. A. Naeemi and J. D. Meindl, "Conductance modeling for graphene nanoribbon (GNR) interconnects," *IEEE Electron Device Letters*, vol. 28, pp. 428-431, 2007.
45. A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance modeling and optimization for single- and multi-wall carbon nanotube interconnects," *Proceedings of the IEEE Design Automation Conference (DAC)*, pp. 568-573, 2007.
46. C. Kocabas, H.-S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, et al., "Radio frequency analog electronics based on carbon nanotube transistors," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 105, pp. 1405-1409, 2008.
47. K. Jensen, J. Weldon, H. Garcia, and A. Zettl, "Nanotube radio," *Nano Letters*, vol. 7, pp. 3508-3511, 2007.
48. Y. Awano, S. Sato, D. Kondo, M. Ohfuti, A. Kawabata, M. Nihei, et al., "Carbon nanotube via interconnect technologies: size-classified catalyst nanoparticles and low-resistance ohmic contact formation," *Physica Status Solidi A*, vol. 203, pp. 3611-3616, 2006.
49. A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, "Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators," *Nano Letters*, 2002.
50. M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, "Sorting carbon nanotubes by electronic structure using density differentiation," *Nature Nanotechnology*, vol. 1, pp. 60-65, 2006.
51. A. Nish, J.-Y. Hwang, J. Doig, and R. J. Nicholas, "Highly selective dispersion of single-walled carbon nanotubes using aromatic polymers," *Nature Nanotechnology*, vol. 2, pp. 640-646, 2007.
52. Y. Wang, D. Maspoch, S. Zou, G. Schatz, R. Smalley, and C. Mirkin, "Controlling the shape, orientation, and linkage of carbon nanotube features with nano affinity templates," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 103, pp. 2026-2031, 2006.

53. S. J. Kang, C. Kocabas, H.-S. Kim, Q. Cao, M. A. Meitl, D.-Y. Khang, et al., "Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic applications," *Nano Letters*, vol. 7, pp. 3343-3348, 2007.
54. N. Patil, A. Lin, E. R. Myers, H.-S. P. Wong, and S. Mitra, "Integrated wafer-scale growth and transfer of directional carbon nanotubes and misaligned-carbon-nanotube-immune logic structures," *Proceedings of the VLSI Technology Symposium*, 2008.
55. H. Ko and V. Tsukruk, "Liquid-crystalline processing of highly oriented carbon nanotube arrays for thin-film transistors," *Nano Letters*, vol. 6, pp. 1443-1448, 2006.
56. K. Yamamoto, S. Akita, and Y. Nakayama, "Orientation and purification of carbon nanotubes using ac electrophoresis," *Journal of Physics D, Applied Physics*, vol. 31, p. L34, 1998.
57. A. Vijayaraghavan, S. Blatt, D. Weissenberger, M. Oron-Carl, F. Hennrich, D. Gerthsen, et al., "Ultra-large-scale directed assembly of single-walled carbon nanotube devices," *Nano Letters*, vol. 7, pp. 1556-1560, 2007.
58. G. F. Close and H.-S. P. Wong, "Fabrication and characterization of carbon nanotube interconnects," *Proceedings of the IEEE International Electron Devices Meeting (IEDM)*, p. 203, 2007.
59. G. F. Close and H.-S. P. Wong, "Assembly and characterization of multi-wall carbon nanotube interconnects," *IEEE Transactions on Nanotechnology*, vol. 7, pp. 596-600, 2008.
60. Y.-C. Tseng, P. Xuan, A. Javey, R. Malloy, Q. Wang, J. Bokor, et al., "Monolithic integration of carbon nanotube devices with silicon MOS technology," *Nano Letters*, vol. 4, pp. 123-127, 2004.
61. A. Narayanan, Y. Dan, V. Deshpande, N. D. Lello, S. Evoy, and S. Raman, "Di-electrophoretic integration of nanodevices with CMOS VLSI circuitry," *IEEE Transactions on Nanotechnology*, vol. 5, p. 101, 2006.
62. P. Rice, T. M. Wallis, S. E. Russek, and P. Kabos, "Broadband electrical characterization of multiwalled carbon nanotubes and contacts," *Nano Letters*, vol. 7, pp. 1086-1090, 2007.
63. S. C. Jun, J. H. Choi, S. N. Cha, C. W. Baik, S. C. W. Lee, H. J. Kim, et al., "Radio-frequency transmission characteristics of a multi-walled carbon nanotube," *Nanotechnology*, vol. 18, pp. 255701-255705, 2007.
64. G. F. Close, S. Yasuda, B. Paul, S. Fujita, and H.-S. P. Wong, "A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors," *Nano Letters*, vol. 8, pp. 706-709, 2008.
65. G. F. Close, S. Yasuda, B. Paul, S. Fujita, and H.-S. P. Wong, "Measurement of Subnanosecond delay through multi-wall carbon nanotube local interconnects in a CMOS integrated circuit," *IEEE Transactions on Electron Devices*, 2009.

CHAPTER 4

Progresses and Challenges of Nanowire Integrated Circuitry

Zhiyong Fan, Johnny C. Ho, and Ali Javey

4.1 INTRODUCTION

Advancements in electronic materials have driven the drastic growth of the semiconductor industry in the past few decades. The number of transistors within an integrated circuit has increased exponentially, doubling approximately every two years. This device scaling trend links to and improves our quality of life in many aspects, including transistor processing speed, computing memory capacity, sensors, and even the number and size of pixels in digital cameras and camcorders. However, the conventional planar silicon technology cannot be scaled indefinitely and there is an active, extensive research effort to investigate alternative technologies.[1] Furthermore, there has been significant effort in recent years to enable new functionalities, unattainable by conventional *complementary metal oxide semiconductor* (CMOS) electronics, by utilizing synthetic electronic materials while developing new fabrication process schemes.[2–8]

Nanostructures, specifically *one-dimensional* (1D) *nanowires* (NWs), have recently attracted huge research attention due to their unique physical properties. In principle, NWs are the ideal active channel materials for the *metal-oxide-semiconductor field-effect transistors* (MOSFETs) because of their superb electrostatics and ability to form coaxial gate stacks.[6,9] In this regard, the NW channel potentially can be modulated more efficiently by the gate electrode, which can minimize the short-channel effects.

Apart from electrostatics, NWs have an extraordinary high surface-area-to-volume ratio and radii comparable to the Debye screening length, resulting in a dominant role of surface electrostatics

in the carrier conduction through the entire material. These properties enable interesting sensor applications. Biological, chemical, and optical NW sensor arrays are the typical examples of nanotechnology-based, highly responsive sensors. For instance, Si NW arrays can allow label-free, highly sensitive multiplexed real-time detection of various antigens, enabling diagnosis and treatment of many complex diseases.[10–12] Also, as chemical sensors, indium tin oxide (In_2O_3) and zinc oxide (ZnO) NWs exhibit parts-per-billion sensitivity to different chemicals such as nitrogen dioxide (NO_2), a hazardous pollutant.[2,13]

In addition to sensors, NWs have been shown to be a highly promising material system for photovoltaic devices because of the high crystalline quality and ease of non-epitaxial synthesis on amorphous substrates. Recently, we demonstrated the template-assisted synthesis of highly ordered, vertical single-crystalline NWs of n-type cadmium sulfide (CdS) directly on aluminum (Al) substrates embedded in p-type cadmium telluride (CdTe) thin film to achieve a *three-dimensional* (3D) heterostructure for novel solar-cell modules.[14] The advantages of this 3D structure include enhancing the photocarrier separation and collection by orthogonalizing the direction of light absorption and *electron-hole pairs* (EHPs) separation with an efficiency of ~6%. Also, the entire cell structure can be transferred onto any substrate such as plastic for flexible photovoltaic applications.

Because of their reduced dimensionality, NWs also exhibit improved mechanical properties compared to their bulk counterparts.[5,15] For instance, the elastic bending modulus, an important physical quantity for cantilever applications of individual indium (In)-doped ZnO NWs, is found to be ~100 GPa.[16] This improved modulus makes ZnO NWs the ideal materials as nanocantilevers and nanoresonators in *nanoelectromechanical systems* (NEMS). Furthermore, they can enable high-performance, flexible electronics and sensor circuitry because of the ease of their assembly on nonconventional, low-temperature substrates such as plastics, further enhancing the potential application regime of the electronic materials.[8,17–21] In this chapter, we review some of the recent advancements in the use of semiconductor NWs for electronics and sensing applications.

4.2 Synthesis of Single-Crystalline Nanowires

Various fabrication and growth methods for semiconductor NWs have been demonstrated. In one approach, NWs are fabricated by lithographic patterning and etching of bulk and/or silicon-on-insulator substrates.[7,22] The main advantage of this process is the control in the placement and fabrication of NW arrays on substrates. Another approach involves the growth of NWs via the "bottom-up" processes that rely on the packing of the atoms and molecules along

energetically preferential directions; therefore, the grown materials have good crystallinity with smooth surfaces, giving them superb materials properties.[23–25] In the bottom-up approach, NWs either are grown directly on the desired substrate or are first grown and then transferred to a receiver substrate. This chapter focuses on and thoroughly discusses only the bottom-up technique.

The dominant NW growth mechanism in this bottom-up technique is known as *vapor-liquid-solid* (VLS) or *vapor-solid-solid* (VSS) via catalytic *chemical vapor deposition* (CVD). The VLS mechanism was first reported in 1964 by Wagner et al., but it was not until the late 1990s that the concept was popularized by Lieber et al. and others to control the composition and structure of NWs for various applications.[23,26–31] As shown in Fig. 4.1*A*, catalytic nanoclusters such as gold (Au) particles are first deposited onto the growth substrates. The sample is then heated to the optimal growth temperature, followed by the introduction of the precursor gas species, such as silane or tetrachlorosilane for Si NW growth. At this stage, Si atoms are absorbed by the catalytic nanoparticles. Once the alloyed nanoparticles reach the supersaturation point, precipitation of single crystals takes place. Eventually, the diameter and the length of NWs grown are dictated by the catalysts' diameter and the growth time, respectively, through the catalytic growth process. During the growth, the catalytic seeds remain either in the solid (VSS) or liquid (VLS) phase, depending on the catalyst and the NW material systems.

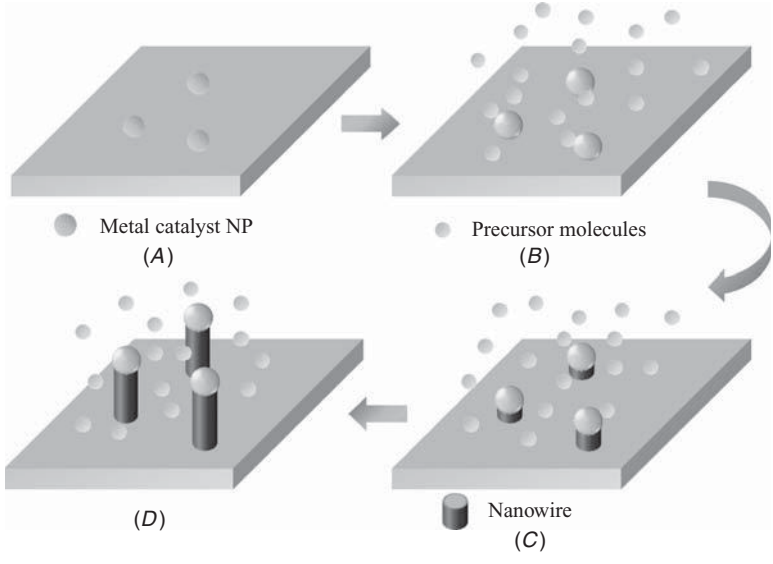


Figure 4.1 Process schematic of the bottom-up VLS NW growth mechanism via catalytic CVD.

One of the main characteristics of this VLS growth mechanism is the utilization of eutectic temperature as the NW growth temperature, providing that the correct choice of catalyst materials is used. For example, during normal *vapor-solid* (VS) growth mode, crystalline Si can only be deposited at temperatures above 800°C, and no high-quality single crystalline Si films can be deposited on any surface below this temperature. In the VLS growth mode of Si NWs by Au catalyst, Au particles form a Au-Si eutectic alloy phase at ~363°C and adsorb Si gas atoms to nucleate crystalline NW growth at a temperature just higher than the eutectic temperature. If the growth temperature is too high or even approaches the VS growth mode, there is simultaneous VS deposition on the NW surface to cause a tapering effect, that is, a nonuniform NW diameter along the entire length of the NW. In that regard, the use of optimal growth temperature and process parameters

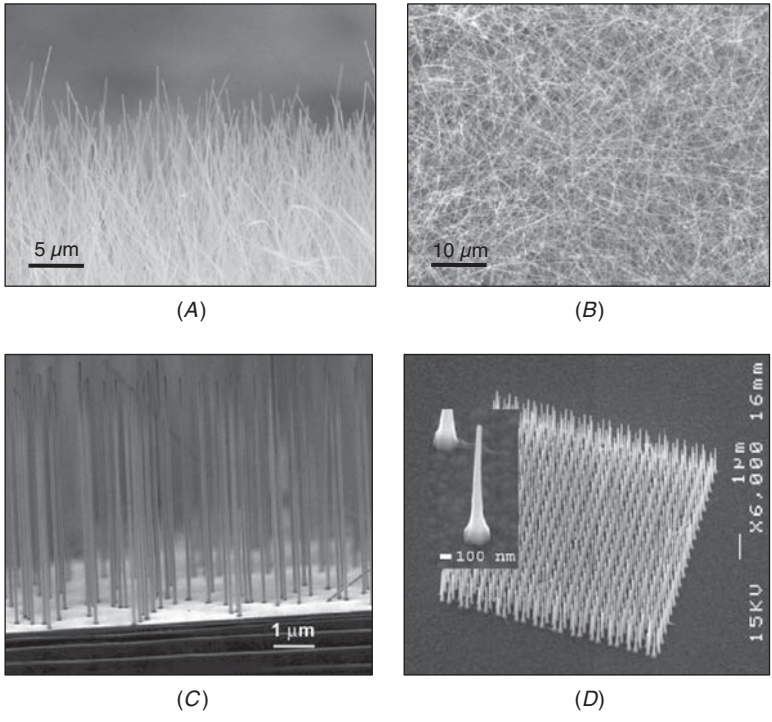


Figure 4.2 Scanning electron microscope images of representative as-grown NWs. (*A*) Side view of non-epitaxial Ge NWs. Reproduced with permission from Ref. 41. Copyright 2009 American Chemical Society. (*B*) Top view of non-epitaxial Si NW. (*C*) Side view of epitaxial Si NWs. Reproduced with permission from Ref. 42. Copyright 2005 American Chemical Society. (*D*) Tilted angular view of epitaxial InP NWs. Reproduced with permission from Ref. 43. Copyright 2003 Institute of Physics.

is critical to ensure catalytic growth without the competing VS process. In the VSS process, the growth takes place at temperatures well below the eutectoid and the melting temperature of the catalyst particles.[32] An example of a VSS process is the growth of Si NWs by Al nanoparticle seeds.[33]

With the advancement in the understanding of the growth mechanism, a variety of elemental semiconducting NWs (e.g., silicon, germanium, silicon/germanium alloy, germanium/silicon core/shell) and compound semiconducting NWs—for example, cadmium sulfide (CdS), cadmium selenide (CdSe), gallium nitride (GaN), indium arsenide (InAs), zinc oxide (ZnO), and indium oxide (In_2O_3)—have been grown.[8,19,27,30,34–40] Typical *scanning electron microscope* (SEM) images of the as-grown NWs are shown in Fig. 4.2.[41–43] NWs can be grown either epitaxially on single-crystalline substrates or non-epitaxially on amorphous substrates. The latter results in randomly oriented forests of NWs, often with a mixture of crystal orientations.[20,21,44] On the other hand, epitaxial growth results in vertically oriented NW arrays.[6,33,42,45] The choice of epitaxial growth depends on the requirements of the desired application and the needed fabrication process scheme.

4.3 Characterization of Nanowires

In order to utilize NWs for technological applications, it is crucial to understand their physical properties in terms of electrical, optical, mechanical, and structural aspects.

4.3.1 Crystallinity and Composition Control of Nanowires

Transmission electron microscopy (TEM) is often used to examine the crystallinity and structural morphology of NWs. Figure 4.3 shows TEM images of some representative semiconductor NWs grown by the VSS/VLS processes. Figure 4.3*A* shows the TEM image of a representative ZnO NW grown with the VLS process.[46] The *high-resolution* (HR) TEM images and electron diffraction patterns (Fig. 4.3*B*) depict the single-crystalline structure of the ZnO NWs with $a = 0.32$ nm and $c = 0.52$ nm, which are in close agreement with the literature-reported values for hexagonal ZnO bulk crystal. Figure 4.3*C* shows the typical HRTEM images of non-epitaxially grown InAs NWs with no dominant grown axis.[19] Several NWs studied here grew in the [211] direction (Fig. 4.3*c1*), the [210] direction (Fig. 4.3*c2*), and $\sim 7^\circ$ off the [111] direction (Fig. 4.3*c3*). Data obtained from standardless x-ray *energy dispersive spectroscopy* (EDS) elemental analysis (not shown here) gave In/As ratios ranging from 1.2 to 1.5, indicating that the composition of the NWs is close to the expected stoichiometry.

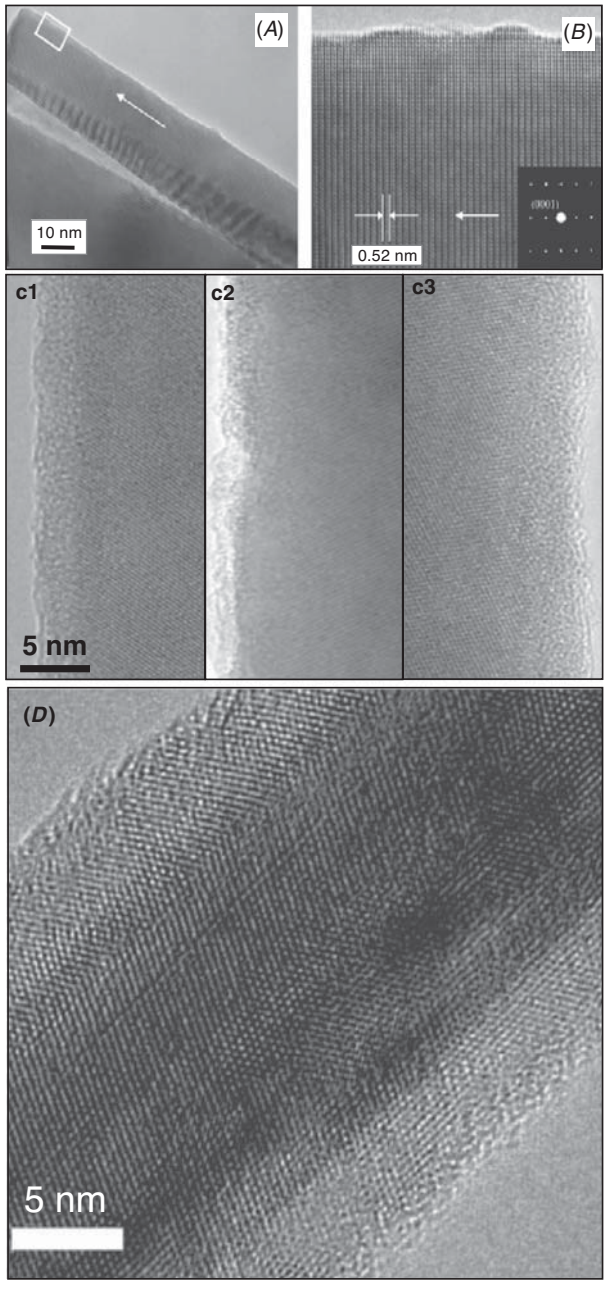


Figure 4.3 Transmission electron microscope images of representative as-grown NWs. (*A,B*) ZnO NWs. Reproduced with permission from Ref. 46. Copyright 2004 American Chemical Society. (*C*) InAs NWs. Reproduced with permission from Ref. 19. Copyright 2008 Springer. (*D*) Ge/Si core/shell NWs, showing an abrupt interface. Reproduced with permission from Ref. 47. Copyright 2005 National Academy of Sciences.

Figure 4.3*D* shows HRTEM studies of Ge/Si core/shell NWs that demonstrate the composition control and structural quality of the grown NWs.[27,47] The TEM image illustrates an NW with a core diameter of 15 nm Ge (dark gray) and a shell thickness of 5 nm Si (light gray); the color contrast between core and shell is caused by the difference in atomic weights of Ge and Si. The lattice fringes and the sharp interface between Ge and Si show that the core/shell structure is epitaxial and consistent with cross-sectional elemental mapping results. All these results reveal success in obtaining high crystal structural quality in bottom-up NWs.

4.3.2 Electrical Transport Properties of Nanowires

Besides the structural imaging of NWs, electrical transport spectroscopy is another important approach for characterizing the properties of NWs for potential electronic and optoelectronic applications. Specifically, to date, Ge/Si core/shell and InAs NWs have been shown to exhibit the highest hole and electron mobility, respectively, in NW material systems.[19,27,47,48] The Ge/Si core/shell NW heterostructure utilizes the formation of 1D hole-gas in the Ge quantum well confined by the epitaxial Si shell. Furthermore, the Si shell provides a high-quality, wider band-gap surface passivation layer for the Ge core. Typical output and transfer characteristics of a FET based on a single Ge/Si NW heterostructure with a channel length $L \sim 1\ \mu$m and NW diameter $d \sim 18$ nm are shown in Fig. 4.4.[27,47] In this structure, Ni *source/drain* (S/D) metal contacts are used to directly contact the Ge/Si channel. Ni is shown to result in near-ohmic contacts to the valance band of intrinsic Ge/Si NWs with minimal Schottky Barriers (SBs) at the interface. Hafnium oxide (HfO_2) high-κ dielectric (~3 nm thick) with metal gate stacks was used to enable efficient electrostatic control of the NW channel. The drain currents (I_d) of Ge/Si NW FETs linearly increase and then saturate as the V_{ds} is increased (Fig. 4.4*A*), similar to the pinch-off behavior of conventional MOSFETs. The transfer curves show an ON current (I_{on}) ~ 14 μA at $V_d = 1$ V, with a peak transconductance ($g_m = dI/dV_g$) of ~26 mS. Importantly, the unit width normalized values of $g_m = 1.4\,\text{mS}\,\mu\text{m}^{-1}$ and $I_{on} = 0.78\,\text{mA}\,\mu\text{m}^{-1}$ using the entire NW diameter as the channel width already exceed the values of 0.8 mS um^{-1} and 0.71 mA μm^{-1} that have recently been reported in sub-100-nm channel length silicon p-MOSFETs with high-κ dielectrics. It is clearly evident that the Ge/Si core/shell NW structure outperforms the state-of-the-art advanced p-type MOSFET structures.

In addition to the p-type materials and elemental semiconductors, n-type compound semiconducting NW materials, such as InAs, have recently attracted significant research effort because of their high electron mobility and ease of near-ohmic metal contact formation.[6,19,48] The electrical properties of a representative single InAs NW FET,

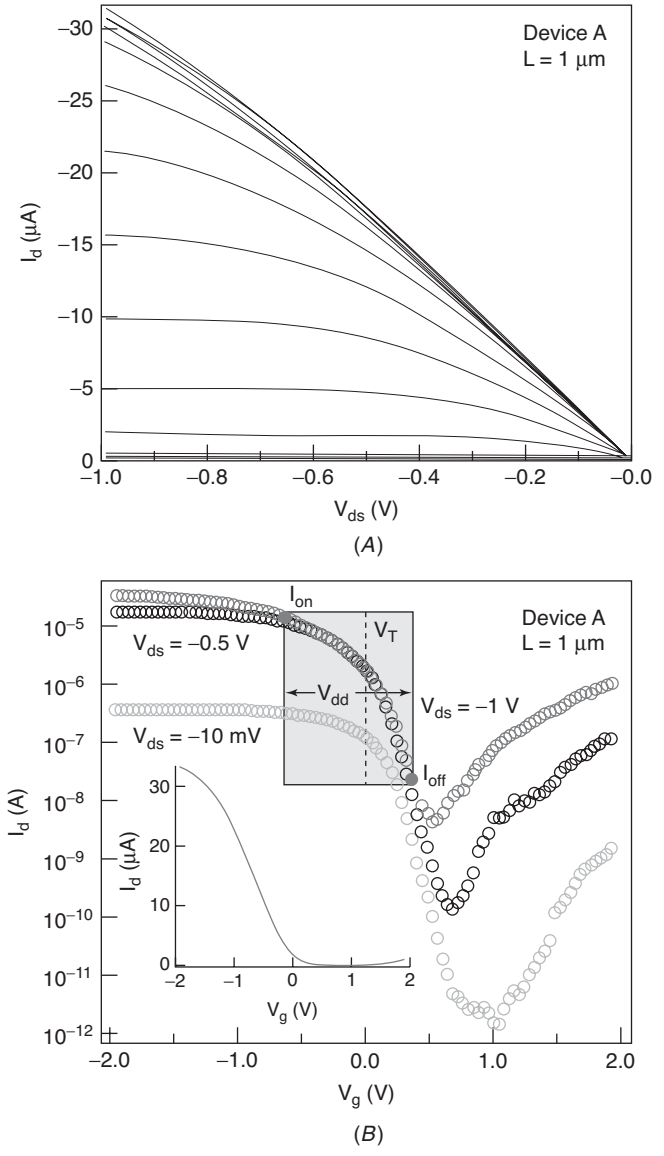


FIGURE 4.4 Electrical characterization of high-performance p-type NW FETs. (*A*) Output and (*B*) transfer characteristics of a representative single Ge/Si core/shell NW FET with a channel length $L \sim 1\ \mu$m and NW diameter $d \sim 18$ nm. Reproduced with permission from Ref. 27. Copyright 2006 Nature Publishing Group.

fabricated by using Ni (~50 nm) S/D metal contacts in a common back-gated geometry (50 nm thermal oxide as gate dielectric and heavily B doped Si substrate as the gate), with diameter (i.e., channel width) $d \sim$ 25 nm (with the subtraction of 2 nm native oxide) and a channel length $L \sim 9.9\ \mu$m are shown in Fig. 4.5.[19] This NW FET shows $I_{on} \sim 12\ \mu$A at $V_{ds} = 3$ V, $V_g = 5$ V with a respectable $I_{on}/I_{off} > 10^3$ and a minimal

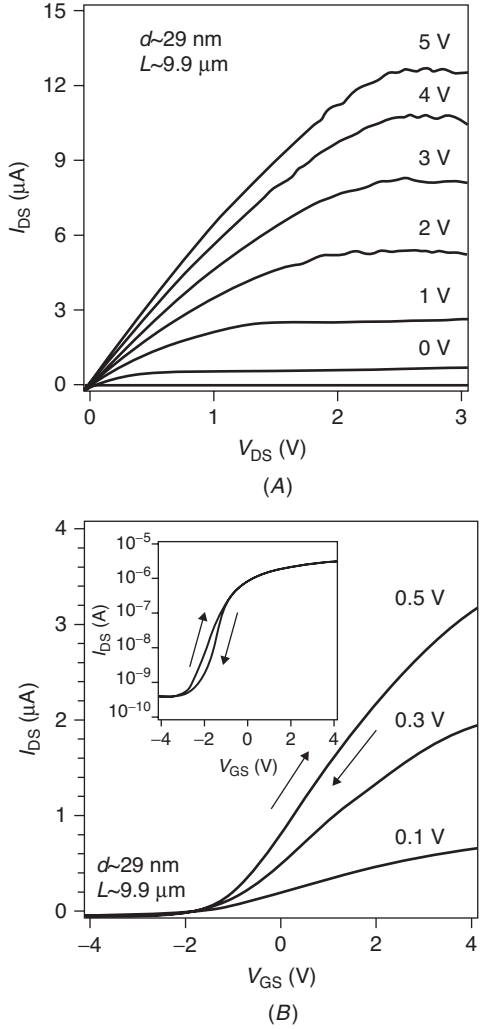


Figure 4.5 Electrical characterization of high performance n-type NW FETs. (*A*) Output and (*B*) transfer characteristics of a representative single InAs NW FET with a channel length L ~ 10 μm and NW diameter $d \sim 30$ nm. Reproduced with permission from Ref. 19. Copyright 2008 Springer.

hysteresis, corresponding to a current density of ~0.5 mA/μm as normalized with the NW diameter. This on current for this long-channel device is comparable to that of state-of-the-art Si MOSFETs ($I_{on} \sim 1$ mA/μm), even though the channel length is more than two orders of magnitude greater.

Understanding the effects of NW diameter miniaturization on the carrier mobility and the electrical properties is essential for the design of optimal NW FETs. The diameter dependence is expected to vary depending on the material system and the fabrication/growth scheme. Figure 4.6 shows the detailed electrical characterization to access the field-effect mobility as a function of InAs NW diameter

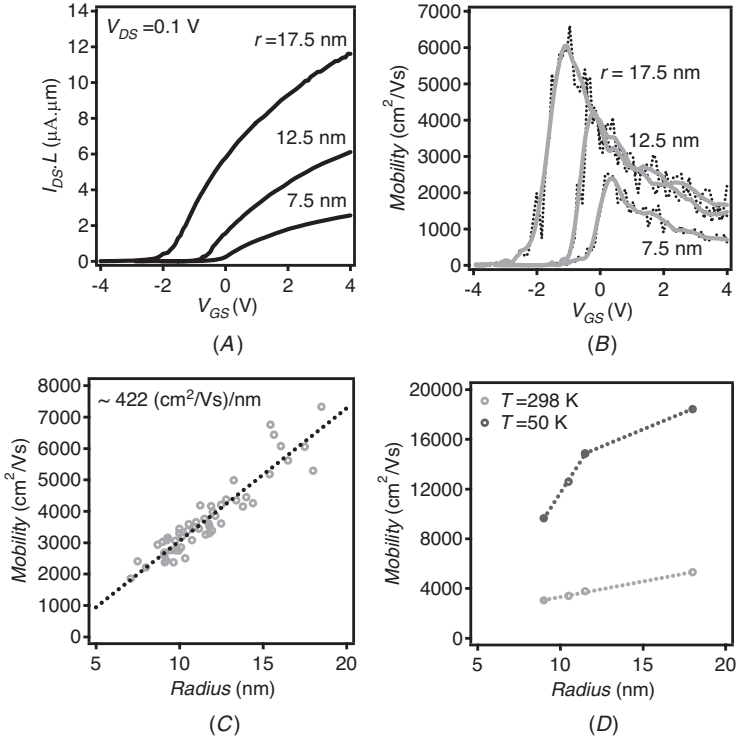


FIGURE 4.6 *I-V* characterization of InAs NW FETs. (*A*) Device output characteristics normalized by channel length ($I_{DS}L$-V_{GS}) at $V_{DS} = 0.1$ V for three separate long-channel devices ($L = 8.4$, 9.6, and 8.4 μm) with NW radii of $r = 17.5$, 12.5, and 7.5 nm, respectively. (*B*) Field-effect mobility as a function of V_{GS} for three corresponding NWs of different radii in (*A*). (*C*) Peak field-effect mobility as a function of radius for more than 50 different devices with NWs ranging from 7 to 18 nm in radius post oxide subtraction. (*D*) The dependency of field-effect mobility on radius for four NWs of different radii at temperatures of 50 and 298 K. Reproduced with permission from Ref. 48. Copyright 2009 American Chemical Society.

while elucidating the role of surface/interface fixed charges and trap states on the electrical properties.[48] The transfer characteristics of representative InAs NW FETs with NW radius ~ 7.5 to 17.5 nm and channel length ~ 6 to 10 μm are shown in Fig. 4.6*A*. Long-channel device structures are used for this study to ensure the diffusive transport of carriers (rather than ballistic or quasiballistic transport), in which intrinsic transport properties such as carrier mobility can be obtained. The VLS/VSS-grown InAs NWs exhibit n-type characteristics although they were not intentionally doped during the growth. This is attributed to the high concentration of electrons arising from surface fixed charges and possible local imbalance in stoichiometry. It is very clear that NWs with larger diameters have higher I_{on} and more negative threshold voltages. This behavior can be attributed to a larger cross-sectional area (i.e., effective channel width) for the large-diameter NW, but it could also be due to the reduced carrier scattering with increasing diameter. In order to perform a more thorough investigation, the field-effect mobility (μ_n) can be deduced from the low-bias transconductance.

Figure 4.6*B* shows μ_n as a function of gate voltage for the same set of NWs. The peak μ_n is increased for larger diameter NWs with the values of ~ 2,500, 4,000, and 6,000 $cm^2/(Vs)$ for $r = 7.5$, 12.5, and 17.5 nm, respectively. Figure 4.6*C* compiles more than 50 NWs with different radius, ranging from ~7 to 18 nm, showing that the peak μ_n linearly increases with the radius with a slope of ~422 $(cm^2/(Vs))/nm$. To understand the source of mobility degradation for smaller NWs, temperature-dependent electron transport measurements with $r \sim 8$ to 20 nm at 298 and 50 K were conducted and depicted in Fig. 4.6*D*. Even at low temperatures (i.e., 50 K), in the regime where phonons and surface/interface traps are mostly frozen out, the mobility still increases monotonically with radius, suggesting that the observed mobility dependency at 50 K is probably mainly attributed to the enhanced surface roughness scattering of electrons in the miniaturized NWs. The difference in the mobility between 298 and 50 K is attributed to other factors such as phonon scattering and interface/surface trap states. Although thinner NWs are attractive for short-channel devices because of their superb electrostatics, the drastic effect of NW radius on the field-effect mobility suggests that the NW diameter needs to be carefully chosen to enable optimal performance by compromising carrier transport and electrostatic efficiencies.

4.3.3 Photoconductivity of Photonic Nanowires

In addition to the electronic applications, several semiconducting NW materials are optically active such as CdSe NWs with a direct bandgap of 1.76 eV, which is an ideal candidate material for the photodetection of visible light. In order to utilize CdSe NWs as optical sensors,

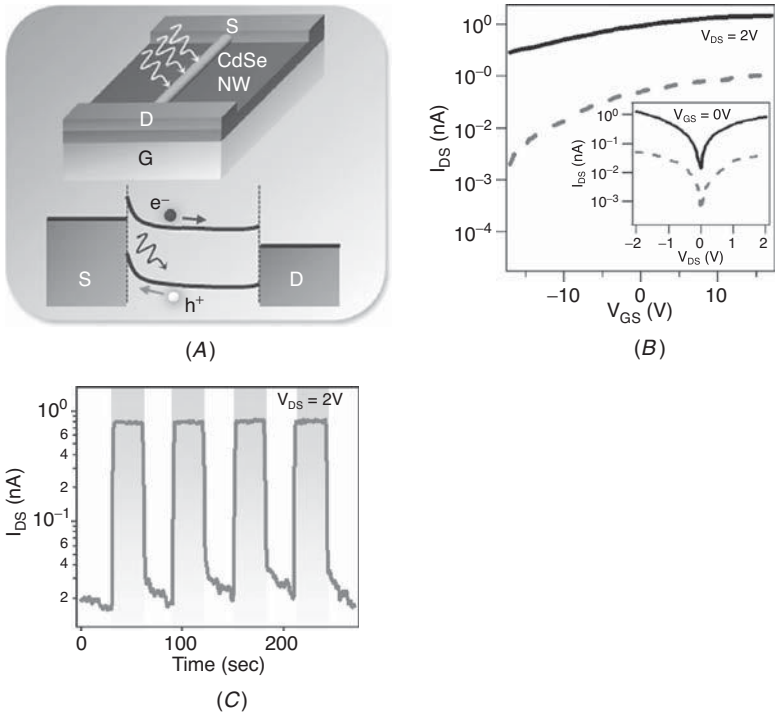


Figure 4.7 Highly sensitive, direct bandgap NW photodiode. (*A*) Schematic (*top*) and the band diagram (*bottom*) of a CdSe NW photodetector with Ni/Pd Schottky S/D contacts. (*B*) I_{DS}-V_{GS} and I_{DS}-V_{DS} (*inset*) curves of a representative CdSe NW device before (dashed line) and after (solid line) white light illumination, exhibiting ~100 times the current modulation. (*C*) Transient of a single CdSe NW device with an illumination intensity of 4.4 mW/cm^2. Reproduced with permission from Ref. 8. Copyright 2008 National Academy of Sciences.

Schottky devices were fabricated by contacting the NWs with high-work-function Ni/Pd (5/45 nm) S/D electrodes as depicted in Fig. 4.7*A*.[8] CdSe NWs are grown intrinsically without any intentional doping and exhibit n-type behavior (Fig. 4.7*B*) due to their surface Fermi-level pinning. Without the illumination of visible light, the device exhibits large dark resistance, $R_{dark} \sim 140$ GΩ, because of the Schottky barriers at the S/D interfaces that limit the carrier injection from the metal into the intrinsic semiconductor NWs. On light illumination, a drastic decrease of ~100× in the device resistance, $R_{light} \sim 2$ GΩ, is observed that is attributed to the efficient electron/hole photogeneration and field-induced carrier separation in CdSe NWs. Figure 4.7*C* shows time-dependent photoconduction measurement of CdSe NWs, showing the consistent photoresponse on multiple cycles of illumination.

4.4 Nanowire Assembly

Controlled assembly of NWs on substrates with high uniformity over large areas presents a major challenge. For epitaxially grown NWs, the vertical orientation is achieved directly during the growth and the precise placement is achieved by lithographically patterning the catalyst seeds on the substrate prior to the growth.[43,45,49–52] As a result, if the application and the device architecture can tolerate the use of crystalline substrates and the vertical orientation of NWs, then epitaxial growth can be readily used to enable precise control over NW assembly.[53,54] However, for many applications, horizontally oriented NWs and/or amorphous substrates are required. In that regard, NWs have to be grown on a substrate first, followed by their transfer to a secondary substrate for eventual device fabrication. In the past, several strategies such as flow-assisted alignment,[55–58] electric-field directed deposition,[59–62] selective chemical patterning of the substrate,[63,64] the Langmuir-Blodgett technique,[65–67] and contact printing[8,19–21,44] have been explored with varying degrees of success. The last is based on the direct transfer of NWs from the growth to the receiver substrate, whereas the other methods rely on first harvesting the NWs into a solution followed by their transfer to the desired substrate. To date, contact printing has been shown to be one of the best demonstrated techniques for assembly of parallel-array NWs on a large scale with high uniformity. This technique has enabled fabrication of integrated circuits with the highest degree of complexity shown to date.[8] As a result, we focus primarily on the contact printing method for the remainder of this section.

4.4.1 Nanowire Contact Printing Methodology

The contact printing technique utilizes shear force to effectively align the NWs, and chemical binding interactions to anchor and transfer the NWs from the growth to the receiver substrate.[20] Figure 4.8*A* schematically demonstrates the process flow for contact printing of NWs, starting with a NW growth substrate (i.e., donor substrate) with random growth orientation (i.e., non-epitaxial growth), resembling a "forest." The growth substrate is then brought in contact with the receiver substrate, followed by directional sliding under a normal pressure of $\sim$10 g/cm^2 (see Ref. 20). During the sliding process, NWs are dragged on the receiver substrate and are aligned by the enabled shear force. If appropriate surface treatment is applied, NWs are anchored by chemical interactions to the receiver substrate, resulting in their breakage and transfer to the receiver substrate as parallel arrays.[20] In order to minimize mechanical interactions while enhancing the chemical interactions, a lubricant, such as an octane and mineral oil mixture, is applied in between the two substrates during the printing process.[20]

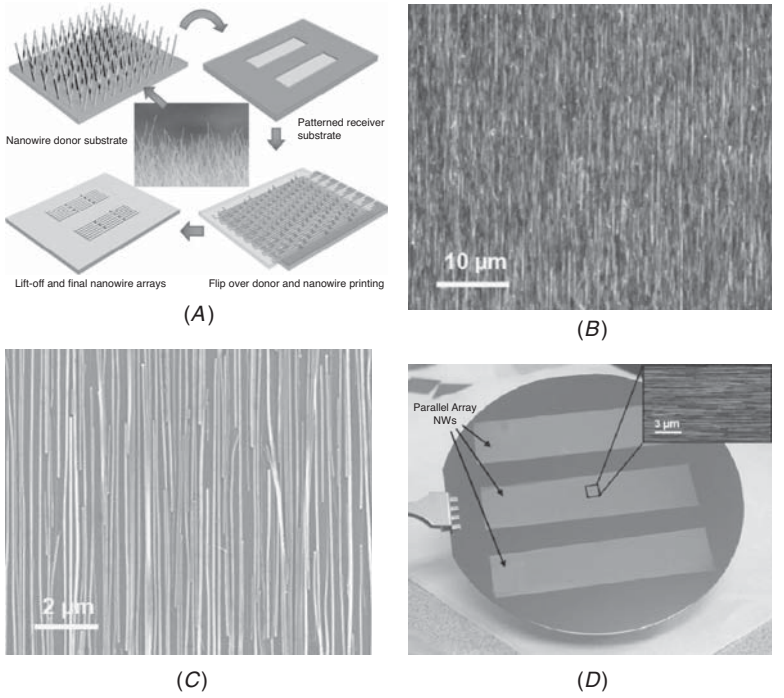


FIGURE 4.8 Nanowire contact printing methodology. (*A*) Schematics of the NW contact printing involving planar growth (donor) substrates. (*B*) Dark-field optical and (*C*) SEM images of Ge NWs ($d \sim 30$ nm) printed on a Si/SiO_2 substrate showing highly dense and aligned monolayer of nanowires. The self-limiting process limits the transfer of NWs to a single layer, without significant NW bundling. (*D*) Wafer-scale NW printing. Large-area and highly uniform parallel arrays of aligned GeNWs ($d \sim 30$ nm) were assembled on a 4-inch Si/SiO_2 wafer. The inset is an SEM image of the printed NW film, showing a density of $\sim$7 NW per μm. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

Figure 4.8*B*,*C* shows the optical and SEM images of well-aligned printed nanowires with a density ~ 8 NW/μm.

It is noteworthy that the interaction force between NWs and receiver substrate is van der Waals and/or hydrogen bonding in nature, depending on the surface treatment. The magnitude of this type of interaction is highly sensitive to surface treatment/functionalization, which will be elaborated later. This nanowire printing method is highly versatile and generic. We have achieved up to 4-inch wafer printing of nanowires, as shown in Fig. 4.8*D*, which is only limited by the NW growth capability (i.e., the size of the growth substrate).

4.4.2 Dynamics of the NW Printing Process

Investigation of NW printing dynamics is fundamentally important to achieve control over the printing characteristics such as NW density and alignment. The dominant physical/chemical interactions involved in the process are for NW-receiver substrate and NW-NW systems.[20] The former interaction favors NW alignment and transfer to the receiver substrate, whereas the latter results in poor NW alignment and uncontrollable breakage of NWs due to NW-NW friction. In order to minimize the effects of NW-NW mechanical friction, a liquid-phase lubricant is applied during the printing process.[20] Figure 4.9

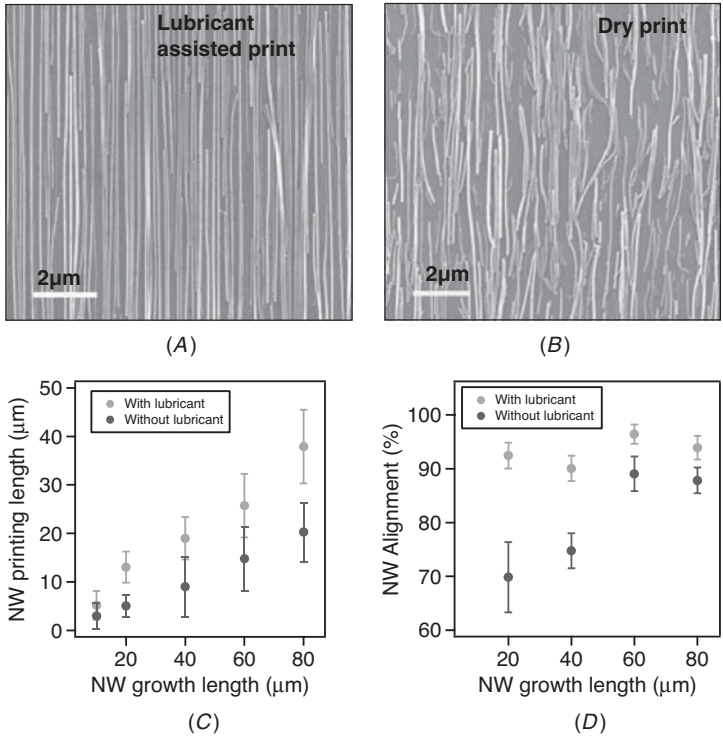


Figure 4.9 The effect of lubricant on the contact printing of the nanowires. SEM images of GeNW printing with (*A*) and without (*B*) lubricant, clearly showing the impact of the lubricant in obtaining highly aligned and ordered NWs. (*C*) The average length and (*D*) orientation alignment of the printed GeNWs as a function of their original length on the growth substrate for contact printing with and without lubricant. For (*A*)–(*D*) the receiver substrate was functionalized with poly-L-lysine. Upper points in each graph are with lubricant. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

shows the effect of lubricant on nanowire printing characteristics. Specifically, by applying octane and mineral oil mixture (2:1, v:v) as the lubricant, NW contact printing process can consistently yield highly dense and well-aligned parallel arrays of NWs (Fig. 4.9*A*), in clear contrast to the NWs assembled by a "dry" printing process (Fig. 4.9*B*).

To quantify the effect of the lubricant on NW printing, statistical analyses of the printed NW length and alignment were performed, as shown in Fig. 4.9*C,D*.[20] The printed NW length demonstrates a linear dependence on the initial NW growth length (i.e., on donor substrate). The average printed NW length, nevertheless, is approximately twice as high when a lubricant is applied as compared to the dry printing.[20] This trend is attributed to the reduction of the undesired mechanical friction by the application of the lubricant. The percentage of aligned NW, defined as $< 5^\circ$ angle with respect to the printing direction, was also examined as a function of the NW length. As shown in Fig. 4.9*D*, application of the lubricant results in $> 90\%$ of printed NWs being well aligned, regardless of the NW growth length. However, dry printing (i.e., without lubricant), results in a noticeably inferior alignment, especially for the shorter NW growth lengths.[20]

The application of lubricant reduces the mechanical friction while enhancing the desirable and highly tunable chemical interactions between NWs and the receiver substrate.[20] As pointed out previously, this interaction is sensitive to receiver substrate surface treatment/functionalization, leading to controllable nanowire printing characteristics. This effect is quantified and demonstrated in Fig. 4.10, where

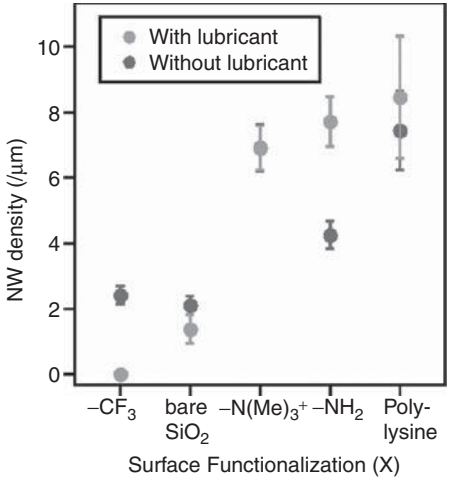


Figure 4.10 Nanowire printing density of Ge NWs ($d \sim 15$ nm) as a function of the surface functionalization of the receiver substrate. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

the printing process is conducted on Si/SiO_2 substrates with various surface functionalizations, including siloxane monolayers and poly-L-lysine.[20] The printed NW density for "wet" printing is significantly more sensitive to the surface functional groups of the receiver substrate, as compared to that obtained from "dry" printing. Specifically, for the receiver substrates functionalized with $–CF_3$ terminal groups, which are well known to be highly hydrophobic and "nonsticky," almost no transfer of NWs ($<10^{-3}$ NW/μm) from the donor to the receiver substrate is observed for wet printing. On the other hand, an identical printing process on $–NH_2$ and $–N(Me)_3^+$ terminated monolayers resulted in a highly dense NW assembly through the strong surface bonding interactions, approaching $\sim$8 NW/μm.[20] This $\sim$4 orders of magnitude modulation of NW density by controlling the surface chemical interactions is highly desirable for patterned printing of NWs, as discussed later in this chapter. Notably, for "dry" printing, the printed NW density shows a minimal dependence on the surface functional groups, varying only from $\sim$2 to $\sim$7 NW/μm for fluoro- and amine-terminated surfaces, respectively. This result reveals the important role of the lubricant in the controlled and tunable assembly of NWs.

4.4.3 Patterned Nanowire Printing

In order to fabricate NW-based devices and circuits at the designed locations, patterned assembly of NWs on substrates is needed. In this case, receiver substrates with lithographically patterned *photoresist* (PR), electron-beam resist,[8,19,20] or molecular monolayer resist[44] were utilized for the printing process. Figure 4.11 shows an optical image of a pre-patterned PR layer (500 nm thick) on a Si/SiO_2 (thermal oxide, 50 nm) substrate. The subsequent contact printing and resist lift-off yields patterned Ge NW parallel arrays shown in Fig. 4.11*B*, with the zoomed-in SEM image showing high density and good alignment. To achieve higher spatial resolution with contact printing, electron-beam lithography was utilized to define 200-nm-wide open channels on the aforementioned Si substrate, as shown in Fig. 4.11C.[20] The patterned substrate was then used as the receiver substrate for NW contact printing followed by resist lift-off. As shown in Fig. 4.11*D*, individual NWs have been observed in the previously defined fine channels. These results demonstrate the ability to control the number of assembled NWs per site by simply tuning the width of the patterned regions in the resist layer. However, in order to achieve devices with consistent performance, for example, ON current for transistors, parallel arrays of NWs are preferable for the active material because of the averaging effect.

Besides using relatively thick polymer resist layers to define the NW printing patterns, molecular monolayers were also utilized as

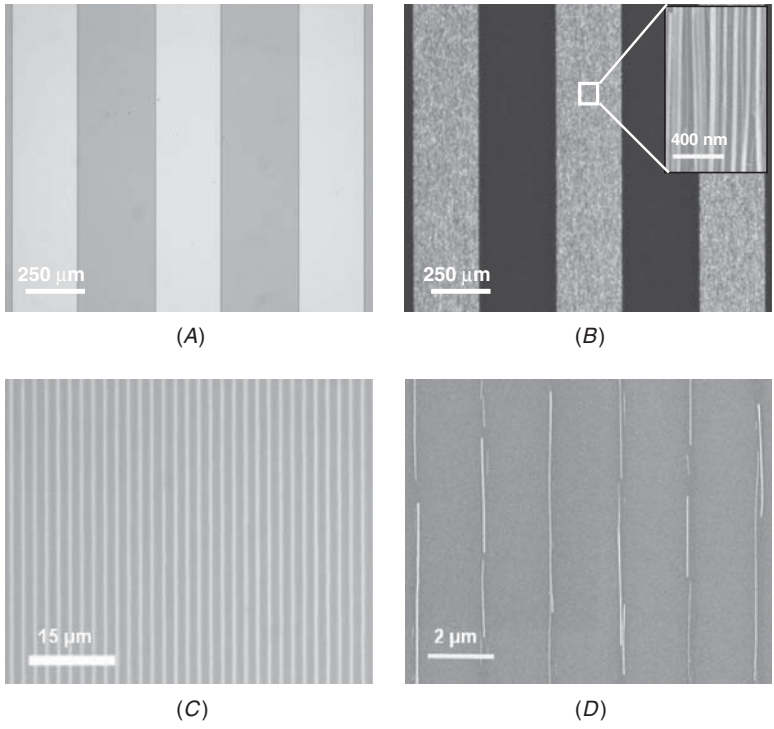


Figure 4.11 Lithographic patterning of polymer resists for patterned Ge-NW printing on Si substrates. (*A*) Bright-field optical image of a patterned PR layer on a Si/SiO_2 substrate prior to the NW printing process. (*B*) Dark-field optical image of the assembled NWs after the printing and PR lift-off processes. Inset shows the SEM image of the well-aligned NW arrays. (*C*) Bright-field optical image of *electron beam lithography* (EBL)-patterned *poly(methyl methacrylate)* (PMMA) layer on a Si/SiO_2 substrate, showing channels with width ~200 nm and 2-mm pitch. (*D*) SEM image of the assembled NWs after NW printing and PMMA lift-off, showing single NW positioning on the substrate. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

an efficient resist layer for patterned NW printing.[44] In this process, the substrates with thermally grown oxide are chemically reacted with *(heptadecafluoro-1,1,2,2-tetrahydrodecyl)dimethylchlorosilane* (HDF) to form highly-stable, fluorinated *self-assembled monolayers* (SAMs) on the surface.[44] To form the pattern on the monolayer, a *very ultraviolet* (VUV) light (172 nm, ~25 mW/cm^2) is projected on the surface of the HDF-treated substrate through a shadow mask, in an oxygen-rich environment.[44] On VUV exposure, C–F bonds are chemically cleaved and oxidized, resulting in the formation of –COOH and –CHO functional end groups, as schematically shown in Fig. 4.12*A*. Because of the nonpolar nature of $–CF_3$ groups, the fluorinated surfaces are

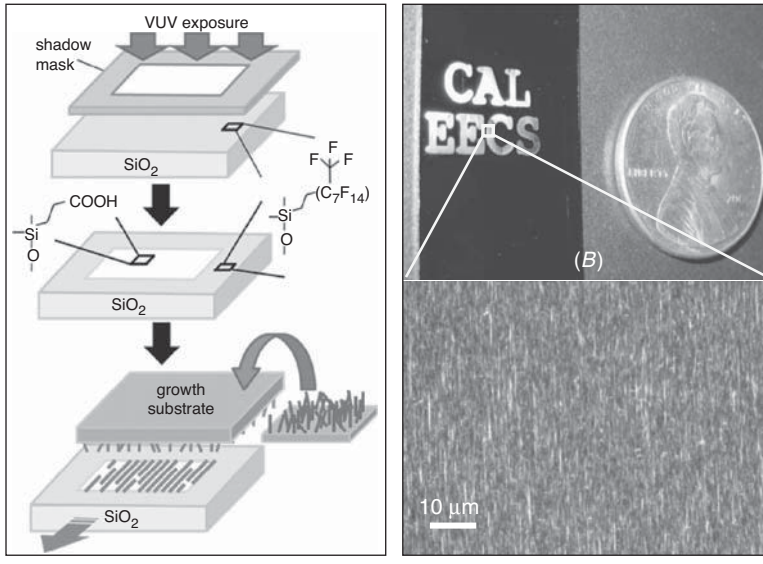


Figure 4.12 Very ultraviolet (VUV) projection patterning of monolayer resist for Si-NW printing on Si substrates. (*A*) Schematic of the patterned NW contact printing process using molecular monolayers as the resist. (*B*) Optical image of the patterned Ge NWs printed on a VUV-exposed Si/SiO_2 substrate with the SAM resist. (*C*) High-magnification optical image of the printed NW arrays, showing high NW density with good alignment. Reproduced with permission from Ref. 44. Copyright 2009 American Chemical Society.

highly nonsticky to NWs, whereas –COOH and –CHO groups interact strongly with the NW surfaces, most likely through hydrogen bonding with the native oxide layer.[44] As a result, this simple process creates a contrast of "sticky" and "nonsticky" regions on the receiver substrate, assisting the subsequent patterned NW printing (Fig. 4.12*A*), without the need for a lift-off process. Figure 4.12*B* shows the optical images of patterned Ge NW parallel arrays on a substrate with a monolayer resist after VUV exposure, where the NWs are assembled only in the VUV pre-exposed areas.

4.4.4 Printing of Nanowire Superstructure

To implement complex functions with semiconductor NWs, they are often required to be assembled/integrated together heterogeneously. In this sense, hierarchical assembly of NW superstructures is of great interest for a number of applications, such as smart sensors composed of many sensing elements, logic circuit arrays that have field-configurable function, and so on. The NW contact printing approach provides a convenient route toward these goals because it involves

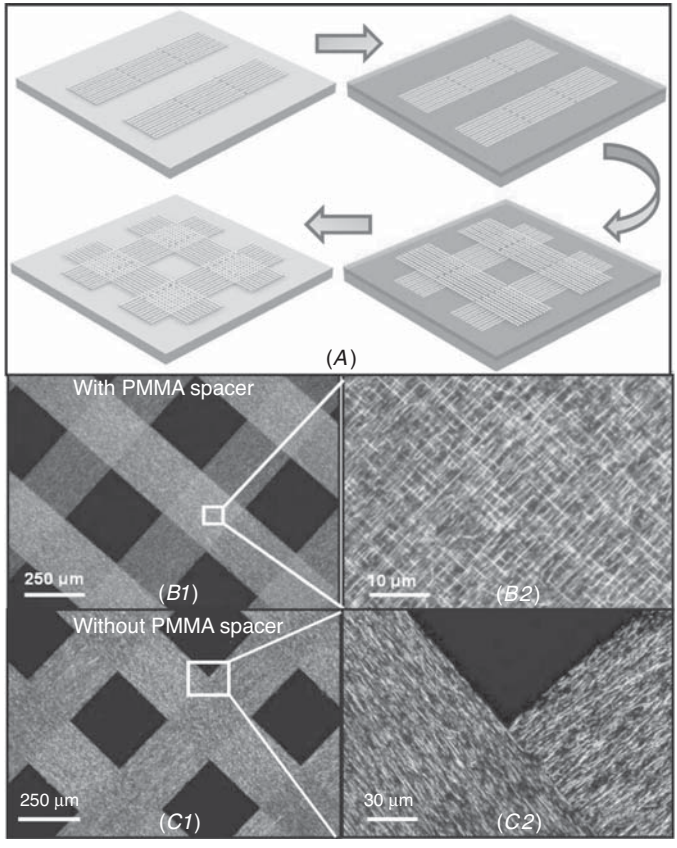


Figure 4.13 Assembly of Ge-NW superstructures on Si substrates. (*A*) Schematic of a multistep NW printing process for the large-area formation of NW crossbars. (*B1*,*B2*) Dark-field optical images of SiNW crossbars formed by a two-step printing process with a PMMA buffer layer. (*C1*,*C2*) Dark-field optical images of assembled Si NWs by a two-step printing process, without the use of a PMMA buffer layer. Without the PMMA buffer layer, NW crossbars are not formed because of the weak NW–NW chemical surface interactions. Reproduced with permission from Refs. 20 and 74. Copyright 2008 American Chemical Society, 2009 Wiley InterScience.

low-temperature processes. In our work, we have achieved large-scale NW crossbar arrays through a multistep printing process,[20] as illustrated in Fig. 4.13*A*. In this process, a layer of parallel Si NW arrays are printed on the receiver substrate in 250-μm channels predefined by photolithography. Then, a layer of *poly(methyl methacrylate)* (PMMA, ~40 nm thick) is spin-coated on the substrate serving as a buffer layer. A subsequent second patterned printing step is then performed with a 90 degree rotation in respect to the first step. After photoresist lift-off, the PMMA buffer layer is etched away by a mild O_2 plasma process

(60 W, 2 min), resulting in the assembly of large arrays of NW crossbars (Fig. 4.13*B1,B2*).[20] Interestingly, the NW printing process is found to be self-limiting. Specifically, NWs are rarely observed to stack on top of each other during a single printing step.[20] This is mainly due to the small NW-NW contact area and weak surface chemical interaction, especially when lubricant is applied. As a result, when the two-step cross-printing is performed without the PMMA buffer layer, the second NW printing layer does not stack on the first layer to form NW-crosses, as shown in Fig. 4.13*C1,C2*.

4.4.5 Roll Printing of Nanowires on Nonconventional Substrates

Nanowire contact printing on planar substrates enables large scale nanomaterial assembly with a convenient and reliable route, which is compatible with a batch-to-batch process. Uniquely, the NW growth (i.e., donor) substrate can be made cylindrical, such as a glass drum, suggesting the feasibility of a potential roll-to-roll compatible NW printing scheme. We have recently shown the use of cylindrical growth substrates for *differential roll printing* (DRP) of NWs, which is a highly scalable process.[21] As shown schematically in Fig. 4.14*A*, the DRP approach utilizes a roller with NWs grown by the VLS/VSS process on its outer surface.[21] The roller is then connected to a pair of wheels and is then rolled on a stationary receiver substrate.[21] Because the wheels on the ends of the roller have a larger diameter than the roller itself, they produce lateral sliding (i.e., shear force) at roller-receiver substrate contact, coupled with a cyclic rotation.[21] This combinational motion results in the directional and aligned transfer of the as-grown NWs from the donor roller to a receiver substrate. This approach reduces the contact area between the donor and receiver substrates because the cylindrical donor substrate rolls over the receiver substrate with only a small tangent contact area consisting of fresh NWs at any given time.[21] This is highly beneficial for printing large areas that would otherwise require large planar growth substrates and long contact-sliding distances. On the other hand, the roller can be repetitively used for the NW growth, which is important for a low-cost roll-to-roll process. And because single-crystalline semiconductor NWs can be grown at relatively low temperature, such as 285°C for Ge NWs,[20] as compared to that for bulk crystalline materials, the choice of the roller material is greatly relaxed such that glass, quartz, or stainless steel tubes with proper radius can be used.[21]

The ability to assemble crystalline semiconductor NW arrays on various substrate materials is of great interest for many technological applications. Because the NW printing is performed at ambient temperatures, the process is highly compatible with a wide range of receiver substrates materials, including those with limited thermal compatibility. For example, as shown in Fig. 4.14, semiconductor NW

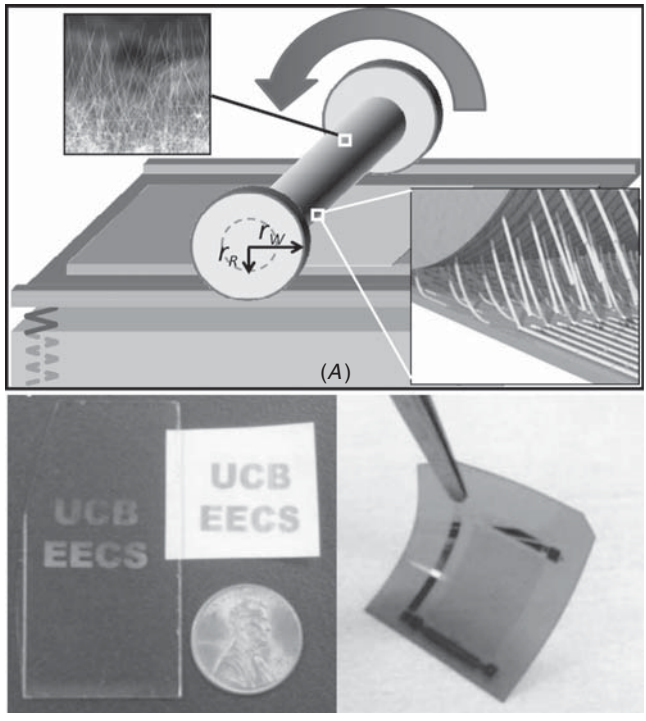


Figure 4.14 NW contact printing involving cylindrical growth (donor) and nonconventional (receiver) substrates. (*A*) Process schematic. The SEM images in the insets show that the grown Ge NWs are randomly oriented on the growth substrate, resembling a forest. The NWs are then aligned and transferred to the receiver substrate by application of a directional shear force, resulting in the printing of submonolayer NW parallel arrays on the receiver substrate. Images are not to scale. Reproduced with permission from Ref. 74. Copyright 2008, 2009 Wiley InterScience. (*B*) Glass and photographic paper. (*C*) Mechanically flexible Kapton plastic. Reproduced with permission from Ref. 21. Copyright 2007 American Physical Society.

arrays were successfully printed on a rigid glass substrate, mechanically bendable paper (Fig. 4.14*B*) and plastic (Fig. 4.14*C*) substrates.[21] An essential requirement for the successful printing of aligned NW arrays, however, is to utilize high-quality NW growth substrates, consisting of high NW density ($\sim$>5 NWs/μm) with near vertical alignment, and free of contaminant and dust particles. When the density of NWs on the growth substrate is relatively low, the grown non-epitaxial NWs mostly exhibit nonvertical orientation because of the less steric forces between the NWs, resulting in poor NW printing outcome (e.g., poor alignment and density).

4.5 Printable Nanowire Arrays for Electronics, Optoelectronics, and Sensors

To date, a broad range of semiconductor materials, including Si, Ge, GaAs, GaN, InAs, CdSe, and ZnO, have been fabricated into nanowire structures.[8,19,20,30,49,50,53,68–73] Because of their unique physical properties, including high carrier mobility, proper direct bandgap, large exciton binding energy, and high surface-to-volume ratio, they have potential applications for electronics, sensing, and energy conversion. NW contact/roll printing provides a practical route toward these technological applications.[8,19–21,44,74] In fact, printed NW arrays can be readily fabricated into functional devices such as transistors,[8,20,21,44] diodes,[20] photodetectors,[8] and gas sensors.[75] The performance of these devices can be controlled by choosing appropriate materials and desired printing channel width and NW density. In the following sections, recent work on fabrication and characterization of these functional devices with printed NW arrays is introduced. Furthermore, the concept-proof all-NW sensory circuitry is also discussed.

4.5.1 Nanowire Parallel Arrays for Electronics

A transistor is one of the fundamental building blocks of integrated circuits. A NW transistor can be simply fabricated by placing source and drain metal contacts on the two ends of a single semiconductor NW, with either a buried bottom gate or fabricated top gate. The same fabrication scheme can be applied to a parallel-array NW transistor, in which a printed NW array is used as the active channel. Figure 4.15*A* shows three SEM images of printed core/shell Ge/Si (~15/

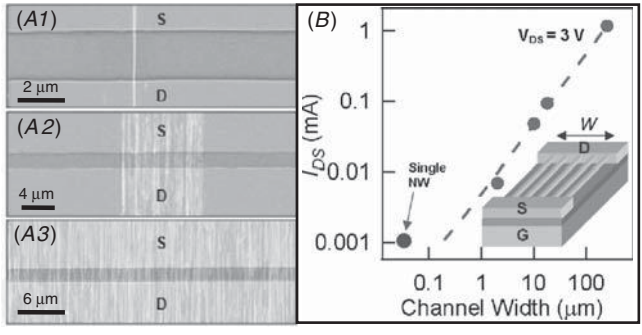


Figure 4.15 Printing NW arrays for electronics. (*A*) From top to bottom, SEM images of a back-gated single NW FET and 10-mm- and 250-mm-wide parallel-arrayed NW FETs. High-mobility Ge/Si (15/5 nm) NWs were used as the channel material. (*B*) ON current as a function of channel width scaling, showing a highly linear trend. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

5 nm) NW arrays configured as back-gated FETs.[20] In these cases, the channel width ranges from a single NW (~30 nm) up to ~250 μm with a fixed channel length of ~2 μm. Note that only the NWs that directly cross the S/D electrodes contribute to the current because there is nearly no NW-NW electrical contact. The average ON current of the fabricated NW FETs linearly scales with the channel width with a slope of ~5 μA/μm,[20] as shown in Fig. 4.15*B*, corresponding to ~5 NW/μm, as a single Ge/Si NW typically delivers ~1 μA/NW in an un-optimized back-gated geometry. This result suggests a uniform NW assembly with a consistent average density on large areas and demonstrates the versatility of the contact printing process for circuit integration of NW device arrays with tunable performance.

The fact that NW printing is a generic process allows assembly of a wide range of NW materials with tunable atomic composition. Therefore, desired materials can be chosen for the designed functionality. For example, high-electron-mobility (μ_n>2000 cm^2/Vs) InAs NWs were printed as the channel material for high-performance transistors, capable of delivering high ON currents.[19] As schematically shown in Fig. 4.16*A*, a FET consisting of an array of printed InAs NWs with a global back-gate geometry can be fabricated. A typical device with $W \sim 200$ μm, $L \sim 3$ μm, and SiO_2 gate dielectric ~ 50 nm can deliver $I_{on} \sim 6$ mA at $V_{DS} = 3$ V, as shown in Fig. 4.16*B*. This corresponds to ~15 μA per NW (~400 NWs bridging S/D).[19]

Carrier field-effect mobility is an important figure of merit of a long-channel FET device as it directly determines the frequency range that the device can be operated. For a typical InAs NW array device, the transconductance g_m was obtained from the $I_{DS} - V_{GS}$ curve for $V_{DS} = 0.1$ V (Fig. 4.16*C*) and the standard square law model $\mu_n = (g_m L^2)/(C_{ox} V_{DS})$ was used to calculate the field-effect mobility, where C_{ox} is the gate oxide capacitance.[19] By multiplying the electrostatically modeled gate oxide capacitance for a single InAs NW ($C_{oxNW} \sim 0.16 \times 10^{-15}$ F, assuming an average NW diameter of ~27 nm and $L = 3$ μm) by the number of NWs in the array FET (~400), $C_{ox} = 6.49 \times 10^{-14}$ F is obtained. From the transfer characteristics and the calculated C_{ox}, a peak field-effect carrier mobility of $\mu_n = 587$ cm^2/Vs (Fig. 4.16*D*) is extracted.[19] The field-effect mobilities reported here are much higher than those of organic semiconductors and amorphous Si, which are typically on the order of ~1 cm^2/Vs.[76,77] This clearly demonstrates the distinct advantage of using crystalline inorganic materials as the channel material for high-performance printable electronic devices.

Printed NW arrays were also configured as diodes by using asymmetric metal contacts.[20] Although axial p-n junction NWs grown with VLS process and in situ doping have been achieved by a number of research groups,[78,79]and these NWs can be printed for NW array p-n junction diodes, such a Schottky diode configuration greatly reduces the complexity of material growth and device fabrication process.

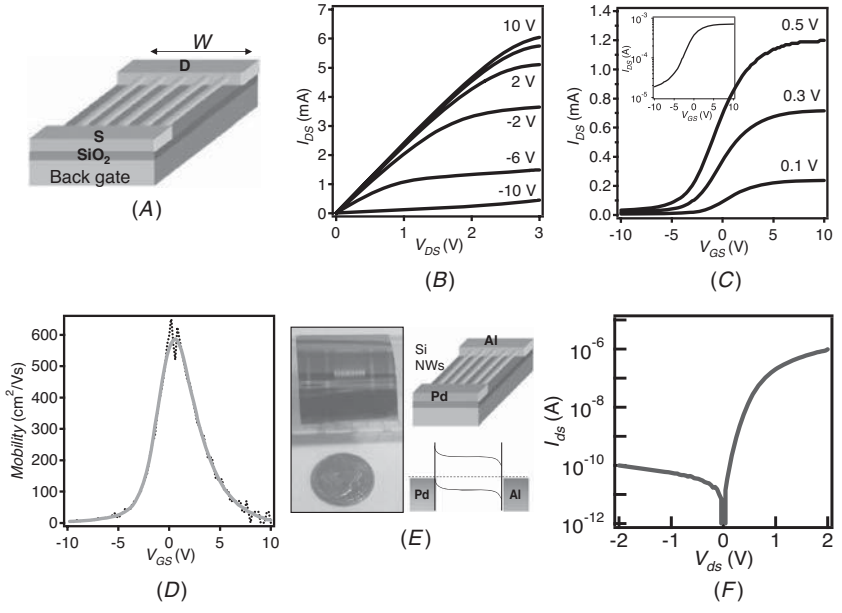


Figure 4.16 Printing NW arrays for high-performance electronics. (*A*) Schematic of a FET consisting of an array of printed InAs NWs with a global back-gate geometry. (*B*) Output characteristics of a representative InAs NW FET with $W \sim 200$ μm ($\sim$400 NWs bridging S/D) and $L \sim 3$ μm. (*C*) Linear-scale transfer characteristics of the same device at $V_{DS} = 0.1$, 0.3, and 0.5 V; the inset shows the log-scale I_{DS}-V_{GS} curve for $V_{DS} = 0.3$ V. (*D*) Field-effect mobility–V_{GS} curve extracted using low-bias ($V_{DS} = 0.1$ V) transconductance and the standard square-law model. The curve corresponds to the same array FET with electrical characteristics shown in (*A–C*). Reproduced with permission from Ref. 19. Copyright 2008 Springer. (*E*) Optical photograph and schematic of a novel diode structure fabricated on parallel arrays of p-SiNWs on a flexible plastic substrate. Asymmetric Pd-Al contacts are used to obtain Schottky diodes with the Pd forming a near-ohmic contact to the valence band and Al resulting in a Schottky interface. (*F*) *I-V* characteristic of a representative SiNW Schottky diode with a channel width ~ 250 μm and length ~ 3 μm. Reproduced with permission from Ref. 20. Copyright 2008 American Chemical Society.

Particularly in our work, printed Si NW arrays were configured as Schottky diodes by using asymmetric Pd/Al S/D contacts on mechanically flexible Kapton substrates (Fig. 4.16*E*).[20] In this structure, the high-work-function Pd metal forms a near ohmic to the p-SiNWs, whereas low-work-function Al results in a Schottky contact.[20] No thermal annealing is applied after the metallization of the S/D contacts in order to prevent interface diffusion and alloying. As a result, Schottky diodes are enabled without the use of dopant profiling (for example, p-n junctions). The fabricated diodes exhibit highly rectifying behavior with $\sim$4 orders of magnitude higher forward than reverse currents (Fig. 4.16*F*).[20] This presents a simple, low-temperature processing

route for the fabrication of rectifiers on plastic substrates, with important practical implications.

4.5.2 Nanowire Parallel-Array Gas Sensors

Semiconductor NWs are ideal candidates for chemical and biological sensing mainly because of their large surface-to-volume ratio and chemically active surfaces, and their tunable carrier concentration and radii comparable to the Debye screening length; thus, channel conductance is extremely sensitive to surface electrostatic perturbation caused by molecular absorption.[2,80,81] However, device-to-device variation of response is a challenge owing to the small surface area of the NWs. In that regard, the use of NW parallel arrays significantly decreases device variations by an averaging effect. To date, researchers have developed a wide range of chemical and biological sensors based on single and arrayed NWs. Some of them have demonstrated higher detection sensitivity than their thin-film counterparts.[13,82] To demonstrate the potency of printed NW arrays for large-area sensor integration, as schematically shown in Fig. 4.17*A*, lightly p-type doped SiNWs were printed on Si/SiO_2 substrates, and two-terminal devices with Ni silicide contacts were fabricated for gas sensing.[75] To render

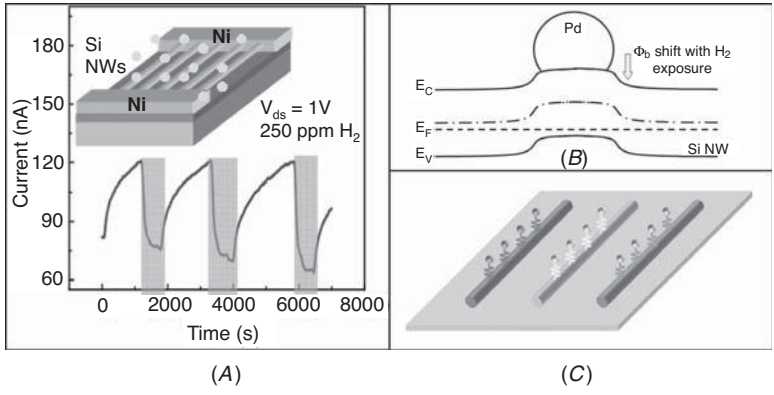


Figure 4.17 NW parallel arrays for gas sensors on Si substrates. (*A*) The current output response of a two-terminal device fabricated on a printed p-Si NW array with Ni metal contacts as a function of exposure cycles to 250 ppm hydrogen (in dry air). The inset shows the schematic of a sensor device. To induce the H_2 sensitivity, Pd nanoparticles are formed on the surface of Si NWs by thin-film evaporation of Pd. (*B*) Qualitative band diagram, showing the effect of Pd nanoparticles on the local band diagram of Si NWs. On H_2 exposure, the work function of Pd nanoparticles is reduced, therefore changing the NW band bending such that the hole-carrier concentration is locally depleted. (*C*) Schematic of an envisioned sensor array, consisting of three different types of NWs sensitive to different chemical species. Reproduced with permission from Ref. 74. Copyright 2009 Wiley InterScience.

the NWs with sensitivity to H_2, ~2-nm-thick Pd film was deposited on the printed NW array, resulting in the formation of Pd nanoclusters on the NW surfaces (Fig. 4.17*A*).[75] Before H_2 exposure, the high work function Pd nanoclusters cause energy band bends upward locally which enhances the hole transport in the NW channel, as shown in Fig. 4.17*B*. On H_2 exposure, formation of PdH_x results in decrease of work function of Pd and downward bending of the energy band, resulting in local depletion of hole-carrier concentration.[75] Consequently, as shown in Fig. 4.17*A*, the conductance of the SiNW array shows a strong dependence on the H_2 exposure, even at relatively low concentrations (e.g., 250 ppm).[75]

It is crucial in many applications for a sensing device to be able to distinguish certain species and measure its concentration from the environment.[83] To achieve this reliably, multiple sensors need to be integrated together to function as a smart sensor. In fact, as a biomimetic device, a smart sensor that can distinguish multiple species is also called an electronic nose. The implementation of the electronic nose usually relies on sensor integration, signal processing, and pattern recognition. It is worth noting that the NW printing method may provide a viable route toward the realization of electronic noses and smart sensors, capable of distinguishing chemical species while determining their concentrations. The sensor components of such a "nose" may be envisioned through a heterogeneous integration of different sensor NW materials, or NWs with different surface functionalization (Fig. 4.17*C*) interfaced with signal processing function. According to Section 4.4.4, this sensing NW array can be readily achieved through a multistep NW printing process.

4.5.3 Toward All-Nanowire Integrated Sensor Circuitry

The ability to fabricate a wide range of electronic and sensor devices, with different functionalities, based on printed NW arrays enables the exploration of heterogeneous NW circuitry. To examine this feasibility, proof-of-concept circuits are fabricated that incorporate NW sensors and transistors to enable on-chip integration of optical sensing and signal amplification.[8]The layout of an individual all-NW circuit is shown in Fig. 4.18*A*. Each individual NW circuit consists of three active device components: (i) an optical nanosensor (NS) based on either a single or parallel arrays of CdSe NWs, (ii) a small FET (T1) based on parallel arrays of 1–5 Ge/Si core/shell NWs, and (iii) a low-resistance buffer FET (T2) with the channel consisting of parallel arrays of ~2000 Ge/Si NWs.[8] The circuitry utilizes T1 to match the output impedance of the NS in a voltage divider configuration to translate the illumination-dependent NS current into potential V_{G2}. Then, the output current of T2 is modulated based on its transfer characteristics resulting in ~5 orders of magnitude amplification of the NS current signal.[8]

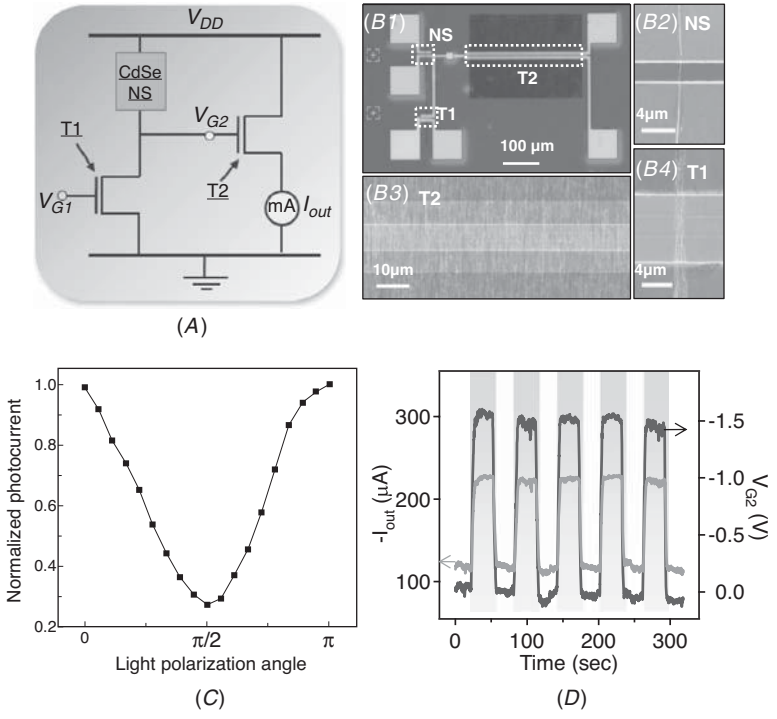


Figure 4.18 Heterogeneous NW assembly for an all-integrated, sensor circuitry. (*A*) Circuit diagram for the all-nanowire photodetector, with high-mobility Ge/Si NW FETs (T1 and T2) amplifying the photoresponse of a CdSe nanosensor. (*B1*) An optical image of the fabricated NW circuitry, consisting of a CdSe nanosensor [NS (*B2*)] and two Ge/Si core/shell NW FETs [T2 and T1, (*B3*) and (*B4*)] with channel widths ~ 300 mm and 1 mm, respectively. Each device element within the circuit can be independently addressed for dynamics studies and circuit debugging. (*C*) Polarization-dependent photoconduction measurement for parallel arrays of aligned CdSe NWs (~40 NWs) assembled by contact printing. (*D*) Circuit output current (blue curve) and voltage divider output voltage (gray curve) response to light illumination (4.4 mW/cm^2). Reproduced with permission from Ref. 8. Copyright 2008 National Academy of Sciences.

In order to fabricate the circuitry, first, uniformly and regularly aligned CdSe and Ge/Si NW arrays are assembled at predefined locations on a Si/SiO_2 (50 nm, thermally grown) substrate by using a two-step NW printing process.[8] Then, Ni/Pd S/D electrodes are deposited on NW arrays, followed by atomic-layer deposition of ~8-nm-thick HfO_2 film as the high-κ gate dielectric. Next, the HfO_2 layer is selectively etched at the bonding pads and vias. Finally, the top gate electrodes (Ni/Pd) are patterned on Ge/Si NWs, and then the vias are formed between the two metal layers at the same time.[8] Figure 4.18*B*

shows an optical image of a fabricated circuit and SEM images of each individual element, clearly showing the highly ordered NW positioning and the on-chip integration. In this study, the high degree of NW alignment without NW bundling and uncontrolled overlap is essential for high-performance and highly uniform transistor and sensor arrays, without any significant circuit-to-circuit output variation.

Importantly, for CdSe optical sensors, the alignment is not only crucial for uniform response of the devices, but also more uniquely to enable well-defined polarized sensitivity, which arises from the 1D nature of NWs.[8] The polarization dependent photoconduction measurements of parallel arrays of CdSe NWs are shown in Fig. 4.18*C*.[8] Specifically, a nearly identical polarization-dependent response is observed for various printed CdSe NW devices with similar minimum and maximum polarization angles, which further illustrates the highly aligned assembly of NWs by contact printing. This is in distinct contrast to the randomly aligned NWs assembled by the drop-casting method, which show different polarized responses depending on the orientation of the particular wire.[8]

Moreover, time-resolved photoresponse measurements were performed for several illumination cycles, as depicted in Fig. 4.18*D*, illustrating average dark and light currents of ~80 mA and ~300 mA, respectively.[8] For circuit-level operation, the operating bias V_{DD} is maintained at –3 V for all measurements while the gate electrode for T1 is biased at $V_{G1} = 3$ V (corresponding to $R_{T1} = 1$–2 GΩ) to match the output impedance of the CdSe NS.[8] The output current is quantitatively matched, with the value estimated based on the circuit layout and the electrical properties of the single-device components. For example, the output current of the circuit can be approximated from the transfer characteristics of T2 and the output voltage of the voltage divider, which is also the input to T2. The output of the voltage divider, V_{G2} can be estimated as $V_{G2} = V_{DD} \times R_{T1}/(R_{T1} + R_{NS})$, corresponding to $V_{G2} \sim -0.02$V and –1.11V for dark and light ($R_{NS\text{-dark}} \sim$ 140 GΩ and $R_{NS\text{-light}} \sim 2$ GΩ) scenarios.[8] The V_{G2} swing defines the operation regime of T2, and this operation regime corresponds to an output current swing of 87–310 mA, which is in good agreement with the measurements.[8]

Further extending the concept of large-scale heterogeneous integration of parallel NW array circuitry, large arrays (i.e., 13 × 20) of the all-nanowire circuits were fabricated on a chip and demonstrated as a proof-of-concept imager (Fig. 4.19*A*).[8] Each circuit component in the array operates as a single pixel with an observed functional pixel yield of ~80% in this study.[8] The majority of failure elements are caused by the materials and processing issues such as defective NWs and fabrication failures (Fig. 4.19*B*).[8] The functional pixels exhibited an average photocurrent of ~420 mA with a standard deviation of ~165 mA. This reasonably small circuit-to-circuit variation is due to the uniformity

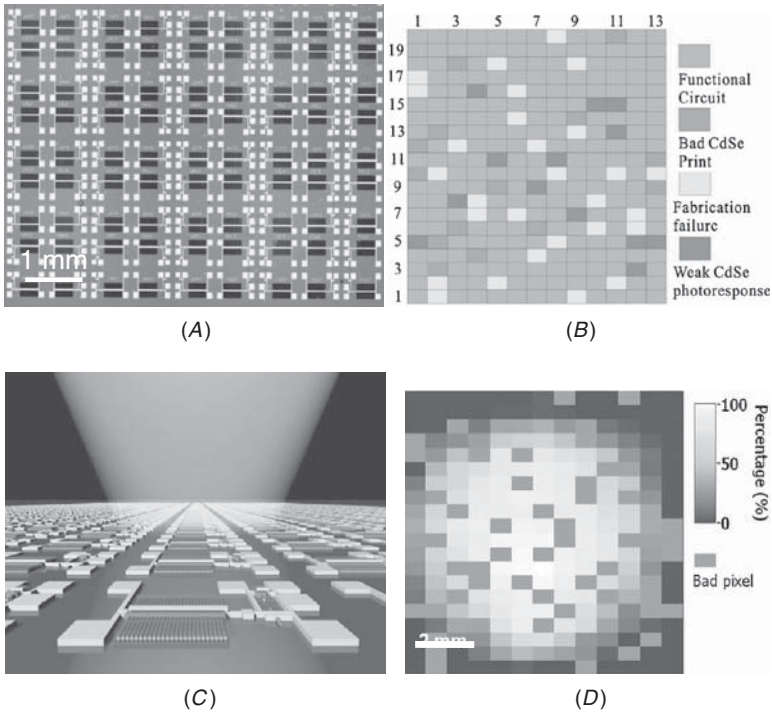


Figure 4.19 Large-scale and heterogeneous integration of NWs for a proof-of-concept image sensing. (*A*) Optical image of an array of all-nanowire photodetector circuitry with each circuit element serving as an independently addressable pixel. (*B*) A defect analysis map showing the functional and defective NW photodetector circuit elements. (*C*) A perspective picture showing the imaging function of the circuit array. (*D*) An output response of the circuit array, imaging a circular light spot. The contrast represents the normalized photocurrent. Reproduced with permission from Refs. 8 and 74. Copyright 2008 National Academy of Sciences, 2009 Wiley InterScience.

of the assembled nanowire arrays, which demonstrates the potency of the NW printing technology for system integration.

To illustrate the image sensing functionality of the all-NW circuit array, a halogen light source is projected and focused onto the center of the array matrix (Fig. 4.19*C*), and the photoresponse of each individual circuit element is measured. The output current is characterized for each individual working circuit and digitized into a 0–100 scale with "0" and "100" representing the minimum and maximum measured intensities, respectively.[8] The recorded intensity level of each circuit is incorporated into a 2D contour plot to generate a contrast map (Fig. 4.19*D*). The contour map shows the spatial intensity variation clearly from the center to the outer edge of the circuit matrix,

and this matches the intensity profile of the projected circular light pattern.[8] This work not only demonstrates NW device integration at an unprecedented scale, but also illustrates and presents a novel platform based on printed NW arrays that may enable a number of technological applications, utilizing NWs as the building blocks, that are unattainable with conventional fabrication processing methods.

4.6 Conclusion and Outlook

NWs are a novel class of synthetic electronic materials that can be readily configured as various device elements with desired functionality on both rigid and mechanically flexible substrates. Although they may present an optimal structure for future nanoscale, gate-all-around MOSFETs, they may more uniquely enable new technological applications through integration with nonconventional substrates in a format of roll-to-roll printable NW electronics and sensors (Fig. 4.20). Their low-temperature processing enables the fabrication of high-performance, heterogeneous integrated circuits. Although significant progress has been made in their synthesis and processing, it remains to be seen whether they can be incorporated into fully integrated circuits with high large-area uniformity and large degrees of complexity. However, to date, simple circuit elements on large areas have shown their versatility and potential for use in large-scale integrated circuits.

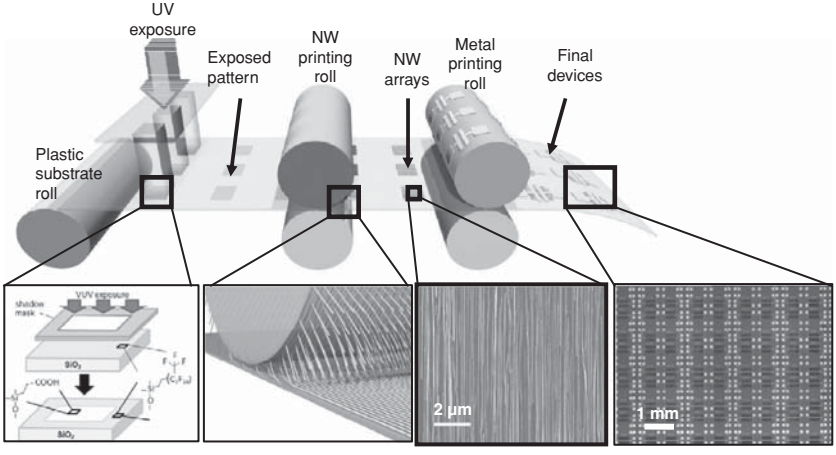


Figure 4.20 Schematic of an envisioned roll-to-roll printable NW electronics and sensors fabrication. The process involves fluorinated monolayer patterning of the receiver substrate to define "sticky" and "nonsticky" regions for the subsequent patterned transfer and assembly of NWs by contact printing. Following the printing of NW active components, devices are fabricated by defining the source/drain and gate electrodes. Reproduced with permission from Ref. 74. Copyright 2009 Wiley InterScience.

Acknowledgments

This work was financially supported by DARPA, Intel Corporation, MARCO/MSD Focus Center Research Program, NSF COINS, Berkeley Sensor and Actuator Center, and Lawrence Berkeley National Laboratory. All fabrication was performed at the UC Berkeley Microlab facility.

References

1. R. F. Service, "Materials science: is silicon's reign nearing its end?" *Science,* vol. 323, pp. 1000-1002, 2009.
2. Z. Y. Fan and J. G. Lu, "Gate-refreshable nanowire chemical sensors," *Applied Physics Letters,* vol. 86, pp. 123510, 2005.
3. Y. Cui, Q. Q. Wei, H. K. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science,* vol. 293, pp. 1289-1292, 2001.
4. E. Rossinyol, J. Arbiol, F. Peiro, A. Cornet, J. R. Morante, B. Tian, et al., "Nanostructured metal oxides synthesized by hard template method for gas sensing applications," *Sensors and Actuators B—Chemical,* vol. 109, pp. 57-63, 2005.
5. Z. L. Wang, R. P. Gao, Z. W. Pan, and Z. R. Dai, "Nano-scale mechanics of nanotubes, nanowires, and nanobelts," *Advanced Engineering Materials,* vol. 3, pp. 657-661, 2001.
6. C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, et al., "Nanowire-based one-dimensional electronics," *Materials Today,* vol. 9, pp. 28-35, 2006.
7. Y. G. Sun, D. Y. Khang, F. Hua, K. Hurley, R. G. Nuzzo, and J. A. Rogers, "Photolithographic route to the fabrication of micro/nanowires of III-V semiconductors," *Advanced Functional Materials,* vol. 15, pp. 30-40, 2005.
8. Z. Y. Fan, J. C. Ho, Z. A. Jacobson, H. Razavi, and A. Javey, "Large-scale, heterogeneous integration of nanowire arrays for image sensor circuitry," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 105, pp. 11066-11070, 2008.
9. R. Tu, L. Zhang, Y. Nishi, and H. J. Dai, "Measuring the capacitance of individual semiconductor nanowires for carrier mobility assessment," *Nano Letters,* vol. 7, pp. 1561-1565, 2007.
10. J. Hahm and C. M. Lieber, "Direct ultrasensitive electrical detection of DNA and DNA sequence variations using nanowire nanosensors," *Nano Letters* vol. 4, pp. 51-54, 2004.
11. W. U. Wang, C. Chen, K. H. Lin, Y. Fang, and C. M. Lieber, "Label-free detection of small-molecule-protein interactions by using nanowire nanosensors," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 102, pp. 3208-3212, 2005.
12. G. F. Zheng, F. Patolsky, Y. Cui, W. U. Wang, and C. M. Lieber, "Multiplexed electrical detection of cancer markers with nanowire sensor arrays," *Nature Biotechnology,* vol. 23, pp. 1294-1301, 2005.
13. D. H. Zhang, Z. Q. Liu, C. Li, T. Tang, X. L. Liu, S. Han, et al., "Detection of NO_2 down to ppb levels using individual and multiple In_2O_3 nanowire devices," *Nano Letters,* vol. 4, pp. 1919-1924, 2004.
14. Z. Y. Fan, H. Razavi, J. W. Do, A. Moriwaki, O. Ergen, Y. L. Chueh, et al., "Three-dimensional nanopillar-array photovoltaics on low-cost and flexible substrates," *Nature Materials,* vol. 8, pp. 648-653, 2009.
15. J. H. Song, X. D. Wang, E. Riedo, and Z. L. Wang, "Elastic property of vertically aligned nanowires," *Nano Letters,* vol. 5, pp. 1954-1958, 2005.

16. Y. H. Huang, Y. Zhang, X. Q. Wang, X. D. Bai, Y. S. Gu, X. Q. Yan, et al., "Size independence and doping dependence of bending modulus in ZnO nanowires," *Crystal Growth & Design,* vol. 9, pp. 1640-1642, 2009.
17. A. J. Baca, J. H. Ahn, Y. Sun, M. A. Meitl, E. Menard, H. S. Kim, et al., "Semiconductor wires and ribbons for high-performance flexible electronics," *Angewandte Chemie International Edition,* vol. 47, pp. 5524-5542, 2008.
18. Y. G. Sun, H. S. Kim, E. Menard, S. Kim, I. Adesida, and J. A. Rogers, "Printed arrays of aligned GaAs wires for flexible transistors, diodes, and circuits on plastic substrates," *Small,* vol. 2, pp. 1330-1334, 2006.
19. A. C. Ford, J. C. Ho, Z. Fan, O. Ergen, V. Altoe, S. Aloni, et al., "Synthesis, contact printing, and device characterization of Ni-catalyzed, crystalline InAs nanowires," *Nano Research,* vol. 1, p. 32, 2008.
20. Z. Y. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, et al., "Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing," *Nano Letters,* vol. 8, pp. 20-25, 2008.
21. R. Yerushalmi, Z. A. Jacobson, J. C. Ho, Z. Fan, and A. Javey, "Large scale, highly ordered assembly of nanowire parallel arrays by differential roll printing," *Applied Physics Letters,* vol. 91, pp. 203104, 2007.
22. M. C. McAlpine, H. Ahmad, D. Wang, and J. R. Heath, "Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors," *Nature Materials,* vol. 6, pp. 379-384, 2007.
23. R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of crystal growth," *Applied Physics Letters,* vol. 4, pp. 89-90, 1964.
24. E. I. Givargizov, "Fundamental aspects of VLS growth," *Journal of Crystal Growth,* vol. 31, pp. 20-30, 1975.
25. Y. Y. Wu and P. D. Yang, "Direct observation of vapor-liquid-solid nanowire growth," *Journal of the American Chemical Society,* vol. 123, pp. 3165-3166, 2001.
26. C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bulletin,* vol. 32, pp. 99-108, 2007.
27. J. Xiang, W. Lu, Y. J. Hu, Y. Wu, H. Yan, and C. M. Lieber. "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature,* vol. 441, pp. 489-493, 2006.
28. F. Qian, S. Gradecak, Y. Li, C. Y. Wen, and C. M. Lieber, "Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes," *Nano Letters,* vol. 5, pp. 2287-2291, 2005.
29. X. F. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, "Single-nanowire electrically driven lasers. *Nature,* vol. 421, pp. 241-245, 2003.
30. Z. H. Zhong, F. Qian, D. L. Wang, and C. M. Lieber, "Synthesis of p-type gallium nitride nanowires for electronic and photonic nanodevices," *Nano Letters,* vol. 3, pp. 343-346, 2003.
31. X. F. Duan, Y. Huang, Y. Cui, J. F. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature,* vol. 409, pp. 66-69, 2001.
32. S. N. Mohammad, "For nanowire growth, vapor-solid-solid (vapor-solid) mechanism is actually vapor-quasisolid-solid (vapor-quasiliquid-solid) mechanism," *Journal of Chemical Physics,* vol. 131, 224702, 2009.
33. Y. W. Wang, V. Schmidt, S. Senz, and U. Gosele, "Epitaxial growth of silicon nanowires using an aluminium catalyst," *Nature Nanotechnology,* vol. 1, pp. 186-189, 2006.
34. G. F. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Advanced Materials,* vol. 16, pp. 1890-1893, 2004.
35. A. B. Greytak, L. J. Lauhon, M. S. Gudiksen, and C. M. Lieber, "Growth and transport properties of complementary germanium nanowire field-effect transistors," *Applied Physics Letters,* vol. 84, pp. 4176-4178, 2004.
36. P. C. Chang, Z. Fan, C. J. Chien, D. Stichtenoth, C. Ronning, and J. G. Lu, "High-performance ZnO nanowire field effect transistors," *Applied Physics Letters,* vol. 89, pp. 133113, 2006.

37. Z. Y. Fan and J. G. Lu, "Zinc oxide nanostructures: synthesis and properties," *Journal of Nanoscience and Nanotechnology,* vol. 5, pp. 1561-1573, 2005.
38. J. S. Jie, W. J. Zhang, Y. Jiang, X. M. Meng, Y. Q. Li, and S. T. Lee, "Photoconductive characteristics of single-crystal CdS nanoribbons," *Nano Letters,* vol. 6, pp. 1887-1892, 2006.
39. C. Li, D. H. Zhang, S. Han, X. L. Liu, T. Tang, and C. W. Zhou, "Diameter-controlled growth of single-crystalline In_2O_3 nanowires and their electronic properties," *Advanced Materials,* vol. 15, pp. 143-146, 2003.
40. L. Dai, X. L. Chen, J. K. Jian, M. He, T. Zhou, and B. Q. Hu, "Fabrication and characterization of In_2O_3 nanowires," *Applied Physics A—Materials,* vol. 75, pp. 687-689, 2002.
41. H. Ko, J. Lee, B. E. Schubert, Y. Chueh, P. W. Leu, R. S. Fearing, et al., "Hybrid core-shell nanowire forests as self-selective chemical connectors," *Nano Letters,* vol. 9, pp. 2054-2058, 2009.
42. A. I. Hochbaum, R. Fan, R. R. He, and P. D. Yang, "Controlled growth of Si nanowire arrays for device integration," *Nano Letters,* vol. 5, pp. 457-460, 2005.
43. T. Martensson, M. Borgstrom, W. Seifert, B. J. Ohlsson, and L. Samuelson, "Fabrication of individually seeded nanowire arrays by vapour-liquid-solid growth," *Nanotechnology,* vol. 14, pp. 1255-1258, 2003.
44. T. Takahashi, K. Takei, J. C. Ho, Y. L. Chueh, Z. Fan, and A. Javey, "Monolayer resist for patterned contact printing of aligned nanowire arrays," *Journal of the American Chemical Society,* vol. 131, pp. 2102-2103, 2009.
45. T. Martensson, C. P. T. Svensson, B. A. Wacaser, M. W. Larsson, W. Seifert, K. Deppert, et al., "Epitaxial III-V nanowires on silicon," *Nano Letters,* vol. 4, pp. 1987-1990, 2004.
46. P. C. Chang, Z. Y. Fan, D. W. Wang, W. Y. Tseng, W. A. Chiou, J. Hong, et al., "ZnO nanowires synthesized by vapor trapping CVD method," *Chemistry of Materials,* vol. 16, pp. 5133-5137, 2004.
47. W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, "One-dimensional hole gas in germanium/silicon nanowire heterostructures," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 102, pp. 10046-10051, 2005.
48. A. C. Ford, J. C. Ho, Y. L. Chueh, Y. C. Tseng, Z. Y. Fan, J. Guo, et al., "Diameter-dependent electron mobility of InAs nanowires," *Nano Letters,* vol. 9, pp. 360-365, 2009.
49. P. D. Yang, H. Q. Yan, S. Mao, R. Russo, J. Johnson, R. Saykally, et al., "Controlled growth of ZnO nanowires and their optical properties," *Advanced Functional Materials,* vol. 12, pp. 323-331, 2002.
50. J. H. He, J. H. Hsu, C. W. Wang, H. N. Lin, L. J. Chen, and Z. L. Wang, "Pattern and feature designed growth of ZnO nanowire arrays for vertical devices," *Journal of Physical Chemistry B,* vol. 110, pp. 50-53, 2006.
51. M. T. Borgstrom, G. Immink, B. Ketelaars, R. Algra, and E. P. A. M. Bakkers, "Synergetic nanowire growth," *Nature Nanotechnology,* vol. 2, pp. 541-544, 2007.
52. V. Gottschalch, G. Wagner, J. Bauer, H. Paetzelt, and M. Shirnow, "VLS growth of GaN nanowires on various substrates," *Journal of Crystal Growth,* vol. 310, pp. 5123-5128, 2008.
53. T. Bryllert, L. E. Wernersson, L. E. Froberg, and L. Samuelson, "Vertical high-mobility wrap-gated InAs nanowire transistor," *IEEE Electron Device Letters,* vol. 27, pp. 323-325, 2006.
54. C. Thelander, C. Rehnstedt, L. E. Froberg, E. Lind, T. Martensson, P. Caroff, et al., "Development of a vertical wrap-gated InAs FET," *IEEE Transactions on Electron Devices,* vol. 55, pp. 3030-3036, 2008.
55. Y. Huang, X. F. Duan, Q. Q. Wei, and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science,* vol. 291, pp. 630-633, 2001.
56. C. Yan, T. Zhang, and P. S. Lee, "Flow assisted synthesis of highly ordered silica nanowire arrays," *Applied Physics A—Materials,* vol. 94, pp. 763-766, 2009.

57. C. Y. Geng, Y. Jiang, Y. Yao, X. M. Meng, J. A. Zapien, C. S. Lee, et al., "Well-aligned ZnO nanowire arrays fabricated on silicon substrates," *Advanced Functional Materials,* vol. 14, pp. 589-594, 2004.
58. X. F. Duan, C. M. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, et al., "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature* vol. 425, pp. 274-278, 2003.
59. P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, et al., "Electric-field assisted assembly and alignment of metallic nanowires," *Applied Physics Letters,* vol. 77, pp. 1399-1401, 2000.
60. L. F. Dong, J. Bush, V. Chirayos, R. Solanki, and J. Jiao, "Dielectrophoretically controlled fabrication of single-crystal nickel silicide nanowire interconnects," *Nano Letters,* vol. 5, pp. 2112-2115, 2005.
61. Y. Cao, W. Liu, J. L. Sun, Y. P. Han, J. H. Zhang, S. Liu, et al., "A technique for controlling the alignment of silver nanowires with an electric field," *Nanotechnology,* vol. 17, pp. 2378-2380, 2006.
62. O. Englander, D. Christensen, J. Kim, L. W. Lin, and S. J. S. Morris, "Electric-field assisted growth and self-assembly of intrinsic silicon nanowires," *Nano Letters,* vol. 5, pp. 705-708, 2005.
63. T. J. Morrow, M. W. Li, J. Kim, T. S. Mayer, and C. D. Keating, "Programmed assembly of DNA-coated nanowire devices," *Science,* vol. 323, pp. 352-352, 2009.
64. R. Yerushalmi, J. C. Ho, Z. A. Jacobson, and A. Javey, "Generic nanomaterial positioning by carrier and stationary phase design," *Nano Letters,* vol. 7, pp. 2764-2768, 2007.
65. S. Jin, D. M. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu, and C. M. Lieber, "Scalable interconnection and integration of nanowire devices without registration," *Nano Letters,* vol. 4, pp. 915-919, 2004.
66. A. Tao, F. Kim, C. Hess, J. Goldberger, R. R. He, Y. G. Sun, et al., "Langmuir-Blodgett silver nanowire monolayers for molecular sensing using surface-enhanced Raman spectroscopy," *Nano Letters,* vol. 3, pp. 1229-1233, 2003.
67. X. L. Li, L. Zhang, X. R. Wang, I. Shimoyama, X. M. Sun, W. S. Seo, et al., "Langmuir-Blodgett assembly of densely aligned single-walled carbon nanotubes from bulk materials," *Journal of the American Chemical Society,* vol. 129, pp. 4890-4891, 2007.
68. C. K. Chan, H. L. Peng, G. Liu, K. McIlwrath, X. F. Zhang, R. A. Huggins, et al., "High-performance lithium battery anodes using silicon nanowires," *Nature Nanotechnology,* vol. 3, pp. 31-35, 2008.
69. A. I. Hochbaum, R. K. Chen, R. D. Delgado, W. J. Liang, E. C. Garnett, M. Najarian, et al., "Enhanced thermoelectric performance of rough silicon nanowires," *Nature,* vol. 451, pp. 163-168, 2008.
70. D. Wang and H. Dai, "Germanium nanowires: from synthesis, surface chemistry, and assembly to devices," *Applied Physics A—Materials,* vol. 85, pp. 217-225, 2006.
71. J. A. Czaban, D. A. Thompson, and R. R. LaPierre, "GaAs core-shell nanowires for photovoltaic applications," *Nano Letters,* vol. 9, pp. 148-154, 2009.
72. Z. H. Wu, X. Mei, D. Kim, M. Blumin, H. E. Ruda, J. Q. Liu, et al., "Growth, branching, and kinking of molecular-beam epitaxial GaAs nanowires," *Applied Physics Letters,* vol. 83, pp. 3368-3370, 2003.
73. Z. Y. Fan, D. W. Wang, P. C. Chang, W. Y. Tseng, and J. G. Lu, "ZnO nanowire field-effect transistor and oxygen sensing property," *Applied Physics Letters,* vol. 85, pp. 5923-5925, 2004.
74. Z. Y. Fan, J. C. Ho, T. Takahashi, R. Yerushalmi, K. Takei, A. C. Ford, et al., "Toward the development of printable nanowire electronics and sensors," *Advanced Materials,* vol. 21, pp. 3730-3743, 2009.
75. K. Skucha, Z. Fan, K. Jeon, A. Javey, and B. Boser, "Palladium/silicon nanowire Schottky barrier based hydrogen sensors," *Sensors and Actuators B—Chemical,* vol. 145, pp. 232-238, 2010.

76. M. Harting, J. Zhang, D. R. Gamota, and D. T. Britton, "Fully printed silicon field effect transistors," *Applied Physics Letters,* vol. 94, pp. 193509, 2009.
77. R. A. Street, "Thin-film transistors," *Advanced Materials,* vol. 21, pp. 2007-2022, 2009.
78. T. T. Ho, Y. F. Wang, S. Eichfeld, K. K. Lew, B. Z. Liu, S. E. Mohney, et al., "In situ axially doped n-channel silicon nanowire field-effect transistors," *Nano Letters,* vol. 8, pp. 4359-4364, 2008.
79. C. J. Kim, D. Lee, H. S. Lee, G. Lee, G. S. Kim, and M. H. Jo, "Vertically aligned Si intrananowire p-n diodes by large-area epitaxial growth," *Applied Physics Letters,* vol. 94, 2009.
80. A. Kolmakov and M. Moskovits, "Chemical sensing and catalysis by one-dimensional metal-oxide nanostructures," *Annual Review of Materials Science,* vol. 34, pp. 151-180, 2005.
81. Y. Zhang, A. Kolmakov, S. Chretien, H. Metiu, and M. Moskovits, "Control of catalytic reactions at the surface of a metal oxide nanowire by manipulating electron density inside it," *Nano Letters,* vol. 4, pp. 403-407, 2004.
82. C. H. Wang, X. F. Chu, and M. W. Wu, "Detection of H_2S down to ppb levels at room temperature using sensors based on ZnO nanorods," *Sensors and Actuators B—Chemical*, vol. 113, pp. 320-323, 2006.
83. V. V. Sysoev, B. K. Button, K. Wepsiec, S. Dmitriev, and A. Kolmakov, "Toward the nanoscopic 'electronic nose': Hydrogen vs. carbon monoxide discrimination with an array of individual metal oxide nano- and mesowire sensors," *Nano Letters,* vol. 6, pp. 1584-1588, 2006.

PART II

Molecular Electronics

This page intentionally left blank

CHAPTER 5

Printed Organic Electronics: From Materials to Circuits

Manuela La Rosa, Nunzia Malagnino, Alessandro Marcellino, Donata Nicolosi, Luigi Occhipinti, Fabrizio Porro, Giovanni Sicurella, Raffaele Vecchione, Luigi Fortuna, Mattia Frasca, and Elena Umana

5.1 Introduction

Printed organic electronics is a novel and unconventional technology that has the potential to revolutionize the world of electronics and bring a new perspective. Organic electronics offers the challenge of many intriguing possibilities that are not compatible with standard inorganic electronics. The opportunity to manufacture low-cost and large-area devices using low-cost, low-temperature techniques makes organic electronics suitable for flexible applications over plastic substrates, thus enabling the exploitation of a broad range of new applications. Since the realization of the first *organic thin-film transistor* (OTFT) in 1983,[1] an intense research effort has been dedicated to both the improvement of organic materials and the development of innovative deposition and manufacturing techniques for low-cost electronics assessment. Up to now, organic thin film transistors have been investigated for applications in various fields, from electronic backplanes in *organic light-emitting diodes* (OLEDs) for rollable displays, to chemical and bio-*field effect transistor* (FET) sensors, to simple logic circuits to be associated with *radiofrequency identification* (RFID) tags, as well as thin-film batteries and e-paper in new multifunctional systems.[2–5] In this perspective, organic materials scouting has been identified as a promising field for developing innovative electronic devices for flexible and low-cost applications. The reduced investment required to manufacture organic electronic devices and the possibility of conceiving innovative systems on rollable substrates are the reasons for the

great effort spent in recent years on organic materials research and on the assessment of stamp-based processing techniques. Organic material properties have been tailored to obtain required features for electronic applications by designing new molecules with enhanced properties, improved lifetime, and environmental stability, as well as solution processability and feasible charge mobility. Thus, the possibility of modifying the composition and material preparation is the strongest trend in postsilicon technologies in the electronics application field. Thanks to the improvements obtained in recent years, organic semiconductors exhibited charge mobility values comparable to amorphous silicon and polysilicon.[6–8] Moreover, organic conductors such as PEDOT:PSS (*poly(3,4-ethylene dioxythiophene):poly(styrene sulfonate)*), if opportunely doped, exhibited conductivity up to 500 S/cm.[9,10] On the other hand, stamp-based imprinting processes are going down to tens of nanometers in scale, without the high costs of conventional lithography. *Nanoimprint lithography* (NIL) and soft lithography (SL) processes,[11,12] based on hard and soft stamps, respectively, are continuously being improved, and equipment manufacturers are investing to realize machinery to manufacture organic devices on large areas. Imprinting lithography, combined with low-cost deposition techniques such as spin-coating and inkjet printing, is currently adopted to realize multilayered structures by using materials processed by solution. The combination of these aspects, materials, and process paves the way to the fabrication of new active and passive devices for advanced applications. In this perspective, a consolidated workflow going from materials to devices is required: a complete technology platform that describes the process flowchart and the tools used in the design, layout, and realization of an organic electronic circuit. Materials needed in the manufacturing process flow are both organic (substrates, conductors, dielectrics, semiconductors) and inorganic (solvents, hard stamps, printable metals, etc.). The equipment must be selected both for the manufacturing process (spin coater, soft lithography press, mask aligners, etc.) and for the measurement/characterization process. Moreover, electronic design automation software comprising device models, simulation tools, layout design tools, and design validation tools must be defined for product design test and qualification.

This chapter aims to introduce the adopted organic electronics technology framework and to discuss progress in this direction. Printing and imprinting processes are illustrated, showing patterning results with minimum feature sizes down to 200 nm. The selected manufacturing steps represent the core of a complete process flow to fabricate organic devices such as organic thin-film transistors. Moreover, the scaling of the process is underlined to demonstrate the feasibility of organic technologies for the realization of electronic architectures with higher levels of complexity in terms of integrated gates.

5.2 Materials for Organic Electronics

The prime key to organic electronic technology development is the availability of a set of organic materials (semiconductors, conductors, dielectrics) with good electrical and chemical characteristics and compatible solvents. There are many challenges to be overcome when synthesizing novel organic materials for printed electronic applications. First of all, they must, of course, be processable from the liquid phase. Other fundamental requirements are their stability in ambient conditions, and their performance must be reproducible. Moreover, in combining a feasible set of materials, an all-organic multilayered functional device structure is obtained by imprinting techniques. In term of electric performance, the adopted organic materials must satisfy some requirements that strongly affect OTFT performance: organic conductors with large conductivities are required for the realization of source and drain contacts; organic semiconductors with high charge carrier mobility and high I_{on}/I_{off} ratios are needed to ensure high current values and low leakages; and as for the adopted organic dielectric, high-*k* materials are required as gate dielectrics, whereas low-*k* dielectrics are needed as organic insulating materials. To this aim, in recent decades, research in the field of organic materials for electronics applications has been vigorous, with the aim of obtaining materials that ensure the required electrical performance but also are easy to process and guarantee long-term stability for device longevity. Many conducting and semiconducting polymers and small-molecule semiconductors have been synthesized with improved electrical performance. However, because small molecules are insoluble in common solvents, they need to be deposited through expensive vapor phase deposition techniques. Thus, polymers remain the materials of choice for low-cost organic electronics exploitation. The versatility of polymers enables their adoption in many application areas ranging from organic electronics devices such as OLEDs,[3] organic transistors, and organic photovoltaics,[4] to smart packaging, e-paper, and printed RFID inks and transducers.[5]

5.2.1 Organic Conductors

In 1977, Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa discovered that conjugated polymers (films of polyacetylene, *trans*-$(CH)_x$) could be opportunely doped, tuning their conductivity in the range from insulator to conductor.[13] That discovery paved the way to the creation of a new generation of polymers: the conducting polymers. These materials maintain polymers' mechanical properties, such as lightness and mechanical flexibility, yet offer electrical behavior typical of semiconductors or conductors. Moreover, polymeric materials present many advantages because they can be deposited

from solution, thus enabling the adoption of innovative low-cost and low-temperature manufacturing techniques. In recent years, these interesting properties have motivated intense research into innovative materials scouting. The possibility of reducing manufacturing costs by adopting low-cost deposition techniques from the liquid phase is highly appealing. Thus, a huge effort is continually made to improve the properties of polymeric materials (dielectrics, conductors, and semiconductors).

Among the available conducting polymers, the most commonly used are *polyaniline* (PANI) and PEDOT:PSS, which can be deposited from solution through low-cost deposition and patterning techniques such as spin coating, dip coating, microcontact printing (μCP), or inkjet printing. PEDOT:PSS, if opportunely doped, has exhibited the highest conductivity values, on the order of hundreds of siemens per centimeter. Moreover, PEDOT:PSS film conductivity can be enhanced more than 100-fold if a liquid or solid organic compound, such as dimethyl sulfoxide (DMSO), *N*, *N*-dimethylformamide (DMF), glycerol, or sorbitol, is added to its aqueous solution.[9] This discovery is very important for fundamental studies and practical applications of conducting polymers, because PEDOT:PSS has become one of the most used conducting polymers—for example, as an important hole-injecting and -transporting material for OLEDs.

5.2.2 Organic Semiconductors

Many organic semiconductors have been synthesized and extensively characterized, to be used as active materials in OTFT device manufacturing. According to the type of charge carrier, holes or electrons, organic semiconductors can be classified as p- or n-type. Moreover, organic semiconducting materials can be divided into two groups: polymers and small molecules. Small molecules, because of their crystalline structure in the solid state, are generally more stable against environmental conditions; however, for the same reason they are poorly soluble in common solvents and thus cannot be deposited by liquid phase, but only through vapor deposition techniques. More specifically, organic semiconductors exhibiting the best electrical performance are small molecules such as pentacene or *alpha-sexithiophene* (α-6T) deposited over a substrate, through expensive and high-temperature evaporation processes. Whereas p-type organic semiconductors generally exhibit air-stable behavior, the n-channel types still need to be improved in terms of stability and feasibility and to obtain electrical performance comparable to that of their p-channel counterparts. In an effort to resolve these issues, many research groups are working to synthesize small-molecule soluble organic semiconductors and novel n-channel semiconducting polymers.

In a recent study,[14] OTFTs realized with a highly soluble printable n-channel polymer are demonstrated with electron mobility up to 0.45–0.85 cm^2/Vs in ambient conditions, with Au contacts and various polymeric dielectrics with an operating voltage of 60 V. Just as an example, among the most commonly used organic semiconductors, both polymers and low-molecular-weight molecules, processable from the liquid phase, we can mention Tips-pentacene, DB-TTF, DH-6T, P3HT, and PTAA. In Ref. 15, organic field-effect transistors realized using tetrathiafulvalene derivates such as the solution-processed dithiophene- and dibenzo-tetrathiafulvalene (DT- and DB-TTF) single crystals as active materials are reported with mobility up to 3.6 cm^2/Vs and I_{on}/I_{off} ratio greater than 10^6. Among small molecules, an opportunely functionalized pentacene, triisopropylsilyl pentacene (TIPS-pentacene), can be used as a soluble organic semiconductor for OTFT active-layer realization. In Ref. 16, OTFTs have been fabricated using solution-processable TIPS-pentacene as the active material. The obtained devices exhibited a field-effect mobility greater than 1.2 cm^2/Vs, a subthreshold slope of 0.2–0.7 V/dec, and I_{on}/I_{off} ratio greater than 10^8. These devices, like many of the OTFTs reported in the literature, used a doped silicon wafer as both the sample substrate and OTFT gate electrode, with thermally grown silicon dioxide serving as the gate insulator. In Ref. 17, patterned bottom-gate solution-processed TIPS-pentacene OTFTs on glass substrates are reported with mobility of 0.6 cm^2/Vs and subthreshold slope as low as 0.4 V/dec. Concerning soluble semiconducting polymers, a thiophene derivate, the regioregular head-to-tail poly(3-hexylthiophene) (HT-P3HT), is among the most extensively studied and used, because of its easy synthesis and relatively high mobility in an inert atmosphere. In Ref. 18, OTFTs based on an HT-P3HT active layer exhibited mobility as high as 0.2 cm^2/Vs and current I_{on}/I_{off} ratio of 10^6 when processed and characterized in an inert atmosphere. Poorer mobility and significantly lower I_{on}/I_{off} ratios were demonstrated in Ref. 19 when the devices were fabricated in ambient air, and the characteristics degraded further on exposure to air and light. Because of this sensitivity to environmental conditions,[20] P3HT-based OTFTs exhibit stability problems in air and need to be opportunely coated to be protected from oxygen or humidity. In Ref. 21, organic field-effect transistors fabricated using the polymeric semiconductor polytriarylamine (PTAA) are demonstrated with good environmental stability and processability. Interdigitated electrode structures were printed with a PEDOT formulation and different insulator layers were deposited by spin coating, resulting in a field-effect mobility of 3×10^{-3} cm^2/Vs and I_{on}/I_{off} ratio of about 10^3. The choice of organic semiconductor is wide but is strongly affected by the right selection of the adopted dielectrics that are described in the following section.

5.2.3 Organic Dielectrics

A fundamental role in the performance of OTFT devices is played by the gate dielectric, whose primary purpose is to isolate the gate contact from the rest of the structure. Dielectric requirements are to be printable and to have a high dielectric constant to obtain transistors with low-voltage operation. Moreover, the organic dielectric layer should be as thin as possible and pinhole-free in order to provide homogeneous surfaces between organic semiconductor and dielectric. Inorganic, organic, and hybrid (inorganic/organic) materials have been investigated as gate dielectric materials. Promising materials, that are very often used as OTFT gate dielectrics include poly(methyl methacrylate) (PMMA),[22] poly(styrene) (PS), poly(vinylphenol) (PVP),[23] poly(vinyl alcohol) (PVA),[24] and benzocyclobutene (BCB).[25,26] Ultra-thin cross-linked polymers, that is, polymers in which chemical bonds have been created between chains, are characterized by increased glass transition temperature T_g, strength, and toughness, and thus they are generally more robust as dielectric materials, exhibiting a high capacitance.[27] It has been demonstrated that high-capacitance gate insulators can be obtained even from a well-ordered, densely packed, very thin self-assembled monolayer (SAM)[28] and that the incorporation of high-dielectric-constant inorganic nanoparticles into the polymer matrix increases the thin-film dielectric constant.[29] As most OTFTs are fabricated according to the *bottom-gate* architecture, where the semiconductor is deposited on top of the insulator, the surface of the latter is greatly responsible for the quality of the insulator-semiconductor interface, which in turn crucially controls the performance of the device. Because the interface between the gate dielectric and the semiconductor is the active area where charge transport takes place, defects in this area act as traps; thus a semiconductor/gate-dielectric interface presenting imperfections and increased roughness implies a decrease in mobility and device performance. Dielectric properties of a material include breakdown field strength, dielectric constant, and loss factor. In contrast to inorganic materials, the properties of organic materials are not stable in terms of frequency of the applied field and temperature. Thus, whereas the dielectric constant of SiO_2 is 3.78 in the frequency of 10^2–10^{10} Hz, in the case of organic materials the dielectric constant depends on frequency and temperature, and the trend is quite complex.[30]

5.3 Stamp-Based Fabrication Processes

Standard silicon-based electronic devices are manufactured through the adoption of conventional, and expensive, high-temperature manufacturing techniques such as photolithography and vapor-phase deposition. Moreover, a controlled environment is required to ensure

device feasibility. In order to overcome these issues, much effort has been made toward transferring acquired know-how in the field of conventional manufacturing techniques into a novel all-organic approach. Up to now, many unconventional printing and imprinting techniques have been developed to be applied for organic electronic device manufacturing, and huge investments have been made by many equipment manufacturers to set up large-scale production machines. Moreover, various low-cost printing techniques have been developed such as screen printing, flexography, gravure printing, inkjet printing, and nonconventional lithography. These techniques are all based on simple mechanisms to print the desired structures over a surface that could be silicon glass or the less expensive plastic. The adoption of printing techniques for organic electronic device manufacturing enables the realization of low-cost, light, and flexible devices and also enables roll-to-roll processing over large areas. Exploitation of printed organic electronics offers the opportunity to develop novel electronic applications providing competitive performance at less cost compared to standard silicon-based electronics. As for the imprinting processes, two main methodologies can be identified: nanoimprint lithography and soft lithographic techniques.

5.3.1 Nanoimprint Lithography

NIL processes have the main advantage of enabling downscaling of feature sizes to a few nanometers, and they have been investigated to guarantee the realization of circuits with the necessary switching speed. Nanoimprint lithography is a very promising imprinting technique that, according to the International Technology Roadmap for Semiconductors (ITRS), is considered a next-generation lithography to be employed at the 35-nm node.[31] The NIL technique uses a hard stamp, generally made of silicon or UV-transparent quartz, to pattern the desired structures. This technique allows feature sizes down to tens of nanometers to be obtained, is characterized by a very high throughput, and gives the opportunity to pattern over large areas.

The NIL technique can adopt one of two different patterning methods: UV-based and hot embossing. In the first case a UV-transparent mold (generally quartz) is used and structures are patterned by means of UV photopolymerization of an organic curable resist. In the second case a thermoplastic resist, such as PMMA, is first heated at a temperature higher than its glass transition temperature T_g and then patterned by applying high pressure and further cooling.[32] The patterning of Hyflon® dielectric by hot embossing NIL with a minimum feature size of 120 nm is shown in Fig. 5.1. This imprinting step is the first and most critical on the process flowchart described in Section 5.3.4.

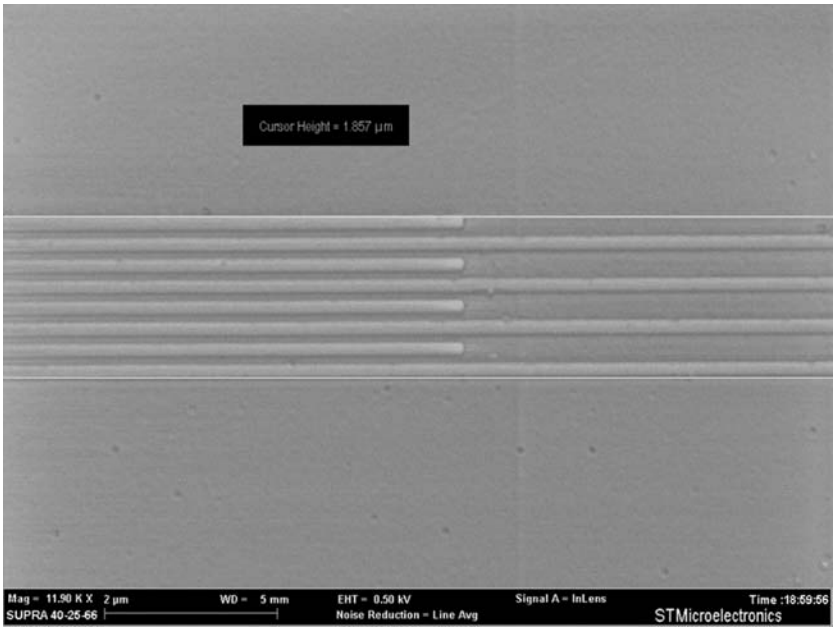


Figure 5.1 SEM image of Hyflon dielectric material patterned by NIL hot embossing at 120-nm feature size. Copyright © IEEE 2008.

5.3.2 Soft Lithography

The soft lithographic techniques include many unconventional lithographic processes to transfer a pattern over the desired substrate, such as microcontact printing (μCP), micromolding, and related techniques such as micromolding in capillaries (MIMIC), replica molding (REM), microtransfer molding (μTM), and solvent-assisted micromolding (SAMiM). SL techniques make use of a soft elastomeric stamp that is obtained as a replica of a hard stamp. The most commonly used elastomer for soft stamp manufacturing is poly(dimethylsiloxane) (PDMS), for example, Sylgard 184 from Dow Corning, but other elastomers such as polyurethanes, polyimides, and cross-linked Novolac resin (a phenol formaldehyde polymer) have also been used. Starting from a silicon mold, several soft stamps can be obtained; thus the SL manufacturing technique is very cost effective. In SL, the minimum feature size achievable is limited to hundreds of nanometers. More specifically, μCP is a nonphotolithographic technique allowing routine patterning of self-assembled monolayers (SAMs), containing regions terminated by different chemical functionalities.[11] An "ink" is deposited over the elastomeric PDMS stamp, which is then brought into conformal contact with the substrate in order to transfer "ink" molecules over the surface. Microcontact printing was first

demonstrated for SAMs of alkanethiols on gold. The thiol "ink" is transferred to the substrate where it forms a SAM that can act as a resist against etching.

Another nonphotolithographic technique is MIMIC, which allows creating continuous patterns over a substrate both planar and curved. In this case, complex microstructures can be formed by putting the soft PDMS stamp in conformal contact over the desired substrate. Channels are filled for microcapillarity with a polymer precursor; the polymer is then cured into a solid, and the stamp is removed. A complementary replica of the mold is obtained. MIMIC is able to generate features down to 1 μm in size.

In the replica molding technique, a PDMS stamp is created from a silicon master. Prepolymer is poured over the soft stamp and then cured. In this way as many copies as desired can be created without damaging the original master. It has been demonstrated that this technique allows resolution on the nanometer scale to be obtained.[11] In microtransfer molding, a PDMS stamp is filled with a liquid prepolymer and placed over a substrate. The precursor is then cured and the stamp removed, leaving the desired pattern. It can be used over both planar and nonplanar surfaces. The technique can generate features as small as 250 nm, and multilayer systems can be created. In solvent-assisted micromolding (SAMiM), a polymer solvent is spread over the PDMS stamp, which is then put in contact with the polymer. The solvent swells the polymer, and the resulting fluid covers the stamp surface conformally. After solvent evaporation, the negative pattern is obtained. Features as small as 60 nm have been produced. Soft lithography techniques have been used in our laboratories to imprint high-resolution patterns into PEDOT:PSS and PMMA films. More specifically, soft embossing and micromolding in capillaries have been performed on PEDOT:PSS formulation. Conducting polymer PEDOT:PSS lines with 1-μm feature size fabricated by microcapillarity through a PDMS stamp are shown in Fig. 5.2*A*. The adoption of the MIMIC technique allowed patterning without any residual, providing a better thickness profile; on the other hand, only interconnected structures can be reproduced. The replica molding process has been adopted in our labs to obtain interdigitated structures of PMMA dielectric from a relief stamp with line width of 900 nm and spacing of 600 nm, as shown in Fig. 5.2*B*.

5.3.3 Mold Manufacturing

Patterned silicon masters are used either to produce soft molds for SL or with the function of hard molds for NIL. Mold manufacturing is performed by combining both optical and e-beam lithography in a mix and match process,[11,33,34] following the process flow described in Fig. 5.3. Hard molds are fabricated through conventional processes

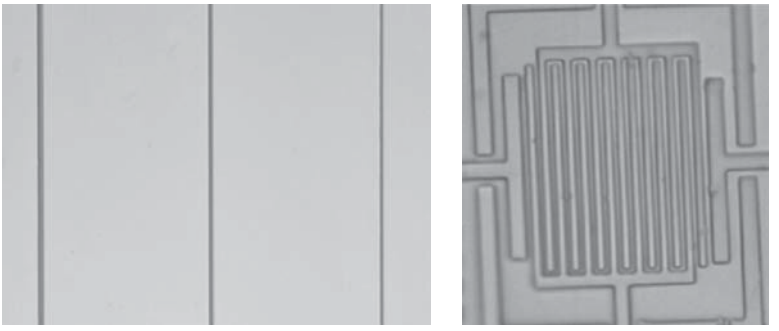


Figure 5.2 (*A*) PEDOT:PSS patterned by microcapillarity at 1 μm and (*B*) optical microscopy images of PMMA structures with minimum feature size 600 nm patterned by replica molding. Copyright © IEEE 2008.

such as e-beam lithography, optical lithography, or reactive ion etching (wet or dry). More specifically, optical lithography is used to define micrometer structures, whereas e-beam is used to define submicrometer structures. When both micrometer and submicrometer structures are required, the two techniques are combined in a mix and match process. The complete process to produce both positive and negative molds is shown in Fig. 5.3. It comprises three successive steps: optical lithography, e-beam lithography, and *reactive ion etching* (RIE). In step 1, optical lithography is applied to realize large structures, with feature sizes greater than 2 μm, over the silicon master. To achieve this goal, standard clear field lithographic masks, in association with positive resist, are used. Then, the resist is developed and a 20-nm-thick nickel layer is thermally evaporated. Finally, resist removal is performed through a lift-off process. When submicron structures need to be realized, e-beam lithography is adopted. The described process allows realizing aligned submicron structures as source and drain electrodes. It comprises the following steps: first, a thick film of PMMA resist is deposited, then e-beam is applied, and finally the resist is developed. Then, nickel is thermally evaporated, and finally lift-off is performed. At this stage, metallic patterns over the silicon substrate are revealed. In the third step, low-relief patterns are created in silicon by RIE and the metallic mask is removed with a lift-off operation. At the end of the manufacturing process, the silicon master is subjected to an antisticking treatment, which is a necessary step for applications in NIL or SL in order to facilitate the release of the patterned organic material. A simple antisticking procedure can be performed as follows: chloroorganosilanes (such as trichlorododecylsilane) react with surface silanols, thus producing a hydrophobic monolayer on the surface of the silicon template. Following the described procedure, molds

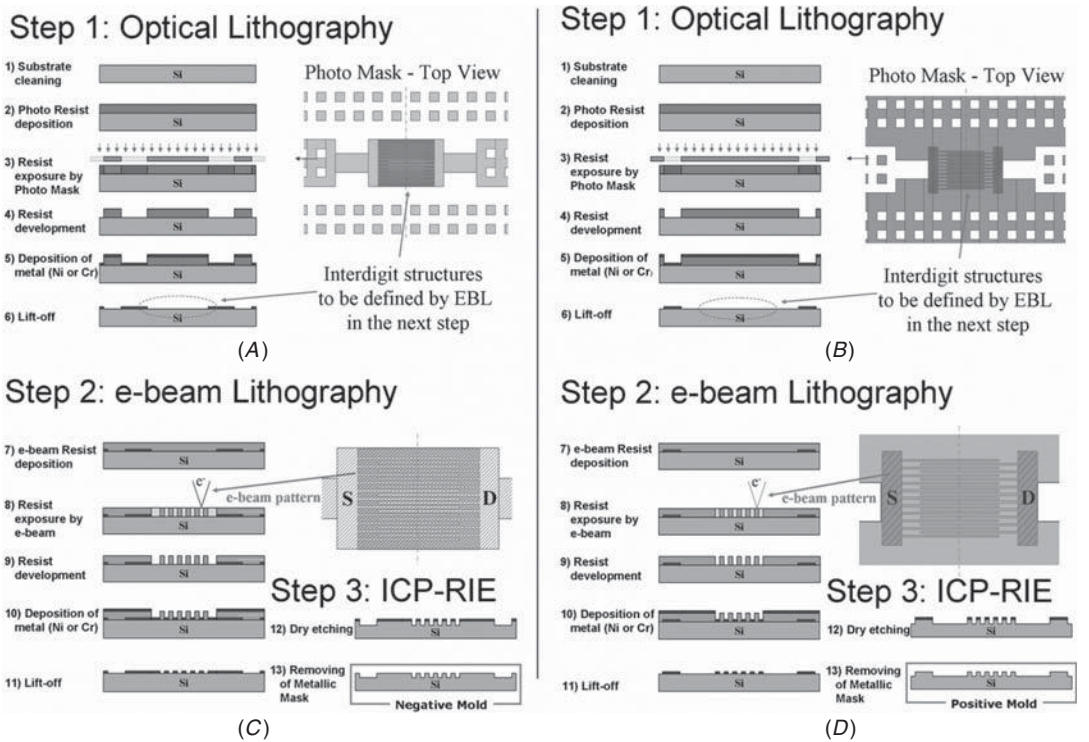
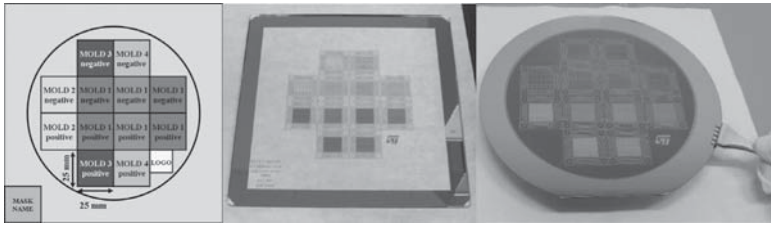


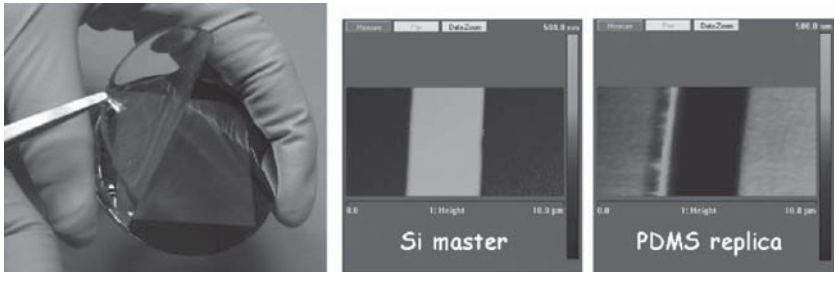
FIGURE 5.3 Step 1: optical lithography for negative (*A*) and positive (*B*) molds. Step 2 and 3: E-beam lithography of interdigit structures and reactive ion etching of negative (*C*) and positive (*D*) molds. Copyright © IEEE 2008.



(*A*) (*B*) (*C*)

Figure 5.4 (*A*) Lithographic mask scheme, (*B*) mask layout, and (*C*) realized mold masters in silicon wafer.

have been fabricated and a 7-inch photo mask has been designed for defining structures on silicon master by optical lithography. With this technique, test structures have been fabricated in our laboratories in the range from 50 nm up to 10 μm. The photo mask is composed of many subunits of 2.5 cm $\times$ 2.5 cm size, each one corresponding to a mold, as shown in Fig. 5.4*A,B*. A silicon mold master comprising different hard stamps to be used for NIL is shown in Fig. 5.4*C*. After UV lithography on a 6-inch silicon substrate, molds can be separated by cutting along scribe lines. Soft stamps are realized through a sequence of four steps: PDMS pouring over the hard mold, PDMS degassing in air, curing in oven, and finally stamp peeling-off. This last phase is reported in Fig. 5.5*A* showing the elastomeric stamp obtained from the hard mold. The PDMS soft stamp replicates the silicon mold structures, as shown by the AFM images of Fig. 5.5*B*. The selection between hard and soft stamp patterning is strictly related to the employed materials and the desired geometric feature size. The adoption of suitable imprinting and deposition techniques allows realizing printed organic circuits with feature sizes from micrometer to nanometer scale.



(*A*) (*B*)

Figure 5.5 PDMS stamps for soft lithography: (*A*) peel off, (*B*) AFM images of silicon, and PDMS structure reproduction.

5.3.4 Process Flowchart

The techniques described in the previous section are used to define the printed electronics whole manufacturing process. The adopted process flowchart is reported in Fig. 5.6, which shows the sequence of steps required to realize each layer constituting the final organic multilayer device. The manufacturing of a single layer requires three successive phases: imprinting and curing, organic material deposition, and reactive ion etching. The complete process flow requires the adoption of only four molds. The first layer is realized with steps 1 through 3, using mold 1. Imprinting techniques such as NIL or μCP are used to realize the device bottom contacts. This is a critical point of the manufacturing process when submicron-feature-size structures have to be obtained. Patterned structures are filled with an organic conductor using a spin coater or an inkjet printer. In steps 4 and 5 the processing of the low-k dielectric layer is shown. This layer is required to insulate devices, pads, and vias one from the other when required. Holes are made on the dielectric layer (step 5) through the adoption of mold 2, in order to obtain the semiconductor well and conductive interconnections for pads and vias. Then, organic semiconductor is locally deposited by means of the inkjet printing deposition technique as shown in step 6. The deposition and patterning of the gate dielectric layer (so-called high-*k*, also to distinguish it from other isolating dielectric layers) is shown in steps 7 and 8. Also in this case, holes for pads and vias interconnections are obtained by an imprinting technique, using mold 3. The last layer, which comprises the device top contacts, is described in steps 9 and 10. The organic conductor is deposited by inkjet printing or spin-coating and then patterned through an imprinting technique using mold 4. The described flowchart can be adopted to fabricate organic electronic fundamental components such as *organic thin-film capacitors* (OTFCs) and *organic thin-film resistors* (OTFRs). Moreover, OTFTs, which are the basic building blocks of an organic electronic circuit, with feasible electrical performance can be manufactured through layer-by-layer deposition. More specifically, OTFTs in a top gate and bottom contact architecture have been considered.

5.4 Organic Thin-Film Devices

The recent advances obtained in the field of organic electronics are the results of a parallel effort spent in two different directions: improvement in device manufacturing, and wider availability of materials with enhanced electrical performance. Liquid-phase organic materials allow organic device manufacturing by combining deposition and printing/imprinting techniques in a multilayer structure such as the OTFT. Organic thin-film transistors are field-effect devices

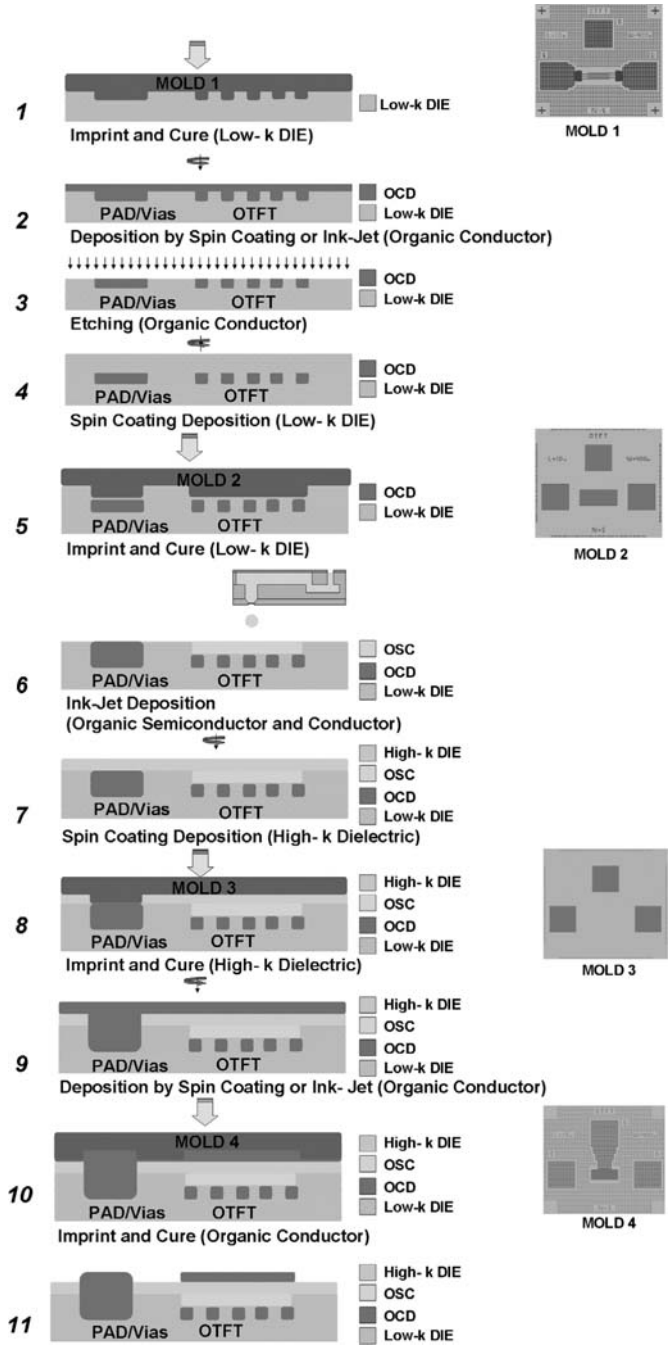


Figure 5.6 Multilayer all-organic device technology process flow. Copyright © IEEE 2008.

with organic thin-film semiconductors as the active layer. In terms of performance, organic transistors cannot be compared to inorganic semiconductor transistors; however, the opportunity to realize low-cost, large-area, and flexible devices by using economic manufacturing techniques opens the way to the development of innovative electronic applications. Analogously to its silicon-based counterpart, the OTFT device has three terminals, and by applying a voltage to the gate terminal, the current flowing through the channel can be opportunely tuned. The main features of OTFT are the mobility μ, which describes the ability of charge carriers to move through the active semiconducting layer, and the ratio I_{on}/I_{off} between the "on" and "off" current, which should be as high as possible, as a result of a low leakage current. Both of them are strongly affected by manufacturing technique and materials interaction. The full exploitation of organic electronics has been hindered by the lack of n-channel semiconductors with the needed requirements. The availability of an organic CMOS technology could allow improved organic circuit performance, resulting in circuit speed-up and lower power consumption. In our laboratories, hole-transporting (p-channel) OTFTs have been realized and characterized and dedicated architectural solutions like ratioed logic p-type circuitries have been considered. The adopted OTFT has top-gate architecture with a conduction channel between the drain and source contacts, and is characterized by a multifinger structure, with N_f fingers, a width $W = W_f N_f$, and a channel length L that tunes the current flowing from the drain to the source. The adoption of a multifinger structure allows the device size to be minimized while keeping the same performance. The section view and the multifinger structure of the realized OTFTs are shown in Figs. 5.7*A* and 5.7*B*, respectively.

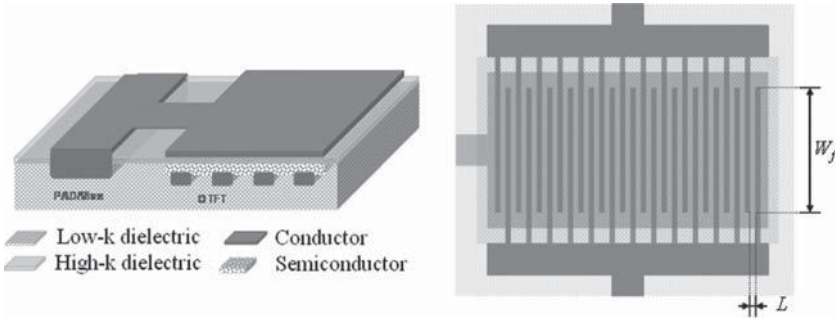
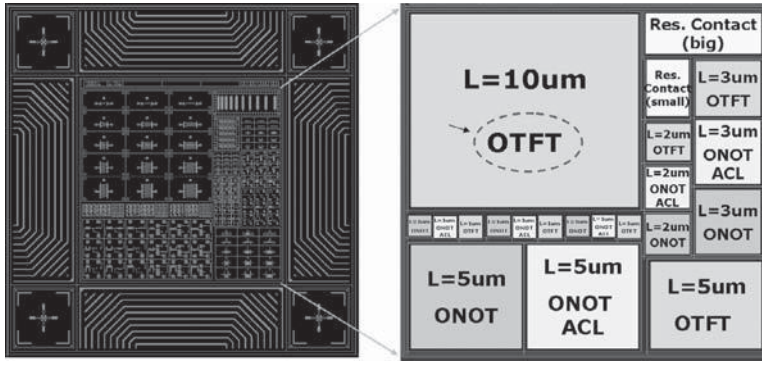


FIGURE 5.7 (*A*) Schematic 3D section view of an interdigitated OTFT with a gate pad, and (*B*) OTFT multifinger structure. Copyright © IEEE 2008.

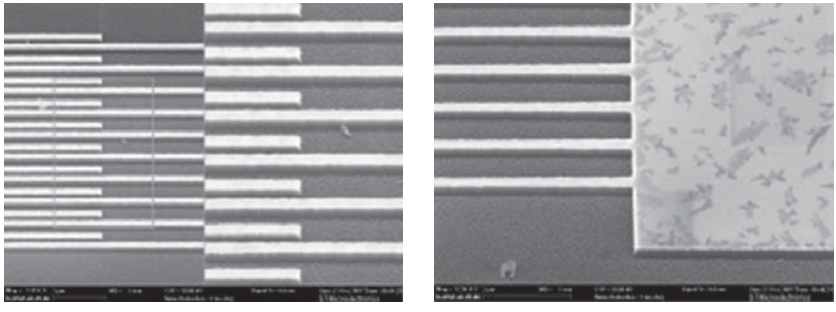


(*A*) (*B*)

FIGURE 5.8 (*A*) Mold layout and (*B*) schematic view of the included structures.

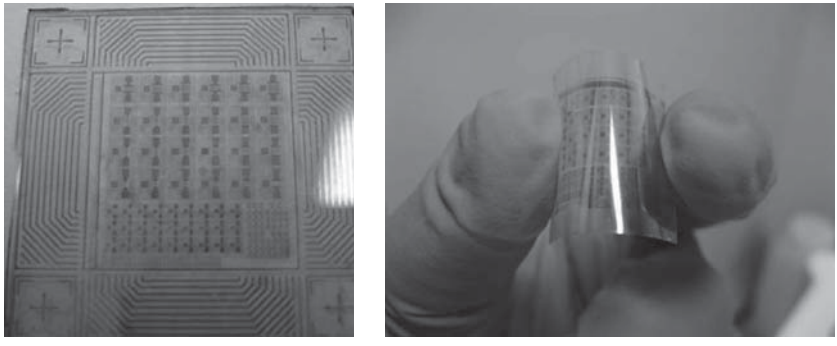
5.4.1 Device Design and Layout

In order to characterize the developed technology, a large number of test transistors with scaled feature sizes have been designed. The layout of a single mold is shown in Fig. 5.8; Fig. 5.9 shows the morphological characterization of 200-nm silicon master interdigitated structures. Top-gate transistor arrays with scaled feature sizes L from 1 to 10 μm have been designed, realized, and characterized over both glass and plastic substrates, as shown in Fig. 5.10, following the flow schematized in Fig. 5.6. A simple way to fabricate a top-gate bottom-contact OTFT device is depositing organic semiconductor and dielectric everywhere on patterned source and drain electrodes. Finally, the gate electrode must be aligned on the top. Several types of organic semiconductors based either on polymers or on small molecules have



(*A*) (*B*)

FIGURE 5.9 SEM images of 200-nm silicon master interdigitated structure.



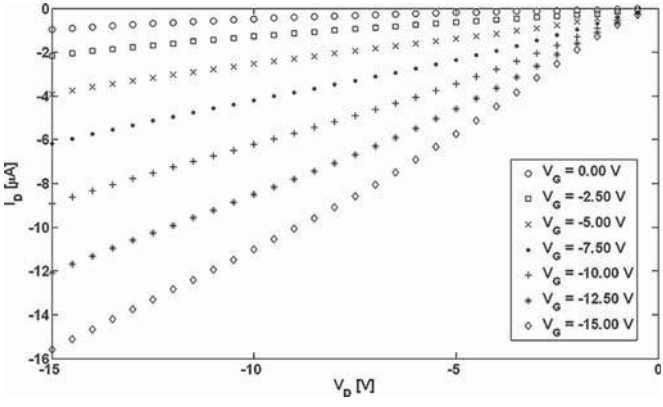
(*A*) (*B*)

FIGURE 5.10 Top-gate printed transistors on (*A*) glass substrate and (*B*) plastic substrate at 5 μm.

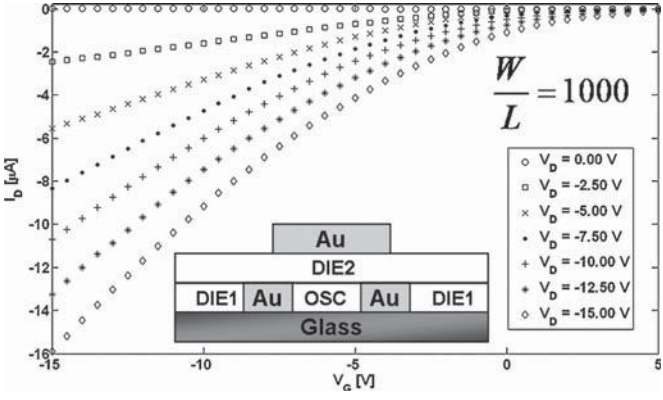
been tested. Various formulations of PEDOT:PSS conducting polymer have been adopted to realize both interconnections and OTFT electrodes. The films obtained were characterized by a low roughness ($\sim$2 nm on 300- to 400-nm thin film), mechanical robustness (conductivity maintained under bending, no cracks at low bending radius), and long-term stability (no degradation induced by temperature, humidity, or time). The realized devices have been electrically characterized, and reliability tests have been performed.

5.4.2 OTFT Device Electrical Characterization

The electrical characterization has been performed using an Agilent Semiconductor Parameter Analyzer 4155 and a Cascade Microtech-MicroChamber AttoGuard Probe Station. The tungsten tips must scratch the soft polymers to contact the buried source and drain pads. Both dc and ac analyses have been performed. In the dc analysis, the transfer characteristics have been measured for a variety of drain voltages V_d varying from 0 V to –15 V with a step of 2.5 V; output characteristics have been measured for a gate voltage V_g varying in the same range (–15 V to 0 V). Some results are reported in Fig. 5.11*A*,*B* for samples realized over a glass substrate, having $W/L = 1{,}000$ ($L = 5$ μm; $W_f = 200$ μm; $N_f = 25$). The obtained results proved the field-effect behavior of fabricated devices, though their performance could be further improved. At this stage, these results are useful to verify process-step feasibility. The fabrication process is continually optimized in response to synthesis of new materials and availability of new equipment. Improvements are expected from better control and optimization of single process steps that can increase device performance and reproducibility.



(*A*)



(*B*)

Figure 5.11 Dc measurement for a printed bottom-contact OTFT over a glass substrate having $L = 5\ \mu$m; $W_f = 200\ \mu$m; $N_f = 25$ ($W/L = 1{,}000$): (*A*) output and (*B*) transfer characteristics.

5.4.3 OTFT Device Modeling

The printed technology design flow requires the improvement of organic device characterization and models. In particular, a compact model of the organic transistor is fundamental for the development of organic applications. In literature, the behavior of the OTFT, analogously to the inorganic transistor, is generally described by the equations for the three operation regions: off, linear, and saturation regimes. These equations are opportunely modified to take into account the specific features of the organic transistor. More specifically, the OTFT behavior is modeled according to the universal mobility law

(UML) and variable-range hopping (VRH)[35]:

$$I_{ds} = \mu_0 \cdot \frac{W}{L} C_{ox} \cdot \left[\left(V_{gte}\right)^{2m+2} - \left(V_{gte} - V_{dse}\right)^{2m+2} \right] \cdot (1 + \lambda V_{ds}) + I_0;$$

$$\mu_0 = \frac{K_3 \cdot C_{ox}^{2m}}{(2m+1)(2m+2)\left(2 \cdot \varepsilon_0 \cdot \varepsilon_p \cdot k \cdot T\right)^m}. \tag{5.1}$$

Starting from equations developed in Ref. 35, the model has been suitably modified in Ref. 36, where a single equation, (5.1), is proposed to describe the drain current I_{ds} in the three regimes. The exponential factor m takes into account the specific features of the adopted organic semiconductor: note that when $m = 0$, the reported model turns into the classic MOSFET one. New strategies are investigated to characterize and model OTFT behaviors from experimental data.[37,38] An organic transistor model has been implemented by considering the differences in performances and in features due to technology variations. Moreover, the adoption of several organic materials by various process techniques produces organic transistors that are characterized by dissimilar performance. For these reasons, a compact model has been implemented that takes into account the actual spread in parameters obtained from statistical analysis. The model was developed using various static and dynamic experimental data on several transistors to determine the parameter values required to define organic thin-film transistor behavior. The compact model described in Eq. (5.1) and the organic transistor parameters are extracted by gray-box identification procedures developed ad hoc; in detail, this involves an optimization algorithm that identifies the set of model parameter values for which the predicted data best fit with the experimental ones. The developed model with the identified parameters is then integrated in the CAD environment. A total of 12 parameters tune the model according to the adopted technology and processing techniques.[37] The model parameters are given in Table 5.1. In Fig. 5.12*A*,*B*, the I_{ds} current curves, related to a sample printed over a glass substrate, having $W/L = 200$ ($L = 5\ \mu$m; $W_f = 200\ \mu$m; $N_f = 5$) obtained by adopting the identified parameter values in the organic transistor compact model (5.1) are shown and compared with the related experimental data sets.

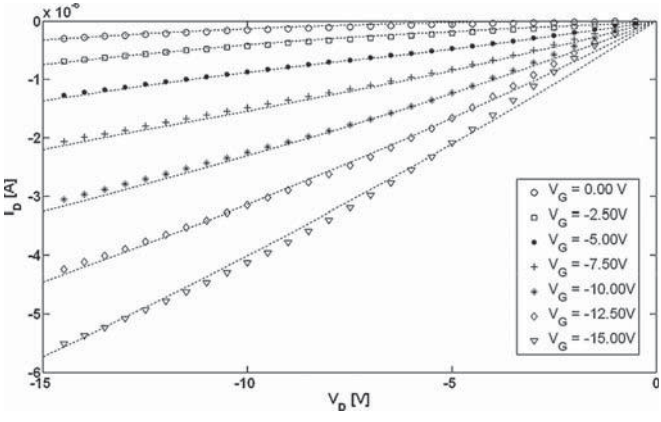
5.4.4 CAD Integration

A fundamental issue in organic electronics exploitation is the development of design tools such as *computer-aided design* (CAD) software, technology libraries, and the design of testbeds and demonstrators. All these key points are synthesized in the development of a printed electronic technology platform that comprises a design platform and the technology itself. The design platform is a set of libraries, design

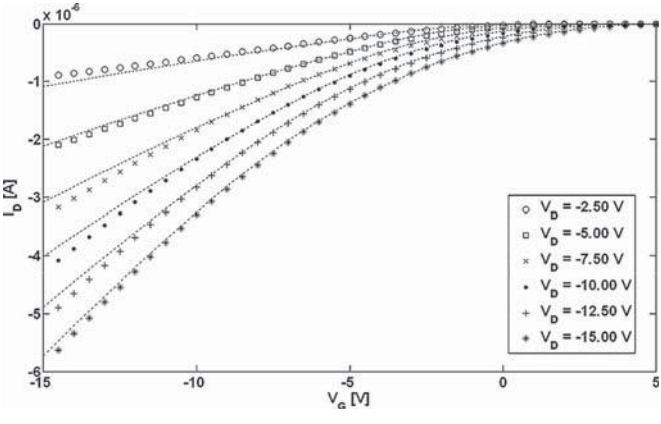
Parameter	Description
W	Channel width
L	Channel length
C_{ox}	Oxide capacitance
ε_0	Vacuum permittivity
ε_p	Relative permittivity of polymeric semiconductor
K_3	UML model constant
k	Boltzmann constant
m	Mobility model parameter
I_0	Leakage current
λ	Output conductance parameter
V_{gte}	V_{gt} effective voltage
V_{dse}	V_{ds} effective voltage

Table 5.1 Parameters of the OTFT Compact Model

rules, design flows, and design tools; the technology is defined as a set of technology steps in process order, associated with equipment and recipes, materials, know-how, procedures, and characteristics used to produce semiconductor devices. The development of the technology platform includes several activities, done in parallel and regrouped in successive phases, to supply the design platform and the production technology for organic materials: feasibility, definition, design and development, validation, and qualification. The integration of the new organic electronic technology into a CAD framework requires adapting the standard procedures to an unusual technology: uncommon manufacturing processes compared to standard silicon technologies are involved in this case. Thus, ad hoc tools must be developed in the CAD framework for both layout design and device model simulation. An ad hoc design kit for printed electronics has been developed by defining: technological parameters, fundamental components library (OTFT, OTFR, OTFC), analog device models for simulation (compact model), and physical checking rules. Moreover, the OTFT compact model has been implemented and integrated into the Cadence™ analog simulation environment by means of a VerilogA description in the Eldo™ simulator (Mentor Graphics), thus simplifying the design of both digital[39] and analog[40,41] complex organic circuits by compensating the effect of process variations.[42] OTFT compact



(*A*)



(*B*)

Figure 5.12 Parameter identification method validation: experimental data versus simulated data: (*A*) OTFT output and (*B*) transfer curves, for a printed bottom-contact OTFT over a glass substrate having $L = 5\ \mu$m; $W_f = 200\ \mu$m; $N_f = 5$ ($W/L = 200$).

model integration in the CAD environment made it possible to design circuitries based on organic transistors in the same way as the inorganic counterparts. Once organic circuit design reliability has been tested by means of simulation tools, the layout of the entire system can be drawn. The layout design tools assist designers during the production of layouts feasible by the technology, according to process limitations and electrical characteristics of the materials. Design tools use information stored into the technology Design Kit, which is a software module. The Design Kit has been realized by means of the technology information specified in the Design Rules Manual

Layer	Name	Description	Patterning	Mold	Type	Material
1	SBT	Substrate (standard)	optical litho	1 positive	DIE Low-k	PMMA
2	EBL1	Substrate (submicron)	e-beam litho			
3	OCD1	Bottom Contacts	-	-	Conductor	PEDOT:PSS
4	DIE1	Filling Dielectric	optical litho	2 positive	DIE Low-k	PMMA
5	OSC1	Organic Semiconductor	inkjet printing	-	Semicond.	P3HT
6	OCD2	Intermediate Contacts	inkjet printing	-	Conductor	PEDOT:PSS
7	FED1	Field Effect Dielectric	optical litho	3 positive	DIE High-k	PVDF-TrFE
8	OCD3	Top Contacts (standard)	optical litho	4 positive	Conductor	PEDOT:PSS
9	DIE2	Filling Dielectric	optical litho	5 positive	DIE Low-k	PMMA

Feature	*Description*	*Layout Rule*
L	Channel Length	L=F
W_f	Fingers width	$W_f = 20\ F \div 60\ F$
N	Number of fingers (-1)	$N = 5 \div 40$
L_S	Length of source fingers	$L_S = F$
L_D	Length of drain fingers	$L_D = F$
W_D	Drain contact width	$W_D = 10\ F$
W_S	Source contact width	$W_S = 10\ F$
W_{space}	Space between fingers and contacts	$W_{space} = 10\ F$
L_{space}	Space between external fingers and borders	$L_{space} = 5\ F$
L_N (n=0…N)	Distance of n-*th* finger from origin	$L_N = L_{space} + n(L_S/2 + L + L_D/2)$
W_G	Gate contact width	$W_G = W_f + W_{space}$
L_G	Gate contact length	$L_G = 2L_{space} + N(L_S/2 + L + L_D/2)$
w	OTFT total width	$w = W_f + 2W_{space} + W_D + W_S$
h	OTFT total length	$h = L_G$
W_{OSC}	OSC layer width	$W_{OSC} = w$
L_{OSC}	OSC layer length	$L_{OSC} = h$

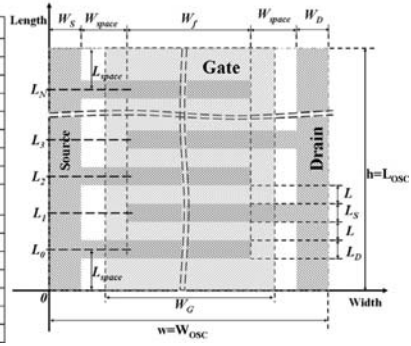


Figure 5.13 DRM layer definition and OTFT layout rules. Copyright © IEEE 2008.

(DRM), which consists of a collection of rules defining the technology specifics. It contains the molds alignment flowchart (as reported in Fig. 5.6), the layers definition table, general layout rules (including spacing, distances, and overlap) and basic device layout rules described in Fig. 5.13. All the designed molds have been drawn in the Cadence environment using the Virtuoso® Layout Editor.

5.4.5 Printed Electronic Circuits

The developed technology platform for printed electronics has been adopted for the design and simulation of several organic circuits, either digital[39] or analog,[40] and to develop library blocks including both basic logic gates and advanced digital circuits: XOR, MUX, decoders, buffer three-states, DRAM and SRAM cells, latches, and flip-flops. Organic radioed logic gates have been designed by adopting a conventional pseudo-PMOS architecture that uses only p-type organic transistors. These configurations are mainly constituted by a driver circuit implementing the logic function and a load circuit usually constituted by a transistor operating in the saturation region. Moreover, unconventional circuital solutions, suited to organic device electrical characteristics, have been designed.

The proposed architectures face the problem of reduced performance of organic transistors by introducing new solutions dedicated

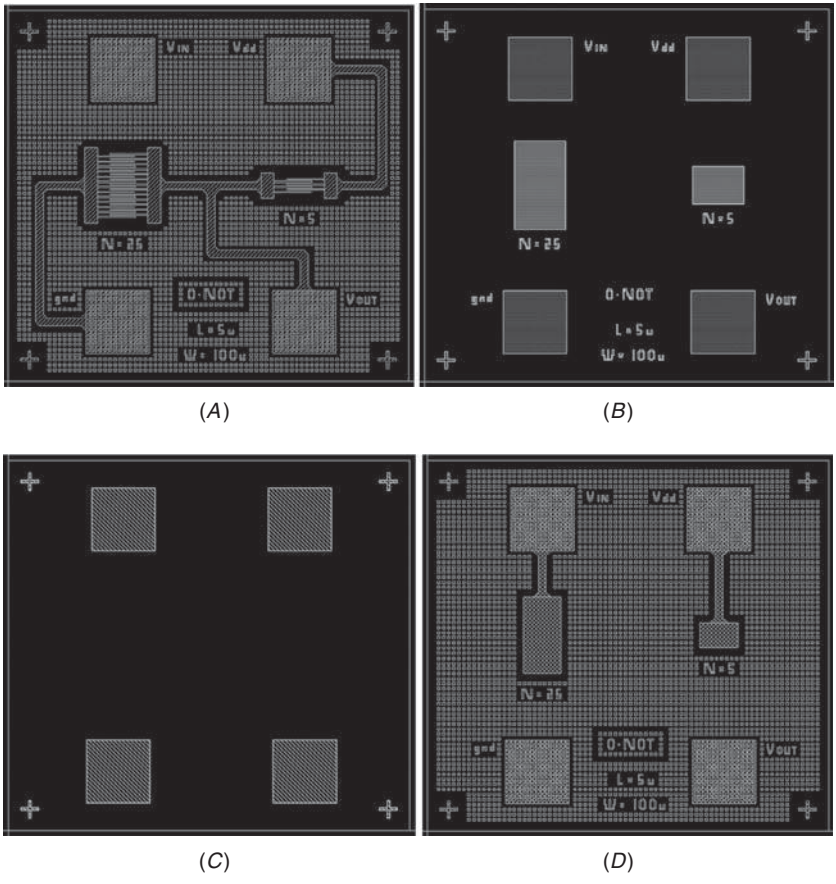


Figure 5.14 Organic inverter mask layout: (*A*) mold 1, (*B*) mold 2, (*C*) mold 3, (*D*) mold 4.

to organic devices. The design choice enhances speed and reduces area occupancy. Thus, to speed up logic gates and minimize power consumption, a load with two transistors and one capacitor (active capacitive load) has been adopted. The proposed architectures have been simulated in the CAD environment and test prototype layouts have been designed. The technology Design Kit just described has been used for mask fabrication and mold manufacturing. As an example, Fig. 5.14 shows the mask layout of an organic ratioed logic inverter. Starting from the designed masks, the four molds have been realized and adopted for organic inverter manufacturing. OTFT fabrication steps described in Fig. 5.6 have been applied to test process feasibility. The source and drain electrodes have been realized in gold by

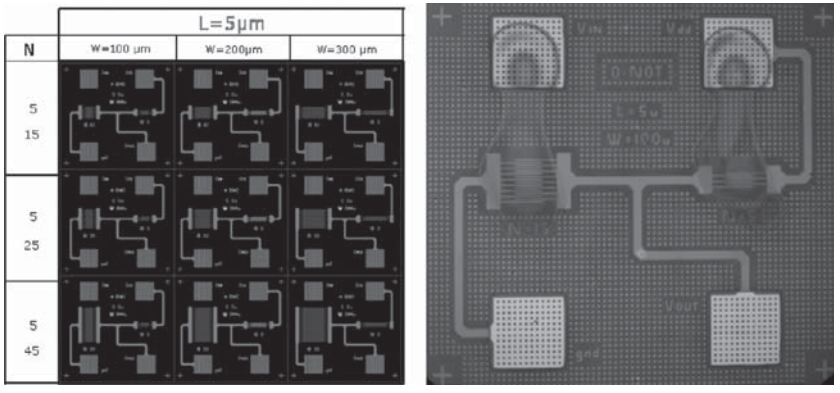


Figure 5.15 (*A*) Standard ONOT blocks layout. (*B*) Standard PMOS with polymer gate at 5 μm.

microcontact printing, nanoimprinting, and photolithography techniques. The organic semiconducting layer has been deposited by spin-coating and inkjet printing. Both metal-based (Au, Pt) and inkjet-printed polymer (PEDOT:PSS) gate and top connection layers have been realized. In Fig. 5.15*A*, the layouts of standard Organic NOT (ONOT) gates are shown considering different channel widths and numbers of fingers. In Fig. 5.15*B*, a printed circuit is shown. In particular, inkjet printing has been adopted to deposit the OSC layer and to realize the gate and both the top connection layers and via filling by PEDOT:PSS. The design and manufacturing platform has been assessed through the design of a 4-bit organic *arithmetic logic unit* (ALU) demonstrator whose schematic blocks are shown in Fig. 5.16. An outline of the architecture and behavioral simulation are presented. In particular, the 4-bit ALU allows both logic and arithmetic operations, which are enabled by MUX input signal S. The logic unit is able to perform AND and OR operations while the arithmetic operations are performed by the adder block. Both logic unit and adder internal circuits are shown in Ref. 32. The adder block has a critical path of 2 ms and critical working frequency of 0.5 kHz, with the larger feature size ($L = 10$ μm) technology, which is expected to be improved considerably in later technology generations with smaller feature sizes down to $L = 0.2$ μm. The complete ALU is constituted by 180 OTFTs and 36 OTFCs. Figure 5.17 reports a typical example of both logic operations and full adder functions, performed in parallel, and selected by setting up the *S* control signal at high or low logic value, respectively, as underlined by the variation of the output values *Z0*, *Z1*, *Z2*, *Z3*.

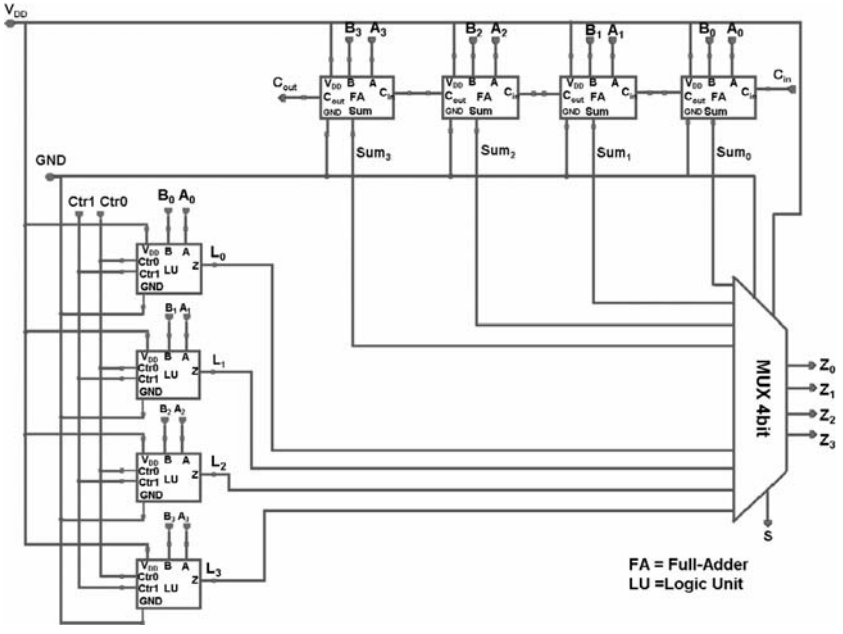


FIGURE 5.16 All-organic 4-bit ALU schematic block. Copyright © IEEE 2008.

5.5 Conclusions

The development of stamp-based technologies for processing of organic materials is due to their interesting electrical and mechanical properties, to their potential low cost, and to the possibility of scaling the device feature size down to a few nanometers. In silicon technology, scaling down requires the adoption of sophisticated and expensive manufacturing equipment. The adoption of printing and imprinting technologies enables feature-size scaling down at more reasonable costs. The full exploitation of printed organic electronics could represent a breakthrough in the development of brand-new applications, in which the electronics (transducers, displays, and circuitry) are printed over the desired surface. From a market perspective, organic electronic development requires interaction among material suppliers, equipment manufacturers, and electronic industry players in order to overcome the limitations of material performances by introducing innovative solutions in process manufacturing and circuit design. The implementation of a technology platform is a fundamental step toward the definition of material requirements and the selection of process steps for technology test vehicle deployment. The scaling down of organic electronic devices to subnanometer feature size paves the way to organic thin-film transistors with higher

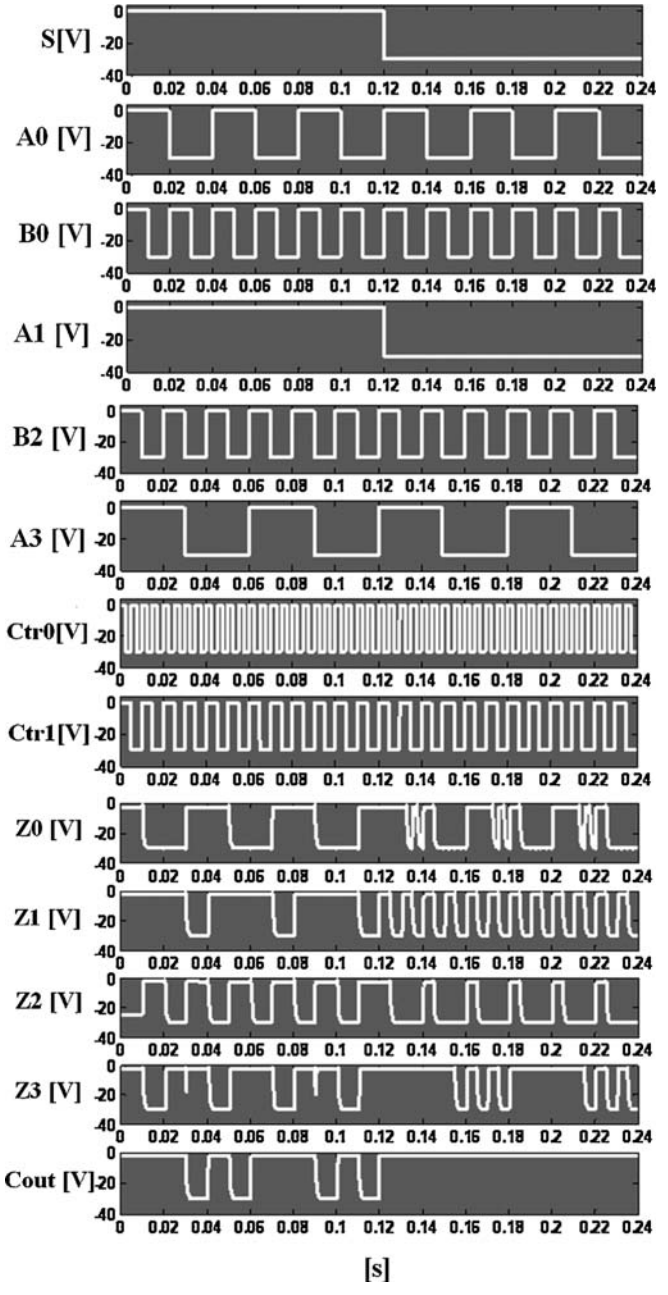


Figure 5.17 Organic ALU logic and adder operations. Copyright © IEEE 2008.

performance in terms of speed and reliability. Much work still remains to identify disruptive applications that can drive the development of organic printed electronics from lab to market. Foreseen application fields range from biotechnology to low-weight space electronic devices, and the technology is open to vast research and development possibilities.

References

1. E. Ebisawa, T. Kurokawa, and S. Nara, "Electrical properties of polyacetylene/polysiloxane interface," *Journal of Applied Physics*, vol. 54, pp. 3255-3260, 1983.
2. C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: a review of recent advances," *IBM Journal of Research & Development*, vol. 45, pp. 11-27, 2001.
3. J. Jang, "Displays develop a new flexibility," Materials Today, vol. 9(4), pp. 46-52, 2006.
4. H. Hoppe and N. S. Sariciftci, "Organic solar cells: An overview," *Journal of Materials Research*, vol. 19(7), pp. 1924-1945, 2004.
5. L. Torsi and A. Dodabalapur, "As plastic analytical sensors," *Analytical Chemistry*, pp. 381-387, 2005.
6. B. S. Ong, Y. L. Wu, P. Liu, and S. Gardner, "High-performance semiconducting polythiophenes for organic thin-film transistors," *Journal of the American Chemical Society*, vol. 126, pp. 3378-3379, 2004.
7. M. Heeney, C. Bailey, K. Genevicius, M. Shkunov, D. Sparrowe, S. Tierney, et al., "Stable polythiophene semiconductors incorporating thieno[2,3-*b*]thiophene," *Journal of the American Chemical Society*, vol. 127(4), pp. 1078-1079, 2005.
8. I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, et al., "Liquid-crystalline semiconducting polymers with high charge-carrier mobility," *Nature Materials*, vol. 5, pp. 328-333, 2006.
9. J. Ouyang, Q. Xu, C. Chu, Y. Yang, G. Li, and J. Shinar, "On the mechanism of conductivity enhancement in poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) film through solvent treatment," *Polymer*, vol. 45, pp. 8443-8450, 2004.
10. http://www.clevios.com .
11. Y. Xia and G. M. Whitesides, "Replica molding with a polysiloxane mold provides this patterned microstructure," *Angewandte Chemie International Edition*, vol. 37, pp. 550-575, 1998.
12. C. M. Sotomayor-Torres, S. Zankovych, J. Seekamp, A. P. Kam, C. Clavijo Cedeño, T. Hoffmann, et al., "Nanoimprint lithography: an alternative nanofabrication approach," *Materials Science and Engineering*, vol. C23, pp. 23-31, 2003.
13. H. Shirakawa, E. J. Louis, A. G. MacDiarmid, C. K. Chiang, and A. J. Heeger, "Synthesis of electrically conducting organic polymers: halogen derivatives of polyacetylene, $(CH)_x$," *Journal of the Chemical Society, Chemical Communications*, pp. 578-580, 1977.
14. H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, et al., "A high-mobility electron-transporting polymer for printed transistors," *Nature*, vol. 457, pp. 679-686, 2009.
15. M. Leufgen, O. Rost, C. Gould, G. Schmidt, J. Geurts, L. W. Molenkamp, et al., "High-mobility tetrathiafulvalene organic field-effect transistors from solution processing," *Organic Electronics*, vol. 9(6), pp. 1101-1106, 2008.
16. S. K. Park, C.-C. Kuo, J. E. Anthony, and T. N. Jackson, "High-mobility solution-processed OTFTs," *IEDM Technical Digest*, pp. 113-116, 2005.
17. S. K. Park, J. E. Anthony, and T. N. Jackson, "Solution-processed TIPS-pentacene organic thin-film-transistor circuits," *IEEE Electron Device Letters*, vol. 28(10), pp. 877-879, 2007.

18. H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielen, K. Bechgaard, B. M. W. Langeveld-Voss, et al., "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, pp. 685-688, 1999.
19. Z. Bao, A. Dodabalapur, and A. Lovinger, "Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility," *Applied Physics Letters*, vol. 69, pp. 4108-4110, 1996.
20. M. S. A. Abdou, F. P. Orfino, Y. Son, and S. Holdcroft, "Interaction of oxygen with conjugated polymers: charge transfer complex formation with poly(3-alkylthiophenes)," *Journal of the American Chemical Society*, vol. 119, pp. 4518-4524 1997.
21. D. Zielke, A. C. Hübler, U. Hahn, N. Brandt, M. Bartzsch, U. Fügmann, et al., "Polymer-based organic field-effect transistor using offset printed source/drain structures," *Applied Physics Letters*, vol. 87, 123508, 2005.
22. S. Uemura, M. Yoshida, S. Hoshino, T. Kodzasa, and T. Kamata, "Investigation for surface modification of polymer as an insulator layer of organic FET," *Thin Solid Films*, vol. 438, p. 378, 2003.
23. M. Halik, H. Klauk, U. Zschieschang, T. Kriem, G. Schmid, W. Radlik, et al., "Fully patterned all-organic thin film transistors," *Applied Physics Letters*, vol. 81, p. 289, 2002.
24. P. Parashkov, E. Becker, G. Ginev, T. Riedl, H. H. Johannes, and W. Kowalsky, *Journal of Applied Physics*, vol. 95, p. 1594, 2004.
25. L. L. Chua, P. K. H. Ho, H. Sirringhaus, and R. H. Friend, "High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors," *Applied Physics Letters*, vol. 84, p. 3400, 2004.
26. L. L. Chua, J. Zaumseil, J. F. Chang, E. C. W. Ou, P. K. H. Ho, H. Sirringhaus, et al., *Nature*, vol. 434, p. 194, 2005.
27. M.-H. Yoon, H. Yan, A. Facchetti, and T. J. Marks, "Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics," *Journal of the American Chemical Society*, vol. 127, pp. 10388-10395, 2005.
28. Y. D. Park, D. H. Kim, Y. Jang, M. Hwang, J. A. Lim, and K. Cho, "Low-voltage polymer thin-film transistors with a self-assembled monolayer as the gate dielectric," *Applied Physics Letters*, vol. 87, 243509/1-3 (2005).
29. Z. Bao, "Organic materials for thin film transistors," *Materials Matters*, vol. 2(2), 4-6, 2007.
30. T. A. Osswald and G. Menges, *Materials Science of Polymers for Engineers*, Hanser Gardner Publications, 1996.
31. *International Technology Roadmap for Semiconductors*, 2006 Update, "Lithography." Available at http://www.itrs.net/Links/2006Update/FinalToPost/08_Lithography2006Update.pdf.
32. L. Fortuna, M. Frasca, M. Gioffrè, M. La Rosa, N. Malagnino, A. Marcellino, et al., "On the way to plastic computation," *IEEE Circuits and Systems Magazine*, Third Quarter 2008.
33. M. D. Austin and S. Y. Chou, "Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography," *Applied Physics Letters*, vol. 81, p. 4431, 2002.
34. Y. Jang, Y. D. Park, J. A. Lim, H. S. Lee, W. H. Lee, and K. Cho, "Patterning the organic electrodes of all-organic thin film transistors with a simple spray printing technique," *Applied Physics Letters*, vol. 89, 183501), 2006.
35. A. R. Brown, D. M. de Leeuw, E. E. Havinga, and A. Pomp, "A universal relation between conductivity and field-effect mobility in doped amorphous organic semiconductors," *Synthetic Metals*, vol. 68, pp. 65-70, 1994.
36. M. Fadlallah, G. Billiot, W. Eccleston, and D. Barclay, "DC/AC unified OTFT compact modeling and circuit design for RFID applications," *Solid-State Electronics*, vol. 51, pp. 1047-1051, 2007.
37. M. Fadlallah, W. Benzarti, G. Billiot, W. Eccleston, and D. Barclay, "Modelling and characterization of organic thin film transistors for circuit design," *Journal of Applied Physics*, vol. 99, 104504, 2006.

38. D. Natali, L. Fumagalli, and M. Sampietro, "Modeling of organic thin film transistors: effect of contact resistances," *Journal of Applied Physics*, vol. 101, 014501, 2007.
39. M. La Rosa, D. Nicolosi, G. Sicurella, L. Fortuna, and M. Frasca, "Organic dynamic random access memory," in *Proceedings of Organic Electronics Conference and Exhibition '06*, Frankfurt, Sep 2006.
40. L. Fortuna, M. Frasca, M. La Rosa, D. Nicolosi, G. Sicurella, and E. Umana, "Organic Chua's circuit," *International Journal of Bifurcation and Chaos*, vol. 17(9), pp. 3035-3045, 2007.
41. M. La Rosa, L. Fortuna, M. Frasca, G. Sicurella, S. Castello, and E. Umana, "All organic nonlinear oscillator," in *Proceedings of the 10th Experimental Chaos Conference*, Catania, June 2008.
42. L. Fortuna, M. Frasca, M. La Rosa, L. Occhipinti, G. Sicurella, and E. Umana, "Nonlinear electronic circuits through organic transistors,"*Proceedings of International Conference on Organic Electronics*, Eindhoven, June, 2006.

This page intentionally left blank

CHAPTER 6

One-Dimensional Nanostructure-Enabled Chemical Sensing

Aihua Liu

6.1 Introduction

The rapid advance in nanoscience and nanotechnology provides increasingly robust methods and tools to solve difficult problems and offers new chances to reach an in-depth understanding of nano-bio interface interactions[1] Nanostructured materials have been widely used in the anode material for lithium rechargeable batteries, fuel cells, electronic devices, catalyst supports, and photovoltaic cells because of their remarkable chemical properties.[2,3] Advances in nanotechnology may be able to provide more sensitive detection systems for air and water quality monitoring, allowing the simultaneous measurement of multiple parameters and real-time response capability.[4] One-dimensional (1D) nanostructures such as nanowires, nanotubes, and nanobelts (or nanoribbons) have become the focus of intensive research because of their unique properties and their potential for fabrication into high-density nanoscale devices including sensors, electronics, and optoelectronics.[5] This is because 1D nanostructures can be used for both efficient transport of electrons and optical excitation, and these two factors make them critical to the function and integration of nanoscale devices.[5] In fact, 1D nanosystems are the smallest-dimension structures that can be used for efficient transport of electrons and are thus critical to the function and integration of these nanoscale devices. Nanowires, or nanoribbons, and nanotubes can be developed into particularly sensitive chemical sensors because

of their high surface-to-volume ratios.[6] The extraordinary properties of nanowires/nanoribbons and nanotubes are attractive for the fabrication of novel analytical devices that have advantages over traditional devices in many aspects: for example, low cost, simple design, and improved selectivity and sensitivity. Developing wireless nanodevices and nanosystems is of critical importance for sensing, medical science, homeland safety, and even personal electronics.[7]

The use of various routes for the fabrication of metal oxide nanoarchitectures for environmental sensing applications has been reviewed elsewhere.[8] Advances in chemical sensing on the basis of metal-oxide nanowires and nanotubes has also been summarized.[9] Very recently, a wide range of 1D nanostructured materials, including metal-oxide nanowires/nanoribbons/nanotubes, polymer nanowires/nanotubes, and metal nanowires, have been extensively reported. These 1D nanostructures are fundamental to the development of smart and functional materials, devices, and systems.[10]

A major area of application for nanowires and nanotubes is likely to be the sensing of important molecules, for either medical or environmental purposes. Over the past 10 years, *carbon nanotubes* (CNTs) have found a wide range of applications in nanoelectronic devices, chemical sensors, and bionanotechnology, owing to their unique chemical, electronic, and mechanical properties. CNTs have found significant application in the preparation of gas sensors, because CNTs exhibit ultrahigh surface-to-volume ratios in these structures, which make their electrical properties extremely sensitive to surface-adsorbed species.[11,12] CNTs have also shown excellent electrocatalytic properties and therefore provide novel electrode materials for electroanalytical applications.[13–16]

However, there have been no systematic reviews of the recent progress in the preparation of sensors based on other 1D nanostructures. In this chapter, the development of chemical sensors using nanowires or nanotubes is highlighted. The sensing application of CNTs is not covered in this chapter, because CNT-based sensing has been widely reported and reviewed.[17–19]

6.2 Semiconducting Metal Oxide Nanowire-Based Sensing

The development of a robust method for integrating high-performance semiconductors on flexible plastics could enable exciting avenues in fundamental research and novel applications.[6] One area of vital relevance is chemical and biological sensing, which, if implemented on biocompatible substrates, could yield breakthroughs in implantable or wearable monitoring systems.[6] Scaling of the metal-oxide semiconductor *field-effect transistor* (FET) has been the basis of

the semiconductor industry for nearly 30 years. Traditional materials have been pushed to their limits, which mean that entirely new materials (such as high-gate dielectrics and metal gate electrodes) and new device structures are required. These materials and structures will probably allow metal-oxide semiconductor devices to remain competitive for a relatively long time. Beyond this time scale, entirely new device structures (such as nanowire or molecular devices) and computational paradigms will certainly be needed to improve performance. The development of new nanoscale electronic devices and materials places increasingly stringent requirements on metrology.[20] Nanowire-based sensors have the advantages of sensitivity, spatial resolution, and rapid response associated with individual nanowires. For example, RuO_2-based nanowires are good and relevant candidates for interconnects and optoelectronics.[21] Based on the target analytes of interest, these sensors are generally classified into gas sensors, humidity sensors, bacterial pathogen sensors, and biosensors. The basis of these sensors is the nanoelectronics.

6.2.1 Nanowire-Based Nanoelectronics or Nano-optoelectronics

Nanowire-based nanoelectronic devices are innovative electronic building blocks. Self-assembled molecular nanowire, including molecular design and 1D crystal growth, has attracted great interest. The resistance measurement of individual wire may find application to a FET, which is a possible alternative to conventional transistors.[22–24] Nanowire transistors enable high on-off ratios, ultralarge integration, and logic circuits.[25] Moreover, a multichannel transistor has been proposed where dimensional uniformity of the wires is strictly required, because even slight nonuniformities may cause variations in device properties.[24] Appropriate molecular design and control of interfacial interactions can be used to grow single-crystalline wire with an extensive π-stacking motif. Resistance measurements of an individual molecular wire indicate that these structural features are advantageous for electrical transport. Finally, FETs with single- and double-wire channels have been fabricated to give some indication of the potential application of the molecular wires.[26] Nanowire devices with reduced nanocontact area magnify the contribution of contact electrical properties. Although many two-contact-based ZnO nanoelectronics have been demonstrated, it remains unclear whether the electrical properties are from the nanocontacts or the nanowires. High-quality ZnO nanowires with a small deviation and an average diameter of 38 nm have reportedly been used to fabricate more than 30 nanowire devices. Conventional FET and nanowire devices are shown in Fig. 6.1*A*. According to the temperature behaviors of current-voltage curves and resistances, the

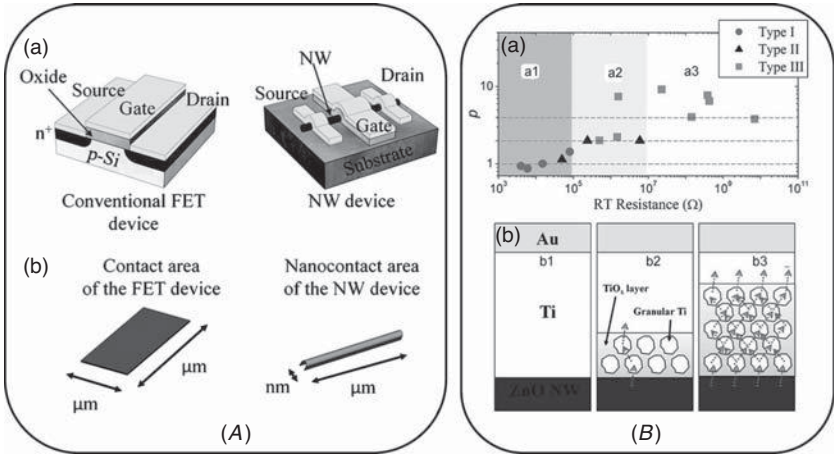


Figure 6.1 (*A*), Schematic illustration of conventional FET and nanowire devices (*a*) and with their corresponding contact areas (*b*). (*B*), The fitting exponent parameters *p* as a function of *RT* resistance for as-fabricated ZnO nanowire devices of types I, II, and III, marked as circles, triangles, and squares, respectively. It is approximately separated into regions (*a1*, *a2*, and *a3*) according to the exponent parameters of the devices (*a*). (*b*), Three different nanocontact models (*b1*, *b2*, and *b3*) corresponding to the ZnO nanowire devices belonging to regions *a1*, *a2*, and *a3* in panel (*a*). Reprinted with permission from Ref. 27. Copyright ©2008 American Chemical Society.

devices could be grouped into three types. Type I devices expose thermally activated transport in ZnO nanowires, which could be considered as two ohmic nanocontacts of the Ti electrode contacting directly on the nanowire. Those nanowire devices having a high resistance at room temperature can be fitted accurately with the thermionic-emission theory and classified into type II and III devices according to their rectifying and symmetrical current-voltage behaviors. The type II device has only one deteriorated nanocontact and the other one ohmic contact on single ZnO nanowire. An insulating oxide layer with thickness less than 20 nm should be introduced to describe electron hopping in the nanocontacts, so as to signalize one- and higher-dimensional hopping conduction in type II and III devices.[27]

A photonic sensor based on subwavelength nanowires that are capable of detecting molecules in solution by absorbance, fluorescence, and *surface-enhanced Raman scattering* (SERS) was designed by Yang and his co-workers.[28] These authors used single-crystalline SnO_2 nanowires as the passive optical components in the devices, in which the photons instead of electrons allow optical spectroscopy to be carried out on the analyte. The use of the evanescent wave sensors in absorbance and fluorescence mode (Fig. 6.2) as well as evanescent wave SERS mode (Fig. 6.3) can also be attained. Potentially, portable

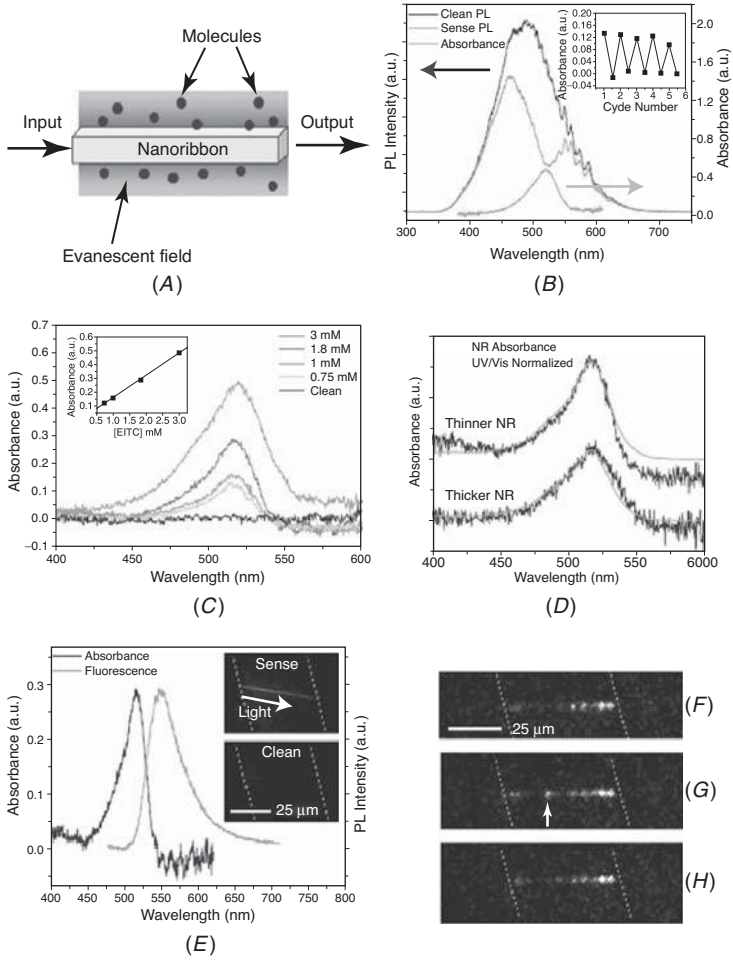
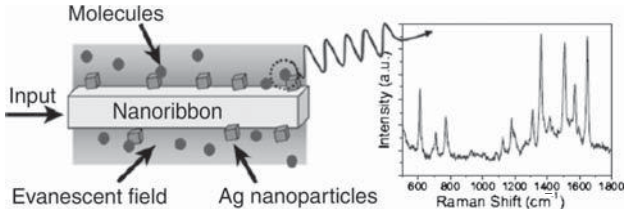
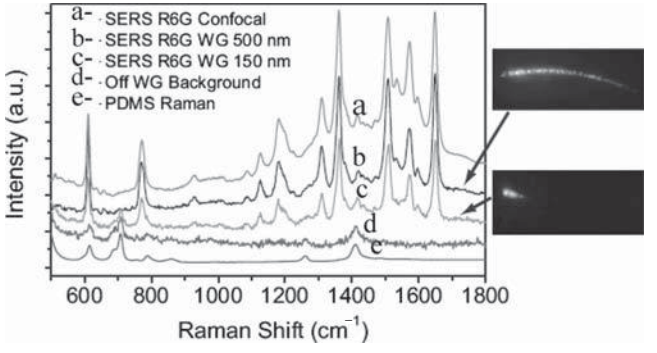


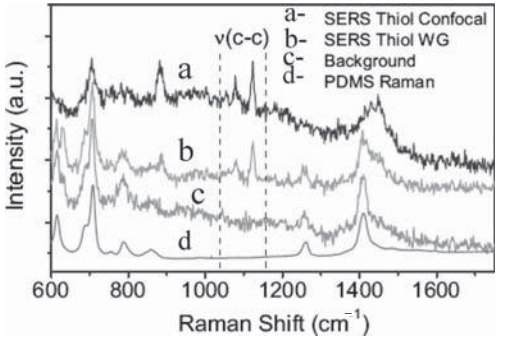
Figure 6.2 Evanescent wave sensors in absorbance and fluorescence modes. (*A*) Schematic illustration of the absorbance geometry. (*B*) Raw waveguided fluorescence spectra before and during the flow of a 3 mM solution of eosin-5-isothiocyanate (EITC) through a single sensing channel. (*Inset*) Cycling of the device through multiple sensing cycles, using pH 12 water to clean the waveguide. The resulting absorption spectrum is shown in (*C*) underneath the raw spectra. (*C*) Absorption spectra of four EITC solutions of different concentrations. (*Inset*) Peak absorbance versus EITC concentration showing the linear response of the sensor in this range. (*D*) Comparison of thin ($d < 150$ nm) and thick ($d > 200$ nm) nanoribbon waveguides. The black traces are the raw waveguide absorption data and the gray traces (normalized) were taken with a conventional UV-visible spectrometer. (*E*) Overlaid absorbance and fluorescence spectra of a 1.84-mM EITC solution using the same waveguide. (*Insets*) Photoluminescence images of a sensor in the presence of EITC (*upper image*) and water (*lower image*). (*F–H*) A series of photoluminescence images, captured at 187 frames s^{-1} (5-ms snapshots), of k-DNA-YOYO1 molecules flowing past a sensor. Here, 442-nm light (<10 nW) is guided from right to left. The arrow in (*G*) denotes a single molecule passing through the evanescent field. Reprinted with permission from Ref. 28.



(*A*)



(*B*)



(*C*)

FIGURE 6.3 Nanoribbon evanescent wave SERS sensor. (*A*), Schematic illustration of the sensor. Analyte molecules in close proximity to a metal-decorated nanoribbon show amplified Raman scattering, which is then detected with the microscope objective. (*B*), Resonant SERS spectra of 100 μM Rhodamine 6G (R6G). Light is delivered to the particles by direct excitation (line *a*) or by the evanescent field of the waveguide (SERS R6G WG, line *b*). Large ($d \sim 500$ nm) and small ($d \sim 150$ nm) waveguides yielded identical spectra. The background (line *d*) was acquired with the beam positioned off the end facet of the waveguide. A Raman spectrum of PDMS (line *e*) verifies that the background results from PDMS. (*Insets*) Scattering images taken of the large (*top*) and small (*bottom*) waveguides. (*C*) Nonresonant SERS of bound dodecanethiol. Direct (line *a*) and waveguide-excited (line *b*) SERS spectra both show the distinct C-C stretching modes of the thiol ligands at 1,080 cm^{-1} and 1,122 cm^{-1}. Background (line *c*) and PDMS Raman (line *d*) spectra are provided for clarity. Reprinted with permission from Ref. 28.

multioptical sensors can hinge on the provision of cheap, fast, and reliable detectors capable of deconvoluting complex mixtures. An imperative step in this process is the addition of chemical specificity to the sensor while simultaneously providing a multiplexed geometry for high-throughput analysis. The sensor is portable, which will certainly benefit from the advent of on-chip microcavity lasers and the continual efforts toward integrating both active and passive optical elements on a single photonic chip. The use of evanescent fields to guide light and to perform spectroscopy may play a major role in the design of next-generation compact optical sensors.[28] Therefore, this sensor is promising for the development of on-site analytical experimentation, field detection of biochemical toxins, and portable analysis of water contaminants.[28]

6.2.2 Metal-Oxide-Nanowire-Enabled Gas Sensors

Increasing awareness of air pollution and personal safety as well as strict control of automotive emissions makes environmental monitoring one of the most important applications for reliable gas sensors. Currently, there is still need to improve sensitivity and selectivity, to shorten response time, and to increase the stability of the sensors, although great progress has been made in the detection of toxic gases as well as poisonous organic vapors including methanol and chloroform.

Solid-state gas sensors play a major role in semiconductor processing, environmental sensing, personal safety, and homeland security.[29] Gas sensors also have a higher economic impact in agriculture, in the automotive and aerospace industries.[29] In Ref. 30, Shimizu and Egashira summarized the basic sensing mechanisms, effects of grain size and the geometry of grain connections, promoting effects of noble metals, effects of sensor configuration, and the prospects of semiconductor gas sensors. The high surface-to-volume ratio of nanowires makes them natural competitors as new sensors. However, the major challenges were to produce quasi-1D nanostructures composed of well-established sensor materials such as SnO_2, ZnO, and TiO_2,[31,32] and to integrate individual nanowires.[29] Nonstoichiometric metal-oxide materials such as In_2O_3, ZnO, and SnO_2 films have been extensively studied for use as toxic-chemical sensors,[33,34] among which ammonia (NH_3),[35] CO,[29] and NO_2 sensors working under practical conditions are particularly interesting for industrial applications and environmental studies. The In_2O_3 nanowires are n-type semiconductors, and the on/off ratio of the FET can reach 1000.[36] It is especially possible to use surface treatment and doping dependence of In_2O_3 nanowires as ammonia sensors via electrical measurements at room temperature.[35] On exposure to a small amount of NO_2 or NH_3, the nanowire transistors showed a decrease in conductance of up to five or six orders of magnitude, in addition to substantial shifts in the threshold gate voltage. The devices exhibit significantly improved chemical

sensing performance compared to existing solid-state sensors in many aspects, such as sensitivity, selectivity, and response time, as well as the lowest detection limits. Interestingly, UV light can be used as a "gas cleanser" for In_2O_3 nanowire chemical sensors, leading to a recovery time as short as 80 seconds.[37]

Nanowires of different metal oxides (SnO_2, ZnO) have been grown by an evaporation-condensation process.[38] The SnO_2 nanowires were used to produce a gas sensor based on a Pt/oxide/SiC structure and operated as a Schottky diode; these have been produced by thermal evaporation.[38] Diffusion of oxygen into the device can affect the response of individual SnO_2 nanowires to this gas. Different oxygen partial pressures lead to strong changes in their electrical resistance, even at room temperature. Because surface models fail to explain the experimentally observed long-term resistance transients, it is necessary to describe the interaction mechanisms between oxygen species and SnO_2 nanowires by taking ion diffusion into account.[39] SnO_2 is a wide-bandgap (3.6 eV) semiconductor; thus, for an n-type SnO_2 single crystal, the intrinsic carrier concentration is primarily determined by deviations from stoichiometry in the form of equilibrium oxygen vacancies, which are predominantly atomic defects. This is because the electrical conductivity of nanocrystalline SnO_2 depends strongly on surface states produced by molecular adsorption, which results in space-charge layer changes and band modulation. NO_2, a combustion product that plays a key role in tropospheric ozone and smog formation, acts as an electron-trapping adsorbate on SnO_2 crystal faces and can be sensed by monitoring the electrical conductance of the material.[40] Because NO_2 can chemically adsorb strongly on many metal oxides,[41] commercial sensors based on particulate or thin-film SnO_2 operating at 300–500°C can enhance the surface molecular desorption kinetics and continuously "clean" the sensors.[42] The high-temperature operation of these oxide sensors is not favorable in many cases, particularly in an explosive environment. Individual SnO_2 nanoribbons are small, fast, and sensitive devices for detecting ppm-level NO_2 at room temperature under UV light, because these nanodevices can be operated under laboratory conditions over many cycles without loss of sensitivity.[40] Therefore, the advantages of low-temperature and potentially drift-free operation make SnO_2 nanoribbons good candidates for miniaturized, ultrasensitive gas sensors.[40] Further increase in sensitivity should be achievable by using thinner nanoribbons, developing ohmic SnO_2-metal contacts, and decorating these structures with catalysts. With such innovations, the chemical detection of single molecules on nanowires may soon be realized.

A soft-chemistry route was performed to self-assemble crystalline tungsten oxide nanowires into bundles at low temperature.[43] The controlled synthesis of 1D tungsten oxide nanowires is particularly fascinating because bulk tungsten oxide exhibits manifold

properties, including electrochromism, semiconductivity, catalytic activity, and sensing properties. The high surface-to-volume ratio combined with the high purity of the material makes these nanowire bundles ideal candidates for gas-sensing devices. Actually, tungsten oxide nanowire-based sensors exhibited an extraordinarily high sensitivity to NO_2. Another major advantage of the tungsten oxide sensor at low temperature is not only the possibility of fabricating low-energy-consumption devices, but also the ability to tailor the gas-sensing properties of the nanobundles by in situ functionalization of the surface with specific organic and bioorganic receptors in order to provide high selectivity.[43]

The detection of organic vapors in the air is very important, because almost all organics are hazardous. Chiang et al. found that efficient chemical sensors can be realized with $LiMo_3Se_3$ nanowires in the Chevrel phase.[44,45] Bundles of several tens of $LiMo_3Se_3$ nanowires can be obtained by dissolving $LiMo_3Se_3$ in water or in *dimethyl sulfoxide* (DMSO). The drop-coating of the nanowire solutions onto solid substrates followed by solvent evaporation produces nanometer-thick metallic films that react to chemical species with an increase in their electrical resistance (Fig. 6.4). Lithium iodide (LiI)- and *cetyltrimethylammonium bromide* (CTAB)-doped nanowire films can be manufactured by mixing the nanowires with LiI in solution or by diffusing CTAB into films. The additives lead to a decrease in the electrical conductivity of the films. However, LiI increases the electrical film response to polar analytes, whereas *cetyltrimethylammonium* (CTA) increases the electrical film response to nonpolar analytes.[45] The LiI-doped $LiMo_3Se_3$ nanowire films can be used for the detection of several organic solvents (see Fig. 6.4). After injection into the test chamber, all analytes adsorb quickly onto the nanowire films. Generally, 90% of the adsorption is completed within 5 s. Only the combination of methanol and the nonmodified $LiMo_3Se_3$ nanowire film extended the adsorption time beyond 60 s. These authors attributed this continuing adsorption to partial dissolution of the nanowire film in the presence of the good solvent methanol at relatively high partial pressure (13.25 torr).[45] Adsorption also strongly depends on the analyte and on the doping agent in the film. LiI-doped films adsorb methanol and water more strongly than native and CTAB-doped films. CTAB-doped films, on the other hand, have a stronger affinity for hexane than for water or methanol. This $Mo_6S_3I_6$ nanowire networks can change their resistance in response to the presence of analyte vapors such as methanol, ethanol, acetone, water, ammonia, chloroform, and pyridine.[46]

6.2.3 Nanowire-Enabled Humidity Sensors

Humidity control is important in science, technology, and daily life. Over the years, many detection techniques have been explored, from

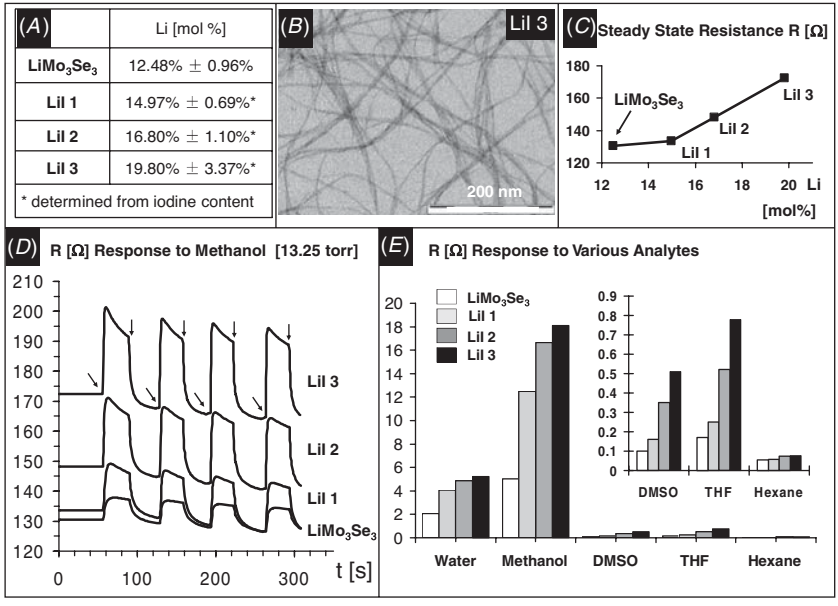


FIGURE 6.4 Sensing properties of LiI-doped $LiMo_3Se_3$ nanowire films. (*A*) Li content and labeling scheme (molar percentages are given according to [Li]/([Li] + [Mo] + [Se]) × 100); (*B*) TEM image of LiI/$LiMo_3Se_3$ (LiI 2); (*C*) steady-state resistance data; (*D*) methanol (13.25 torr)-induced resistance data (addition and removal of analyte are shown with arrows); (*E*) resistance response of several LiI/$LiMo_3Se_3$ films to vapors of water (1.23 torr), methanol (13.25 torr), DMSO (0.04 torr), tetrahydrofuran (7.60 torr), and hexane (7.55 torr). Reprinted with permission from Ref. 45. Copyright © 2006 American Chemical Society.

the old wet- and dry-bulb thermometry to modern capacitive, resistive, and thermally conductive moisture detectors.[47] To further promote the sensitivity, selectivity, and chemical and thermal stability of detectors, intensive efforts have been made to explore a humidity sensor based on nanostructured materials such as carbon nanotubes[48] and nanowire films.[47] For example, a humidity sensor using a single SnO_2 nanowire based on a FET nanodevice has been fabricated.[47] A single SnO_2 nanowire of 250 nm in diameter is placed between two Au electrodes of 100-nm thickness and deposited with Pt by focused ion beam microscopy as the top electrode to improve contact. In order to measure the current signals through the SnO_2 nanowire, two Au electrodes are connected with a support chip by an Au wire binding technique. This sensor has fast and sensitive response to relative humidity (RH) in air from a wide range of atmospheres at 30°C. The response sensitivity of the sensor to RH is linear to 90%.[47] The interaction between water vapor and the surface of the nanowire is mainly

dominated by physical adsorption. Therefore, the response can be reversible when the humidity changess.

6.2.4 Metal-Oxide Nanowires for Bacterial Pathogen Sensing

Foodborne and waterborne bacterial pathogens are a serious health threat worldwide. The major foodborne pathogens include *Salmonella typhimurium*, *Listeria monocytogenes*, *Staphylococcus aureus*, *Campylobacter jejuni*, *Clostridium perfringens*, *Yersinia enterocolitica*, and *Escherichia coli* O157:H7.[49] The principal waterborne pathogens of concern are *E. coli* O157: H7, *Campylobacter jejuni, Salmonella typhimurium*, *Salmonella java*, *Shigella sonnei*, *Shigella flexneri,* and *Leptospira grippotyphosa*.[50,51] The emerging bacterial pathogens of concern are *Legionella*, *Mycobacterium avium* complex (Mac), *Aeromonas hydrophila*, and *Helicobacter pylori*.[50,51] Either current or emerging concerns are those commonly recognized as the etiological agents in waterborne outbreaks or those being recognized more often as causes of other serious illnesses that have the potential for waterborne transmission.[51] The conventional methods, for instance, biochemical tests, plating and culturing, flow cytometry, microscopy, and luminescence, have mainly depended on time-consuming enrichment steps, followed by biochemical identification, having a total assay time of up to 1 week. Biosensors based on a combination of biological receptors and physical or chemical transducers present a unique technology with great potential to meet the need for the rapid, online, real-time detection of biological agents.[52] Nanowires may offer new and sometimes unique opportunities in this rich and interdisciplinary area, because the diameters of the nanowires can be comparable to the sizes of biological and chemical species being detected, and thus represent excellent primary transducers for producing signals that ultimately interface with macroscopic instruments. Another field of the development of nanowires is to explore biosensing applications. Nanostructured device-fabricated metal oxide nanowires (e.g., In_2O_3 nanowires[53]) are good candidates to manufacture future generations of biosensors. Nanotubes and nanowires have very high surface-to-volume ratios and, therefore, promise very high sensitivities. It has been proven to be possible to use either nanowires or carbon nanotubes as successful sensors for a number of biological analytes.[54] Therefore, the combination of these two nanomaterials may offer an interesting comparison and also become a novel sensing strategy.

Inorganic nanowires exhibit unique electrical properties[55–58] that can be exploited for sensing.[59,60] Nanowire-based rapid and sensitive diagnosis of viruses was reviewed in Ref. 61. Lieber and his co-workers reported direct, real-time electrical detection of single virus particles with high selectivity by using nanowire FETs.[59,62] Measurements

made with nanowire arrays modified with antibodies for influenza A showed discrete conductance changes characteristic of binding and unbinding in the presence of influenza A but not paramyxovirus or adenovirus. Simultaneous electrical and optical measurements using fluorescently labeled influenza A were used to demonstrate conclusively that the conductance changes correspond to binding/unbinding of single viruses at the surface of nanowire devices.[62] The pH-dependent studies further show that the detection mechanism is caused by a field effect, and that the nanowire devices can be used to rapidly determine isoelectric points and variations in receptor-virus binding kinetics for various conditions.[62] Studies of nanowire devices modified with antibodies specific for either influenza or adenovirus show that multiple viruses can be selectively detected in parallel.[62] The possibility of large-scale integration of these nanowire devices suggests potential for simultaneous detection of a large number of distinct viral threats at the single-virus level.[59,62] With the incorporation of field-effect transistor compatible technology, *complementary metal-oxide semiconductor* (CMOS) nanowire-based label-free immunodetection can be used for the specific detection of below 100-fM concentrations of antibodies as well as for real-time monitoring of the cellular immune response (Fig. 6.5).[63] This approach eliminates the need for hybrid methods and enables system-scale integration of these sensors with signal processing and information systems.[63] In addition, the ability to monitor antibody binding and sense the cellular immune response in real time with readily available technology should facilitate widespread diagnostic applications.

Peptide tags for enhanced cellular and protein adhesion to single-crystalline sapphire (α-Al_2O_3) permit conformation alignment of the basic amino acids toward the surface so that the charged groups can undergo local electrostatic interactions with the surface oxide.[64] In this approach, peptide K1 ($-(GK)_6$) was cloned onto the C terminus of *maltose binding protein* (MBP), and the resultant mutant protein showed a half-maximal binding at 10^{-7} to 10^{-6} M, which showed an approximately 500- to 1000-fold improvement in binding to sapphire's A-face compared with wild-type MBP. Targeting proteins to metal oxide surfaces with peptide tags may provide a facile one-step alternative coupling chemistry for the formation of protein bioassays and biosensors.[64] Biomolecules can covalently attach to the electrochemically active surface of In_2O_3 nanowire mat devices. A *self-assembled monolayer* (SAM) of *4-(1,4-dihydroxybenzene)butylphosphonic acid* (HQ-PA) was generated on an *indium tin oxide* (ITO)-coated glass and In_2O_3 nanowire surface. The hydroquinone group contained in the HQ-PA SAM can be electrochemically oxidized to quinone (Q-PA) at +330 mV. The monolayer of Q-PA was allowed to react with a thiol-terminated DNA. Arrays of In_2O_3 nanowires on a single substrate were electrochemically activated in a selective manner to Q-PA. Activated In_2O_3

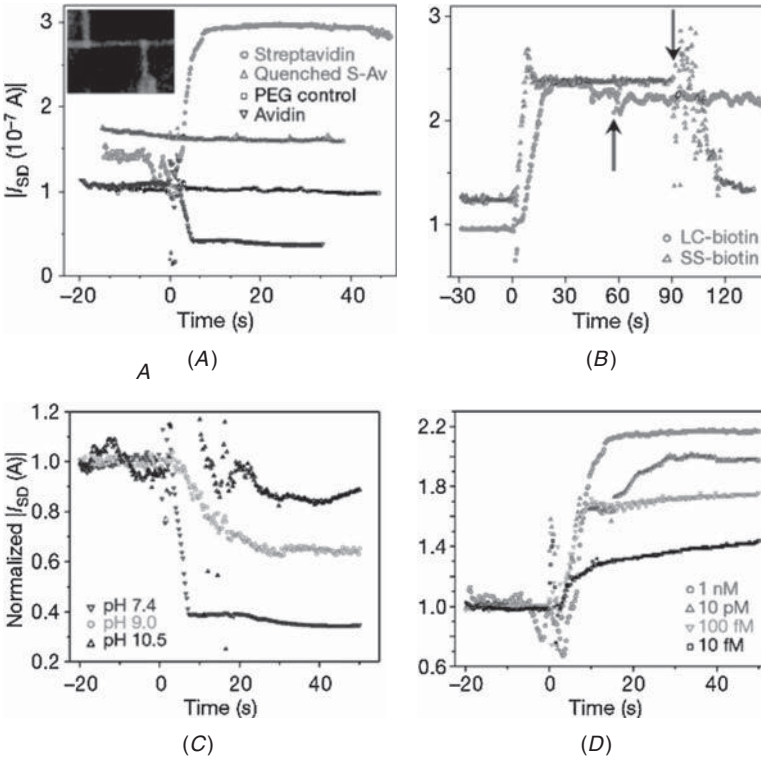


Figure 6.5 Label-free immunosensor with CMOS-compatible semiconducting nanowires for protein detection. (*A*) Specific recognition and protein charge determination of avidin/streptavidin. All additions used 1-nM solution. The inset shows a fluorescence micrograph of a biotin-functionalized device after fluorescently labeled streptavidin addition. (*B*) Verification of surface charge by cleavage. Streptavidin (1 nM) addition to LC-biotin- or SS-biotin-functionalized devices. The arrow indicates reducing agent [tris(2-carboxyethyl)phosphine] addition. (*C*) Biotinylated sensor response to protein charge, by addition of 1-nM avidin in buffers with different pH values. (*D*) Detection response with decreasing streptavidin concentration. For (*C*) and (*D*), currents were normalized by dividing the measured I_{SD} by the pre-addition average current. Reprinted with permission from Ref. 63.

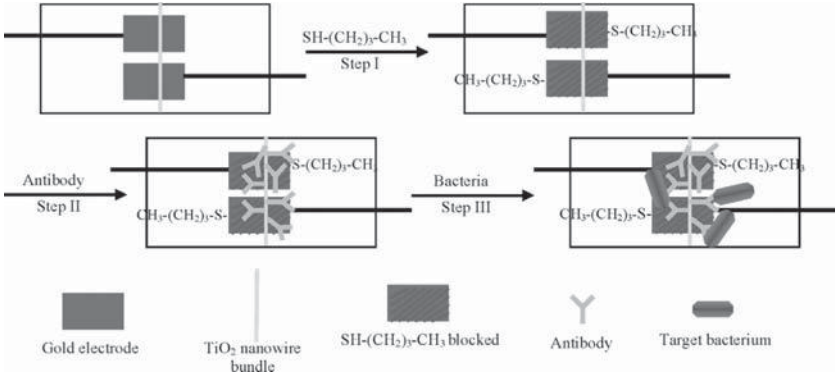
nanowires underwent reaction with HS-DNA and gave a positive fluorescence response after pairing with the dye-DNA. The DNA was paired to its complementary strand tagged with a fluorescent dye. A device was subsequently prepared on a SiO_2-supported mat of In_2O_3 nanowires by depositing gold electrodes on the mat surface. The reaction strategy optimized on ITO was applied to this In_2O_3 nanowire-based device. The unactivated In_2O_3 nanowires gave no response, thus demonstrating selective functionalization of an In_2O_3 nanowire array.

This may be a key step for the fabrication of large-scale, inexpensive, nanoscale biosensors in the future.[53]

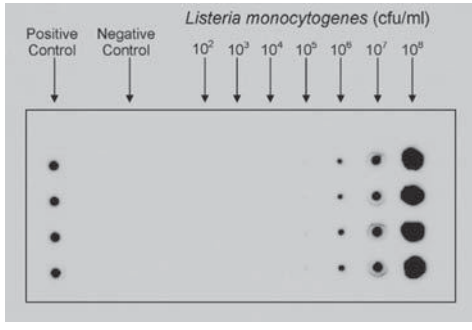
The direct detection of biomolecules based on In_2O_3 nanowires is also reported. For instance, *prostate-specific antigen* (PSA) is an oncological marker for the presence of prostate cancer, which may be the most frequently diagnosed cancer among men. PSA can be complementarily detected using *n*-type In_2O_3 nanowires and *p*-type carbon nanotubes based on covalent attachment of antibodies to In_2O_3 nanowire surfaces via the on-site surface synthesis of a succinimidyl linking molecule. The In_2O_3 nanowires and *single-walled carbon nanotubes* (SWNTs) were combined for the detection of PSA, which revealed complementary electrical response on PSA binding.[65] Furthermore, detection of PSA in solution has been demonstrated to be effective as low as 5 ng/mL, a level useful for clinical diagnosis of prostate cancer.[65] This work will significantly promote the incorporation of nanomaterials into medically relevant biosensors.

On the other hand, the immunologically based biosensors or immunosensors (based on antibody-antigen affinity reactions) are among the most promising because of their high specificity and versatility in the detection of bacteria. A novel TiO_2 nanowire-bundle microelectrode-based immunosensor was demonstrated as a sensitive, specific, and rapid technology for detection of *L. monocytogenes* on the basis of immunoassay dot-blot analysis.[66] The TiO_2 nanowire bundle was connected to gold microelectrodes with mask welding. Monoclonal antibodies were immobilized on the surface of a TiO_2 nanowire bundle to capture *L. monocytogenes* specifically. Impedance change caused by the nanowire-antibody-bacteria complex was measured and correlated to bacterial number (Fig 6.6*A*). This nanowire-bundle-based immunosensor could detect as little as 10^2 cfu/mL of *L. monocytogenes* in 1 h without significant interference from other foodborne pathogens (Fig. 6.6*B*).[66]

Recently, electrochemical intracellular sensors based on ZnO nanowires have been demonstrated as efficient nanosensors for monitoring human cell activity with minute pH changes.[67] This was empirically established in several experiments in which, after ZnO nanowire penetration and equilibration for 5 min, the electrode was withdrawn and the cells were monitored by microscope. This study demonstrated that ZnO nanowires are minimally invasive tools appropriate for monitoring pH changes inside living cells. The ZnO nanowire electrode was used to obtain only one measurement at a specific time and was not reused. Calibration measurements of the solution surrounding the cell after the measurement inside the cell can allow quantitative estimation of the detection signal. For calibration, the ZnO nanowire electrode was placed in the solution surrounding the cells directly after the intracellular measurement and obtained a pH value of 6.77, whereas the actual pH value of the surrounding solution was 7.4; so,



(*A*)



(*B*)

Figure 6.6 (*A*) Schematic illustration of bacteria detection using TiO_2 nanowire-bundle-microelectrode based impedance immunosensor. (*B*) Detection of *Listeria monocytogenes* based on immunoassay dot-blot analysis. Reprinted with permission from Ref. 66. Copyright © 2008 American Chemical Society.

this difference between the actual and the measured pH values should come from the strong association constant of the binding to the cell material.[67] The introduction of the ZnO-nanowire-based pH sensors into a single cell's cytoplasm can measure the intracellular pH value without obviously affecting cellular viability.

6.2.5 Metal Oxide Nanowires for Biosensing

Hydrogen peroxide (H_2O_2) is the product of many enzymatic reactions that are catalyzed by a large number of oxidases. The H_2O_2 concentration can be correlated to the concentration of target substrates, which is practically important in the field of biosensor development. Luminescent cadmium(II) (8-hydroxyquinoline) chloride (CdqCl) (here 8-hydroxyquinoline is expressed as q) complex nanowires can

be synthesized via a sonochemical solution route with a chemical composition of $Cd(C_9H_6NO)Cl$.[68] Transmission electron microscopy and scanning electron microscopy images show that the CdqCl nanowires are approximately 50 nm in diameter and approximately 2–4 mm in length. Cdq_2 micrometer-scaled flakes can be transformed to CdqCl nanowires by increasing the ratio of $CdCl_2$ to q. A new fluorescent sensing strategy for detecting H_2O_2 and glucose has been developed based on the combination of luminescent nanowires and the biocatalytic growth of *Au nanoparticles* (AuNPs).[68] An investigation of the quenching effects of AuNPs and $AuCl_4^-$ on the fluorescence of CdqCl nanowire has shown that the dominant factor for the fluorescence quenching of CdqCl nanowires is that the Stern-Volmer quenching constant of AuNPs is larger than that of $AuCl_4$.[68] On the other hand, vertically aligned copper oxide (CuO) nanowires were synthesized by directly heating copper foil on a hot plate under ambient conditions. The as-grown CuO nanowire film is mechanically stable and was facilely attached to a *glassy carbon* (GC) electrode, offering an excellent electrochemical sensing platform. The CuO nanowire electrode shows excellent electrocatalytic response to H_2O_2 with significantly lower overpotentials at –0.2 V (vs. Ag/AgCl) for its oxidation and reduction and also exhibits a fast response (5 s) and high sensitivity of 204.15 mA cm^{-2} for the amperometric detection of H_2O_2. The novel vertically aligned CuO nanowire electrode is readily applicable to other analytes and has great potential applications in the electrochemical detection.[69]

6.3 Metal Oxide Nanotube-Based Sensing

6.3.1 Metal Oxide Nanotube-Based Gas Sensing

The tubular morphology is particularly attractive for sensing applications because it may provide access to three different contact regions: the inner and outer surface as well as the tube ends.[70] Therefore, tubular structures are advantageous over nanoparticles in exploring nanodevices. Many synthetic procedures, such as sulfurization by heating, decomposition of precursor crystals, solvothermal synthesis, and template-based synthesis, are used for the synthesis of inorganic nanotubes.[71–73] Therefore, a wide range of metal-oxide nanotubes are prepared.[74–77] Optically transparent titanium oxide nanotube-array films can serve as excellent hydrogen sensors, which exhibited a four-order magnitude drop in resistance with exposure to 1000 ppm hydrogen at room temperature.[78] A novel strategy was developed to synthesize porous and polycrystalline In_2O_3 nanotubes with diameters of about 20–60 nm using layer-by-layer assembly on CNT templates in combination with subsequent calcination. This novel

approach can be extended to synthesize other metal oxide nanotubes such as NiO, SnO_2, Fe_2O_3, and CuO.[79] Hematite (α-Fe_2O_3) is the most stable iron oxide with n-type semiconducting properties under ambient conditions. α-Fe_2O_3 nanotubes can be used for gas sensing materials.[80] Vanadium oxide nanotubes (VO_X-NTs) can used as nitric oxide (NO) gas sensors.[81] This gas sensor consisted of a gas-responsive multiwalled VO_X-NT layer deposited on a ceramic chip with two Ag-Pd electrodes, a gas sensor signal collecting system, and a computer data-processing system. The absorption of different gases in the VO_X-NTs layer changed the permittivity and conductivity of the material and consequently altered the voltage of the sensor, whose response to NO was both sensitive and reversible at room temperature.[81] By measuring the voltage change of the sensor, various gas concentrations could be determined. The VO_X-NTs-based gas sensor responded only to NO and water vapor in the exhaled air, which can meet the demands of clinical diagnosis of exhaled NO.[81]

MCo_2O_4 (where M denotes Ni, Cu, or Zn) nanotubes were prepared by a porous alumina-template method, and the application of the MCo_2O_4 nanotubes to gas sensors displayed excellent selectivity and high sensitivity to various gases such as ethanol and SO_2 due to the 1D electron-conductivity characteristic and hollow nanotube structure.[82] Moreover, the In_2O_3 nanotubes exhibited superior sensitivity to ammonia at room temperature, as well as good reproducibility and short response/recovery time because of their ultrahigh surface-to-volume ratio, polycrystallinity, and porous structure.[79] Generally, nanotube-based gas sensors show better sensitivity than nanowire-based sensors if both have the same chemical composition, which contributes to the better enriching ability of hollow-structured nanotubes.

6.3.2 Titanate Nanotube-Based Electrochemical Sensors

Electrochemical biosensors have extensive applications in the point-of-care diagnostic devices that are used along with handheld analyzers for rapid, onsite delivery of diagnostic information. Such portable electrical devices play an increasing role in health care, homeland security, and environmental monitoring. The development of nanotechnology offers great potential for improvement in point-of-care devices. The nanotubes are unique nanostructures with uniform nanometer-sized channels possessing electronic conductivity and high specific surface area. Additionally, they are physically and chemically stable. Although metal-oxide-based nanotubes are widely reported, their applications in electrochemical sensors are fewer. The main problems may lie in the fact that it is difficult to pretreat nanotube powder to make it dispersible. Another reason is that most nanotubes lack electrochemical activity. TiO_2 nanotubes have been most studied because

of their electronic and optical characteristics; therefore, their applications in photocatalysis and rechargeable lithium batteries have been explored, though the main work on these nanotubes is still focusing on the synthesis process.[83,84] On the other hand, *titanate* ($H_2Ti_3O_7$) *nanotubes* (TNTs) have aroused great interest. Composed of corrugated ribbons of edge-sharing TiO_6 octahedra[85] and of multilayered structures with a nanometer-scale inner-core cavity exposed to the outer surface,[86] TNTs may provide a unique reaction vessel for analytes. It has been recently reported that $H_2Ti_3O_7$ might be protonic by nature; therefore, the surface of the TNTs may easily be negatively charged after treatment with weak bases.[83,85] Furthermore, active groups such as hydroxyls on the surface of nanotubes may exhibit some kind of interaction with the analytes in the solution. Actually, the electrochromism and electrochemical properties and their applications on the basis of TiO_2-NTs and titanate nanotubes have been researched.[87] Therefore, the preparation of transition-metal-oxide nanotubes such as titanium-dioxide (titania, TiO_2) nanotubes and TNTs[88,89] as well as VO_x-NTs.[70,90–92] has attracted great attention. A recent overview of TNT-based electrochemical sensing can be found elsewhere.[93] In this section, the use of TNTs for novel electrochemical sensors.[88,89,94] is highlighted, and titanate nanostructures with various morphologies for electrochemical sensing are compared.

Heme Protein Immobilized in Titanate Nanotubes Retaining Peroxidase Activity and Exhibiting Direct Electron Transfer

The enzyme electrode is the fundamental component of amperometric biosensors. The selection of appropriate combinations of materials such as enzyme, electron transport mediator, binding and encapsulation materials, conductive support matrix, and solid support governs the efficiency of the electrodes in terms of electron transfer kinetics, mass transport, stability, and reproducibility for the construction of enzyme-modified electrodes. Studies of redox protein immobilized in metal-oxide nanotubes can help in understanding the interaction mechanism between protein and membrane as well as providing another approach to enzyme engineering. Transmission electron micrographs show that TNTs are hollow tubes with two open ends. Each single nanotube is made up of three to four layers with an intershell spacing of ~0.4 nm, and the inner diameter is 4–5 nm according to TEM images.[86] Therefore, the TNT morphology may be suitable for the encapsulation of *myoglobin* (Mb) considering that the size of Mb is of 2.5 × 3.5 × 4.5 nm.[89] The spectroscopic properties can be used to confirm the protein state in the composite. For instance, the Soret peak for Mb in TNT film is not obviously changed, which suggests that Mb is not denatured.[89,95] *Fourier transform infrared* (FT-IR) spectroscopic studies showed that Mb exhibited an actually undisturbed second structure in the Mb-TNT film.[89]

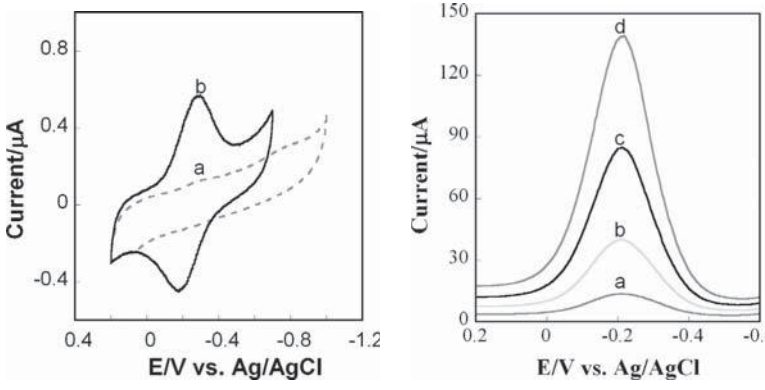


Figure 6.7 (*A*) Cyclic voltammograms of TNT/PG electrode (*a*) and Mb-TNTs/PG electrode (*b*). CVs were measured in 0.1 M HAc-NaAc buffer solution (pH 5.5). Scan rate, 0.1 V s^{-1}. (*B*) Square-wave voltammograms (SWVs) of Mb-TNT/PG electrode in 0.1 M HAc-NaAc buffer solution (pH 5.5). SWV conditions: potential amplitude, 100 mV; equilibration time, 5 s; step height, 4 mV; and frequency, (*a*) 25 Hz, (*b*) 50 Hz, (*c*) 75 Hz, and (*d*) 100 Hz. Reprinted with permission from Ref. 89. Copyright © 2005 American Chemical Society.

Figure 6.7*A* shows *cyclic voltammograms* (CVs) of TNT- and Mb-TNT-cast film-covered basal plane *pyrolytic graphite electrodes* (PGEs) in acetate buffer (pH 5.5). TNT-cast film-covered PGEs exhibited no redox peaks within the potential window studied; however, a nearly reversible redox couple with the apparent formal peak potential (E_p) of –0.239 V was observed for the Mb-TNT composite-covered PGE, which indicates that the direct electron transfer of Mb is achieved through the incorporation of Mb into TNT film. Both the cathodic peak current (i_{pc}) and the anodic peak current (i_{pa}) increased linearly with a scan rate up to 5 V s^{-1}, characteristic of thin-layer electrochemistry.[96] The average surface concentration of electroactive Mb in TNT film was estimated to be 0.15 nmol, accounting for about 15% of the total amount of Mb on the electrode surface. The electron-transfer of Mb within the TNTs film was further studied by *square-wave voltammetry* (SWV). SWV is known to be powerful in characterizing the electrochemistry of interfacially confined redox species.[97] A typical square-wave voltammogram of Mb-TNTs is shown in Fig. 6.7*B*. On the basis of a nonlinear regression analysis program derived from the theory for SWV of a surface-confined species of apparent standard potential values, the apparent heterogeneous electron-transfer rate constant can be calculated.[98,99] The k_{ET} value for Mb in TNTs was 86 ± 7 s^{-1} based on the program reported by Li and colleagues[99] However, the k_{ET} values for Mb immobilized in some surfactant films were reported to be

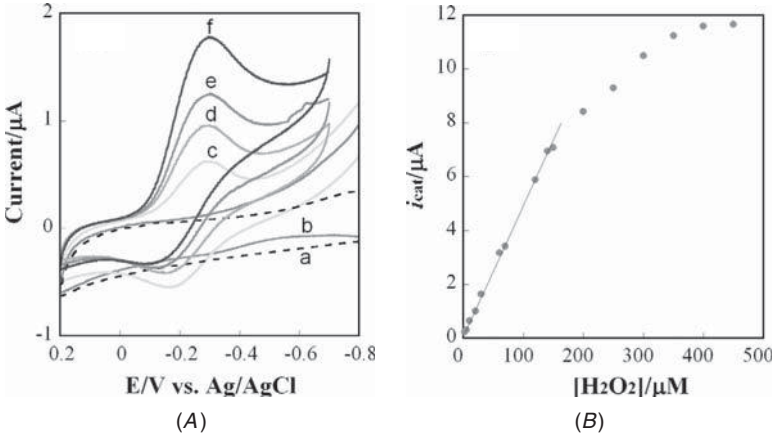


Figure 6.8 (*A*) Cyclic voltammograms of the TNTs/PG electrode (*a*) in the absence and (*b*) in the presence of 150 μM H_2O_2. (*c–f*) Cyclic voltammograms of the Mb-TNTs/PG electrode in the presence of (*c*) 0, (*d*) 5, (*e*) 10, and (*f*) 20 μM H_2O_2. Cyclic voltammograms were measured in 0.1 M HAc-NaAc buffer solution (pH 5.5). Scan rate, 0.2 V s^{-1}. (*B*) Electrocatalytic current (i_{cat}) as a function of H_2O_2 concentration for the Mb-TNT/PG electrode. Reprinted with permission from Ref. 89. Copyright © 2005 American Chemical Society.

within 30–59 s^{-1}.[100] Therefore, it is obvious that Mb exhibited a higher electron-transfer rate constant in TNTs film than that in other films. The enzymatic activity of Mb in the TNT film was examined by studying its ability to electrocatalytically reduce hydrogen peroxide (H_2O_2) using the Mb-TNT film-modified electrode. The cathodic peak (–0.3V) was significantly enhanced in the presence of H_2O_2, whereas the corresponding anodic peak decreased, suggesting that an electrocatalytic reduction of H_2O_2 occurred (Fig. 6.8*A*). The i_{pc} value increased with the increasing concentration of H_2O_2 added. No peaks were observed at the TNT-only cast electrode in the presence of H_2O_2. The electrocatalytic current (i_{cat}) linearly increased with increasing concentration of H_2O_2 in the beginning and thereafter began to level off, suggesting that the immobilized enzyme responds to the presence of the substrate in a Michaelis-Menten model (Fig. 6.8*B*). Herein, the i_{cat} value is defined as the difference between i_{pc} in the presence of H_2O_2 and i_{pc} in the absence of H_2O_2 for the Mb-TNTs electrode. The i_{cat} values are linear with increasing concentration of H_2O_2 in the range of 2–160 μM for the Mb-TNTs electrode. The lower detection limit is 0.6 μM H_2O_2. The Lineweaver-Burk plot shows an apparent Michaelis-Menten constant (K_M) of 140 μM. Compared with other films reported thus far, the Mb-TNT film presented excellent catalytic performance in the detection of H_2O_2: for example, lower detection limit and wider linear

range. The Mb-TNT film demonstrated a smaller K_M value, indicating that Mb entrapped in the TNT film shows higher peroxidase-like activity.[89] The enhanced direct electron transfer for heme proteins immobilized into titanate nanotubes has an impact on the development of third-generation biosensors with higher sensitivity.

On the other hand, TNTs were used to immobilize *lactate oxidase* (LOx) to prepare electrochemical biosensors for detection of lactate.[101] The nanotubes offered a pathway for direct electron transfer between the electrode surface and the active redox centers of LOx, which enabled the biosensor to operate at a low working potential and to avoid the influence of O_2 presence on the amperometric current response. The biosensor exhibited a sensitivity of 0.24 μA cm^{-2} mM^{-1}, a 90% response time of 5 s, and a linear response in the range from 0.5 to 14 mM.[101] Although the direct electron transfer between the electrode and the redox center of enzymes obviated the need for redox mediators for electrochemical enzymatic sensors,[101] there is no breakthrough compared with the pioneering work of direct electrochemistry of Mb immobilized in TNT film.[89] Very recently, layered *titanate nanosheets* (TNS) intercalated with Mb[102] or *horseradish peroxidase* (HRP)[103] for direct electrochemistry has also been reported. However, neither the HRP-TNS film-coated electrodes nor those coated with Mb-TNS film showed improved analytical performance. Thus, layered nanosheets may be comparable with multilayered nanotubes in the enhancement of electron transfer. Nevertheless, the stability of the heme-protein-TNS films is unknown. Other strategies, such as co-immobilization of HRP and chitosan onto Au-modified TiO_2 nanotube arrays for electron transfer, have been reported; however, the sensitivity is lower.[104] It may be limited by the active amount of HRP on the nanotubes. The pursuit of novel nanostructures may lead to new opportunities in applications. For example, carbonized TiO_2 nanotubes (TNT/C) prepared by carbonization with organic polymers possessed advantages contributed by the high conductivity of carbon and the nanostructure of TiO_2 nanotubes.[105] The TNT/C nanotube was used as a supporting matrix to immobilize *hemoglobin* (Hb) to explore its direct electron transfer ability.[105] For better comparison, the analytical properties of some heme proteins encapsulated in various nanostructures are listed in Table 6.1.

Tunable Titanate-Nanotube Electrode Sensitive to Nitrate Ion in Solution

Transition-metal elements display a number of oxidation states with possible redox-active properties.[111] Therefore, the development of transition-metal NTs holds great significance for novel sensing applications. These transition-metal-oxide NTs have two unique structural features, mixed cation valences and an adjustable oxygen deficiency, which are the bases for creating and tuning many novel electric,

Film	Detection Range (μM)	Detection Limit (μM)	References
Mb-titanate nanotubes	2–160	0.6	89
Mb-nanocrystalline TiO_2	6–80	3.0	89
Mb-titanate nanosheets	2–160	0.6	102
HRP-titanate nanosheets	2.1–185	0.7	103
HRP-Au-TiO_2 nanotube	5–400	2	104
Hb-TNT/C	1–100	0.94	105
Mb-mesoporous silica	4–124	0.8	106
HRP-silica sol-gel	20–2,600	n.a.	107
Mb-zirconium phosphonates	n.a.	n.a.	108
Mb-$CaCO_3$ multilayer	5–80	2.0	109
Mb-magadiite nanocomposite	n.a.	n.a.	110

n.a., not available.

Table 6.1 Sensing Properties of Heme Proteins Immobilized in Nanostructures

chemical, optical, and magnetic properties.[10] For instance, the redox properties of TiO_2 changed when human serum albumin adsorbed onto a TiO_2-nanoparticle (TNP)-coated electrode.[112] Here an interesting property of the titanate-nanotube-based electrode is introduced. Figure 6.9 shows CVs of TNT/PGE in the presence of different concentrations of nitrate. The anodic peak at –1.2 V decreased with the increasing concentration of nitrate in the buffer solution. Meanwhile, another pair of redox peaks with an anodic peak at –1.58 V gradually appeared on the addition of nitrate. This is an unexpected finding, because nitrate is an electrochemically inactive anion. The anodic peak at –1.58 V increased with the increasing concentration of nitrate up to 1.2 mM; then, this peak decreased with a further increase in nitrate concentration and finally disappeared when nitrate was above 5.6 mM (Fig. 6.9*B*). In all cases, a systematically negative shift in the redox peak potential was observed when the nitrate concentration increased.[94] More interestingly, the appearance/disappearance of the redox peaks can be tuned with the immersion of the electrode from acetate buffer solution to nitrate solution. The redox peaks disappeared when the electrode was dipped in 8.0-mM nitrate solution (Fig. 6.10*B*). However, the redox peak recovered when the electrode was rinsed and immersed in bare acetate buffer (Fig. 6.10*C*). The redox peak shape and peak size with the same peak potential were restored. Figure 6.10

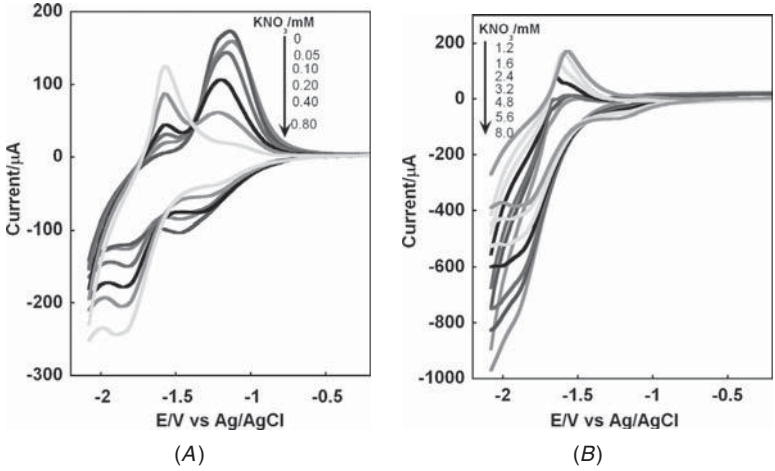


Figure 6.9 Cyclic voltammograms of TNTs/PG electrode in the presence of different concentration of KNO_3 in 0.1 M acetate buffer solution (pH 5.5). Nitrate concentration is shown on the arrow. (*A*) and (*B*) show the systematic CV change varying the KNO_3 concentration. Scan rate, 0.2 Vs^{-1}. Reprinted with permission from A. Liu et al., *Applied Physics Letters*, vol. 90, 253112, 2007. Copyright © 2007 American Institute of Physics.

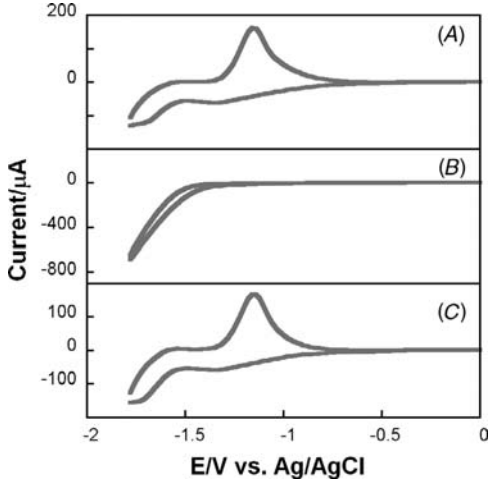


Figure 6.10 Cyclic voltammograms of TNT/PG electrode. (*A*) and (*C*): 0.1 M bare acetate buffer (pH 5.5); (*B*): 0.1 M acetate buffer solution(pH 5.5) containing 8.0 mM nitrate. The sequence of CV measurement was (*A*) → (*B*) → (*C*). CVs were measured by switching the TNT/PG electrode between 0.1 M bare acetate buffer and 8.0 mM nitrate solution, rinsing the electrode with water after measurement in nitrate solution. Scan rate, 0.2 Vs^{-1}. Reprinted with permission from A. Liu et al., *Applied Physics Letters*, vol. 90, 253112, 2007. Copyright © 2007 American Institute of Physics.

demonstrates the tunable results of one cycle for the TNTs/PG electrode changing between 0.1 M acetate buffer in the absence and in the presence of 8.0 mM nitrate. It should be noted here that the effects can be repeated for many cycles, just like a switch with an on/off function. Also, any CVs in the presence of intermediate nitrate concentration can be reversibly recovered when the electrode is transferred into bare acetate buffer. TNP film also exhibited similar effects on the redox properties of Ti(IV)/Ti(III), though the anodic peak current response for TNP/PGE was obviously lower than that for TNTs/PGE, confirming a decisive role of the surface states as an origin of the effect.

Generally, the reduction of Ti(IV) is consistent with the formation of Ti(III) on the surface sites and accompanied by proton adsorption or intercalation.[113] The electrolyte can permeate the porous matrix of the nanostructured electrodes. Electron transport occurs via diffusion; therefore, there is a decreasing charge-transfer resistance with increasing nitrate on the electrode surface, which may make titanium oxide lose charge accumulation. However, the removal of nitrate may add charge accumulation when the titanium oxide electrode is changed to bare acetate buffer. A similar result was reported for a nanocrystalline TiO_2 electrode, in which the CV presents an almost ideal faradaic behavior with negligible charge accumulation. If the faradaic charge transfer dominates, the current through the capacitor is low and the charge accumulated becomes insignificant, so the redox peaks become smaller, or even disappear completely.[114] The electrolyte composition may affect the extent of electron accumulation and the nature of charge compensation.[115] The phenomenon described here may find potential application in designing novel nitrate sensors.

Selective Detection of Dopamine in the Presence of Ascorbate and Uric Acid at Titanate-Nanotube Electrode

Another major goal in developing nanostructure-based sensing is to explore its application in electroanalytical chemistry. The development of a sensitive electrochemical method for the determination of *dopamine* (DA) has attracted much attention, because DA is an important neurotransmitter. However, the detection of DA has usually encountered interference from *ascorbic acid* (AA) and *uric acid* (UA). CVs of individual DA, AA, and UA at bare or TNT-modified *glassy carbon electrodes* (GCEs) (TNT/GCEs) are shown in Fig. 6.11. The redox peak of DA at bare GC electrode is very broad with a ΔE_p value of 0.130 V (Fig. 6.11*A*). A well-defined redox pair with obviously increased current response was obtained for DA at TNTs/GCE. The negatively shifted E_{pa} (0.185 V) and the positively shifted E_{pc} (0.135 V) results in a much smaller ΔE_p value (0.05 V) at TNT/GCE. Here, ΔE_p is defined as the difference of the anodic peak potential (E_{pa}) and the cathodic peak potential (E_{pc}); that is, $\Delta E_p = (E_{pa} - E_{pc})$. The oxidation peaks for DA, AA, and UA are very close to each other at bare

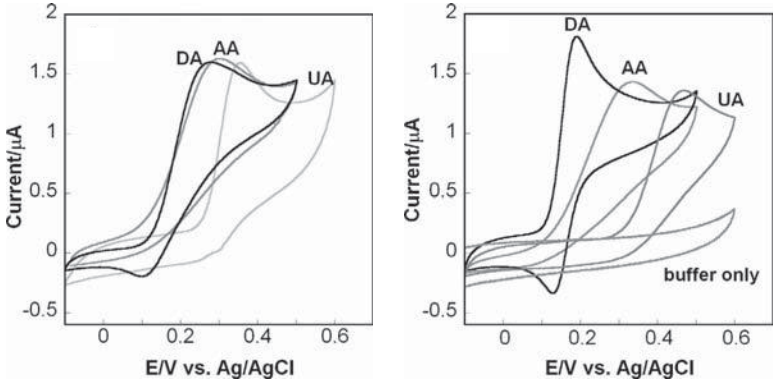


Figure 6.11 Cyclic voltammograms of individual DA, AA, and UA (each 0.1 mM) buffered with 0.1 M phosphate (pH 7.4). (*A*) Bare GC electrode and (*B*) TNT/GC electrode. Scan rate, 0.05 V s^{-1}. Reprinted with permission from A. Liu, et al., *Advanced Functional Materials*, vol. 16, pp. 371–376, 2006. Copyright © 2006 Wiley-VCH Verlag GmbH.

GCE (Fig. 6.11*A*); therefore, it is impossible to separate AA, DA, and UA. Nevertheless, the electrochemical oxidation of DA, AA, and UA at TNT/GCE was observed at 0.185, 0.320, and 0.440 V, respectively (Fig. 6.11*B*). TNT/GCE did not exhibit redox peaks in the potential window of –0.1 to 0.6 V. Figure 6.12 shows linear sweep voltammograms of a physiological solution containing AA (0.1 mM) and UA (0.3 mM) with a varying concentration of DA at TNT/GCE. No peak at 0.16 V was observed in the absence of DA (black line). When DA is present in the foregoing solution, the i_{pa} value at 0.16 V increases with the increasing DA concentration, whereas the voltammetric peak at 0.30 V is not obviously changed (Fig. 6.12). The linear range is within 0.1–30 μM DA. These results strongly suggest that DA can be selectively determined at TNT/GCE in the presence of a large excess of AA and UA.

6.4 Polymer-Based Nanowires or Nanotubes for Sensing

In the large field of nanotechnology, polymer matrix based nanocomposites have become a prominent area of current research and development.[116] Although conducting polymer nanowires are newcomers into the 1D chemical sensing and biosensing area,[5] electrochemically active conjugated polymers have already been widely used to prepare electrochromic devices. Conjugated polyheterocylic polymers, such as polyanilines, polypyridines, polypyrroles, polythiophenes, and poly(3,4-ethylenedioxylthiophene), have a dynamic,

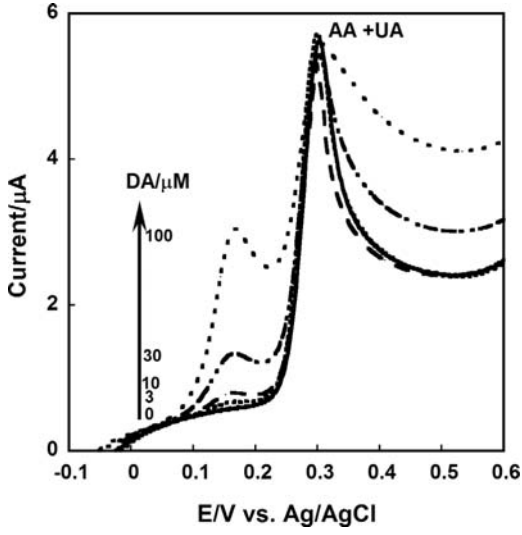


Figure 6.12 Linear sweep voltammograms of TNTs/GC electrode in 0.1 M phosphate buffer solution (pH 7.4) containing a physiological level of AA (0.1 mM) and UA (0.3 mM) with a varying concentration of DA. DA concentration is shown on the arrow. Scan rate, 0.05 V s^{-1}. Reprinted with permission from Ref. 88. Copyright © 2006 Wiley-VCH Verlag GmbH.

color-tunable "smart window." Thus, in this section, recent developments in the polymer nanotube-based sensing are addressed. For example, polypyrrole nanowires 300 nm in diameter and 50 to 60 μm in length were synthesized by chemical polymerization inside SiO_2-coated alumina membranes. Temperature-dependent electrical resistance studies show that the chemically synthesized nanowires were more ordered compared to electrochemically synthesized nanowires. Gas sensors based on a single polypyrrole nanowire exhibited good sensitivity toward ammonia, and provided a reliable detection at concentration as low as approximately 40 ppm.[117] Individual multisegmented Au-*poly(3,4-ethylenedioxythiophene)*(PEDOT)-Au nanowires demonstrated electrical transport and chemical sensing properties. Temperature-dependent conductivity measurements show that different charge transport mechanisms influence these properties in two types of PEDOT nanowires. Charge transport in PEDOT/poly(4-styrenesulfonic acid) nanowires is in the insulating regime of the metal-insulator transition and is dominated by hopping, whereas PEDOT/perchlorate (ClO_4^-) nanowires are slightly on the metallic side of the critical regime. The vapor-sensing properties of individual nanowires to water and methanol reflected the fact that the two kinds of PEDOT nanowires operated in different transport

regimes. Nanowires in the metallic transport regime showed much greater sensitivity to vapor-phase analytes than those in which transport is dominated by hopping.[118] Zhu and his coworkers reviewed the preparation of *polydiacetylene* (PDA) nanowires by self-assembly and self-polymerization as well as exploring their potential for future technological applications.[119] PDAs have been made sensitive to external stimuli such as light and chemical entities by incorporating a spectrophotometrically active moiety or a receptor unit as the head group of the PDA molecule. This makes them suitable for applications such as sensing and actuating. Furthermore, owing to the delocalization of π-conjugated electrons, PDAs have been exploited as good candidates for organic nonlinear optical materials.[119]

Functionalized nanoscale structures may enhance the amount of material exposed to surface interactions with analyte molecules to affect properties such as fluorescence or conductivity, which may result in novel sensing applications. Al_2O_3 filters (200 nm) can be used as templates to form polymer nanotubes containing an energy donor (perylene). The perylene is isolated from chemical interactions, but can undergo electronic energy transfer to acceptor molecules in aqueous solutions passing through the membrane. This energy transfer is analyzed quantitatively in terms of Forster transfer mechanisms and provides a way for the chemically inert filter to sense the presence of analyte molecules in the filtrate.[120] The negatively charged calcein diffused through the pores of *polypropyleneimine* (PPI) dendrimer-functionalized nanotubes more rapidly compared with the positively charged rhodamine 6G.[121] Moreover, the separation ability of PPI nanotubes depends on the nanotube pore size and the binding site density. Therefore, the dendrimer-based nanotubes are scaffolds for molecular recognition in confined nanoscale environments.

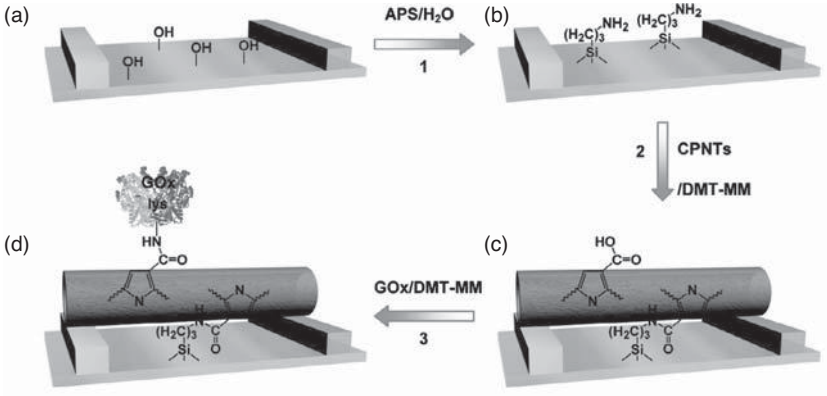
Glucose sensors have been studied most extensively because of their usefulness in diagnostic analysis of diabetes. The glucose sensors usually detect an oxidation current originating from the electrolysis of hydrogen peroxide (H_2O_2), which, in turn, is produced enzymatically by *glucose oxidase* (GOx).[122] Glucose sensing is widely reported by immobilizing GOx on carbon nanotubes.[123,124] The detection of glucose based on a liquid-ion gated field-effect transistor configuration in which enzyme-functionalized polypyrrole nanotubes are employed as the conductive channel has been reported. *Carboxylated polypyrrole nanotubes* (CPNTs) were fabricated by the chemical polymerization of an intrinsically functionalized monomer (*pyrrole-3-carboxylic acid*, P3CA) without degradation in major physical properties. The CPNTs possessed not only well-defined functional groups but also electrical properties comparable to those of nonsubstituted polypyrrole. Importantly, the carboxylic acid functional group can be utilized for various types of chemical and biological functionalization. A liquid-ion gated FET sensor was readily constructed on the basis of the chemical

functionality of CPNTs. In the first stage, the CPNTs were immobilized onto a microelectrode substrate via covalent linkages. It is noteworthy that the covalent immobilization allowed high-quality contact between the nanotubes and the microelectrodes in the liquid phase. The second stage involved the covalent binding of GOx to the nanotubes (Fig. 6.13*A*). The covalent functionalization generally provides excellent enzymatic activity and thermal stability. The fabricated FET sensor provided real-time response (an increase in source-drain current) and high sensitivity toward the various concentrations (0.5–20 mM) of glucose (Fig. 6.13*B*). The enzymatic product of hydrogen peroxide played a pivotal role in modulating the charge transport property of CPNTs.[125]

Growing ordered polymer nanowires within a pre-patterned electronic circuit, so that electrical contacts to the nanowires are made in situ during the growth procedure, avoids the time-consuming and challenging task of manipulating nanowires into position and making electrical contacts postsynthesis. The polyaniline nanowire devices consist of two gold or platinum metal nanoelectrodes separated by an air gap, across which the polymer nanowires are grown by a template-free electrochemical method. Through these techniques, the dimensionality of nanowire bridges across the device gap, from an array down to a single row and, ultimately, to a single nanowire, can be controlled. The technique, which as shown leads to ultimate integration, is simple to use and would be well suited to the commercial production of devices. This technique can be used to make chemoresistor-type sensor devices and is effective in the detection of ammonia gas at levels as low as 0.1×10^{-6} bar.[126]

The one-step incorporation of functional biological molecules into the conducting polymer nanowire during its synthesis within built-in electrical contacts is a major advantage over *silicon nanowire* (SiNW) and CNT devices that require postsynthesis functionalization alignment and positioning. However, the major disadvantage of conducting polymer nanowires is that they are mechanically weak.[5] Functional nanoscale devices can be assembled from indium

Figure 6.13 (*A*) Schematic illustration of reaction steps for a sensor platform based on CPPy nanotubes: (*a*) microelectrode substrate, (*b*) aminosilane-treated substrate, (*c*) immobilization of the nanotubes onto a substrate, and (*d*) binding of GOx to the nanotubes. (*B*) Schematic illustration of an enzyme FET sensor platform based on GOx-CPNTs (*a*). The source (S), drain (D), liquid-ion gate (G), Ag/AgCl reference electrode (R), and Pt counterelectrode (C) are shown. (*b*) ISD-EG curve of the FET measured at ± 0.01 V s^{-1} ($V_{SD} = -0.01$ V). (*Inset*) Expanded ISD-EG curve between 0 and 0.1 V). The redox state of CPNTs depending on the EG is shown as well as the working potential range suitable for a sensing test. Reprinted with permission from K. Yoon et al., *Journal of Physical Chemistry B*, vol. 112, 9992–9997, 2008. Copyright © 2008 American Chemical Society.



Reaction 1. Hydrolysis: $H_2N(CH_2)_3Si(OCH_3)_3 + 3H_2O \rightarrow H_2N(CH_2)_3Si(OH)_3 + 3CH_3OH$

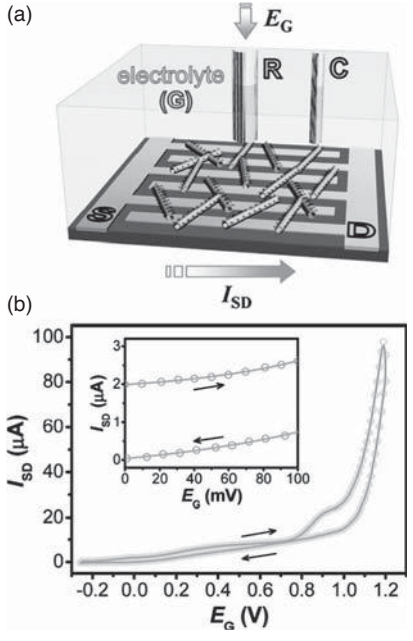
Condensation: $H_2N(CH_2)_3Si(OH)_3 + 3OH\text{-substrate} \rightarrow H_2N(CH_2)_3Si(O)_3\text{-substrate}$

Reaction 2. Condensation: pyrrole-COOH + $H_2N(CH_2)_3Si(O)_3$-substrate →

pyrrole-CONH$(CH_2)_3Si(O)_3$-substrate

Reaction 3. Condensation : pyrrole-COOH + H_2N-lys-GOx → pyrrole-CONH-lys-GOx

(*A*)



(*B*)

Figure 6.13

phosphide nanowires, whose electrical properties are controlled by selective doping. Gate-voltage-dependent transport measurements demonstrate that the nanowires can be predictably synthesized as either *n*- or *p*-type. These doped nanowires function as nanoscale field-effect transistors and can be assembled into crossed-wire p-n junctions that exhibit rectifying behavior. Significantly, the *p*-*n* junctions emit light strongly and are perhaps the smallest light-emitting diodes.[127]

6.5 Metal Nanowire-Based Biosensing

Metal nanowires have been the focus of many of the recent studies because their potential use as active components or interconnects in fabricating electronic, photonic, and sensing devices.[128,129] Core/shell bimetallic nanowires were utilized to increase the SERS activity, similar to that utilized for spherical nanoparticles.[130] A nanocob design of silver nanowires decorated with AuNPs, which are separated from the silver core by a nanoscale polymer shell composed of both hydrophilic and hydrophobic blocks, allows trapping of guest molecules of different types inside the predesigned "hot inner shell," making these nanocobs promising candidates for applications in SERS-based sensors.[131] Effective resistance against surfactant fouling is obtained by magnetically switching the surface orientation of alkanethiol-coated gold nanowires (containing a short nickel segment) between horizontal and vertical positions to allow the transducer to perform the measurement and reset it to the protection mode between successive measurements.[132]

Metal nanowires can also be used for virus detection. For example, the use of copper nanowires for the assembly of the central channel of tobacco mosaic virus particles[133,134] and the use of Au/Ag striped nanowires as multiplexed immunoassay platforms for pathogen detection have been reported.[135] On the other hand, SiNWs have been shown to be novel materials for sensing. It was reported that biotin-modified SiNWs were used to detect streptavidin down to at least a picomolar concentration range.[54] The antigen-functionalized SiNWs show reversible antibody binding and concentration-dependent detection in real time. These nanowires could be exploited in array-based screening and in vivo diagnostics for sensitive, label-free, and real-time detection of a wide range of biological species.[127] Recently, boron-doped SiNWs have been used to create highly sensitive, real-time electrically based sensors for biological and chemical species, because amine- and oxide-functionalized SiNWs exhibit pH-dependent conductance that was linear over a large dynamic range and could be understood in terms of the change in surface charge during protonation and deprotonation.[136] For instance, two-terminal SiNW electronic devices that function as ultrasensitive and selective detectors

of DNA were constructed.[137] The surfaces of the silicon nanowire devices were modified with peptide nucleic acid receptors designed to recognize the wild type versus the ΔF508 mutation site in the cystic fibrosis transmembrane receptor gene. Sequentially introducing wild-type or mutant DNA samples that exhibit a time-dependent conductance increase consistent with the peptide nucleic acid (PNA)-DNA hybridization enabled identification of fully complementary versus mismatched DNA samples; thereby, conductance measurements can be made.[137] The detection limit is in the femtomolar range (several tens). This nanowire-based approach represents a step forward in direct, label-free DNA detection and could provide a pathway to integrated, high-throughput, multiplexed DNA detection for genetic screening and biothreat detection.[137] An additional approach using a microneedle sensor platform with integrated silicon nanowire tip of 50 nm height and 50–100 nm width can be developed for intracellular biochemical detection.[138] Because of the virtue of miniaturized size and high sensitivity, this sensor has a great potential for studying individual cells or localized bioenvironments by revealing the pH level and/or enzyme activities.[138] The fabrication of the microneedle sensor was primarily based on conventional silicon processing, which was achieved using a silicon-on-insulator wafer with a 50-nm-thick (*100*) p-type Si device layer as the substrate. With proper chemical modification, this sensor could enable localized biochemical sensing within biological cells, such as neurotransmitter activities during synaptic communication between neuron cells.[138]

Proteins assembled on an Au nanowire are manipulated by an electrical potential applied on the nanowire, which can lead to the modulation of molecular fluorescence. The molecular modality can be unequivocally correlated with the modulated fluorescence, which enables the specific fluorescence from a single target protein to be unambiguously distinguished from background noise and nonspecific fluorescence (Fig. 6.14). As demonstrated through a thrombin assay, this simple method can significantly push the sensitivity and specificity of the protein detection down to the single molecule level.[139] More interestingly, with the synthesis of hybrid nanostructure consisting of two actin filaments tethered to the two ends of a Au nanowire, the adenosine-triphosphate-fueled motility of the hybrid nanostructure on a myosin monolayer can be associated with a solid support.[140] This research is promising for development of a molecular motor.

6.6 Concluding Remarks

The emerging nanotechnology field has opened new and exciting opportunities to explore analytical application of nanostructured materials. Among them, 1D nanostructures such as nanowires or nanobelts

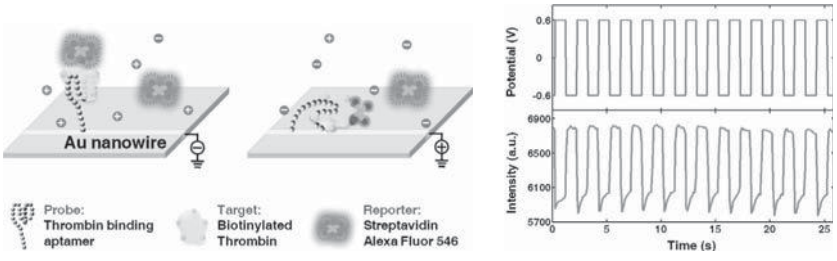


Figure 6.14 (*A*) Schematic illustration of an electrically modulated fluorescence protein assay including a thrombin-binding aptamer probe grafted on an Au nanowire. The target is a biotinylated thrombin, and the reporter, a fluorophore-labeled streptavidin. When a negative potential is applied on the nanowire, the negatively charged probe-target-reporter complex is repelled from the surface (*left*); when a positive potential is applied on the nanowire, the complex is attracted toward the nanowire (*right*). The fluorescence intensity from the probe-target-reporter complex is modulated as a function of the distance between the fluorophore and Au nanowire because of the *surface energy transfer* (SET). In contrast, a reporter molecule nonspecifically bound to a surface site other than the target molecule is immobilized; neither its position nor its fluorescence can be modulated by the electrical field. (*B*) Electrical potential applied on the nanowire (*top*) and modulated fluorescence measured from a sample at a 100-nM thrombin concentration (*bottom*) are shown synchronously versus time. Reprinted with permission from S. Huang et al., *Nano Letters*, vol. 8, pp. 2829–2833, 2008. Copyright © 2008 American Chemical Society.

and nanotubes have attracted great attention because of their extraordinary physical and chemical properties, which offer great promise in the development of chemical sensing or biosensing, facilitating a significant improvement over the selectivity and sensitivity of current methods. Recent advances in the development of sensors including gas sensors, humidity sensors, immunosensors, and electrochemical sensors using nanowires or nanotubes have been summarized in this chapter. Nanowires and nanoribbons as well as nanotubes will have an important impact on the exploration of nanoscale devices, nanosensors, and detectors using optical, field-effect transistor, electrochemical, electric, and magnetic transducers.

6.7 Future Perspectives

Rapid development in sensing applications of one-dimensional nanostructures has occurred in the past 10 years. The preparation of quasi-one-dimensional nanostructures as new sensing materials is essential for the advancement of chemical sensors. The conjugation of nanostructured materials and biomaterials for biosensing is encouraging. Miniaturization of the sensor is a trend, and thus single

nanowire- or nanoribbon- and nanotube-related sensors will be developed and hold great promise for microfluidic or nanofluidic system, which may exhibit high selectivity and sensitivity. It is still a challenge to make these sensing devices commercially available for practical use. With the advancement of nanotechnology, more sensing platforms will be established to enhance sensitivity and selectivity. Although many sensing concepts based on 1D nanostructures have been proved, incorporating these materials into routine functional integrated devices remains a challenge. Even though there has been tremendous advancement in fabrication techniques of 1D nanostructures, there are still difficulties associated with the fabrication of these nanostructures with well-controlled and consistent dimensions, morphology, phase purity, and chemical composition. On the other hand, new techniques used for decorating 1D nanostructures are attractive, which may provide additional opportunities to improve the performance of the devices. For example, networks of SWNTs decorated with Au/Pd nanocubes by electrodeposition can be integrated within an electrically contacted network of SWNTs, which served as docking points for attaching GOx to facilitate the detection of glucose.[141] Based on the proposed method, the detection limit of this glucose biosensor is 1 μM, which is a fivefold improvement in detection limit compared with those glucose biosensors based on carbon nanotubes and metallic nanoparticles and nanowires.[141] On the other hand, it is still a challenge to find practical routes to prepare large quantities of 1D nanostructures rapidly and at reasonable cost. The assembly and alignment of 1D nanostructures is also an area that needs improvement, but that may have widespread technological applications.[5] Advances in assembling more complex 1D nanostructure arrays and integrating them with nanoscale electronics may lead to wide applications in clinical diagnostics, food safety, environmental science, and antiterrorism.

Acknowledgment

This work was supported in part by the 100 Talents Project, Chinese Academy of Sciences.

References

1. F. Hook, B. Kasemo, M. Grunze, and S. Zauscher, "Quantitative biological surface science: challenges and recent advances," *ACS Nano*, vol. 2, pp. 2428-2436, 2008.
2. D. Astruc, F. Lu, and J. R. Aranzaes, "Nanoparticles as recyclable catalysts: the frontier between homogeneous and heterogeneous catalysis," *Angewandte Chemie International Edition,* vol., 44, pp. 7852-7872, 2005.
3. D. T. Mitchell, S. B. Lee, L. Trofin, N. Li, T. K. Nevanen, H. Soderlund, et al., "Smart nanotubes for bioseparations and biocatalysis," *Journal of the American Chemical Society,* vol. 124, pp. 11864-11865, 2002.

4. D. G. Rickerby and M. Morrison, "Nanotechnology and the environment: a European perspective," *Science and Technology of Advanced Materials*, vol. 8, pp. 19-24, 2007.
5. A. K. Wanekaya, W. Chen, N. V. Myung, and A. Mulchandani, "Nanowire-based electrochemical biosensors," *Electroanalysis,* vol. 18, pp. 533-550, 2006.
6. M. C. McAlpine, H. Ahmad, D. Wang, and J. R. Heath, "Highly ordered nanowire arrays on plastic substrates for ultrasensitive flexible chemical sensors," *Nature Materials,* vol. 6, pp. 379-384, 2007.
7. Z. L. Wang, "Towards self-powered nanosystems: from nanogenerators to nanopiezotronics," *Advanced Functional Materials,* vol. 18, pp. 3553-3567, 2008.
8. O. K. Varghese and C. A. Grimes, "Metal oxide nanoarchitectures for environmental sensing," *Journal of Nanoscience and Nanotechnology,* vol. 3, pp. 277-293, 2003.
9. A. Liu, "Towards development of chemosensors and biosensors with metal-oxide-based nanowires or nanotubes," *Biosensors and Bioelectronics,* vol. 24, pp. 167-177, 2008.
10. Z. L. Wang, "Nanobelts, nanowires, and nanodiskettes of semiconducting oxides—from materials to nanodevices," *Advanced Materials,* vol. 15, pp. 432-435, 2003.
11. J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, et al., "Nanotube molecular wires as chemical sensors," *Nature*, vol. 287, pp. 622-625, 2000.
12. R. J. Chen, N. R. Franklin, J. Kong, J. Cao, T. W. Tombler, Y. Zhang, et al., "Molecular photodesorption from single-walled carbon nanotubes," *Applied Physics Letters,* vol. 79, pp. 2258-2260, 2001.
13. A. Liu, I. Honma, M. Ichihara, and H. Zhou, "Poly(acrylic acid)-wrapped multi-walled carbon nanotubes composite solubilization in water: definitive spectroscopic properties," *Nanotechnology*, vol. 17, pp. 2845-2849, 2006.
14. J. Wang, X. Cai, G. Rivas, H. Shiraishi, P. A. M. Farias, and N. Dontha, "DNA electrochemical biosensor for the detection of short DNA sequences related to the human immunodeficiency virus," *Analytical Chemistry,* vol. 68, pp. 2629-2634, 1996.
15. J. Wang, J. Li, A. J. Baca, J. Hu, F. Zhou, W. Yan, et al., "Amplified voltammetric detection of DNA hybridization via oxidation of ferrocene caps on gold nanoparticle/streptavidin conjugates," *Analytical Chemistry,* vol. 75, pp. 3941-3945, 2003.
16. A. Liu, I. Honma, and H. Zhou, "Simultaneous voltammetric detection of dopamine and uric acid at their physiological level in the presence of ascorbic acid using poly(acrylic acid)-multiwalled carbon-nanotube composite-covered glassy-carbon electrode," *Biosensors and Bioelectronics,* vol. 23, pp. 74-80, 2007.
17. J. Wang, "Carbon-nanotube based electrochemical biosensors: A review. *Electroanalysis,* vol. 17, 7-14, 2005.
18. P. Patel-Predd, "Smarter, faster nano sensor." Available at https://www.technologyreview.com/biomedicine/20976/. Accessed June 19, 2008.
19. B. Mahar, C. Laslau, R. Yip, and Y. Sun, "Development of carbon nanotube-based sensors—a review. *IEEE Sensors Journal*, vol. 7, pp. 266-284, 2007.
20. E. Vogel, "Technology and metrology of new electronic materials and devices," *Nature Nanotechnology,* vol. 2, pp. 25-32, 2007.
21. Y.-L. Chueh, C. H. Hsieh, M. T. Chang, L. J. Chou, C. Lao, J. Song, et al., "RuO_2 nanowires and RuO_2/TiO_2 core/shell nanowires: From synthesis to mechanical, optical, electrical, and photoconductive properties." *Advanced Materials,* vol. 19, pp. 143-149, 2007.
22. S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley, L. J. Geerligs, et al., "Individual single-wall carbon nanotubes as quantum wires," *Nature*, vol. 386, pp. 474-477, 1997.
23. A. L. Briseno, S. C. B. Mannsfeld, C. Reese, J. M. Hancock, Y. Xiong, S. A. Jenekhe, et al., "Perylenediimide nanowires and their use in fabricating

field-effect transistors and complementary inverters," *Nano Letters,* vol. 7, pp. 2847-2853, 2007.
24. C. T. Black, "Self-aligned self assembly of multi-nanowire silicon field effect transistors," *Applied Physics Letters,* vol. 87, 1631163, 2005.
25. C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, et al., "Nanowire-based one-dimensional electronics," *Materials Today*, vol. 9, pp. 28-35, 2006.
26. Y. Wakayama, R. Hayakawa, T. Chikyow, S. Machida, T. Nakayama, S. Egger, et al., "Self-assembled molecular nanowires of 6,13-bis(methylthio)pentacene: growth, electrical properties, and applications," *Nano Letters,* vol. 8, pp. 3273-3277, 2008.
27. Y.-F. Lin and W.-B. Jian, "The impact of nanocontact on nanowire based nanoelectronics," *Nano Letters,* vol. 8, pp. 3146-3150, 2008.
28. D. J. Sirbuly, A. Tao, M. Law, R. Fan, and P. Yang, "Multifunctional nanowire evanescent wave optical sensors," *Advanced Materials,* vol. 19, pp. 61-66, 2007.
29. A. Kolmakov, Y. Zhang, G. Cheng, and M. Moskovits, "Detection of CO and O_2 using tin oxide nanowire sensors," *Advanced Materials,* vol. 15, pp. 997-1000, 2003.
30. Y. Shimizu and M. Egashira, "Basic aspects and challenges of semiconductor gas sensors," *MRS Bulletin*, vol. 24, pp. 18-24, 1999.
31. Z. W. Pan, Z. R. Dai, and Z. L. Wang, "Nanobelts of semiconducting oxides," *Science*, vol. 291, pp. 1947-1949, 2001.
32. A. Michailowski, D. AlMawlawi, G. Cheng, and M. Moskovits, "Highly regular anatase nanotubule arrays fabricated in porous anodic templates," *Chemical Physics Letters,* vol. 349, pp. 1-5, 2001.
33. D. E. Williams, "Semiconducting oxides as gas-sensitive resistors," *Sensors and Actuators B: Chemical,* vol. 57, pp. 1-16, 1999.
34. H. Nanto, T. Minami, and S. Takata, "Zinc-oxide thin-film ammonia gas sensors with high sensitivity and excellent selectivity," *Journal of Applied Physics,* vol. 60, pp. 482-484, 1986.
35. C. Li, D. Zhang, B. Lei, S. Han, X. Liu, and C. Zhou, "Surface treatment and doping dependence of In_2O_3 nanowires as ammonia sensors. *Journal of Physical Chemistry B,* vol. 107, 12451-12455, 2003.
36. C. Li, D. Zhang, S. Han, X. Liu, T. Tang, and C. Zhou, "Diameter-controlled growth of single-crystalline In_2O_3 nanowires and their electronic properties," *Advanced Materials,* vol. 15, pp. 143-146, 2003.
37. C. Li, D. Zhang, S. Han, X. Liu, T. Tang, B. Lei, et al., Synthesis, electronic properties, and applications of indium oxide nanowires. *Annals of the New York Academy of Sciences,* vol. 1006, 104-121, 2003.
38. S. Kaciulis, L. Pandolfi, E. Comini, G. Faglia, M. Ferroni, G. Sberveglieri, et al., "Nanowires of metal oxides for gas sensing applications," *Surface and Interface Analysis*, vol. 40, pp. 575-578, 2008.
39. F. Hernandez-Ramirez, J. D. Prades, A. Tarancon, S. Barth, O. Casals, R. Jimenez-Diaz, et al., "Insight into the role of oxygen diffusion in the sensing mechanisms of SnO_2 nanowires," *Advanced Functional Materials,* vol. 18, pp. 2990-2994, 2008.
40. M. Law, H. Kind, B. Messer, F. Kim, and P. Yang, "Photochemical sensing of NO_2 with SnO_2 nanoribbon nanosensors at room temperature," *Angewandte Chemie International Edition,* vol. 41, pp. 2405-2408, 2002.
41. J. Tamaki, M. Nagaishi, Y. Teraoka, N. Miura, N. Yamazoe, K. Moriya, et al., "Adsorption behavior of carbon monoxide and interfering gases on tin dioxide," *Surface Science*, vol. 221, pp. 183-196, 1989.
42. N. Barsan, M. Schweizer-Berberich, and W. Göpel, "Fundamental and practical aspects in the design of nanoscaled SnO_2 gas sensors: a status report," *Fresenius Journal of Analytical Chemistry,* vol. 365, pp. 287-304, 1999.
43. J. Polleux, A. Gurlo, N. Barsan, U. Weimar, M. Antonietti, and M. Niederberger, "Template-free synthesis and assembly of single-crystalline tungsten

oxide nanowires and their gas-sensing properties," *Angewandte Chemie International Edition,* vol. 45, pp. 261-265, 2006.
44. X. Qi, F. E. Osterloh, S. A. Barriga, J. A. Giacomo, and S. Chiang, "Molecular adsorption to $LiMo_3Se_3$ nanowire film chemiresistors," *Analytical Chemistry,* vol. 78, pp. 1306-1311, 2006.
45. X. Qi, F. E. Osterloh, J. A. Giacomo, and S. Chiang, "Effect of additives on $LiMo_3Se_3$ nanowire film chemical sensors," *Langmuir*, vol. 22, pp. 8253-8256, 2006.
46. M. Devetak, B. Bercic, M. Uplaznik, A. Mrzel, and D. Mihailovic, "$Mo_6S_3I_6$ nanowire network vapor pressure chemisensors," *Chemistry of Materials,* vol. 20, pp. 1773-1777, 2008.
47. Q. Kuang, C. Lao, Z. L. Wang, Z. Xie, and L. Zheng, "High-sensitivity humidity sensor based on a single SnO_2 nanowire," *Journal of the American Chemical Society,* vol. 129, pp. 6070-6071, 2007.
48. X. Huang, Y. Sun, L. Wang, F. Meng, and J. Liu, "Carboxylation multi-walled carbon nanotubes modified with $LiClO_4$ for water vapour detection," *Nanotechnology*, vol. 15, pp. 1284-1288, 2004.
49. Institute of Food Technologies, "Scientific status summary: bacteria associated with foodborne diseases." Retrieved September 1, 2004, from www.ift.org.
50. B. H. Rosen, "Waterborne pathogens in agricultural watersheds." Watershed Science Institute, WSSI-Technical Note 2, USDA, Ed. 2000.
51. Health Canada, *Bacterial Waterborne Pathogens—Current and Emerging Organisms of Concern*, retrieved February 2006 from http://www.hc-sc.gc.ca/ewh-semt/pubs/water-eau/pathogens-pathogenes/index-eng.php.
52. D. Ivnitski, I. Abdel-Hamid, P. Atanasov, and E. Wilkins, "Biosensors for detection of pathogenic bacteria," *Biosensors and Bioelectronics,* vol. 14, pp. 599-624, 1999.
53. M. Curreli, C. Li, Y. Sun, B. Lei, M. A. Gundersen, M. E. Thompson, et al., "Selective functionalization of In_2O_3 nanowire mat devices for biosensing applications," *Journal of the American Chemical Society,* vol. 127, pp. 6922-6923, 2005.
54. Y. L. Bunimovich, G. Ge, K. C. Beverly, R. S. Ries, L. Hood, and J. R. Heath, "Electrochemically programmed, spatially selective biofunctionalization of silicon wires," *Langmuir*, vol. 20, pp. 10630-10638, 2004.
55. J. Hu, T. W. Odom, and C. M. Lieber, "Chemistry and physics in one dimension: synthesis and properties of nanowires and nanotubes," *Accounts of Chemical Research,* vol. 32, pp. 435-445, 1999.
56. L. J. Lauhon, M. S. Gudiksen, D. Wang, and C. M. C. M. Lieber, Epitaxial core–shell and core–multishell nanowire heterostructures. *Nature,* vol. 420, pp. 57-61, 2002.
57. M. C. McAlpine, R. S. Friedman, S, Jin, K.-H. Lin, W. U. Wang, and C. M. Lieber, "High-performance nanowire electronics and photonics on glass and plastic substrates," *Nano Letters,* vol. 3, pp. 1531-1535, 2003.
58. G. Zheng, W. Lu, S. Jin, and C. M. Lieber, "Synthesis and fabrication of high-performance n-type silicon nanowire transistors," *Advanced Materials,* vol. 16, pp. 1890-1893, 2004.
59. F. Patolsky and C. M. Lieber, "Nanowire nanosensors," *Materials Today*, vol. 8, pp. 20-28, 2005.
60. F. Patolsky, G. Zheng, and C. M. Lieber, "Nanowire-based biosensors," *Analytical Chemistry,* vol. 78, pp. 4260-4269, 2006.
61. E. Bentzen, D. W. Wright, and J. E. Crowe, "Nanoscale tools for rapid and sensitive diagnosis of viruses," *Future Virology,* vol. 1, pp. 769-781, 2006.
62. F. Patolsky, G. Zheng, O. Hayden, M. Lakadamyali, X. Zhuang, and C. M. Lieber, "Electrical detection of single viruses," *Proceedings of the National Academy of Sciences of the United States of America,* vol. 101, pp. 14017-14022, 2004.

63. E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak, D. B. Turner-Evans, A. D. Hamilton, et al., "Label-free immunodetection with CMOS-compatible semiconducting nanowires," *Nature*, vol. 445, pp. 519-522, 2007.
64. E. M. Krauland, B. R. Peelle, K. D. Wittrup, and A. M. Belcher, "Peptide tags for enhanced cellular and protein adhesion to single-crystalline sapphire," *Biotechnology and Bioengineering,* vol. 97, pp. 1009-1020, 2007.
65. C. Li, M. Curreli, H. Lin, B. Lei, F. N. Ishikawa, R. Datar, R.; et al., "Complementary detection of prostate-specific antigen using In_2O_3 nanowires and carbon nanotubes," *Journal of the American Chemical Society,* vol. 127, pp. 12484-12485, 2005.
66. R. Wang, C. Ruan, D. Kanayeva, K. Lassiter, and Y. Li, "TiO_2 nanowire bundle microelectrode based impedance immunosensor for rapid and sensitive detection of *Listeria monocytogenes*," *Nano Letters,* vol. 8, pp. 2625-2631, 2008.
67. M. Willander, P. Klason, L. L. Yang, S. M. Al-Hilli, Q. X. Zhao, and O. Nur, "ZnO nanowires: chemical growth, electrodeposition, and application to intracellular nano-sensors," *Physica Status Solidi (c)*, vol. 5, 3076-3083, 2008.
68. H. Pan, H. Lin, Q. Shen, and J.-J. Zhu, "Cadmium(II) (8-hydroxyquinoline) chloride nanowires: synthesis, characterization and glucose-sensing application," *Advanced Functional Materials,* vol. 18, pp. 3692-3698, 2008.
69. W. Jia, M. Guo, Z. Zheng, T. Yu, Y. Wang, E. Rodriguez, E.; et al., Vertically aligned CuO nanowires based electrode for amperometric detection of hydrogen peroxide. *Electroanalysis,* vol. 20, pp. 2153-2157, 2008.
70. M. E. Spahr, P. Bitterli, R. Nesper, M. Müller, F. Krumeich, and H. U. Nissen, "Redox-active nanotubes of vanadium oxide," *Angewandte Chemie International Edition,* vol. 37, pp. 1263-1265, 1998.
71. G. R. Patzke, F. Krumeich, and R. Nesper, "Oxidic nanotubes and nanorods: anisotropic modules for a future nanotechnology," *Angewandte Chemie International Edition,* vol. 41, pp. 2446-2461, 2002.
72. M. Kogiso, Y. Zhou, and T. Shimizu, "Instant preparation of self-assembled metal-complexed lipid nanotubes that act as templates to produce metal-oxide nanotubes," *Advanced Materials,* vol. 19, pp. 242-246, 2007.
73. S. Mukherjee, K. Kim, and S. Nair, "Short, highly ordered, single-walled mixed-oxide nanotubes assemble from amorphous nanoparticles," *Journal of the American Chemical Society,* vol. 129, pp. 6820-6826, 2007.
74. J. Jung, T. Shimizu, and S. Shinkai, "Self-assembling structures of steroidal derivatives in organic solvents and their sol-gel transcription into double-walled transition-metal oxide nanotubes," *Journal of Materials Chemistry,* vol. 15, pp. 3979-3986, 2005.
75. Q. Kuang, Z.-W. Lin, W. Lian, Z.-Y. Jiang, Z.-X. Xie, R.-B. Huang, et al., "Syntheses of rare-earth metal oxide nanotubes by the sol-gel method assisted with porous anodic aluminum oxide templates" *Journal of Solid State Chemistry,* vol. 180, pp. 1236-1242, 2007.
76. M. Kogiso, Y. Zhou, and T. Shimizu, "Instant preparation of self-assembled metal-complexed lipid nanotubes that act as templates to produce metal oxide nanotubes," *Advanced Materials,* vol. 19, pp. 242-246, 2007.
77. L. Li, Y. Yang, G. Li, and L. Zhang, "Conversion of a Bi nanowire array to an array of Bi-Bi_2O_3 core-shell nanowires and Bi_2O_3 nanotubes," *Small*, *vol*. 2, pp. 548-553, 2006.
78. G. K. Mora, O. K. Varghese, M. Paulose, K. G. Ong, and C. A. Grimes, "Fabrication of hydrogen sensors with transparent titanium oxide nanotube-array thin films as sensing elements," *Thin Solid Films*, vol. 496, pp. 42-48, 2005.
79. N. Du, H. Zhang, B. D. Chen, X. Y. Ma, Z. H. Liu, J. B. Wu, et al., "Porous indium oxide nanotubes: layer-by-layer assembly on carbon-nanotube templates and application for room-temperature NH_3 gas sensors," *Advanced Materials,* vol. 19, pp. 1641-1645, 2007.

80. J. Chen, L. Xu, W. Li, and X. Gou, "$\alpha-Fe_2O_3$ nanotubes in gas sensor and lithium-ion battery applications," *Advanced Materials,* vol. 17, pp. 582-586, 2005.
81. Y. Li, Z. Huang, and S. Rong, "A vanadium oxide nanotube-based nitric oxide gas sensor," *Sensors and Materials,* vol. 18, pp. 241-249, 2006.
82. G. Zhang, B. Guo, and J. Chen, "MCo_2O_4 (M = Ni, Cu, Zn) nanotubes: template synthesis and application in gas sensors," *Sensors and Actuators B: Chemical,* vol. 114, pp. 402-409, 2006.
83. Z. R. Tian, J. A. Voigt, J. Liu, B. McKenzie, and H. Xu, "Large oriented arrays and continuous films of TiO_2-based nanotubes," *Journal of the American Chemical Society,* vol. 125, pp. 12384-12385, 2003.
84. T. Kasuga, M. Hiramatsu, A. Hoson, T. Sekino, and K. Niihara, "Formation of titanium oxide nanotube," *Langmuir*, vol. 14, pp. 3160-3163, 1998.
85. B. D. Yao, Y. F. Chan, X. Y. Zhang, W. F. Zhang, Z. Y. Yang, and N. Wang, "Formation mechanism of TiO_2 nanotubes," *Applied Physics Letters,* vol. 82, pp. 281-283, 2003.
86. Q. Chen, W. Zhou, Q. Chen, G. Du, and L. Peng, "Trititanate nanotubes made via a single alkali treatment," *Advanced Materials,* vol. 14, pp. 1208-1211, 2002.
87. H. Tokudome and M. Miyauchi, "Electrochromism of titanate-based nanotubes," *Angewandte Chemie International Edition,* vol. 44, pp. 1974-1977, 2005.
88. A. Liu, M. D. Wei, I. Honma, and H. Zhou, H., Biosensing properties of titanate-nanotube films: selective detection of dopamine in the presence of ascorbate and uric acid. *Advanced Functional Materials,* vol. 16, pp. 371-376, 2006.
89. A. Liu, M. Wei, I. Honma, and H. Zhou, "Direct electrochemistry of myoglobin in titanate nanotubes film," *Analytical Chemistry,* vol. 77, pp. 8068-8074, 2005.
90. T. Chirayil, P. Y. Zavalij, and M. S. Whittingham, "Hydrothermal synthesis of vanadium oxides," *Chemistry of Materials,* vol. 10, pp. 2629-2640, 1998.
91. M. Niederberger, H.-J. Muhr, F. Krumeich, F. Bieri, D. Gunther, and R. Nesper, "Low-cost synthesis of vanadium oxide nanotubes via two novel non-alkoxide routes," *Chemistry of Materials,* vol. 12, pp. 1995-2000, 2000.
92. F. Krumeich, F.; H.-J. Muhr, M. Niederberger, F. Bieri, B. Schnyder, and R. J. Nesper, "Morphology and topochemical reactions of novel vanadium oxide nanotubes," *Journal of the American Chemical Society,* vol. 121, pp. 8324-8331, 1999.
93. A. Liu, "Titanate-nanotube based electrochemical biosensing," in E. M. Mernstein, Ed., *Bioelectrochemistry Research Developments*, pp. 209-223, Nova Science Publishers, New York, 2008.
94. A. Liu, H. Zhou, I. Honma, and M. Ichihara, "Switchable titanate-nanotube electrode sensitive to nitrate," *Applied Physics Letters,* vol. 90, p. 253112, 2007.
95. A.-E. F. Nassar, W. S. Willis, and J. F. Rusling, "Electron transfer from electrodes to myoglobin: facilitated in surfactant films and blocked by adsorbed biomacromolecules," *Analytical Chemistry,* vol. 67, pp. 2386-2392, 1995.
96. Bard, A.; Faulkner, L. R., *Electrochemical Methods: Fundamentals and Applications*, 2nd ed., Wiley, New York, 2001.
97. J. H. Reeves, S. Song, and E. F. Bowden, "Application of square wave voltammetry to strongly adsorbed quasireversible redox molecules," *Analytical Chemistry,* vol. 65, pp. 683-688, 1993.
98. J. J. O'Dea and J. G. Osteryoung, "Characterization of quasi-reversible surface processes by square-wave voltammetry," *Analytical Chemistry,* vol. 65, pp. 3090-3097, 1993.
99. C. Fan, H. Wang, S. Sun, D. Zhu, G. Wagner, and G. Li, "Electron-transfer reactivity and enzymatic activity of hemoglobin in a SP Sephadex membrane," *Analytical Chemistry,* vol. 73, pp. 2850-2854, 2001.
100. N. Hu and J. F. Rusling, "Electrochemistry and catalysis with myoglobin in hydrated poly(ester sulfonic acid) ionomer films," *Langmuir*, *vol*. 13, pp. 4119-4125, 1997.

101. M. Yang, J. Wang, H. Li, J.-G. Zheng, and N. N. Wu, "A lactate electrochemical biosensor with a titanate nanotube as direct electron transfer promoter," *Nanotechnology*, vol. 19, 075502, 2008.
102. L. Zhang, Q. Zhang, and J. Li, "Layered titanate nanosheets intercalated with myoglobin for direct electrochemistry," *Advanced Functional Materials,* vol. 17, pp. 1958-1965, 2007.
103. L. Zhang, Q. Zhang, X. Lu, and J. Li, "Direct electrochemistry and electrocatalysis based on film of horseradish peroxidase intercalated into layered titanate nano-sheets," *Biosensors and Bioelectronics,* vol. 23, pp. 102-106, 2007.
104. A. K. M. Kafia, G. Wua, and A. Chen, "A novel hydrogen peroxide biosensor based on the immobilization of horseradish peroxidase onto Au-modified titanium dioxide nanotube arrays," *Biosensors and Bioelectronics,* vol. 24, pp. 566-571, 2008.
105. C. Guo, F. Hu, C. M. Li, and P. K. Shen, "Direct electrochemistry of hemoglobin on carbonized titania nanotubes and its application in a sensitive reagentless hydrogen peroxide biosensor," *Biosensors and Bioelectronics,* vol. 24, pp. 819-824, 2008.
106. Z. Dai, X. Xu, and H. Ju, "Direct electrochemistry and electrocatalysis of myoglobin immobilized on a hexagonal mesoporous silica matrix," *Analytical Biochemistry,* vol. 332, pp. 23-31, 2004.
107. J. Li, S. N. Tan, and H. Ge, "Silica sol-gel immobilized amperometric biosensor for hydrogen peroxide," *Analytica Chimica Acta,* vol. 335, pp. 137-145, 1996.
108. F. Bellezza, A. Cipiciani, U. Costantino, and S. Nicolis, "Catalytic activity of myoglobin immobilized on zirconium phosphonates," *Langmuir*, vol. 20, pp. 5019-5025, 2004.
109. H. Liu and N. Hu, "Comparative bioelectrochemical study of core-shell nanocluster films with ordinary layer-by-layer films containing heme proteins and $CaCO_3$ nanoparticles," *Journal of Physical Chemistry B,* vol. 109, pp. 10464-10473, 2005.
110. S. Peng, Q. Gao, Q. Wang, and J. Shi, "Layered structural heme protein magadiite nanocomposites with high enzyme-like peroxidase activity," *Chemistry of Materials,* vol. 16, pp. 2675-2684, 2004.
111. A. Liu, M. Ichihara, I. Honma, and H. Zhou, "Vanadium-oxide nanotubes: synthesis and template-related electrochemical properties," *Electrochemistry Communications,* vol. 9, pp. 1766-1771, 2007.
112. F. Y. Oliva, L. B. Avalle, and O. R. Cámara, "Electrochemical behaviour of human serum albumin-TiO_2 nanocrystalline electrodes studied as a function of pH: Part 1. Voltammetric response," *Journal of Electroanalytical Chemistry,* vol. 534, pp. 19-29, 2002.
113. L. A. Lyon and J. T. Hupp, "Energetics of the nanocrystalline titanium dioxide/aqueous solution interface: approximate conduction band edge variations between $H_0 = -10$ and $H- = +26$," *Journal of Physical Chemistry B,* vol. 103, pp. 4623-4628, 1999.
114. F. Fabregat-Santiago, I. Mora-Seró, G. Garcia-Belmonte, and J. Bisquert, "Cyclic voltammetry studies of nanoporous semiconductors. Capacitive and reactive properties of nanocrystalline TiO_2 electrodes in aqueous electrolyte," *Journal of Physical Chemistry B,* vol. 107, pp. 758-768, 2003.
115. G. Boschloo and D. Fitzmaurice, "Electron accumulation in nanostructured TiO_2 (anatase) electrodes," *Journal of Physical Chemistry B,* vol. 103, pp. 7860-7868, 1999.
116. D. R. Paul and L. M. Robeson, "Polymer nanotechnology: Nanocomposites," *Polymer*, vol. 49, pp. 3187-3204, 2008.
117. S. Hernandez, D. Chaudhuri, W. C. Nosang, and M. A. Mulchandani, "Single polypyrrole nanowire ammonia gas sensor," *Electroanalysis,* vol. 19, pp. 2125-2130, 2007.
118. Y. Cao, A. E. Kovalev, R. Xiao, J. Kim, T. S. Mayer, and T. E. Mallouk, "Electrical transport and chemical sensing properties of individual conducting polymer nanowires," *Nano Letters,* vol. 8, pp. 4653-4658, 2008.

119. W. Zhou, Y. Li, and D. Zhu, "Progress in polydiacetylene nanowires by self-assembly and self-polymerization," *Chemistry—An Asian Journal*, vol. 2, pp. 222-229, 2007.
120. S. Lee, A. M. Muller, R. Al-Kaysi, and C. J. Bardeen, "Using perylene-doped polymer nanotubes as fluorescence sensors," *Nano Letters,* vol. 6, pp. 1420-1424, 2006.
121. E. N. Savariar, M. M. Sochat, A. Klaikherd, and S. Thayumanavan, "Functional group density and recognition in polymer nanotubes," *Angewandte Chemie International Edition,* vol. 48, pp. 110-114, 2009.
122. J.-I. Anzai, H. Takeshita, Y. Kobayashi, T. Osa, and T. Hoshi, "Layer-by-layer construction of enzyme multilayers on an electrode for the preparation of glucose and lactate sensors: Elimination of ascorbate interference by means of an ascorbate oxidase multilayer," *Analytical Chemistry,* vol. 70, pp. 811-817, 1998.
123. J. Wang and M. Musameh, "Enzyme-dispersed carbon-nanotube electrodes: a needle microsensor for monitoring glucose," *Analyst*, vol. 128, pp. 1382-1385, 2003.
124. A. Salimi, R. G. Compton, and R. Hallaj, "Glucose biosensor prepared by glucose oxidase encapsulated sol-gel and carbon-nanotube-modified basal plane pyrolytic graphite electrode," *Analytical Biochemistry,* vol. 333, pp. 49-56, 2004.
125. H. Yoon, S. Ko, and J. Jang, "Field-effect-transistor sensor based on enzyme-functionalized polypyrrole nanotubes for glucose detection," *Journal of Physical Chemistry B,* vol. 112, pp. 9992-9997, 2008.
126. N. T. Kemp, D. McGrouther, J. W. Cochrane, and R. Newbury, "Bridging the gap: polymer nanowire devices," *Advanced Materials,* vol. 19, pp. 2634-2638, 2007.
127. X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, pp. 66-69, 2001.
128. Y. Sun and Y. Xia, "Large-scale synthesis of uniform silver nanowires through a soft, self-seeding, polyol process," *Advanced Materials,* vol. 14, pp. 833-837, 2002.
129. M. Zach, K. Ng, and R. M. Penner, "Molybdenum nanowires by electrodeposition," *Science*, vol. 290, pp. 2120-2123, 2000.
130. S. E. Hunyadi and C. J. Murphy, "Bimetallic silver–gold nanowires: fabrication and use in surface-enhanced Raman scattering," *Journal of Materials Chemistry,* vol. 16, pp. 3929-3935, 2006.
131. R. Gunawidjaja, S. Peleshanko, H. Ko, and V. V. Tsukruk, "Bimetallic nanocobs: decorating silver nanowires with gold nanoparticles," *Advanced Materials,* vol. 20, pp. 1544-1549, 2008.
132. R. Laocharoensuk, A. Bulbarello, S. B. Hocevar, S. Mannino, B. Ogorevc, and J. Wang, "On-demand protection of electrochemical sensors based on adaptive nanowires," *Journal of the American Chemical Society,* vol. 129, pp. 7774-7775, 2007.
133. S. Balci, A. M. Bittner, K. Hahn, C. Scheu, M. Knez, and A. Kadric, et al., "Copper nanowires within the central channel of tobacco mosaic virus particles," *Electrochimica Acta*, vol. 51, pp. 6251-6257, 2006.
134. S. Balci, K. Noda, A. Bittner, A. Kadri, C. Wege, H. Jeske, H.; et al., "Self-assembly of metal-virus nanodumbbells," *Angewandte Chemie International Edition,* vol. 46, pp. 3149-3151, 2007.
135. J. B.-H. Tok, F. Y. S. Chuang, M. C. Kao, K. A. Rose, S. S. Pannu, M. Y. Sha, et al., "Metallic striped nanowires as multiplexed immunoassay platforms for pathogen detection," *Angewandte Chemie International Edition,* vol. 45, pp. 6900-6904, 2006.
136. Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, pp. 1289-1292, 2001.

137. J. Hahm and C. M. Lieber, "Direct ultrasensitive electrical detection of DNA and DNA sequence variations using nanowire nanosensors," *Nano Letters,* vol. 4, pp. 51-54, 2004.
138. I. Park, Z. Li, X. Li, A. P. Pisano, and R. S. Williams, "Towards the silicon nanowire-based sensor for intracellular biochemical detection," *Biosensors and Bioelectronics,* vol. 22, pp. 2065-2070, 2007.
139. S. Huang and Y. Chen, "Ultrasensitive fluorescence detection of single protein molecules manipulated electrically on Au nanowire," *Nano Letters,* vol. 8, pp. 2829-2833, 2008.
140. I. Willner, B. Basnar, and B. Willner, "From molecular machines to microscale motility of objects: application as 'smart materials,' sensors, and nanodevices," *Advanced Functional Materials,* vol. 17, pp. 702-717, 2007.
141. J. C. Claussen, A. D. Franklin, A. ul Haque, D. M. Porterfield, and T. S. Fisher, "Electrochemical biosensor of nanocube-augmented carbon nanotube networks," *ACS Nano*, vol. 3, pp. 37-44, 2009.

This page intentionally left blank

CHAPTER 7

Cross-Section Fabrication and Analysis of Nanoscale Device Structures and Complex Organic Electronics

David W. Steuerman and Erich C. Walter

7.1 Introduction

A primary impediment to the advancement of molecular, polymer, and nanoscale electronics is the lack of available tools for characterization of devices and nanostructures. Our ability to synthesize and fabricate complex materials, molecules, and devices has far surpassed our instrumental abilities to probe their fundamental properties. Furthermore, device structures face the most extreme limitations to characterization, as virtually all traditional methods fail when materials are sandwiched between two electrodes.[1] The tools most often applied by chemists, such as mass spectrometry, infrared spectroscopy, and nuclear magnetic resonance, simply do not meet the demands required to explore emergent chemical signatures from materials systems sandwiched between electrodes. Examples of promising techniques developed and used across many disciplines to explore device structures include subsurface atomic force microscopy,[2] thermoelectric measurements,[3] single-molecule field-effect transistor measurements,[4,5] surface-enhanced Raman spectroscopy,[6] near-field scanning optical microscopy,[7] and Kelvin probe microscopy.[8] These examples provide a glimpse of the characterization complexity required for progress in device fabrication and analysis. Although much

has been learned about complex devices using these techniques, virtually no images of these complex devices exist.

This chapter provides examples of applications of cross-sectional imaging in complex structures. We begin the following section with a discussion of cross-section fabrication and describe in detail the procedure for creating lift-out cross sections. Our emphasis is on examining nanoscale and organic device structures with the primary concern of preserving a material's native structural integrity for electron microscopy representative imaging studies. Next, we concentrate on two distinct materials categories where the ability to extract and examine cross sections has proven valuable: organized nanoparticle assemblies and complex polymer devices. We conclude this chapter with a discussion of how cross sections could provide new and valuable insight in other systems.

7.1.1 Traditional Use of Cross Sections

Knowledge of layer structure and properties is of extreme importance in traditional electronic devices. This has become increasingly important as the dimensions of the layers, transistors, and vias in electronic devices shrink and as the devices become more and more complex. In order to verify structure and observe the possible points of failure; internal components of complex devices must be exposed. The traditional methods of preparing device cross sections, which include ultramicrotomography, polishing, electrochemical etching, and ion milling, do not achieve the same versatility and thinness of samples that can be obtained through the use of a *focused ion beam* (FIB). Microelectronic device imaging, modification, and characterization with FIBs began in the 1980s[9,10] and has become a well-established technique in semiconductor device failure analysis among other applications.[11–15]

Specifically relevant to this chapter is the FIB preparation of sample cross sections that can be as thin as ~100 nanometers (Fig. 7.1*A*).[16] In order to investigate morphologies and failure modes of device components embedded beneath the surface, thin slices are cut and extracted from the sample.[17] These extracted slices can be used for TEM imaging or subsequent analysis by other techniques, such as scanning probe microscopies. The use of a FIB to produce thin cross sections of complex devices reveals essential information that is often otherwise unobtainable. This is a general method with the potential to generate relatively unblemished nanoscale cross sections of a wide variety of materials without altering the sample structure.

Several different methods to prepare and extract cross sections of materials for subsequent analysis using FIB have been developed. The application of this technique to nanoscale devices, as shown in Fig. 7.1*B*, is a natural extension of FIB device cross-sectioning. This

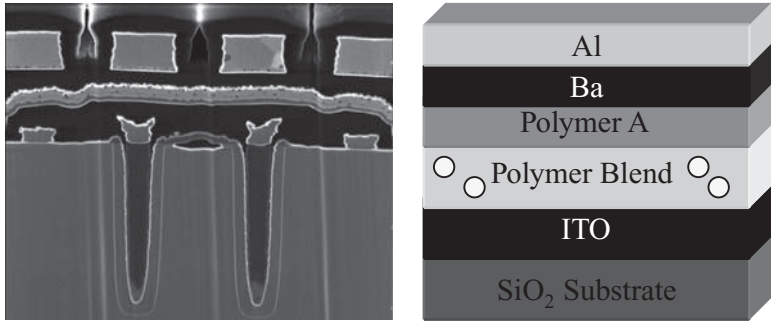


Figure 7.1 (*A*) Typical cross section of a group of transistors imaged via scanning electron microscopy. (*B*) Idealized schematic of a modern organic electronic device structure. Note the number of layers and variety of interfaces present. The circles are indicative of the integration of heterogeneous layers, such as polymer blended with nanoparticles. (*A*) adapted from http://www.fibinternational.com/samples.html.

technique allows direct visualization of material position in complex structures and interfaces. It is imperative to understand morphology of interfaces in particular because they have profound effects on device characteristics.[18,19] This more complete appreciation of structure-property relationships will further our understanding of devices and lead to more rapid performance and manufacturing optimization.

7.2 Device Cross-Section Fabrication and Imaging Considerations

Rendering a material sufficiently transparent to an electron beam, necessary for *transmission electron microscopy* (TEM) imaging, is often an incredibly challenging and delicate task. A variety of mechanical and chemical polishing techniques can be used, but conditions vary greatly by material.[20,21] Variations on polishing techniques were largely developed with bulk materials in mind and were not meant to produce a suitable sample for TEM at a specific position on a wafer. Creating cross-sectional samples of individual devices or other complex structures necessitates a different approach to sample preparation. This role was filled by FIB instruments, which can mill trenches in virtually any material and reliably produce cross-sectional samples in just a few hours. In this section, we discuss some of the precautions that should be taken when preparing samples for FIB cross-sectioning. This is followed by a step-by-step discussion of the FIB cross-section fabrication process.

7.2.1 Sample Preparation Prior to Cross-sectioning

As with any characterization technique, great care must be taken to ensure that minimal damage is done to the sample during processing. To this end, we suggest some minor procedures to protect the device or structure of interest so that it is minimally altered prior to imaging the cross section. Deposition of a sacrificial layer protects the surface of the future cross section from ion damage. The addition of a top layer of material does not pose a significant limitation, because most of the structures that benefit from cross-section analysis are usually beneath a metallic or dielectric layer. The protective layer can be deposited after electrical characterization to assess the performance of the device before cross-sectioning. In our studies, we have found that the electron beam evaporation of a 200-nm-thick layer of SiO_2, chosen mainly for its optical transparency, is suitable. We speculate that many other dielectrics would provide suitable protection, provided that the resulting film was not substantially strained. This 200-nm layer also protects the thin cross section against delamination during its mechanical transfer from the original device to the imaging substrate or grid. We have observed this step to be crucial in our analysis of organic *light-emitting diodes* (LEDs), as the most common mode of failure during fabrication was delamination of the polymers from the bottom electrodes. Finally, a thin layer of Au is sputter-deposited on the sacrificial dielectric to prevent charging, which would lead to poor imaging in the *scanning electron microscope* (SEM).

7.2.2 Cross-section Fabrication Procedure

Presently, most modern commercial FIB instruments provide a semi-automated method to produce lift-out cross-section samples from any position on a substrate with sub-100-nm accuracy. Depending on the desired sample type, the dimensions of the cross section are usually the critical parameters. Typical values for the cross sections prepared by the FIB are 12 mm long by 3 mm deep by 150 nm thick. Cross sections of this size will likely suffice for imaging most devices, because the electrodes and active components are near the surface and typically not thicker than a few hundred nanometers. The cross-sectional thickness is a parameter that can be readily optimized to produce structurally robust cross-section samples and the best conditions for imaging. In our experience, 150-nm-thick samples have yielded TEM images with satisfactory contrast. Other experimental probes of the cross section may require thicker or thinner samples, but this must be balanced with the need to maintain the structural integrity of the cross section. If the desired cross-sectional area extends deeper than ~3 mm below the surface, artifacts from re-ablated material from ion milling may become a serious concern. Additionally, one should also

keep in mind contamination from deposition of the Ga^+ beam source itself if elemental analysis is employed.

The greatest concern during the fabrication procedure is to limit the sample's exposure to and subsequent damage from the ion beam and, to a lesser extent, the electron beam. In order to minimize damage inherent to ion imaging, a dual-beam SEM/FIB was used. This approach requires more time to ensure that the foci of the ion-beam and electron beam are at an identical position on the substrate. The two beams come from separate columns, requiring that the sample be rotated such that the surface is normal to the beam flux. Finding the eucentric position is time consuming, but crucial to make cross sections in precise areas on the substrate. These requisite alignments of the beams and sample can usually be performed in an expendable region of the sample to further reduce sample damage. After alignment, one can begin the cross-section fabrication procedure at the desired area on the substrate by imaging via SEM.

The first step after identifying the desired cross-section region is the fabrication of alignment markers. These markers will define the size of the cross section, so care should be exercised in choosing their separation. Square markers (Fig. 7.2*A*) are deposited via FIB-assisted cleavage of a Pt-organometallic vapor plume injected just above the substrate. The Ga beam is rastered in a square pattern where the alignment markers are to be placed. As the Ga ions strike the plume, they cleave the Pt from the molecule and subsequently deposit the metal on the surface in the desired location. The FIB is then used to mill an "X" in each Pt square (Fig. 7.2*B*). These completed markers are used as references to ensure that the FIB does not impinge on the final cross-section area throughout the fabrication process. Using the Pt-organic vapor again, a thin Pt protective/supporting layer is deposited over the fabrication area between the markers (Fig. 7.2*C*). Next, the ion beam is used to mill two large trenches on either side of the cross section (Fig. 7.2*D–F*). Throughout the fabrication process, the alignment markers are reimaged to account for any drift that may have occurred. This pair of trenches will be repeatedly widened and deepened using progressively smaller ion beam apertures. The reduction in aperture size leads to less ion flux and less aggressive etching of the cross-section's faces. The area between these trenches slowly erodes until the separation reaches the final cross-section thickness. Midway through this thinning, the cross section is nearly freed from the substrate by milling along the bottom and sides of the wall (Fig. 7.2*G*). On completion, the cross section is suspended above the substrate by two thin tabs of Pt (Fig. 7.2*I*). In this geometry, the final cross section (10 mm $\times$ 3 mm $\times$ 150 nm) can be readily removed by a micromanipulated pulled glass rod and placed on a TEM grid. This procedure is referred to as the lift-out technique and was pioneered by Overwijk et al.[22]

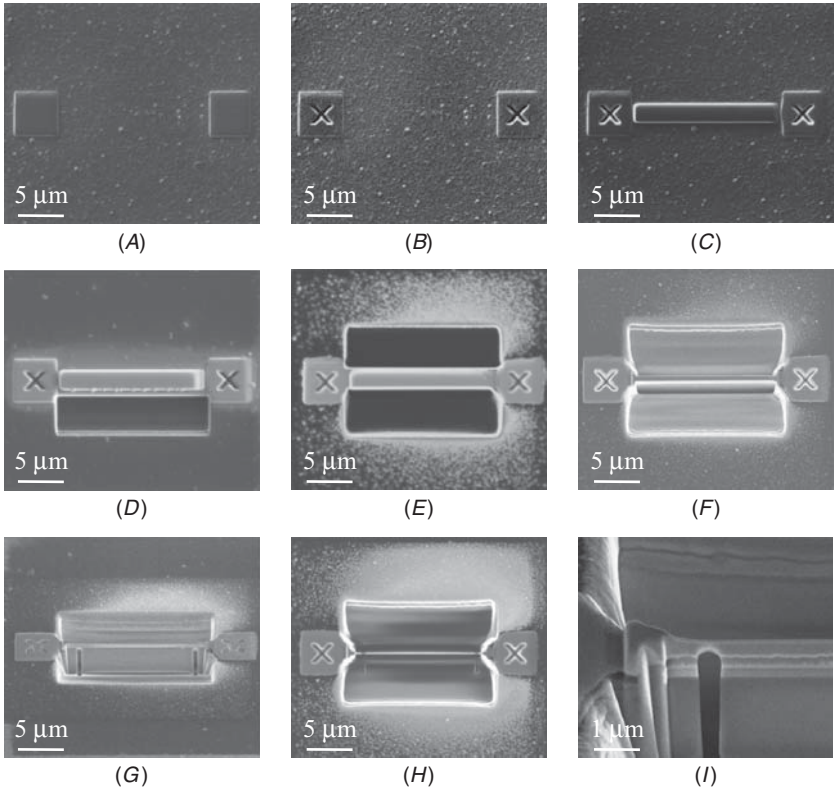


Figure 7.2 Sequence of fabrication steps employed to produce a FIB lift-out cross section for imaging: (*A*) deposition of Pt squares, (*B*) etching of alignment "X's," (*C*) deposition of Pt protective layer, (*D*) initial milling of trench, (*E*) milling of second trench, (*F*) continued milling of both trenches to thin the wall between them, (*G*) cross-section bottom and sides etched to begin freeing from the substrate (Note: sample tilted from top-down view), (*H*) final milling of trenches to produce thin cross section, (*I*) close-up after the fine milling of one of the two remaining Pt tabs that keep the cross section attached, yet suspended above the substrate.

The final delicate matter of removing the lift-out cross section with a micromanipulator requires patience, practice, and luck. This is where the ultimate yield of successful cross sections is largely defined. Once the appropriate cross-section dimensions and etch rates are adopted, most of the work within the FIB chamber proceeds with few complications. The rate of successful excision of the lift-out sample must be taken into consideration when one fabricates cross sections. In the beginning, we recommend making three or four cross sections from each device under test. Realistically, initial yields will be approximately 25%. Upon performing this procedure routinely, yields will likely reach 75 to 100%.

7.3 Case Studies

It is hard to imagine a more useful source of feedback when attempting to fabricate or optimize the performance of new materials or devices than actually seeing the finished product with nanometer resolution or better. In the following case studies we highlight five sophisticated structures that have been investigated with the aid of cross-sectional fabrication. The first group focuses on organized assemblies of nanoparticles. Case 1 is the study of molecularly assembled colloidal CdSe *nanocrystals* (NCs) embedded in an optical cavity. An examination of InAs *quantum dots* (QDs) embedded in a GaAs matrix synthesized via molecular beam epitaxy techniques is the subject of case 2. The second group explores complex polymer systems with an emphasis on novel device architectures. Case 3 is the study of a polymer-inorganic nanostructure hybrid photovoltaic. Case 4 is an example of device failure in a polymer device. Finally, the structure of polymer-polymer and polymer-electrode interfaces in a *polymer light-emitting diode* (PLED) is considered in case 5. It should be mentioned that not all case studies used the FIB cross-section fabrication technique, but we believe that it would be equally applicable to all the systems discussed.

7.3.1 Nanoscale Structures of Embedded Assemblies of Nanoparticles

The integration of nanomaterials into complex device structures has been a common theme in many technological and fundamental research pursuits.[23,24] Often, the precise positioning of a single nanoparticle or nanowire is critical to device performance. Electrical characterization of individual nanowires, for instance, requires pinpoint accuracy in the placement of contact electrodes; otherwise, shorts or nonohmic contacts can potentially ruin sensitive measurements. Fortunately, most measurements of this type occur at the surface of a substrate where atomic force microscopy or scanning electron microscopy techniques can assess the quality of the nanostructure initially and after device fabrication. On the other hand, a variety of structural platforms require embedded nanomaterials, making alternative approaches to imaging a necessity.

Case 1: Quantum Dot Assemblies by Molecular Beam Epitaxy

In order to understand and optimize the optoelectronic properties of quantum dots, a thorough knowledge of their shape and chemical composition is crucial. Given that the electronic states of these nanoscale artificial atoms are keenly size dependent, it follows that tools to assess the size, shape, and elemental composition can play a key role in understanding their complex behavior. In the case of

colloidal nanocrystals, which are synthesized by wet chemical methods, TEM has played a vital role in correlating optical and electronic properties with size and shape in a tremendous variety of nanostructures.[25] Nanocrystals of this type are readily transferred from solution environments to TEM grids for image analysis. On the other hand, artificial atoms resulting from strain engineering during *molecular beam epitaxy* (MBE) are frequently embedded in a host matrix.[26,27] This section concentrates on the nanoscale imaging of these QDs and the inherent challenge of imaging subsurface features. The Stranski-Krastanov growth mode in MBE has been applied to produce a wealth of quantum confined structures in recent years.[28] Characteristic of Stranski-Krastonov systems, layer-plus-island growth produces quantum-dot structures that can be controlled by strain engineering. The strain results from lattice mismatch of the QD material and host matrix. The embedded nature of these systems has a number of benefits, but likely the most important is that these nanostructures are readily integrated into semiconductor device architectures.

As interest in Stranski-Krastanov QDs increased, a pivotal discovery was made that paved the way for sophisticated control of the assembly of multiple QDs. In the mid-1990s, it was observed that a single QD could promote nucleation of another QD along the growth axis, thereby producing a pathway to yield vertically aligned QDs.[29] This was accomplished in a frequently studied system, InAs QDs that are fully embedded in a GaAs matrix. This breakthrough in assembly enabled the exploration of quantum mechanical phenomena beyond that of a single particle. Artificial atoms could be strategically positioned with near atomic-level precision (along the growth direction), thereby allowing the study of coupled QDs or QD molecules. This was accomplished by repeatedly depositing a few monolayers of InAs followed by up to nearly 100 monolayers of GaAs. The thickness of the GaAs spacer layer could be used to tune the electronic coupling between InAs QDs. Exploration of interdot coupling has been probed by photoluminescence,[30] and eventually electrical manipulation of QD coupling was achieved.[31]These assemblies of QDs have become a playground for exploring fundamental quantum mechanics and even model systems to study quantum information processing.[32–34] Arguably none of this research would have come to fruition without the unquestionable visual verification that the QDs were indeed stacked.

A TEM cross section (Fig. 7.3*A*) of an early example of InAs QDs in a GaAs matrix clearly demonstrates the correlation between QDs in the different layers of Stranski-Krastanov growth.[29] Such cross-section images allowed the authors to directly observe the QD-QD correlation as a function of spacer thickness. Remarkably, better than 95% correlation between vertically aligned QDs was observed at a separation of 36 monolayers. After evaluating many similar structures, the

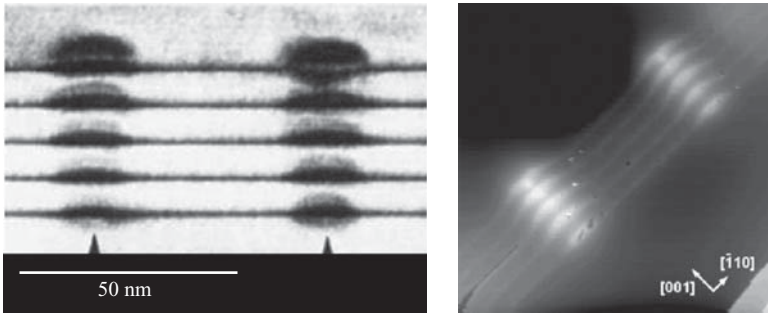


FIGURE 7.3 (*A*) TEM image and (*B*) STM image of vertically oriented InAs QDs in a GaAs matrix. (*A*) Adapted from Ref. 29. (*B*) Adapted from Ref. 35.

authors estimated that correlated nucleation ceased at a spacing of 200 monolayers.

Although these complex assemblies of QDs are nearly ideal for creating QD molecules, each QD possesses unique size, shape, and composition characteristics. Lack of this kind of detailed knowledge can significantly hamper quantitative understanding of optical and electronic properties of QD molecules. Imaging of cross sections has been demonstrated, but because of the large degree of strain and the difficulty in distinguishing In from Ga at the atomic level, traditional TEM imaging has proven insufficient. Fortunately, the flexibility of the cross section does not preclude the use of scanning probe techniques. An ultrahigh-vacuum, scanning tunneling microscopy study provided atomically resolved images of vertically aligned QDs (Fig. 7.3*B*).[35] Once again, a cross-section preparation technique gained access to the embedded QDs, and the authors of this study were able to definitively resolve the profile of individual QDs. Minor and short-range fluctuations in elemental composition of individual QDs also became apparent. The tunneling difference between sites occupied by In or Ga allowed visualization of the gradients present in the heterogeneous InGaAs alloy. In complementary studies, cross sections of individual QDs were examined by advanced analytical TEM techniques, including electron-energy-loss spectroscopy, to further explore alloying in these systems.[36]

Case 2: Molecularly Driven Assembly of Colloidal Nanoparticles in Optical Cavities

Optical cavities are frequently used to increase the sensitivity of many absorption and fluorescence techniques. In the most elementary cavities, one can think of the system classically as an integrated multipass sample cell.[37] Naturally, the greater number of passes produces

increased absorbance in accordance with Beer's law. Cavities that confine photons to subwavelength volumes with very little loss have to be treated quantum mechanically, which can lead to fundamentally new physics such as cavity quantum electrodynamics.[38,39] The focus of this section is the microscopy of colloidal nanoparticles in a 1D dielectric vertical cavity,[40] but the application of cross-sectional imaging would apply equally well to more complex cavity structures.

In the previous section, cross-sectional imaging was applied to an all-inorganic or "hard" materials system. Here, we discuss the application of FIB lift-out cross-section preparation and subsequent TEM imaging of wet-chemically synthesized materials and organic compounds. Specifically, we examine a *dielectric Bragg reflector* (DBR) cavity where CdSe *nanocrystals* (NCs) are assembled with the aid of conjugated disulfide-terminated molecules at the center (antinode) of the optical cavity. First, we briefly describe the cavity fabrication.

Fabrication of the DBR cavity begins with the electron beam evaporation of 5.5 pairs of TiO_2/SiO_2 quarter-wavelength layers deposited on a 1-mm-thick glass substrate. Next, the sample is capped with a thin SiO_2 layer to position a suitable surface for the molecular assembly of QDs in the center of the completed cavity. This SiO_2 surface is functionalized by immersing the sample into a 1 mM solution of 1,4-dihexyloxy-2,5-bis[4′-thiolstyryl]benzene in toluene for 2–4 hours.[41] This molecule contains two thiol functionalities for chemically binding CdSe QDs. The CdSe QD (6.8 nm diameter) layer is assembled by soaking the modified substrate in a QD solution for 12 to 16 hours (Fig. 7.4*A*). The same molecular self-assembly procedures can be repeated multiple times to achieve a sufficiently high optical density. Finally, a second TiO_2/SiO_2 DBR that is identical to the first series of

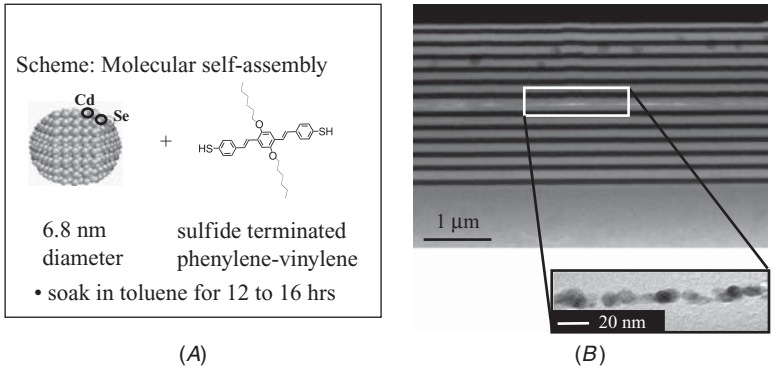


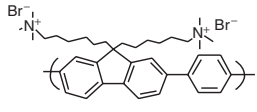
Figure 7.4 (*A*) Quantum dots and molecules used in assembly within optical cavity. (*B*) TEM image of the optical cavity cross section. (*Inset*) The resulting single monolayer of quantum dots in the center of the cavity structure. (*B*) adapted from Ref. 40.

depositions is evaporated to complete the cavity structure. To verify the positioning of NCs at the antinode of the cavity and assess the integrity of the NC layer structure after the deposition of the top portion of the cavity, FIB lift-out samples are fabricated and imaged by TEM.

Discerning the difference between TiO_2 layers from SiO_2 layers is straightforward (Fig. 7.4*B*).[40] Some inhomogeneity can be seen in the SiO_2 layers, which likely reduces dielectric cavity quality. This can be due to "spitting" from the source during deposition and is not uncommon when evaporating such refractory materials with an electron beam. Cross-section imaging can readily be used in optimization of dielectric layer quality, as well as to verify the thicknesses of individual layers. Control over the thickness is crucial if one wishes to produce the quarter-wavelength-thick layers necessitated by the DBR cavity design. These thicknesses and the calibration of the thickness monitor in the deposition tool can be determined by profilometry and ellipsometry techniques, but evaluation of the molecularly assembled CdSe layer must be probed by imaging the cross section. The inset of Fig. 7.4*B* shows the center of the cavity where NCs were assembled. Individual NCs are readily resolved, and the monolayer coverage can be qualitatively evaluated. For instance, this inset shows gaps between individual NCs and almost no stacked NCs. Therefore, this cavity possessed submonolayer coverage of NCs. The shape and size of the NCs also appeared identical to unembedded NCs, suggesting that the processing did not affect NC characteristics. Furthermore, no NCs were ever observed outside the central deposition region, signifying that NCs are not vertically mobile during the dielectric deposition. Imaging of the molecular components of the system proved too difficult, but the following sections show that it is possible in polymer systems.

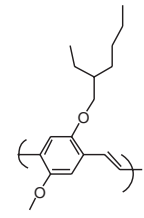
7.3.2 Organic Electronics

As the science of organic electronics continuously matures, performance often improves at the expense of increasingly complex materials and device architectures. Although synthetic chemists can produce an infinite number of modifications to polymeric materials in order to optimize device performance, there are often too many constraints to place on a single material. Depending on the device application, one may wish to engineer any combination or all of the following parameters: electron or hole injection efficiency, absorbance spectrum, emission spectrum, emission lifetime, etc. A PLED, for instance, is typically built on a transparent *indium tin oxide* (ITO) electrode modified by a buffer layer that has been optimized for hole injection. Next, a hole transport layer and emissive layer are deposited (usually by spin casting), followed by electron transport and injection layer addition. The PLED is finally completed by the deposition of a cathode (often a high-work-function metal).[42] Many variations of this scheme



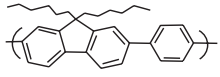
PFN$^+$ Br$^-$

poly[9,9-bis(6'-(*N,N,N*-trimethylammonium)-hexyl) fluorene-co-alt-phenylene] dibromide



MEH-PPV

poly[2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene]



PFP

poly[9,9-bis(6'-hexyl)fluorene-co-alt-phenylene]

P3HT

poly(3,4-ethylenedioxythiophene)

Figure 7.5 Chemical structures, names, and abbreviations of relevant polymers.

exist, but at their core all possess components embedded between electrodes. Most of the diversity in organic electronics is derived from the staggering array of materials that can be integrated into devices. Examples of two common chemical structures as well as a pair of more specialized polymers germane to this chapter are displayed in Fig. 7.5. Besides multilayer approaches to improve performance characteristics, the integration of inorganic materials is also commonly used. These polymer-inorganic hybrid systems are usually in the form of nanoparticle-doped materials. Although performance-based figures of merit are crucial to evaluating device platforms, nanoscale structural characterization of completed devices is instrumental in the development of devices with the aforementioned complexity.

Case 3: Complex Inorganic-Organic Hybrid Photovoltaics

Many polymer photovoltaics suffer from intrinsically low carrier mobility, and this hurts their overall efficiency.[43] Better charge separation and transport of electrons to the electrodes are approaches to improve the efficiency of polymer photovoltaics. In an effort to improve efficiency, as well as other device properties, nanoscale components can be dispersed in the polymer layers.[44,45] This nanoscale device will have structural elements that can vary by nanometers; so, it is critical to actually see where these elements are and how they are oriented to help understand the physical measurements and optimize device performance. A prime example of a complex inorganic-organic nanoscale device is the integration of cadmium selenide nanoparticles and nanorods into polymer solar cells.[46] Nanoparticles and nanorods

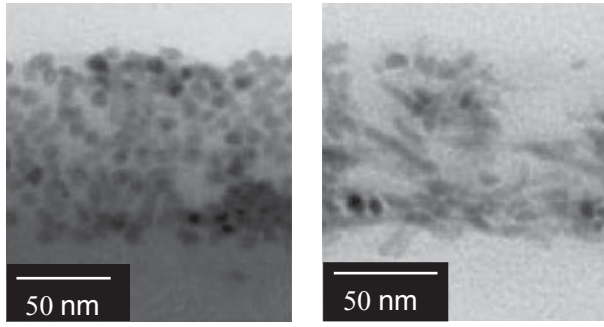


Figure 7.6 Cross-section TEM image of CdSe nanocrystals (*A*) and nanorods (*B*) integrated into a P3HT film spun on an epoxy substrate. Both panels adapted from Ref. 46.

were used to carry electrons more efficiently between layers and widen the absorption spectrum of the entire device. The nanoparticles and different length nanorods were co-dissolved in a solution of the conjugated polymer *poly-3(hexylthiophene)* (P3HT) and spin-cast onto PEDOT:PSS coated ITO substrates. The CdSe nanomaterials and P3HT were chosen for their solubilities as well as their complimentary absorption spectra in the visible region. A cross section of one film is shown in Fig. 7.6. The cross sections depicted here were obtained with a microtome and are of films cast onto support substrates specifically to survive the microtome process. The authors were attempting to determine the effect changing the length and diameter of nanorods had on the efficiency of the photoconversion. The devices with higher-aspect-ratio nanorods were shown to have higher efficiencies. This increase was attributed to better charge separation due to the wire length lowering the potential recombination. The orientation of the rods perpendicular to the substrate also has an effect on the charge separation, as longer nanorods promote increasingly efficient electron conduction within the polymer matrix. Obtaining a physical picture of the location and orientation of the nanoscale elements provided crucial morphological information, thus allowing the authors to explain the operational characteristics and physical properties of the device. In this case, a cross-sectional TEM picture is able to provide support for the hypothesis that the orientation of the nanorods perpendicular to the device electrodes can provide a directed path for electrical transport.

Case 4: Failure Analysis in a Polymer Bilayer Device

Failure analysis of device structures is common in the semiconductor and technology manufacturing sectors.[47,48] Devices are frequently composed of complex multilayer structures and corresponding

multiple interfaces. Evaluating these interfaces in a completed system is challenging, but crucial if we are to understand the performance characteristics of the final device. This concept is particularly important when devices fail catastrophically, such that the desired electrical characterization techniques cannot be applied. This is precisely what can happen in some bilayer PLEDs.

A number of studies have demonstrated that the efficiencies of multilayer PLEDs are substantially higher than their single-layer counterparts.[49–51] This widespread approach to performance optimization often requires small molecules or multiple polymers, in the form of either blends or multiple layers. In the multilayer approach, each polymer is individually tailored to address specific functions such as charge carrier injection/transport, carrier separation, light absorption, or emission. A central assumption behind this scheme is an understanding of the resulting complex interfaces. The use of conjugated polymers as the electron transport layer is less common, primarily because when multilayers are spun cast from organic solvents, some mixing of the components is unavoidable. The subject of this section is device failure as a result of a bilayer structure whose constituent polymers have similar solubility characteristics.

Attempts to fabricate bilayer PLEDs by spin coating *poly[9,9-bis(6′-hexyl)fluorene-co-alt-phenylene*] PFP on *poly[2-methoxy-5-(2′-ethylhexyloxy)-1,4-phenylene vinylene]* (MEH-PPV) (Fig. 7.7) has always resulted in devices that behave like short circuits.[52] The complete device structure should have been ITO on a glass slide with a layer of MEH-PPV, a layer of PFP, and an Al cathode on top. Assuming no mixing between the polymer layers, the resulting separation between electrodes should have been approximately 60 nm. High currents and ohmic responses from electrical characterization suggested that this

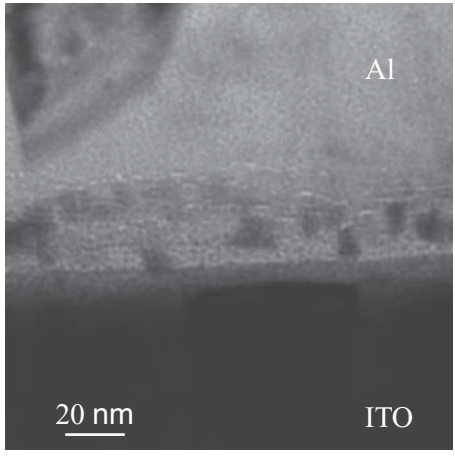


Figure 7.7 TEM image of a failed device structure resulting from PFP cast from toluene on top of MEH-PPV without annealing.

was clearly not the case, but what did the polymer junction look like? How thick was the bilayer? Were the observed shorts due to pinholes? The FIB lift-out cross-section fabrication was used to answer these questions.

The fabrication of the cross section was as described in Sections 2.1 and 2.2. Subsequent imaging of these devices verified that large areas of the anode and evaporated cathode were in intimate contact (Fig. 7.7). The identity of each layer can be verified by selected area diffraction or *secondary ion mass spectrometry* (SIMS), but when compared to the images in the following section, it will be clear that there is virtually no polymer separating the two electrodes. At the ITO/Al interface there is some evidence of heterogeneity and small grain sizes. We speculate that this may be a remnant of the organic layers. It appears that once MEH-PPV is cast, subsequent casting of PFP dissolves the majority of the predeposited polymer under our experimental conditions. In this particular polymer bilayer pair all devices failed, but it should be kept in mind that the flexibility of the FIB lift-out technique allows for site-specific examination. Thus, failure analysis of specific devices or regions can be performed anywhere on the wafer without affecting other functional devices. In the next section, we revisit polymer bilayer structures and demonstrate the combined strengths of the FIB lift-out technique and TEM imaging as applied to organic electronics.

Case 5: Polymer-Polymer and Polymer-Electrode Interfaces

In an effort to overcome the type of device failure discussed in the previous section, polymers with drastically different solubility characteristics have been explored within the multilayer architecture paradigm. One such pathway is the use of materials with charged functional groups such as *conjugated polyelectrolytes* (CPs). Because of the presence of the charged groups, which can be ionized in high-dielectric media, CPs are soluble in water and polar organic solvents. This provides a natural pathway to fabricate multilayer devices by solution means by alternating solvent polarity between layers. In fact, the efficiencies of multilayer PLEDs with CPs have already been shown to be substantially higher than those of their single-layer counterparts.[50,51,53] However, the operational assumption throughout this work and others like it has been that the casting of the top layer does not disrupt the underlying neutral conjugated polymer layer. This section examines this assumption by comparing cross-sectional images of a variety of bilayer polymer systems and devices.[52] As an added benefit, a discussion of the metal-polymer interfaces that are ubiquitous to organic electronics is also addressed. All of the cross-sectional images in this section were fabricated as described in section 2 of this chapter, only after the devices were characterized electrically.

Figure 7.8*A* is an image of a completed device composed of ITO/MEH-PPV/PFN+Br^-/Al. As alluded to earlier, the contrast

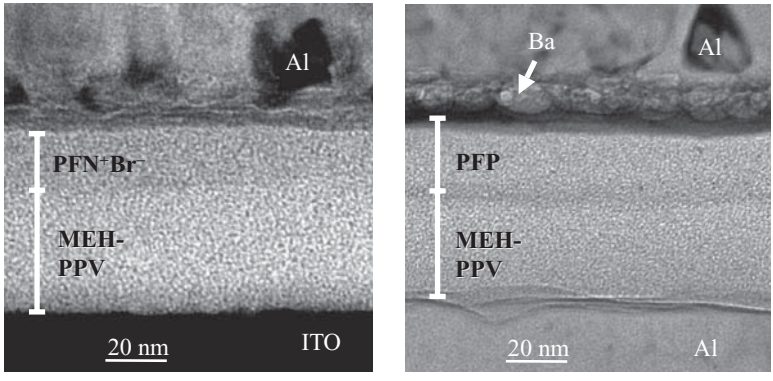


Figure 7.8 (*A*) TEM image of completed bilayer polymer device where both polymers are cast from dissimilar solvents. (*B*) TEM image of completed bilayer polymer device where both polymers are cast from similar solvents, but the MEH-PPV layer was annealed just prior to depositing the PFP layer. Both panels adapted from Ref. 52.

between the two polymer layers is small, but it is present. The white markers are included to clarify the demarcation of the layers. The interface position in the TEM image is consistent with single-layer thickness measurements made with an atomic force microscope. As designed, the interface between the conjugated polyelectrolyte PFN+Br^- and MEH-PPV is sharp and shows no evidence of substantial intermixing, because methanol is a poor solvent for the underlying polymer. The differences between the polymers also eliminate driving forces for mixing in the solid state, because MEH-PPV is hydrophobic and PFN+Br^- is hydrophilic. This conclusion is bolstered by the fact that the contrast in each polymer is constant, indicating that there is no compositional gradient between layers. As mentioned previously, the contrast difference between the bulk of each polymer layers is small. This makes it difficult to assess the interfacial width, but this region is estimated to be less than 2 nm from the TEM image.

To obtain a cross-sectional image of Al/MEH-PPV/PFN/Ba/Al (the subject of the previous subsection), the MEH-PPV was annealed after it was spun on the substrate. The heating process renders it significantly less soluble, and therefore PFN, which is cast from a nonpolar solvent, can be spun on top of it (Fig. 7.8*B*). The MEH-PPV interface varies smoothly from 2 to 15 nm along the length of the cross section. This is in contrast to the interface observed in Fig. 7.8*A*, suggesting that there is more intermixing between MEH-PPV and PFN than between MEH-PPV and PFN+Br^-. This mixing may be solvent mediated or

may evolve in the solid state; more analysis is required to be certain. It should be mentioned that contrary to Fig. 7.8*A*, there is little or no contrast difference between the polymer layers, yet the interface is clearly darker than the bulk of either MEH-PPV or PFN. We speculate that this could be due to interfacial dipoles or a contact potential phenomenon. Our discussion of polymer-polymer interfaces will be revisited, but now we describe polymer-metal interfaces.

We define the area bounded by bulk polymer signature and crystalline cathode material as the polymer-cathode interface. The PFN+Br−/Al interface is approximately 10 nm thick (Fig. 7.8*A*) and has some nanometer-scale morphological features as indicated by its parallel structures. This could be the result of aluminum oxide formation or an indication of Al diffusing into the polymer, most likely during the evaporation process. A comparison of Figs. 7.8*A* and 7.8*B* provides insight into the differences between two common electrode/polymer interfaces. The key variation is that the PFP/Ba interface is substantially rougher than that of PFN+Br^-/Al. This difference between Ba and Al does not depend on whether the polymer is PFP or PFN+Br^- (data not shown). It is likely due to the high degree of crystallinity of deposited Al and the small grain sizes of Ba.

The characterization of polymer-polymer interfaces in systems is intrinsically difficult because the contrast results from variations in electron scattering. Our source of differential scattering is a result of differences in molecular composition or polymer density. Because most conjugated polymers consist of light atoms such as carbon, hydrogen, oxygen, sulfur, and nitrogen, scattering is weak. The polymers discussed in this section both contain carbon and hydrogen. MEH-PPV possesses some oxygen, whereas PFN+Br^- has pairs of nitrogen and bromide ions. Overall, the electron density differences are small, thus explaining the weakly observed contrast. Stains and dyes were avoided to preserve the integrity of the native device structure,[54–56] albeit at the expense of contrast.

Because of the inherent challenge of distinguishing one polymer layer with a carbon-based backbone from another polymer layer composed of similar atomic building blocks, alternative techniques need to be used to validate conclusions drawn from TEM images. We now describe the SIMS approach employed to aid in the interpretation of images of multilayer polymer structures. This technique has been used previously to characterize various types of interfaces, including polymers.[57–61] In brief, the SIMS technique calls for a high-energy ion beam (typically, Ga^+, O_2^-, or Cs^+) directed on the sample surface and the generated ions, atoms, clusters of atoms, and molecular fragments are detected as a function of time by the mass spectrometer, which is proportional to the depth profile of the sample. Thus, this technique allows observation of elemental composition as function of depth from the surface of the sample. SIMS can provide depth profiles

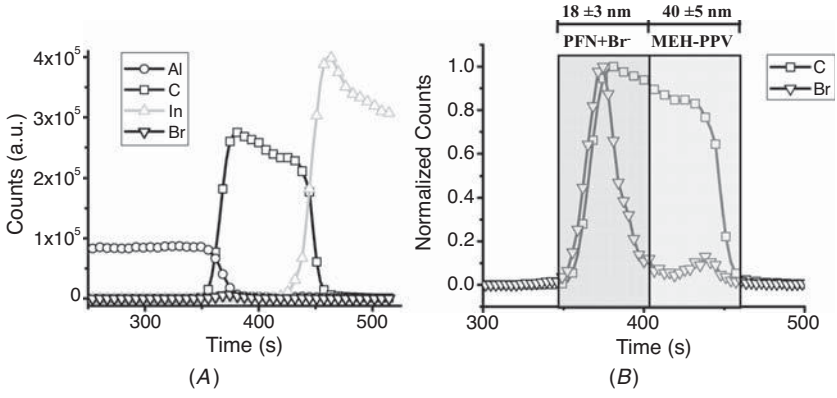


FIGURE 7.9 SIMS signal from a device structure identical to that of Fig. 7.8*A*. (*A*) Four separate mass channels are monitored as a function of time to determine which layer is actively being etched by an oxygen plasma. (*B*) Normalized SIMS spectra of the Br and C ions that have been correlated with individual etch craters to determine the thickness of each polymer layer. Both panels adapted from Ref. 52.

with resolution to a few nanometers and parts-per-million sensitivity. The etching beam is typically rastered over an area approximately 150 mm by 150 mm, where the generated ion fragments from the central 20 mm by 20 mm region are chosen for detection as a function of time by mass spectroscopy.

Because conjugated polymers generally have similar elemental composition (largely composed of C, O, and H), determining the thickness of the individual layers of the bilayers can be quite challenging by mass spectrometry techniques. However, the ITO/MEH-PPV(unannealed)/PFN+Br^-/Al device (Fig. 7.8*A*) provides a valuable testbed to evaluate our TEM images. This opportunity arises because the PFN+Br^- layer contains bromide counterions, which are readily distinguishable from other fragments by SIMS. Figure 7.9*A* plots the intensity of key fragments from an ITO/MEH-PPV(unannealed)/PFN+Br^-/Al device as a function of time that the ion beam is incident on the surface. First, removal of the Al top electrode is observed. As the Al signal decays, C and Br signals grow because the PFN+Br^- layer is being fragmented. Because there are two Br ions and 30 C atoms per monomer, the Br signal is much lower than the C signal. At 400 s, the Br signal drops significantly, while the C signal persists for another 100 s. Fragments of In are eventually detected once the oxygen plasma reaches the depth of the ITO-coated glass substrate. The normalized fragment intensity for C and Br allows us to focus on the polymer bilayer where the first source of C (presumably from the PFN+Br^-) is correlated with a large signal in the Br channel (Fig. 7.9*B*). Approximately midway through the C-rich

region of the SIMS spectrum, C amplitude shallowly decreases and Br signal drops ~90% in intensity. The combination of these two spectral characteristics indicate that the C signal comes from distinct polymer layers. These aforementioned spectral features are used to determine the thicknesses of the constituent polymer layers (PFN+Br^-/MEH-PPV).

To resolve each individual layer, multiple craters are etched to different depths corresponding to the emergence and appearance of the elemental fragments just discussed. The first crater was etched until the Al signal dropped and the C signal began. A second crater was etched slightly deeper and progressed until the Br signal approached the baseline. For the final and deepest etch, a third crater was created that stopped at the beginning of the In signal. A profilometer was used to determine the depth of all three craters, which in turn revealed the thicknesses of the two polymer layers. This combination of SIMS and the profilometry measurements suggest that the PFN+Br^- and the MEH-PPV layer thicknesses are 22 ± 3 nm and 58 ± 5 nm, respectively. These values agree with the results obtained from cross-sectional TEM image analysis. Thus, SIMS spectral signatures support distinct partitioning of the polymer bilayer constituents observed in the TEM images.

Having established the characterization in device configurations, we focus on other double-layer model structures. Because both polymers of the P3HT/PFN+Br^- interface were spun cast from solvents with very different polarity (toluene and methanol), a sharp interface occurs with little or no mixing of the layers (Fig. 7.10*A*). The interface is itself is quite clear, but not the source of the contrast, which could be a high-density polymer phase, an interfacially charged region, or another source of electron scattering. There is no significant variation in the thickness of this interface, suggesting it is more robust

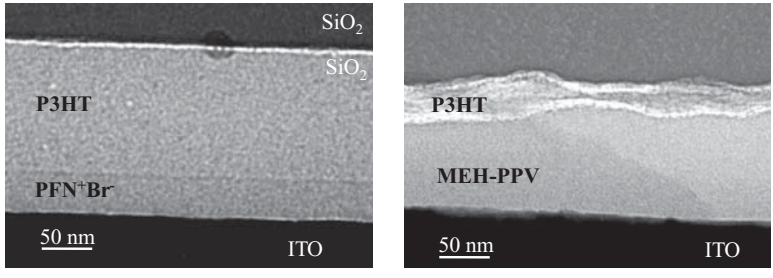


Figure 7.10 (*A*) TEM image demonstrating a sharp, well-defined interface between two polymers (P3HT spun on PFN$^+Br^-$). (*B*) TEM image demonstrating a poorly defined polymer-polymer interface (P3HT spun on MEH-PPV). Both panels adapted from Ref. 52.

than those observed in Figs. 7.8*B* and 7.10*B*. An example of a complex interface that can result when two neutral polymers spun cast from the same solvent, MEH-PPV(toluene)/P3HT(toluene), is presented in Fig. 7.10*B*. The resulting interface is nonuniform and difficult to define. It appears that the P3HT solution partially dissolves some of the initial MEH-PPV film, resulting in a complex and heterogeneous bilayer. This kind of bilayer structure suggests that it would be difficult to engineer recombination regions by controlling the confinement of holes or electrons to one particular polymer in systems like these. In fact, it is surprising that the underlying MEH-PPV layer was not dissolved completely on casting the P3HT layer, as in the case of MEH-PPV(unannealed)/PFP. This pair emphasizes both the degree of variation between polymer-polymer interfaces that can result in bilayer structures and the strength of cross-sectional TEM analysis.

7.4 Future Opportunities and Conclusions

Although the focus of this chapter has been on the preparation of lift-out cross sections, which was developed for transmission electron studies, these samples could be examined by any number of techniques such as atomic force microscopy, scanning tunneling microscopy, or near-field scanning optical microscopy. In fact, it was shown in Ref. 44 that exposed cross sections could provide fruitful samples for STM investigations. We believe this to be indicative of the potential for sample fabrication in this unique geometry. Further, lift-out cross sections may provide novel paths to fabricate device structures that might otherwise be inaccessible or unreliable. For instance, one can envision the use of the cross section to define large, well-controlled, few-nanometer gap junctions. This would be accomplished by fabricating a traditional micron-scale planar molecular tunnel junction between two metallic electrodes. Spacing between the metals would be defined by the thickness of the molecular monolayer. This junction would be cut away by the lift-out technique and transferred to a substrate. Subsequently, each electrode could be individually wired by electron beam lithography. This protocol could produce planar tunnel junctions with dimensions of ~100 nm tall by ~10 mm with a gap that could be controlled by the width of the molecular monolayer or another dielectric layer. Besides the exploration of this somewhat exotic device geometry, extending the cross-section technique to other polymer optoelectronic and molecular electronic systems would provide access to previously unavailable structural insight. The potential for better correlation between measured performance and theoretical modeling is likely. This could prove crucial in nanoscale junctions, where tunneling currents dominate and are exquisitely sensitive to electrode separation.

In conclusion, we have discussed the preparation of cross-section samples and cited five example systems that substantially benefited from their characterization. The materials systems ranged from traditional inorganic solid-state materials to complex polymeric device structures. In all cases the cross section provided a wider appreciation of how different materials and various processing options relate to interfaces in complex structures, and even functioning devices. From the studies highlighted here, we have attempted to demonstrate that the inherently rich and complex features buried beneath the surface can be made accessible.

References

1. E. M. Vogel, "Technology and metrology of new electronic materials and devices," *Nature Nanotechnology*, vol. 2, pp. 25-32, 2007.
2. G. S. Shekhawat and V. P. Dravid, "Nanoscale imaging of buried structures via scanning near-field ultrasound holography," *Science*, vol. 310, pp. 89-92, 2005.
3. P. Reddy, S.-Y. Jang, R. Segalman, and A. Majumdar, "Thermoelectricity in molecular junctions," *Science*, vol. 315, pp. 1568-1571, 2008.
4. J. Park, A. N. Pasupathy, J. I. Goldsmith, C. Chang, Y. Yaish, J. R. Petta, et al., "Coulomb blockade and the Kondo effect in single-atom transistors," *Nature*, vol. 417, pp. 722-725.
5. W. Liang, M. P. Shores, M. Bockrath, J. R. Long, and H. Park, "Kondo resonance in a single-molecule transistor," *Nature*, vol. 417, pp. 725-729.
6. M. E. Stewart, C. R. Anderton, L. B. Thompson, J. Maria, S. K. Gray, J. A. Rogers, et al., "Nanostructured plasmonic sensors," *Chemical Reviews*, vol. 108, pp. 494-521, 2008.
7. R. C. Dunn, "Near-field scanning optical microscopy," *Chemical Reviews*, vol. 99, pp. 2891-2927, 1999.
8. H. Hoppe, T. Glatzel, M. Niggemann, A. Hinsch, M. Ch. Lux-Steiner, and N. S. Sariciftci, "Kelvin probe force microscopy study on conjugated polymer/fullerene bulk heterojunction organic solar cells,". *Nano Letters*, vol. 5, pp. 269-274, 2005.
9. J. R. A. Cleaver, E. C. G. Kirk, R. J. Young, and H. Ahmed, "Scanning ion beam techniques for the examination of microelectronic devices," *Journal of Vacuum Science and Technology B*, vol. 6, pp. 1026-1029, 1988.
10. E. C. G. Kirk, R. A. McMahn, J. R. A. Cleaver, and H. Ahmed, "Scanning ion microscopy and microsectioning of electron beam recrystallized silicon on insulator devices," *Journal of Vacuum Science and Technology B*, vol. 6, pp. 1940-1943, 1988.
11. R. Krueger, "Dual-column (FIB–SEM) wafer applications," *Micron*, vol. 30, pp. 221-226, 1999.
12. A. Lins, L. A. Giannuzzi, F. A. Stevie, B. Price, M. Tucker, and N. Gutman, "FIB/TEM analysis of paint layers from Thomas Eakins' *The Crucifixion*, 1880," *Materials Research Society Symposium Proceedings*, vol. 712, 2002.
13. S. Matsui and Y. Ochiai, "Focused ion beam applications to solid state devices," *Nanotechnology*, vol. 7, pp. 247-258, 1996.
14. C. R. Perrey, C. B. Carter, J. R. Michael, P. G. Kotula, E. A. Stach, and V. R. Radmilovic, "Using the FIB to characterize nanoparticle materials," *Journal of Microscopy*, vol. 214, pp. 222-236, 2004.
15. M. W. Phaneuf, "Applications of focused ion beam microscopy to materials science specimens," *Micron*, vol. 30, pp. 277-288, 1999.
16. L. A. Giannuzzi and F. A. Stevie, "A review of focused ion beam milling techniques for TEM specimen preparation," *Micron*, vol. 30, pp. 197-204, 1999.

17. R. M. Langford and A. K. Petford-Long, "Preparation of transmission electron microscopy cross-section specimens using focused ion beam milling," *Journal of Vacuum Science and Technology A*, vol. 19, pp. 2186-2193, 2001.
18. L.-M. Chen, Z. Hong, G. Li, and Y. Yang, "Recent progress in polymer solar cells: manipulation of polymer:fullerene morphology and the formation of efficient inverted polymer solar cells," *Advanced Materials*, vol. 21, pp. 1434-1449, 2009.
19. J. R. Heath and M. A. Ratner, "Molecular electronics," *Physics Today*, vol. 56, pp. 43-49, 2003.
20. P. J. Goodhew, *Practical Methods in Electron Microscopy: Thin Foil Preparation for Electron Microscopy*, vol. 2, New York, Elsevier, 1985.
21. K. C. Thomson-Russell and J. W. Edington, *Practical Electron Microscopy in Materials Science: Electron Microscope Preparation Techniques in Material Science*, London, Macmillan, 1977.
22. M. H. F. Overwijk, F. C. van den Heuvel, and C. W. T. Bulle-Lieuwma, "Novel scheme for the preparation of transmission electron microscopy specimens with a focused ion beam," *Journal of Vacuum Science and Technology B*, vol. 11, p. 2021, 1993.
23. D. L. Klein, R. Roth, A. K. L. Lim, A. P. Alivisatos, and P. L. McEuen, "A single-electron transistor made from a cadmium selenide nanocrystal," *Nature*, vol. 389, pp. 699-701, 1997.
24. X. Duan, Y. Huang, R. Agarwal, and C. M. Lieber, "Single-nanowire electrically driven lasers," *Nature*, vol. 421, pp. 241-245, 2003.
25. C. B. Murray, C. R. Kagan, and M. G. Bawendi, "Synthesis and characterization of monodisperse nanocrystal and close-packed nanocrystal assemblies," *Annual Review of Materials Science*, vol. 30, pp. 545-610, 2000.
26. D. Bimberg, M. Grundmann, and N. N. Ledentsov, *Quantum Dot Heterostructures*, Wiley, New York, 1998.
27. P. W. Fry, I. E. Itskevich, D. J. Mowbray, M. S. Skolnick, J. J. Finley, J. A. Barker, et al., "Inverted electron-hole alignment in InAs-GaAs self-assembled quantum dots," *Physical Review Letters*, vol. 84, pp. 733-736, 2000.
28. C. Teichert, "Self-organization of nanostructures in semiconductor heteroepitaxy," *Physics Reports*, vol. 365, pp. 335, 2002.
29. Q. Xie, A. Madhukar, P. Chen, and N. P. Kobayashi, "Vertically self-organized InAs quantum box islands on GaAs(100)," *Physical Review Letters*, vol. 75, pp. 2542-2545, 1995.
30. M. Bayer, P. Hawrylak, K. Hinzer, S. Fafard, M. Korkusinski, Z. R. Wasilewski, et al., "Coupling and entangling of quantum states in quantum dot molecules," *Science*, vol. 291, pp. 451-453, 2001.
31. H. J. Krenner, M. Sabathil, E. C. Clark, A. Kress, D. Schuh, M. Bichler, et al., "Direct observation of controlled coupling in an individual quantum dot molecule," *Physical Review Letters*, vol. 94, p. 057402, 2005.
32. D. Loss and D. P. Divincenzo, "Quantum computation with quantum dots," *Physical Review A*, vol. 57, pp. 120-126, 1998.
33. A. Imamoglu, D. D. Awschalom, G. Burkard, D. P. DiVincenzo, D. Loss, M. Sherwin, et al., "Quantum information processing using quantum dot spins and cavity QED," *Physical Review Letters*, vol. 83, pp. 4204-4207, 1999.
34. E. Biolatti, R. C. Iotti, P. Zanardi, and F. Rossi, "Quantum information processing with semiconductor macroatoms," *Physical Review Letters*, vol. 85, pp. 5647-5650, 2000.
35. D. M. Bruls, P. M. Koenraad, H. W. M. Salemink, J. H. Wolter, M. Hopkinson, and M. S. Skolnick, "Stacked low-growth-rate InAs quantum dots studied at the atomic level by cross-sectional scanning tunneling microscopy," *Applied Physics Letters*, vol. 82, pp. 3758-3760, 2003.
36. P. Wang, A. L. Bleloch, M. Falke, P. J. Goodhew, J. Ng, and M. Missous, "Direct measurement of composition of buried quantum dots using aberration-corrected scanning transmission electron microscopy," *Applied Physics Letters*, vol. 89, p. 072111, 2006.

37. J. Altmann, R. Baumgart, and C. Weitkamp, "Two-mirror multipass absorption cell," *Applied Optics*, vol. 20, p. 995, 1981.
38. E. M. Purcell, "Spontaneous emission probabilities at radio frequencies," *Physical Review B*, vol. 69, p. 681, 1946.
39. S. Ghosh, W. H. Wang, F. M. Mendoza, R. C. Myers, X. Li, N. Samarth, A. C. Gossard, and D. D. Awschalom, "Enhancement of spin coherence using Q-factor engineering in semiconductor microdisc lasers," *Nature Materials*, vol. 5, pp. 261-264, 2006.
40. Y. Q. Li, D. W. Steuerman, J. Berezovsky, D. S. Seferos, G. C. Bazan, and D. D. Awschalom, "Cavity enhanced Faraday rotation of semiconductor quantum dots," *Applied Physics Letters*, vol. 88, p. 193126, 2006.
41. D. S. Seferos, D. A. Banach, N. A. Alcantar, J. N. Israelachvili, and G. C. Bazan, "α,ω-Bis(thioacetyl)oligophenylenevinylene chromophores from thioanisol precursors," *Journal of Organic Chemistry*, vol. 69, pp. 1110-1119, 2004.
42. Y. Shirota and H. Kageyama, "Charge carrier transporting molecular materials and their applications in devices," *Chemical Reviews*, vol. 107, pp. 953-1010, 2007.
43. L. Bozano, S. A. Carter, J. C. Scott, G. G. Malliaras, and P. J. Brock, "Temperature- and field-dependent electron and hole mobilities in polymer light-emitting diodes," *Applied Physics Letters*, vol. 74, p. 1132, 1999.
44. A. P. Alivisatos, "Semiconductor clusters, nanocrystals, and quantum dots," *Science*, vol. 271, pp. 933-937, 1996.
45. J. M. Rehm, G. L. McLendon, Y. Nagasawa, K. Yoshihara, J. Moser, and M. Grätzel, "Femtosecond electron-transfer dynamics at a sensitizing dye−semiconductor (TiO_2) interface," *Journal of Physical Chemistry*, vol. 100, pp. 9577-9578, 1996.
46. W. U. Huynh, J. J. Dittmer, and A. P. Alivisatos, "Hybrid nanorod-polymer solar cells," *Science*, vol. 295, pp. 2425-2427, 2002.
47. S. Tsuji, A. M. Tanaka, H. Iwama, N. Tsutsui, K. Kuroda, and H. Saka, "Cross-sectional characterization of thin-film transistors with transmission electron microscopy," *Journal of Vacuum Science and Technology B*, vol. 13, pp. 1353-1357.
48. E. J. Crawford, L. Gignac, K. Barth, J. Petrus, and E. Levine, "Focused ion beam sectioning and lift-out method for copper and resist vias in organic low-*k* dielectrics," *Microscopy and Microanalysis*, vol. 8, pp. 502-508, 2002.
49. X. Gong, S. Wang, D. Moses, G. C. Bazan, and A. J. Heeger, "Multilayer polymer light-emitting diodes: white-light emission with high efficiency," *Advanced Materials*, vol. 17, pp. 2053-2058, 2005.
50. L. S. Hung and C. H. Chen, "Recent progress of molecular organic electroluminescent materials and devices," *Materials Science and Engineering R*, vol. 39, pp. 143-222, 2002.
51. J. Li, T. Sano, Y. Hirayama, T. Tomita, H. Fujii, and K. Wakisaka, "Improvement of electroluminescence efficiency of blue-polymer-light-emitting diodes using polymer hole-transporting and electron-transporting layers," *Japanese Journal of Applied Physics*, vol. 45, pp. 3746-3749, 2006.
52. D. W. Steuerman, A. Garcia, M. Dante, R. Yang, J. P. Löfvander, and T.-Q. Nguyen, "Imaging the interfaces of conjugated polymer optoelectronic devices," *Advanced Materials*, vol. 20, pp. 528-534, 2008.
53. X. Gong, S. Wang, D. Moses, G. C. Bazan, and A. J. Heeger, "Multilayer polymer light-emitting diodes: white-light emission with high efficiency," *Advanced Materials*, vol. 17, pp. 2053-2058, 2005.
54. Z. Yin, J. Yang, N. Coombs, M. A.Winnik, R. A. Ryntz, and P. V. Yaneff, "Quantitative probing the interfacial structure of TPO/CPO by TEM via EDX," *Polymer*, vol. 48, pp. 1297-1305, 2007.
55. J. S. Trent, J. I. Scheinbeim, and P. R. Couchman, "Electron microscopy of PS/PMMA and rubber-modified polymer blends: use of ruthenium tetroxide as a new staining agent," *Journal of Polymer Science: Polymer Letters Edition*, vol. 19, pp. 315-319, 1981.

56. R. J. Spontak, M. C. Williams, and D. A. Agard, "Interphase composition profile in SB/SBS block copolymers, measured with electron microscopy, and microstructural implications," *Macromolecules*, vol. 21 pp. 45-47, 1988.
57. M. S. Wagner, "Molecular depth profiling of multilayer polymer films using time-of-flight secondary ion mass spectrometry," *Analytical Chemistry,* vol. 77, pp. 911-922, 2005.
58. J. K. J. Van Duren, X. Yang, J. Loos, C. W. T. Bulle-Lieuwma, A. B. Sieval, J. C. Hummelen, et al., "Relating the morphology of poly(p-phenylene vinylene)/methanofullerene blends to solar-cell performance," *Advanced Functional Materials*, vol. 14, pp. 425-434, 2004.
59. W.-Y. Chen, Y.-C. Ling, B.-J. Chen, H.-H. Shih, and C.-H. Cheng, "Diffusion study of multi-organic layers in OLEDs by ToF-SIMS ," *Applied Surface Science*, vol. 252, pp. 6594-6596, 2006.
60. W. Song, Z. Li, S. K. So, Y. Qiu, Y. Zhu, and L. Cao, "Dynamic SIMS characterization of interface structure of Ag/Alq3/NPB/ITO model devices," *Surface and Interface Analysis*, vol. 32, pp. 102-105, 2001.
61. B. Kim, H. Kang, K. Char, K. Katsov, G. H. Fredrickson, and E. J. Kramer, "Interfacial roughening induced by the reaction of end-functionalized polymers at a PS/P2VP interface: quantitative analysis by DSIMS," *Macromolecules*, vol. 38, pp. 6108-6111, 2005.

CHAPTER 8

Microfabrication and Applications of Nanoparticle-Doped Conductive Polymers

Bonnie L. Gray and Ajit Khosla

8.1 Introduction

Nanotechnology has enabled the development of new materials at the nanoscale with new properties compared to bulk materials. Although the development of nanoscale devices and *nanoelectromechanical systems* (NEMS) and sensors directly using nanoparticles is a fast-moving field of nanotechnology, one exciting application is the employment of these new nanoparticles to realize new multifunctional composite materials that exploit the novel characteristics of nanoparticles by combining them with materials that have well-known manufacturing methods and patterning at the microscale. Although nanoparticles may be utilized for many different applications, such as to make improvements in strength or make a polymer magnetic, of particular interest to microelectronics and other microsystems development are nanomaterials and polymers that can be combined to yield *conductive nanocomposite polymers* (C-NCPs) for applications in flexible electronic routing, flexible electrodes, microsensors, actuators, and packaging.

Polymer materials are increasingly used in microelectronics and other microsystems applications such as *microelectromechanical systems* (MEMSs), microsensors, and microfluidics. Polymers have many advantages over other materials including low cost, mechanical properties such as flexibility and mechanical compliance, and ease

of inexpensive processing. Many polymer materials provide greater mechanical yield strain and are less brittle than more traditional silicon-based MEMS materials. Polymers, especially elastomers, can be deformed to a very high degree, making them very attractive for applications that require high flexibility. Many polymer materials are also of low cost, with relatively lower cost processing compared to silicon-based microfabrication, which may require specialized microelectronics fabrication equipment. Polymer substrates can be obtained in virtually any shape and size, as opposed to flat silicon wafers cut along crystal planes. Electronics and optoelectronics are also migrating toward polymers for devices and applications such as memory, transistors, optoelectronic devices, and flexible displays. Furthermore, polymers provide functionality not possible with conventional silicon-based microfabrication, for realization of new sensors, actuation, and packaging, as well as fluid-tight platforms for microfluidics and biomedical microdevices and systems.

Polymers that are commonly used for microsystems have been used as base materials for a whole host of C-NCPs and include *polydimethylsiloxane* (PDMS) silicone and other elastomers that may be molded or photopatterned; SU-8 photopatternable epoxy and other conductive pastes and epoxies derived primarily from the integrated circuit packaging industry; polystyrene, polystyrene/polypropylene copolymer, *poly(methyl methacrylate)* (PMMA), polyurethane, polyimide, polyethylene, polycarbonate, and more.

Nanocomposite polymers (NCPs) can be made by embedding nanoparticles (e.g., nanosized flakes, spheres, cylinders or tubes) into a polymer matrix that forms the base, or matrix. Sometimes other polymers or other materials are added to enhance the polymer properties or aid in dispersion of nanoparticles, which may tend to agglomerate in their natural state. C-NCPs are those materials in which the nanoparticles that are added to the polymer cause or enhance conductivity once a certain threshold of nanoparticle percentage is reached, known as the percolation threshold (see Section 8.2), above which the addition of more nanoparticles does not continue to provide a large increase in conductivity. This percolation threshold is a function of both polymer and nanoparticle properties, and it is advantageous if the percolation threshold is low, because this results in a conductive material that may retain many of the mechanical and other desirable properties of the intrinsic polymer that made it attractive to use initially.

Although many materials researchers have focused on in-depth characterization of C-NCP materials, microfabrication engineers and micromachinists have investigated the ability to pattern some of these nanocomposite conductive polymers into microscale structures using newly emerging research in the patterning of undoped polymer microstructures. Such patterning techniques include micromolding via soft lithography, photopatterning using UV light in a process similar to integrated circuit photolithography, and microembossing.

In addition to microelectronics, nanocomposite polymers are finding employment in other microsystems areas, including MEMS, microsensors, microfluidics, and biomedical microdevices. Conductive nanocomposite polymers may make excellent conductive lines for electronic interconnect for components in a flexible polymer package. Furthermore, the sensitivity of nanocomposite polymer conductivity to applied forces makes them excellent force/pressure sensors and strain gauges, as well as chemical sensors that detect polymer expansion in the presence of analyte. Other functionality of nanocomposite polymers can be employed for other applications, and some of these are introduced briefly throughout the chapter without detracting from the chapter's primary focus of conducting nanocomposite polymers for microsystems applications.

The chapter is outlined as follows: First, a discussion of NCP general characteristics is given in Section 8.2, in which the important concepts of fill factor and percolation threshold are introduced. Section 8.3 follows with a discussion of the different nanoparticle materials and morphologies often employed for C-NCPs generally, with a bias toward micropatternable C-NCPs. Section 8.4 is organized primarily by polymer base matrix, with subheadings for various nanoparticle dopants, discussing representative research that has been performed for each material, its preparation, and micropatterning methodology. Section 8.5 addresses sample applications of C-NCPs, particularly in microelectronics and microsystems, and the chapter ends with Section 8.6, which summarizes the chapter and discusses future directions.

8.2 Fill Factor and Percolation Threshold

The electrical conductivity of a conductive nanocomposite polymer is strongly dependent on the volume fraction of nanoparticles in the polymer matrix, known as the *fill factor*. At low fill factors, the NCP behaves much as it would without filler and primarily takes on the characteristics of the undoped polymer, including low conductivity. At high fill factors, the polymer may take on very different properties as specified by the filler material. However, care must be taken that the filler density is not too high, because this may have a detrimental effect on, for example, the polymer mechanical properties or proper curing at the expense of higher conductivity. A thermosetting polymer that cannot cure because of high fill factor, or one that has substantially lower flexibility than the undoped polymer, is usually undesirable.

Volume percent is the volume of solute divided by the volume of solution multiplied by 100 to get the percentage. *Weight percent* is equal to the weight of solute divided by the weight of solution multiplied by 100%. It should be noted that both of these are used in the literature, or their fractional amounts found by leaving out the multiplication by 100 to get percentage. In general, volume percent is used when the two items being mixed are both liquids, and weight percent is used

when one or both are in solid (e.g., nanoparticle powder) form. The two are related based on the densities of both materials.

Percolation threshold is the point at which the first continuous chain of linked conductive filler particles is present, and can be explained using percolation theory.[1] In mathematics, percolation theory describes the behavior of connected clusters in a random graph and is applicable to many systems in materials science and other areas. In addition to modeling completed electronic pathways set up by conducting nanoparticles in an insulating matrix, it can also be used to model many other things. The usual example is to consider a porous medium in which a liquid is poured on top, and to consider the probability that a pathway exists for the liquid from the top to the bottom of the porous material sample through the pores in the sample. A similar situation arises in C-NCPs, except the pathways are set up by completed electronic pathways between nanoparticles, and the "liquid" is electrons.

For C-NCPs, percolation threshold p_c is mathematically defined as a filler volume fraction at which an infinite spanning cluster appears in an infinite system.[2] If the fill factor p is increased above this point, that is, $p > p_c$, the probability of finding a spanning cluster extending from one side to the other side is 1. For volume fractions $p < p_c$, the probability is 0. In addition to volume percent, weight percent can be used to express percolation threshold.

For conductive nanocomposite polymers, this translates to a dramatic drop in resistivity if the fill factor is increased above the percolation threshold, because of probabilistic conductive pathways being set up in the insulating matrix. Conductivity tapers off with further increase in fill factor, giving rise to the typical S-shaped curve shown in Fig. 8.1. The amount of conductive filler required to reach the

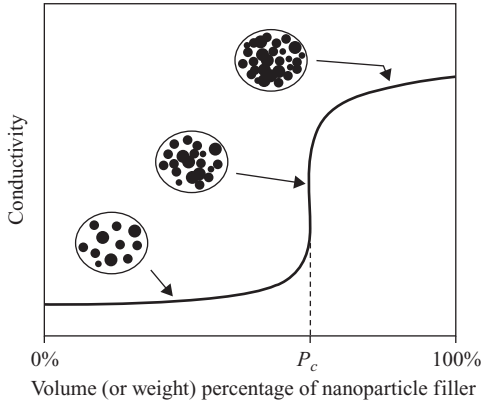


Figure 8.1 Typical "S-shaped" graph for conductivity versus volume (or weight) percentage of nanoparticle filler in polymer matrix for conductive nanocomposite polymer. The percolation threshold (p_c) is labeled.

percolation threshold is dependent on many factors, including size and shape of filler nanoparticles, nanoparticle aspect ratio, nanoparticle material conductivity, mixing (dispersal) method, filler distribution and agglomeration tendency of many nanoparticles (especially unfunctionalized nanoparticles), and surface interactions with the polymer matrix material.

Percolation theory was historically derived using spherical particle models. However, *aspect ratio* (ratio of length to diameter of nanoparticle) seems to play a central role in percolation threshold determination. The small size and large aspect ratio of many nanoparticles, such as *carbon nanotubes* (CNTs) and silver rods, are generally helpful in lowering the percolation threshold. For example, CNTs may have aspect ratios from 100 to 10,000, and very low percolation thresholds as a result. In addition, percolation threshold generally increases as particle size decreases.[3] However, the degree of convolution and entanglement in very high aspect ratio fibers may play a more complex role[4]: long fibrous shapes significantly complicate predictions, as tubes may bend back on themselves or provide other geometric challenges. Research activity is ongoing to model and experimentally determine C-NCP behavior accounting for other effects, such as agglomeration caused by attraction of nanoparticles during mixing and thermal effects.[5]

8.3 Nanoparticle Shapes and Materials

Nanoparticles come in a wide variety of materials, shapes, and sizes. From simple silver flakes and amorphous carbon black, to highly tailored metal and carbon nanorods and nanotubes with controllable sizes, shapes, and numbers of cylindrical walls, nanoparticles are available in an ever-increasing variety. As new nanoparticles come along, so do new ways of utilizing their often unique properties and embedding them in an ever-growing number of polymer base materials. This section begins with a few basic shape definitions, then proceeds to describe a few various nanoparticles that have been primarily used for NCPs, especially C-NCPs, although it should be noted that micropatternability of many of the C-NCPs has not been demonstrated.

8.3.1 Nanoparticle Shapes

Nanoparticles commonly used as fillers in polymers come in many different shapes and sizes. Common nanoparticle shapes include spherical, flake, rods or cylinders, fibers, and random assortments that may contain all of these shapes. These shapes can play a role in the percolation threshold, ability to uniformly mix particles, and mechanical changes (e.g., Young's modulus) to the polymer matrix, in addition to

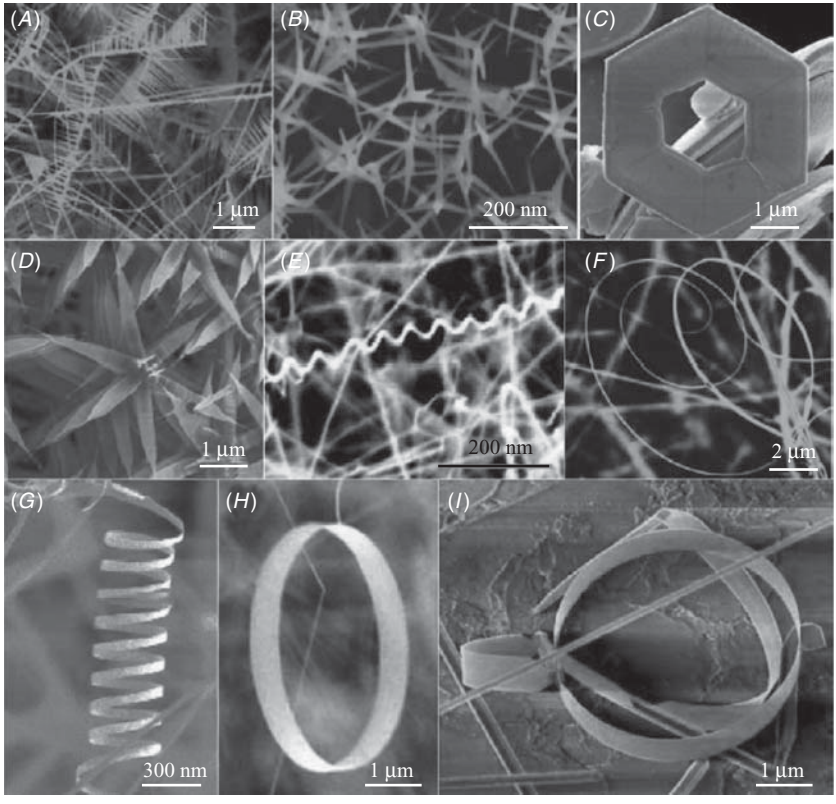


Figure 8.2 A wide variety of shapes of nanoparticle fillers are available, with more discovered all the time. These particle nanoparticles are all ZnO, but are of a wide variety of different shapes.[6]

conductivity changes imparted by the nanoparticles' conductivity. As noted in Section 8.2, aspect ratio (length to width ratio) is thought to play a large role in percolation threshold, as it seems that conductive percolation paths are, in general, more easily set up between long and thin nanoparticles. Nanoparticles are available in an ever-increasing variety of shapes (see Fig. 8.2),[6] which complicates their use as fillers and the ultimate behavior of the NCP.

8.3.2 Metal-Based Nanoparticles

Many different metals have been used as nanoparticle fillers in a variety of shapes and sizes. Metals include silver, gold, aluminum, nickel, copper, and platinum and include flakes, rods, spheres, and random assortments that may contain all of these shapes. These nanoparticles are generally commercially available in sizes ranging from 3 nm to

500 nm and with a purity of greater than 99.5% (in some cases 99.9%), where purity of a given sample of nanoparticles gives an indication of the level of contaminants, that is, materials other than that specified (100% minus the purity).

The most common metal nanoparticles for micropatternable electrically conducting nanocomposite polymers are silver, with gold being perhaps the next most common. Silver offers a very low electrical resistivity (1.617×10^{-8} Ω-m at 298 K) in its pure form and is less expensive than gold. There have been a number of recent efforts to manufacture and synthesize silver nanorods[7,8] and nanotubes[9] with high aspect ratio as compared to other silver nanoparticles such as flakes or spheres. Silver powder (average diameter 2–3 μm) and gold nanoparticles (average diameter 5–10 nm) have been utilized for C-NCP,[10,11] as well as 13-nm gold nanoparticles[12] and gold nanorods (length of 61.6 nm ± 6.3 nm and diameter of 13.9 nm ± 2.6 nm).[13]

Among all other metallic nanoparticles, platinum has generated interest due to its common employment as an electrode material in biomedicine and chemistry. Efforts are being made to develop platinum nanorods that can be used to develop electrically conducting micropatternable polymers.[14,15] These nanorods have an average diameter of 3 to 4 nm and are 20 to 60 nm long. Copper nanowires (diameter 25 nm and length 2 μm) and aluminum (average diameter 102 nm)[16] have also been demonstrated specifically for C-NCP.

8.3.3 Carbon-Based Nanoparticles

Carbon has been extensively explored as a filler for C-NCPs. Early work involved the utilization of carbon black to make conductive polymers for employment as electrodes or sensors, or for improved polymer mechanical properties. In 1991, Iijima discovered a new shape for carbon: the *carbon nanotube* (CNT).[17] Since this discovery, there has been increasing activity surrounding C-NCPs using this remarkable new material.

Carbon black is a material produced by the incomplete combustion of heavy petroleum products. Carbon black is a form of amorphous carbon that has a high ratio of surface area to volume, although its ratio is low compared to those of activated carbon and carbon nanotubes. Carbon black is primarily used as a reinforcing filler in rubber products, especially tires. However, carbon black is very inexpensive compared to other nanoparticles that have greater purity and are produced using more controlled methods, and it has been around for decades; it was one of the first nanoparticles used for C-NCP.

Carbon nanotubes have exceptional electrical, mechanical, electrochemical, chemical, thermal, and thermo electric properties.[18] Carbon nanotubes have high strength, stiffness, high electrical and thermal conductivity, low density, and high aspect ratio that can be tailored

to some degree. Many potential applications have been proposed that exploit these extraordinary properties, such as nanoelectronics, chemical and physical sensors, biosensors, actuators, composites, integrated circuit manufacturing, and scanning probes.[19] CNTs can have high aspect ratio, high conductivity, and an added advantage of generally achieving percolation at lower concentration than spherical fillers, which makes them an excellent choice for electrically conducting NCPs.

CNTs can be generally classified as *single-walled* carbon nanotubes (SWCNTs) and *multiwalled* carbon nanotubes (MWCNTs). Conceptually, a SWCNT can be formed by rolling a graphene sheet (hexagonal structure) into a cylinder and a MWCNT is composed of concentric graphene cylinders with an interlayer spacing of 0.34 nm.[20] Like many nanoparticles, CNT properties are highly dependent on structure, size, aspect ratio, and morphology. They are also dependent on atomic structure and can be made semiconducting or highly conducting depending on chirality,[20] making them very useful for electronic applications, even though purity of chirality may be difficult to achieve. In addition, CNT resistance changes as a function of mechanical deformation, rendering them useful as a sensor material and in NEMS.[21] Furthermore, CNTs can be actuated via application of an electric field in a phenomena that resembles the piezoelectric effect, although the mechanism is quite different.[22]

Exploitation of CNTs for their unique properties is an intense area of nanotechnology research. Research in CNT-based C-NCPs seek to embed CNTs in a polymer matrix in order to impart one or more of the unique characteristics of CNTs to the polymer, while the polymer matrix retains its own desirable characteristics, such as ease of micropatterning, flexibility, and low cost. Carbon has been utilized as a nanoparticle in C-NCPs more often than any other material, with perhaps the exception of silver, and has been embedded in many different polymer matrices, which are covered in Section 8.4.

One problem with CNTs is that they are extremely difficult to get in either purely metallic (conductive) or semiconducting form and, if available, are usually very expensive. Thus, 40% conducting and 60% semiconducting CNTs are typically used in our laboratory, which is a much higher percentage of metallic than those typically desired by nanoelectronics researchers.

8.3.4 Other Nanoparticle Materials

Other nanoparticle materials are used primarily for reasons other than to provide conductivity and are discussed briefly only to help put C-NCPs in context. Although many researchers have focused on utilizing nanoparticles to make polymers conductive, another area of intense research has focused on the realization of high-k dielectrics

for on-chip and *printed wire board* (PWB)-level low-area capacitors. This can be achieved by doping polymers with ceramic nanoparticles such as barium titanate and silica. The target k is usually 50 to 200 (see Ref. 23) for applications such as organic *field-effect transistors* (FETs). Various nanoparticles have been used to render a polymer magnetic (e.g., Refs. 24–26) or improve its mechanical characteristics, sometimes with an effect on conductivity. Specialized applications also exist in which more exotic nanoparticles are used, such as expandable spheres for actuation[27] or quantum dots.[28]

8.4 Conductive Nanocomposite Polymers for Microsystems: Preparation and Micropatterning

Polymeric materials are usually nonconductive, with extremely low electrical conductivity on the order of 10^{-10} to 10^{-15} S/m. Dispersing conductive materials into the polymer matrix can form conductive composites, provided a few conditions are met as previously discussed in Section 8.2.

A wide variety of polymer materials exist, a subset of which have been utilized for C-NCPs, and a smaller subset for micropatternable C-NCPs. Although many classification methods and characterizations for polymer materials exist, a few definitions help in the understanding of the differences between commonly used C-NCP based materials. A *thermosetting polymer* is one that irreversibly cures, generally after it has been poured in a precured state into a mold master. The curing process transforms the resin into a plastic or elastomer by a crosslinking process. Energy (e.g., heat; hence, *thermo*set) and/or catalysts are added that cause the molecular chains to react at chemically active sites and crosslinking to occur. The crosslinking process forms a molecule with a larger molecular weight that is solid. A *thermoplastic* is a polymer that turns to a liquid when heated and freezes to a very glassy state when cooled. Most thermoplastics are high-molecular-weight polymers. Unlike thermosetting polymers, thermoplastic polymers can be remelted and remolded, usually using an embossing, or stamping, process under heat. For reviews of micropatterning processes associated with undoped thermosetting and thermoplastic polymers, please see Ref. 29.

The method and uniformity of nanoparticle dispersion can have a huge impact on the characteristics of the final C-NCP material. Nanoparticle dispersion in polymers can be classified into two main categories: physical dispersion and chemical dispersion. Physical dispersion involves physically separating agglomerates of nanoparticles, nanorods, or bundles of CNTs that are tied up or clumped up together by van der Waals forces,[30] whereas chemical methods involve manipulating the surface chemistry of the nanoparticles.

Three main physical dispersion mechanisms are commonly used: ultrasonic (or sonic) agitation, shear mixing, and ball milling.[31] The most popular technique is ultrasonic agitation, in which the nanoparticles are first manually stirred in a solvent and then exposed to ultrasonic waves/irradiation. There are two different types of ultrasonic waves that can be used. The first is low-frequency ultrasonic (~20–24 kHz) in which the composite is placed in an ultrasonic bath and is agitated for a specified time. The second involves using higher frequency ultrasonic waves (~42–50 kHz), in which an ultrasonic probe is immersed into the mixed composite. The probe is usually operated in pulse mode (e.g., cycles of 10 seconds on followed by 15 seconds off), which provides mixing by repeatedly allowing the sample to settle back under the probe after each burst and minimizes heating of the sample, which can be especially problematic if the polymer is a thermoset because premature curing may occur. Another problem is that the shock waves generated by ultrasonic pulses lead to collisions between nanoparticles. Consequently, the agglomerated nanoparticles may be eroded and split by the collisions.[32,33] For example, it has been observed that prolonged exposure to ultrasonics can damage CNTs. However, ultrasonic dispersion is still the preferred physical method because it is quick and easy to use, the dispersion is good as compared to other physical methods, and low-frequency ultrasonics seem to minimize damage to fragile nanoparticles. The second physical method, shear mixing, is often employed for viscous monomers/polymers and photoresists. Nanoparticle aggregates are forced apart by high speed shear mixing, often using a magnetic stirrer at speeds reaching 1,000 to 5,000 RPM. The viscosity of the solvent/polymer matrix does not allow the nanoparticles to reaggregate.[34] One potential drawback is that a magnetic stirrer cannot be used with magnetic materials such as nickel or iron. Ball milling is another physical technique that consists of a rotary cylinder along with iron or plastic balls to break the clumps of carbon nanotubes. However, it still may break the carbon nanotubes.[35] The related technique of bead milling uses small balls (micrometers in diameter) to disperse nanoparticles[36] to minimize breakage.

Chemical dispersion methods involve manipulating the surface chemistry of the nanoparticles and come in two basic varieties: covalent and noncovalent methods. Covalent methods consist of functionalizing the surface of nanoparticles (e.g., with –OH or –COOH groups for CNTs). Noncovalent methods make use of surfactants that attach to the nanoparticles and prevent them from aggregating. Functionalization of CNTs and other nanoparticles is still a heavily researched topic, because chemical dispersion methods are highly promising and very gentle methods of uniform dispersion compared to physical methods.

SWCNTs are particularly problematic to uniformly disperse in that they are generally insoluble in common solvents and polymers

and difficult to chemically functionalize without altering the CNT properties.[37] Lengthy sonication (in which care must be taken not to damage the SWCNTs), in situ polymerization in the presence of SWCNTs, and special functionalization techniques can be used to alleviate dispersion problems.

The next sections detail various C-NCPs arranged first by base polymer and second by nanoparticle dopant. It should be noted that the references and materials that are addressed are not necessarily an exhaustive list, but are fairly representative of the C-NCP field with particular emphasis on microsystems and micropatternability, although not all materials listed have been micropatterned.

8.4.1 Epoxies and Photopatternable SU-8

Epoxies have been utilized by the microelectronics industry as adhesives for decades and are the primary resins used in overmolding integrated circuits, transistors, and hybrid circuits; in making printed circuit boards; and as a conductive adhesive or conductive polymer for flip-chip interconnect. An epoxy is a thermosetting polymer formed from reaction of an epoxide "resin" with polyamine "hardener." Most common epoxy resins are produced from a reaction between epichlorohydrin and bisphenol-A, or similar. Most epoxies cure at room temperature, although heat may speed curing time.

SU-8 is an epoxy-based negative-tone near-UV photoresist that was originally developed by IBM.[38] A photoresist is called negative when the areas exposed to certain wavelengths of light are crosslinked because of energy imparted by the light and thus remain on the substrate during development while the unexposed (uncrosslinked) areas are developed away. SU-8 is sensitive to wavelengths below 400 nm and will absorb light at wavelengths shorter than 360 nm.[39] Exposure to near-UV light causes a photo acid generator in the SU-8 formulation to become a strong acid, which catalyzes the thermal crosslinking of SU-8. The manufacturer of SU-8, Microchem Corporation,[39] distributes many formulations of SU-8, denoted by a numerical suffix ranging from 2 to 100, which denotes the estimated thickness of the resulting SU-8 film in micrometers when spun at 3,000 RPM. SU-8 enables fabrication of high-aspect-ratio structures. By choosing the correct SU-8 formulation and controlling the spin speed, various thicknesses of SU-8 can be spun onto the substrate from 2 μm to greater than 200 μm in a single coating.[40] SU-8 consists of EPON Resin SU-8 (Shell Chemical) dissolved in a solvent (GBL, or gammabutyrolacton). The chemical formula for SU-8 is shown in Fig. 8.3.[41] SU-8 has been widely employed in microelectronics, MEMS, and microfluidics as both a structural material (e.g., Ref. 42) and as a master mold for fabricating microstructures in other polymers via soft lithography.[42,43] The possibility of doping SU-8 with nanoparticle fillers to make it conductive is

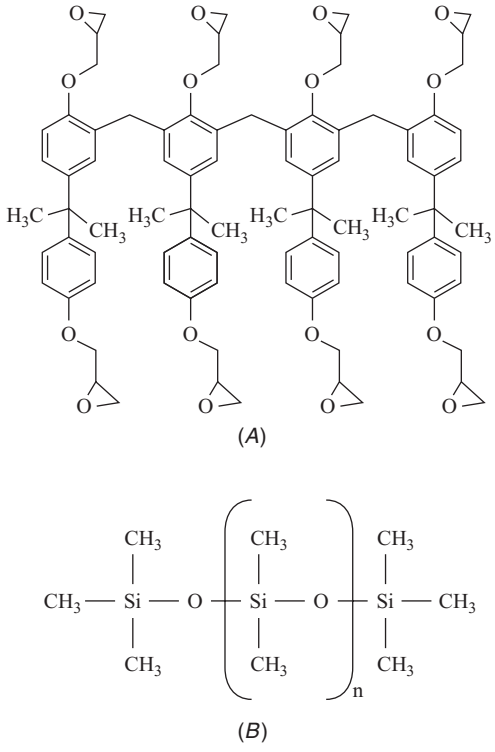


Figure 8.3 Chemical formulas for two of the most common micropatternable polymers: *A*) SU-8 photopatternable epoxy[41]; (*B*) polydimethylsiloxane (PDMS).

of great interest to MEMS and microsystems researchers as many applications in both MEMS and microfluidics require patterned electrical leads to provide for transducers. The general method of providing electrical leads is to deposit and pattern metal leads through either lift-off or masked etching methods. However, the adhesion of metals to polymers (including SU-8) is poor, requiring adhesion-promoting steps prior to metal deposition, such as short periods of plasma etching to alter surface chemistry.[44] Many of these issues could be solved by the introduction of a conductive form of SU-8, which would have better adhesion to nonconducting SU-8 layers through crosslinking at the interface.

Silver and Gold

Conductive epoxies can be made from epoxy adhesives that are doped with micro- or nanoscale particles. For cost and historical reasons, silver has been one of the most popular metallic fillers used. Although originally micron-scale silver flakes were employed,[45] silver

nanoparticles have been widely used in nonphotopatternable epoxies and adhesives for years in the electronics packaging industry.[23] The embedding of silver either results directly in improved adhesive conductivity, or provides additional bridging during subsequent sintering. Filler size has a large effect of percolation threshold,[45–47] with typical filler sizes ranging from 20 to 1,000 nm, with spherical, mixed size, and fibrous shapes also reported.[46] Typical fill factors that result in conductivity have a large range depending on particle size and structure, from <10% to more than 50%. Such epoxies are typically prepared by simple stirring or sonication. Micropatterning is generally not the aim of such materials and is thus not addressed by most researchers.

Photosensitive micropatternable SU-8-silver nanocomposites have also been demonstrated. Researchers have developed a silver and SU-8 composite using silver powder with a mean particle dimension of 1.5 μm.[48,49] They were able to make SU-8 highly conductive, but at the cost of its rheological and optical properties. Silver nanoparticles were added to the SU-8 resin together with a solvent to control (lower) viscosity and powder sedimentation. Unfortunately, their composite could not be applied to the substrate using conventional SU-8 spinning and required a scraper process for deposition and lost most of its patterning ability due to agglomeration of the powder causing shadowing of the resist below the particles. However, lines down to 5 μm could be patterned.[49] Polymerized thickness was demonstrated to drop off sharply with silver volume fraction below 20%, although this could be somewhat compensated for by an increase in UV-light dosage energy. Percolation thresholds as low as 6 vol% were reported.

In addition to silver, SU-8 and gold have been combined for a C-NCP.[41] The gold was either 100- to 300-nm powder, or 5-nm gold in colloidal suspension. Gold, benzene, and SU-8 were mixed, with a practical 14 vol% percolation threshold that still allowed spinning and photopatterning. Higher filling fractions using gold powder were also demonstrated. Stress-strain curves were also presented, although large variation existed between samples.

Nickel and other ferromagnetic metal nanoparticles have reportedly been mixed with SU-8, although primarily for magnetic actuation purposes rather than conductivity. The interested reader is referred to Ref. 25.

Carbon Nanoparticles

CNTs have also been utilized with epoxy-based conductive adhesives for electrical contact, for example, as high-frequency conductors in electromagnetic shielding.[23] Similarly to silver, MW- and SWCNTs have been embedded in epoxies not intended for micropatterning applications. Simple mixing, sonication, ball milling, and shear mixing using high-speed (2,000 RPM) mixers have all been utilized for

nanoparticle dispersion. Very small percolation thresholds have been reported for MWCNTs (<0.005 wt%) and SWCNTs (0.05–0.23 wt%) with diameters below 2 μm and lengths up to several millimeters.[50] For SWCNTs, a pretreatment was required to avoid agglomeration (ethanol solution saturated with sodium hydroxide). The samples were cast against an aluminum mold. Another SWCNT-epoxy C-NCP[51] also showed a very low percolation threshold ($<10^{-4}$ wt%). The composite was mixed using sonication, and purified SWCNTs were used that had average length of 516 $\pm$ 286 nm and average diameter of 1.35 $\pm$ 0.15 nm, and were dispersed in *N*,*N*-dimethylformamide (DMF) prior to slowly being added to epoxy resin. Percolation thresholds of 0.0025 wt% for MWCNTs have also been reported.[5] For these materials, shear mixing at 2,000 RPM was utilized to disperse MWCNTs with average diameter of approximately 50 nm and lengths of 17 $\pm$ 3 μm in epoxy resin. For these C-NCPs, conductivities of 1 to 10 Ω-cm were achieved.

Carbon black and CNTs have also been successfully mixed with photopatternable SU-8 by a number of researchers. Percolations thresholds of 0.6 wt% have been reported for carbon black,[52] although fairly rough structures were produced. Films were spun onto silicon substrates and patterned using UV light with a mask aligner. Film adhesion was improved using an oxygen-helium plasma prior to spinning. Electrical resistivity of approximately 1 Ω-cm was achieved. Others have achieved percolation thresholds of 1 to 2 vol% with carbon black nanoparticles.[53] Other researchers have mixed CNTs with SU-8 mainly for reasons of mechanical performance, but have not performed a thorough exploration of their conductivity (e.g., percolation threshold) (see Refs. 41 and 54, with Ref. 41 quoting resistances of approximately 35 MΩ for 5 wt% and 500–600 MΩ for 1 wt% SWCNT in SU-8 microstructures).

Other Materials

Another common nonmetallic and non-carbon-based nanomaterial mixed with SU-8 is silica[55,56] to create photopatternable epoxies with, for example, improved optical performance for waveguides and improved mechanical performance such as wear resistance. An exotic SU-8 based nanocomposite includes quantum dots embedded in SU-8 (see Ref. 28) that can be patterned using two-photon polymerization into complex three-dimensional shapes. However, conductivity is not the aim of these NCPs.

8.4.2 Elastomers, Including PDMS

Elastomers are polymers with the property of elasticity, which means that they deform reversibly under stress. Each of the monomers that link to form the polymer is usually made of carbon, hydrogen, oxygen,

and/or silicon. Elastomers are usually thermosets (requiring vulcanization, or curing) but may also be thermoplastic.

Silicones are largely inert, man-made thermosetting polymers based on silicon together with carbon, hydrogen, oxygen, and sometimes other chemical elements, and have widespread use in every day life. One particular form of silicone, polydimethylsiloxane (PDMS, whose chemical formula is shown in Fig. 8.3*B*), is a nonconductive silicone-based elastomer that has been under special focus in microsystems research for more than a decade for its flexibility and ease of micromolding for rapid prototyping of microdevices and systems. PDMS has played an important role in *lab-on-a-chip* (LOC) systems, serving as an important material in chip fabrication because of its properties such as transparency, biocompatibility, and good flexibility. Many microfluidic devices have been fabricated by micromolding PDMS including micromixers, microchannels, valves, pumps, and interconnect structures for a wide variety of applications for LOC analysis. However, the addition of electronic functionality to PDMS-based microfluidic systems has lagged behind, because it has proven difficult to integrate, embed, or pattern conducting lines on PDMS because of the weak adhesion between PDMS and metals and other conducting polymers. The integration of conductive tracks or structures in bulk PDMS is extremely important for signal routing and interfacing to signal-processing electronics, and to power active devices. Potential applications include electrokinetic micropumps, microsensors, microheaters, and microelectrodes. There is a great need for flexible, conducting PDMS that can be micromolded and integrated with PDMS-based LOC systems to provide electronic functionality.

One of the major problems encountered is dispersion of conductive particles in PDMS. It is especially very difficult to disperse CNTs in a PDMS matrix. One way to overcome this is to dilute the PDMS elastomer in an organic solvent such as heptane or toluene and then ultrasonicate the desired quantity of carbon filler. Functionalized carbon nanotubes (e.g., with —OH or —COOH) are preferable as dispersion is less problematic because of surface interrelations.[57] Dispersion of metallic fillers such as silver, aluminum, copper, and gold also benefits from dilution of PDMS, to which can be added the desired quantity of fillers followed by ultrasonicating the mixture. In the SFU Microinstrumentation Laboratory, we have observed that nanoparticles are easier to disperse and cover more surface area than micron-sized particles. Hence, a lesser quantity (by weight) of metallic filler can render PDMS conductive (lower percolation threshold) and it maintains its self-leveling properties.

The usual microfabrication process used for PDMS microstructures is micromolding, in a process called soft lithography,[43] where the polymer is cured at room temperature or elevated heat (hot plate) against a suitable master, usually micropatterned silicon or SU-8.

UV-light patternable PDMS formulations exist (e.g., Ref. 10), although their patterning usually results in sidewalls with a fairly large slope.

In addition to thermosets, thermoplastic elastomers based on polystyrene, polyurethane, and polystyrene/polypropylene copolymer have also been utilized for highly flexible C-NCP.

Silver and Other Metallics

Silicone-based nanocomposites doped with silver have been explored for percolation threshold as early as 1992, although generally with somewhat larger particles than nanoscale (0.5–35+ μm) and not with a specific aim toward microelectronics and microsystems applications or micropatterning.[58] In 2007, Niu et al.[59] demonstrated micromolding of a silver-PDMS C-NCP using silver particles of 1 to 2 μm in diameter. A conductivity of 102 $(\Omega\text{-m})^{-1}$ was achieved at 86 wt% of silver in a PDMS matrix. They reported that at high weight percentages of silver, PDMS lost its self-leveling properties, resulting in polymers that formed like clay, thus requiring a plastering method of patterning as opposed to spin-coating.

In 2008, Cong and Pan[10] developed conductive photopatternable PDMS nanocomposites that provide both high electrical conductivity and photopatternability. These photosensitive composite materials, which consist of a photosensitive component, a conductive filler (1–2 μm silver or carbon, the latter covered in the next section), and a PDMS pre-polymer curing agent, can be used as a negative photoresist or a positive photoresist by addition of *2,2-dimethoxy-2-phenyl acetophenone* (DMAP) and benzophenone as photoinitiators, respectively. For the silver-filled nanocomposites, percolation occurred around 18 vol%. At high concentrations of silver powder (20 vol%), the nanocomposites became highly viscous and the researchers were unable to obtain a uniform coating over the substrate surface. The photosensitive silver-PDMS nanocomposite was sensitive only to light below 365 nm and could be photopatterned with features 65 μm to several millimeters in layers 10 to 150 μm thick.

Silver nanoparticles were also used to dope a polystyrene/polypropylene copolymer.[3] Percolation thresholds of 13 to 16 vol% were achieved (with 0.2 Ω-cm resistivity) with 100-nm particles. The polymer matrix was styrene-ethylene-propylene-styrene block-copolymer compound (SEPS), which was melted and mixed with silver, then compression molded (embossed). A batch mixer was used to physically disperse the nanoparticles.

A polyurethane-based C-NCP filled with platinum has been demonstrated[60] with a percolation threshold of approximately 6.5 vol% for 50%-50% water-methanol reduced platinum salt samples, resulting in conductivities up to 2.2 Ω/square at 15 vol%. The C-NCP could be microfabricated by photopatterning, with a fairly large minimum feature size of 350 μm.

Polystyrene-based C-NCPs have been demonstrated using copper nanowires,[61] with functionalized (1-octanethiol, $C_8H_{17}SH$) and nonfunctionalized copper nanowires having 0.25 vol% and 0.5 vol% percolation thresholds, respectively. The functionalization was employed to prevent agglomeration and improve nanoparticle dispersion. The copper nanowires were 25 nm in diameter and 1.78 μm in average length. The nanowires were dispersed in 1.2% thermoplastic polystyrene resin in suspension in an ultrasonic bath and ultrasonicated. The suspension was cast in an evaporation dish and solvent evaporated under heat.

Carbon Black

Conductive PDMS has been demonstrated by the addition of a fine carbon black at 10% or higher concentration by weight[62] to PDMS. It was observed that electrical conductivity increased with carbon black concentration from 5.6×10^{-14} to $\sim 5 \times 10^{-1}$ $(\Omega\text{-m})^{-1}$. This work was improved in 2002,[63] where the electric conductivity was shown to increase from 10^{-6} to 10^{-1} $(\Omega\text{-m})^{-1}$ when less than 3% carbon black aggregates were dispersed into PDMS. In addition to silver, PDMS has also been doped with 40- to 100-nm carbon black with conductivity onset at about 10 wt% carbon black.[59] In that research, carbon black was easily dispersed in PDMS through mixing and micromolded against thick photoresist (AZ4620) masters up to 20 μm thick, yielding microstructures approximately 10 μm wide. Another micromoldable carbon black-PDMS C-NCP is utilized for microfingerprint sensors[64] and was fabricated with 20 wt% carbon black to very small feature sizes (50 μm $\times$ 30 μm $\times$ 8 μm).

Other researchers have worked with polypropylene/polyurethane thermoplastic elastomer mixtures enhanced with carbon black, using standard melt-mixing.[65] Resistivities down to 100 Ω-cm were obtained.

The useful operating range of conductivity should be greater than 10^{-1} $(\Omega\text{-m})^{-1}$ for carbon to be useful for most sensor-related applications.[66] The levels of conductivity obtained is highly dependent on type of carbon black used, the particle size, and how well it is dispersed in the polymer matrix.

Carbon Nanotubes

The conductivity levels offered by carbon black PDMS composite are inferior to those of CNTs and are generally not sufficient for sensor or signal routing in LOC systems. However, functionalized CNTs have shown more promising results.

MWCNT-PDMS samples with conductivity that is highly dependent on the CNT concentration have been developed, with a percolation threshold of 4 wt%.[66] The MWCNTs were 1 to 2 μm in length and 40 to 60 nm in diameter and were sonicated in chloroform and

mixed with PDMS solution, sonicated further, degassed in a vacuum chamber, and cured against a macroscale-sized mold (4 cm × 1 cm × 1 cm) overnight. Other researchers have performed microfabrication of pressure sensor strain gauge arrays of MWCNT-PDMS nanocomposites in undoped PDMS, using 10 wt% MWCNTs.[67] Yet another MWCNT-PDMS C-NCP was demonstrated with a sheet resistance as low as 50 Ω/square, and a percolation threshold of 2 wt%.[68] Microfabricated structures were fabricated in the material via micromolding.

In the Microinstrumentation Laboratory at SFU, we have achieved a percolation threshold at 0.8 wt% of MWCNT in a PDMS matrix.[69] We use a prolonged ultrasonic agitation (3 hours) at low frequencies (24 kHz) to minimize CNT damage in the viscous PDMS, followed by 20 minutes of manual stirring. After this step, the crosslinking agent is added and manually mixed and ultrasonically agitated for 20 minutes. The size of CNTs had a very high aspect ratio: 60 to 100 nm in diameter and 5 to 15 μm in length. We have utilized this to micromold a wide range of structures intended for microelectrode arrays, microelectronic routing, and chip-to-chip interconnect.

Since then, an embedded microfabricated strain gauge sensor array via microcontact printing has been demonstrated.[70] Toluene was used to aid in dispersion of CNTs in PDMS that was magnetically stirred. The contact printing employed a PMMA stamp that applied spin-coated C-NCP (approximately 50 μm thick) to the stamp for transferral to a bulk undoped PDMS substrate via microcontact printing. Lines approximately 40 μm thick, 10 mm long, and 200 μm wide with 400-μm gaps were thus printed. The percolation threshold was approximately 6 to 12 wt%.

Aspect ratio has been examined for MWCNTs in VMQ.[4] VMQ is a silicone rubber having methyl and vinyl substitutions on the polymer chain, and it differs from PDMS, where only methyl groups are included. Surprisingly, longer aspect ratios demonstrated higher percolation threshold. The authors speculate that perhaps the greater convolution and entanglement of their higher-aspect-ratio fibers (500:1 length:width ratio MWCNTs) may have prevented percolation, as compared to their 50:1 aspect ratio MWCNTs, although this was not explored in detail. Still, percolation thresholds below 1 wt% were achieved with conductivities comparable to those found by other researchers.

Polyurethane thermosetting elastomer has also been employed for a MWCNT C-NCP.[68] These results were not as good as those already discussed for PDMS from the same publication, resulting in a percolation threshold around 10 wt% and worse conductivity results. Although many polystyrene C-NCPs have also been reported,[61] very low percolation thresholds using SWCNTs (0.05 wt%) and MWCNTs (0.014 wt%) have been demonstrated by Curran et al.,[71] with conductivities up to 33 S/m.

Other Nanoparticles

Other nanoparticles have been mixed with PDMS with different purposes besides conduction. These include expandable microspheres for actuation[27] and magnetic actuation,[72] along with many other topics of research for specialized materials.

8.4.3 Other Polymers

Many other polymers have been investigated for C-NCP and microfabrication of C-NCP. A few representative materials and associated research are presented here.

Various thermoplastic polymers (often epoxy-based) have been utilized for many years in the microelectronics industry for flip-chip applications. For these applications, the thermoplastic polymer is heated, and flip-chip connections are achieved on cooling. More recently, thermoplastic polymers have been doped with conductive fillers for an improvement in conductivity level (see, e.g., Refs. 73 and 74). In these works, silver flake particles are most often employed, and patterning is accomplished via C-NCP filling around other sacrificial micromachined polymers.

In addition to CNT-doped polystyrene, Ramasubramaniam and Chen[37] also investigated CNT-doped polycarbonate. By functionalizing the SWCNT with poly(phenyleneethynylene)s (PPEs), the researchers were able to uniformly disperse the CNTs easily without damage via sonication. The polycarbonate-based C-NCPs had higher conductivities than polystyrene for the same SWCNT loading, with conductivities of 480 S/m at 7 wt% of functionalized SWCNTs, and percolation thresholds at 0.11 wt%.

PMMA and other acrylate-based polymers have been investigated. C-NCPs have been demonstrated using the following fillers: carbon black,[75] CNTs,[76–78] and various metallic fillers such as gold and silver.[49] Metallic fillers have included silver nanospheres and needles 1 μm $\times$ 30 in size, in percentages of 8 to 40 vol%, and gold nanospheres 0.1 to 5 μm in size.[49] A UV-curable carbon black/acrylic resin C-NCP was developed by mixing acrylic monomer, acrylate-functionalized oligomer, a photoinitiator, and carbon black filler.[75] Various carbon powders (graphites and acetylene black) were employed and mixed via ultrasonication with the polymer resin and other materials in a dark room to prevent premature curing. Crosslinking was accomplished via UV light, into 36 μm-thick-films and 2-mm-thick plates. Results showed conductivities up to 600 mS/cm for acetylene black at 10 wt%, with a percolation threshold around 1 wt%. Regular carbon black graphite had a much higher percolation threshold (30 wt%). CNTs have also been employed for acrylate-based C-NCP. Purified SWCNTs mixed with PMMA resulted in well-dispersed CNTs using *dimethylformamide* (DMF) solvent in films 30 μm

thick.[78] Conductivities of 0.1 mS/cm were achieved with 2 wt% and higher CNT loading. The researchers also note that unaligned SWCNTs had better conductivity than aligned ones, possibly because percolation paths had trouble forming when the conductors were aligned and not crossing, although this speculation is open to further research. Other groups have demonstrated C-NCP using SWCNTs[76] and functionalized CNTs[77] with UV-curable diacrylate and PMMA, respectively. One of these groups[76] was able to nanoimprint their polymer, which was mixed via sonication and had volume resistivity of less than 100 $(\Omega\text{cm})^{-1}$ for a percolation threshold around 0.1 wt%. Printing was accomplished using a PDMS stamp. Only resistivity changes were monitored by Yoon et al.,[77] as they were able to utilize their material as a vapor sensor as discussed under applications in Section 8.5.

Polyethylene-based C-NCP include materials doped with carbon black intended for gas sensing[79] and those doped with MWCNT and prepared by melt-blending through an extruder.[80] For the carbon black filled polymer, 20 wt% carbon black was utilized and mixed via stirring. The resistivity was still too high, so a grafting of carbon black to the surface was performed before testing as a vapor sensor. For the MWCNT work, the percolation threshold was about 7.5 wt% with 5 Ω-cm resistivity achieved using 10- to 30-nm diameter, 1- to 10-μm length carbon nanotubes at greater than 85% purity.

Polyimide and MWCNTs can be mixed with *N*,*N*-dimethylacetamide (DMAc) to uniformly disperse the 20- to 40-nm diameter, 5- to 15-μm length MWCNTs of 95 to 98% purity in polyimide via stirring.[81] Curing resulted in polyimide films 10 to 30 μm thick. The percolation threshold was around 1 wt%, yielding resistivities down to below 0.5 Ω-cm. The C-NCP was microfabricated as a pressure sensor utilizing a photopatterned nondoped SU-8 chamber filled with the C-NCP material (Fig. 8.4) via the damascene process, which simply means filling the chamber and wiping off any excess before topping it with an SU-8 membrane.

Conductive polymers have been directly filled with nanoparticles for conductivity improvements. For example, a polypyrrole-MWCNT nanocomposite (PPy-MWCNT) has been developed primarily for use as a micropatterned conductimetric glucose sensor (see Section 8.5)[82] with improved conductivity and sensitivity over PPy alone. Patterning was accomplished via electropolymerization on electrodes of the simply mixed nanocomposite material.

Other polymer materials that have been investigated as nanocomposite polymers include nematic elastomers and CNTs[83] and hydrogels with CNTs,[84] both with the intended purpose of actuation. In the latter case, the C-NCP could be micromolded against a silicone master. CNTs mixed with the hydrogel consisted of *poly(vinyl alcohol)* (PVA)

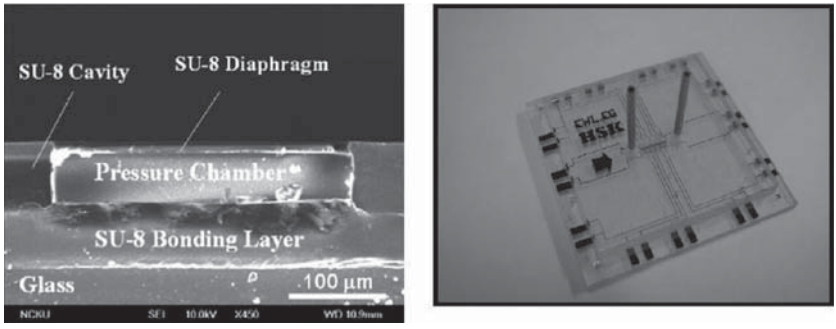


Figure 8.4 Pressure sensor made of undoped SU-8 diaphragm and membrane filled with carbon black filled polyimide C-NCP: (*A*) cross-sectional view; (*B*) completed sensor.

and *polyallylamine* (PPA), with 0.8 mL of 10% aqueous PVA, 0.2 mL of 10% aqueous PPA, and 1 mL of carbon nanotubes sonicated into the mixture at various weight percentages (2%, 3%, 4%, 5%, 6.6%).

8.4.4 Printable Nanocomposite Polymers

Printing conductive polymers is the fabrication method of choice in the flexible electronics industry for applications such as organic transistors, solar cells, and electronic paper. Most of the time, conductive polymers such as polypyrrole, rather than nanoparticle-based nanocomposites, are printed. Alternatively, nanoparticles, CNTs, or nanoparticle colloids are printed directly, rather than C-NCP where the nanoparticles have been evenly distributed in a permanent polymer matrix.[85–87] However, printing of C-NCP has been demonstrated, of which a few examples are given here. As outlined in the pervious sections, an embedded microfabricated strain gauge sensor array via microcontact printing has been demonstrated using a CNT embedded in PDMS.[70] Other researchers[76] were able to nanoimprint their acrylate-SWCNT C-NCP, which had volume resistivity of less than 100 $(\Omega\text{cm})^{-1}$ for a percolation threshold around 0.1 wt%. In addition, other printable NCPs have been developed.[88] These researchers briefly discuss both nonconductive NCP for utilization, for example, in capacitors and inductors, as well as printable C-NCPs, and several other printable NCPs for packaging applications. *Polyaniline* (PANI)-based CNT nanocomposites have been investigated for laser-driven printing[89] with conductivities ranging from 0.001 to 100 S/cm for concentrations of 0.1 wt% to 40 wt%. CdS nanoparticles embedded in polystyrene-based polymer have also been reported using laser-induced printing.[90]

8.5 Applications of Conductive Nanocomposite Polymers in Microsystems

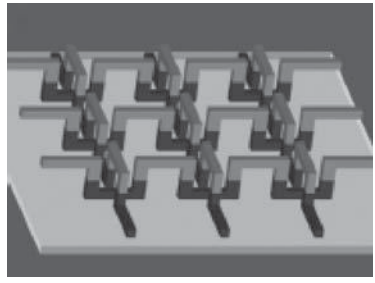
8.5.1 Electronic Packaging, Interconnect, and Electrodes

Composites consisting of highly conductive filler powder dispersed in a flexible polymer matrix have been commonly used in the electronics packaging industry for die attach, solderless connections, and electromagnetic and antistatic shielding.[58] Although originally micron-scale silver flakes were employed, silver nanoparticles have been widely used in nonphotopatternable epoxies and adhesives for years in the electronics packaging industry.[23] The embedding of silver either results directly in improved adhesive conductivity or provides additional bridging during subsequent sintering. Micromachined epoxy bumps embedded with silver flakes have also been used for flip-chip packaging[74] for *micro-optical electromechanical systems* (MOEMSs) whereby photodetectors were integrated with micromachined mirrors and optical waveguides.

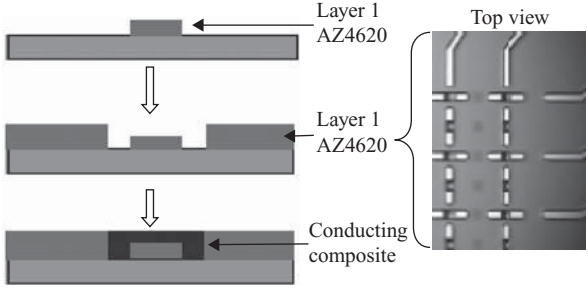
CNTs have also been utilized with epoxy-based conductive adhesives for electrical contact, such as high-frequency conductors in electromagnetic shielding.[23] Furthermore, SU-8 has been doped with carbon black and patterned using x-rays for heat sinks for localized microelectronics and MEMS cooling.[91]

Three-dimensional connection of electrical signals can be an important issue, especially to transfer electrical signals among different layers or even between chips. PDMS has also been doped with carbon black (40–100 nm), silver (1–2 μm), or CNT nanoparticles (60–100 nm diameter, 5–15 μm length) to realize different types of 3D electronic interconnect structures (see Figs. 8.5 and 8.6) for high density level-to-level[59] or chip-to-chip[69] interconnect. Such interconnects rely on both the flexibility and high conductivity of C-NCP.

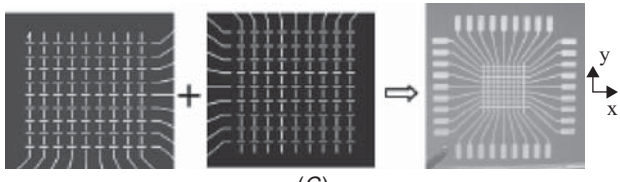
The potential to utilize C-NCP as electrodes is particularly interesting in the realization of flexible lab-on-a-chip systems and flexible microsensors. For example, Jiguet et al.[49] have developed photopatternable electrode arrays in SU-8 and silver C-NCPs (Fig. 8.7). C-NCPs based on carbon black embedded in PDMS have also been employed to realize electrodes for operation of a *giant electrorheological* (GER) valve.[92] *Electrorheological* (ER) fluids are suspensions of nonconducting nano- or microparticles (up to 50 μm in diameter) in an electrically insulating fluid. The apparent viscosity of these fluids changes reversibly by a factor of up to 100,000 in response to an electric field. For example, a typical ER fluid can go from the consistency of a liquid to that of a gel, and back, with response times on the order of milliseconds. For the reported valve,[92] the micropatterned electrodes are C-NCP. These electrodes set up a field that manipulates the ER fluid.



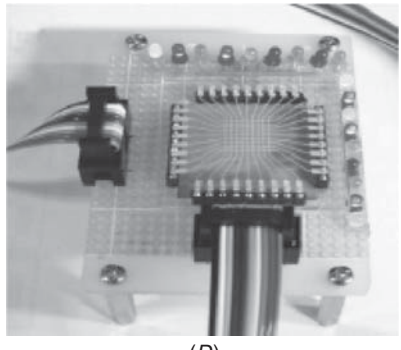
(*A*)



(*B*)



(*C*)



(*D*)

Figure 8.5 Patterning and bonding of multilayers of 3D conductive lines of C-NCP PDMS: (*A*) illustration; (*B*) microfabrication process flow; (*C*) reverse bonding of two halves into one plate with jumped lines; (*D*) testing with LEDs to show functionality of bonded plate with multilevel electronic lines.[59]

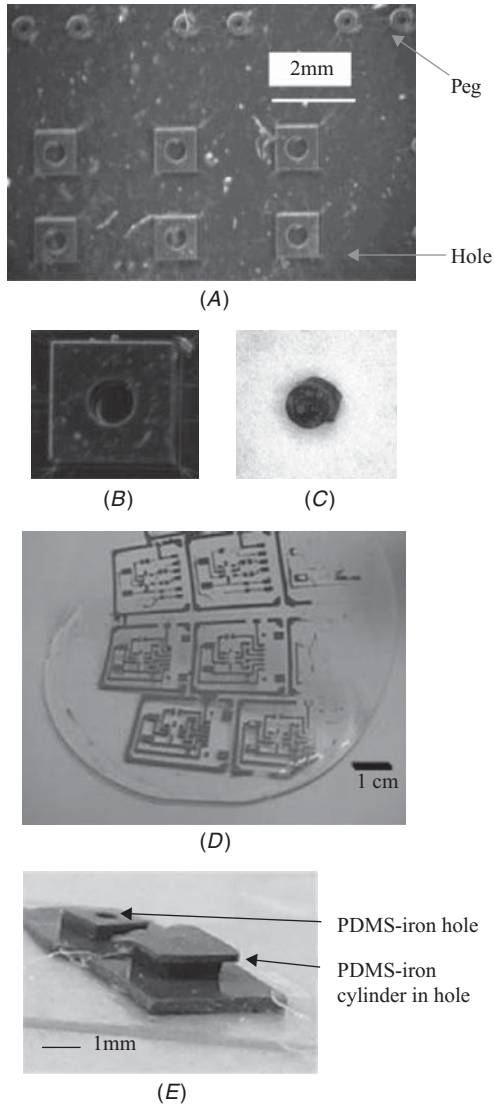


Figure 8.6 Chip-to-chip interconnect structures: (*A–C*) electronic interconnect mating structures in PDMS doped with CNTs[69]; (*D*) electronic routing in conductive PDMS embedded in flexible nonconductive PDMS; (*E*) iron-PDMS structure that can be actuated to facilitate assembly.[72]

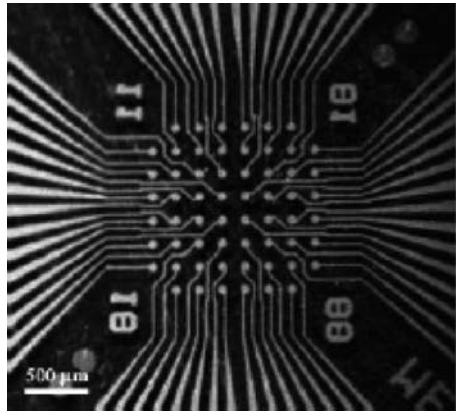


Figure 8.7 Electrodes in silver and SU-8 nanocomposite loaded with 20% silver powder.[49]

The GER effect is able to provide high-pressure changes in a GER control channel to fully close or open a microchannel in proximity using a pressurized thin membrane.

C-NCP have also been utilized for electrodes for chemical sensors, such as for glucose.[82] In this case, a polypyrrole-MWCNT nanocomposite (PPy-MWCNT) was developed primarily for use as a micropatterned conductimetric glucose sensor with improved conductivity and sensitivity over PPy alone. Patterning was accomplished via electropolymerization on electrodes of the simply mixed nanocomposite material. The microgap with electropolymerized C-NCP was then coated with glucose oxidase, an enzyme that undergoes a reaction in the presence of glucose or hydrogen peroxide that is detectable electrochemically.[93] Very basic sensitivity tests demonstrated that the sensor was sensitive to glucose levels between 5 and 20 mM, which falls within the important physiological range for diabetics.

In addition to conductive nanoparticles for C-NCP, silica and other insulating nanoparticle fillers have been extensively employed for high-k dielectrics for capacitors and inductors as discussed previously. Ceramic dopants such as barium titanate and silica have been used to make high-k dielectric materials, with a target k of 50 to 200 usually[23] for applications such as organic FETs. Micropatternable capacitors for PWB substrates have been realized using epoxy films 2 to 25 μm thick doped with barium titanate.[94]

8.5.2 Sensors

Pressure/Strain/Tactile Sensors

By far the most well-studied application of micropatterned C-NCPs is their utilization in piezoresistive pressure, strain, and tactile sensors.

The piezoresistive effect describes the changing electrical resistance of a material due to applied mechanical stress. The piezoresistive effect differs from the piezoelectric effect in that the piezoresistive effect only causes a change in resistance; it does not produce an electric potential. The *gauge factor* (GF) is used to give the sensitivity of a strain gauge to applied strain. The GF is the product of strain and the quotient of change in strain gauge electrical resistance and unstrained resistance of strain gauge. The gauge factor is given by[66]

$$\mathrm{GF} = (\Delta R/R)/(\Delta L/L) = \Delta R/\varepsilon R$$

where ε is the applied strain, ΔR is the change in strain gauge resistance, R is the baseline unstrained resistance of the strain gauge, ΔL is the change in strain gauge length, and L is the baseline length.

It has been demonstrated that the conductivity of an elastomer doped with conductive nanoparticles (e.g., carbon black or silver) increases with increasing strain, which may be attributed to better contact between particles in strained materials.[59] In general, the lower the nanoparticle doping, the higher the sensitivity or gauge factor[66,81] for samples above the percolation threshold. This effect has been exploited for utilization as a strain sensor,[70] pressure sensors,[10,66,81] a microfingerprint sensor,[64] and biologically inspired hair cell sensors.[95] Relative resistance changes of 113% under 42% strains have been reported.

In addition, C-NCP have been utilized for pressure (Fig. 8.8; see Ref. 96) and tactile sensors[67,68] by employing the conductive lines instead as electrodes for capacitive sensors or capacitive sensor arrays. For these sensors, applied force or pressure compresses the insulating material between the two electrodes. As capacitance of a structure is inversely proportional to the distance between the two electrodes, the capacitance goes up with applied pressure. This effect can be applied to a single capacitor for a pressure sensor, or to multiple capacitors in an array that can be read out using multiplexing for more complex tactile sensing (Fig. 8.9; see Ref. 67).

For both types of sensors, a wide variety of materials have been employed for the C-NCPs: for example, CNTs in PDMS, CNTs in polyimide, silver in PDMS, carbon black in PDMS, and CNTs in polyurethane.

Chemical Sensors

In addition to the glucose sensor electrodes mentioned previously, C-NCPs have been utilized in many other vapor/gas and liquid chemical sensors using a property whereby the material expands in the presence of an analyte. These sensors are basically the same as the piezoresistive sensors discussed in the last section, except the resistance changes as a result of polymer expansion in the presence of analyte rather

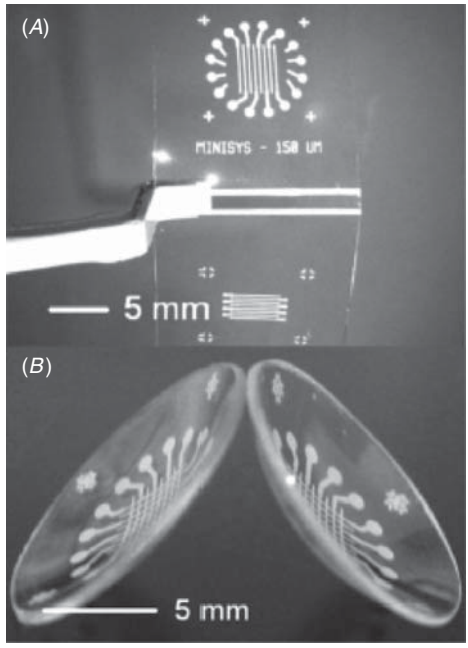
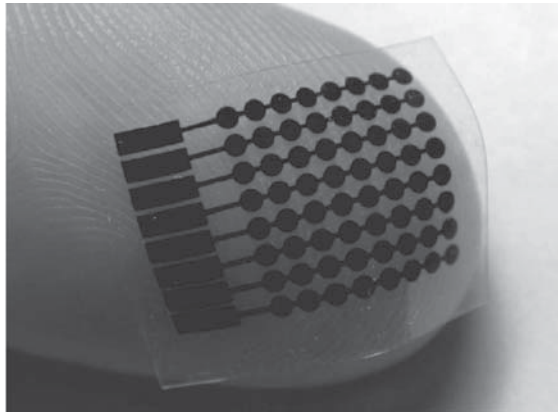


Figure 8.8 PDMS-silver C-NCP capacitive micropressure sensor in flexible PDMS substrate.[96] (*A*) Flattened sensors as fabricated; (*B*) sensor integrated into a curved surface.

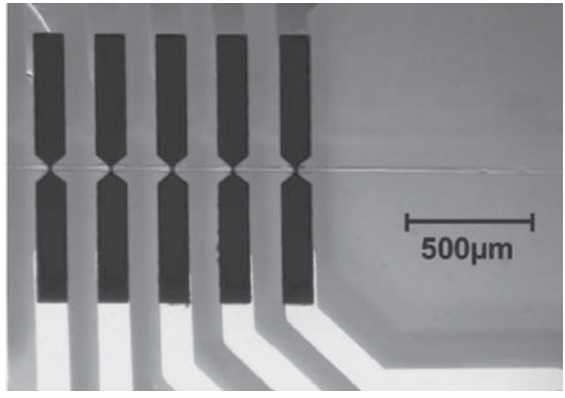
than because of an externally applied physical force. This effect is illustrated in Fig. 8.10. When the C-NCP matrix is exposed to analyte, the reaction between the molecules and the C-NCP matrix material changes the physical properties and dimensions of the polymer. The physical distance change between nanowires due to swelling may be the mechanism of resistance increase.[77]

Such chemical sensors have been developed for detecting a wide range of gases and vapors: functionalized CNTs in PMMA for wireless gas sensors for biohazardous solvent vapor detection[77]; carbon-black grafted carbon black-polyethylene for chloroform gas sensors[79]; CNT doped polyvinyl acetate for solvent detection[97]; MWCNTs in polystyrene for detection of tetrahydrofuran vapor[54]; CNT-doped polymers for a composite sensor capable of detecting a variety of vapors, otherwise known as an "electronic tongue"[98]; and SU-8 patterned silicone doped with carbon black for detection of alcohols and acetone.[99]

In addition, this detection mechanism whereby the resistance changes due to sorption of molecules, can be utilized for detecting liquids, for example, using carbon-black-doped polypropylene/polyurethane for alcohols.[65]



(*A*)



(*B*)

Figure 8.9 CNT-filled PDMS structures: (*A*) pressure sensors; (*B*) combined microfluidic channel with C-NCP electrodes.[67]

8.5.3 Actuators

NCPs have additionally been micropatterned into microactuators. Conductive, magnetic, and insulating nanoparticles have been employed, with a representative example of each discussed in this section. CNTs mixed with a hydrogel consisting of PVA and polyallylamine (PPA) have been reported that result in electroactive (electrically stimulated) microactuators that can be fabricated via micromolding against a silicone master.[84] The actuators were electrically stimulated and displacement (bending) measured using optics. Displacement for a 5 mm $\times$ 10 mm $\times$ 1 mm unimorph cantilever was on the order of 50 to 150 μm at the tip. It should be noted that a large number of other electroactive polymer actuators and microactuators

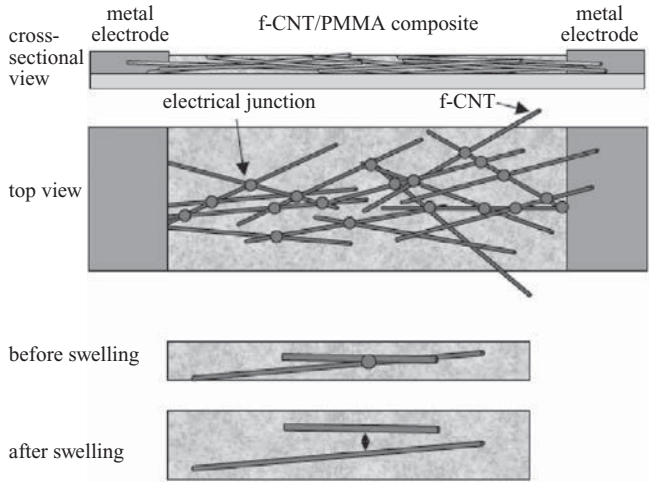


FIGURE 8.10 Illustration of principle of vapor and liquid sensors based on analyte-induced C-NCP expansion.[77] The resistance goes up as the nanocomposite expands in the presence of analyte.

based on conducting polymers, often with carbon black nanoparticles, have been reported. The interested reader is referred to Refs. 100 and 101 for a thorough discussion.

In addition, a number of magnetically actuated polymers doped with ferromagnetic iron-based or nickel micro- or nanoparticles have been reported (e.g., Refs. 24 and 26). In one example,[25] 80- to 150-nm nickel nanospheres were mixed with UV-patternable SU-8 at 1.33 to 13.3 wt% nanoparticles for MEMS actuators. Cantilevers 10, 11, and 12 mm long by 250 μm wide and 70 μm thick were deflected up to 1.5 mm at the tip. In addition, iron-PDMS composites have been suggested as a method of improving chip-to-chip attachment by microstructures.[72] In this case, iron-PDMS posts are expanded longitudinally and shrunk radially for easier insertion of an interconnect cylinder into a mating hole structure.

More exotic actuators have also been developed, including those based on expandable polymer microspheres that expand on application of heat in a PDMS matrix.[27]

8.5.4 Miscellaneous Devices of Note

C-NCPs may be utilizable as temperature sensors. For example, Niu et al.[92] have demonstrated the resistivity of carbon-black doped PDMS to increase with increasing temperature, while that of silver-doped PDMS exhibits a peak at 120°C and falls off after that. In 2007 (see

Ref. 59), this same research group also published another paper in which they had fabricated paperlike thermonic displays using PDMS-silver nanocomposites.

Optical devices can be realized by doping SU-8 with quantum dots and patterning it using two-photon polymerization.[28] Such materials and patterning methods may have applications in diffractive optical elements and 3D photonic crystals.

8.6 Summary and Future Directions

Many different C-NCPs based on a wide variety of conductive nanoparticles embedded in a diverse range of polymer bases have been demonstrated. Many of these materials have demonstrated micropatternability using conventional means such as photopatterning, micromolding, and printing, which is essential for their adoption into the MEMS and microsystems communities. Many of these materials are highly flexible and solve the problem of mechanical mismatch between metals and polymers.[102]

However, a question inevitably arises: how good (conductive) are these C-NCP materials and how practical is it to employ them in practical MEMS, microfluidic, lab-on-a-chip, and other microsystems? In general, even the best C-NCPs have conductivities at least a couple of orders of magnitude lower than most metals (e.g., silver, aluminum) regardless of the frequency of the electronic signal. Researchers continue to investigate methods of improving conductivity, while keeping the percolation thresholds low. Other particles in the nanoregime need to be investigated, including nanorods and other nanoparticles of silver, gold, platinum, aluminum, graphene, and fullerene. One potential solution to lower material conductivity is to employ films of C-NCPs that are much thicker than the submicrometer film thicknesses obtainable using conventional metallization techniques such as sputtering and e-beam deposition. Most C-NCP micropatterning methods such as photopatterning and micromolding inherently result in thicker films, so this may offer a practical solution. These greater thicknesses result in lower resistance for a given conducting line simply due to the larger cross-sectional area of the conductor.

In addition to research into the materials themselves, methods of micropatterning and integration with microdevices and systems are required. We are intensely investigating these aspects at the Microinstrumentaion Lab at Simon Fraser University, for a wide range of applications such as microfluidic device packaging, interdevice interconnect and assembly, MEMS actuators, chemical sensors, and RF MEMS. Other researchers are investigating similar areas, as well as microrobotic and other applications.

Other considerations revolve around the cost, purity, availability, and environmental and health concerns surrounding current and future nanoparticles. Current prices of these highly specialized materials created in small batches are very expensive, especially for the relatively large amounts of nanoparticles required for microsystem electronic packaging applications. Purity is an area of concern for those desiring pure metal materials, or either metallic or semiconducting CNT purity. Finally, research into the effects of various nanoparticles on human health and the environment is in its infancy and is not a straightforward problem given the huge variety of nanoparticle materials and shapes available, and nanomaterials that continue to be developed. This research is absolutely essential to determine whether or not C-NCPs offer a practical and responsible solution to many of the application areas discussed in this chapter.

References

1. J. W. Essam, "Percolation theory," *Reports on Progress in Physics*, vol. 43, pp. 53-911, 1980.
2. D. Stauffer and A. Aharony, *Introduction to Percolation Theory*, 2nd ed., Philadelphia, Taylor and Francis, 1994.
3. M. Karttunen, P. Ruuskanen, V. Pitkänen, and W. M. Albers, "Electrically conductive metal polymer nanocomposites for electronics applications," *Journal of Electronic Materials*, vol. 37(7), pp. 951-954, 2008.
4. Z.-M. Dang, M.-J. Jiang, D. Xie, S.-H. Yao, L.-Q. Zhang, and J. Bai, "Supersensitive linear piezoresistive property in carbon nanotubes/silicone rubber nanocomposites," *Journal of Applied Physics*, vol. 104, p. 024114:1-6, 2008.
5. J. K. W. Sandler, J. E. Kirk, I. A. Kinloch, M. S. P. Shafer, and A. H. Windle, "Ultra-low electrical percolation threshold in carbon-nanotube-epoxy composites," *Polymer*, vol. 44, pp. 5893-5899, 2003.
6. Z. L. Wang, "Self-assembled nanoarchitectures of polar nanobelts, nanowires," *Journal of Materials Chemistry*, vol. 15, pp. 1021-1024, 2005.
7. A. Sujatha, S. Thotapalli, and P. B. Mandal, "One step synthesis of silver nanorods by autoreduction of aqueous silver ions with hydroxyapatite: an inorganic-inorganic hybrid nanocomposite," *Journal of Biomedical Materials Research Part A*, vol. 80(2), pp. 391-398, 2007.
8. Y. Ni, X. Ge, H. Liu, Z. Zhang, Q. Ye, and F. Wang, "Fabrication of nanorod copper-polymer composites by γ-irradiation route in a heterogeneous system," *Chemistry Letters*, vol. 30(5), p. 458, 2001.
9. L. Qu, G. Shi, X. Wu, and B. Fan, "Facile route to silver nanotubes," *Advanced Materials*, vol. 16(14), pp. 1200-1203, 2004.
10. H. Cong and T. Pan, "Photopatternable conductive PDMS materials for microfabrication," *Advanced Functional Materials*, vol. 18(13), pp. 1912-1921, 2008.
11. C. E. Hoppe, C. Rodríguez-Abreu, M. Lazzari, M. A. López-Quintela, and C. Solans, "One-pot preparation of gold-elastomer nanocomposites using PDMS-graft-PEO copolymer micelles as nanoreactors," *physica status solidi (a)*, vol. 205(6), pp. 1455-1459, 2007.
12. V. Pardo-Yissar, R. Gabai, A. N. Shipway, T. Bourenko, and I. Willner, "Gold nanoparticle/hydrogel composites with solvent-switchable electronic properties," *Advanced Materials*, vol. 13(17), pp. 1320-1323, 2001.
13. C. J. Murphy and C. J. Orendorff, "Alignment of gold nanorods in polymer composites and on polymer surfaces," *Advanced Materials*, vol. 17(18), pp. 2173-2177, 2005.

14. R. Krishnaswamy, H. Remita, M. Impéror-Clerc, C. Even, P. Davidson, and B. Pansu, "Synthesis of single-crystalline platinum nanorods within a soft crystalline surfactant-PtII Complex," *Chemical Physics*, vol. 7(7), p. 1510, 2006.
15. O. Antoine,Y. Bultel, and R. Durand, "Oxygen reduction reaction kinetics and mechanism on platinum nanoparticles inside Nafion," *Journal of Electroanalytical Chemistry*, vol. 499(1), pp. 85-89, 2001.
16. X. Huang, P. Jiang C. Kim, Q. Ke, and G. Wang, "Preparation, microstructure and properties of polyethylene aluminum nanocomposite dielectrics," *Composites Science and Technology*, vol. 68(9), pp. 2134-2140, 2008.
17. S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, p. 56, 1991.
18. S. Reich, C. Thomsen, and J. Maultzsch, *Carbon Nanotubes: Basic Concepts and Physical Properties*, New York, Wiley-VCH, 2004.
19. M. Meyyappan, Ed., *Carbon Nanotubes: Science and Applications*, Boca Raton, FL, CRC Press, 2005.
20. C. Li, E. T. Thostenson, and T.-W. Chou, "Sensors and actuators based on carbon nanotubes and their composites: a review," *Composites Science and Technology*, vol. 68, pp. 1227-1249, 2008.
21. M. P. Anatram and F. Leonard, "Physics of carbon nanotube electronic devices," *Reports on Progress in Physics*, vol. 69, pp. 507-561, 2006.
22. M. Roukes, "Nanoelectromechanical systems face the future," *Physics World*, vol. 4, pp. 25-31, 2001.
23. J. E. Morris, "Nanopackaging: nanoelectronics and electronics packaging," in Nanopackaging, J. E. Morris, Ed., New York, Springer, pp. 1-14, 2008.
24. H. J. Cho and C. H. Ahn, "Microscale resin-bonded permanent magnets for magnetic micro-electro-mechanical systems applications," *Journal of Applied Physics*, vol. 93(10), pp. 8674-8676, 2003.
25. N. Damean, B. A. Parviz, J. N. Lee, T. Odom, and G. M. Whitesides, "Composite ferromagnetic photoresist for the fabrication of microelectromechanical systems," *Journal of Micromechanics and Microengineering*, vol. 15, pp. 29-34, 2005.
26. J. J. Mack, B. N. Cox, M. Lee, J. C. Y. Dunn, and B. W. Wu, "Magnetically actuable polymer nanocomposites for bioengineering applications," *Journal of Materials Science*, vol. 42, pp. 6139-6147, 2007.
27. B. Samel, P. Griss, and G. Stemme, "A thermally responsive PDMS composite and its microfluidic applications," *Journal of Microelectromechanical Systems*, vol. 16(1), pp. 50-57, 2007.
28. B. Jia, J. Li, and M. Gu, "Two-photon polymerization for three-dimensional photonic devices in polymers and nanocomposites," *Australian Journal of Chemistry*, vol. 60, pp. 484-495, 2007.
29. H. Becker and L. E. Locascio, "Polymer microfluidic devices (review)," *Talanta*, vol. 56, pp. 267-287, 2002.
30. J. Jiang, G. Oberdorster, and P. Biswa, "Characterization of size, surface charge, and agglomeration state of nanoparticle dispersions for toxicological studies," *Journal of Nanoparticle Research*, vol. 11, pp. 77-89, 2009.
31. K. Sato, J.-G. Li, H. Kamiya, and T. Ishigaki; "Ultrasonic dispersion of TiO_2 nanoparticles in aqueous suspension," *Journal of the American Ceramics Society*, vol. 91(8), pp. 2481-2487, 2008.
32. S. J. Doktycz and K. S. Suslick, "Interparticle collisions driven by ultrasound," *Science*, vol. 247, pp. 1067-1069, 1990.
33. K. Higashitani, K. Yoshida, N. Tanise, and H. Murata, "Dispersion of coagulated colloids by ultrasonication," *Colloids and Surfaces A: Physicochemical and Engineering Aspects*, vol. 81, pp. 167-175, 1993.
34. R. Andrews, D. Jacques, M. Minot, and T. Rantell, "Fabrication of carbon multiwall nanotube/polymer composites by shear mixing," *Macromolecular Materials and Engineering*, vol. 287(6), pp. 287-395, 2002.

35. Y. A. Kim, T. Hayashi, Y. Fukai, and M. Endo, "Effect of ball milling on morphology of cup-stacked carbon nanotubes," *Chemical Physics Letters*, vol. 355(3-4), pp. 279-284, 2002.
36. M. Inkyo, T. Tahara, T. Iwaki, F. Iskandar, C.-J. Hogan, Jr., and K. Okuyama, "Investigation of nanoparticle dispersion by centrifugal bead separation," *Journal of Colloid and Interface Science*, vol. 304, pp. 535-540, 2006.
37. R. Ramasubramaniam and J. Chen, "Homogeneous carbon nanotube/polymer composites for electrical applications," *Applied Physics Letters*, vol. 83(14) , pp. 2928-2930, 2003.
38. H. Lorenz, M. Despont, N. Fahrni, N. LaBianca, P. Renaud, and P. Vettiger, "Su-8: a low-cost negative resist for MEMS," *Journal of Micromechanics and Microengineering*, vol. 7, pp. 121-124, 1997.
39. *Microchemistry Online*, http://www.microchem.com/products/pdf/SU8_50-100.pdf (retrieved September 2009).
40. M. B. Chan-Park, J. Zhang, Y. Yan, and C. Y. Yue, "Fabrication of large Su-8 mold with high aspect ratio microchannels by UV exposure dose reduction," *Sensors and Actuators B: Chemical*, vol. 101, pp. 175-182, 2004.
41. H. C. Chiamori, J. W. Brown, E. V. Adhiprakasha, E. T. Hantsoo, J. B. Straalsund, N. A. Melosh, et al., "Suspension of nanoparticles in SU-8: processing and characterization of nanocomposite polymers," *Microelectronics Journal*, vol. 39, pp. 228-236, 2008.
42. S. Westwood, S. Jaffer, and B. L. Gray, "Enclosed SU-8 and PDMS microchannels with integrated interconnects for chip-to-chip and world-to-chip connections," *Journal of Micromechanics and Microengineering*, vol. 18(6), p. 064014, 2008.
43. Y. Xia and G. M. Whitesides, "Soft lithography," *Annual Review of Materials Science*, vol. 28, pp. 153-184, 1998.
44. J. Ge and J. K. Kivilahti, "Effects of surface treatments on the adhesion of Cu and CrCu metallizations to a multifunctional photoresist," *Journal of Applied Physics*, vol. 92, pp. 3007-3015, 2002.
45. L. Ye, Z. Lai, J. Liu, and A. Tholen, "Effect of Ag particle size on electrical conductivity of isotropically conductive adhesives," *IEEE Transactions Electronics Packaging Manufacturing*, vol. 22(4), pp. 299-302, 1999.
46. H. P. Wu, X. J. Wu, M. Y. Ge, G. Q. Zhang, Y. W. Wang, and J. Z. Jiang, "Effect analysis of filler sizes on percolation threshold of isotropical conductive adhesives," *Composites Science and Technology*, vol. 67, pp. 1116-1120, 2007.
47. P. Gonon and A. Boudefel, "Electrical properties of epoxy/silver nanocomposites," *Journal of Applied Physics*, vol. 99, p. 024308, 2006.
48. S. Jiguet, A. Bertsch, H. Hofmann, and P. Renaud, "SU-8-Silver photosensitive nanocomposite,"*Advanced Engineering Materials*, vol. 6, pp. 719-724, 2004.
49. S. Jiguet, A. Bertsch, H. Hofmann, and P. Renaud, "Conductive SU8 photoresist for microfabrication,"*Advanced Functional Materials*, vol. 15, pp. 1511-1516, 2005.
50. A. Moisala, Q. Li, I. A. Kinlich, and A. H. Windle, "Thermal and electrical conductivity of single- and multi- walled carbon nanotube-epoxy composites," *Composites Science and Technology*, vol. 66, pp. 1285-1288, 2006.
51. M. B. Bryning, M. F. Islam, J. M. Kikkawa, and A. G. Yodh, "Very low conductivity threshold in bulk isotropic single-walled carbon nanotube-epoxy composites," *Advanced Materials*, vol. 17, pp. 1186-1191, 2005.
52. N. Hauptman, M. Žeglič, M. Maček, and M. K. Gunde, "Carbon based conductive photoresist," *Journal of Materials Science*, vol. 44, pp. 4625-4632, 2009.
53. M. Lillemose L. Gammelgaarda, J. Richtera, E. V. Thomsena, and A. Boisen, "Epoxy based photoresist/carbon nanoparticle composites," *Composites Science and Technology*, vol. 68, pp. 1831-1836, 2008.
54. B. Zhang, R. W. Fu, M. Q. Zhang, X. M. Dong, P. L. Lan, and J. S. Qiu, "Preparation and characterization of gas-sensitive composites from multi-walled carbon nanotubes/polystyrene," *Sensors and Actuators B*, vol. 109, pp. 323-328, 2005.

55. S. Jiguet, M. Judelewicz, S. Mischler, H. Hofman, A. Bertsch, and P. Renaud, "SU-8 nanocomposite coatings with improved tribological performance for MEMS," *Surface Coatings and Technology*, vol. 201, pp. 2289-2295, 2006.
56. A. Voight, M. Heinrich, C. Martin, A. Llobera, G. Gruetzner, and F. Pérez-Murano, "Improved properties of epoxy nanocomposites for specific applications in the field of MEMS/NEMS," *Microelectronic Engineering*, vol. 84, pp. 1075-1079, 2007.
57. N. Zhang, J. Xie, M. Guers, and V. K. Varadan, "Chemical bonding of multi-walled carbon nanotubes to SU-8 via ultrasonic irradiation," *Smart Materials and Structures*, vol. 12, pp. 260-263, 2003.
58. G. R. Ruschau and R. E. Newnham, "Critical volume fractions in conductive composites," *Journal of Composite Materials*, vol. 26(18), pp. 2727-2735, 1992.
59. X. Niu, S. Peng, L. Liu, W. Wen, and P. Sheng, "Characterizing and patterning of PDMS-based conducting composites," *Advanced Materials*, vol. 19, pp. 2682-2686, 2007.
60. M. G. Urdanetta, R. Delille, and E. Smela, "Stretchable electrodes with high conductivity and photo-patternability," *Advanced Materials*, vol. 19, pp. 2629-2633, 2007.
61. G. A. Gelves, B. Lin, U. Sundararaj, and J. A. Haber, "Electrical and rheological percolation threshold of polymer nanocomposites prepared with functionalized copper nanowires," *Nanotechnology*, vol. 19, p. 215712, 2008.
62. M. A. Unger, H.-P. Chou, T. Thorsen, A. Scherer, and S. R. Quake, "Monolithic microfabricated valves and pumps by multilayer soft lithography," *Science*, vol. 288(5463), pp. 113-116, 2000.
63. S. P. Rwei, F. H. Ku, and K. C. Cheng, "Characterizing and patterning of PDMS-based conducting composites," *Colloid and Polymer Science*, vol. 280, pp. 1110-1115, 2002.
64. M. Lu, A. Bermak, and Y.-K. Lee, "Fabrication technology of piezoresistive conductive PDMS for micro fingerprint sensors," *MEMS 2007, Kobe*, pp. 251-254, 2007.
65. E. Segal, R. Tchoudakov, M. Narkis, and A. Siegmann, "Sensing of liquids by electrically conductive immiscible polypropylene/thermoplastic polyurethane blends containing carbon black," *Journal of Polymer Science*, vol. 41, pp. 1428-1440, 2003.
66. J. Lu , M. Lu , A. Bermak, and Y.-K. Lee, "Study of piezoresistance effect of carbon nanotube-PDMS composite materials for nanosensors," *Proceedings of the 7th IEEE International Conference on Nanotechnology, Hong Kong (August 2-5, 2007)*, pp. 1240-1243, 2007.
67. C. Liu, "Nanocomposite conductive elastomer: microfabrication processes and applications in soft-matter MEMS sensors," *Materials Research Society Symposium Proceedings*, vol. 947, pp. A07-A01, 2007.
68. J. Engel, J. Chen, N. Chen, S. Pandya, and C. Liu, "Multi-walled carbon nanotube filled conductive elastomers: materials and application to micro transducers," *19th IEEE International Conference on Micro Electro Mechanical Systems, Istanbul*, pp. 246-249, 2006.
69. A. Khosla and B. L. Gray, "Preparation, characterization, and micromoulding of multi-walled carbon nanotube polydimethylsiloxane conducting nanocomposite polymer," *Materials Letters*, vol. 63(13-14), pp. 1203-1206, 2009.
70. C.-X. Liu and J.-W. Choi, "Patterning conductive PDMS nanocomposites in an elastomer using microcontact printing," *Journal of Micromechanics and Microengineering*, vol. 19, p. 085019, 2009.
71. S. A. Curran, D. H. Zhang, W. T. Wondmagegn, A. V. Ellis, J. Cech, S. Roth, et al., "Dynamic electrical properties of polymer-carbon nanotube composites: enhancement through covalent bonding," *Journal of Materials Research*, vol. 21, pp. 1071-1077, 2006.

72. S. Jaffer, B. L. Gray, D. G. Sahota, and M. H. Sjoerdsma, "Mechanical assembly and magnetic actuation of polydimethylsiloxane-iron composite interconnects for microfluidic systems," *Proceedings of SPIE*, 6886-0Q-1, 2008.
73. K. W. Oh and C. H. Ahn, "A new flip-chip bonding technique using micromachined conductive polymer bumps,"*IEEE Transactions on Advanced Packaging*, vol. 22(4), pp. 586-591, 1999.
74. K. W. Oh, C. H. Ahn, and K. P. Roenker, "Flip-chip packaging using micromachined conductive polymer bumps and alignment pedestals for MOEMS," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 5(1), pp. 119-126, 1999.
75. A. Salmi, S. Benfarhi, J. B. Donnet, and C. Decker, "Synthesis of carbon-polyacrylate nanocomposite materials by cross-linking polymerization," *European Polymer Journal*, vol. 42, pp. 1966-1974, 2006.
76. T. Fugigaya, S. Haraguchi, T. Fukumaru, and N. Nakashima, "Development of novel carbon nanotube/photopolymer nanocomposites with high conductivity and their application to nanoimprint photolithography," *Advanced Materials*, vol. 20, pp. 2151-2155, 2008.
77. H. Yoon, J. Xie, J. K. Abraham, V. K. Varadan, and P. B. Ruffin, "Passive wireless sensors using electrical transition of carbon nanotube junctions in polymer matrix," *Smart Materials and Structures*, vol. 15, pp. S14-S20, 2006.
78. F. Du, J. E. Fischer, and K. I. Winey, "Coagulation method for preparing single-walled carbon nanotube/Poly(methyl methacrylate) composites and their modulus, electrical conductivity, and thermal stability," *Journal of Polymer Science*, vol. 41, pp. 3333-3338, 2003.
79. J. Chen and N. Tsubokawa, "Novel gas sensor from polymer-grafted carbon black: vapor response of electrical resistance of conducting composites prepared from poly(ethylene-block-ethylene oxide)-grafted carbon black," *Journal of Applied Polymer Science*, vol. 77, pp. 2437-2447, 2000.
80. T. McNally, P. Pötschke, P. Halley, M. Murphy, D. Martin, S. E. J. Bell, et al., "Polyethylene multiwalled carbon nanotube composites," *Polymer*, vol. 46, pp. 8222-8232, 2005.
81. C. Gau, H. S. Ko, and H. T. Chen, "Piezoresistive characteristics of MWNT nanocomposites and fabrication as a polymer pressure sensor," *Nanotechnology*, vol. 20, p. 185503, 2009.
82. K.-S. Teh and L. Lin, "MEMS sensor material based on polypyrrole-carbon nanotube nanocomposite: film deposition and characterization," *Journal of Micromechanics and Microengineering*, vol. 15, pp. 2019-2027, 2005.
83. S. Coutry, J. Mine, A. R. Tajbakhsh, and E. M. Terentjev, "Nematic elastomers with aligned carbon nanotubes: new electromechanical actuators," *Europhysics Letters*, vol. 64(5), pp. 654-660, 2003.
84. A. Mazzoldi, M. Tesconi, A. Tognetti, W. Rocchia, G. Vozzi, G. Pioggia, et al., "Electroactive carbon nanotube actuators: soft-lithographic fabrication and electro-chemical modeling," *Materials Science and Engineering C*, vol. 28, pp. 1057-1064, 2008.
85. D. Zhang, K. Ryu, X. Liu, E. Polikarpov, J. Ly, M. E. Thompson, et al., "Transport, conductive, and flexible carbon nanotube films and their application in organic light emitting diodes," *Nano Letters*, vol. 6(9), pp. 1880-1886, 2006.
86. M. Baibarac and P. Gomez-Romero, "Nanocomposites based on conducting polymers and carbon nanotubes from fancy materials to functional applications," *Nanoscience and Nanotechnology*, vol. 6(1), pp. 1-14, 2006.
87. G. Gruner, "Carbon nanotube films for transport and plastic electronics," *Journal of Materials Chemistry*, vol. 16, pp. 3533-3539, 2006.
88. R. N. Das, H. Lin, K. I. Papathomas, J. M. Lauffer, N. Card, et al., "Printable nanocomposites for advanced organic packaging," Electronic Components and Technology Conference, pp. 316-322, 2007.
89. G. B. Blanchet, C. R. Fincher, and F. Gao, "Polyaniline nanotube composites: a high-resolution printable conductor," *Applied Physics Letters*, vol. 82(8), pp. 1290-1292, 2003.

90. F. Antolini, A. Ghezelbash, C. Esposito, E. Trave, L. Tapfer, and B. A. Korgel, "Laser-induced nanocomposite formation for printed circuit nanoelectronics," *Materials Letters*, vol. 60, pp. 1095-1098, 2006.
91. F. Dawan, Y. Jin, J. Goettert, and S. Ibekwe, "High functionality of a polymer nanocomposite material for MEMS applications," *Microsystem Technologies*, vol. 14, pp. 1451-1459, 2008.
92. X. Niu, W. Wen, and Y.-K. Lee, "Electrorheological-fluid-based microvalves," *Applied Physics Letters*, vol. 87, p. 243501, 2005.
93. J. N. Patel, B. L. Gray, B. Kaminska, and B. D. Gates, "Flexible glucose sensor utilizing multilayer PDMS process," IEEE 30th Annual Engineering in Medicine and Biology Conference, Vancouver, August 2008.
94. R. N. Das, J. M. Lauffer, and V. R. Markovich, "Fabrication, integration, and reliability of nanocomposite based embedded capacitors in microelectronics packaging," *Journal of Materials Chemistry*, vol. 18, pp. 537-544, 2008.
95. C. Liu, J. Engel, J. Chen, N. Chen, S. Pandya, Y. Yang, et al., "Polymer micro- and nano-scale fabrication technology development for bioinspired sensing," *International Conference on Nano/Micro Engineered and Molecular Systems*, pp. 1470-1473, 2006.
96. H. Cong and T. Pan, "Microfabrication of conductive PDMS on flexible substrates for biomedical applications," *Proceedings of 4th IEEE International Conference on Nano/Micro Engineering and Molecular Systems, Shenzhen*, pp. 731-734, 2009.
97. C. Wei, L. Dai, A. Roy, and T. B. Tolle, "Multifunctional chemical vapor sensors of aligned carbon nanotube polymer composites," *Journal of the American Chemical Society*, vol. 128, pp. 1412-1413, 2006.
98. G. Pioggia, F. Di Francesco, A. Marchetti, M. Ferro, R. Leardi, and A. Ahluwalia, "A composite sensor array impediometric electronic tongue: Part II. Discrimination of basic tastes," *Biosensors and Bioelectronics*, vol. 22, pp. 2624-2628, 2007.
99. V. T. S. Wong, A. Huang, and C.-M. Ho, "SU-8 lift-off patterned silicone chemical vapor sensor arrays," *18th IEEE International Conference on Micro Electro Mechanical Systems*, pp. 754-757, 2005.
100. R. H. Baughman, R. L. Shacklette, and R. L. Elsenbaummer, "Microelectromechanical actuators based on conducting polymers," in *Topics in Molecular Organization and Engineering, Volume 7: Molecular Electronics*, P. I. Lazarev, Ed., pp. 267-289, Dordrecht, The Netherlands, Kluwer Academic, 1991.
101. R. H. Baughman, "Conducting polymer artificial muscles," *Synthetic Metals*, vol. 78, pp. 339-353, 1996.
102. J. N. Patel, B. Kaminska, B. L. Gray, and B. D. Gates, "A sacrificial SU-8 mask for direct metallization on PDMS," *Journal of Micromechanics and Microengineering*, vol. 19 num. 11, 115014 (10 pp.), 2009.

CHAPTER 9

Single-Electron Conductivity in Organic Nanostructures for Transistors and Memories

Sandro Carrara

9.1 Introduction

Much effort has been devoted to building a transistor based on single-electron trapping since the first theoretical prediction of Coulomb blockade in 1986. Devices operating at a few kelvins were fabricated in the first 10 years; the first device able to properly operate at room temperature was described in the literature only in 1997. Problems arose that were mainly due to prohibitive constraints on the transistor geometry. For example, not all the features of Coulomb blockade were observed at room temperature in early devices.

Most of these problems have now been solved, thanks to new advancements in silicon technology, which is now ready to scale down to devices under 10 nm. The possibility of fabricating a gate length of 6 nm in a *metal-oxide semiconductor field-effect transistor* (MOSFET) by using *ultrathin silicon-on-insulator* (UTSOI) technology[1] has already been proved. Chip production, presently at 90-nm node technology, will probably reach the sub-10-nm scale regime within the next 15 years, as expected.[2]

A MOSFET can be used as an amplifier or as a switcher. In both cases, an important parameter is how fast the transistor can switch from the "off" to the "on" state. It affects the maximum clock frequency in digital circuits and the unity gain frequency for analog applications. A smaller gate length improves this parameter. Therefore, much effort will be spent to scale down *complementary metal oxide semiconductor*

(CMOS) structures in the next decade. However, decreasing the gate length implies higher electric fields along the channel, thus making it critical to control the voltage in smaller structures. This fact demands new manufacturability requirements, such as gate stacks with higher dielectric constant[3] and alternative doping techniques to produce shallow and abrupt junction profiles.[1] Extremely low sizes may present problems such as doping nonuniformities, depletion regions leading to short circuits due to punch-through or tunneling effects, leakages, and breakdowns.[4] Aggressive MOSFET scaling can also affect parameter fluctuations and channel region continuity.[5] Moreover, simulations considering various device architectures, including *silicon on insulator* (SOI) and *silicon on nothing* (SON), show that conventional technology cannot match all requirements of the Silicon Industries Roadmap.[6] It does not appear to be achievable to maintain the same evolution rate in coming decades simply through development of currently available devices,[4] and therefore, new and revolutionary designs are required to replace the actual transistor paradigms.[2] The physical thickness of insulators for CMOS technology has decreased to 1.2 nm.[3] In the next decade, it will be possible to fabricate transistors having gate length of 6 nm interfaced to a gate electrode with 1-nm insulator thickness with CMOS silicon technology. In such a structure, tunneling currents will appear, and a Coulomb trap may occur in such transistors if the channel is shorter. So, *single-electron transistors* (SETs) can be seen as the ultimate result of transistor scaling. New designs for memories and logic circuits are possible at the nanoscale by using SETs as basic elements.[7] This possibility led earlier applied research in Japanese companies such as Hitachi[8] and Fujitsu[9] in the 1990s.

On the other hand, relatively easy methods of obtaining metal nanoparticles encapsulated by organic coaters[10] open a new way to confine single electrons. The confining regions thus obtained have sizes of a very few nanometers, and therefore, they may be useful to fabricate devices working at room temperatures. These organic nanoparticles behave as quantum dots.

However, dealing with molecular devices is a great issue. The nature of individual molecules placed between the device electrodes could affect the current conductivity by two orders of magnitude,[11] and current conductivity could also be greatly affected by the electrode-molecule interface rather than by specific molecule behavior.[12] The creation of metal filaments between electrodes may also affect the junctions' behavior.[13] These phenomena support the common belief that molecular electronics cannot dethrone silicon technology, at least for another decade.[14] Therefore, techniques to develop SETs by using molecular nanostructures have to be compared with those that use silicon ones. Many reviews of SET physics[15,16] and their working characteristics[5–8] have appeared in the literature. Although some good reviews have appeared recently,[7] no recent paper discusses

all the possible techniques to fabricate nanostructures working as a SET. Therefore, the aim of this chapter is to summarize all of the methods for single-electron device fabrication.

9.2 Transistors Working at 4 K

From the technological point of view, a device that works properly only at 4 K has a limited scope of application. However, more than two decades of experiments in this field have shown important results and have supplied many useful solutions for the history of the SET operating at room temperature. Therefore, this part of the whole effort toward SETs could not be neglected. Thus, the main experiments on SET operating at very low temperatures are briefly summarized in this section.

The first experiments that observed single-electron phenomena at a few kelvins were done in 1988, with structures made by point contact tunnel junctions,[18] and in 1991 and 1992 in structures made by insulating barriers.[19,20] The thermal energy must be less than the electrostatic energy in order to have single-electron trapping in a quantum dot:

$$\frac{e^2}{2C} \geq kT. \tag{9.1}$$

The electrostatic energy for trapping electrons at the nanoscale is in the range between 8×10^{-23} and 8×10^{-21} J.[21] This means there are only two possible ways to fabricate structures capable of exploiting single-electron trapping: decreasing the temperature to a few kelvins in order to obtain low values of thermal energy, or decreasing dot capacitance in order to increase the electrostatic energy. The latter option implies working with capacitance values on the order of 10^{-18} F,[21] which can be obtained if the size of the dot is less than 10 nm. Simulations show that the appearance of all the Coulomb blockade features requires a dot size less than 3 nm.[22] Such dot sizes are not technologically easy to obtain. Therefore, first successful experiments were conducted working at low temperature.

On the basis of the fabrication technique used to build up the structures, all published work for devices working at very low temperature can be divided in various groups. The first group is for SETs fabricated with conventional MOSFET structures. In this case, the SET structure is realized by the creation of an island to trap electrons directly along a very narrow channel of a usual MOSFET. The scheme of the realized device is shown in Fig. 9.1. The island acting as a quantum dot was created with electron-beam lithography on top of a silicon layer.[23] Further etching of the buried oxide was performed in order to create a free-standing bridge between the source and the drain electrodes. A further 40 to 50 nm of oxide layer was thermally grown in order to

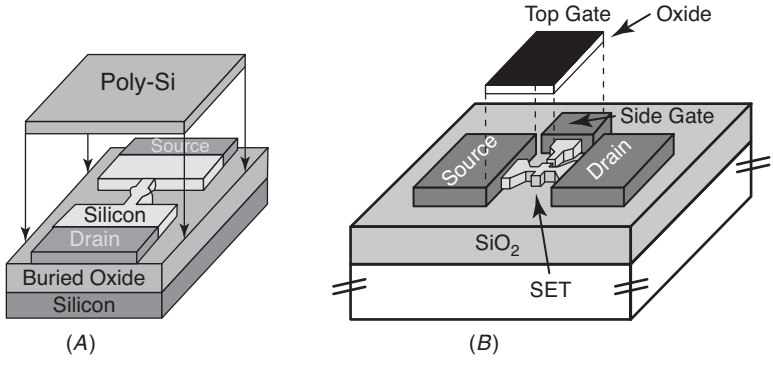


Figure 9.1 Typical schematics of device structures in the case of a SET fabricated by electron-beam lithography. The quantum dot is formed into the channel region of a MOSFET. (*A*) Possible SET structure having only the top gate electrode. (Reprinted from Ref. 23, copyright 2000, with permission from American Institute of Physics.) (*B*) SET structure having the top gate electrode and an in-plane gate. (Reprinted from Ref. 25, copyright 2001, with permission from American Institute of Physics.)

enhance the dot size effect. Finally, a polysilicon gate was deposited as the top electrode covering the island, source, and drain regions. A variation of this structure was fabricated with a lateral gate[24] or with a dual gate configuration.[25] In this case, SET control is done by means of the in-plane gate. Further, it was possible to obtain an island size of about 10 nm by adding *reactive ion etching* (RIE) after the electron-beam lithography.[25] Another possibility to obtain electronic confinement in MOSFETs is by fabricating optimized access resistances larger than the quantum resistance ($\sim$25.8 kΩ).[26] This fact suggested different ways to fabricate SETs in CMOS or SOI structures. For example, SET devices were fabricated reducing the lateral channel size by electron-beam lithography[26]; by forming vertical pattern-dependent oxidation[27]; by modulation-doped SiGe heterostructures[28,29]; by sidewall depletion regions in the gate[30]; or by Coulomb islands in fully depleted SOI structures.[31] Figure 9.2 shows *scanning electron microscopy* (SEM) images for two such possible structures. The first is obtained by electron-beam lithography on a 10-nm-thick SOI layer that is highly resistive and highly doped. The second is a 110-nm-wide heterostructure obtained by low-pressure chemical vapor deposition in a UHV chamber. In the latter case, the channel was obtained in a series of layers in the following sequence: an 11-nm-thick silicon channel, a 5.7-nm-thick $Si_{0.81}Ge_{0.19}$ spacer layer, a 5.7-nm n-doped $Si_{0.81}Ge_{0.19}$ layer, a 35-nm $Si_{0.81}Ge_{0.19}$ spacer layer, and a final 15-nm Si cap layer. Both structures show constrictions along the source-drain channels providing the single charge accumulation and, therefore, they show Coulomb blockade effects. Top gate electrodes complete the SET geometry in

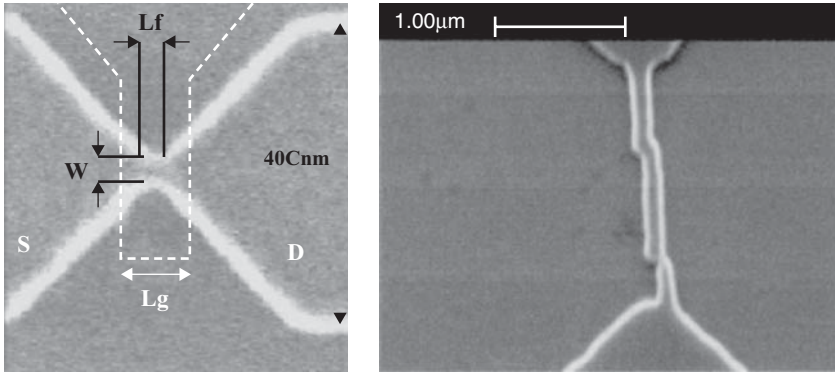


Figure 9.2 Source-drain channels for SETs fabricated by using electron-beam lithography. The accumulation island is formed by the creation of regions with resistance larger than the quantum resistance. (*a*), Island obtained by lateral etching in a 10-nm-thick SOI layer. (Reprinted from Ref. 26, copyright 2003, with permission from IEEE.) (*b*) Constriction induced on a 110-nm-wide bend-wire geometry by using chemical vapor deposition, lithography, and subsequent RIE. (Reprinted from Ref. 28, copyright 2003, with permission from American Institute of Physics.)

both cases, as in the case of Fig. 9.1. Structures with accumulation regions in silicon-based source-drain channel were built both with p- and n-type silicon.[23,31] The conductivity is not due to the charge type but to the carriers trapped in the dot, and thus the electrical transport is similar for p- and n-type silicon. Of course, the possibility of creating dot islands by means of restrictions, cuts, or highly resistive regions along a wire may also be pursued by using wires not fabricated with silicon. For example, Coulomb blockade phenomena were observed in Pt nanowires and in *multiwalled carbon nanotubes* (MWNTs). In the first case, the trapping island was formed because the Pt wires may contain both atomic and clustered Pt. Moreover, hydrocarbon debris and amorphous C islands were obtained because of gas precursors during electron-beam-induced deposition.[32] In this case, a high access resistance is formed between the Pt nanocrystals in the wire. High access resistance is also provided by MWNTs because tunneling junctions are formed between the nanotubes and the contact electrodes.[33,34] The MWNT/electrode resistance crucially depends on the metal used for electrode formation.[35] Moreover, electric transport in *single-walled carbon nanotubes* (SWNTS) occurs through well-separated and discrete electron states,[36] which may contribute to electron confinement and, therefore, to Coulomb blockade.[37] Tunneling junctions could also be realized by means of oxide growth. For example, structures such as metal/metal-oxide/metal/metal-oxide/metal were realized by combining ion-beam sputtering[38] or multiple-angle

evaporation[39] to electron-beam lithography. In these cases, the SETs were realized only to fabricate and characterize superconducting transistors.

On the other hand, individual metal or semiconducting nanoparticles, stabilized by organic coatings and fabricated by any method, are immediately available as insulated islands for charge accumulation. Nanoparticles could be chemically synthesized[10] and then placed between metallic electrodes by various deposition techniques or trapping methods. The problem is how to form a separation gap between metal electrodes that is small enough to electrically address the single nanoparticle. Different methods were initially considered to solve this problem: angled evaporation was considered to close the gap in gold electrodes,[40,41] electromigration was used to open a small gap in a wire,[42,43] and gold disks were used to stop up the gap between island and electrodes.[44,45] A review of the possible ways to fabricate electrodes with very small gaps in between is presented in Ref. 46. Typical features of single-electron conductivity were observed at very low temperature in all the structures that employed nanoparticles: current suppression near zero voltage, called the Coulomb gap,[25,28,31,32,34,35,38,42,44] Coulomb staircase,[42,45] and *negative differential resistance* (NDR).[18,26,31,39] Similar periodic oscillations have also been observed in the source-drain conductance.[23,25,27,43] Rhombic features were measured in differential conductance plotted on gate and drain-source voltages.[28,37,40] All these behaviors were predicted for single-electron trapping by the theory. In these experiments, the device working temperatures were kept at 4.2 K or less, down to 20 mK.[38]

9.3 Room-Temperature Inorganic Transistors

The operability of some types of SETs presented in the previous section has been also tested at higher temperatures. Periodical oscillations in the conductance were observed up to 40 K,[27] and a Coulomb gap was clearly seen up to 150 K,[25,34] or even at 300 K,[42] even in noised I-V curves. As we have seen, the dot capacitance should be down to 10^{-18} F to obtain a structure working at room temperature.[21] Such a capacitance value can be obtained only with sizes below 10 nm. The first structures with such a size and clearly showing single-electron trapping at room temperature were realized by using *scanning tunneling microscopy* (STM). Coulomb blockade was first observed at room temperature in 1992 on metallic nanoparticles,[47] whereas Coulomb blockade and NDR were observed on semiconductor nanoparticles only in 1995.[48] In 1996, single-electron junctions were fabricated by using a piezoactuator to approach the single nanoparticles.[49] Such a setup was successfully used to investigate the behavior of organic junctions[50] or biotransistors[51] at nanoscale, but it is useless to fabricate real

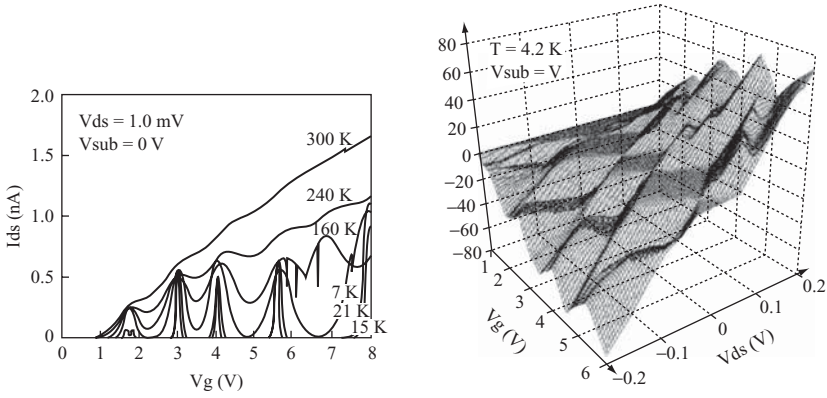


Figure 9.3 Current-voltage characteristics measured with SET structures. (*A*) The curves demonstrate that the staircase at 300 K is closely related to the NDR effect recorded under 240 K. Temperature scanning shows clearly that single-electron phenomenon is evidenced with a decrease in temperature due to the effect of the balance between the thermal and the electrostatic energy shown in Eq. (9.1). (*B*) The surface shows that clear stairs also appear on the gate and drain-source voltages. (Reprinted from Ref. 52, copyright 1997, with permission from the American Institute of Physics.)

transistors. Therefore, it was necessary to wait until December 1997 to get the first device really working as a SET.[52] That device is presented here as the first room-temperature SET because it clearly shows all the features of a single-electron transistor. Coulomb blockade was registered at room temperature and NDR at low temperature. The registered NDR was strictly related to staircase features measured at room temperature, as clearly shown by Fig. 9.3*A*. Moreover, gate control was also reported, as shown in Fig. 9.3*B*, even if it was shown only at 4.2 K. This is because the gate control is much more evident at a few kelvins than at room temperature.

This SET device was realized by fabricating a point-contact MOSFET. The scheme of the device is shown in Fig. 9.4. The channel was realized with a p-type, (001)-oriented silicon-on-insulator structure. The substrate was prepared by the implanted oxygen technique. The point-contact region was defined with electron-beam lithography. The final structure was realized with anisotropic etching by using tetramethylammonium hydroxide because it is compatible with *very large-scale integrated* (VLSI) processes. The gate oxide was 50 nm. The channel thickness was less than 20 nm. The point-contact region width was less than 30 nm. Unfortunately, the authors do not show SEM images of the working devices. They declare that point-contact MOSFETs show the usual behavior until 30 nm in width and that the Coulomb blockade effects were observed when the width decreased beyond that point.[52] In 2002, the same research group published SEM images

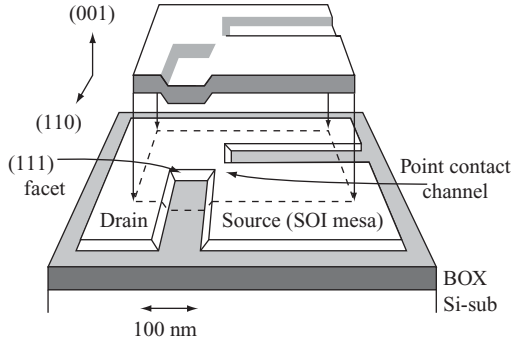


Figure 9.4 Scheme of principle for SET fabrication by means of point-contact MOSFET geometry. (Reprinted from Ref. 52, copyright 1997, with permission from the American Institute of Physics.)

showing clear point-contact regions presenting widths below 30 nm,[53] as shown in Fig. 9.5. They also suggested another etching to further decrease the point-contact region in the MOSFET. The region is narrowed and thinned with a further isotropic etching by using a solution made with $NH_4OH/H_2O_2/H_2O$, and successive removal of the formed oxide by HF.[53] An increase in peak conductance was obtained after this second etching step. They were able to show NDR on drain current upon gate voltage[54] and drain voltage.[55] Finally, they obtained

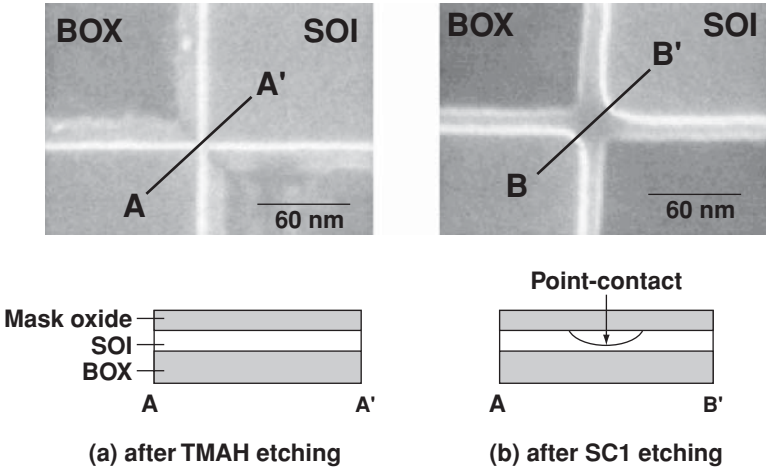


Figure 9.5 SEM images of point-contact MOSFETs, with cross-sectional schematic views of the etching processes. Etching processes carried out (*a*) by using tetramethylammonium hydroxide (TMAH), and (*b*) by using $NH_4OH/H_2O_2/H_2O$ (SC1). (Reprinted from Ref. 53, copyright 2002, with permission from American Institute of Physics.)

an ultranarrow channel having width less than 10 nm.[55] With such narrow structures, it was possible to observe large regions of blockade rarely observed before, even at low temperature. The appearance of Coulomb blockade clearly indicates that the ultranarrow channel has substructures behaving as quantum dots. However, the reason why this channel is constituted by dots was not immediately clear.[52] A silicon dot and two tunneling barriers are self-formed in the narrow point-contact region.[53] This may be due to gate formation processes. After the removal of the oxide required for etching, a 30-nm-thick gate oxide is formed by low-pressure chemical vapor deposition by using conventional fabrication techniques.[53] A polysilicon gate electrode is deposited by ion implantation. A too-long oxidation time seems to create a discontinuity in the ultranarrow channel.[54] However, the phenomenon of dot self-formation in the point-contact channel region is still not clearly understood, and further investigations are required. Some uncontrolled processes may act during gate ion implantation, like those observed in *focused ion beam* (FIB) lithography[56] or in the *chemical vapor deposition* (CVD) of silicon nanoclusters. In fact, a SET has been obtained by using electron beam lithography and successive RIE on a 20-nm-thick source-drain channel of nanocrystalline silicon formed by using plasma-enhanced CVD.[57] The fabricated structure was similar to that shown in Fig. 9.2*A*, but the width W and the length L_f were both equal to 20 nm. *Transmission electron microscopy* (TEM) and Raman spectroscopy have shown that the nanoclusters were typically 4 to 8 nm in size and that they are embedded in an amorphous silicon matrix. A clear Coulomb staircase was published in 2003, in which the tunneling barrier formation around the nanocrystalline silicon was engineered by means of a high-temperature annealing process.[57] A room-temperature staircase in drain-current/gate-voltage characteristic has been also observed in self-assembled silicon quantum dots formed by low-pressure CVD,[58] and Coulomb blockade has been measured in highly uniform silicon quantum dots obtained by using digital-CVD in order to pulse gas into the plasma.[59]

To complete the range of possibilities for building room-temperature SETs with silicon technology, we further consider constrictions in source-drain channels. We have seen in the previous section as accumulation quantum dot can exist in CMOS structures even simply by large enough access resistances along the channel.[26] Therefore, it is possible to realize SETs operating at room temperature by decreasing the size of structures like those shown in Fig. 9.1. Access resistance variations along a 16-nm-width channel have been obtained by using electron beam lithography and further RIE removal, thanks to noise present in the e-beam.[60] Electron-beam lithography may be also used to sculpt a quantum dots in silicon. Figure 9.6 presents a nanopillar formed within a silicon channel. The room-temperature conductance of this device was attributed to some resonance Coulomb

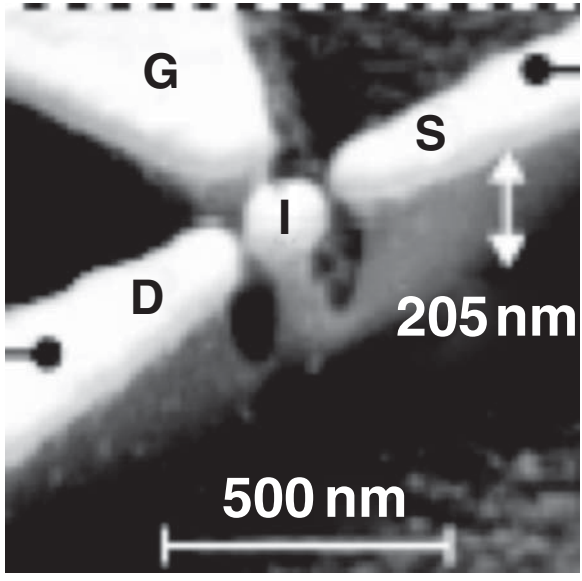
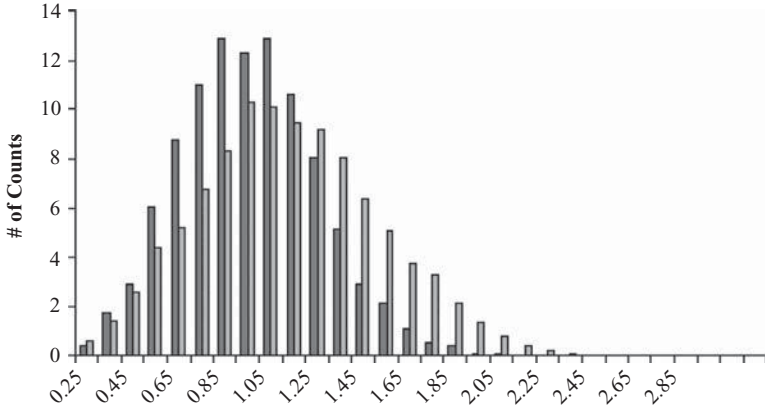


Figure 9.6 SEM image of a resonant Coulomb-force device obtained by nanopillars fabricated using electron-beam lithography and RIE. (Reprinted from Ref. 61, copyright 2004, with permission from the American Institute of Physics.)

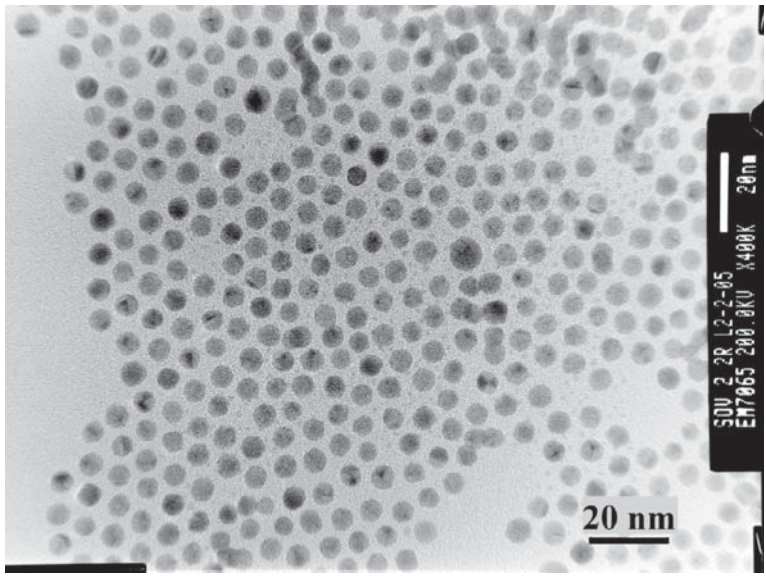
force acting along the channel, although the usual features related to Coulomb blockade were not observed because the pillar was not small enough.[61]

9.4 Room-Temperature Organic Transistors

Single-electron transistors may also be fabricated by using organic nanoparticles. Thiolated gold nanoparticles may be prepared by following the modified version of the Brust method[62] as described in Ref. 63. Particles of different size, with average radius in the range between 1 nm and 5 nm, are fabricated by appropriately changing the synthesis conditions. For example, to obtain a particle core radius of 1 nm, the following reaction conditions are chosen: 1:1 dodecanethiol:$AuCl_4$ mole ratio; fast delivery of the $NaBH_4$ reducing agent (10 s); reaction time of 3 h after reducing agent addition. All processing steps are performed at room temperature. The vapor transfer technique[64] is used to further narrow down the particle size distribution, as shown in Fig. 9.7*A*. For that, acetone is slowly added to a saturated toluene solution by passive vapor transfer, until the solution volume is increased by 50%. The solution is then isolated, and after an extended equilibration period with stirring, centrifuged and finally decanted to remove



(*A*)



(*B*)

Figure 9.7 (*A*) Histogram showing the effect of radius narrowing by using the vapor transfer techniques on a nanoparticles sample, and (*B*) TEM image of a sample of 5-nm particles. (Reprinted from Ref. 66, copyright 2006, with permission from IEEE.)

the soluble fraction. This procedure is repeated several times. Final results are examined for cluster core distribution determination by using TEM, as shown in Fig. 9.7*B*. The nanoparticles thus prepared may be also investigated by *atomic force microscopy* (AFM).[65] Obviously, AFM and TEM imaging returns a local investigation of the considered samples, whereas *small-angle x-ray scattering* (SAXS) experiments are used for information on the whole monodisperse nanoparticle solution. The average radius of the particles is measured, because the SAXS experiments are performed on a millimeter-sized region of the solution and not on a nanometric area of a TEM grid. Moreover, TEM measurements show only the radius of the metallic core, whereas SAXS spectra give information about the total particle size, including the organic surrounding coating.[66] The linearity of the spectra shape in SAXS confirms that the sample contains monodisperse nanoparticles.

These monodisperse nanoparticles were used to fabricate organic SET by placing a single particle in between tunneling barriers. To get such a two-tunneling-barrier system, electrical contacts with gaps close to a very few nanometers have to be fabricated. An electrochemical method to form nanocontacts may be used to erode nanocontacts on an 80- to 200-nm-thick gold layer deposited by thermal evaporation onto a Si/SiO_2 chip with 5 nm of titanium as the stick layer. This method for obtaining nanometer gaps has been called ELENA (electrochemical nanodeposition) by Céspedes et al.[67] It has been used to fabricate metallic electrodes with a separation on the nanometer scale. The method is based on previous experiments by Morpurgo and coworkers, who proposed a two-step process.[68] The method was also successfully tested by other authors.[69,70] It may be used for electrochemical erosion, but also for materials deposition, as schematically shown in Fig. 9.8. Toward this aim, an electrochemical cell was

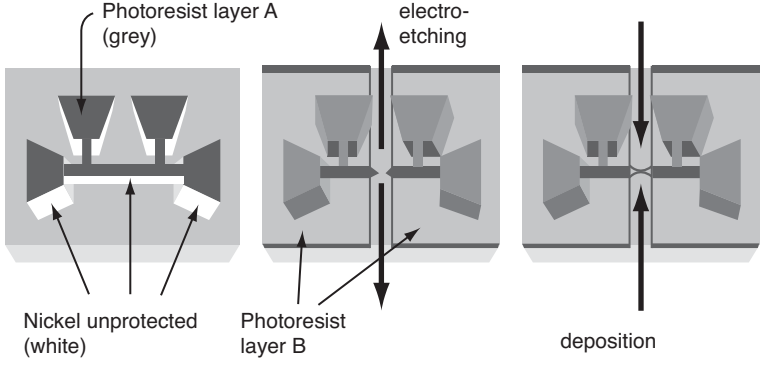


Figure 9.8 Schematic drawings of electrochemical erosion/deposition process. A separation can be formed in a wire by using this method. The formed gap can be closed by reversing the electrochemical potential. (Reprinted from Ref. 46, copyright 2005, with permission from Elsevier.)

organized onto a region of the gold layer deposited by thermal evaporation. The counterelectrode was a platinum wire. The etching solution was chloride acid or *aqua regia* diluted in water (1:3). Aqua regia is an extremely powerful acid mixture commonly used for dissolving noble metals and composed of three parts of concentrated hydrochloric acid and one part of concentrated nitric acid. Etching voltage equal to 2.0 V was used. An automatic system was used to switch to zero the etching voltage to stop the process exactly when the nanogap was formed in between the conducting layer. The measured current flowing between the pads just before the complete circuit interruption usually revealed quantized conductance, as shown in Fig. 9.9*A*. This quantized conductivity proved that a nanometer-sized contact was forming. After the nanogap fabrication, the transistor needed to be completed by insertion of the quantum dot in between the gap. To locate a nanoparticle in between, a toluene solution of monodisperse nanoparticles was deposited by drop casting onto the fabricated nanocontacts. Samples prepared in this way were immediately used for electrical characterization. All the measurements were performed at room temperature. The current/voltage characteristics registered onto such nanostructures present a well-defined current blockade across zero voltage, as shown in Fig. 9.9*B*. Current depressions around zero voltage like that shown in Fig. 9.9*B* are the proof that single-electron trapping is occurring into the organic nanoparticles.[75] From the equation of the threshold voltage,[76]

$$V_{threshold} = \frac{e}{C} \tag{9.2}$$

it is easy to estimate the equivalent dot capacitance, which is in the range of 0.1 aF. This value fits the particle size quite well. The expected capacitance of a single nanoparticle may be calculated from its size by[74]

$$C = 2\pi\varepsilon_0\varepsilon_r R. \tag{9.3}$$

If ε_r is the dielectric constant of the thiol coating and $R = 1$ nm is the gold core radius (see Fig. 9.7*A*), then the capacitance from Eq. (9.3) is equal to 0.26 aF, the same order of magnitude as that calculated from the current-voltage blockade in Fig. 9.9*A*. A wider characterization performed by also using the gate potential further confirmed the single-electron trapping phenomenon and showed 3D curves similar to those in Fig. 9.3*B*, but acquired at room temperature.[66] The gate potential was provided either by using the back gate or by fabricating a gate on the top of the organic nanostructure. In this case, staircases or negative resistance regions corresponding to single-electron trapping

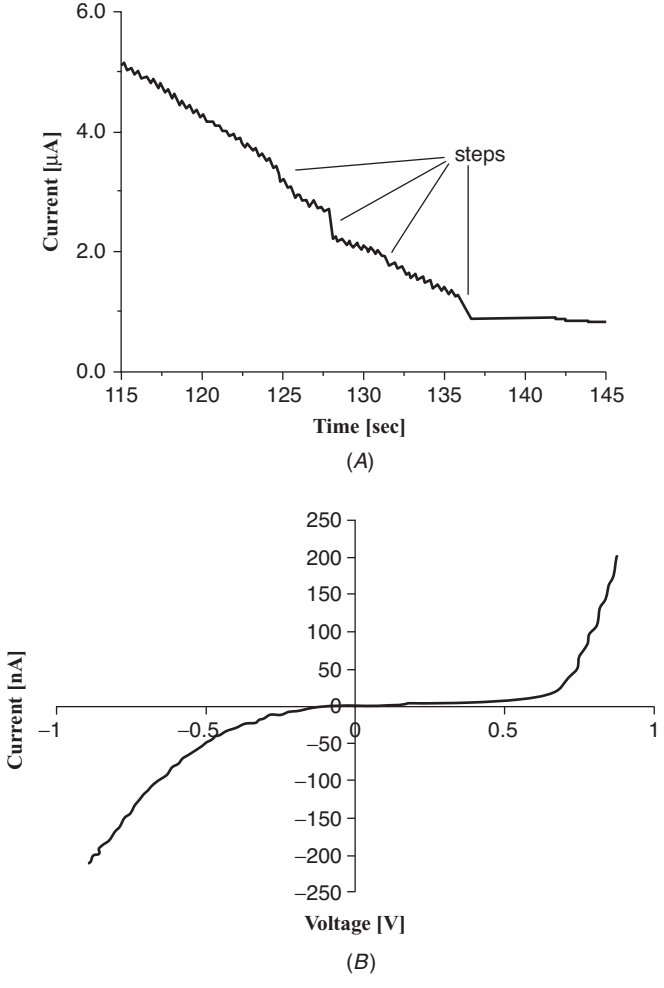


Figure 9.9 (*A*) Current versus time registered during electrochemical erosion of a connection between two pads to form a nanogap. (*B*) Evident Coulomb blockade measured on the formed nanogap after the insertion of a gold nanoparticle in between. (Reprinted from Ref. 66, copyright 2006, with permission from IEEE.)

were clearly observed in the drain-source current versus the source-drain voltage and the gate voltage. The top gate was obtained by depositing evaporated gold onto an insulating polymeric film obtained by Langmuir-Blodgett deposition onto the nanocontacts after the particle drop casting. The acquired curves have shown regions of current suppression due to Coulomb blockade, as evidenced by the revealing terraces in the 3D graph. Of course, nanocontact fabrication by using

electro-erosion may represent a huge drawback for mass production of organic SETs. For mass production, nanotip and nanocontact fabrication may be obtained by using x-ray lithography and synchrotron radiation sources.[71]

9.5 Room-Temperature Memories with Organic SETs

Thiolated gold nanoparticles in between microcontacts were also considered to investigate possible applications of organic quantum dots to SET-based memories. Standard UV lithography and subsequent evaporation of metallic thin films has been used to build up gold microcontacts onto a p-doped silicon wafer with a 1-μm-thick thermally grown oxide provided with a titanium back gate layer. The procedure follows standard, well-known processes.[72] The contact arrays were designed with the purpose of organizing a predetermined number of nanoparticles between surface electrodes. A variety of contacts in the array were made to test both three-terminal field-effect transistors and five-terminal devices (four pads and one gate) that allow four-point measurements. The substrates were treated with silane in order to improve nanoparticle deposition. The silanization was performed by following a well-known procedure.[73] The substrates were cleaned for 15 min in toluene, and then for 20 min in a water solution of hydrogen peroxide and ammonia (5:1:1) at 70°C. Then, the samples were immersed for 4 min in a solution of 3-aminopropyltriethoxysilane; finally, they were rinsed and sonicated in toluene. After the silanization, a toluene solution of nanoparticles was deposited by drop casting between the microelectrodes. Measurements at room temperature on these structures have shown hysteresis similar to that in Fig. 9.10. This hysteresis

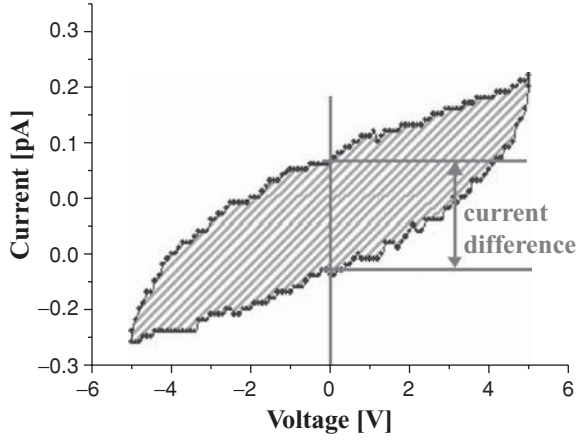


Figure 9.10 Area and current-difference near zero voltage for hysteretic cycles. (Reprinted from Ref. 66, copyright 2006, with permission from IEEE.)

may be modeled by accounting for different parameters. Two main parameters were considered: the current difference between the back and forward voltage, and the cycle area, as schematically shown in Fig. 9.10. The current flowing across the connections is affected by the nanoparticle multilayer in between. The parameters of the single cycle also vary one order of magnitude with solution concentrations. Figure 9.11*A* reports data from measurements on a sample prepared by using an initial drop with different nanoparticle concentrations. The current increases as the solution concentration increases, and the hysteretic

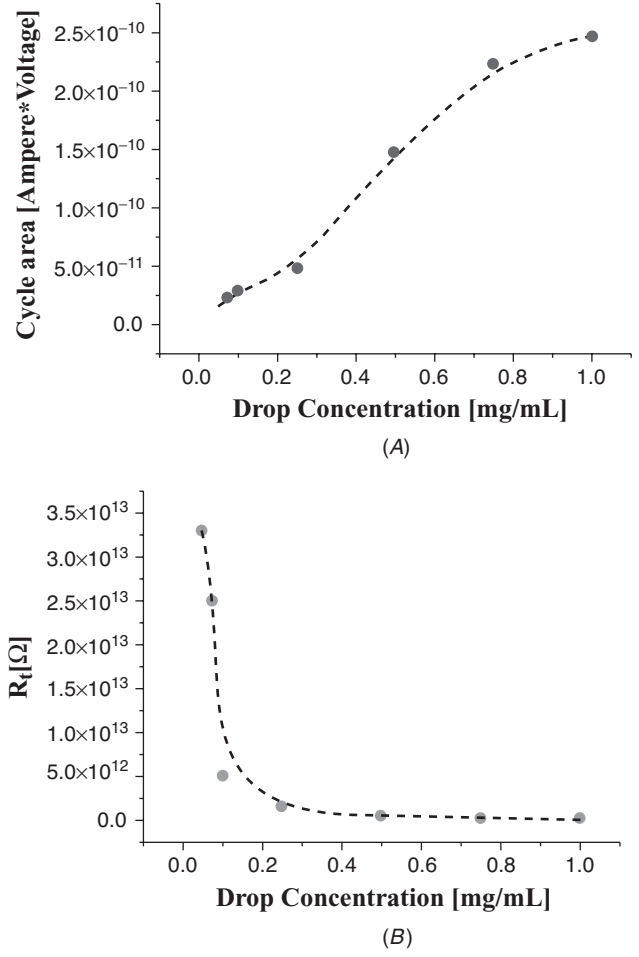


Figure 9.11 Trends of area (*A*) and tunneling resistance (*B*) calculated from hysteretic cycles on concentrations of nanoparticles in drops cast to form an organic quantum-dot film. (Reprinted from Ref. 66, copyright 2006, with permission from IEEE.)

area also increases while the cycle shape narrows. The transient of current increases with concentration in response to voltage steps as well. Both these currents are related to the average nanoparticle film tunneling resistance. The average tunneling resistance of the samples may be defined as[74]

$$R_t = \frac{dV}{dI} \tag{9.4}$$

Figure 9.11 also reports the behavior of the tunneling resistance calculated on the hysteresis cycles as a function of the drop concentration. Very similar results have been obtained on voltage step response.[66] These behaviors are consistent with the interpretation that the metal-organic nanoparticles are acting as quantum dots in the interconnections. Data have also shown an increased capacity to store electric charge with increasing particle number. This means that when the number of dots in the organic connection grows, more electrons are charged inside. Moreover, if a great number of closely packed dots lie in the organic connections, the tunneling distance between the nanoparticles decreases, so that the tunneling resistance of the organic interconnections decreases, and the tunneling current through the film increases. A more precise analysis of the average capacitance value of the nanoparticles film in between the micro-contacts may be used to confirm that each single particle is acting as individual quantum dots in these structures. Table 9.1 reports the capacitance values for the capacitance of the nanoparticle films as calculated by response to a voltage step on the drop concentrations used for film fabrication. The average radius of the nanoparticles used was 2 nm, and the available area in between the electrodes was 3 μm $\times$ 2 μm. A sample prepared with a concentration of 1 mg/ml results in many layers of nanoparticles, whereas a sample made with a concentration of 0.05 mg/mL corresponds to a single monolayer. Equation (9.3) gives a value equal to 0.39 pF for the total capacitance of such a single monolayer. This value is fairly near to that in Table 9.1 for 0.05 mg/ml. This is direct proof that the organic particles are acting as quantum dots in the net created by the monolayer in between the electrodes. Moreover, Eq. (9.1)

Concentration [mg/ml]	1	0.75	0.5	0.25	0.1	0.075	0.05
Capacitance [pF]	230	225	69.2	13.3	0.715	0.432	0.384

Table 9.1 Values of the Equivalent Average Capacitance for Nanoparticle Films as Estimated by Voltage-Step Response on Drop Concentrations Used for Film Fabrication

gives us the correct ratio between electrostatic and thermal energies to obtain single-electron trapping at room temperature within particles with 2 nm of radius.

9.6 The Patents

To show the relevance to industry of the work done during the past 20 years on single-electron technology, a brief overview of patents is given in this section. This worldwide competition showed the great effort of many industrial entities. For example, Sharp, Hitachi, NEC, Texas Instruments, the Korean Electronics Telecomm, and the Japanese Nippon Telegraph and Telephone Corporation contributed toward it. This challenge first began in the 1990s, and it is still ongoing.

Among the proposed technologies, many do not correspond to devices sufficiently robust and reliable for use in commercial products. The sizes required by such technologies are sometimes prohibitive to be reached in a production line, and the fabrication costs for a single transistor are often too high. However, the scaling down of the production technology for CMOS chips, currently at the 90-nm node, suggests the feasibility of many proposed solutions in the near future. The first industry to address this field was NEC, in June 1993, with a Japanese patent.[77] In this patent, two opposite electrodes are connected by means of a conducting wire embedded in a film. The next year, in October, with another Japanese patent, Hitachi protected an invention that concerned a quantum-dot based architecture.[78] In the same year, Nippon Telegraph and Telephone Corporation came out with a similar patent,[79] but the structure sizes involved were too wide to ensure room-temperature operation. In a 1995 patent by Japanese Matsushita, with a request for U.S. patent in 1997, the potentiality to obtain organized structures of proteins with a step of only 0.15 nm was envisaged to overcome the size limitations of SETs at room temperature.[80] The first work based on silicon dioxide and polycrystalline silicon appeared with a patent by Toshiba in September 1998,[81] in which the problem of the too-large size was tackled by using high-cost methods such as STM,[82] AFM,[83,84] and FIB lithography,[85] and by using multilayer structures of about 100 nm.[86]

Since 2000, a great increase in patent activity has taken place, benefiting from new opportunities offered by scientific and technological research. Among these, it is worth citing the possibility of obtaining quantum dots from different sources: from molecules stabilized with thiols, patented by Sharp in April 2001[87]; from ion impurities, patented by Hyundai in the same month[88]; and from nanometric pores obtained by electrochemical etching in a silicon matrix, patented by Samsung in 2002.[89,90] Texas Instruments protected its results in the field of SET with the contribution of two independent groups: in 2001

the group of Shye-Lin Wu, based in Taiwan, showed structures with silicon nanowires,[91] and in 2002 the group of Christoph Wasshuber, based in Texas, showed structures with pairs of electrically coupled granules.[92] These patents protected the idea of using granules for electron trapping[91], and the idea of measuring trapping conditions.[92]

More recently, the challenge has shifted to obtaining nanostructures enabling SETs to operate at room temperature. Recent works have been devoted to alternative technologies: nanometric islands based on silicon dioxide,[93] nanoparticles,[94] self-assembly,[95] and various functional groups of alkanes.[96] These last works have been focused on island size, whereas the critical problem of how to provide suitable electrical contacts between the small island and the two electrode pairs began to be addressed with a patent in December 2004.[97] Applications of SETs to memory (e.g., Refs. 91, 92, 97) and metrology[99] were finally considered. This very broad activity and the large number of documents present in international patent databases demonstrate the continuous effort of the electronic industry toward a feasible technology to exploit research in SET devices.

9.7 Conclusions

In this chapter, we have seen various ways to fabricate a device presenting all the characteristics of a single-electron transistor. We have also seen applications of organic materials for transistors and memories by showing data from structures made by gold nanoparticles stabilized by a thiol coating. These particles were synthesized with sizes in the range of 1 to 5 nm. They were considered in thin films between micro- and nanocontacts with the aim of investigating different interconnection lengths and different possible applications. In all cases, the nanoparticles in the organic films were acting as quantum dots, storing charge by trapping single electrons.

Hence, the possibility has been demonstrated of obtaining single-electron conductivity by fabricating organic films with metallic nanoparticles with sizes below 10 nm. The reported data confirm that organic materials of such a size could be employed to develop transistors and/or memories based on single-electron phenomena. The key factor for construction of these devices remains to build up a very small space region enabling single-electron confinement. Room-temperature operation requires island sizes of less than a very few nanometers. This size limitation is still out of reach of the present UV lithography.

However, it is possible to fabricate organic or inorganic SETs working at room temperature. The obtained point-contact devices have shown behavior clearly related to single-electron trapping, and they may be fabricated, in principle, by using some industrially available

processes. For example, SETs fabrication is possible by using focused ion beams to obtain quantum-dot islands in metallic structures[100] or in carbon nanotubes.[101] Quantum islands have been formed with organometallic nanoparticle chains.[102] Nanocontacts have been realized by means of electron-beam lithography,[103] and nanotips by synchrotron radiation source x ray.[71] Emerging technologies such as nanoimprinting,[104] electrochemical etching and deposition,[68] crossed nanowires,[105] and molecular assembly[106] may also provide interesting solutions for single-electron devices. However, the CMOS industry needs methodologies that are completely compatible with industrial fabrication processes. For that, point-contact MOSFETs made with silicon material have the highest probability of being included in future in CMOS production.

Acknowledgments

Alexander Korotkov is acknowledged for his kindness in providing some references. Daniele Caviglia is greatly acknowledged for useful discussions on nanocontact fabrications. Dino Albini is acknowledged for the proofreading of the final manuscript.

References

1. M. Leong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, "Silicon device scaling to the sub-10-nm regime," *Science*, vol. 306, pp. 2057-2060, 2004.
2. M. T. Bohr, "Nanotechnology goals and challenges for electronics applications," *IEEE Transactions on Nanotechnology*, vol. 1, pp. 56-62, 2002.
3. R. Chau, "Advances metal gate/high-*k* dielectric stacks for high-performance CMOS transistors," in *Proceedings of the American Vacuum Society, 5th International Conference on Microelectronics and Interfaces (ICMI), Santa Clara, March 2004*, pp. 1-3, 2004.
4. J. Camargo Da Costa, J. Hoekstra, M. J. Goosseng, C. J. M. Verhoeven, and A. H. M. Van Roermund, "Consideration about nanotechnology GSI processors," *Analog Integrated Circuits and Signal Processing*, vol. 124, pp. 59-71, 2000.
5. A. Schmid and Y. Leblebici, "Robust circuit and system device methodologies for nanometer-scale devices and single-electron transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 112, pp. 1156-1166, 2004.
6. C. Fenouillet-Beranger, T. Skotnicki, S. Monfray, N. Carriere, and F. Boeuf, "Requirements for ultra-thin-film devices and new materials for the CMOS roadmap," *Solid-State Electronics*, vol. 148, pp. 961-967, 2004.
7. S. M. Goodnick and J. Bird, "Quantum-effect and single-electron devices," *IEEE Transactions on Nanotechnology*, vol. 14, pp. 368-385, 2003.
8. M. I. Lutwyche and Y. Wada, "Estimate of the ultimate performance of the single-electron transistor," *Journal of Applied Physics*, vol. 175, pp. 3654-3661, 1994.
9. N. Y. Yama, S. Muto, K. Ikamura, M. Takatsu, T. Mori, Y. Sugiyama, et al., "Quantum functional device for advanced electronics," *Solid-State Electronics*, vol. 140, pp. 505-511, 1996.
10. M. J. Hostetler, J. E. Wingate, C.-J. Zhong, J. E. Harris, R. W. Vachet, M. R. Clark, et al., "Alkanethiolate gold clusters molecules with core diameters from 1.5 to

5.2 nm: core and monolayer properties as a function of core size," *Langmuir*, vol. 114, pp. 17-30, 1998.
11. S. T. Pantelides, M. Di Ventra, N. D. Lang, and S. N. Rashkeev, "Molecular electronics by the numbers," *IEEE Transactions on Nanotechnology*, vol. 1, pp. 86-90, 2002.
12. D. R. Stewart, D. A. A. Ohlberg, P. A. Beck, Y. Chen, R. Stanley Williams, J. O. Jeppensen, et al., "Molecule-independent electrical switching in Pt/organic monolayer/Ti devices," *Nano Letters*, vol. 4, pp. 133-136, 2004.
13. K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," *Nature*, vol. 433, pp. 47-50, 2005.
14. R. F. Service, "Next-generation technology hits an early midlife crisis," *Science*, vol. 302, pp. 556-559, 2003.
15. A. N. Korotkov, "Coulomb blockade and digital single-electron devices," in *Molecular Electronics*, J. Jortner and M. A. Ratner, editors, Oxford, UK, Blackwell, 1997.
16. H. Ahmed and K. Nakazato, "Single-electron devices," *Microelectronic Engineering*, vol. 32, pp. 297-315, 1996.
17. K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, pp. 606-632, 1999.
18. P. J. M. van Bentum, H. van Kempen, L. E. C. van de Leemput, and P. A. A. Teunissen, "Single-electron tunneling observed with point-contact tunnel junction," *Physics Review Letters*, vol. 60, pp. 369-372, 1988.
19. P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, and M. H. Devoret, "Direct observation of macroscopic charge quantization," *Zeitschrift für Physik B: Condensed Matter*, vol. 85, pp. 327-332, 1991.
20. M. H. Devoret, D. Esteve, and C. Urbina, "Single-electron transfer in metallic nanostructures," *Nature*, vol. 360, pp. 547-553, 1992.
21. D. V. Averin and K. K. Likharev, "Coulomb blockade of single-electron tunneling, and coherent oscillations in small tunnel junctions," *Journal of Low-Temperature Physics*, vol. 62, pp. 345-373, 1986.
22. S. Carrara, V. Erokhin, P. Facci, and C. Nicolini, "On the role of nanoparticle sizes in monoelectron conductivity," in *Nanoparticles in Solids and Solutions*, J. Fendler and I. Dékány, editors, NATO ASI Series 3, *High Technology*, vol. 18, pp. 497-503, Dordrecht, The Netherlands, Kluwer, 1996.
23. L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, "Double-dot charge transport in Si single-electron/hole transistors," *Applied Physics Letters*, vol. 76, pp. 1591-1593, 2000.
24. T. Sakamoto, H. Kawaura, and T. Baba, "Single-electron transistors fabricated form a doped-Si film in a silicon-on-insulator substrate," *Applied Physics Letters*, vol. 72 , pp. 795-796, 1998.
25. Q. Tilke, R. H. Blick, and H. Lorenz, "Fabrication and integration possibilities of ultrasmall quantum dots in silicon-on-insulator materials," *Journal of Applied Physics*, vol. 90, pp. 942-946, 2001.
26. X. Jehl, M. Sanquer, G. Bertrand, G. Gugan, S. Deleonibus, and D. Fraboulet, "Silicon single electron transistors with SOI and MOSFET structures: the role of access resistances," *IEEE Transactions on Nanotechnology*, vol. 2, pp. 308-313, 2003.
27. Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, et al., "Fabrication Method for IC-Oriented Si Single-Electron transistors," *IEEE Transactions on Electron Devices*, vol. 47, pp. 147-153, 2000.
28. A. Notargiacomo, L. Di Gaspare, G. Scappucci, G. Mariottini, F. Evangelisti, E. Giovine, et al., "Single-electron transistor based on modulation-doped SiGe heterostructures," *Applied Physics Letters*, vol. 83, pp. 302-304, 2003.
29. A. Notargiacomo, L. Di Gaspare, G. Scappucci, G. Mariottini, E. Giovine, R. Leoni, et al., "A single electron transistor based on SiGe wires," *Materials Science and Engineering*, vol. C23, pp. 671-673, 2003.
30. D. H. Kim, S.-K. Sung, K. R. Kim, J. D. Lee, B.-G. Park, B. H. Choi, et al., "Silicon single-electron transistors with sidewall depletion gates and their

application to dynamic single-electron transistor logic," *IEEE Transactions on Electron Devices*, vol. 49, pp. 627-635, 2002.
31. Y. Zhang, F. A. Baron, K. L. Wang, and Z. Krivokapic, "Complementary single-electron/hole action of nanoscale SOI CMOS transistors," *IEEE Electron Device Letters*, vol. 25, pp. 492-494, 2004.
32. L. Rotkina, J.-F. Lin, and J. P. Bird, "Nonlinear current-voltage characteristics of Pt nanowires and nanowire transistors fabricated by electron-beam deposition," *Applied Physics Letters*, vol. 83, pp. 4426-4428, 2003.
33. N. Yoneya, E. Watanabe, K. Tsukagoshi, and Y. Aoyagi, "Coulomb blockade in multiwalled carbon nanotube island with nanotube leads," *Applied Physics Letters*, vol. 79, pp. 1465-1467, 2001.
34. M. Ahlskog, R. Tarkiainen, L. Rochier, and P. Hakonen, "Single-electron transistor made of two crossing multiwalled carbon nanotubes and its noise properties," *Applied Physics Letters*, vol. 77, pp. 4037-4039, 2000.
35. A. Kanda, Y. Ootuka, K. Tsukagoshi, and Y. Aoyagi, "Electron transport in metal/multiwall carbon Nanotubes/metal structures (metal = Ti or Pt/Au)," *Applied Physics Letters*, vol. 79, pp. 1354-1356, 2001.
36. S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley, L. J. Geerligs, et al., "Individual single-walled carbon nanotubes as quantum wires," *Nature*, vol. 386, pp. 474-477, 1997.
37. J. Kong, C. Zhou, E. Yenilmez, and H. Dai, "Alkaline metal-doped n-type semiconductor nanotubes as quantum dots," *Applied Physics Letters*, vol. 77, pp. 3977-3979, 2000.
38. T. Wagner, W. Krech, B. Frank, H. Mühlig, H.-J. Fuchs, and U. Hübner, "Fabrication and measurements of metallic single electron transistors," *IEEE Transactions on Applied Superconductivity*, pp. 4277-4280, 1999.
39. M. Sillanpää, J. S. Pentilä, M. A. Paalanen, and P. J. Hakonen, "Transport measurements in SISNSIS single-electron transistors," *Physica B*, vol. 284, pp. 1826-1827, 2000.
40. K. L. Bolotin, F. Kuemmeth, A. N. Pasupathy, and D. C. Ralph, "Metal-nanoparticle single-electron transistors fabricated using electromigration," *Applied Physics Letters*, vol. 84, pp. 3154-3156, 2004.
41. H. Park, A. K. L. Lim, A. P. Alivisatos, J. Park, and P. L. McEuen, "Fabrication of metallic electrodes with nanometer separation by electromigration," *Applied Physics Letters*, vol. 75, pp. 301-303, 1999.
42. S. H. M. Persson, L. Olofsson, and L. Gunnarson, "A self-assembled single-electron tunneling transistors," *Applied Physics Letters*, vol. 74, pp. 2546-2548, 1999.
43. H.-M. So, J. Kim, W. S. Yun, J. W. Park, J.-J. Kim, D. J. Won, et al., "Molecule-based single electron transistor," *Physica E*, vol. 18, pp. 243-244, 2003.
44. T. Junno, M. H. Magnusson, S.-B. Carlsson, K. Deppert, J.-O. Malm, L. Montelius, et al., "Single-electron devices via controlled assembly of designed nanoparticles," *Microelectronic Engineering*, vol. 47, pp. 179-183, 1999.
45. S.-B. Carlsson, T. Junno, L. Montelius, and L. Samuelson, "Mechanical tuning of tunneling gaps for the assemble of single-electron transistors," *Applied Physics Letters*, vol. 75, pp. 1461-1463, 1999.
46. S. Carrara, J. Riley, V. Bavastrello, E. Stura, and C. Nicolini, "Review: Methods to fabricate nanocontacts for electrical addressing of single-molecules," *Sensors and Actuators B: Chemical*, vol. 105, pp. 542-548, 2005.
47. C. Schonenberger, H. van Houten, H. C. Donkersloot, A. M. T. van der Putten, and L. G. J. Fokkink, "Single-electron tunneling up to room temperature," *Physica Scripta*, vol. T45, pp. 289-293, 1992.
48. V. Erokhin, P. Facci, S. Carrara, and C. Nicolini, "Observation of room temperature mono-electron phenomena on nanometer-Sized CdS particles," *Journal of Physics D: Applied Physics*, vol. 28, pp. 1-5, 1995.
49. P. Facci, V. Erokhin, S. Carrara, and C. Nicolini, "Room temperature single electron element," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 93, pp. 10556-10559, 1996.

50. S. Carrara, V. Bavastrello, M. K. Ram, and C. Nicolini, "Nanometer size polymer based Schottky junction," *Thin Solid Films*, vol. 510, pp. 229-234, 2006.
51. A. Alessandrini, M. Salerno, S. Frabboni, and P. Facci, "Single-metalloprotein wet biotransistor," *Applied Physics Letters*, vol. 86, pp. 133902-133906, 2005.
52. H. Ishikuro and T. Hiramoto, "Quantum mechanical effects in the silicon quantum dot in a single-electron transistor," *Applied Physics Letters*, vol. 71, pp. 3691-3693, 1997.
53. M. Saitoh and T. Hiramoto, "Observation of current staircase due to large quantum level spacing in a silicon single-electron transistor with low parasitic series resistance," *Journal of Applied Physics*, vol. 91, pp. 6725-6728, 2002.
54. M. Saitoh, T. Murakami, and T. Hiramoto, "Large Coulomb blockade oscillations at room temperature in ultranarrow wire channel MOSFETs formed by slight oxidation process," *IEEE Transactions on Nanotechnology*, vol. 2, pp. 241-244, 2003.
55. M. Saitoh and T. Hiramoto, "Extension of Coulomb blockade region by quantum confinement in the ultrasmall silicon dot in a single-hole transistor at room temperature," *Applied Physics Letters*, vol. 84, pp. 3172-3194, 2004.
56. T. W. Kim, D. C. Choo, J. H. Shim, and S. O. Kang, "Single-electron transistors operating at room temperature, fabricated utilizing nanocrystals created by focused-ion beam," *Applied Physics Letters*, vol. 80, pp. 2168-2170, 2002.
57. Y. T. Tan, T. Kamiya, Z. A. K. Durrani, and H. Ahmed, "Room temperature nanocrystalline silicon single-electron transistors," *Journal of Applied Physics*, vol. 94, pp. 633-637, 2003.
58. B. H. Choi, S. W. Hwang, I. G. Kim, H. C. Shin, Y. Kim, and E. K. Kim, "Fabrication and room temperature characterization of a silicon self-assembled quantum-dot transistor," *Applied Physics Letters*, vol. 73, pp. 3219-3131, 1998.
59. A. Dutta, S. Oda, Y. Fu, and M. Willander, "Electron transport in nanocrystalline Si based single electron transistors," *Japan Journal of Applied Physics*, vol. 39, pp. 4647-4650, 2000.
60. L. Zhuang, L. Guo, and S. Y. Chou, "Silicon single-electron quantum-dot transistor switch operating at room temperature," *Applied Physics Letters*, vol. 72, pp. 1205-1207, 1998.
61. D. V. Scheible and R. H. Blick, "Silicon nanopillars for mechanical single-electron transport," *Applied Physics Letters*, vol. 84, pp. 4632-4634, 2004.
62. M. Brust, M. Walker, D. Bethell, D. J. Schiffrin, and R. Whyman, "Synthesis of thiol-derivatised gold nanoparticles in a two-phase liquid-liquid system," *Journal of the Chemical Society, Chemical Communications*, p. 801, 1994.
63. M. J. Hostetler, J. E. Wingate, C.-J. Zhong, J. E. Harris, R. W. Vachet, M. R. Clark, et al., "Alkanethiolate gold cluster molecules with core diameters form 1.5 to 5.2 nm: core and monolayer properties as a function of core size," *Langmuir*, vol. 14, p. 17, 1998.
64. R. L. Whetten, J. T. Khoury, M. M. Alvarez, S. Murthy, I. Vezmar, Z. L. Wang, et al., "Nanocrystal gold molecules," *Advanced Materials*, vol. 8, p. 428, 1996.
65. F. Sbrana, M. T. Parodi, D. Ricci, and E. Di Zitti, "Langmuir films of thiolated gold nanoparticles transferred onto functionalized substrate: 2-D local organization," *Materials Science and Engineering*, vol. C22, pp. 187-191, 2002.
66. S. Carrara, B. Samorì, M. Di Pasquale, A. Ansaldo, M. T. Parodi, D. Ricci, et al., "Hybrid nanostructures: organic interconnections and device applications," in *Proceedings of the 1st IEEE International Conference on Nano-Networks*, Lausanne, Switzerland, September 14-16, 2006.
67. O. Céspedes, M. A. Bari, C. Dennis, J. J. Versluijs, G. Jan, J. O'Sullivan, et al., "Fabrication and characterization of Ni nanocontacts," *Journal of Magnetism and Magnetic Materials*, vol. 242-245, pp. 492-494, 2002.
68. A. F. Morpurgo, C. M. Marcus, and D. B. Robinson, "Controlled fabrication of metallic electrodes with atomic separation," *Applied Physics Letters*, vol. 74, pp. 2084-2086, 1999.

69. C. Z. Li, H. X. He, and N. J. Tao, "Quantized tunneling current in the metallic nanogaps formed by electrodeposition and etching," *Applied Physics Letters*, vol. 77, pp. 3995-3997, 2000.
70. H. X. He, S. Boussaad, B. Q. Xu, C. Z. Li, and N. J. Tao, "Electrochemical fabrication of atomically thin metallic wires and electrodes separated with molecular-scale gaps, *Journal of Electroanalytical Chemistry*," vol. 522, pp. 167-172, 2002.
71. S. Carrara, D. Ricci, E. Di Zitti, E. Di Fabrizio, M. Altissimo, and M. Tormen, "A route to fabricate nanocontacts by x-ray lithography for the realization of single electron transistors and highly sensitive biosensors," *Materials Letters*, vol. 60, pp. 3682-3685, 2006.
72. A. Ansaldo, D. Ricci, F. Gatti, E. Di Zitti, and S. Cincotti, "Investigating Schottky barriers effects in carbon nanotube FETs," in *Electronic Properties of Novel Nanostructures: XIX International Winterschool/Euroconference on Electronic Properties of Novel Materials, AIP Conference Proceedings, vol. 723*, pp. 570-573, H. Kuzmany, J. Fink, M. Mehring, and S. Roth, editors.
73. D. F. Siqueira Petri, G. Wenz, P. Schunk, and T. Schimmel, "An improved method for the assembly of amino-terminated monolayers on SiO_2 and the vapor deposition of gold layers," *Langmuir*, vol. 15, pp. 4520-4523, 1999.
74. R. Parthasarathy, X.-M. Lin, and H. M. Jaerger, "Electronic transport in metal nanocrystal arrays: the effect of structural disorder on scaling behavior," *Physical Review Letters*, vol. 87, pp. 186807-1, 2001.
75. M. H. Devoret, D. Esteve, and C. Urbina, "Single-electron transfer in metallic nanostructures," *Nature*, vol. 360, pp. 547-553, 1992.
76. V. Erokhin, P. Facci, S. Carrara, and C. Nicolini, "Observation of room temperature mono-electron phenomena on nanometer-sized CdS particles," *Journal of Physics D: Applied Physics*, vol. 28, pp. 1-5, 1995.
77. O. Yukinori, "Manufacture of single electron transistor," Japanese Patent JP5145062., filed November 18, 1991, and issued June 11, 1993.
78. W. Yasuo and M. Ratobitsuchi, "Single-electron transistor," Japanese Patent JP6302806, filed April 14, 1993, and issued October 28, 1994.
79. N. Shunji and M. Takashi, "Single electron transistor," Japanese Patent JP6196720, filed December 25, 1992, and issued July 15, 1994.
80. I. Yamashita, "Single electron transistor using protein," US Patent 5,646,420, with priority on Japanese patents JP19950016857 19950203, filed February 5, 1996, and issued July 8, 1997.
81. O. Tamashiro, "Single-electron transistor and its manufacture," Japanese patent JP10261790, filed March 17, 1997, and issued September 29, 1998.
82. P.; Kang-Ho, H.; Jeong-Sook, Lee; and El-Hang, "Method for manufacturing a single electron transistor by using a scanning tunneling microscopy," US Patent 5,710,051, filed August 8, 1996, and issued January 20, 1998.
83. O. Kimitaka and I. Atshuhusa, "Single-electron transistor and its manufacturing method," Japanese patent JP2001077346, filed September 07, 1999, and issued March 23, 2001.
84. P.; Kang-Ho, H.; Jeong-Sook, and Lee; El-Hang, "Method for manufacturing a single electron transistor by using a scanning tunneling microscopy," US Patent 5,710,051, filed August 8, 1996, and issued January 20, 1998.
85. K., Eun Kyu, P., Young Ju .K., Tae Whan, K., Seung Oun, C., Dong Chul, S., and Jae Hwan, "Fabrication method of single electron tunneling transistors using a focused-ion beam," by Korea Institute of Science and Technology with priority on Korea Patent KR2001036222, filed December 27, 2001, and issued July 4, 2002.
86. Y.; Tsutomu, K.; Sang-Jae "Single electron transistor having multilayer structure," US Patent 6,573,526, filed A, pril 19, 2002, and issued June 3, 2003.
87. O. Kimitaka and I. Atsuhisa, "Single-electron transistor and its manufacturing method thereof," Japanese Patent JP2001119038, filed October 21, 1999, and issued April 27, 2001.

88. P.; Byung Gook, K.; Dae Hwan, "Method for fabricating single electron transistor," US Patent 6,211,013, filed March 17, 2000, and issued April 3, 2001.
89. L.; Jo-won, K.; Chung-woo, K.; Byong-man, and K.; Moon-kyung, "Single electron transistor using porous silicon," US Patent 6,414,333, filed March 10, 2000, and issued July 2, 2002.
90. L.; Jo-won, K.; Chung-woo, K.; Byong-man, and K.; Moon-kyung, "Single electron transistor using porous silicon and manufacturing method thereof," US Patent 6,479,365, filed March 5, 2002, and issued November 12, 2002.
91. W.; Shye-Lin, "Single electron transistor memory array," US Patent 6,204,517, filed April 9, 1998, and issued March 20, 2001.
92. W. Christoph, "Single-electron memory," US Patent 6,487,112, filed November 19, 1999, and issued November 26, 2002.
93. W. Shie-Lin, "Structure and fabrication method for nanometer silicon island of a single electron transistor," Taiwan Patent TW502339, filed June 12, 1998, and issued September 11, 2002.
94. K. Yun Ho, "Single electron transistor using nano particle," Korean Patent KR2003079180, filed April 04, 2002, and issued October 10, 2003.
95. Gil-Ho, "Single electron transistor using strain-induced self-assembled quantum dots," Korean Patent KR2003013192, filed August 7, 2001, still pending.
96. O. Takuji and E. Hiroaki, "Organometallic complex, method for producing the same, and charge retention material and single electron transistor produced by using the complex," Japanese Patent JP2004059552, filed July 31, 2002, and issued February 26, 2004.
97. "New method to fabricate nanometric structures working as SET transistors at room temperature [translation]," Italian Patent Request GE2004A000112, filed July 20, 2004, and still pending
98. L.; Jo-won, K.; Moon-kyung, K.; Byong-man, Y.; Seok-yeol, and R.; Hyung-lae, "MNOS-type memory using single electron transistor and driving method thereof," by Samsung Electronics Corporation, US Patent 6,313,503, filed June 22, 2000, and issued November 6, 2001.
99. J. H., Jefferson; T. J., Phillips, "Single charge carrier transistor, method of holding a charge carrier within a quantum dot, and method of detection," by Qinetiq Ltd, US Patent 6,498,354, filed December 13, 2000, and issued December 24, 2002.
100. T. W. Kim, S. O. Kang, D. C. Choo, and J. H. Shim, "Room-temperature observation of the Coulomb blockade effects in Al two-terminal diodes fabricated using a focused ion-beam nanoparticles process," *Applied Physics Letters*, vol. 76, pp. 1036-1038, 2000.
101. D. Tsuya, K. Ishibashi, M. Suzuki, and Y. Aoyagi, "Local Ar beam irradiation for making tunneling barriers and its application to single electron inverter in multi-wall carbon nanotubes," *Physica E*, vol. 19, pp. 157-160, 2003.
102. T. Sato, H. Ahmed, D. Brown, and B. F. G. Johnson, "Single electron transistor using a molecular linked gold colloidal particle chain," *Journal of Applied Physics*, vol. 82, pp. 696-701, 1997.
103. K. Liu, Ph. Avouris, J. Bucchignano, R. Martel, and S. Sun, "Simple fabrication scheme for sub-10 nm electrodes gaps using electron-beam lithography," *Applied Physics Letters*, vol. 80, pp. 865-867, 2002.
104. A. P. Kam, J. Seekamp, V. Solovyev, C. Clavijo Cedegno, A. Goldshmidt, and C. M. Sotomayor Torres, "Nanoimprinted organic field-effect transistors: fabrication, transfer mechanisms end solvent effects on device characteristics," *Microelectronic Engineering*, vol. 73-74, pp. 809-813, 2004.
105. P. J. Kuekes, D. R. Stewart, and R. S. Williams, "The crossbar latch: logic value storage, restoration, and inversion in crossbar circuits," *Journal of Applied Physics*, vol. 97, pp. 034304-1, 034301-5, 2005.
106. V. Erokhin, T. Berzina, and M. P. Fontana, "Electron beam irradiation for structuring of molecular assemblies," *IEEE Transactions on Nanobioscience*, vol. 3, pp. 6-15, 2004.

This page intentionally left blank

CHAPTER 10

Recent Developments toward the Synthesis of Supramolecular Bioelectronic Nanostructures

John D. Tovar, Stephen R. Diegelmann, and Brian D. Wall

Supramolecular materials derived from the assembly of molecularly well-defined precursors are being applied in many areas of current technology. Their length scales are in a regime not easily accessed through chemical synthesis, lithography, or nanofabrication. Although increasingly small nanostructured components can be fabricated for integrated circuitry, replicating comparable processes in the soft materials domain is very difficult. Self-assembly has emerged as a powerful tool to construct advanced materials from molecular components with pre-programmed interactions that ultimately lead to the formation of defined objects with higher structural order and with lengths in one, two, or three dimensions in the 1 to 100 nm regime. In this chapter, we discuss briefly some of the enthalpic and entropic currencies (as referred to in energy terms of kilocalories per mole) that are exchanged to build supramolecular materials, and then highlight how they can be used collectively to construct novel electronic structures. Organic electronic materials in general are becoming increasingly important for many clinical biomaterials efforts, and the ability to scale their dimensionality down to the nanoscale will lead to many potentially innovative new therapies. We discuss some of the current organic bioelectronic state-of-the-art and then discuss emerging strategies from our laboratory and others to render the organic electronic materials into one-dimensional (1D) nanoscale

fibrils that resemble in part the structural components of the extracellular matrix.

10.1 "Supramolecular Synthons" Used to Construct Self-Assembled Materials

The self-assembly of hierarchically structured objects from molecular precursors comes with a severe entropic penalty because particular conformations must be established in the molecular framework, and degrees of freedom in the system as a whole are lost as multiple molecules come together into defined and, relatively speaking, more ordered objects. However, enthalpic gains in system stability can successfully overcome the entropic costs to provide a net thermodynamic favorability. These enthalpic stabilizations reflect in many cases an electrostatic attraction that can be built into a self-assembling strategy through molecular design. These interactions are individually weak, usually being on the order of 1 to 10 kcal/mol compared to the approximately 100 kcal/mol strength of a typical hydrocarbon covalent bond. However, when several of these interactions can be set into play, the collective stabilization becomes quite significant. Desiraju classified these general interactions as *supramolecular synthons* after the synthons of retrosynthetic analysis strategy championed by the eminent organic chemist E. J. Corey for the synthesis of complex organic molecules. We will only briefly describe these interactions here, and we refer the reader to more specialized textbooks and reviews that elaborate on the physics and applications of these interactions in the context of supramolecular assembly and pi-conjugated materials.[1–3]

There are several flavors of electrostatic interactions wielded by the supramolecular engineer to promote a particular motif of self-assembly. The strongest of these are classical point charge pairings among positively and negatively charged atoms or functional groups that can provide up to 60 kcal/mol of stabilization. Common examples are formal ionic bonds and coordination complexes. These interactions are tempered by the nature of the solvation sphere or the medium that can screen the extent of the coulombic attraction, such as the case of protein salt bridges between ammonium salts and carboxylates at physiological pH. Dipoles within molecules can also exert electrostatic interactions with point charges (worth 15 to 50 kcal/mol) or even with other dipoles (worth 1 to 5 kcal/mol), such as water molecules solvating a sodium ion, or liquid crystalline molecules interacting in a particular phase. The lone pairs on oxygen are not formally charged but still exert an attractive force on a nearby center of positive charge. The classical hydrogen bond is simply a variation on this ion-dipole theme. The relative charge distributions within more

ionizable X–H bonds (such as R–NH_2 and R–OH) lead to a formal δ^+ charge on the proton that then can partake in stabilizing interactions with nearby anions or dipoles, typically gaining up to 15 kcal/mol of enthalpic stabilization.

Quadrupoles also wage unique forms of enthalpic stabilization (about 0 to 5 kcal/mol in aqueous media). Although subtle in their effects, quadrupolar interactions are important for the energy transporting characteristics of organic electronic materials in an intermolecular sense. The nonspherical charge distribution of an aromatic ring places substantial negative charge above and below the ring, leading to charge deficiency at the edges of the ring. Thus, an aromatic system can stack favorably through an "edge-to-face" T-shaped arrangement, or through a "slip stack" where the pi systems are planar but offset. It should be stressed that the common depiction of a pi-stack involving perfect centered alignment of two aromatics is actually quite repulsive! As optimal pi-electron overlap for most aromatic molecules would be desirable for energy transport, a substantial amount of research has been devoted to learning how to overcome quadrupolar repulsions in thin films or even single crystals.[4,5] The quadrupolar charge distribution can also exert a stabilizing influence with ions and dipoles depending on the electronics involved among the two interacting species. One important example is the "cation-pi" interaction,[6] a fairly recently elucidated interaction that has very important implications for protein folding and ligand-receptor interactions.

These examples of enthalpic stabilization have originated from static ions or dipoles existing within the molecular framework. Because Nature abhors a vacuum, a molecule in the presence of a solvating field must find some way to interact favorably with the solvent at the molecular level. If specific ion, dipolar, or quadrupolar interactions are not present, *induced* influences must be established. This is not unreasonable, because the electric field exerted by an ionic charge is on the order of 10^6 V/cm! The polarizability of a covalent bond, even within "inert" hydrocarbons, will allow for a redistribution of charge in the presence of an electric field associated with a nearby charge, dipole, etc., thereby generating a local δ^+ and δ^- within the bond. This induced charge can now act in an electrostatically favorable sense even though the interacting unit is formally neutral. As may be expected, induced dipole interactions are fairly short range and weak. One might be quick to rule these interactions to be minor players, but they play very important roles in the stabilization of self-assembled monolayers made up of long hydrocarbon chains. With no clear sources of electrostatic stabilization existing among hydrocarbon chains, both interacting partners must mutually induce dipoles that can stabilize each other. These are referred to as London forces, dispersion forces, or van der Waals forces and can provide less than 1 kcal/mol *per interaction*.

Finally, there is one very important entropic effect that crucial for realizing supramolecular assembly schemes, the *hydrophobic effect*. As mentioned earlier, a solute is stabilized by the medium via collective electrostatic interactions from the individual solvent molecules. Therefore, as solutes come together to react, to bind or to assemble, they must shed or alter their solvation sphere. If we consider five molecules that assemble into one larger structure, we see this as an entropic loss. If the enthalpic gains established from new intermolecular interactions within the aggregate cannot compensate for this entropic loss, we would not expect the assembly process to be favorable or thermodynamically spontaneous. However, this analysis neglects the fact that the five molecules establishing favorable interactions among themselves in essence act as a new solvation sphere. The solvents previously needed to solvate the assembling molecule are now "freed" from their interactions, thereby increasing the *overall* disorder within the system as a whole. The gained entropy within the solvent (plus any enthalpic gains from enhanced solvent-solvent interactions) plays an incredibly influential role within any type of supramolecular assembly scheme, be it a self-assembling molecule or a biological protein.

Using these enthalpic and entropic considerations as a foundation, an elegant range of self-assembled supramolecular low-dimensional materials have been prepared. These range from zero-dimensional (0D, where all three dimensions are in the 1 to 100 nm regime) spherical micelles and vesicles formed from linear surfactants, to 1D cylindrical structures from polymers or peptide amphiphiles (where two dimensions are in the 1 to 100 nm range), to 2D structures such as lipid bilayers (where one dimension is in the 1 to 100 nm range). Although supramolecular assembly is relevant to the formation of liquid crystalline bulk phases, block copolymer morphologies, and other extended materials, we focus here on the supramolecular synthesis of well-defined and isolable 1D objects. The geometries of the assembled objects in many instances can be dictated by choice of molecular geometry as articulated by Israelachvili.[7] Although a comprehensive review of molecular self-assembly is well beyond the scope of this chapter, we highlight a few key examples of discrete 1D nanostructures with electronically interesting functionality built by employing these supramolecular design principles. The interested reader is referred to the excellent review put out by Schenning and Meijer in 2005 for a broader coverage of supramolecular electronic materials.[2]

10.2 One-Dimensional Supramolecular Assemblies of Pi-Electron Materials

Difficult synthetic challenges must be overcome to prepare complex 1D aromatic architectures capable of entering the realm of devices for

bioelectronics. Pi-conjugated organic polymers can give well-ordered molecular architectures, but exact control over polymer aggregation, pi-electron backbone planarization, and domain morphology leading to desired electronic properties in the bulk solid-state structure is not trivial. For bioelectronic materials, conductive features with sizes on the order of tens to hundreds of nanometers are needed for intimate interactions with cellular components. This size regime is relatively untouched in the soft materials arena, because it is beyond the limits of most top-down fabrication techniques (such as nanolithography) and beyond the synthetic ability and efficiency for covalently linked bottom-up designs. Nature's ability to utilize this regime is beginning to be mimicked with fundamental understandings of noncovalent interactions and the emergence of supramolecular biomaterials chemistry. The use of noncovalent interactions to construct supramolecular assemblies of pi-electronic materials is maturing from proof-of-principle examples to promising systems showing elegant control of molecular packing and pi-electron interactions at the nanoscale, as discussed next in a very brief sampling of instructive examples.

Schenning, Meijer, and coworkers developed functionalized oligo(*p*-phenylene vinylene)s such as OPV-3 (Fig. 10.1) substituted with hydrogen-bonding self-complementary ureidotriazine units. The ureidotriazine undergoes strong hydrogen bonding in organic solvents, leading to the formation of dimeric structures. The hydrogen-bonded dimers then aggregate in a 1D fashion leading to the formation of well-defined helical and columnar nanoscopic objects.[8] These supramolecular structures form when dissolved in dodecane, a nonpolar solvent that allows the ureidotriazene moieties to establish hydrogen-bonding interactions within a supramolecular dimer without significant competition from the solvent. The chiral stacks were characterized by UV-Vis, fluorescence, and *circular dichroism* (CD) spectroscopy, all of which were compared to the same

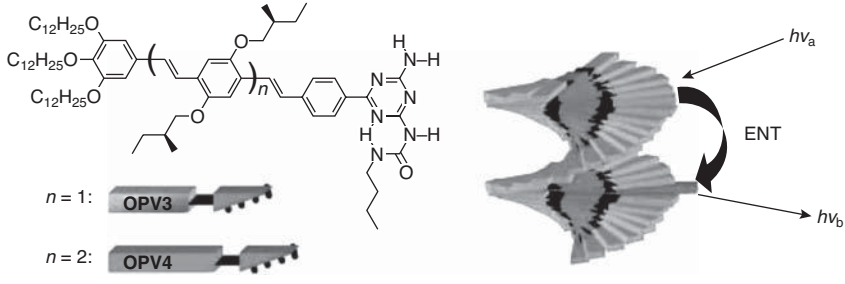


Figure 10.1 Oligophenylene vinylenes that undergo dimerization and self-assembly into 1D helical nanostructures capable of energy transfer to low-bandgap dopants. From Ref. 8, with permission. Copyright 2004, Wiley-VCH Verlag GmbH & Co. KGaA.

spectroscopic measurements taken in chloroform, a solvent that inhibits assembly by more effectively solvating the triazine. The results obtained for the samples in chloroform were shown to be that of the molecularly dissolved species due to the absence of a Cotton effect in the CD spectra and lack of spectral shifts in the UV-Vis. The samples in dodecane showed a blue-shifted absorbance and a red-shifted quenched luminescence, along with a strong bisignated Cotton effect consistent with the exciton coupling model for chromophores locked in a twisted and chiral environment. All of these trends differed from the molecularly dissolved species, indicating that they arise from the intermolecular pi-electron interactions within the aggregate. Heating the spectroscopic solutions provided enough of a stimulus to disrupt the aggregate into the molecular components, a process that was reversible on cooling back to the initial temperature. This thermochromism was readily tracked through spectroscopic observation of the optical signatures corresponding to the aggregated and molecularly dissolved species.

To show the versatility that this complementary hydrogen-bonding subunit has for creating optoelectronic supramolecular aggregates, several variants were made to explore the potential for organic electronic devices. The first variant involved the inclusion of oligomers of greater pi-electron conjugation length (OPV-4, a tetramer with a smaller optical bandgap).[9] The combination of the longer conjugated monomer into ordered aggregates of OPV-3 at a low mol percent (1.2 mol%) created an acceptor unit mixed within the stack of higher-energy OPV-3 chromophores. After excitation of the dominant OPV-3 trimer within the aggregate, the excitation energy was efficiently transferred to the lowest-lying electronic state of the more conjugated OPV-4 oligomer dopant, as evidenced by very efficient quenching of the less conjugated OPV-3 oligomer fluorescence and enhanced fluorescence corresponding to the longer conjugated OPV-4. This effect was observed only after a mixture of the OPV-3 and OPV-4 molecules was heated above the transition temperature (from assembled aggregate to molecularly dissolved) and then allowed to cool, thus reforming a random dispersal of OPV-4 hydrogen-bonded dimers within the 1D supramolecular stacks. The general dynamic properties of the ensemble allow for the incorporation of different acceptor units while still fostering self-assembly and allow for a way to tune the emission wavelength of the overall system through tuning the electronic properties of the component molecular parts.

Würthner and coworkers have studied the assembly properties of perylene diimides (PDIs) in the context of light-harvesting materials and organogelators.[10] They found that the unsubstituted imide units on the PDI molecules could form hydrogen bonds with alkyl-substituted melamines to self-assemble into mesoscopic superstructures.[11] With the success of the complementary hydrogen-bonding

subunits attached to OPVs and the evidence of energy migration through supramolecular aggregates, more complex electronic donor-acceptor variants were developed whereby the PDI with its two preexisting hydrogen bonding triads acted as a complementary hydrogen bonding unit to the Meijer OPVs (Fig. 10.2). The OPVs were substituted with a melamine subunit that would allow for the hydrogen bonding with the PDI unit but would not readily allow for the formation of noncovalent OPV dimers.[12] The supramolecular organization of the donor-acceptor-donor chromophore triads (D-A-D) formed helical columnar stacks as been previously shown with substituted OPVs. *Atomic force microscopy* (AFM) confirmed the chiral aggregates formed in methylcyclohexane, which, because of their D-A-D aggregation of p-type electron-donating OPVs and n-type electron-accepting PDIs, displayed very efficient photoinduced electron transfer and might potentially be used for the development of supramolecular photovoltaics.

Stupp and coworkers established the self-assembling properties of dendron rod-coil molecules (DRCs), triblock molecules containing 3,5-dihydroxy-benzoic ester dendritic segments, biphenyl ester rigid-rod segments, and flexible coil-like polymers.[13] The DRC motif was designed to encourage hydrogen bonding among the dendrons and pi-pi stacking among the rod segments to create 1D growth, and to discourage crystallization due to the flexible coils. These molecules formed birefringent gels in dichloromethane, a sign of the presence of 1D nanostructures that were identified as such with *transmission electron microscopy* (TEM) and AFM. Much like the Meijer OPVs, the DRC nanostructures arise from hydrogen bonding among the dendron segment followed by directional aggregation into ribbon-like structures. Different solvents led to different morphologies: the DRCs also formed self-supporting gels in ethyl methacrylate, but in this solvent they formed defined helical materials that could be used to sequester cadmium ions from the nonpolar medium. On exposure of the cadmium templated nanostructures to hydrogen sulfide gas, a helical morphology of CdS semiconductor was obtained.[14] Later work extended this motif into a more general form that enabled the inclusion of different pi-conjugated rod segments such as oligo(thiophene), oligo(phenylene-vinylene), and oligo(phenylene), where Fig. 10.3 shows a quaterthiophene variant.[15] The gelation and assembly of these structures is the same as seen previously, where a 1 wt% solution of the quaterthiophene DRCs in toluene was molecularly dissolved at high temperature but led to the gelation on cooling. The assembled quaterthiophene structures showed a similar spectroscopic response to that discussed previously, with a blue-shifted absorbance and a red-shifted and quenched luminescence. To test the feasibility of these aggregates for devices, a solid-state film was cast from an iodine-doped 1 wt% assembled gel that exhibited a conductivity of

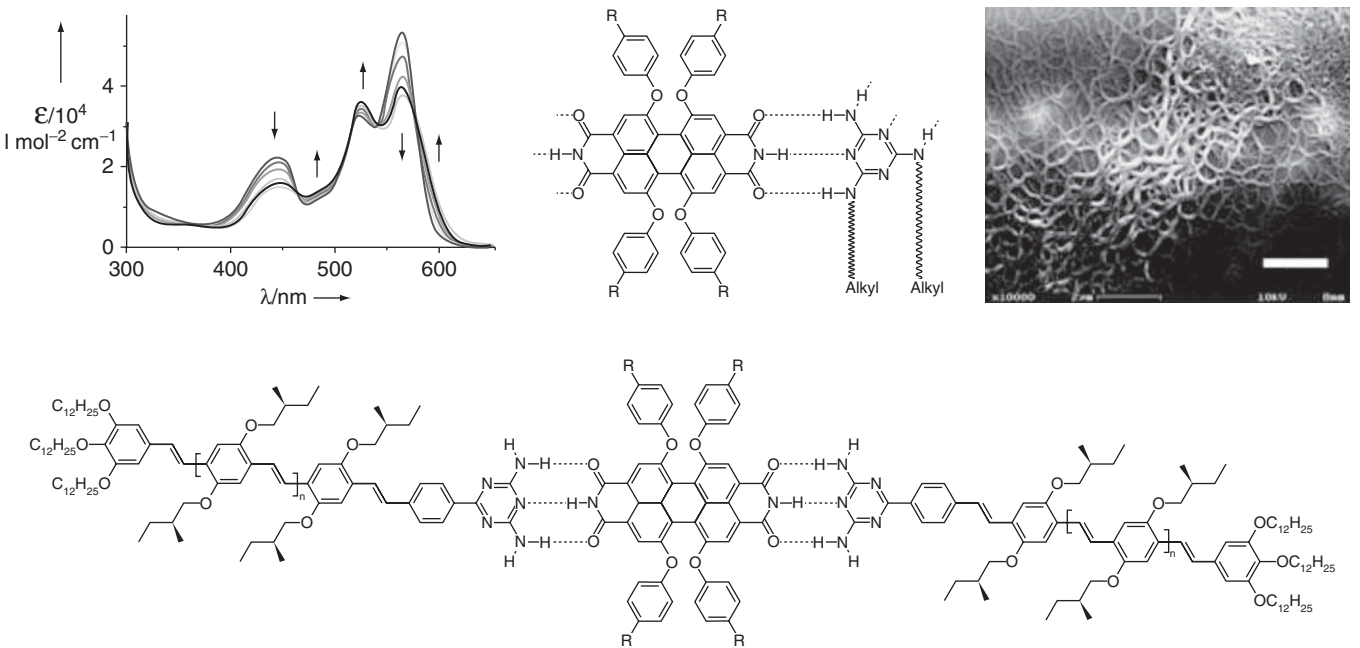


Figure 10.2 A perylene diimide (PDI)-melamine self-assembly scheme leading to fibrous materials (*top*) that was then extended into OPV-PDI triads (*bottom*). Modified from Refs. 11 and 12, with permission. Copyrights 1999, Wiley-VCH Verlag GmbH & Co. KGaA, and 2002, American Chemical Society.

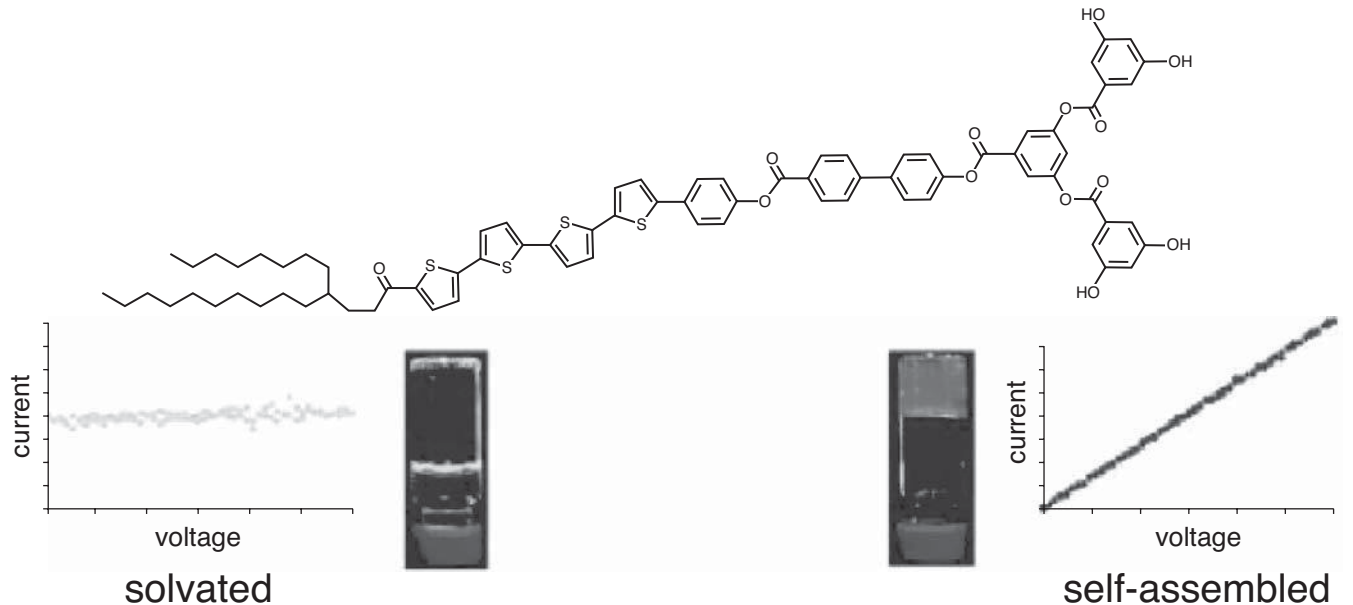


Figure 10.3 An oligothiophene-based dendron rod-coil molecule that leads to electrically conductive nanoribbons on chemical doping. Modified from Ref. 15 with permission. Copyright 2004, American Chemical Society.

7.9×10^{-5} S/cm. This value was three orders of magnitude larger than the films constructed from the molecularly dissolved monomer units, thus revealing the influence and the functional attributes of the supramolecular pi-stacking as a conduit for electrical charge migration within nanoscale dimensions.

For electronic materials to be developed to interface with biologically relevant species, the aggregated structure needs to present a biologically benign surface capable of integrin-mediated recognition.[16] One approach is to use oligopeptides to develop a hierarchical structure. Peptides are well known for forming common hydrogen-bonding motifs such as the α-helix and the β-sheet, and recent research has used the natural propensities for peptides to adopt these secondary structures as a means of making a new electronic materials. Frauenrath and coworkers constructed self-assembling polymer-oligopeptide conjugates bearing diacetylene units (Fig. 10.4).[17] The formation of β-sheet secondary structural motifs in halogenated organic solvents (such as methylene chloride) among the molecular components led to the formation of aggregates that simultaneously aligned the diacetylene subunits favorably for an efficient topochemical polymerization induced by UV irradiation. This created a conjugated polydiacetylene polymer covalently linked with periodically spaced peptide chains. Several new self-assembling compounds have since been synthesized with varying abilities to assemble and/or to undergo topochemical polymerization.[18] Hydrogen bonding was shown to be an important factor for the formation of robust organogels and for an efficient topochemical polymerization: molecules capable of supporting multiple stabilizing hydrogen-bond interactions about both sides of the diacetylene unit gelled and formed polydiacetylenes on irradiation, where those with minimal or no hydrogen bonding capabilities on one end of the diacetylene did not polymerize at all into polydiacetylene. This again highlights the stringent requirement for preorganization of monomers through noncovalent interactions that was necessary to form highly conjugated polymers.

The 1D supramolecular structures discussed thus far have relied to different extents on specific hydrogen-bonding motifs that, when coupled with pi-pi interactions, led to clear electronic delocalization within the resulting nanostructured aggregates. These nanomaterials have demonstrated their potential for energy migration, photoinduced electron transfer, and electrical conductivity. Given the influence of the hydrogen bonding to direct molecular self-assembly into nanoscale objects, the *organic* solvents used to dissolve the molecules were relatively nonpolar. From a biological application standpoint, it would be preferable to construct these materials from *aqueous* and *physiologically relevant* solutions. Self-assembly in aqueous conditions becomes more difficult, as the solvent (water) now competes with hydrogen bonding and other electrostatic interactions, making the

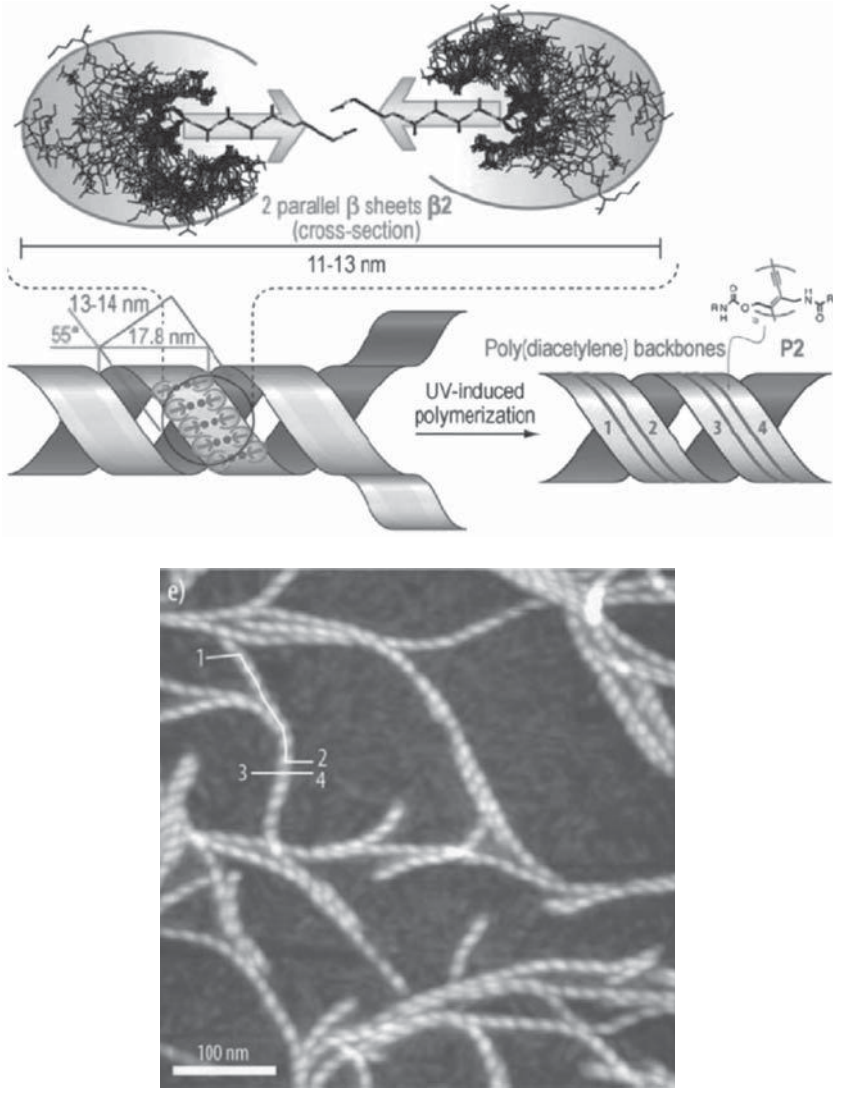


Figure 10.4 Self-assembly of oligopeptides linked with coil polymer segments and diacetylenes positions the alkynes in favorable geometries to facilitate the topochemical polymerization into polydiacetylene, ultimately leading to a helical nanostructured material. Modified from Ref. 17 with permission. Copyright 2006, Wiley-VCH Verlag GmbH & Co. KGaA.

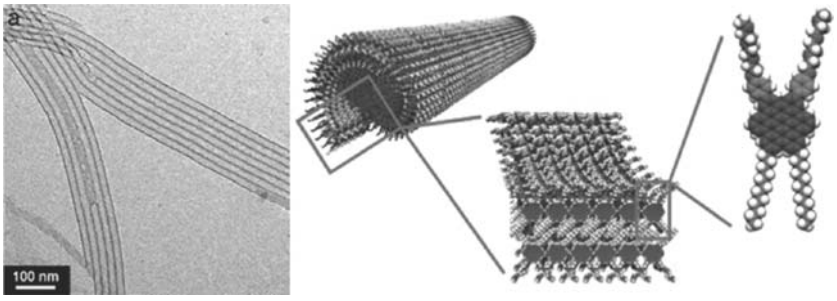


Figure 10.5 Amphiphilic hexabenzocoronenes that self-assemble into well-defined nanotubes. Modified from Ref. 20 with permission. Copyright 2005, National Academy of Sciences (USA).

desired intermolecular solute-solute interactions less potent. In addition, the pi-conjugated moieties themselves tend to be very hydrophobic, making their extension into water even more difficult. The development of new assembly schemes whereby water screening becomes less detrimental to supramolecular interactions will be needed to promote the aqueous self-assembly of artificial electronic materials.

Aida and coworkers reported an amphiphilic *hexabenzocoronene* (HBC) that underwent assembly in THF solvent as well as in water-THF mixtures (Fig. 10.5).[19,20] The HBC motif is well known to form discotic liquid crystals with strong pi-stacking among the flat aromatic units. The Aida molecular design installed hydrophobic alkane chains on one edge of the HBC core and hydrophilic tetraethylene oxide chains on the other. Dissolution was achieved in *tetrahydrofuran* (THF) at elevated temperatures, and on cooling the self-assembly occurred. The proposed molecular assembly involves a bilayer of HBC molecules, whereby the alkyl chains are interdigitated in a crystalline manner, leaving the surfaces of the bilayer decorated with the ethylene oxide chains. These polar groups interact favorably with the THF solvent and prevent extended multilayer formation. In THF, the formation of large nanotubes was observed (20 nm diameter, much larger than typical single-walled *carbon nanotubes*, CNTs), but in aqueous cosolvents, a helical morphology was obtained. On chemical oxidation, the generation of radical cation charge carriers was evident in optical absorption and in actual electrical measurements. They have used these materials for photoconductivity[21] and as templates for other supramolecular interactions through the incorporation of positively charged isothiouronium ion side chains.[22] In the latter example, the cationic isothiouronium surface allowed for complexation with anionic species such as anthraquinone-2-carboxylate that quenched the aggregate emission through photoinduced electron transfer. This new example has shown that well-defined monomers can construct higher

ordered nanostructures through noncovalent interactions that can persist in aqueous environments.

Lee and coworkers have studied several amphiphilic rod-coil oligophenylene self-assembling systems leading to micelles, vesicles, helical structures, and many other low-dimensional motifs.[23] Their design strategy involves the alteration of the lengths of rod segment (oligophenylene) and coil segment (oligoethylene oxide) in order to control the nature of the resulting aggregate. More complex molecular architectures such as branched or dendritic presentation of the ethylene oxide fragments can also be used to control the shapes of the supramolecular objects. In many cases, these assemblies form in organic solvents, but with sufficient hydrophilic character, the molecules are water soluble and also assemble in aqueous conditions. Although the aqueous assembly of these oligophenylene molecules is indeed an important advance, it is known that the presentation of oligoethylene oxide moieties can be used to resist the adhesion of proteins and might therefore affect the nanostructure's ability to foster protein-based molecular recognition with cells.[24] To overcome this limitation, specific carbohydrates have also been attached covalently to the hydrophilic coil segments, thereby providing a possible handle for cellular recognition.[25] Given that the molecular assembly leads to a nanostructure presenting multiple sugar units, this scheme could prove to be a powerful method to encourage the multivalency in ligand-receptor interactions known to enhance the binding between cells and artificial surfaces.

From single monomers, very complex and elegant supramolecular architectures can be constructed with varying properties. These nanoscale objects materials fill the void in accessible size regimes from typical micro- or nanofabrication techniques used to process soft materials. The use of fundamental intermolecular interactions to construct supramolecular structures from well-characterized monomeric precursors is a powerful route to nanoelectronic materials. Protein-based hydrogen-bonding motifs should allow for the ability to construct a biocompatible material and possibly incorporate a secondary function that may promote cell adhesion or other biologically important interactions, an important consideration for compatibility in biologically relevant environments. The examples shown here give a broad and representative view of the many promising and elegant contemporary systems for application as bioelectronic nanomaterials.

10.3 Electrically Conductive Polymers as Biomaterials

The nanomaterials described in the last section could be considered as exotic designer semiconductors—they are available through sometimes lengthy chemical synthesis on material scales usually on the

order of grams or less. Conducting polymers are more readily available on multigram scales and above, but fashioning them into isolated 1D objects is difficult with current lithography. In specialized cases, block copolymers can form nanoscale materials, but the individual components are now intimately if not covalently linked within a large area network or domain rather than being isolable and manipulatable structures. Like most plastics, pi-electron conjugated polymers in their pristine neutral state are not electrically conductive. Redox chemistry (most commonly leading to polymer oxidation) induces a change in electronic structure that leads to an electrically conductive material. This property can be switched on and off repeatedly by simple application of an electrical potential, or through exposure to suitable oxidants and reductants. The intricacies of this process are well established, and we refer curious readers to the recent edition of the *Handbook of Conducting Polymers* for more information.[26] Conductive polymers have been used successfully in many biomedical applications such as for controlled drug delivery because of their switching capabilities and biocompatibility.[27]

Two major conducting polymers are quite prevalent in the biomedical engineering (Fig. 10.6): polypyrrole (PPy) and poly(3,4-ethylenedioxythiophene) (PEDOT). Both of these polymers are derived from the polymerization of electron-rich heteroaromatic rings, and the resulting polymers have favorable materials properties such as aqueous processability, established biocompatibility, ease of deposition via electropolymerization, and electrically responsive switching between insulating and conductive states. PPy unfortunately suffers from long-term instability, performance variation due to coupling defects, and the possibility of reduction (back to the neutral insulating

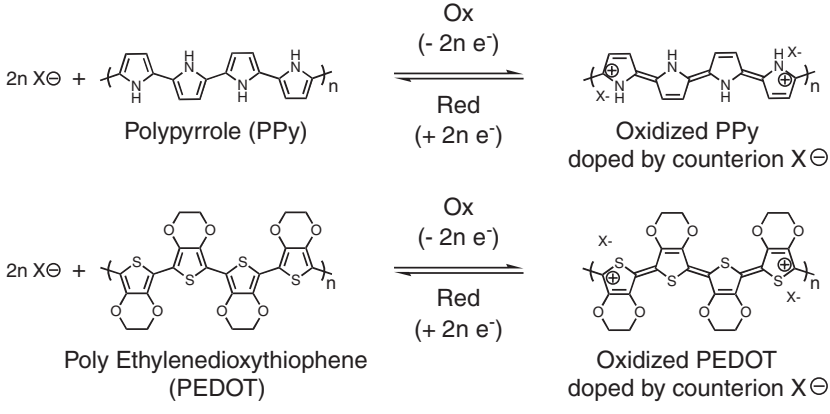


Figure 10.6 Neutral (insulating) and oxidized (conductive) chemical structures depicting the important forms of PPy and PEDOT. Note that the actual localization of charges here is only schematic.

form) by biologically relevant reducing agents. PEDOT has most commonly been used as a surface modification agent for optoelectronic devices, specifically to make conductive transparent oxide surfaces less rough yet still highly electrically conductive. It is now starting to find use as a biological coating as well.[28] Other specialty polymers have been employed in biological settings such as polythiophene electrolytes or oxygenated polypyrroles.[29,30]

10.3.1 Electrodes at Neural and Cardiac Interfaces

Neural and cardiac electrodes are seeing increased usage in a number of diagnostic, therapeutic, and treatment applications; everything from brain implants (Fig. 10.7), pacemakers, and cochlear implants, to the treatment of epilepsy, depression, chronic pain, and Parkinson's disease, to the regulation of breathing and bladder and bowel control. These implanted electrodes work by sensing or sending electrical pulses and are therefore highly dependent on the contact at the tissue-electrode interface. "Classical" electrodes, made from materials such as gold, platinum, iridium, titanium, or steel, are biocompatible or bio-inert but suffer the drawback of having poor contact with tissue. This poor contact can provoke an immune response and scar tissue formation around the electrode, which drastically diminishes the long-term electrode performance. Furthermore, these interfaces may not be mechanically robust, which poses a problem for implants subject to muscle contractions during device operation. Ideally, an electrode coating is needed that is conductive, adhesive, and biocompatible to address the electrode-tissue interface.

A neurological probe's ability to sense an action potential from a neuron is dependent on both the surface area of the recording site

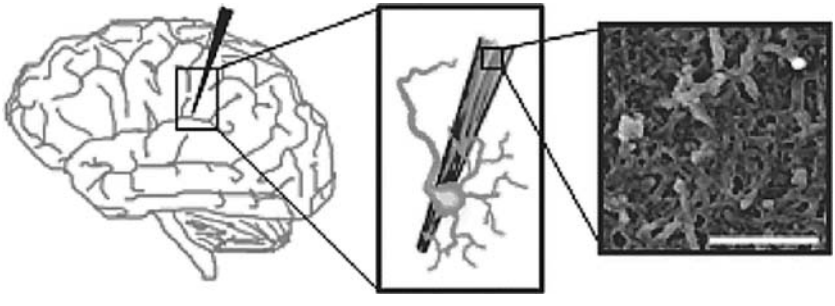


Figure 10.7 Biocompatible conductive coatings play a major role in the performance at the neural-electrode interface by encouraging the adhesion of cells to the electrode surface as schematically depicted on different length scale: Direct insertion into the brain (*left*) should ideally elicit cell-electrode interactions (*center*) that are facilitated by proper surface roughness and chemistry (*right*). From Ref. 43, with permission. Copyright 2009, American Chemical Society.

and the impedance of the surface. Recording the activity of a single neuron requires a decreased electrode size down to that of a single cell. Unfortunately, a decreased electrode surface area causes an increase in the impedance, leading to reduced sensitivity and charge-transfer capability.[31,32] Conductive polymers such as PPy have been used for just this purpose, and because of rough surface morphology, electropolymerized PPy leads to an increased overall surface area for a given geometric space. This in effect increases the capacitance at the recording site and decreases the impedance. These films are also porous and allow for effective ion exchange into and out of surrounding tissue, which is important for rapid electrochemical response of the polymer. The redox chemistry occurring at the recording site transduces the ionic current associated with ion channel flux into electric current detected with common electronics. PPy, unfortunately, is not well suited for long-term implantation, and PEDOT has begun to receive increased interest. In time-based studies, PPy/poly(styrene sulfonate) (PSS) retained only 5% of its original activity over 16 hours, whereas PEDOT/PSS retained 89% over the same time period.[33]

Probes using conductive materials such as silicon, gold, and iridium are currently being used to both stimulate and record electronic impulses from cells. Unfortunately, the flat, smooth surfaces of these metal probes do not encourage the adhesion of cells and thus limit their overall utility. Conductive polymers have been employed as biomaterials for effective surface modifications to optimize interaction between the stimulating/recording electronics and living cells. Although PPy and PEDOT have been used successfully for this purpose, Martin's group also demonstrated that hydroxymethylated PEDOT (PEDOT-MeOH) provides a more effective probe surface modifier. PEDOT-MeOH has lower impedance that PPy, is more stable to biological reductants for long-term implant potential, and adds more aqueous solubility for processing and biocompatibility. It is also possible to dope PEDOT-MeOH with PSS and short oligopeptides (such as the amino acid sequence CDPGYIGSR, a substructure of laminin known to encourage cell adhesion). These two dopants allow for better processing than dopants used with PPy and provide a rougher surface morphology, which in turn leads to enhanced cell adhesion.[34] Recently, Ying, Yu, and coworkers have developed a series of functionalized PEDOT materials with a variety of linker groups that are covalently attached to the polymer backbone (Fig. 10.8).[28] These monomers could be polymerized from aqueous emulsions and deposited on a wide array of substrates such as metal electrodes or even Tygon tubing. These polymers express established chemical linkers that could be used in the future to conjugate biosignals onto the PEDOT coatings and should lead to better immobilization of expressed signals without dramatically affecting film formation or electronic properties.

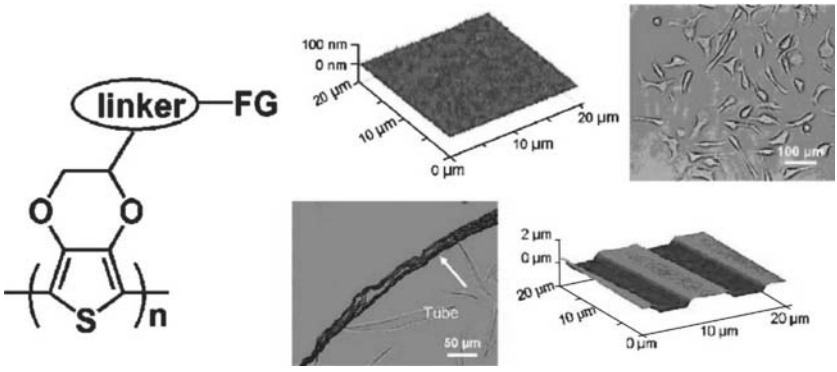


Figure 10.8 Functionalized EDOT monomers can be polymerized from aqueous emulsions to provide conductive polymers (*left*) for coatings on a variety of surfaces, such as macroelectrodes (*upper middle AFM*) and microelectrode arrays (*lower right*), that encourage cell adhesion (*upper right image*). Substrates as unusual as plastic surgical tubing could even be used. From Ref. 28, with permission. Copyright 2008, American Chemical Society.

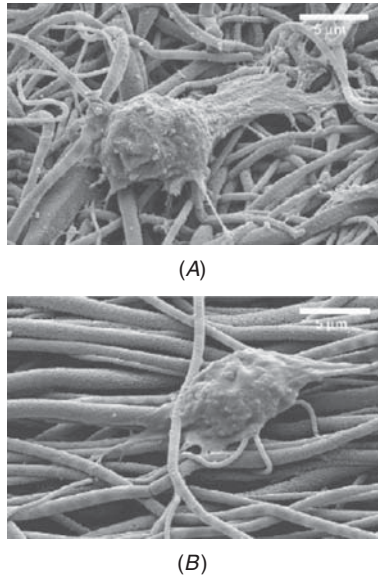
10.3.2 Cell Growth and Guidance

Electrically conductive biomaterials are also being used to control the shape and growth of cells. Size, shape, and growth of cultured cells can somewhat be controlled by environmental conditions including type of cell culture medium, supplements in the medium, inclusion or exclusion of growth factors, or addition of hormones. These control techniques address the environment surrounding the cultured cells but overlook the attachment surface. Because mammalian and other cells must attach to a surface to survive, the nature of the attachment itself provides another handle for cell morphology control. Many factors play a role in influencing what type of surface is presented to an attached cell; surface charge density, wettability, and roughness can all be used to influence cellular attachment, metabolism, and/or function. PPy again has potential as a conductive biomaterial because of its switchable surface characteristics. For example, PPy in its reduced insulating form inhibits proper cellular adhesion, whereas oxidation of the polymer into the conductive state leads to much greater degrees of cell spreading. Both of these electronic states have been shown to be nontoxic to cells. This material acts as an active and switchable surface to control cell growth and differentiation,[35] a property that has been applied recently for tissue engineering. Likewise, PEDOT films also encourage cell adhesion and spreading on a variety of planar and curved surfaces (see Fig. 10.8).

In the context of cellular engineering, the polymer surfaces mentioned earlier are *hundreds* of microns in size and thereby provide isotropic guidance cues to a specific cell with respect to any

directionality in the growth or extension of cellular processes. Nevertheless, prospects for engineering at the *tissue* level are quite high, such as for the development of nerve guidance channels. A current clinical approach to repair peripheral nerve damage requires an autologous nerve graft, where the graft is removed from the patient's own nerve tissue at a healthy donor site. Although this has the advantage of tissue compatibility, the graft causes loss of function at the donor site and brings the possibility of mismatched dimensions between donor and acceptor site.[36] Alternatives to autologous nerve grafts are synthetic tubular guidance channels made from materials such as collagen, laminin, fibronectin, silicone, or other polymers. The goal of these types of natural and synthetic nerve guidance channels is to direct axon resprouting through physical cues. Electrical stimulation may also play an inherent role in the function of autologous nerve grafts. Electrical charge and external electromagnetic fields can stimulate the extension, proliferation, differentiation, and regeneration of many different cell types. Electrically conductive biomaterials offer two key advantages for nerve tissue engineering applications. First, electrical stimulation through the cell adherent surface would localize the electromagnetic field to the polymer surface, providing more spatial control over externally applied fields. Second, many conductive polymers present unique surfaces properties that can be varied through the type of dopant and surface morphology in order to tailor the types of cells adhered or even allow for surface patterning. Overall, using PPy as a nerve cell guidance material has been shown to enhance nerve cell differentiation in culture and increase the neurite growth length while invoking little immune response in animal implants.[37] Recent work with PPy-coated electrospun polymer nanofibers has shown preferential cellular elongation on aligned nanomaterials (Fig. 10.9).[38]

Other electronic materials making impacts in the biomaterials realm are the many types of carbon nanotubes. Unlike the other 1D materials discussed in this chapter, CNTs can be considered as single molecules because they are composed of covalently linked graphene sheets that have been schematically rolled up and stitched together. CNTs can be produced industrially and are now commercially available in bulk quantities with varying degrees of purity. Their mechanical strength and toughness as well as chemical stability and high conductivity make them an obvious candidate for a conductive biomaterial electrode coating, particularly in applications where the mechanical rigidity of the underlying matrix is important. The performance of CNT-based electrodes is much better than that of current state-of-the-art electrodes in the ability to reduce impedance, increase charge capacity, and facilitate charge transfer, and they provide dual electronic and ionic conductivities. However, CNTs still need improvement in their electrochemical properties, long-term



(*A*)

(*B*)

Figure 10.9 Rat PC-12 nerve cells adhered to both random (*A*) and aligned (*B*) polypyrrole fibers. From Ref. 38, with permission. Copyright 2009, Elsevier.

durability, and biocompatibility. CNTs are also prepared as mixtures of single and multiwalled nanotubes with different diameters and different electronic properties (some are insulating, some semiconductive, and some metallic!). These as-synthesized nanotubes are incredibly hydrophobic and often difficult to dissolve in aqueous media without the help of surfactants and other solubilizers. Purification, functionalization, and separation on the basis of electronic structure or size remains a substantial challenge in modern CNT research.[39,40]

One strategy to address the shortcomings of CNTs is to co-deposit or layer CNTs with other known conductive biomaterials (such as PEDOT) to take advantage of the individual beneficial properties of each. The surfaces of CNTs can also be modified directly in order to covalently install functional groups for cell adhesion.[41] It has been shown that CNTs can promote neurite growth to a greater extent if they are coated with bioactive molecules. For example, a coating of 4-hydroxynonenal was applied to CNTs to encourage adhesion, and this composite system was able to elicit neurons to extend multiple neurites with extended branching versus CNTs without the coating.[42] CNTs have also been modified in a layer-by-layer approach with polyelectrolytes.[43] Although these CNT surface alterations have helped to make the nanotubes more soluble in aqueous environments and more adherent for cells, these alterations can also alter the inherent electronic properties of the nanotubes. CNTs have also been covalently surface modified with nerve growth factors to successfully regulate the survival and differentiation of neurons.[44] The

conductance of CNTs can also be enough to stimulate a neuronal response where the surface modification simply acts as a solubilizing agent. For example, CNTs were functionalized with poly(ethylene glycol) (PEG) to make them soluble in aqueous solutions and increase their bioavailability. These PEG-CNTs were then deposited onto glass coverslips in varying thicknesses in order to control the overall conductivity. Studies of neuronal interactions with a range of conductivities showed that there is an ideal range for the promotion of neuronal growth and neurite extension, and these data are now being applied to other CNT systems as well as other conductive electrode surface materials.[45]

10.4 Peptide-Oligothiophene Conjugates for Bionanostructures

There is now broad recognition of the importance of developing biologically relevant nanomaterials with electronic functions. Self-assembly of pi-conjugated molecules into low-dimensional objects has usually been executed in organic solvents, thus precluding useful transitions into biological applications. Likewise, the current difficulties in fashioning conducting polymers into defined nanomaterials have precluded the development of stand-alone conductive nanomaterials. Carbon nanotubes have been one approach to meet this challenge, but there are several issues of purity, composition, and ability to achieve biological recognition that affect the size and the bioelectronic properties of the nanotube samples. The structural proteins of the extracellular matrix are composed of 1D materials, and the ability to bring useful optoelectronic properties with this dimensionality could have a major impact on bridging the biotic-abiotic interface. One class of organic semiconductors that has received much interest in this regard is the *oligothiophene* family of p-channel (electron-donating) materials. Over the past year, new work has been reported with oligothiophene 1D nanomaterials built from the assembly of peptide-based components (Fig. 10.10). The intention with these approaches is to bring the electronic properties of the oligothiophenes into biologically compatible applications.

Bäuerle and coworkers prepared a designer oligo(ethyleneoxide)-peptide sequence with sufficient solubility that they could achieve the solution-phase "click chemistry" functionalization of the peptides onto a central quaterthiophene unit (Fig. 10.11, *left* and *center*).[46] The peptide-pi-conjugated hybrid was indeed soluble in many common organic solvents, but there was still some tendency toward aggregation. The final molecular architecture presented oligoethylene oxide units at the two termini of the linear molecule, and these in practice minimized the intermolecular pi-electron delocalization within the

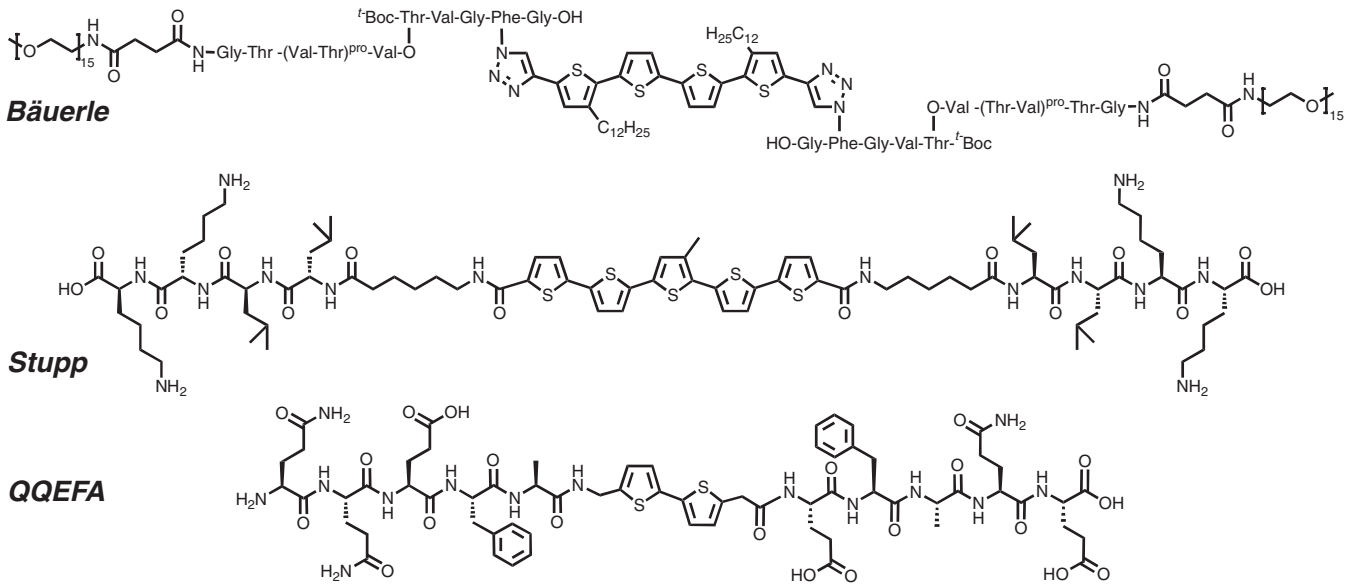


FIGURE 10.10 Oligothiophene peptides recently reported by the Bäuerle, Stupp, and Tovar groups as reported in Refs. 46, 47, and 48.

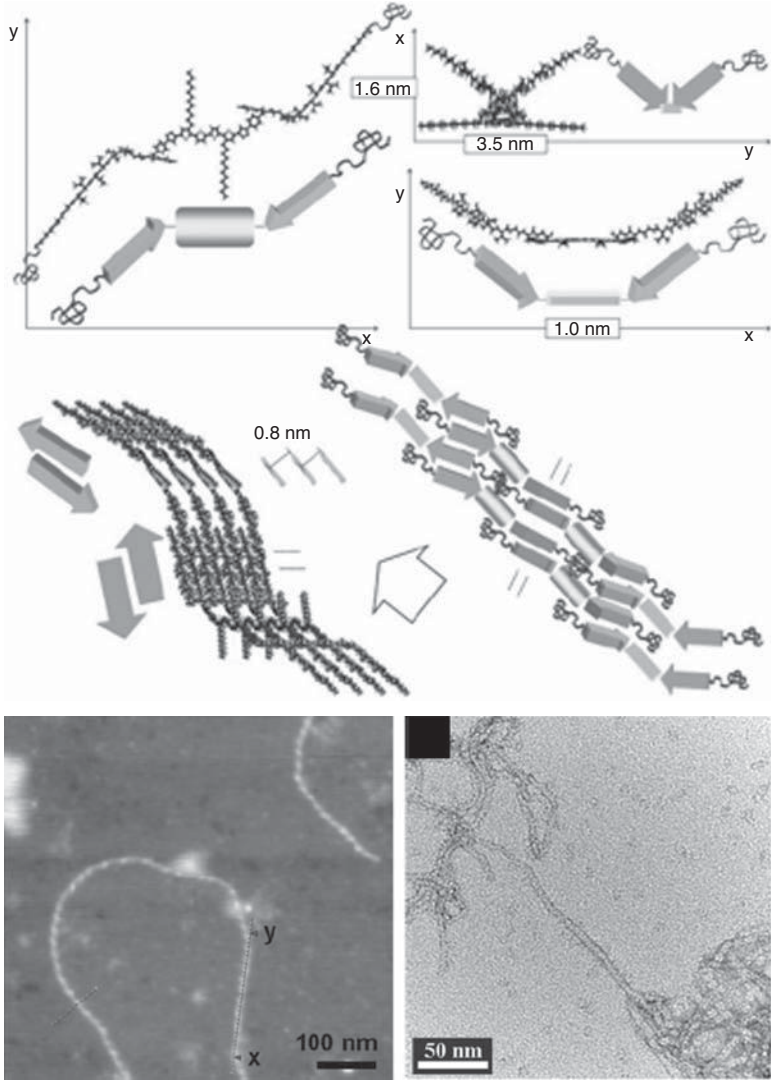


Figure 10.11 A model proposed for the assembly of the Bäuerle peptide (*top*) along with images formed by the Bäuerle peptide (*bottom left*, AFM) and the Stupp peptide (*bottom right*, TEM). Modified from Refs. 46 and 47 with permission. Copyrights 2009, Wiley-VCH Verlag GmbH & Co. KGaA and Royal Society of Chemistry.

resulting nanomaterials necessary for delocalized electronic structures. These elegant multifunctional molecules offer many design strategies for continued development, such as a novel switch in peptide backbone connectivity that could be used for promoting solubility until a late stage of synthesis. A careful switching condition was developed for more controlled self-assembly leading to well-defined 1D nanostructures between 8 and 12 nm in height with the functional quaterthiophene unit embedded within.

Stupp and coworkers shortly thereafter reported an even longer quinquethiophene segment covalently attached within the peptide backbone (Fig. 10.11, *right*).[47] In their synthesis approach, a small peptide sequence with multiple ionizable groups (lysine here) was prepared independently using standard solution-phase coupling techniques. The peptide was installed to the central quinquethiophene through solution-phase amidation between a quinquethiophene diacid and the N termini of the peptide sequence. These molecules formed self-assembled structures in water that were observed to be on the order of 5 to 10 nm in height. Here, methanolic solutions could be used to study the spectroscopic properties of molecularly dissolved material, whereas addition of water led to extended self-assembly. There were pronounced temperature effects whereby heating led to the establishment of β-sheet-rich assemblies. It is clear from the work of Bäuerle and Stupp that there is great promise for peptidic materials bearing pi-electron function that can form well-defined nanomaterials under organic or even completely aqueous conditions.

In our own research, we sought a synthetic strategy that would allow for the preparation of the electronic peptides directly on the solid-phase resin supports commonly used for automated peptide synthesis.[48] This required the independent preparation of pi-conjugated "amino acids" that would react analogously to the amino acid building blocks commercially available for peptide solid-phase synthesis. To validate this approach, we prepared one such amino acid around a bithiophene pi-electron unit. Indeed, this unit could be built into a peptide sequence with no need for solution-phase synthetic chemistry that can often require laborious purification steps to isolate desired peptidic materials from reaction by-products. One such pi-conjugated peptide prepared through this solid-phase approach is the QQEFA peptide illustrated at the bottom of Fig. 10.10.

Standard spectroscopies were used to characterize the assembly process (Fig. 10.12). The infrared (IR) spectrum for QQEFA displayed characteristic absorptions found in other synthetic β-sheet systems. Circular dichroism of freely soluble QQEFA yielded no meaningful absorption, whereas acidification and assembly led to intense absorptions associated with the pi-conjugated unit (Fig. 10.12*A*). The data indicate that the bithiophenes rest in twisted chiral environments as expected from the slight twists found in natural β-sheet motifs. The

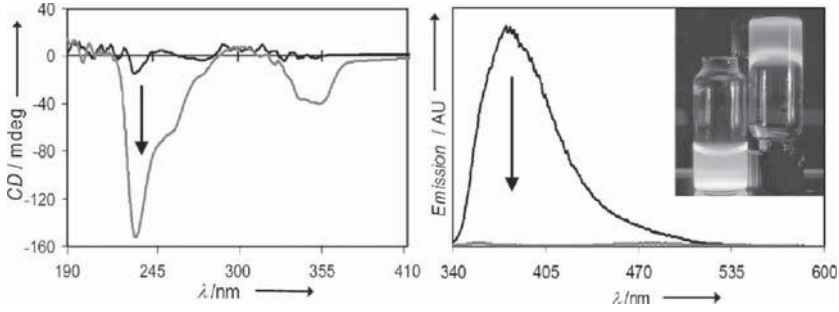


Figure 10.12 Spectroscopy of the QQEFA peptide prepared in our laboratories. (*A*) Circular dichroism of the QQEFA peptide in basic solution (molecularly dissolved, dark upper trace) and in acidic solution (assembled, gray lower trace). (*B*) Fluorescence spectra of the basic solution (dark upper trace) and once acidified (gray lower trace). (*Inset*) Photo of the bulk phenomena, where the basic molecular solution is to the left, and the self-assembled hydrogel is to the right. Modified from Ref. 48 with permission. Copyright 2008, American Chemical Society.

CD crossover at 320 nm (coincident with the low-energy UV-Vis absorption λ_{max}) is a classic signature for exciton coupling observed routinely in other optoelectronic molecules assembled from organic solvents. Exciton coupling is one observation of a well-defined intermolecular pi-electron interaction among two or more chromophore units leading to a direct perturbation of the overall electronic properties. The exciton coupling was further verified by examining the fluorescence of QQEFA in solution and in aggregates (Fig. 10.12*B*). Molecularly dissolved QQEFA absorbs at 320 nm, resulting in strong photoluminescence, but the fluorescence is dramatically quenched on acidification.[49] These photophysical behaviors support the formation of tapelike aggregates with intimate pi-pi contact, a design element that will play a critical role in bioelectronic applications requiring pi-stacking or spectroscopic observables that vary with assembly or solvation.

Atomic force microscopy was used to visualize the components that comprise the self-supporting gel (Fig. 10.13). The subtle energy landscape for amyloid assembly offers many thermodynamic sinks on the road from free molecule to large amyloid-like fiber. The predominant features were high-aspect-ratio fibrillar 1D nanostructures typically 2 to 5 nm in height. In some cases, we could experimentally resolve the appearance of superstructural helicity with fairly regular periodicities as is common for many other naturally occurring amyloid plaques.[50] Molecular modeling of a model peptide revealed an antiparallel β-sheet assembly motif shown in Fig. 10.13 (*right*) that is consistent with the observed spectroscopy and microscopy. This

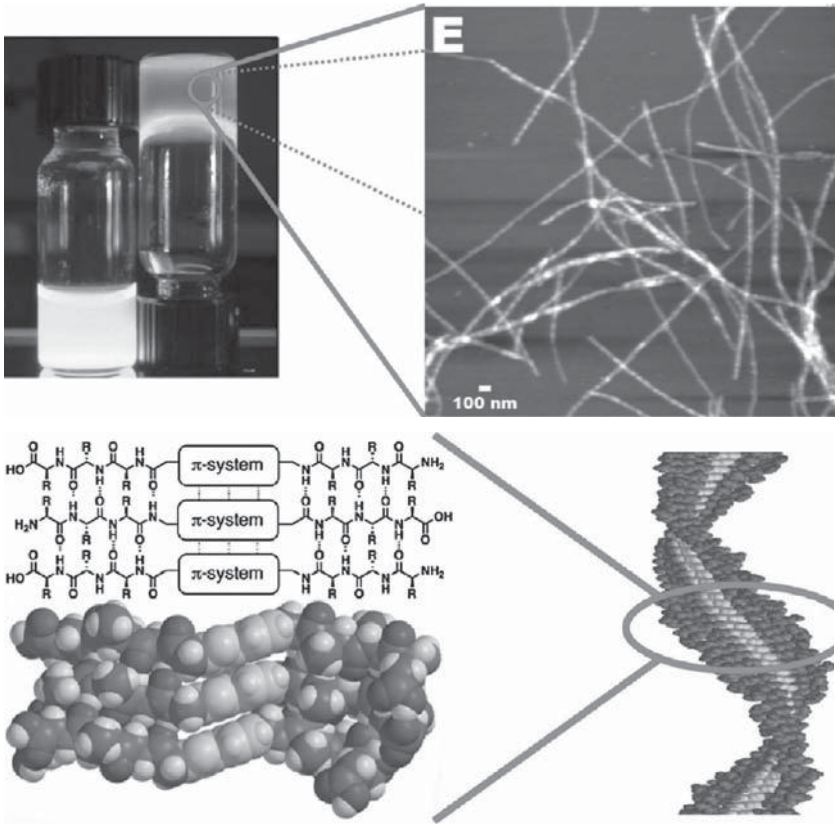


Figure 10.13 AFM image of the self-supporting hydrogel that formed on acidification of a solution of the QQEFA peptide showing the 1D nanomaterials that compose the gel (*top*). A space-filling molecular model of the structure of the resulting aggregates showing the helical twist sense of the β-sheet (*bottom*). Modified from Ref. 48 with permission. Copyright 2008, American Chemical Society.

leads to twists similar to those within natural β-sheet structures ($\sim 9^\circ$ between individual molecules) and the intermolecular pi-stacking distance falls at about 5 Å. This distance is longer than what one typically associates with strong pi-stacking, but the perturbation in the present case is enough that exciton coupling can be observed and has been previously exploited for energy transfer among indole side chains of assembled tryptophan-containing peptides as well as among stilbenes covalently attached to α-helical peptides.[51,52]

Our work is continuing to expand the scope of pi-electron units that can be incorporated within these structures. We have developed new reaction strategies to diversify these materials even more through the use of easily prepared (or even commercially available) building

blocks with varying electronic properties (such as easily oxidized, easily reduced, or highly fluorescent). We have also devised new strategies to control the presentation of the β-sheet peptide polarity, another important consideration in terms of influencing how the peptide β-sheets interact in an intermolecular sense within a given supramolecular aggregate. Finally, because the nanostructure formation seems to be a general approach, we have successfully incorporated bioactive signals on the peptide termini such that the resulting nanostructures present a dense concentration of bioadhesive signals for cell adhesion and proliferation. Our progress along these new fronts will be reported in the near future.

10.5 Concluding Remarks

Supramolecular assembly is a powerful approach to construct a variety of low-dimensional objects with a variety of unique functions. Conducting polymers are also powerful biomaterials for nerve repair and cardiac regulation. Exciting new developments in the supramolecular assembly of well-defined pi-conjugated electronic materials in physiological environments are now underway. It will soon be possible to construct 1D nanomaterials that can directly interface useful electrical function with living cells, whether for therapeutic or diagnostic applications. The ability to influence cells through external nanostructured biomaterials as well as the ability to detect cellular events or harness biological energy sources will be the subject of many new and exciting scientific inquiries in the coming years, and self-assembled organic electronic materials stand to play large roles in these important pursuits.

Acknowledgments

Our work in this area is supported by the Johns Hopkins University. S.R.D. was supported by the Institute for NanoBioTechnology as an NSF-IGERT Predoctoral Fellow (DGE-0549350).

References

1. J. W. Steed and J. L. Atwood, *Supramolecular Chemistry*, 1st ed., Wiley, New York, 2000.
2. F. J. M. Hoeben, P. Jonkheijm, E. W. Meijer, and A. P. H. J. Schenning, "About supramolecular assemblies of π-conjugated systems," *Chemical Reviews,* vol. 105, p. 1491, 2005.
3. E. V. Anslyn and D. A. Dougherty, *Modern Physical Organic Chemistry*, 1st ed., University Science Books, Sausalito, CA, 2006.
4. J. Cornil, D. Beljonne, J.-P. Calbert, and J.-L. Brédas, "Interchain interactions in organic π-conjugated materials: impact on electronic structure, optical response, and charge transport,"*Advanced Materials,* vol. 13, p. 1053, 2001.

5. J. E. Anthony, J. S. Brooks, D. L. Eaton, and S. R. Parkin, "Functionalized pentacene: improved electronic properties from control of solid-state order," *Journal of the American Chemical Society,* vol. 123, p. 9482, 2001.
6. J. C. Ma and D. A. Dougherty, "The cation-pi interaction," *Chemical Reviews,* vol. 97, 1303, 1997.
7. J. N. Israelachvili, *Intermolecular and Surface Forces*, 2nd ed., Academic Press, San Diego, 1992.
8. A. Schenning, P. Jonkheijm, E. Peeters, and E. W. Meijer, "Hierarchical order in supramolecular assemblies of hydrogen-bonded oligo(*p*-phenylene vinylene)s," *Journal of the American Chemical Society,* vol. 123, p. 409, 2001.
9. F. J. M. Hoeben, L. M. Herz, C. Daniel, P. Jonkheijm, A. P. H. J. Schenning, C. Silva, et al., "Efficient energy transfer in mixed columnar stacks of hydrogen-bonded oligo(*p*-phenylene vinylene)s in solution," *Angewandte Chemie, International Edition,* vol. 43, p. 1976, 2004.
10. X. Q. Li, V. Stepanenko, Z. J. Chen, P. Prins, L. D. A. Siebbeles, and F. Würthner, "Functional organogels from highly efficient organogelator based on perylene bisimide semiconductor," *Chemical Communications*, p. 3871, 2006.
11. F. Würthner, C. Thalacker, and A. Sautter, "Hierarchical organization of functional perylene chromophores to mesoscopic superstructures by hydrogen bonding and pi-pi interactions," *Advanced Materials,* vol. 11, p. 754, 1999.
12. A. P. H. J. Schenning, J. von Herrikhuyzen, P. Jonkheijm, Z. Chen, F. Würthner, and E. W. Meijer, "Photoinduced electron transfer in hydrogen-bonded oligo(—phenylene vinylene)-perylene bisimide chiral assemblies," *Journal of the American Chemical Society,* vol. 124, p. 10252, 2002.
13. E. R. Zubarev, M. U. Pralle, E. D. Sone, and S. I. Stupp, "Self-assembly of dendron rodcoil molecules into nanoribbons," *Journal of the American Chemical Society,* vol. 123, p. 4105, 2001.
14. E. D. Sone, E. R. Zubarev, and S. I. Stupp, "Semiconductor nanohelices templated by supramolecular ribbons," *Angewandte Chemie, International Edition,* vol. 41, p. 1705, 2002.
15. B. W. Messmore, J. F. Hulvat, E. D. Sone, and S. I. Stupp, "Synthesis, self-assembly, and characterization of supramolecular polymers from electroactive dendron rodcoil molecules," *Journal of the American Chemical Society,* vol. 126, p. 14452, 2004.
16. S. E. Sakiyama-Elbert and J. A. Hubbell, "Functional biomaterials: design of novel biomaterials," *Annual Review of Materials Research,* vol. 31, p. 183, 2001.
17. E. Jahnke, I. Lieberwirth, N. Severin, J. P. Rabe, and H. Frauenrath, "Topochemical polymerization in supramolecular polymers of oligopeptide-functionalized diacetylenes," *Angewandte Chemie, International Edition,* vol. 45, p. 5383, 2006.
18. E. Jahnke, N. Severin, P. Kreutzkamp, J. P. Rabe, and H. Frauenrath, "Molecular level control over hierarchical structure formation and polymerization of oligopeptide-polymer conjugates," *Advanced Materials,* vol. 20, p. 409, 2008.
19. J. P. Hill, W. S. Jin, A. Kosaka, T. Fukushima, H. Ichihara, T. Shimomura, et al., "Self-assembled hexa-peri-hexabenzocoronene graphitic nanotube," *Science*, vol. 304, p. 1481, 2004.
20. W. Jin, T. Fukushima, M. Niki, A. Kosaka, N. Ishii, and T. Aida, "Self-assembled graphitic nanotubes with one-handed helical arrays of a chiral amphiphilic molecular graphene," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 102, p. 10801, 2005.
21. Y. Yamamoto, T. Fukushima, Y. Suna, N. Ishii, A. Saeki, S. Seki, et al., "Photoconductive coaxial nanotubes of molecularly connected electron donor and acceptor layers," *Science*, vol. 314, p. 1761, 2006.
22. G. Zhang, W. Jin, T. Fukushima, A. Kosaka, N. Ishii, and T. Aida, "Formation of water-dispersible nanotubular graphitic assembly decorated with isothiouronium ion groups and its supramolecular functionalization," *Journal of the American Chemical Society,* vol. 129, p. 719, 2007.
23. J. H. Ryu, D.-J. Hong, and M. Lee, "Aqueous self-assembly of aromatic rod building blocks," *Chemical Communications*, p. 1043, 2008.

24. K. L. Prime and G. M. Whitesides, "Adsorption of proteins onto surfaces containing end-attached oligo(ethylene oxide)—a model system using self-assembled monolayers," *Journal of the American Chemical Society,* vol. 115, p. 10714, 1993.
25. J. H. Ryu, E. Lee, Y. B. Lim, and M. Lee, "Carbohydrate-coated supramolecular structures: Transformation of nanofibers into spherical micelles triggered by guest encapsulation," *Journal of the American Chemical Society,* vol. 129, p. 4808, 2007.
26. T. A. Skotheim and J. R. Reynolds, editors, *Handbook of Conducting Polymers*, CRC Press, New York, 2007.
27. P. M. George, D. A. LaVan, J. A. Burdick, C. Y. Chen, E. Liang, and R. Langer, "Electrically controlled drug delivery from biotin-doped conductive polypyrrole," *Advanced Materials,* vol. 18, p. 577, 2006.
28. S. C. Luo, E. M. Ali, N. C. Tansil, H. H. Yu, S. Gao, E. A. B. Kantchev, et al., "Poly(3,4-ethylenedioxythiophene) (PEDOT) nanobiointerfaces: thin, ultrasmooth, and functionalized PEDOT films with in vitro and in vivo biocompatibility," *Langmuir*, vol. 24, p. 8071, 2008.
29. A. Herland and O. Inganas, "Conjugated polymers as optical probes for protein interactions and protein conformations," *Macromolecular Rapid Communications*, vol. 28, p. 1703, 2007.
30. C. A. Thomas, K. Zong, P. Schottland, and J. R. Reynolds, "Poly(3,4-alkylenedioxypyrrole)s as highly stable aqueous-compatible conducting polymers with biomedical implications," *Advanced Materials,* vol. 12, p. 222, 2000.
31. S. J. Paik, Y. Park, and D. I. Cho, Roughened polysilicon for low impedance microelectrodes in neural probes," *Journal of Micromechanics and Microengineering,* vol. 13, p. 373, 2003.
32. K. A. Ludwig, J. D. Uram, J. Y. Yang, D. C. Martin, and D. R. Kipke, "Chronic neural recordings using silicon microelectrode arrays electrochemically deposited with a poly(3,4-ethylenedioxythiophene) (PEDOT) film," *Journal of Neural Engineering*, vol. 3, p. 59, 2006.
33. H. Yamato, M. Ohwa, and W. Wernet, "Stability of polypyrrole and poly(3,4-ethylenedioxythiophene) for biosensor application," *Journal of Electroanalytical Chemistry,* vol. 397, p. 163, 1995.
34. Y. H. Xiao, X. Y. Cui, J. M. Hancock, M. B. Bouguettaya, J. R. Reynolds, and D. C. Martin, "Electrochemical polymerization of poly(hydroxymethylated-3,4-ethylenedioxythiophene) (PEDOT-MeOH) on multichannel neural probes," *Sensors and Actuators B, Chemical*, vol. 99, p. 437, 2004.
35. J. Y. Wong, R. Langer, and D. E. Ingber, "Electrically conducting polymers can noninvasively control the shape and growth of mammalian-cells," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 91, p. 3201, 1994.
36. L. Dahlin, F. Johansson, C. Lindwall, and M. Kanje, "Future perspective in peripheral nerve reconstruction," *International Review of Neurobiology*, vol. 87, p. 507, 2009.
37. C. E. Schmidt, V. R. Shastri, J. P. Vacanti, and R. Langer, "Stimulation of neurite outgrowth using an electrically conducting polymer," *Proceedings of the National Academy of Sciences of the United States of* America, vol. 94, p. 8948, 1997.
38. J. Y. Lee, C. A. Bashur, A. S. Goldstein, and C. E. Schmidt, "Polypyrrole-coated electrospun PLGA nanofibers for neural tissue applications," *Biomaterials*, vol. 30, p. 4325, 2009.
39. M. S. Strano, C. A. Dyke, M. L. Usrey, P. W. Barone, M. J. Allen, H. W. Shan, et al., "Electronic structure control of single-walled carbon nanotube functionalization," *Science*, vol. 301, p. 1519, 2003.
40. M. S. Arnold, S. I. Stupp, and M. C. Hersam, "Enrichment of single-walled carbon nanotubes by diameter in density gradients," *Nano Letters,* vol. 5, p. 713, 2005.

41. N. Saito, Y. Usui, K. Aoki, N. Narita, M. Shimizu, K. Hara, et al., "Carbon nanotubes: biomaterial applications," *Chemical Society Reviews,* vol. 38, p. 1897, 2009.
42. M. P. Mattson, R. C. Haddon, and A. M. Rao, "Molecular functionalization of carbon nanotubes and use as substrates for neuronal growth," *Journal of Molecular Neuroscience,* vol. 14, p. 175, 2000.
43. E. Jan, J. L. Hendricks, V. Husaini, S. M. Richardson-Burns, A. Sereno, D. C. Martin, et al., "Layered carbon nanotube-polyelectrolyte electrodes outperform traditional neural interface materials," *Nano Letters,* vol. 9, p. 4012, 2009.
44. K. Matsumoto, C. Sato, Y. Naka, A. Kitazawa, R. L. D. Whitby, and N. Shimizu, "Neurite outgrowths of neurons with neurotrophin-coated carbon nanotubes," *Journal of Bioscience and Bioengineering*, vol. 103, p. 216, 2007.
45. E. B. Malarkey, K. A. Fisher, E. Bekyarova, W. Liu, R. C. Haddon, and V. Parpura, "Conductive single-walled carbon nanotube substrates modulate neuronal growth," *Nano Letters,* vol. 9, p. 264, 2009.
46. E. K. Schillinger, E. Mena-Osteritz, J. Hentschel, H. G. Börner, and P. Bäuerle, "Oligothiophene versus β-sheet peptide: synthesis and self-assembly of an organic semiconductor-peptide hybrid," *Advanced Materials,* vol. 21, p. 1562, 2009.
47. D. A. Stone, L. Hsu, and S. I. Stupp, "Self-assembling quinquethiophene-oligopeptide hydrogelators," *Soft Matter*, vol. 5, p. 1990, 2009.
48. S. R. Diegelmann, J. M. Gorham, and J. D. Tovar, "One-dimensional optoelectronic nanostructures derived from the aqueous self-assembly of π-conjugated oligopeptides," *Journal of the American Chemical Society,* vol. 130, p. 13840, 2008.
49. M. Kasha, H. R. Rawls, and M. Ashraf El-Bayoumi, "The exciton model in molecular spectroscopy," *Pure and Applied Chemistry*, vol. 11, p. 371, 1965.
50. P. Mesquida, C. K. Riener, C. E. MacPhee, and R. A. McKendry, "Morphology and mechanical stability of amyloid-like peptide fibrils," *Journal of Materials Science: Materials in Medicine*, vol. 18, p. 1325, 2007.
51. V. Kayser, D. A. Turton, A. Aggeli, A. Beevers, G. D. Reid, and G. S. Beddard, "Energy migration in novel pH-triggered self-assembled β-sheet ribbons," *Journal of the American Chemical Society,* vol. 126, p. 336, 2004.
52. O. Y. Kas, M. B. Charati, K. L. Kiick, and M. E. Galvin, "Manipulating association of electroactive chromophores via the use of peptidic templates," *Chemistry of Materials*, vol. 18, p. 4238, 2006.

This page intentionally left blank

PART III

Nanodevices

This page intentionally left blank

CHAPTER 11

New Developments in Nanostructured Electrode Materials for Advanced Li-Ion Batteries

Ying Wang, Chuan Cai, and Dongsheng Guan

11.1 Introduction

Recent increases in demand for oil, the associated price increases, and environmental issues are continuing to exert pressure on an already stretched world energy infrastructure. Hence, the development of new energy technologies, such as lithium-ion batteries, solar cells, fuel cells and biofuels, attracts extensive attention. As novel technologies render these technologies cheaper and safer, it is expected that they will replace fossil fuels in the coming decades. However, the new technologies have not been widely utilized, because their performance is limited by device structures and material properties. Recently, molecular or atomic engineering techniques have been used to produce nanostructured materials with enhanced properties, which leads to a variety of efficient energy conversion devices and high-density energy/power storage.

One alternative energy/power source under serious consideration is electrochemical energy production, as long as this source is designed to be more sustainable and more environmentally benign. The representative system for such electrochemical energy storage and conversion is the Li-ion battery, which is a light-weight, efficient, and rechargeable power source for electronic devices such as laptop

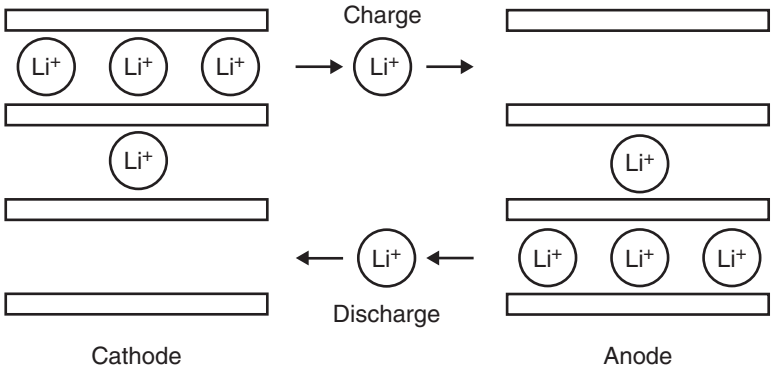


Figure 11.1 Schematic illustration of a Li-ion battery.

computers, digital cameras, and cellular phones.[1] It has also been intensively studied for use as power supplies in electric vehicles (EVs) and hybrid electric vehicles (HEVs). In spite of their high energy density,[2] Li-ion batteries have unexpectedly low power density due to large polarization at high charge-discharge rates. The polarization results from slow lithium diffusion in active materials, increasing the resistance of electrolytes as the charge-discharge process speeds up. One method to solve this problem is to develop nanostructured electrode materials that provide large surface area and short diffusion paths for ionic transport and electronic conduction.

The working mechanism of Li-ion batteries is illustrated in Fig. 11.1. A combination of a negative lithium intercalation material (anode) with another lithium intercalation material (cathode) having a more positive redox potential gives a Li-ion transfer cell. Anode and cathode are separated by the electrolyte, which is an electronic insulator but a Li-ion conductor. On charging, Li ions are released by the cathode and intercalated at the anode. When the cell is discharged, Li ions are extracted by the anode and inserted into the cathode. Electrode materials must meet three fundamental requirements to reach the goal of a high specific energy and energy density: (i) a high specific charge and charge density, that is, a high number of available charge carriers per mass and volume unit of the material; (ii) a high cell voltage, resulting from a high (cathode) and low (anode) standard redox potential of the respective electrode redox reaction; and (iii) a high reversibility of electrochemical reactions at both cathodes and anodes to maintain the specific charge for hundreds of charge-discharge cycles.

Based on these requirements, nanostructured electrode materials have broad prospects in Li-ion batteries because they offer huge surface area, short mass and charge diffusion distance, and freedom for volume change during charge-discharge cycles. Thus, they are expected to improve Li-ion intercalation properties. Many studies of the

materials have been reported hitherto, and more efforts are underway. To outline their development, we introduce a variety of nanostructured cathode and anode materials in this chapter.

11.2 Nanostructured Cathode Materials

11.2.1 Nanostructured Lithium Transition Metal Oxides

There are two main categories of cathode materials.[3,4] One is layered compounds with anion close-packed lattices; transition metal cations occupy alternate layers between anion sheets, and Li ions are intercalated into the remaining empty layers. $LiTiS_2$, $LiCoO_2$, $LiNi_{1-x}Co_xO_2$, and $LiNi_xMn_xCo_{1-2x}O_2$ belong to this group. The spinels with transition metal cations ordered in all the layers can be included in this group as well. This class of materials has the advantage of higher energy density (energy per unit of volume) owing to their more compact lattices. The other group of cathode materials has more open structures, such as vanadium oxides, the tunnel compounds of manganese oxides, and transition metal phosphates (e.g., olivine, $LiFePO_4$). In general, materials in the second group are safer and cheaper than those in the first group.

Presently, three intercalation materials are used commercially as cathode materials for rechargeable lithium batteries: $LiCoO_2$, $LiNiO_2$, and $LiMn_2O_4$. $LiCoO_2$ is the most popular among the possible cathode materials because of its easy production by solid-state or chemical approaches.[5,6] However, the specific capacity of $LiCoO_2$ ranges from 137 to 140 mAh/g, far from its theoretical capacity of 273 mAh/g.[7] In addition, Li_xCoO_2 is quite expensive and highly toxic. The reversible capacity of Li_xNiO_2 is higher than that of Li_xCoO_2,[8] but preparation of $LiNiO_2$ is more complicated than that of $LiCoO_2$, even if $LiNiO_2$ is isostructural to $LiCoO_2$.[9,10] $LiMn_2O_4$ is the third most popular cathode material for Li-ion batteries, which has advantages of low toxicity and abundant material source. In principle, $Li_xMn_2O_4$ permits the intercalation/extraction of Li ions in the range of $0 < x < 2$.[11] However, lithium metal oxides still suffer from some intrinsic limitations. For example, $LiCoO_2$ has a decent lithium diffusion coefficient, 5×10^{-9} cm^2/s,[12] whereas the conductivity of this material is as low as 10^{-3} S/cm.[13] To improve the intercalation/deintercalation kinetics of the material, it is necessary to downsize the material to achieve short diffusion distance and large surface area.

Research work on nanostructured lithium metal oxides has been reported in several recent reports. Synthesis of $LiMn_2O_4$ nanoparticles could be conducted by a sol-gel method combined with postcalcination.[14] The nanoparticles have a size of 10 nm at the calcination temperature of 350°C, whereas submicron-sized particles are

obtained at 550°C. $LiMn_2O_4$ nanoparticles were found to behave differently in different voltage ranges. In comparison with a large nonporous cathode, the nanoparticle cathode shows improved capacity and cyclability in the 3-V discharge range, whereas in the 4-V discharge region, it exhibits decreased capacity and improved cyclability. The enhancement in capacity and cyclability is due to the reduced charge-transfer resistance of the nanoparticle cathode compared to large cathode material.

A thin film of $LiCoO_2$ could be deposited at room temperature in a nanocrystalline state using planar magnetron radiofrequency (RF) sputtering.[15] Subsequent heating of the films at 300°C causes the average grain size to increase, but still within the nanosized dimensions, whereas the lattice distortion is reduced by the heating. Such a nanocrystalline film of $LiCoO_2$ annealed at low temperature demonstrates improved electrochemical performance.

Nanostructured $LiNi_{0.5}Mn_{1.5}O_4$ can be synthesized using solution methods (e.g., the Pechini method[16]) followed by heat treatment with or without the assistance of polymers,[17] It is also noteworthy that heating nanorodlike $LiNi_{0.5}Mn_{1.5}O_4$ up to 800°C can break the nanorods into nanoparticulate $LiNi_{0.5}Mn_{1.5}O_4$ with size in the range of 70 to 80 nm. Such a nanoparticulate $LiNi_{0.5}Mn_{1.5}O_4$ cathode shows good electrochemical characteristics at a wide range of rates (from *C*/4 to 15*C*) when cycled between 3.5 and 5 V.

11.2.2 Nanostructured Metal Oxides

Nanostructured Vanadium Oxides

Vanadium oxide is a typical intercalation compound because of its layered structure. For Li-ion intercalation applications, vanadium oxide offers advantages of low cost, abundant source, easy synthesis, and high energy densities. Orthorhombic crystalline V_2O_5 consists of layers of VO_5 square pyramids that share edges and corners.[18,19] The reversible electrochemical lithium intercalation into V_2O_5 at room temperature was first reported by Whittingham in 1976.[20] High Li intercalation capacity was also reported for hydrated vanadium pentoxide ($V_2O_5 \cdot nH_2O$), such as $V_2O_5 \cdot nH_2O$ xerogels[21,22] and $V_2O_5 \cdot nH_2O$ aerogels.[23] Specific energies of over 700 WAh/kg were measured for Li-ion cells with a xerogel cathode.[22]

To date, a large number of nanostructured vanadium oxides have been achieved and investigated. Spahr and coworkers first adopted a combination of sol-gel reaction and hydrothermal treatment of vanadium oxide precursor in the presence of amine to make vanadium oxide nanorolls.[24] When the amine is replaced by ammonia in synthesis, a new type of vanadium oxide nanorolls (nanotubes) with alternating interlayer distances is produced.[25] VO_x nanorolls can intercalate a variety of molecules and ions reversibly without change

in the crystalline structure. Their Li intercalation capacities have been found up to 200 mAh/g; however, there is structural breakdown during redox cycles and degradation in cycling performance due to the morphological flexibility.

Martin and coworkers have adopted a template-based method to grow polycrystalline V_2O_5 nanorod arrays.[26] The nanorod arrays deliver three times the capacity of the thin film electrode at a high rate of 200*C* and four times the capacity of the thin-film control electrode above 500*C*. Afterwards, the volumetric energy densities of V_2O_5 nanorod arrays were further improved by increasing the surface area of nanorods.[27] On the other hand, single-crystal V_2O_5 nanorod arrays were produced by a template-based electrodeposition method.[28–30] The single-crystal V_2O_5 nanorod arrays show higher capacity and enhanced rate capability in comparison with the sol-gel derived polycrystalline V_2O_5 film.

Using the similar template-based electrodeposition method but with different growth conditions, Wang et al. have prepared nanotube arrays of $V_2O_5{\cdot}nH_2O$.[31] The nanotubes were formed when using lower voltage and shorter deposition time compared to the conditions for preparing nanorods. The $V_2O_5{\cdot}nH_2O$ nanotube arrays demonstrate an initial high capacity of 300 mAh/g, about twice the initial capacity of 140 mAh/g from the $V_2O_5{\cdot}nH_2O$ film. Subsequently, the authors used a two-step electrodeposition method to prepare Ni-$V_2O_5{\cdot}nH_2O$ core-shell nanocable arrays.[32] Figure 11.2 compares the electrochemical performance of Ni-$V_2O_5{\cdot}nH_2O$ nanocable arrays, single-crystal V_2O_5 nanorod arrays, and sol-gel derived V_2O_5 films. Obviously Ni-$V_2O_5{\cdot}nH_2O$ nanocable arrays demonstrate remarkably improved capacity and rate capability in comparison with the other two. The intercalation capacities of both nanorod arrays and sol-gel films decrease rapidly as the current density increases, whereas nanocable arrays are able to retain the high capacity at high current density (discharge rate), indicating the excellent high-rate performance of nanocable arrays. As shown in Fig. 11.2*C*, Ni-$V_2O_5{\cdot}nH_2O$ nanocable array has energy density and power density significantly higher than those of the nanorod array and sol-gel film by at least one order of magnitude, which is ascribed to the enhanced surface area and the reduced internal resistance.

V_2O_5 films with novel nanosized features were further explored. Lee et al. prepared platelet and fibrillar structured V_2O_5 films using solution methods and found their initial discharge capacities are 1,240 and 720 mAh/g, respectively, which are far larger than the initial discharge value (260 mAh/g) of the conventional plain structure film.[33] Such large discharge capacity values are ascribed to the combined effects of the reduced Li^+ diffusion distance, which prevents concentration polarization of Li^+ in the V_2O_5 electrode and poor interlayered crosslinking offering more Li^+ intercalation. However, platelet and

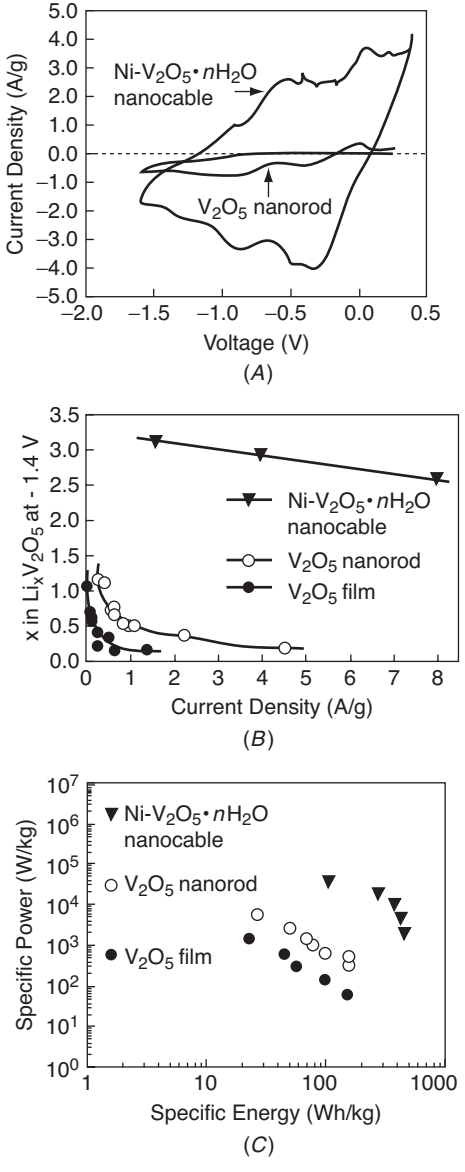


Figure 11.2 (*A*) Cyclic voltammograms of Ni-V_2O_5·nH_2O nanocable array and V_2O_5 nanorod array using a scan rate of 10 mV/s. (*B*) Relationship between current density and Li intercalation capacity of Ni-V_2O_5·nH_2O nanocable array, V_2O_5 nanorod array, and sol-gel film from chronopotentiometric measurements. (*C*) Ragone plot for Ni-V_2O_5·nH_2O nanocable array, V_2O_5 nanorod array and sol-gel film.[32]

fibrillar structured V_2O_5 films were easily degraded during electrochemical cyclic tests.

Three-dimensional ordered macroporous (3DOM) V_2O_5 electrode materials with nanometer-sized features synthesized by a colloidal-crystal-templated method were also investigated.[34] Such 3D ordered structure provides several advantageous features for Li-ion intercalation/deintercalation process: the continuous network ensures the electrical conductivity; the large open pores facilitate the transport of electrolyte; and the thin walls shorten the Li diffusion distances. Such photonic structures were later utilized for a real electrochemical cell system.[35]

Other highly porous materials include mesoporous vanadium oxide with nanometer-sized pores that permit the easy diffusion of Li ions. Liu et al. synthesized mesoporous vanadium oxide with pore sizes ranging from 3 to 4 nm by electrodepositing from a $VOSO_4$ solution in the presence of a block polyalkylene oxide polymer (P123).[36] The material delivers a capacity of 125 mAh/g at a high rate of 50*C*, corresponding to a capacitance of 450 F/g, which is comparable to that of porous carbon capacitors. Thus, the mesoporous vanadium oxide is very promising as cathode material for high-power Li-ion batteries and fills in the gap between batteries and capacitors. Moreover, the mesoporous structure provides elasticity that allows for dimensional change during Li-ion intercalation/deintercalation, and thus offers good cyclability.

Hydrothermal synthesis is another powerful tool to transform transition metal oxides into high-quality nanostructures. Li et al. have studied the synthesis and electrochemical behavior of orthorhombic single-crystalline V_2O_5 nanobelts formed by hydrothermal treatment of aqueous solutions of V_2O_5 and H_2O_2.[37] The nanobelts have widths of 100 to 300 nm, thicknesses of 30 to 40 nm, and lengths up to tens of micrometers. The authors have proposed a dehydration-recrystallization-cleavage mechanism for the formation of V_2O_5 nanobelts. A high initial discharge capacity of 288 mAh/g was found for the V_2O_5 nanobelts in a voltage range of 4.0 to 1.5 V; subsequently, the capacity decreased to 191 mAh/g for the second cycle, then remained steady for the next four cycles.

Apart from anhydrous crystalline V_2O_5 nanobelts, $V_2O_5{\cdot}0.9H_2O$ nanobelts and $V_2O_5{\cdot}0.6H_2O$ nanorolls were synthesized with hydrothermal treatment of NH_4VO_3 in the presence of various acids.[38] The $V_2O_5{\cdot}0.9H_2O$ nanobelts are tens of micrometers long, 100 to 150 nm wide, and 20 to 30 nm thick. The $V_2O_5{\cdot}0.6H_2O$ nanorolls are half-tube nanostructured as a result of incomplete scrolling. It is interesting to note that $V_2O_5{\cdot}0.6H_2O$ nanorolls show higher intercalation capacity (253.6 mAh/g) than $V_2O_5{\cdot}0.9H_2O$ nanobelts (223.9 mAh/g) under a current density of 0.6 mA/g, which can be ascribed to the higher surface area and lower water content of nanorolls. The effect of water

content on the electrochemical behavior was confirmed later by a fact that the capacities of nanorolls and nanobelts increases to 287.8 mAh/g and 307.5 mAh/g, respectively, after annealing and dehydration of these nanostructures.

Single-crystal V_2O_5 nanowires can also be achieved by a combination of hydrothermal process of polycrystalline V_2O_5 and postcalcination treatment.[39] The nanowires have diameters of 50 to 200 nm and lengths up to 100 μm and deliver a high initial capacity of 351 mAh/g. A combination of hydrothermal method and postannealing process was also used by Lutta et al. to obtain vanadium oxide nanofibers.[40] The nanofibers deliver capacities exceeding 100 mAh/g that remain stable over 10 cycles. Obviously, morphology and water content have significant effect on the electrochemical performance of nanostructured vanadium oxides. For example, Cui and coworkers found that Li diffusion constant in V_2O_5 nanoribbons is faster than that in bulk materials by three orders of magnitude, leading to a remarkable enhancement in power density (360C).[41] It can be concluded that Li-ion batteries based on nanostructured vanadium oxides have not only higher energy density but also higher power density and thus will find applications in electric and hybrid electric vehicles.

Nanostructured Manganese Oxides

Apart from traditional nanostructured layered materials that intercalate guest species between the interlayers, there are other inorganic compounds demonstrating high lithium storage capacity by electrochemically reacting with Li ions. For example, the Li-ion intercalation of nanostructured manganese oxide involves formation/decomposition of lithium oxide, which is facilitated by formation of metallic manganese. Interestingly, nanostructured manganese oxide can act as either cathode or anode materials by controlling the working voltage range. Arrays of amorphous MnO_2 nanowires have been prepared by anodic electrodeposition into alumina templates.[42] These MnO_2 nanowires function as rechargeable cathodes for Li-ion battery cells and deliver a capacity of 300 mAh/g when cycled between 3.5 and 2 V vs. Li/Li^+. Wu et al. have reported the electrochemical synthesis of interconnected MnO_2 nanowires without using any template or catalyst.[43] These interconnected MnO_2 nanowires act as cathode materials when cycled to a middle voltage (1.5 V vs. Li/Li^+). When further cycled to a low voltage (0 V vs. Li/Li^+), such nanostructures exhibit a high capacity of over 1000 mAh/g, higher than that of commercially used carbon families as anode materials.

In addition, nanostructured MnO_2 of different crystallographic types and morphologies have been synthesized through the solution route and investigated as Li-ion battery cathode materials. Nanocrystals of α-, β-, and γ-MnO_2 could be synthesized by simple hydrothermal decomposition of a $Mn(NO_3)_2$ solution.[44] Typically, β-MnO_2 crystals are produced with a variety of novel shapes,

including 1D nanowires, 2D hexagonal starlike structures and dentritelike hierarchical nanostructures. However, β-MnO_2 nanostructures show low capacity and poor cycling stability, whereas α- and γ-MnO_2 1D nanostructures demonstrate favorable electrochemical performance. α-MnO_2 nanowires deliver a capacity of 204 mAh/g when discharged to 1.5 V vs. Li/Li^+ and retain a capacity of 112 mAh/g after 20 cycles at the current rate of 50 mA/g. γ-MnO_2 nanorods deliver a capacity of more than 210 mAh/g and retain a capacity of 148 mAh/g after 20 cycles at the current rate of 50 mA/g.

In another report, Ho and Yen prepared an α/γ-MnO_2 mixed-phase coating on Pt through cathodic deposition from $Mn(NO_3)_2$ aqueous solution.[45] The morphology of such an α/γ-MnO_2 coating resembles a honeycomb consisting of flake structures in the nanometer scale. Remarkably, the α/γ-MnO_2 coating shows a gradual increase in capacity and crystalline stability after cyclic test. Its Li-intercalation capacity increases from 182 mAh/g for the first cycle to 209 mAh/g for the 10th cycle between 4.0 and 2.0 V vs. Li/Li^+. Such enhancement in capacity and crystallization after cycling is ascribed to the mixed α/γ-MnO_2 phases and the nanosized structure. As mentioned previously, bulk β-MnO_2 or nanostructured β-MnO_2 rapidly converts to $LiMn_2O_4$ spinel on Li intercalation, resulting in unfavorable electrochemical performance. However, mesoporous β-MnO_2 demonstrates a remarkably high Li intercalation capacity of 284 mAh/g, corresponding to a composition of $Li_{0.92}MnO_2$.[46] Bruce's group reported the first synthesis of mesoporous β-MnO_2 with a highly ordered pore structure and highly crystalline walls.[46] Figures 11.3*A* and 11.3*B* show typical *transmission electron microscopic* (TEM) images of mesoporous β-MnO_2, clearly demonstrating the highly ordered pore structure with a wall thickness of 7.5 nm. Figures 11.3*C* through 11.3*H* show TEM images of mesoporous β-MnO_2 after first charge, end of discharge after 30 cycles, and end of charge after 30 cycles. Both the β-MnO_2 crystal structure and the mesoporous structure are preserved on cycling. The thin walls of the mesoporous β-MnO_2 allow volume changes during Li intercalation/deintercalation, and 81% capacity is retained after 50 cycles. High capacities of more than 230 mAh/g are also reported for layered MnO_2 nanobelts, synthesized by Ma et al. using the hydrothermal treatment of Mn_2O_3 powders in an aqueous solution of NaOH.[47] The nanobelts are self-assembled into bundles with narrow size dispersion of 5 to 15 nm width and demonstrate a high capacity of 230 mAh/g up to 30 cycles.

11.2.3 Nanosized Coatings on Cathode Materials

Nanosized Coatings on Lithium Transition Metal Oxides

It should be noted that the nanoparticulate forms of lithium transition metal oxides such as $LiCoO_2$, $LiNiO_2$, or their solid solutions can react with the electrolyte and lead to safety problems. In the case of

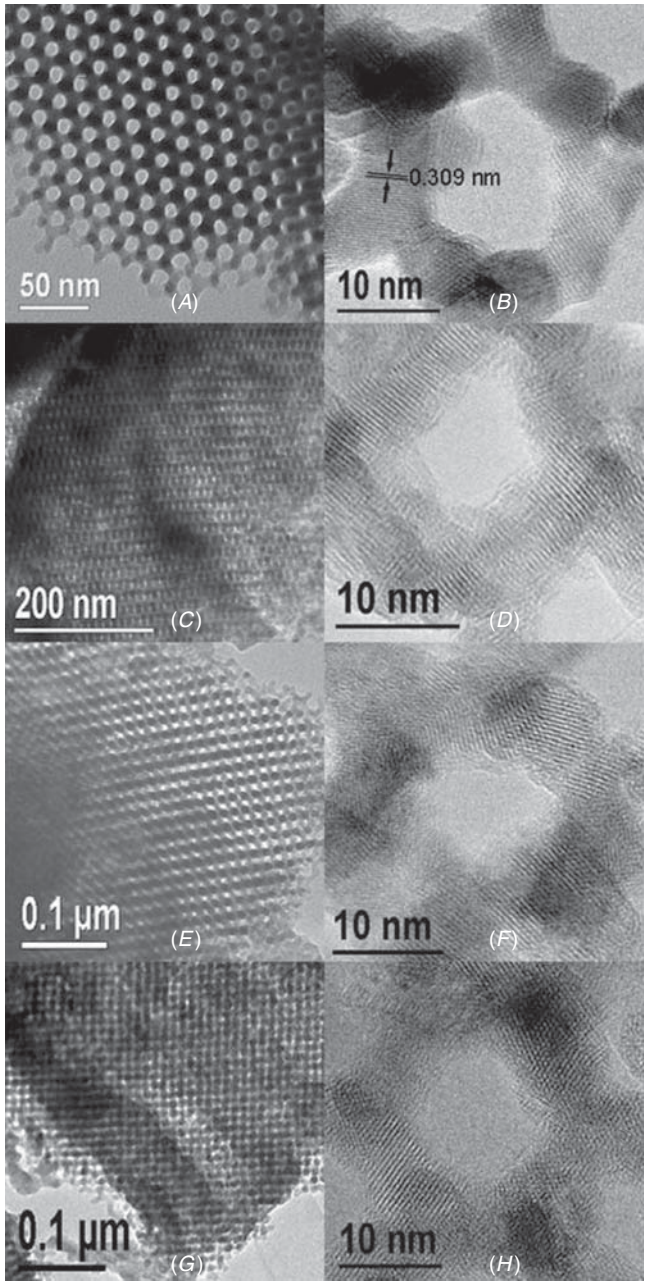


Figure 11.3 TEM and high-resolution TEM images of mesoporous β-MnO_2: (*A,B*) as prepared; (*C,D*) after discharge; (*E,F*) end of discharge after 30 cycles; and (*G,H*) end of charge after 30 cycles.[46]

$LiMn_2O_4$, the use of nanoparticles causes undesirable dissolution of Mn. Significant efforts have been made to increase the stability of these nanocrystalline lithium metal oxides. Better stability can be achieved by coating the electrode materials with a nanosized stabilizing surface layer.

As for $LiCoO_2$, coatings of various phosphates and oxides have been studied and significant improvements in capacity retention have been demonstrated. Kim et al. made an extensive study on the effect of the MPO_4 (M = Al, Fe, Sr, and Ce) nanoparticle coatings on $LiCoO_2$ cathode material.[48] They found that the extent of the coating coverage is affected by the nanoparticle size and morphology despite the same coating concentration and annealing temperature. Smaller nanoparticles of $AlPO_4$ or $FePO_4$ with a size less than 20 nm fully encapsulated $LiCoO_2$, whereas $CePO_4$ particles with a size larger than 150 nm or whisker-shaped $SrHPO_4$ only partially covered $LiCoO_2$. Not surprisingly, the $LiCoO_2$ fully covered by $AlPO_4$ or $FePO_4$ exhibits the highest intercalation capacity of 230 mAh/g in a voltage range of 4.8 and 3 V at a rate of 0.1*C*. Nevertheless, the $CePO_4$- and $SrHPO_4$-coated cathodes show better capacity retention than the $FePO_4$-coated cathode at 90°C, which is attributed to the continuous Fe metal ion dissolution at this temperature. The improvement in the electrochemical performance in the coated cathode is ascribed to the suppression of cobalt dissolution and the nonuniform distribution of local strain by the coating layer.

In addition to coatings of phosphates, surface modification of $LiCoO_2$ by coating various oxides such as ZrO_2,[49] Al_2O_3,[50] SnO_2,[51] MgO,[52] or ZnO[53] has been widely investigated. In the case of ZnO-coated $LiCoO_2$, the ZnO coating reduces the cobalt dissolution and prevents the inorganic surface films such as LiF from covering the $LiCoO_2$ particles. Moreover, the ZnO coating alleviates the cycle-life degradation caused by inappropriate conductive carbon. Based on the impedance spectra, the charge-transfer resistance of ZnO-coated $LiCoO_2$ is much smaller than that of the uncoated cathode, although the ZnO coating layer is more resistant than the $LiCoO_2$ surfaces. It can be concluded that surface modification with ZnO improves the high-voltage cyclability of the $LiCoO_2$ cathodes.

Replacing the liquid electrolyte with nonflammable solid electrolyte such as sulfide electrolyte is also a solution to the safety problems. However, the energy densities and power densities of solid-state lithium batteries are relatively low for practical applications. One way to improve the rate capability of solid-state batteries is to add a buffer film with a thickness in nanometer scale between the electrode and electrolyte materials. A thin layer of $Li_4Ti_5O_{12}$ with thickness of a few nanometers was chosen to be coated on the $LiCoO_2$ cathode.[54] The $Li_4Ti_5O_{12}$ is also an Li intercalation material that ensures the electronic conduction; however, this material intercalates Li ions at voltages lower than 1.5 V and thus does not act as an intercalation material

in the voltage range of $LiCoO_2$. The power densities of the solid-state batteries with the thin $Li_4Ti_5O_{12}$ layer between the $LiCoO_2$ cathode and sulfide electrolyte are greatly increased and comparable to those of commercial lithium batteries, which is attributed to the suppression of the Li-ion transfer.

$LiMn_2O_4$ or substituted $LiMn_2O_4$ is very attractive as a cathode material because it is safer and cheaper than $LiCoO_2$. However, this material suffers from capacity fading, especially at elevated temperatures. Coating of nanosized oxides on $LiMn_2O_4$ will help to improve its cycling performance. The electrochemical behavior of nanosized ZnO-coated $LiMn_2O_4$ was examined at 55°C.[55] After 50 cycles at 55°C, the coated $LiMn_2O_4$ shows capacity retention of 97%, much higher than the capacity retention (58%) of the bare cathode. ZnO coating collects HF from the electrolyte and thus decreases the Mn dissolution in the electrolyte, then subsequently reduces the interfacial resistance.

Similarly, coating of amorphous ZrO_2 on $LiMn_2O_4$ can improve the high-temperature cyclability by picking up acidic species from electrolyte.[56] Besides, the ZrO_2-coated $LiMn_2O_4$ exhibits tremendously improved cycling stability at high rates up to 10*C* because of the following mechanisms. First, ZrO_2 can form a few stable phases with Li and thus amorphous ZrO_2 matrix possibly possesses high solubility of Li. Therefore, the ZrO_2 coating can act as a highly Li-conducting solid electrolyte interface, which reduces the interfacial resistance. Second, the rigid oxide coating strongly bonds to $LiMn_2O_4$, which tolerates the lattice stress resulting from volume expansion during lithium intercalation. Last, ZrO_2 can collect HF from electrolyte to reduce Mn dissolution as ZnO does.

Nanosized Coatings on Lithium Phosphates

Lithium phosphate is presently the focus as the cathode for Li-ion batteries, because it is inexpensive, abundantly available, environmentally friendly, and thermally stable in the fully charged state, and it has a large theoretical capacity of 170 mAh/g. However, the low electronic conductivity (10^{-9} to 10^{-5} S/cm) of $LiFePO_4$ seriously restricts the application of lithium phosphate to high power lithium batteries.[57,58]

One effective method to improve the conductivity is to adopt conductive coatings deposited on the surface of $LiFePO_4$. Most coatings are carbonaceous and deposited during the synthesis process. Pioneering work on carbon-coated $LiFePO_4$ was carried out by Ravet et al.[59,60] Sucrose was used as one carbon source[60] and was added on the initial hydrothermal samples[61] or during pyrolysis.[62] Other methods include thermal decomposition of pyrene [63] or citric acid based sol-gel processing.[64] It should be noted that the electrochemical properties of $LiFePO_4$ are influenced by the quality of carbon coatings.[65] The structure of carbon can be controlled by the use of additives during $LiFePO_4$

synthesis. $LiFePO_4$ coated with the more graphitic carbon has higher conductivity and shows better electrochemical performance. Another factor that influences the electrochemical performance of $LiFePO_4/C$ composites is the porosity. Gaberscek and coworkers prepared microsized porous $LiFePO_4/C$ particles with different morphology by using different techniques such as solid-state or sol-gel methods.[66] The composites prepared at a relatively high heating rate (>5 K/min) have interconnected pores and show the best electrochemical performance, for example, more than 140 mAh/g at $C/2$ rate during continuous cycling.

In addition to carbon coating, metal coating such as silver has been successfully used to increase the conductivity as well.[67] Another type of coating is a conductive inorganic layer such as metallic Fe_2P, as investigated by Rho et al.[68] In their study, mixture of Fe_2P and FeP were deposited on the surface of the $LiFePO_4$ along with carbon and the by-product Li_3PO_4 by surface reduction reactions. Fe_2P is coated directly on the $LiFePO_4$, whereas carbon and Li_3PO_4 sit on the outer surface of the crystallites. Such surface layer structure facilitates significantly improved rate capabilities and superior cyclability: a high capacity of 105 mAh/g is achieved at a very high rate of $14.8C$. Recently, Wang and Su's group designed a $LiFePO_4$ spherical structure coated by a π-bond character planar polymer—polyacene (PAS)—by pyrolysis of the phenol-formaldehyde resin.[69] The conductivity of $LiFePO_4$-PAS structure is drastically increased to 10 S/cm. High capacities and excellent cycling performance are achieved for the $LiFePO_4$-PAS structure in a wide temperature range of –20 to 60°C. In a similar manner, electronically conducting RuO_2 was used as an oxidic nanoscale interconnect for carbon-containing porous $LiFePO_4$ to improve electrode performance.[70] RuO_2 with a particle size of about 5 nm was deposited on the carbon-$LiFePO_4$ with an average pore size of 50 nm by using cryogenic decomposition of RuO_4 at low temperature. The resulted C-$LiFePO_4/RuO_2$ composite maintains the morphology and structure of the original C-$LiFePO_4$, as revealed by high-resolution TEM images in Fig. 11.4. Nanosized RuO_2 as an oxide adheres well with oxides such as $LiFePO_4$, simultaneously ensuring good contact with carbon. Hence, RuO_2 repairs the incomplete carbon network in porous $LiFePO_4$ and thus improves the kinetics and rate capability of the composite. It is found that the original C-$LiFePO_4$ electrode shows decent performance at low current rates, but the performance deteriorates at high current rates. The C-$LiFePO_4/RuO_2$ shows improved electrochemical behavior at high rates.

The problems of low electronic conductivity and slow diffusion of Li ions in $LiFePO_4$ can be further alleviated by modifying with conductive species and by minimizing particle size simultaneously. For example, a nanocomposite of $LiFePO_4$ with a carbon xerogel could be formed from a resorcinol-formaldehyde precursor. This

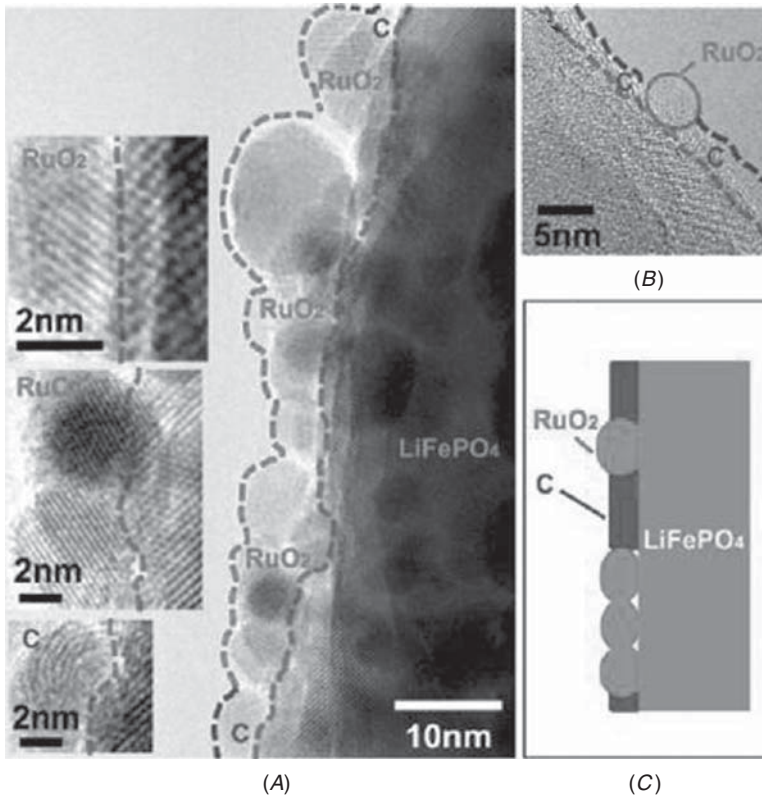


Figure 11.4 (*A*,*B*) High-resolution TEM images of C-$LiFePO_4$ after RuO_2 coating. (*C*) Schematic of the repair of the electronically conducting network of carbon on porous $LiFePO_4$ by nanosized RuO_2.[70]

nanocomposite achieves 90% theoretical capacity at $C/2$ with very good stability at room temperature.[71] Such excellent electrochemical performance is due to modification with carbon and control of particle size to the nanometer scale.

11.2.4 Nanostructured Composites

Nanostructured Carbon-Oxide Composites

As noted previously, a severe limitation for most cathode materials is their poor electronic conductivity. To improve the electrochemical kinetics, the cathode materials could be embedded within an electronically conducting network, for example, some thin coating of conductive material. The coatings must be thin enough, within nanoscale so that ions can penetrate through them without appreciable polarization. Furthermore, the internal electrical field generated by electrons

may enhance the ionic motions.[72] Such surface modifications alleviate the problem of low electronic conductivity; at the same time, reducing the size of the active material would shorten the diffusion length for lithium.

One of the commonly studied carbon-based composites is carbon/vanadium oxide composite. C-coated V_2O_5 nanoparticles can be synthesized via burning off C-coated V_2O_3 nanoparticles around 400°C in air.[73] The thickness and weight percentage of carbon can be manipulated by varying the conditions of the burning process. The optimal carbon content is found to be 2 to 3% by weight. Because of the carbon coating, these C-V_2O_5 nanoparticles have good interparticle electrical contact and do not have the usual drawbacks of nanoparticles, such as poor active mass integrity and high surface reactivity. Therefore, C-coated V_2O_5 nanoparticles are found to have higher capacity, better rate capability, and better cyclability than V_2O_5 microparticles or nanoparticles. The Li intercalation capacity of C-V_2O_5 nanoparticles reaches 290 mAh/g at high rates. Later, higher capacities exceeding 400 mAh/g at high rates were achieved with V_2O_5 nanoribbons/carbon nanotube nanocomposites.[74]

Apart from vanadium oxides, some nanostructured lithium vanadium oxides have also been reported to form nanocomposites with carbon, which exhibit excellent electrochemical characteristics. For example, mixing the precursor of $Li_{1+\alpha}V_3O_8$ with a suspension of carbon black resulted in nanocomposites of $Li_{1+\alpha+x}V_3O_8/\beta$-$Li_{1/3}V_2O_5$/C.[75] β-$Li_{1/3}V_2O_5$ was a by-product formed when the initial $Li_{1+\alpha}V_3O_8$ was reduced by carbon. Here, carbon particles play critical roles as reducing agents, as growth-limiting agents to restrict the electroactive material within the nanoscale, and as electronically conducting agents. The $Li_{1+\alpha+x}V_3O_8/\beta$-$Li_{1/3}V_2O_5$/C nanocomposite shows significantly better electrochemical performance in comparison with the standard $Li_{1+\alpha}V_3O_8$. Similarly, acetylene black was used to prompt the reduction of potassium permanganate, yielding amorphous manganese oxide/carbon composites.[76] The as-prepared composite delivers a high capacity of 231 mAh/g at a current density of 40 mA/g, showing good electrochemical performance at high rates.

A number of lithium phosphate/carbon composites have also been studied as cathode materials for lithium batteries, including those of general formula $LiMPO_4$ (M = Fe, Mn, Co, Ni)[77] and $Li_3V_2(PO_4)_3$.[78] Among the C-coated $LiMPO_4$ (M = Fe, Mn, Co, Ni) composites, the $LiFePO_4$/C with surface carbon coating of 1.8 wt% achieves an electronic conductivity of 10^{-2} S/cm and shows the best electrochemical performance. In addition, to improve the electronic conductivity of $Li_3V_2(PO_4)_3$, $Li_3V_2(PO_4)_3$ crystallites were wrapped within a conductive carbon network to form a nanocomposite that delivers almost full capacity at high rates.[78] Two Li ions per formula unit are completely extracted in three steps to give a theoretical capacity (100%) of 132 mAh/g at a rate of $C/5$. A theoretical capacity of 95%

is still achieved at a high rate of 5*C*. The sequence of phase transitions between two single phases shows the very low degree of polarization in the discharge curve owing to the facile ion and electron transport. When cycled between 3.0 V and 4.8 V, the $Li_3V_2(PO_4)_3/C$ composite delivers a specific energy density of 2330 mWh/cm^3, comparable to that of $LiCoO_2$ (2750 mWh/cm^3) or $LiFePO_4$ (2065 mWh/cm^3).

Nanostructured Polymer-Oxide Composites

Over the past two decades, there has been great interest in the conductive polymer/transition metal oxide nanocomposite. The hybrid material consists of conductive organic polymers (e.g., polyacetylene, polyaniline, and *polypyrrole*, PPy) interleaved between the layers of an oxide lattice such as V_2O_5. Both oxide and polymer are electrochemically active and this feature makes the polymer/oxide nanocomposite very attractive as the cathode material for lithium batteries. The *layer-by-layer* (LbL) technique, based on physical adsorption of oppositely charged layers, has been widely used to prepare V_2O_5 nanocomposites alternating with polymer layers. One popular example is V_2O_5/polyaniline nanocomposite film fabricated by the LbL technique: the intimate contact between the oxide and polymer within nanoscale results in an improved intercalation capacity.[79] Later, V_2O_5 nanocomposite alternating with blends of chitosan and *poly(ethylene oxide)* (PEO) were prepared using the LbL technique, and the charge storage capability in such nanoarchitectures was investigated.[80] A small amount of chitosan (1%) was added to blend with PEO because the adsorption of alternate layers of PEO and V_2O_5 is not efficient. The V_2O_5/blend showed higher capacity and intercalated 1.77 moles of lithium per mole of V_2O_5. The enhanced electrochemical performance of V_2O_5/blend in comparison with V_2O_5/chitosan is due to a larger number of electrochemically active sites and faster lithium diffusion within the host material. At 20 mV/s, the charges injected were 3.29 mC/cm^2 and 8.02 mC/cm^2 for V_2O_5/chitosan and V_2O_5/blend, respectively.

In a more recent report, polyaniline homogeneously distributed into V_2O_5/polyaniline nanocomposite was found to stabilize the capacity.[81] In this study, a reverse micelle method was used to prepare V_2O_5/polyaniline nanofibers that exhibit improved cycling performance compared to the V_2O_5 nanofibers.[81] The V_2O_5/polyaniline nanofibers containing 30 mol% polyaniline deliver a steady capacity of about 300 mAh/g without morphology change over 10 cycles, whereas the V_2O_5 nanofibers do not retain the morphology after cycling. Some V_2O_5/polymer nanocomposite shows lower storage capacity but better cycling stability compared to pure nanostructured V_2O_5.[82] As reported by Reddy et al., $PVP_xV_2O_5$ ($x = 0.5, 1$) nanobelts exhibit lower capacity but better cyclability compared with V_2O_5 nanobelts. They studied the interaction between the oxide and

polymer and found that the hydrogen atoms in PVP are hydrogen-bonded with the oxygen atoms of the V = O bonds of V_2O_5 nanobelts, which effectively shields the electrostatic interaction between V_2O_5 interlayer and Li ions. As discussed earlier, polymers can be intercalated between the interlayers of V_2O_5; on the other hand, V_2O_5 can be interleaved within a block polymer matrix as well.[83] Mayes et al. used a sol-gel method to create continuous and amorphous V_2O_5 phase within the *poly(oligooxyethylene methacrylate)* (POEM) domains of a poly(oligooxythylene methacrylate)-block-poly(butyl methacrylate) (POEM-*b*-PBMA) copolymer (70 wt% POEM) up to weight ratios of 34% V_2O_5.[83] The resulting nanocomposite film is flexible and semitransparent and the redox activity of V_2O_5 is preserved in such nanocomposite.

Cathode materials other than V_2O_5 can form nanocomposites with conductive polymer as well. Poly(ethylene oxide) (PEO) was used as an electroactive polymeric binder to mix with carbon containing $Li_{1.1}V_3O_8$.[84] The resulted composite electrode shows a capacity of 270 mAh/g at a rate of $5/C$, higher than the capacity (180 mAh/g at $C/5$ rate) of the standard electrode without PEO. Such improved electrode performance is attributed to the more efficient charge-carrier collection within the composite electrode. Among all known cathode materials, elemental sulfur is the cheapest and has the highest theoretical capacity density of 1672 mAh/g assuming a complete reaction to yield Li_2S.[85]

However, Li/S cells suffer from low utilization of active material, because electrochemical reaction with the interior active materials is hindered by the insulated reaction products covering the sulfur particles. Moreover, the dissolved polysulfides transfer onto the surface of the Li anode, causing lithium corrosion and poor rechargeability of Li/S cells. To overcome these two problems, nanodispersed composites with sulfur embedded in a conductive polymer matrix were achieved by heating the mixture of *polyacrylonitrile* (PAN) and sublimed sulfur.[86,87] The composite also show excellent cycling life due to the suppressed dissolution of polysulfides into the electrolyte and thus demonstrates great potential as a cathode material for lithium batteries.

Nanostructured Metal-Oxide Composites and Other Composites

The third most popular composite electrode is metal-based cathode material, exemplified by the Ni-$V_2O_5{\cdot}nH_2O$ core-shell structure discussed in Section 11.3.1. Accordingly, Wang et al. synthesized Ag-$Ag_{0.08}V_2O_5{\cdot}nH_2O$ composite films by dispersing silver nanowires into $V_2O_5{\cdot}nH_2O$ matrix.[88] The composite film is found to deliver twice the capacity of the $V_2O_5{\cdot}nH_2O$ xerogel film, due to further amorphization of $V_2O_5{\cdot}nH_2O$, the increased porosity, and the enhanced electronic conductivity. In a similar concept, $LiCoO_2$/Ag

multilayer film was fabricated by magnetron sputtering and showed enhanced rate capability in comparison with $LiCoO_2$ film of the same thickness.[89] The thickness of the Ag layer is restricted within nanoscale, and the rate capability of the multilayer film improves with the increased thickness of the Ag layer as a result of the enhanced electronic conductivity.

More recently, oxide/metal/polymer composites have been obtained showing very good electrochemical performance. One example is freestanding V_2O_5/Pt/PVA multilayer films with the thicknesses of the V_2O_5, Pt, and PVA at 22, 57, and 704 nm.[90] Other types of composite structures include oxide/oxide composite, such as a double-layer cathode composed of a $LiCoO_2$ main layer with a $LiFePO_4$ sublayer on top of an Al current collector, which shows better tolerance against overcharging than other electrodes including ($LiCoO_2$-$LiFePO_4$ mixture)/Al single layer and $LiFePO_4$/$LiCoO_2$/Al double layer.[91] The enhanced electrochemical performance is attributed to a large increase in the ohmic resistance of the delithiated Li_xFePO_4 layer, which shuts the charging current down during overcharging without shutdown of the separator. The third type of composite structure is polymer/carbon nanocomposite, such as a *polyaniline* (PANI)/multiwalled *carbon nanotube* (CNT) composite synthesized via in situ chemical polymerization. This nanocomposite is utilized as a cathode material in a lithium metal-polymer cell assembled with ionic liquid electrolyte.[92] Such a cell demonstrates a maximum discharge capacity of 139 mAh/g with good cyclability and shows decent high rate performance (111 mAh/g at the 2.0*C* rate).

11.3 Nanostructured Anode Materials

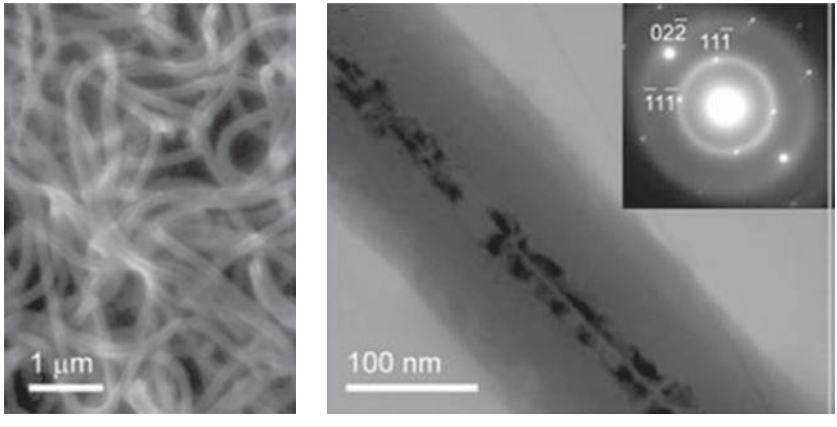
11.3.1 Nanostructured Single Substance

In the following sections, we will introduce nanostructured anode materials, which are crucial for the capacity and cycling life of Li ion batteries as well.[93] Graphite has been one of the most popular commercially available anode materials for Li-ion batteries, but its theoretical capacity is low (372 mAh/g).[94] Therefore, there has been an effort to identify alternative materials for Li-ion batteries with higher energy density, higher power density, and longer lifespan.[95] The materials are generally divided into three groups: (i) single substances such as Si, Sn, and Ge; (ii) oxides such as SnO_2, CuO, TiO_2, Co_3O_4, and NiO; and (iii) composites such as Si-C, Sn-C, SnO_2-C, transition metal oxides (MO, where M is Ti, Ni, Co)–C, SnSb-C, and Si-TiN. Drastic volume change of anode materials during Li-ion intercalation/deintercalation cycling because of their large capacities may destroy their crystal structure and cause significant capacity loss and degradation. One solution to this

problem is to create nanosized anode materials because of their advantages such as large surface area, short diffusion length, and great tolerance to volume variation.

Silicon is considered one of the best substitutes for carbon anodes, because of its high theoretical capacity (4200 mAh/g), low cost, and abundance.[96–98] However, a 400% volume variation of bulk Si electrodes during insertion/extraction processes[99] destroys the structure of the electrode and causes huge capacity loss. A way to alleviate this problem is to produce nanostructured silicon. Cui Group has grown Si nanowires (NWs) directly on the metallic current collector substrate.[100] The charge capacity reaches 4,277 mAh/g, and discharge capacity is 3124 mAh/g in the first cycle. Crystalline-amorphous (c-a) core-shell Si nanowires have been achieved to further improve the power rate and cycling capacity.[95] Figure 11.5 shows the morphology and structure of the Si NWs after cycling. Crystalline Si (c-Si) still exists after 15 cycles with cutoff of 150 mV. Amorphous Si (a-Si) shows better cycling stability due to homogeneous volume variation,[101–104] and the c-Si core functions as mechanical support and electrical contact.

Sn has a lower active voltage (0.3 V) than that of Si (>0.5 V),[105] and Li/Sn alloy has a high specific capacity of 990 mAh/g.[106] But drastic volume variation (259%) still limits its practical applications.[107] Zhang et al. have used the laser-induced vapor deposition method to synthesize nanosized Sn powders, which deliver a charge capacity of 904.4 mAh/g in the first cycle at a current density of 0.2 mA/cm^2.[108] Ge is also a promising anode material because the diffusion of Li in Ge



(*A*) (*B*)

Figure 11.5 Images of the crystalline-amorphous core-shell Si NWs after cycling at 0.2*C* (0.85 A/g) with cutoff voltage of 150 mV: (*A*) Scanning electron microscope image of NWs after 15 cycles. (*B*) TEM and selected area electron diffraction (SAED, *inset*) images of a NW after 15 cycles.[95]

is 400 times faster than that in Si at room temperature.[109] Ge NWs can be grown directly onto metal current collector substrates as well.[110] The electrode exhibits a discharge capacity of 600 mAh/g at a rate of $2C$, together with excellent cycling stability.

11.3.2 Nanostructured Oxides

Nanostructured Tin Oxides

SnO_2 is an attractive anode material because SnO_2 can intercalate twice Li (781 mAh/g) compared to graphite.[111,112] An alloying/dealloying mechanism for the interaction between SnO_2 and Li ions is proposed[113]:

$$4Li^+ + SnO_2 + 4e \Rightarrow Sn + 2Li_2O$$
$$xLi^+ + Sn + xe \Leftrightarrow Li_xSn\,(0 \le x \le 4.4)$$

However, tin oxide anodes also have a problem of drastic volume change during cycling.[113,114] Nanosized tin oxides are able to maintain considerable reversible capacity.

As Besenhard et al. pointed out, when Li incorporates with the nanoparticles, in fact their dimensions change a little.[114] Nanostructured tin oxides also enhance their capacity as they have more surface defects and surface area.[115] Nanocrystalline SnO_2 can be prepared by using a polyol-mediated method[116] or using a combination of sol-gel processing and microwave synthesis method.[117] A simple one-step template-free method and a spray pyrolysis technique have been employed to grow hollow SnO_2 nanospheres[118] and spherical porous SnO_2,[119] respectively. These incompact but interconnected structures help to reduce the volume variation. Other SnO_2 nanostructures include single-crystal SnO_2 nanowires synthesized by Seong et al.; however, the single-crystalline structure changes to a polycrystalline structure during cycling.[120] Naichao Li et al. have fabricated SnO_2 nanofibers that resemble the bristles of a brush by using a template-based method.[121] Figure 11.6 shows cycling performances of SnO_2 thin film and nanostructured SnO_2 electrodes. The discharge capacity increases gradually to 760 mAh/g at a rate of $4C$. The same situation is also found when the rate is $8C$ and even $58C$. It may be caused by growth of fibrils at the end of those "bulbs." The fibrils lead to an increase in the surface area, supplying more active sites to Li. Thermal evaporation method has also been used to prepare SnO_2 nanowires.[115] Interestingly, some nanoparticles appear after the Li-ion intercalation/deintercalation processes, resulting in a structure of nanowires dotted with nanoparticles. Figure 11.7 shows a TEM image of a single-crystalline SnO_2 nanowire after electrochemical cycling. The nanoparticles are separate from each other and exposed

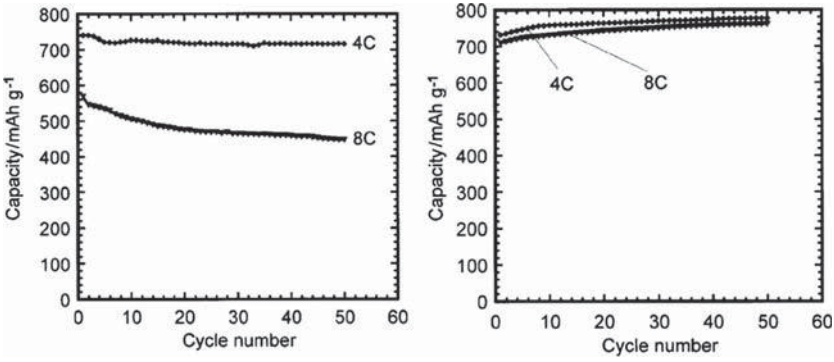


Figure 11.6 Discharge capacity versus cycle number for (*A*) SnO_2 thin-film and (*B*) nanostructured SnO_2 electrodes.[121]

to the electrolyte, offering more volume change flexibility during Li-ion intercalation and deintercalation, and thus the effect of volume variation is alleviated.

Nanostructured Transition-Metal Oxides

In addition to tin oxides, nanostructured transition-metal oxides such as TiO_2, CuO, NiO, and Co_3O_4 are also good candidates for anode materials.[122] The nanostructured oxides electrodes all deliver higher capacities than graphite-based anodes.[2]

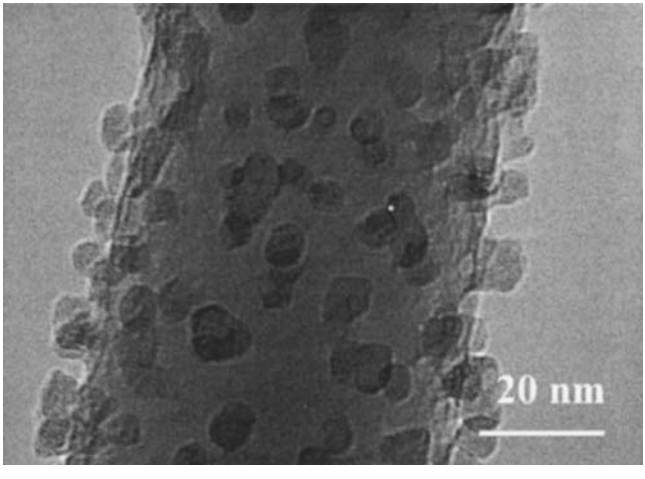


Figure 11.7 TEM image of a single-crystalline SnO_2 nanowire after electrochemical cycling.[115]

Titanium oxide is a good host for Li ions because of its low cost and nontoxicity, high reversible capacity,[123] and high operating voltage (~1.7 V vs. Li^+ (1M)/Li).[124] TiO_2 nanoparticles can be synthesized through sol-gel routes.[124,125] As the size of TiO_2 nanoparticles increases, their accommodating ability for volume change decreases and their discharge capacity becomes lower.[126] 1D TiO_2 nanostructures show higher capacity than TiO_2 nanoparticles. Kim and coworkers have prepared TiO_2 nanotubes with different mass densities.[126] The electrode delivers almost constant capacity of ~260 mAh/g at different current densities (0.5, 1, 5, 10*C*) when the density of electrode is low (0.5 or 1 g/cm^3). H. Qiao et al. have reported microspheres consisting of rutile TiO_2nanorods.[127] This hierarchical porous structure has large specific surface area and provides an excellent diffusion pathway to Li ions. Additionally, crystalline TiO_2 shows better cycling stability than amorphous TiO_2 due to less surface defects and Li-ion trap sites.

Cupric oxides have a higher retention capacity than titanium oxides. Hollow CuO materials have been developed with different morphologies such as hollow cubes, hollow spheres, and urchin-like particles by oxidizing the Cu_2O nanocubes.[128] The electrode based on urchin-like particles shows the best electrochemical performance, which delivers a charge capacity of ~580 mAh/g over 50 cycles. Thermal precursor deposition can be used to obtain CuO nanoparticles of different sizes that show phenomena similar to those present in TiO_2nanoparticles.[129] The discharge capacity of CuO nanoparticles decreases as the size of the nanoparticles increases during the first cycle. But for larger CuO nanoparticles, most capacity is retained in the following cycles. CuO nanorods with a diameter of 10 to 60 nm have also been synthesized to investigate their electrochemical performance.[130]

A conversion reaction mechanism for the interaction between Li ions and transition metal oxides is given as follows[121]:

$$\begin{aligned} MO_x + 2xLi^+ + 2e^- &\rightarrow xLi_2O + M \\ 2Li &\leftarrow 2Li^+ + 2e^- \\ \hline MO_x + 2xLi &\leftrightarrow xLi_2O + M \end{aligned}$$

This mechanism may be only applicable to nanomaterials because bulk Li_2O is electrochemically inert. The reactivity of Li_2O increases when Li_2O nanoparticles are surrounded by nanosized metals.

Nickel oxides are also used as anode materials in Li-ion batteries. Plasma assisted oxidation method, chemical bath deposition, and thermoprecursor deposition have been utilized to prepare vertically aligned NiO nanowalls,[131] porous NiO film composed of interconnected nanoflakes,[132] and spherical clusters of NiO nanoshafts,[133]

respectively. The three structures show better electrochemical properties than nanoparticles[122] and dense films of NiO, which is ascribed to the larger specific surface area and shorter diffusion length. Among them, the NiO nanowalls show the best electrochemical performance with a capacity of approximately 680 mAh/g.

With a theoretical capacity twice that of graphite, Co_3O_4 attracts much attention. Nanosized Co_3O_4 powders have been prepared by chemical decomposition[134] and a spray conversion process.[135] However, the reversible discharge capacity (360 mAh/g) of the powders is low, and their cycling stability is poor. Lou et al. have used a self-supported formation process to obtain needlelike Co_3O_4 nanotubes that show a good cycling stability.[136] The charge capacity of these Co_3O_4 nanotubes remains nearly constant over 30 cycles. In addition, porous Co_3O_4 nanostructured thin films composed of nanoflasks[137] and nanotubes formed from nanoparticles[138] can be fabricated through electrodeposition and sonication, respectively. Similarly, the porosity of these thin films and nanotubes leads to high specific surface area and a subsequent increase in capacity. For example, the Co_3O_4 nanotubes show a high reversible capacity of 1200 mAh/g.

Other Nanostructured Oxides

Lithium cobalt oxide is usually recognized as a conventional cathode material, whereas cobalt oxides are found to exhibit superior electrochemical performance as an anode material. In the same sense, $LiFePO_4$ is one of the most popular cathode materials, whereas $FePO_4$ is reported as a promising anode material. Dongyeon Son et al. have prepared $FePO_4$ nanoparticles using cetyltrimethylammonium bromide as cationic surfactant.[139] The charge capacity of the $FePO_4$ electrode is retained at 375 mAh/g over 30 cycles, which is more than twice the theoretical capacity of $LiFePO_4$ as a cathode material (170 mAh/g). $InVO_4$ has attracted some research interest because of its high intercalation capacity and good cyclability among orthovanadate compounds.[140] A capillary-enforced template-based method has been utilized to prepare $InVO_4$ nanotube arrays,[141] which deliver a high charge capacity of 600 mAh/g at a specific current density of 110 mA/g.

11.3.3 Nanostructured Composites

Nanostructured Silicon-Carbon Composites

Dispersing Si uniformly in a host matrix (e.g., carbon black[142]) is another effective method to reduce drastic volume change of Si during Li-ion intercalation/deintercalation. Carbon not only is a conductive additive, but also supplies ductile a host matrix for dispersing Si nanoparticles.[142] Besides, carbon contributes to the capacity because Li can be intercalated into carbon as well.[143] Hence, the Si-C composite shows higher capacity than bare carbonaceous material, and better

cycling stability than the unsupported Si electrode.[144] Shu et al. have synthesized a cagelike CNTs/Si composite using a chemical vapor deposition method.[145] Si particles are wrapped by a cage formed from tortile CNTs in this structure. The CNTs improve the conductivity and are covered by a *solid electrolyte interphase* (SEI) film that improves the cycling stability of the electrode. The Si-C composite can also be prepared by dispersing nanocrystalline Si in the carbon aerogel.[144] This type of Si-C composite delivers a discharge capacity of about 2,000 mAh/g at *C*/10 rate in the first cycle and a nearly constant capacity of 1450 mAh/g after 50 cycles.

Moreover, composites with other complex structures can be used to increase the capacity and enhance the cycling stability of anode materials as well. A composite with a silicon/graphite/CNTs structure has been prepared by the ball milling technique.[143] This preparation method generates structural defects in *multiwalled carbon nanotubes* (MWNTs) and leads to MWNTs with shorter length. The structural defects benefit the storage, and the shorter length of MWNTs facilitates the diffusion of Li.[146] MWNTs are added into silicon/graphite composite because of its remarkable resiliency[147,148] and good electric conductivity.[149] Moreover, the MWNT network can wrap the flaked graphite particles tightly, which further alleviates the effect of the volume variation. A carbon-coated nano-Si dispersed oxide/graphite composite material has been prepared by Heon-Young Lee et al.[150] The graphite and the inactive oxide function as the elastic matrix. The carbon coating not only suppresses side reactions involving the electrolyte and surface graphite particles, but also enhances the electrical contact between silicon and graphite.

Nanostructured Tin-Carbon Composites

In addition to the Si-C composites, Sn-C composites also show excellent electrochemical performance as anode materials. Sn has a very large theoretical capacity (994 mAh/g), because 1 mol of Sn can store 4.4 mol of Li.[151] However, the Sn electrodes suffer from poor cyclability. One way to improve the cycling stability is to disperse Sn into a carbon matrix that functions as a buffer. Guo et al. have recently prepared the Sn-C composite by embedding Sn nanoparticles in the mesopores of hard carbon spherules.[152] The initial columbic efficiency (charge capacity divided by discharge capacity) is increased remarkably because of the nano-Sn induced deposition of SEI film. Kumar et al. have reported their synthesis of tin-filled carbon nanotubes via a hydrothermal reduction process and a $NaBH_4$-reduction process.[153] Figure 11.8 shows cycling performances of nano-tin and tin-filled carbon nanotubes.[153] Both overall capacity and cycling stability are improved compared to unsupported Sn and MWNT. The electrode obtained from hydrothermal method exhibits a capacity of 1082 mAh/g, and

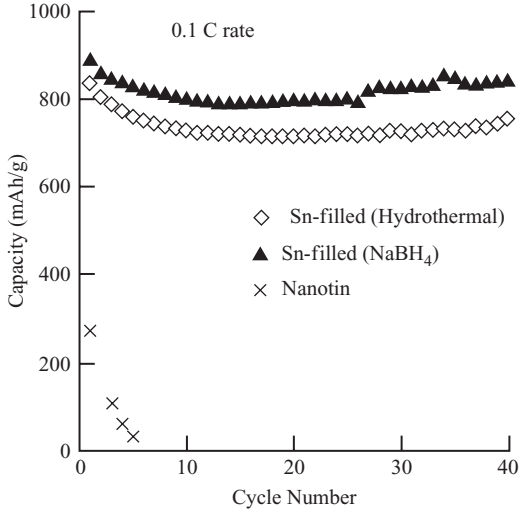


Figure 11.8 Cycling performances of nanotin and the tin-filled carbon nanotubes.

the electrode synthesized from the $NaBH_4$-reduction process delivers a capacity of 1585 mAh/g at a rate of 0.1*C*. Their capacities remain 754 and 844 mAh/g over 40 cycles, respectively. Coating Sn with carbon is another method to prepare the Sn-C composite. Carbon-coated Sn nanoparticles have been synthesized via the hydrothermal method[154] or by mechanical mixing and heating the precursor subsequently.[155]

Nanostructured Tin Oxide-Carbon Composites

The electrochemical performance of tin oxides can also be improved by forming composites with carbonaceous materials. The carbonaceous material serves as the buffering matrix to hinder the agglomeration of nanoparticles and enhance the electrical contact; it also delivers additional capacity at the same time.[156–160] In the work reported by Du et al., polycrystalline SnO_2 nanotubes have been grown on the CNTs layer by layer.[161] These nanotube electrodes exhibit large reversible capacities due to the high specific surface area. SnO_2 can also be dispersed in multiwalled CNTs by using a one-step thioglycolic-acid-assisted wet chemical method[162] or through the oxidation process in supercritical carbon dioxide-methanol solution.[163] The thickness of SnO_2 coating can be controlled by changing pH value and hydrolysis time.[162] Qiao et al.[164] and Chen et al.[105] have both reported SnO_2-C composites with core-shell structures prepared by using the one-pot solvothermal method and the sol-gel method, respectively. The solvothermal method produces the SnO_2-C core-shell structure, and

the sol-gel method yields the C-SnO_2 core-shell structure. Other SnO_2-C composites include SnO_2-C hollow spheres[165] and C-coated SnO_2 nanoparticles.[166] The C-coated SnO_2 nanoparticles deliver a discharge capacity of ~500 mAh/g over 20 cycles. Other than SnO_2-C composites, SnO-CNT composites have attracted some research interest and can be obtained via the sol-gel method.[167] The well-dispersed SnO can hinder or reduce the formation of SEI, which reduces the large capacity loss of pristine CNTs in the first cycle.

Nanostructured Transition Metal Oxide-Carbon Composites

A variety of transition metal oxides can also form composites with carbonaceous materials. Here, carbon is mainly used to improve the electric contact of the electrodes, in addition to acting as a buffering matrix for dispersing host materials. TiO_2 provides facile diffusion paths for Li ions,[168] but its electric conductivity is relatively low ($\sim 10^{-12}$ S/cm),[169] which leads to poor cycling stability.[170] A possible method to solve this problem is to combine TiO_2 with carbonaceous materials. The TiO_2-carbon anodes demonstrate enhanced kinetics of lithiation/delithiation processes and increased diffusion coefficient of Li ions.[169] In the structure of TiO_2-C core-shell composites synthesized by L. J. Fu et al., the carbon shells enwrap the TiO_2 cores and hinder the agglomeration of nanoparticles.[170]

Apart from TiO_2, NiO has a theoretical capacity of 718 mAh/g; however, NiO suffers from aggregation, pulverization, and poor conductivity.[171] Tu's group synthesized NiO-C composites by carbonizing the net-structured[171] and spherical[172] NiO under hydrothermal condition. Carbon filled in the porous NiO stabilizes the structure and improves the electrical conductivity of NiO matrix. Figure 11.9 shows cycling performances of the net-structured NiO and NiO-C nanocomposite electrodes at a rate of $0.1C$. The composite electrodes retain a capacity of 429 mAh/g compared to that of 178 mAh/g for the NiO electrode over 40 cycles. Similar to NiO, CoO has a theoretical capacity of 715 mAh/g and the theoretical capacity of Co_3O_4 is 1100 mAh/g.[122,173] Nanostructured cobalt oxides containing CoO and Co_3O_4 can form composites with mesoporous carbon spheres.[174] The porous carbon provides good electric conductivity and buffer space, in addition to hindering the aggregation of the nanoparticles. Such an electrode delivers a capacity of 550 mAh/g after 30 cycles.

Other Nanostructured Composites

Nanosized SnSb anodes also show high Li-ion intercalation capacities.[175,176] However, the nanoparticles with diameters less than 100 nm easily aggregate together, losing their advantage as nanomaterials and showing gradually decreased capacities due to the drastic volume change.[177,178] Xuejie Huang's group has dispersed

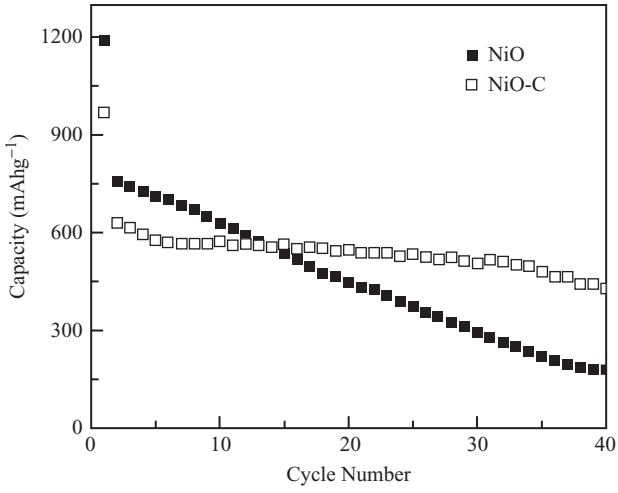


FIGURE 11.9 Capacities of NiO and NiO-C electrodes as a function of cycle number, cycled between 0.02 and 3.0 V at a rate of 0.1*C*.[172]

SnSb nanoparticles on the rigid carbonaceous spherical material such as *mesophase carbon microbeads* (MCMBs) and *hard carbon spherules* (HCSs) to separate these nanoparticles.[179,180,93] The SnSb content should not exceed 30 wt% in the SnSb-MCMB composite; otherwise, severe aggregation will appear again. The SnSb-HCS electrode shows a high coulombic efficiency (82%) in the first cycle, which is ascribed to less surface area being exposed to the electrolyte and thus less formation of the SEI film. The SnSb-HCS electrode shows a capacity of 460 mAh/g over 35 cycles at a current density of 0.2 mA/cm^2.

In addition to carbonaceous material, materials that are electrochemically inert to Li can also serve as a ductile host matrix for Si.[181,182] Nanocrystalline Ni-Si alloy has been reported to form an active/inactive composite, in which Si acts as the active center and Ni functions as the buffering matrix.[181] Such an anode shows a discharge capacity of 1180 mAh/g in the first cycle and retains 800 mAh/g after 25 cycles. Ni dispersed in Co_3O_4 can improve the initial coulombic efficiency. High-energy mechanical milling has been used to synthesize Ni-Co_3O_4 composite.[183] The initial coulombic efficiency is enhanced from 69% for bare Co_3O_4 to 79%, which is ascribed to the optimum contact area of Co_3O_4 and Ni. Sn-coated Cu nanopillars are another composite composed of the active component (Sn) and inactive component (Cu) and can be fabricated by a simple electroplating method.[184] This brushlike structure with large surface area can effectively alleviate the effect of volume change and improve the power rate performance.

11.4 Conclusions

This review clearly reveals the significant influence of materials structure on device performance for energy storage and conversion. The development of high-performance Li-ion batteries can benefit from the distinct properties of nanomaterials, such as high surface areas, short diffusion paths, considerable active sites, and moderate volume change during charge/discharge cycles. However, some challenging issues need to be addressed first. For instance, the huge surface area and low-dimension structure may cause the solubility of cathode materials in the electrolyte; the increased chemical activity of nanomaterials may render cathode materials more sensitive and fragile to impurities and contaminants. To solve these problems, a variety of nanosized thin coatings can be deposited onto nanostructured cathodes with conformal coverage. In contrast to the solubility problem of nanostructured cathode materials, the main challenges faced by anode materials include poor conductivity, low initial coulombic efficiency, and drastic volume variation during electrochemical cycling. The issue of poor conductivity of anode materials can be solved by growing nanostructured anode materials on metallic current collector substrates or by dispersing them in a conductive medium. The effect of drastic volume change during cycling can be reduced by using nanostructured anodes; this effect can be further alleviated by employing nanocomposite materials as anodes.

Nanotechnology has an increasing impact on the world energy balance, on both the supply and demand sides. To realize wide industrialization of nanomaterials for energy applications, further effort is required to achieve controlled and large-scale synthesis of nanostructures and to understand mechanisms of lithium storage in nanomaterials and kinetic transport on the interface between electrode and electrolyte. The effects of nanostructures in battery performance are not only simple consequences of a reduction in size. Interfacial properties are subtle and critical, considering space-charge effects at the interface between nanosized electrode materials and charge transport between electrode and electrolyte. This challenges researchers worldwide to carry out systematic experimental studies and to develop predictive theoretical tools for better fundamental understanding of relationships between nanostructures and electrochemical characteristics of electrode materials.

Acknowledgments

C. C. and D. S. G. would like to acknowledge the LSU Graduate School Enhancement Award and the LSU Graduate School Supplementary Award, respectively.

References

1. W. van Schalkwijk and B. Scrosati, editors, Advances in Li-ion Batteries, Springer, 2002.
2. J. M. Tarascon and M. Armand, "Issues and challenges facing rechargeable lithium batteries," *Nature*, vol. 414, pp. 359-367, 2001.
3. M. S. Whittingham, "Lithium batteries and cathode materials," *Chemical Reviews*, vol. 104(10), pp. 4271-4302, 2004.
4. M. S. Whittingham, Y. Song, S. Lutta, P. Y. Zavalij, and N. A. Chernova, "Some Transition Metal (oxy)phosphates and Vanadium Oxides for Lithium Batteries," *Journal of Materials Chemistry*, vol. 15, pp. 3362-3379, 2005.
5. J. N. Reimers and J. R. Dahn, "Electrochemical and *in situ* x-ray diffraction studies of lithium intercalation in Li_xCoO_2," *Journal of the Electrochemical Society*, vol. 139, pp. 2091-2097, 1992.
6. P. N. Kumta, D. Gallet, A. Waghray, G. E. Blomgren, and M. P. Setter, "Synthesis of $LiCoO_2$ powders for lithium-ion batteries from precursors derived by rotary evaporation," *Journal of Power Sources*, vol. 72, pp. 91-98, 1998.
7. T. Ohzuku and A. Ueda, "Why transition metal (di) oxides are the most attractive materials for batteries," *Solid State Ionics*, vol. 69, pp. 201-211, 1994.
8. T. Ohzuku, A. Ueda, and N. Nagayama, "Electrochemistry and structural chemistry of lithium nickel oxide ($LiNiO_2$)(Rhivin.3m) for 4 volt secondary lithium cells," *Journal of the Electrochemical Society*, vol. 140(7), pp. 1862-1870, 1993.
9. J. R. Dahn, U. von Sacken, and C. A. Michal, "Structure and Electrochemistry of $Li_{1\pm y}NiO_2$ and a new Li_2NiO_2 Phase with the $Ni(OH)_2$ structure," *Solid State Ionics*, vol. 44, pp. 87-97, 1990.
10. A. Rougier, P. Gravereau, and C. Delmas, "Optimization of the composition of the $Li_1-zNi_1+zO_2$ electrode materials: structural, magnetic, and electrochemical studies," *Journal of the Electrochemical Society*, vol. 143, pp. 1168-1175, 1996.
11. L. Abello, E. Husson, Y. R. Repelin, and G. Lucazeau, "Vibrational spectra and valence force field of crystalline V_2O_5," *Spectrochimica Acta*, vol. 39A, pp. 641, 1983.
12. J. B. Goodenough and K. Mizuchima, "Electrochemical cell with new fast ion conductors," US Patent 4,302,518, 1981.
13. J. Molenda, A. Stoklosa, and T. Bak, "Modifications in the electronic structure of cobalt bronze Li_xCoO_2 and the resulting electrochemical properties," *Solid State Ionics*, vol. 36, pp. 53-58, 1989.
14. C. J. Curtis, J. Wang, and D. L. Schulz, "Preparation and characterization of $LiMn_2O_4$ spinel nanoparticles as cathode materials in secondary Li batteries," *Journal of the Electrochemical Society*, vol. 151(4), pp. A590-A598, 2004.
15. J. F. Whitacre, W. C. West, E. Brandon, and B. V. Ratnakumar, "Crystallographically oriented thin-film nanocrystalline cathode layers prepared without exceeding 300°C," *Journal of the Electrochemical Society*, vol. 148(10), pp. A1078-A1084, 2001.
16. M. Kunduraci and G. G. Amatucci, "Synthesis and characterization of nanostructured 4.7 V $Li_xMn_{1.5}Ni_{0.5}O_4$ spinels for high-power lithium-ion batteries," *Journal of the Electrochemical Society*, vol. 153(7), pp. A1345-A1352, 2006.
17. J. C. Arrebola, A. Caballero, M. Cruz, L. Hernán, J. Morales, and E. R. Castellón, "Crystallinity control of a nanostructured $LiNi_{0.5}Mn_{1.5}O_4$ spinel via polymer-assisted synthesis: a method for improving its rate capability and performance in 5 V lithium batteries," *Advanced Functional Materials*, vol. 16(14), pp. 1904-1912, 2006.
18. D. W. Murphy, P. A. Christian, F. J. DiSalvo, and J. V. Waszczak, "Lithium incorporation by vanadium pentoxide," *Inorganic Chemistry*, vol. 18, pp. 2800-2803, 1979.

19. L. Abello, E. Husson, Y. R. Repelin, and G. Lucazeau, "Vibrational spectra and valence force field of crystalline V_2O_5," *Spectrochimica Acta*, vol. 39A, pp. 641-651, 1983.
20. M. S. Whittingham, "The role of ternary phases in cathode reactions," *Journal of the Electrochemical Society*, vol. 123, pp. 315-320, 1976.
21. K. West, B. Zachau-Christiansen, M. J. L. Ostergard, and T. Jacobsen, "Vanadium-oxides as electrode materials for rechargeable lithium cells," *Journal of Power Sources* , vol. 20(1-2), pp. 165-172, 1987.
22. K. West, B. Zachau-Christiansen, T. Jacobsen, and S. Skaarup, "Vanadium oxide xerogels as electrodes for lithium batteries," *Electrochimica Acta*, vol. 38, pp. 1215-1220, 1993.
23. K. Salloux, F. Chaput, H. P. Wong, B. Dunn, and M. W. Breiter, "Lithium intercalation in vanadium pentoxide aerogels," *Journal of the Electrochemical Society*, vol. 142(10), pp. L191-L192, 1995.
24. R. Nesper, M. E. Spahr, M. Niederberger, and P. Bitterli, "Nanotubes, Verwendung solcher Nanotubes sowie Verfahren zu deren Herstellung," International Patent Application PCT/CH97/00470, 1997.
25. K. S. Pillai, F. Krumeich, H. J. Muhr, M. Niederberger, and R. Nesper, "The first oxide nanotubes with alternating inter-layer distances," *Solid State Ionics*, vol. 141, pp. 185-190, 2001.
26. C. J. Patrissi and C. R. Martin, "Sol-gel-based template synthesis and Li-insertion rate performance of nanostructured vanadium pentoxide," *Journal of the Electrochemical Society*, vol. 146(9), pp. 3176-3180, 1999.
27. N. Li, C. J. Patrissi, and C. R. Martin, "Rate capabilities of nanostructured $LiMn_2O_4$ electrodes in aqueous electrolyte," *Journal of the Electrochemical Society*, vol. 147, p. 2044, 2000
28. K. Takahashi, S. J. Limmer, Y. Wang, and G. Z. Cao, "Synthesis and electrochemical properties of single-crystal V_2O_5 nanorod arrays by template-based electrodeposition," *Journal of Physical Chemistry B*, vol. 108(28), pp. 9795-9800, 2004.
29. K.Takahashi, S. J. Limmer, Y. Wang, and G. Z. Cao, "Growth and electrochemical properties of single-crystalline V_2O_5 nanorod arrays," *Journal of Applied Physics*, vol. 44, pp. 662-668, 2005.
30. K. Takahashi, Y. Wang, and G. Z. Cao, "Growth and electrochromic properties of single-crystal V_2O_5 nanorod arrays," *Applied Physics Letters*, vol. 86(5), pp. 053102, 2005.
31. Y. Wang, K. Takahashi, H. Shang, and G. Z. Cao, "Synthesis and electrochemical properties of vanadium pentoxide nanotube arrays," *Journal of Physical Chemistry B*, vol. 109(8), pp. 3085-3088, 2005
32. K. Takahashi, Y. Wang, and G. Z. Cao, "Ni-$V_2O_5{\cdot}nH_2O$ core-shell nanocable arrays for enhanced electrochemical intercalation," *Journal of Physical Chemistry B*, vol. 109, pp. 48-51, 2005.
33. K. Lee, Y. Wang, and G. Z. Cao, "Dependence of electrochemical properties of vanadium oxide films on their nano- and microstructures," *Journal of Physical Chemistry B*, vol. 109, pp. 16700-16704, 2005.
34. H. Yan, S. Sokolov, J. C. Lytle, A. Stein, F. Zhang, and W. H. Smyrl, "Colloidal-crystal-templated synthesis of ordered macroporous electrode materials for lithium secondary batteries," *Journal of the Electrochemical Society*, vol. 150(8), pp. A1102-A1107, 2003.
35. N. S. Ergang, J. C. Lytle, K. T. Lee, S. M. Oh, and W. H. Smyrl, A. Stein, "Photonic crystal structures as a basis for an interpenetrating electrochemical cell system," *Advanced Materials*, vol. 18, pp. 1750-1753, 2006.
36. P. Liu, S. H. Lee, E. Tracy, Y. Yan, and Turner, "Preparation and lithium insertion properties of mesoporous vanadium oxide," *Advanced Materials*, vol. 14(1), pp. 27-30, 2002.
37. G. Li, S. Pang, L. Jiang, Z. Guo, and Z. Zhang, "Environmentally friendly chemical route to vanadium oxide single-crystalline nanobelts as a cathode

material for lithium-ion batteries," *Journal of Physical Chemistry B*, vol. 110(19), pp. 9383-9386, 2006.
38. B. Li, Y. Xu, G. Rong, M. Jing, and Y. Xie, "Vanadium pentoxide nanobelts and nanorolls: from controllable synthesis to investigation of their electrochemical properties and photocatalytic activities," *Nanotechnology*, vol. 17, pp. 2560-2566, 2006.
39. X. Li, W. Li, H. Ma, and J. J. Chen, "Electrochemical lithium intercalation/deintercalation of single-crystalline V_2O_5 nanowire," *Electrochemical Society*, vol. 154(1), pp. A39-A42, 2007.
40. S. T. Lutta, H. Dong, P. Y. Zavalij, and M. S. Whittingham, "Synthesis of vanadium oxide nanofibers and tubes using polylactide fibers as template," *Materials Research Bulletin*, vol. 40(2), pp. 383-393, 2005.
41. C. K. Chan, H. Peng, R. D. Tweten, K. Jarausch, X. F. Zhang, and Y. Cui, "Fast, completely reversible Li insertion in vanadium pentoxide nanoribbons," *Nano Letters*, vol. 7(2), pp. 490-495, 2007.
42. W. C. West, N. V. Myung, J. F. Whitacre, B. V. Ratnakumar, "Electrodeposited amorphous manganese oxide nanowire arrays for high energy and power density electrodes," *Journal of Power Sources*, vol. 126(1-2), pp. 203-206, 2004.
43. M. S. Wu, P. C. J. Chiang, J. T. Lee, and J. C. Lin, "Synthesis of manganese oxide electrodes with interconnected nanowire structure as an anode material for rechargeable lithium ion batteries," *Journal of Physical Chemistry B*, vol. 109(49), pp. 23279-23284, 2005.
44. F. Y. Cheng, J. Z. Zhao, W. E. Song, C. S. Li, H. Ma, J. Chen, et al., "Facile controlled synthesis of MnO_2 nanostructures of novel shapes and their application in batteries," *Inorganic Chemistry* , vol. 45(5), pp. 2038-2044, 2006.
45. W. H. Ho and S. K. Yen, "Characterization of electrolytic manganese oxide coating on Pt for lithium battery applications," *Journal of the Electrochemical Society* vol. 152(3), pp. A506-A510, 2005.
46. F. Jiao and P. T. Bruce, "Mesoporous crystalline -MnO_2—a reversible positive electrode for rechargeable lithium batteries," *Advanced Materials*, vol. 19(5), pp. 657-660, 2007.
47. R. Ma, Y. Bando, L. Zhang, and T. Sasaki, "Layered MnO_2 nanobelts: hydrothermal synthesis and electrochemical measurements," *Advanced Materials*, vol. 16(11), pp. 918-922, 2004.
48. J. Kim, M. Noh, J. Cho, H. Kim, and K. Kim, "Controlled nanoparticle metal phosphates (metal = Al, Fe, Ce, and Sr) coatings on $LiCoO_2$ cathode materials," *Journal of the Electrochemical Society*, vol. 152(6), pp. A1142-A1148, 2005.
49. Y. J. Kim, J. Cho, T. J. Kim, and B. Park, "Suppression of cobalt dissolution from the LiCoO cathodes with various metal-oxide coatings," *Journal of the Electrochemical Society*, vol. 150, pp. A1723-A1725, 2003.
50. L. Lui, Z. Wang, H. Li, L. Chen, and X. Huang, "Al_2O_3–coated $LiCoO_2$ as cathode material for lithium ion batteries," *Solid State Ionics*, vol. 152-153, pp. 341-346, 2002.
51. J. Cho, C. S. Kim, and S. I. Yoo, "Improvement of structural stability of $LiCoO_2$ cathode during electrochemical cycling by sol-gel coating of SnO_2," *Electrochemical and Solid-State Letters*, vol. 3, pp. 362-365, 2000.
52. Z. X. Wang, X. J. Huang, and L. Q. Chen, "Performance improvement of surface-modified $LiCoO_2$ cathode materials—an infrared absorption and x-ray photoelectron spectroscopic investigation," *Journal of the Electrochemical Society*, vol. 150(2), pp. A199-A208, 2003.
53. T. Fang, J. G. Duh, and S. R. Sheen, "Improving the electrochemical performance of $LiCoO_2$ cathode by nanocrystalline ZnO coating," *Journal of the Electrochemical Society*, vol. 152(9), pp. A1701-A1706, 2005.
54. N. Ohta, K. Takada, L. Zhang, R. Ma, M. Osada, and T. Sasaki, "Enhancement of the high-rate capability of solid-state lithium batteries by nanoscale interfacial modification," *Advanced Materials*, vol. 18, pp. 2226-2229, 2006.

55. Y. Sun, K. Hong, and J. Prakash, "The effect of ZnO coating on electrochemical cycling behavior of spinel $LiMn_2O_4$ cathode materials at elevated temperature," *Journal of the Electrochemical Society*, vol. 150, pp. A970-A972, 2003.
56. M. M. Thackeray, C. S. Johnson, J. S. Kim, K. C. Lauzze, J. T. Vaughey, N. Dietz, et al., "ZrO_{2-} and Li_2ZrO_{3-}stabilized spinel and layered electrodes for lithium batteries," *Electrochemistry Communications*, vol. 5, p. 752, 2003.
57. S. Y. Chung, J. T. Bloking, and Y. M. Chiang, "Electronically conductive phospho-olivines as lithium storage electrodes," *Nature* Materials, vol. 1, pp. 123-128, 2002.
58. S. Yang, Y. Song, K. Ngala, P. Y. Zavalij, and M. S. Whittingham, "Performance of $LiFePO_4$ as lithium battery cathode and comparison with manganese and vanadium oxides," *Journal of Power Sources*, vol. 119, pp. 239-246, 2003.
59. N. Ravet, J. B. Goodenough, S. Besner, M. Simoneau, P. Hovington, and M. Armand, "Additives improving phospho-olivines conductivity," *Electrochemical Society Abstracts*, vol. 99–2, p. 127, 1999.
60. N. Ravet, S. Besner, M. Simoneau, A. Vallée, M. Armand, and J. F. Magnan, "Materiaux d'électrode présentant une conductivite de surface élevée," Hydro-Quebec: European Patent 1049182A2, 2000.
61. S. Yang, P. Y. Zavalij, and M. S. Whittingham, "Hydrothermal synthesis of lithium iron phosphate cathodes," *Electrochemistry Communications*, vol. 3, pp. 505-508, 2001.
62. A. D. Spong, G. Vitins, and J. R. Owen, "Solution-precursor synthesis of carbon-coated $LiFePO_4$ for Li-ion cells," *Journal of the Electrochemical Society*, vol. 152, pp. A2376-A2382, 2005.
63. T. Nakamura, Y. Miwa, M. Tabuchi, and Y. Yamada, "Structural and surface modifications of $LiFePO_4$ olivine particles and their electrochemical properties," *Journal of the Electrochemical Society*, vol. 153, pp. A1108-A1114, 2006.
64. M. Gaberscek, R. Dominko, M. Bele, M. Remskar, D. Hanzel, and J. Jamnik, "Porous carbon-decorated $LiFePO_4$ prepared by sol-gel method based on citric acid," *Solid State Ionics*, vol. 176, pp. 1801-1805, 2005.
65. J. D. Wilcox, M. M. Doeff, M. Marcinek, and R. Kostecki, "Factors influencing the quality of carbon coatings on $LiFePO_4$," *Journal of the Electrochemical Society*, vol. 154, pp. A389-A395, 2007.
66. R. Dominko, J. M. Goupil, M. Bele, M. Gaberscek, M. Remskar, D. Hanzel, et al., "Impact of $LiFePO_4$/C composites porosity on their electrochemical performance," *Journal of the Electrochemical Society*, vol. 152, pp. A858-A863, 2005.
67. F. Croce, A. D. Epifanio, J. Hassoun, A. Deptula, T. Olczac, and B. Scrosati, "A novel concept for the synthesis of an improved $LiFePO_4$ lithium battery cathode," *Electrochemical and Solid-State Letters*, vol. 5, pp. A47-A50, 2002.
68. Y. H. Rho, L. F. Nazar, L. Perry, and D. Ryan, "Surface chemistry of $LiFePO_4$ studied by Mössbauer and x-ray photoelectron spectroscopy and its effect on electrochemical properties," *Journal of the Electrochemical Society*, vol. 154, pp. A283-A289, 2007.
69. H. M. Xie, R. S. Wang, J. R. Ying, L. Y. Zhang, A. F. Jalbout, H. Y. Yu, et al., "Optimized $LiFePO_{4-}$polyacene cathode material for lithium-ion batteries," *Advanced Materials*, vol. 18, pp. 2609-2613, 2006.
70. Y. S. Hu, Y. G. Guo, R. Dominko, M. Gaberscek, and J. Jamnik, "Improved electrode performance of porous $LiFePO_4$ using RuO_2 as an oxidic nanoscale interconnect," *Advanced Materials*, vol. 19, pp. 1963-1966, 2007.
71. H. Huang, S. C. Yin, and L. F. Nazar, "Approaching theoretical capacity of $LiFePO_4$ at room temperature at high rates," *Electrochemical and Solid-State Letters*, vol. 4, pp. A170-A172, 2001.
72. J. M. Tarascon, C. Delacourt, A. S Prakash, M. Morcrette, M. S. Hegde, C. Wurm, et al., "Various strategies to tune the ionic/electronic properties of electrode materials," *Dalton Transactions*, vol. 19, pp. 2988-2994, 2004.

73. M. Koltypin, V. Pol, A. Gedanken, and D. Aurbach, "The study of carbon-coated V_2O_5 nanoparticles as a potential cathodic material for Li rechargeable batteries," *Journal of the Electrochemical Society*, vol. 154, pp. A605-A613, 2007.
74. J. S. Sakamoto and B. Dunn, "Vanadium oxide-carbon nanotube composite electrodes for use in secondary lithium batteries," *Journal of the Electrochemical Society*, vol. 149, pp. A26-A30, 2002.
75. D. Dubarry, J. Gaubicher, P. Moreau, and D. Guyomard, "Formation of $Li_{1+n}V_3O_8/\beta$-$Li_{1/3}V_2O_5$/C nanocomposites by carboreduction and the resulting improvement in Li capacity retention," *Journal of the Electrochemical Society*, vol. 153, pp. A295-A300, 2006.
76. X Huang, H. Yue, A. Attia, and Y. Yang, "Preparation and properties of manganese oxide/carbon composites by reduction of potassium permanganate with acetylene black," *Journal of the Electrochemical Society*, vol. 154, pp. A26-A33, 2007.
77. J. Yang and J. J. Xu, "synthesis and characterization of carbon-coated lithium transition metal phosphates $LiMPO_4$ (M = Fe, Mn, Co, Ni) prepared via a nonaqueous sol-gel route," *Journal of the Electrochemical Society*, vol. 153, pp. A716-A723, 2006.
78. H. Huang, S. C. Yin, T. Kerr, N. Taylor, and L. F. Nazar, "Nanostructured composites: a high capacity, fast rate $Li_3V_2(PO_4)_3$/carbon cathode for rechargeable lithium batteries," *Advanced Materials*, vol. 14, pp. 1525-1528, 2002.
79. M. Ferreira, V. Zucolotto, F. Huguenin, R. M. Torresi, and O. N. Oliveira, "Layer-by-layer nanostructured hybrid films of polyaniline and vanadium oxide," *Journal of Nanoscience and Nanotechnology*, vol. 2, pp. 29-32, 2002.
80. F. Huguenin, D. S. dos Santos, A. Bassi, F. C. Nart, and O. N. Oliveira, "Charge storage capability in nanoarchitectures of V_2O_5/chitosan/poly(ethylene oxide) produced using the layer-by-layer technique," *Advanced Functional Materials*, vol. 14, pp. 985-991, 2004.
81. E. A. Ponzio, T. M. Benedetti, and R. M. Torresi, "Electrochemical and morphological stabilization of V_2O_5 nanofibers by the addition of polyaniline," *Electrochimica Acta*, vol. 52, pp. 4419-4427, 2007.
82. C. V. S. Reddy, W. Jin, Q. Y. Zhu, W. Chen, and R. R. Kalluru, "Polymer intercalated V_2O_5 nanostructured cathodes for secondary batteries," *European Physical Journal Applied Physics*, vol. 38, pp. 31-35, 2007.
83. 84. E. A. Olivetti, J. H. Kim, D. R. Sadoway, A. Asatekin, and A. M. Mayes, "Sol-gelsynthesis of vanadium oxide within a block copolymer matrix," *Chemistry of Materials*, vol. 18, pp. 2828-2833, 2006.
84. D. Guy, B. Lestriez and D. Guyomard, "New composite electrode architecture and improved battery performance from the smart use of polymers and their properties," *Advanced Materials*, vol. 16, pp. 553-557, 2004.
85. N. Peter, M. Klaus, K. S. V. Santhannam, and H. Otto, "Electrochemically active polymers for rechargeable batteries," *Chemical Reviews*, vol. 97, pp. 207-282, 1997.
86. J. Wang, J. Yang, J. Xie, and N. Xu, "A novel conductive polymer-sulfur composite cathode material for rechargeable lithium batteries," *Advanced Materials*, vol. 14, pp. 963-965, 2002.
87. J. Wang, J. Yang, C. Wan, K. De, J. Xie, and N. Xu, "Sulfur composite cathode materials for rechargeable lithium batteries," *Advanced Functional Materials*, vol. 13, pp. 487-492, 2003.
88. Y. Wang, K. Lee, H. Shang, B. Wiley, Y. Xia, and G. Cao, "Ag-$Ag_{0.08}V_2O_5 \cdot nH_2O$ composite films as host materials for Li^+ intercalation," *Physica Status Solidi (a)*, vol. 202, R79-R81, 2005.
89. J. S. Wook and S. M. Lee, "$LiCoO_2$/Ag multilayer film cathodes for thin-film rechargeable lithium batteries," *Journal of the Electrochemical Society*, vol. 154, pp. A22-A25, 2007.
90. Y. Li, T. Kunitake, and Y. Aoki, "Synthesis and Li^+ intercalation/extraction in ultrathin V_2O_5 layer and freestanding V_2O_5/Pt/PVA multilayer films," *Chemistry of Materials*, vol. 19, pp. 575-580, 2007.

91. N. Imachi, Y. Takano, H. Fujimoto, Y. Kida, and S. Fujitani, "Layered cathode for improving safety of Li-ion batteries," *Journal of the Electrochemical Society*, vol. 154, pp. A412-A416, 2007.
92. S. R Sivakkumar, D. R. MacFarlane, M. Forsyth, and D. W. Kim, "ionic liquid-based rechargeable lithium metal-polymer cells assembled with polyaniline/carbon nanotube composite cathode," *Journal of the Electrochemical Society*, vol. 154, pp. A834-A838, 2007.
93. Q. Wang, H. Li, L. Chen, and X. Huang, "Novel spherical microporous carbon as anode material for Li-ion batteries," *Solid State Ionics*, vol. 152–153, pp. 43-50, 2002.
94. R. A. Huggins, "Lithium alloy negative electrodes formed from convertible oxides," *Solid State Ionics*, vol. 113–115, pp. 57-67, 1998.
95. L. F. Cui, R. Ruffo, C. K. Chan, H. Peng, and Y. Cui, "crystalline-amorphous core–shell silicon nanowires for high capacity and high current battery electrodes," *Nano Letters*, vol. 9(1), pp. 491-495, 2009.
96. R. A. Sharma and R. N. Seefurth, "Thermodynamic properties of the lithium-silicon system," *Journal of the Electrochemical Society*, vol. 123, pp. 1763-1768, 1976.
97. B. A. Boukamp, G. C. Lesh, and R. A. Huggins, "All-solid lithium electrodes with mixed-conductor matrix," *Journal of the Electrochemical Society*, vol. 128, pp. 725-729, 1981.
98. M. Winter, J. O. Besenhard, M. E. Spahr, and P. Novak, "Insertion electrode materials for rechargeable lithium batteries," *Advanced Materials*, vol. 10, pp. 725-763, 1998.
99. U. Kasavajjula, C. Wang, and A. J. Appleby, "Nano- and bulk-silicon-based insertion anodes for lithium-ion secondary cells," *Journal of Power Sources*, vol. 163, pp. 1003-1039, 2007.
100. K. Candace, P. H. Chan, G. Liu, K. McIlwrath, X. F. Zhan, R. A. Huggins, et al., "High-performance lithium battery anodes using silicon nanowires," *Nature Nanotechnology*, vol. 3, pp. 31-35, 2008.
101. J. T. Yin, M. Wada, K. Yamamoto, Y. Kitano, S. Tanase, and T. Sakai, "Micrometer-scale amorphous Si thin-film electrodes fabricated by electron-beam deposition for Li-ion batteries," *Journal of the Electrochemical Society*, vol. 153(3), pp. A472-A477, 2006.
102. J. P. Maranchi, A. F. Hepp, and P. N. Kumta, "High capacity, reversible silicon thin-film anodes for lithium-ion batteries," *Electrochemical and Solid-State Letters*, vol. 6(9), pp. A198-A201, 2003.
103. S. Ohara, J. J. Suzuki, K. Sekine, and T. Takamura, "Attainment of high rate capability of Si Film as the anode of Li-ion batteries," *Electrochemistry*, vol. 71(12), pp. 1126-1128, 2003.
104. L. Y. Beaulieu, K. W. Eberman, R. L. Turner, L. J. Krause, and J. R. Dahn, "Colossal Reversible Volume Changes in Lithium Alloys," *Electrochemical and Solid-State Letters*, vol. 4 (9), pp. A137-A140, 2001.
105. Y. C. Chen, J. M. Chen, Y. H. Huang, Y. R. Lee, and H. C. Shih, "Size effect of tin oxide nanoparticles on high capacity lithium battery anode materials," *Surface & Coatings Technology*, vol. 202, pp. 1313-1318, 2007.
106. I. Rom, M. Wachtler, I. Papst, M. Schmied, J. O. Besenhard, F. Hofer, et al., "Electron microscopical characterization of Sn/Snsb composite electrodes for lithium-ion batteries," *Solid State Ionics*, vol. 143(3–4), pp. 329-336, 1999.
107. G. X. Wang, J. H. Ahn, J. Yao, S. Bewlay, and H. K. Liu, "Nanostructured Si-C composite anodes for lithium-ion batteries", *Electrochemistry Communications*, vol. 6, pp. 689-692, 2004.
108. T. Zhang, L. J. Fu, J. Gao, Y. P. Wua, R. Holze, and H. Q. Wu, "Nanosized tin anode prepared by laser-induced vapor deposition for lithium ion battery," *Journal of Power Sources*, vol. 174, pp. 770-773, 2007.
109. J. Graetz, C. C. Ahn, R. Yazami, and B. Fultz, "Nanocrystalline and thin film germanium electrodes with high lithium capacity and high rate capabilities," *Journal of the Electrochemical Society*, vol. 151(5), pp. A698-A702, 2004.

110. C. K. Chan, X. F. Zhang, and Y. Cui, "High capacity Li ion battery anodes using Ge nanowires," *Nano Letters*, vol. 8(1), pp. 307-309, 2008
111. Y. Idota, M. Mishima, M. Miyaki, T. Kubota, and T. Miyasaka, "Nonaqueous secondary battery," European Patent Application 65140 A1 94116643.1, 1994.
112. K. Tahara, H. Ishikawa, F. Iwasaki, S. Yahagi, A. Sakkata, and T. Sakai, "Nonaqueous electrolyte secondary battery and its production method," European Patent Application 93111938.2, 1993.
113. I. A. Courtney and J. R. Dahn, "Electrochemical and in situ x-ray diffraction studies of the reaction of lithium with tin oxide composites," *Journal of the Electrochemical Society*, vol. 144(6), 2045-2052, 1997.
114. J. O. Besenhard, J. Yang, and M. Winter, "Will advanced lithium-alloy anodes have a chance in lithium-ion batteries," *Journal of Power Sources*, vol. 68, pp. 87-90, 1997.
115. Z. Ying, Q. Wan, H. Cao, Z. T. Song, and S. L. Feng, "Characterization of SnO_2 nanowires as an anode material for Li-Ion batteries," *Applied Physics Letters*, vol. 87, 113108, 2005.
116. S. H. Ng, D. I. dos Santos, S. Y. Chew, D. Wexler, J. Wang, S. X. Dou, et al., "Polyol-mediated synthesis of ultrafine tin oxide nanoparticles for reversible Li-ion storage," *Electrochemistry Communications*, vol. 9(5), pp. 915-919, 2007.
117. V. Subramanian, B. W. William, H. W. Zhu, and B. Q. Wei, "Novel microwave synthesis of nanocrystalline SnO_2 and its electrochemical properties," *Journal of Physical Chemistry C*, vol. 112(12), pp. 4550-4556, 2008.
118. W. L. Xiong, Y. Wang, C. Yuan Lee, Y. Jim, and L. A. Archer, "Template-free synthesis of SnO_2 hollow nanostructures with high lithium storage capacity," *Advanced Materials*, vol. 18(17), pp. 2325-2329, 2006.
119. L Yuan, Z. P. Guo, K. Konstantinov, J. Z. Wang, and H. K. Liu, "In situ fabrication of spherical porous tin oxide via a spray pyrolysis technique," *Electrochimica Acta*, vol. 51, pp. 3680-3684, 2006.
120. H. K. Seong, M. H. Kim, H. J. Choi, Y. J. Choi, and J. G. Park, "Electrochemical characteristics of single crystalline nanowires and their driven mechanism," *Metals and Materials International*, vol. 14(4), pp. 477-480, 2008.
121. Naichao Li and Charles R. Martin, "A high-rate, high-capacity, nanostructured sn-based anode prepared using sol-gel template synthesis," *Journal of The Electrochemical Society*, vol. 148(2), pp. A164-A170, 2001.
122. P. Poizot, S. Larulle, S. Grugeon, L. Dupont, and J. M. Tarascon, "Nano-sized transition-metal oxides as negative-electrode materials for lithium-ion batteries," *Nature*, vol. 407, pp. 496-498, 2000.
123. C. Natarajan, K. Setoguchi, and G. Nogami, "Preparation of a nanocrystalline titanium dioxide negative electrode for the rechargeable lithium ion battery," *Electrochimica Acta*, vol. 43(21–22), pp. 3371-3374, 1998.
124. G. F. Ortiz, H. Ilie, D. Thierry, L. Pedro, J. L. Tirado, and P. Knauth, "Alternative Li-ion battery electrode based on self-organized titania nanotubes," *Chemistry of Materials*, vol. 21, pp. 63-67, 2009.
125. V. Subramanian, A. Karki, K. I. Gnanasekar, F. P. Eddy, and B. Rambabu, "Nanocrystalline TiO_2 (anatase) for Li-ion batteries," *Journal of Power Sources*, vol. 159(1), pp. 186-192, 2006.
126. J. Kim and J. Cho, "Rate characteristics of anatase TiO_2 nanotubes and nanorods for lithium battery anode materials at room temperature," *Journal of the Electrochemical Society*, vol. 154(6), pp. A542-A546, 2007.
127. H. Qiao, Y. Wang, L. Xiao, and L. Zhang, "High lithium electroactivity of hierarchical porous rutile TiO_2 nanorod microspheres," *Electrochemistry Communications*, vol. 10, pp. 1280-1283, 2008.
128. J. C. Park, J. Kim, H. Kwon, and H. Song, "Gram-scale synthesis of Cu_2O nanocubes and subsequent oxidation to CuO hollow nanostructures for lithium-ion battery anode materials," *Advanced Materials* vol. 21(7), pp. 803-807, 2009.

129. X. J. Zhang, D. G. Zhang, X. M. Ni, J. M. Song, and H. G. Zheng, "Synthesis and electrochemical properties of different sizes of the CuO particles," *Journal of Nanoparticle Research*, vol. 10, pp. 839-844, 2008.
130. X. P. Gao, J. L. Bao, G. L. Pan, H. Y. Zhu, P. X. Huang, F. Wu, et al., "Preparation and electrochemical performance of polycrystalline and single crystalline CuO nanorods as anode materials for Li ion battery," *Journal of Physical Chemistry B*, vol. 108(18), pp. 5547-5551, 2004.
131. B. Varghese, M. V. Reddy, Y. W. Zhu, S. L. Chang, T. C. Hoong, G. V. Subba Rao, et al., "Fabrication of NiO nanowall electrodes for high performance lithium ion battery," *Chemistry of Materials*, vol. 20(10), pp. 3360-3367, 2008.
132. X. H. Huang, J. P. Tu, X. H. Xia, X. L. Wang, J. Y. Xiang, L. Zhang, et al., "Morphology effect on the electrochemical performance of NiO films as anodes for lithium ion batteries," *Journal of Power Sources*, vol. 188(2), pp. 588-591, 2009.
133. L. Yuan, Z. P. Guo, K. Konstantinov, P. Munroe, and H. K. Liu, "Spherical clusters of NiO nanoshafts for lithium-ion battery anodes," *Electrochemical and Solid-State Letters*, vol. 9(11), pp. A524-A528, 2006.
134. G. X. Wang, Y. Chen, K. Konstantinov, J. Yao, J. -H. Ahn, H. K. Liu, et al., "Nanosize cobalt oxides as anode materials for lithium-ion batteries," *Journal of Alloys and Compounds*, vol. 340(1–2), pp. L5-L10, 2002.
135. S. -H. Hong, J.-S. Bae, and H. J. Ahn, "Synthesis of nano-sized Co_3O_4 powder by spray conversion method for anode material of lithium battery," *Metals and Materials International*, vol. 14(2), pp. 229-232, 2008.
136. X. W. Lou, D. Deng, J. Y. Lee, J. Feng, and L. A. Archer, "Self-supported formation of needlelike Co_3O_4 nanotubes and their application as lithium-ion battery electrodes," *Advanced Materials*, vol. 20, pp. 258-262, 2008.
137. S. L. Chou, J. Z. Wang, H. K. Liu, and S. X. Dou, "Electrochemical deposition of porous CO_3O_4 nanostructured thin film for lithium-ion battery," *Journal of Power Sources*, vol. 182, pp. 359-364, 2008.
138. N. Du, H. Zhang, B. D. Chen, J. B. Wu, X. Y. Ma, Z. H. Liu, et al., "Porous Co_3O_4 nanotubes derived from $Co_4(CO)_{12}$ clusters on carbon nanotube templates: a highly efficient material for Li-battery applications," *Advanced Materials*, vol. 19(24), pp. 4505-4509, 2007.
139. D. Son, E. Kim, T.-G. Kim, M. G. Kim, J. Cho, and B. Park, "Nanoparticle iron-phosphate anode material for Li-ion battery," *Applied Physics Letters*, vol. 85, pp. 5875-5877, 2004.
140. S. Denis, E. Baudrin, M. Touboul, and J. M. Tarascon, "Synthesis and electrochemical properties of amorphous vanadates of general formula RVO_4 (R = In, Cr, Fe, Al, Y) vs. Li," *Journal of the Electrochemical Society*, vol. 144, pp. 4099-4109, 1997.
141. Y. Wang and G. Z. Cao, "Synthesis and electrochemical properties of $InVO_4$ nanotube arrays," *Journal of Materials Chemistry*, vol. 17, pp. 894-899, 2007.
142. H. Li, X. J. Huang, L. Q. Chen, Z. G. Wu, and Y. Liang, "A high capacity nano-Si composite anode material for lithium rechargeable batteries," *Electrochemical and Solid-State Letters*, vol. 2(11), pp. 547-549, 1999.
143. Y. Zhang, X. G. Zhang, H. L. Zhang, Z. G. Zhao, F. Li, C. Liu, et al., "Composite anode material of silicon/graphite/carbon nanotubes for Li-ion batteries," *Electrochimica Acta*, vol. 51, pp. 4994-5000, 2006.
144. G. X. Wang, J. H. Ahn, J. Yao, S. Bewlay, and H. K. Liu, "Nanostructured Si-C composite anodes for lithium-ion batteries," *Electrochemistry Communications*, vol. 6, pp. 689-692, 2004.
145. J. Shu, H. Li , R. Z. Yang, Y. Shi, and X. J. Huang, "Cage-like carbon nanotubes/Si composite as anode material for lithium ion batteries," *Electrochemistry Communications*, vol. 8, pp. 51-54, 2006.
146. C. S. Wang, G. T. Wu, X. B. Zhang, Z. F. Qi, and W. Z. J. Li, "Lithium insertion in carbon-silicon composite materials produced by mechanical milling," *Electrochemical Society*, vol. 145, pp. 2751-2758, 1998.

147. M. Endo, T. Hayashi, Y. A. Kim, K. Tantrakarn, T. Yanagisawa, and M. S. Dresselhaus, "Nanofiber toughened polyethylene composites," *Carbon*, vol. 42, pp. 2329-2331, 2004.
148. V. Khomenko, E. Frackowiak, and F. Beguin, "Determination of the specific capacitance of conducting polymer/nanotubes composite electrodes using different cell configurations," *Electrochimica Acta*, vol. 50, pp. 2499-2506, 2005.
149. X. J. He, J. H. Du, Z. Ying, and H. M. Cheng, "Positive temperature coefficient effect in multiwalled carbon nanotube/high-density polyethylene composites," *Applied Physics Letters*, vol. 86, p. 062112, 2005.
150. H. -Y. Lee, and S. M. Lee, "Carbon-coated nano-Si dispersed oxides/graphite composites as anode material for lithium ion batteries," *Electrochemistry Communications*, vol. 6, pp. 465-469, 2004.
151. G. Derrien, J. Hassoun, S. Panero, and B. Scrosati, "Nanostructured Sn-C composite as an advanced anode material in high-performance lithium-ion batteries," *Advanced Materials*, vol. 19, pp. 2336-2340, 2007.
152. B. K. Guo, J. Shu, K. Tang, Y. Bai, Z. X. Wang, and L. Q. Chen, "Nano-Sn/hard carbon composite anode material with high-initial coulombic efficiency," *Journal of Power Sources*, vol. 177, pp. 205-210, 2008.
153. T. P. Kumar, R. Ramesh, Y. Y. Lin, and G. T. K. Fey, "Tin-filled carbon nanotubes as insertion anode materials for lithium-ion batteries", *Electrochemistry Communications*, vol. 6, pp. 520-525, 2004.
154. M. Noh, Y. Kwon, H. Lee, J. Cho, Y. Kim, and M. G. Kim, "Amorphous carbon-coated tin anode material for lithium secondary battery," *Chemistry of Materials*, vol. 17, pp. 1926-1929, 2005.
155. T. Morishita, T. Hirabayashi, T. Okuni, N. Ota, and M. Inagaki, "Preparation of carbon-coated Sn Powders and their loading onto graphite flakes for lithium ion secondary battery," *Journal of Power Sources*, vol. 160, pp. 638-644, 2006.
156. K. T. Lee, Y. S. Jung, and S. M. Oh, "Synthesis of tin-encapsulated spherical hollow carbon for anode material in lithium secondary batteries," *Journal of the American Chemical Society*, vol. 125, pp. 5652-5653, 2003.
157. X. Sun, J. Liu, and Y. Li, "Oxides@C core-shell nanostructures: one-pot synthesis, rational conversion, and Li storage property," *Chemistry of Materials*, vol. 18, pp. 3486-3494, 2006.
158. M. S. Park, Y. M. Kang, J. H. Kim, G. X. Wang, S. X. Dou, and H. K. Liu, "Effects of low-temperature carbon encapsulation on the electrochemical performance of SnO_2 nanopowders," *Carbon*, vol. 46, pp. 35-40, 2008.
159. S. H. Ng, J. Wang, K. Konstantinov, D. Wexler, J. Chen, and H. K. Liu, "Spray pyrolyzed PbO-carbon nanocomposites as anode for lithium-ion batteries," *Journal of the Electrochemical Society*, vol. 153, pp. A787-A797, 2006.
160. S. H. Ng, J. Wang, D. Wexler, S. Y. Chew, and H. K. Liu, "Amorphous carbon-coated silicon nanocomposites: a low-temperature synthesis via spray pyrolysis and their application as high-capacity anodes for lithium-ion batteries," *Journal of Physical Chemistry C*, vol. 111, pp. 11131-11138, 2007.
161. N. Du, H. Zhang, B. D. Chen, X. Y. Ma, X. H. Huang, J. P. Tu, et al., "Synthesis of polycrystalline SnO_2 nanotubes on carbon nanotube template for anode material of lithium-ion battery," *Materials Research Bulletin*, vol. 44, pp. 211-215, 2009.
162. Z. Y. Wang, G. Chen, and D. G. Xia, "Coating of multi-walled carbon nanotube with SnO_2 films of controlled thickness and its application for Li-ion battery," *Journal of Power Sources*, vol. 184, pp. 432-436, 2008.
163. G. M. An, N. Na, X. R. Zhang, Z. J. Miao, S. D. Miao, K. L. Ding, et al., "SnO_2/carbon nanotube nanocomposites synthesized in supercritical fluids: highly efficient materials for use as a chemical sensor and as the anode of a lithium-ion battery," *Nanotechnology*, vol. 18, p. 435707, 2007.
164. H. Qiao, Z. Zheng, L. Z. Zhang, and L. F. Xiao, "SnO_2@C core-shell spheres: synthesis, characterization, and performance in reversible Li-ion storage," *Journal of Materials Science*, vol. 43, pp. 2778-2784, 2008.

165. X. W. Lou, D. Deng, J. Y. Lee, and L. A. Archer, "Preparation of SnO_2/carbon composite hollow spheres and their lithium storage properties," *Chemistry of Materials*, vol. 20, pp. 6562-6566, 2008.
166. T. Moon, C. Kim, S. -T. Hwang, and B. Park, "Electrochemical properties of disordered-carbon-coated SnO_2 nanoparticles for Li rechargeable batteries," *Electrochemical and Solid-State Letters*, vol. 9(9), pp. A408-A411, 2006.
167. M. H. Chen, Z. C. Huang, G. T. Wu, G. M. Zhu, J. K. You, and Z. G. Lin, "Synthesis and characterization of SnO-carbon nanotube composite as anode material for lithium-ion batteries," *Materials Research Bulletin*, vol. 38, pp. 831-836, 2003.
168. L. J. Fu, H. Liu, H. P. Zhang, C. Li, T. Zhang, Y. P. Wu, and H. Q. Wu, "Novel TiO_2/C nanocomposites for anode materials of lithium ion batteries," *Journal of Power Sources*, vol. 159, pp. 219-222, 2006.
169. S. Yoon, B. H. K. C. Lee, M. Park, and S. M. Oh, "Preparation of nanotube TiO_2– carbon composite and its anode performance in lithium-ion batteries," *Electrochemical and Solid-State Letters*, vol. 12 (2), pp. A28-A32 , 2009.
170. L. J. Fu, L. C. Yang, Y. Shi, B. Wang, and Y. P. Wu, "Synthesis of carbon coated nanoporous microcomposite and its rate capability for lithium ion battery," *Microporous and Mesoporous Materials*, vol. 117, pp. 515-518, 2009.
171. X. H. Huang, J. P. Tu, C. Q. Zhang, and J. Y. Xiang, , "Net-structured NiO-C nanocomposite as Li-intercalation electrode material," *Electrochemistry Communications*, vol. 9, pp. 1180-1184, 2007.
172. X. H. Huang, J. P. Tu, C. Q. Zhang, X. T. Chen, Y. F. Yuan, and H. M. Wu, "Spherical NiO-C composite for anode material of lithium ion batteries," *Electrochimica Acta*, vol. 52, pp. 4177-4181, 2007.
173. R. Yang, Z. Wang, J. Liu, and L. Chen, "Nano Co_3O_4 particles embedded in porous hard carbon spherules as anode material for Li-ion batteries," *Solid-State Letters*, vol. 7(12), pp. A496-A499, 2004.
174. H. J. Liu, S. H. Bo, W. J. Cui, F. Li, C. X. Wang, and Y. Y. Xia, "Nano-sized cobalt oxide/mesoporous carbon sphere composites as negative electrode material for lithium-ion batteries," *Electrochimica Acta*, vol. 53, pp. 6497-6503, 2008.
175. H. Li, G. Y. Zhu, X. J. Huang, and L. Q. Chen, "Synthesis and electrochemical performance of dendrite-like nanosized SnSb alloy prepared by co-precipitation in alcohol solution at low temperature," *Journal of Materials Chemistry*, vol. 10, pp. 693-696, 2000.
176. H. Li, L. H. Shi, W. Lu, X. J. Huang, and L. Q. Chen, "Studies on capacity loss and capacity fading of nanosized SnSb alloy anode for Li-ion batteries," *Journal of the Electrochemical Society*, vol. 148, pp. A915-A922, 2001.
177. H. Li, X. J. Huang, L. Q. Chen, G. W. Zhou, Z. Zhang, D. P.Yu, et al., "The crystal structural evolution of nano-Si anode caused by lithium insertion and extraction at room temperature," *Solid State Ionics*, vol. 135(1-4), pp. 181-191, 2000.
178. X. D. Wu, H. Li, X. J. Huang, and L. Q. Chen, "Agglomeration and the surface passivating film of Ag Nano-brush electrode in lithium batteries," *Solid State Ionics*, vol. 149(3–4), pp. 185-192, 2002.
179. L. H. Shi, H. Li, Z. X. Wang, X. J. Huang, and L. Q. Chen, "Nano-SnSb alloy deposited on MCMB as an anode material for lithium ion batteries," *Journal of Materials Chemistry*, vol. 11, pp. 1502-1505, 2001.
180. H. Li, Q. Wang, L. H. Shi, L. Q. Chen, and X. J. Huang, "Nanosized SnSb alloy pinning on hard non-graphitic carbon spherules as anode materials for a Li ion battery," *Chemistry of Materials*, vol. 14(1), pp. 103-108, 2002.
181. G. X. Wang, L. Sun, D. H. Bradhurst, S. Zhong, S. X. Dou, and H. K. Liu, "Nanocrystalline NiSi alloy as an anode material for lithium-ion batteries," *Journal of Alloys and Compounds*, vol. 306, pp. 249-252, 2000.
182. I. S. Kim, P. N. Kumta, and G. E. Blomgren, "Si/TiN nanocomposites novel anode materials for Li-ion batteries," *Electrochemical and Solid-State Letters*, vol. 3(11), pp. 493-496, 2000.

183. Y. M. Kang, M. S. Park, M. S. Song, Y. S. Han, and J. Y. Lee, "A relation between the electrochemical behaviors and morphology of Ni-Co_3O_4 composites prepared by the chemical reduction method or the mechanical milling," *Materials Chemistry and Physics*, vol. 105, pp. 245-249, 2007.
184. L. Bazin, S. Mitra, P. L. Taberna, P. Poizot, M. Gressier, M. J. Menu, et al., "High rate capability pure Sn-based nano-architectured electrode assembly for rechargeable lithium batteries," *Journal of Power Sources*, vol. 188, pp. 578-582, 2009.

This page intentionally left blank

CHAPTER 12

Quantum-Dot Devices Based on Carbon Nanotubes

Ali Kashefian Naieni and Alireza Nojeh

12.1 Introduction

Carbon nanotubes (CNTs) can be thought of as hollow cylinders made by rolling a graphene sheet. The diameter of CNTs can be less than a nanometer to tens of nanometers. Depending on the lattice vector that determines the direction of the roll in the graphene sheet, the CNT will have different properties. *Single-walled carbon nanotubes* (SWNTs) consist of just one cylinder, whereas *multi-walled carbon nanotubes* (MWNTs) are made of more than one concentric cylinder (Fig. 12.1).

Because of their extraordinary properties, CNTs are potential candidates for a wide variety of applications. Thanks to the considerable amount of research being done on various aspects of CNTs around the world, our understanding of their properties is developing rapidly.

Electronically, CNTs can be either metallic or semiconducting. The bandgap of semiconducting nanotubes is inversely proportional to their diameter. This wide variety of electronic properties is a remarkable characteristic of CNTs. Because CNTs have a direct bandgap, they are also very promising for optical applications. The Young's modulus and tensile strength of CNTs are extremely high because of the strong, stable sp^2 hybridized bonds between the carbon atoms that form the nanotubes. CNTs also have a very high thermal conductivity (for more information, see Refs. 1–3).

Quantum dots (QDs), that is, zero-dimensional structures, have been used extensively for the study of quantum-mechanical effects. Because of their similarity to atoms in confining electrons and allowing well-separated energy levels, quantum dots are also called "artificial atoms." Using QD-type structures has made the manipulation of

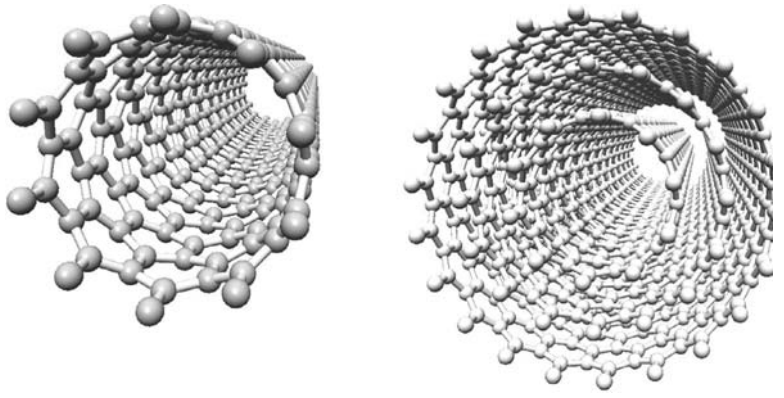


Figure 12.1 A single-walled and a multiwalled CNT.

single electrons possible. Single-electron transistors and diode lasers are examples of their applications (for more information, see Refs. 4 and 5).

In a CNT, electrons are already confined in two dimensions. Nanotubes thus provide a natural vehicle to investigate quantum phenomena in quasi-one-dimensional structures. To make a quantum dot based on CNTs, all that is needed is confinement in the third dimension. Various methods for creating this confinement have been proposed and implemented, and single-electron effects have been observed in such devices. The purpose of this chapter is to discuss some of these methods and the principles behind them.

The chapter has two parts. First, we briefly review the basic physics of operation of single-electron devices. Classical single-electron effects (arising from the quantized nature of electric charge) in small devices and the orthodox theory, which helps in the study of the transport of electrons in single-electron devices, are introduced. Quantum effects (arising from the discrete nature of energy levels) that can be effective because of small dimensions are then discussed.

In the second part, quantum-dot devices based on CNTs are introduced. Each subsection presents a particular effect that can modify the electronic characteristics of CNTs in a localized manner, followed by a discussion of methods that can be used to make CNT QD devices based on that effect.

12.2 Theory of Single-Electron Devices

Consider a conductive island surrounded by an insulating environment. Initially, the numbers of positive and negative charges on the island are equal. If an electron is transferred to the island from outside, the island is not neutral anymore. In this case, a net electrostatic

force repels any other electron approaching the island. Adding another electron to the island will thus require more energy than that of the first transfer. The electrostatic energy stored in the system is

$$E_c = \frac{e^2}{2C}$$

where C is the capacitance of the island and e is the quantum of charge (the charge of an electron). E_c is called the charging energy and is inversely proportional to the capacitance of the island, which is a function of its size: reduction of the island size decreases the capacitance and results in a higher charging energy. Therefore, the energy barrier created by the first electron on the island can prevent other electrons from moving in if the island is small enough. Typically, the amount of charging energy is considerable for an island with dimensions in the mesoscopic to atomic scale. Using this concept, it is possible to create devices that can manipulate single electrons.

Another effect in small islands, with an origin completely different than the classical charging effect just discussed, is the quantum separation of energy levels. When the size of an island is comparable with the wavelength of electrons occupying it, electrons will be found in discrete energy levels. The difference between adjacent energy states is related to the inverse of the island size.

In a more accurate approach for investigating the transfer of electrons to or from an island, the quantization of the energy levels should also be taken into account. A more general term for the energy needed to add an electron to an island is, therefore,

$$E_a = E_c + E_k$$

where E_a is called the addition energy and E_k is the energy level separation inside the island.[6] It is noteworthy that this relation is still an approximation, and in reality the two effects mentioned previously cannot be combined in a simple additive manner; many-body effects (exchange and correlation energies) influence the energy levels of the system.[7] Figure 12.2 shows the electron addition energy and its components as a function of island diameter for a sphere-shape island.

For devices with diameters in the order of 100 nm, the quantum kinetic energy is negligible in comparison with the charging energy. In a few-nanometer-scale island, E_k plays a major role in the addition energy.[6]

The kinetic or thermal energy of the electrons ($k_B T$, where k_B is the Boltzmann constant), enables them to move between various energy levels and can thus wash out the single-electron effects, unless the addition energy is considerably higher than the thermal energy. Therefore, many experiments on single-electron devices have traditionally

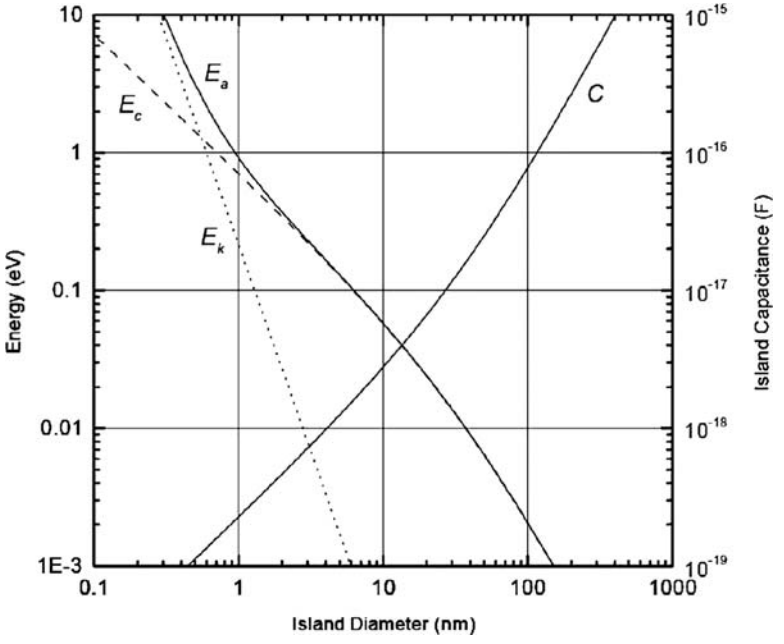


Figure 12.2 Electron addition energy, charging energy, and quantum kinetic energy as a function of the island diameter for a spherical island.[6]

been performed at cryogenic temperatures. However, in atomic- or nanoscale islands, which have very high addition energies, single-electron effects can be observed even at room temperature.

In this section, we first introduce the theory of single-electron devices based on Coulombic effects. Although, because of the size of carbon nanotubes, it is necessary to also consider the energy level separation, this subsection can help in understanding the concepts on which the single-electron devices rely. Next, energy-level separation and resonant tunneling are discussed.

12.2.1 Coulomb Blockade and the Orthodox Theory

Let us start with a single tunnel junction that is biased with a constant current source. The voltage across the junction is measured using a high-impedance voltmeter. The charge on the junction capacitance is a continuous variable and can be a fraction of the unit charge of an electron. On the other hand, the amount of charge that has passed through the junction is a multiple of the quantum of charge. Charge accumulates on the junction until the potential difference across the tunnel junction reaches a threshold value. At this point, an electron tunnels, and the continuously accumulated charge changes

discontinuously. Likharev draws an analogy between this situation and the dripping water from a leaking tap.[8] The frequency of the tunneling event is $f = I/\mathrm{e}$, where I is the current. The change in the electrostatic energy of the system as a result of the tunneling of one electron is

$$\Delta E = \frac{(Q-\mathrm{e})^2}{2C} - \frac{Q^2}{2C} = -\frac{\mathrm{e}\left(Q-\frac{\mathrm{e}}{2}\right)}{C}$$

where Q is the amount of charge on the junction and C is the capacitance of the junction.

If the thermal energy is negligible, the electrons can tunnel only if the energy change is negative. This means that Q must be greater than e/2 for tunneling to happen. Therefore, if $-\frac{\mathrm{e}}{2C} < V < \frac{\mathrm{e}}{2C}$, where $V = Q/C$ is the junction voltage, there will be no tunneling. This is called the Coulomb blockade effect in a single junction.

The tunneling rate of electrons across a tunnel barrier can be calculated using the so-called orthodox theory. According to this theory, this rate depends only on the reduction of the free electrostatic energy of the system as a result of the tunneling event. The tunneling rate can be calculated using the following formula[9,10]:

$$\Gamma(\Delta E) = \frac{\Delta E}{\mathrm{e}^2 R_T \left(\frac{\Delta E}{\mathrm{e}^{\mathrm{k_B}T} - 1}\right)}$$

Here, R_T is the tunnel resistance of the junction, $\mathrm{k_B}$ is the Boltzmann constant, and T is the temperature. ΔE is the electrostatic energy change involved in the tunneling event. When $\mathrm{k_B}T \ll \Delta E$, this equation can be reduced to

$$\Gamma(\Delta E) = \begin{cases} 0 & \Delta E \geq 0 \\ -\dfrac{\Delta E}{\mathrm{e}^2 R_T} & \Delta E < 0 \end{cases}$$

At low temperatures, only the tunneling events that decrease the electrostatic energy can happen. As the applied voltage increases (and thus the electrostatic energy becomes more negative), more electron states in the source region can contribute to the tunneling process (Fig. 12.3), and thus the tunneling rate increases.[6]

In the orthodox theory, quantum-mechanical energy quantization is ignored and the tunneling event is assumed to take a negligibly small time in comparison with other events in the system, especially compared to the time between two successive tunneling events; also, cotunneling (simultaneous tunneling of two or more electrons) is neglected.

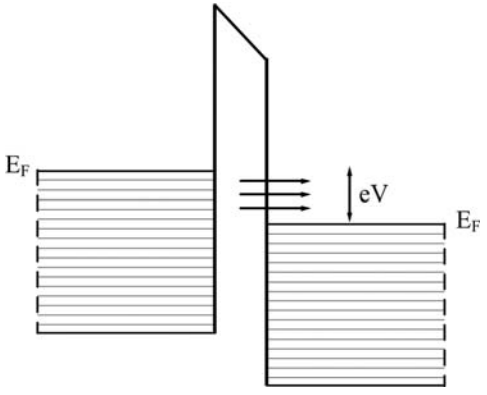


Figure 12.3 Electron energy diagram of a tunnel junction (from Ref. 6, with slight modifications).

The equation discussed previously gives the tunneling rate through one junction. In a practical device, usually more than one junction exists, and various tunneling events are possible, even at the same time. For small systems with a few islands and, therefore, a small number of possible charge states, the probability of each state in time can be calculated using the system of master equations.

$$\frac{dp_i}{dt} = \sum_j [(\Gamma_{j\to i}\, p_j] - \Gamma_{i\to j}\, p_i)$$

$\Gamma_{j\to i}$ shows the tunneling rate from state j to state i.[9,11]

Consider a structure in which an island is connected to two electrodes (which we will call source and drain) with tunnel junctions. No tunneling event, from source and drain to the island or vice versa, can happen when V_{DS} is small and cannot provide the necessary charging energy. Figure 12.4 shows the current-voltage diagram of this device and the energy diagram at different points. In the special case shown in this figure, $C_D > C_S$, so the voltage drop on the source-island junction is more than the other one. As shown in the energy diagrams of Fig. 12.4, as V_{DS} increases in the positive direction, there is no current until the source Fermi level is aligned with one of the energy levels of the island. Before this point, tunneling from source to island increases the electrostatic energy of the system. At V_{th}, the electrons can tunnel to the island with no change in the electrostatic energy. Under this bias, tunneling from the same energy level of the island to the drain reduces the electrostatic energy, which allows the flow of current through the entire system. After this point, the current will charge with the increase in V_{DS}, although with a gradually decreasing slope. As the voltage is increased even further, more of the discrete energy levels of the island enter the range between source and drain Fermi levels. With the inclusion of each new level, the slope of the

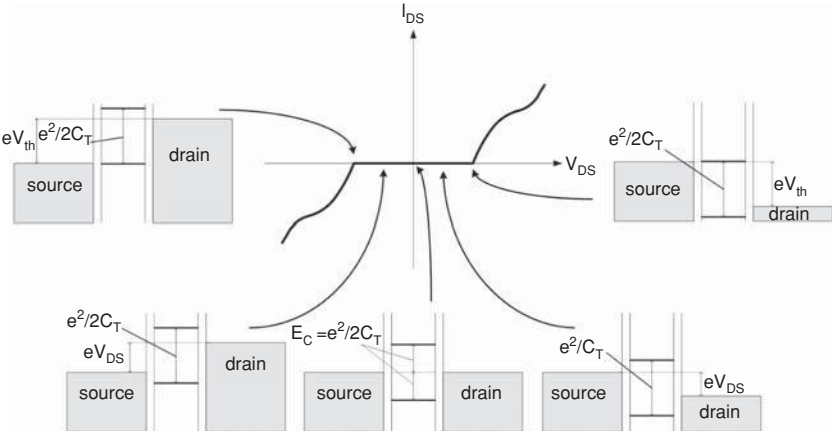


FIGURE 12.4 Typical current-voltage characteristics and energy diagrams of a double-junction structure at different bias values (from Ref. 12, with some modifications).

current-vs.-applied-voltage curve is recovered. If the tunnel resistances of the two junctions are quite different, it can be shown that the I-V characteristics exhibit a distinct stepwise behavior. At negative voltages, charge starts to flow when the condition for tunneling of an electron from the island to the source is reached.

If a gate electrode that is capacitively connected to the island is added to the foregoing device, the resulting structure is a so-called single-electron transistor (Fig. 12.5).

The potential of the island can be controlled by changing the potential of the gate: applying a positive gate voltage lowers all the electronic energy levels. If the gate voltage increases, electrons can eventually accumulate on the island. At the voltage for tunneling of a new electron to the island from source or drain, the amount of charge

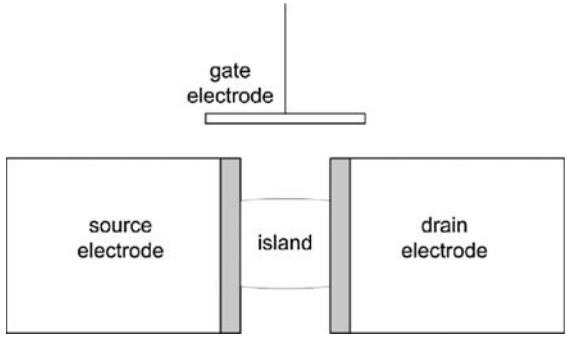


FIGURE 12.5 Schematic of a single-electron transistor.

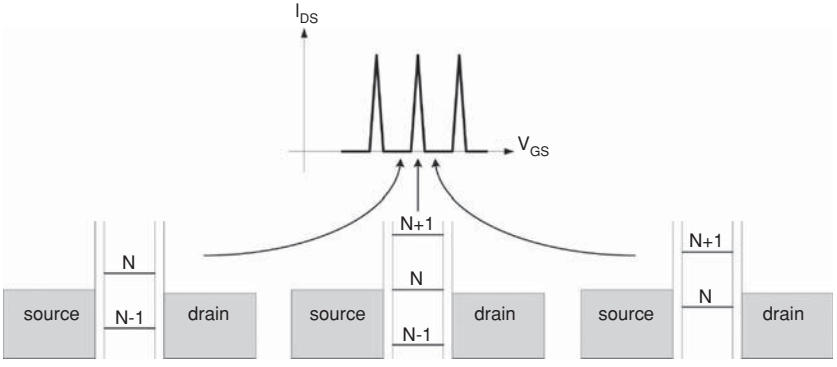


FIGURE 12.6 Drain-source current as a function of gate voltage, and the corresponding energy diagrams of a single-electron transistor (from Ref. 12, with some modifications).

on the island fluctuates by e. As shown in the energy diagrams of Fig. 12.6, before this point, the number of electrons on the island is stable ($N - 1$). When the energy level for the Nth electron is aligned with the Fermi levels of source and drain, electrons can tunnel between the electrodes and the island. In this case, applying a small drain-source voltage breaks the symmetry of the circuit and results in a net flow of electrons passing through the island one by one. A further increase in the gate voltage results in a stable condition with N electrons on the island. As a result, the drain-source current is a periodic function of the gate-source voltage with a period of e/C_G. This is known as Coulomb blockade oscillations.

One can calculate the electrostatic energy change as a result of an electron tunneling from source to island, island to drain, or vice versa for a given number of electrons on the island. By equating these functions of V_{GS} and V_{DS} to zero, four linear relations between V_{GS} and V_{DS} will be derived. Figure 12.7 shows the regions that these relations

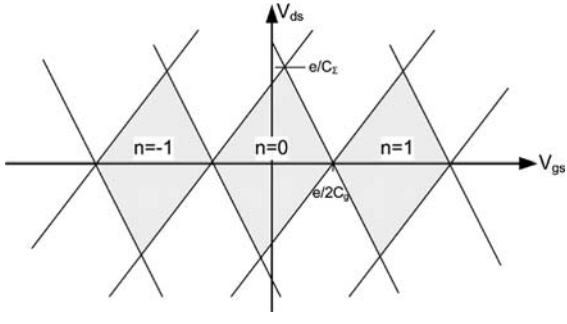


FIGURE 12.7 Coulomb diamond patterns of a single-electron transistor.

specify for a certain number of electrons on the island. In each of these so-called Coulomb diamonds, the current is suppressed because the electrons cannot tunnel from electrodes to the island or from the island to the electrodes, and the number of electrons located on the island is constant. Outside the Coulomb diamonds, the number of electrons on the island can change. The intensity of these fluctuations depends on the difference of the applied voltages from the edges of the diamonds. The shape and size of the diamonds is a function of the gate and junction capacitances.

12.2.2 Resonant Tunneling in Quantum Dots

When a traveling electron encounters a potential barrier, part of its associated wave is reflected and the rest is transmitted. In a double potential barrier structure (Fig. 12.8*A*), the overall transmission probability can be equal to 1 at the resonance energies, where the reflections of the electron wave from the two barriers cancel each other out and the total reflection is 0. Figure 12.8*B* shows the transmission probability of an electron incident on the structure of Fig. 12.8*A* as a function of its energy. The probability has a peak at the resonance energy.[13,14]

Devices that work based on resonant tunneling typically confine electrons in one or two dimensions. In these devices, the source and drain are usually highly doped semiconductors with small bandgaps. The barriers are made of large-bandgap semiconductors (Fig. 12.9*A*). III-V heterostructures are typically used for this purpose.[15] In the figure, without any applied bias, because there is no available state in the quantum well aligned with the occupied states of the electrodes, electrons in the source and drain cannot tunnel through the barriers using resonant tunneling. By increasing the potential difference between source and drain, eventually one of the states in the well will

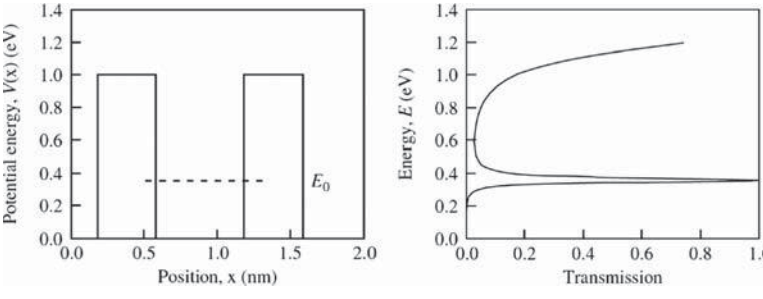


Figure 12.8 *A*) A double potential barrier structure. The resonance energy is shown with a dashed line. (*B*) Transmission probability at different incident electron energies.[13]

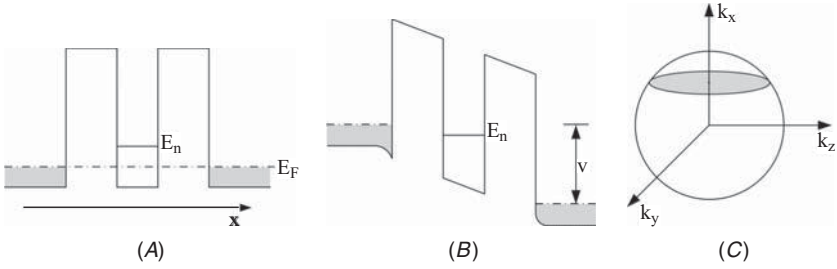


Figure 12.9 (*A*) Energy diagram of a resonant tunneling diode in equilibrium; (*B*) energy diagram of a resonant tunneling diode under bias in the "on" state; (*C*) Fermi sphere of the source. The *k*-states of electrons that can tunnel while conserving the transverse momentum lie on a disk.[16]

enter a range of energy where there are occupied states in the source (between the Fermi level and the bottom of the conduction band). Now, electrons can tunnel from the source into the well. Figure 12.9*B* shows such a situation, where there are also available states in the drain at this energy. The electrons can thus easily tunnel from the well to the drain, and there is a current through the entire structure.[15] The process of using the allowed energy states separated by quantum effects and/or charging energy to regulate the flow of electrons is the essence of single-electron operation.

In a resonant tunneling device, electrons tunnel from the 3D environment of the source to the 2D (or 1D) environment of the quantum well. As there is no potential change in the transverse direction (*y*-*z* plane), the *k*-vector of the electrons is conserved in this plane. We can write the energy of the electrons in the source and in the quantum well as[14]

$$E_{2D} = E_C + \frac{\overline{h}^2 k_x^2}{2m^*} + \frac{\overline{h}^2 k_l^2}{2m^*} \text{ and}$$

$$E_{2D} = E_n + \frac{\overline{h}^2 k_l^2}{2m^*}$$

where E_C is the conduction band edge, E_n is the nth available state in the well, k_x is the component of the electron wave vector in the x direction, k_l is that in the transverse direction, m^* is the effective mass of electrons, and $\overline{h}$ is Planck's constant divided by 2π. Because the energy and transverse wave vector of the electrons do not change after tunneling, it can be concluded that only electrons with a certain component of the wave vector in the x-direction can tunnel to the nth subband of the well.

$$k_x^2 = \frac{2m^*(E_n - E_C)}{\overline{h}^2}$$

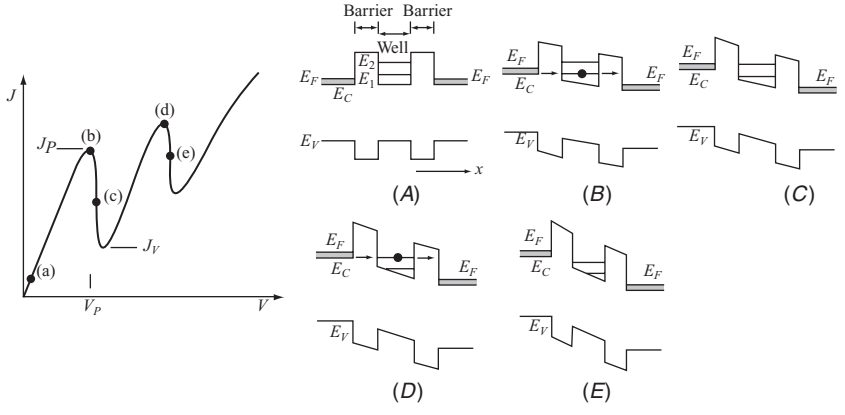


FIGURE 12.10 Current oscillations of a resonant tunneling device and energy diagrams corresponding to different points.[17]

Electrons with this k_x form a disk in the source Fermi sphere (Fig. 12.9*C*). By increasing the voltage, the bottom of the conduction band moves closer to the available state of the quantum well. The disk moves from the pole to the center of the sphere ($E_n = E_C$, $k_x = 0$). Further increase in the bias results in a sharp drop in the current, because there is no electron that can tunnel into the quantum well. This phenomenon is called negative differential resistance. If the voltage is increased enough, the current will experience another peak because of the tunneling of electrons to the next energy state of the well.[14–16]

In resonant tunneling devices, the current experiences a sharp peak when an energy state is between the Fermi levels of source and drain (Fig. 12.10). The resonant tunneling model can explain the current oscillations when the charging effect is negligible.

In microscopic-scale metallic islands, the spacing between the energy levels is typically very small (on the order of microelectron volts). In this case, the separation of energy levels is negligible and Coulomb charging is the dominant factor. In atomic- or nanoscale dots, the Coulomb blockade and the energy quantization may be comparable.

The charging energy and quantum level separation both increase with a decrease in the size of the island. In contrast to the charging energy, which is only a function of the total capacitance (which itself is a function of the shape and size of the island in all dimensions), the energy quantization depends on the size of the island in each dimension. In other words, an island with only one short dimension can have a considerable quantum level separation.[15]

As discussed before, in general, the energy levels of the dot are separated by both Coulomb charging and quantization[18,19]:

$$\Delta E_{\mathrm{T}} = \Delta E + \mathrm{e}^2/C_{\mathrm{G}}$$

where ΔE_T is the total separation of energy levels and ΔE is the quantum-mechanical separation of energy levels. Because the separations between the quantized energy levels are not regular, ΔE_T will be irregular, too. The conductance oscillations in this case have regularity neither in the distance between the peaks nor in the heights of the peaks. The latter is because of different resonant tunneling transmission coefficients at different levels.[18]

12.2.3 Considering Classical and Quantum Effects Together

As mentioned in previous sections, a complete solution for transport through a quantum-dot structure should consider both the charging effect and the quantum level separation in a combined manner. A detailed discussion of this topic is beyond the scope of this chapter. However, much valuable work has been carried out to create more sophisticated models that include both effects.[18] For example, Avrin et al. extended the conventional description of the charging effect to consider the level separation as well.[20,21] In Ref. 20, they showed that for the case of an island with discrete energy levels connected with relatively thick tunneling barriers to two electrodes with continuous energy spectra, the master equation of the orthodox theory is still usable, although the energy dependence of the tunneling rates is different.

Beenakker,[22] Houten et al.,[23] and Meir et al.[24] developed models for the linear response conductance in the resonant tunneling regime that included the charging energy.

Groshev et al. used the non-equilibrium Green's function method for the calculation of transport through a single quantum box level considering the charging effect.[25]

Feng et al.[26] and Fan and Zhang[27] reported on semiclassical simulation of CNTs weakly coupled to metallic electrodes and modulated by a gate electrode. Their approach was based on charging energies and electronic structures determined using the density functional theory.

12.3 Fabrication of Quantum-Dot Devices Based on Carbon Nanotubes

The ultimate goal in nanodevice engineering is to fabricate independent devices with well-behaved and predictable performance that can operate at normal room conditions. An example related to the topic of this chapter could be an integrated circuit of single-electron transistors based on CNT QDs working at room temperature. To make such a circuit, one needs to fabricate CNTs with well-defined properties (chirality, purity, length, alignment) and be able to form the required structures (tunneling barriers, contacts) with predetermined characteristics

in precisely defined locations. Although much effort has been devoted to addressing this problem and significant progress has been made, serious challenges still remain to be solved.

To have a quantum-dot device that can work at room temperature, the sum of charging energy and quantum-mechanical energy level separation of the dot must be significantly more than the thermal energy of electrons. As discussed in previous sections, both these energies are inversely related to the dot size. For these energies to be substantially larger than the thermal energy at room temperature, the device must have dimensions of a few nanometers or smaller. The diameter of a CNT cross section is on the order of a few nanometers. To have a quantum-dot device based on CNTs, which can work at room temperature, we need to make barriers very close to each other on the nanotube (a few tens of nanometers maximum); however, that is not a trivial task with currently available methods.

None of the available techniques for aligned growth of CNTs can provide full control over the type and final configuration of carbon nanotubes on the substrate surface. This lack of control can make the behavior of similarly fabricated devices quite different, and so the reproducibility of the results is a matter of trial and error. This is an important disadvantage in making devices based on CNTs.

Changing the mechanical configuration of a CNT, applying electric potential to it, exposing it to chemicals, or creating CNT-metal interfaces can alter the edges of conduction or valence bands with respect to each other, make the bands bend, move the Fermi energy level, or cause a Schottky barrier, respectively. Various methods based on these phenomena can be used to make the potential barriers needed for a quantum device.

Mechanical perturbations include bends, deformations, strain, and those resulting from intrinsic and extrinsic defects. A wide variety of techniques for the introduction of mechanical perturbations to a CNT have been reported. Some of these make multiple barriers in one process (e.g., making defects in the carbon nanotube using plasma). These methods suffer from the lack of control over the location of the barriers on the tube and each barrier's exact properties. Another group of techniques try to build barriers at specific locations (e.g., making deformations on the carbon nanotube using *atomic force microscopy*, AFM). As each barrier needs to be made separately, fabrication of more complex devices is difficult using this group of methods.

Using electric potentials for the implementation of barriers can improve the control over the specifications of the device. If the electrodes needed to apply the potentials are made using normal fabrication techniques, the minimum achievable size of the device is restricted. Other CNTs can be used as gate electrodes to address this problem. In this case, aligned CNT growth methods should be used, which makes the fabrication more complicated.

Exposure of CNTs to various chemicals can help in making n- or p-type regions on the nanotube. However, the random distribution of adsorbates along the nanotube will not allow the creation of regions with predetermined characteristics.

The Schottky barrier-based techniques cannot engineer the height of the barriers exactly. Because of the same problem as with electric potential techniques, fabrication of devices with lengths of less than 100 nm is challenging with this method; however, successful experiments have been reported.

Currently, most of the reports on this topic are restricted to the demonstration of single-electron effects in one test device rather than building more complex devices because of the fabrication difficulties mentioned earlier. Nonetheless, although there are many challenges to be met before CNT QD devices can appear in commercial products, the unique characteristics of CNTs make their future look very promising.

12.3.1 Inducing Mechanical Perturbations on Carbon Nanotubes

Effects of Strain, Bending, and Deformation on Carbon Nanotubes

Carbon nanotubes with the same atomic bonding structure but with physical deformations can be different electronically. Strain, bends, and deformations can affect the band diagram of a CNT. These alterations commonly happen in CNTs grown with various methods. They can also be used to engineer the electronic properties of CNT-based devices.

In this section, we briefly review the effect of stretching, compression, bending, and radial deformation on nanotubes. These effects have been used or potentially can be used for fabrication of quantum dots.

The Effect of Strain on CNTs The effect of strain on the electrical properties has been investigated theoretically,[28,29] experimentally,[30–33] and by using various simulation methods.[34–40] It has been shown that this effect depends on chirality. For semiconducting nanotubes, strain can either increase or decrease the bandgap based on the value of $(n - m)$ mod 3, where n and m are wrapping indices.[28–33,38] A gap opens up in the band structure of a metallic zigzag nanotube around the Fermi level and increases with compression or stretching.[39] Because of their high symmetry, under tensile strain, armchair tubes show very stable electrical behavior, and no bandgap opening is observed. The effect of strain on bandgap is weaker in a tube with a chiral angle close to the armchair case than in a tube close to the zigzag structure.[28,37]

Using an AFM is a common method for investigating the mechanical characteristics of nanotubes. A pioneering experiment on the electrical properties of a strained tube was reported by Tombler et al.[32]

They used an AFM to push down on a CNT that had been suspended over a trench. They attributed the reduction in the conductance of the strained tube to the change of the nature of the bonds from sp^2 to sp^3 in the contact region of the AFM tip and the nanotube. Maiti et al. suggested that the reduction in the conductance of a zigzag tube under strain is because of the bandgap opening everywhere in the tube.[37] The experimental results of Minot et al.[30] and Cao et al.[31] were in agreement with Maiti's explanation, although, as also suggested by these authors, other mechanisms may also be effective in the change in the transport characteristics of different kinds of nanotubes under strain. He et al. explained the reduction of the current in a metallic zigzag tube under strain with the localization of the electron states[35]: the electron density in the delocalized doubly degenerate π states is reduced with an increase in strain.

The Effect of Cross-Sectional Deformation on CNTs Carbon nanotubes interact with substrates through van der Waals forces. These forces attach the CNT on to the surface and also cause radial deformation in its cross section.[41] Radial deformation can also happen when CNTs go over surface protrusions on the substrate.

Mazzoni and Chacham[42] and Peng and Cho[43] investigated the semiconductor-metal and semiconductor-metal-semiconductor transitions of a zigzag nanotube as a function of cross-sectional deformation, respectively. The origin of the semiconductor-metal transition is the decrease of the conduction band with deformation. As the deformation increases, the valence band energy decreases, and this results in the reopening of the bandgap.

Density functional theory simulation results of Shan et al. confirmed the bandgap closure of various semiconducting zigzag nanotubes as a result of radial deformation.[44] They demonstrated that the bandgap is reduced to zero when the top and bottom sections of the deformed tube are at a certain distance from each other. They suggested that this shows the major role of the maximal cross-sectional curvature of the tubes in their electronic properties. Results for metallic zigzag nanotubes show a bandgap opening. The magnitude of the bandgap change in metallic CNTs is substantially smaller than that in semiconducting tubes.

Nishidate and Hasegawa simulated various semiconducting zigzag nanotubes.[45] They showed that the bandgap change is completely dependent on the radius of the region with the highest curvature on the CNT cross section ($R_{\min}$). According to their results, the bandgap remains almost constant when $R_{\min} > 3.2$ Å and reduces to zero when $R_{\min} \approx 2.4$ Å. The spatial distribution of the conduction band minimum state is concentrated on the high-curvature regions, whereas that of the valence band maximum remains uniform on all the atoms in the cross-sectional plane.

Armchair CNTs show more stable properties as a function of small deformations than zigzag CNTs.[37,46] Mehrez et al. simulated the deformation of armchair nanotubes in an AFM deformation experiment and showed that the bandgap can open up as a result of the interaction of the top and bottom carbon layers of the squashed CNT.[47] The mismatch between the two layers becomes important in further deformations, and this can result in closure and then reopening of the bandgap with more deformation. Under strong deformation, the CNT may lose its structure and show metallic behavior. Gomez-Navarro et al. observed such bandgap oscillations experimentally.[48]

In a cross structure, both the top and the bottom nanotubes deform. Nojeh et al. showed that the deformation induced in the top CNT might lead to two barriers in the conduction band.[49] Because these barriers are very close to each other (Fig. 12.11) as a result of the special configuration of this structure, the resulting dot is very small, which means this device could potentially work at room temperature.

Vitali et al. investigated the density of states of a semiconducting CNT in a cross structure using scanning tunneling microscopy.[50] They observed that a sharp transition from semiconducting to metallic occurs exactly at the intersection of the nanotubes.

The Effect of Bending on CNTs Another mechanical alteration that can change the electronic properties of nanotubes is bending. Bent regions can be observed in CNTs grown using various methods. Depending on the distribution of the bending on the CNT, two different kinds of mechanical behavior can be observed: the bending can be either local or uniformly distributed over a relatively long section of the nanotube. Obviously, bending will naturally lead to some degree of cross-sectional deformation as well. Strong bending in a small portion of the length can result in kinks. A main result of the kink is the localization of π bonds in this region, which causes a decrease in the overall conductance of metallic CNTs.[51] In the case of semiconducting nanotubes, quantum-dot behavior in the kinked area because of discrete energy levels localized in that region has been reported.[52]

The main difference between a kink and a uniform distribution of the bending is that uniform bending does not result in considerable σ-π hybridization. No metal-to-semiconductor or semiconductor-to-metal transition happens as a result of uniform bending.[53] A primary theoretical work on bending using a tight-binding model involving only the π electrons has shown that the bending does not change the bandgap of armchair carbon nanotubes because of their symmetry.[54] Maiti et al.,[37] Rochefort et al.,[51] and Chibotaru et al.[55] confirmed that changes in the density of states and conductance of armchair tubes under uniform bending are negligible. A bandgap opens in

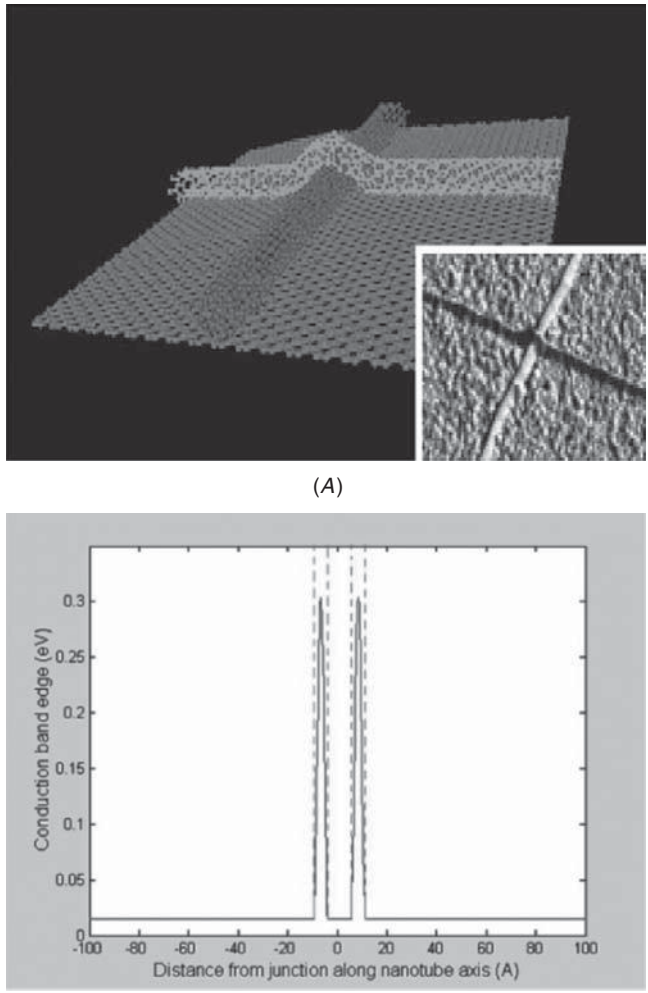


FIGURE 12.11 CNT cross structure (simulation and atomic force micrograph) and conduction band change of the top CNT as a result of deformation.[49]

metallic zigzag CNTs as the bending angle increases.[37,55,56] The simulation results of Farajian et al. showed that the current passing through a semiconducting zigzag tube increases with an increase in the bending angle.[53] Also, it is noteworthy that zigzag tubes show more stiffness against becoming kinked than armchair tubes because of the existence of bonds parallel to the tube axis in the zigzag structure.[53]

Quantum-Dot Devices Based on Bending, Stretching, and Deformation of Carbon Nanotubes

To fabricate QD devices based on the effects just discussed, one must introduce mechanical alterations to a fabricated CNT using available techniques (e.g., using an atomic force microscope) or try to use the mechanical changes that could happen to the CNT during growth (e.g., using fabricated steps on the surface).

One method to make the required tunnel barriers for a quantum dot is to create two kinks on a metallic CNT using AFM. If the kinks are made sufficiently close to each other, single-electron effects can be observed at room temperature. Figure 12.12 shows a device built using this method by Postma et al.[57] The length of the quantum dot can be as small as 20 nm. They were able to see single-electron effects at room temperature. A similar device was reported by D. Bozovic et al.[58]

Biercuk et al. made a device based on AFM-induced kinks and with a gate electrode in the vicinity of each kink. By applying different voltages to the gates, the quantum barriers could be changed from transparent to opaque.[59]

Bezryadin et al. investigated a structure in which a CNT crosses multiple palladium electrodes and performed two-probe and four-probe transport measurements between the electrodes. They attributed the observed quantum effects to the QDs made by barriers induced in the nanotube at the edges of each electrode. The CNT bends at the edges of each electrode because of van der Waals forces between the CNT and the substrate.[60]

Stokes and Khondaker used a CNT that passes over a protruding aluminum gate to make a quantum-dot device (Fig. 12.13). They were

Figure 12.12 QD made using two kinks created by AFM manipulation (scale bar is 25 nm).[57]

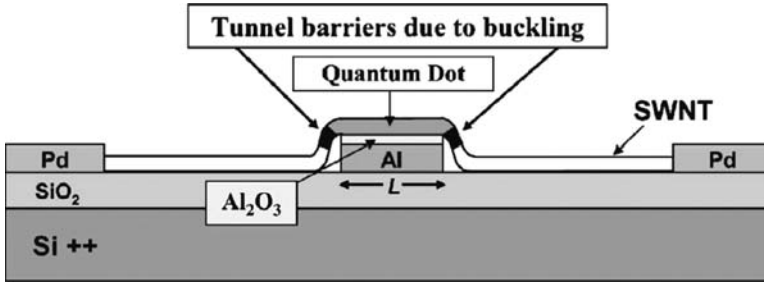


FIGURE 12.13 Schematic of Stokes and Khondaker's device, where a QD is made in a CNT resting on a protruding gate.[61]

able to observe the quantum-dot effects and showed that the tunnel barriers were induced because of the buckling of the CNT at the edges of the gate.[61]

12.3.2 Applying External Electric Potential to Carbon Nanotubes

Effects of External Electric Potential on Carbon Nanotubes

The primary structure for fabrication of single-electron devices based on a carbon nanotube is a carbon nanotube field-effect transistor. By gating the CNT properly, one can make electronically different regions on the nanotube. This method can be used to make devices such as p-n junction[62] or p-i-n junction[63] diodes, transistors,[64,65] and QD-based devices.

There are two mechanisms based on which CNT FETs work.[66,67] In Schottky barrier carbon nanotube field-effect transistors, the contacts have an important role in controlling the conductance of the device. The gate controls the conductance by changing the width of the Schottky barriers at the metal-nanotube interfaces. The electric field at the interface between the CNT and electrode has a major effect on the device performance. The device characteristics are sensitive to the relative position of the contact and the gate, oxide thickness, and the geometries of the contacts.[68]

If there is no considerable Schottky barrier at the contacts, the CNT channel will play the dominant role in controlling the conductance of the device. It has been shown that metals such as palladium or gold make ohmic contacts or contacts with negative Schottky barriers with CNTs.[69,70] As the contacts do not have a major effect on the properties of such devices, it is suggested that the conductance is controlled by band bending in the nanotube channel because of the applied gate voltage.[66,67]

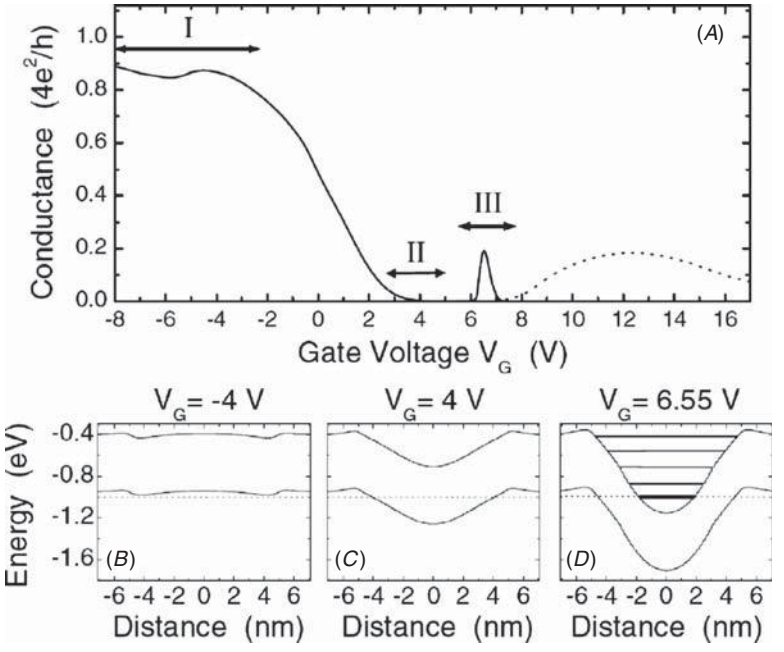


Figure 12.14 (*A*) Conductance vs. gate voltage of a CNT FET with ohmic contacts. (*B–D*) Band diagram in each of the transport regimes of the device.[71]

Leonard et al. investigated the behavior of this type of device using tight binding calculations.[71] The result is shown in Fig. 12.14. The device shows three different transport regimes. At low gate voltages, there is no barrier on the way of the carriers (in this case, holes) through the channel (Fig. 12.14*B*). This is the ON state of the transistor, and the conductance is high. In the second regime, the conductance reduces to zero because of the barrier in the channel induced by the gate voltage. This is the OFF state. Further increase in gate voltage results in the pulling of the conduction band to values less than the Fermi level. The channel is in the inversion state. For small channels, this band bending creates an electrostatically defined QD. The peak in the conductance is because of resonant tunneling of electrons through the separated energy levels of the quantum dot.

If a nanometer-scale gate is used (e.g., using another carbon nanotube as the gate), the electric field at source and drain contacts will not be affected significantly by the gate voltage. Figure 12.15 shows the band diagram of a CNT FET with ohmic (Fig. 12.15*A*) and Schottky (Fig. 12.15*B*) contacts controlled using a back gate or a local gate, respectively, at different gate voltages. In the upper rows of Figs. 12.15*A* and 12.15*B*, the band diagrams of two different kinds of CNT FETs

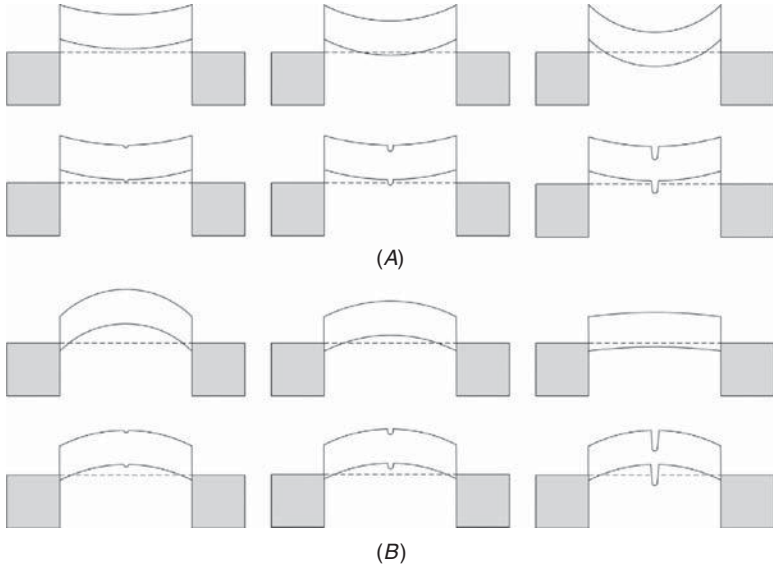


Figure 12.15 Band diagram of CNT FET with back gate (*upper row*) and local gate (*lower row*) at different gate voltages with (*A*) ohmic and (*B*) Schottky contacts.[67]

with back gates are shown. The difference between the two is that the properties of the SB FET are controlled by the contact barriers, but the CNT band diagram has the major effect on the charge transport through the FET with ohmic contacts. As shown in the upper row of Fig. 12.15*A*, the main barrier in front of the carriers (in this case, holes) comes from the bending of the valence band as a result of back-gate positive voltage. Applying a negative gate voltage in an SB FET reduces the width of the Schottky barriers and increases the transport rate of carriers (upper row of Fig. 12.15*B*). Using the local gate, the main barrier in both cases is induced in a short length of the CNT. The switching between ON and OFF states is mainly controlled by this barrier.

QD Devices Based on Carbon Nanotubes Using Electric Potential

Placing multiple metallic electrodes over a semiconducting nanotube is one way to implement CNT QD devices. By applying suitable voltages to independent gates, the CNT region in the vicinity of the gate can be depleted to make the required tunneling barriers. The problem with this method is that the width of the gate is limited by the lithography resolution. Single, double, and multiple quantum-dot devices made with this method have been reported.[72–75] Figure 12.16 shows a schematic of one such device.

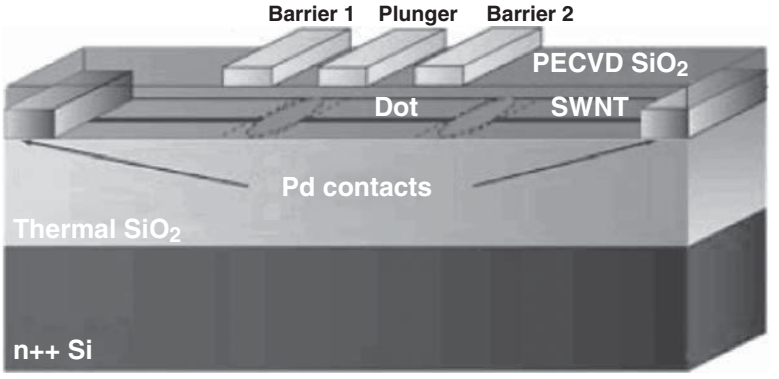


FIGURE 12.16 Schematic of a gate defined quantum-dot device. The outer gates create the tunnel barriers by depleting the segment of nanotube beneath them. The center gate controls the chemical potential of the dot.[73]

Another way to use gates for creating different regions on a CNT was reported by Steele et al.[76] Figure 12.17 shows the schematic of the device with "split gates" and the band diagram of the nanotube for two different sets of applied voltages. The potential of the CNT on the two sides is completely determined by the split gates. Over the trench, the potential of the back gate can affect the CNT. As a result, carriers are confined in the quantum dot using two back-to-back p-n junctions (created by the back gate and the split gates). As the CNT growth is the last step of the fabrication process, the CNT in this device can potentially be ultraclean, with few structural defects.

In order to overcome the limit of the lithography resolution that was present in the previous methods, one can use a metallic CNT for gating a semiconducting one. Although growing CNTs in

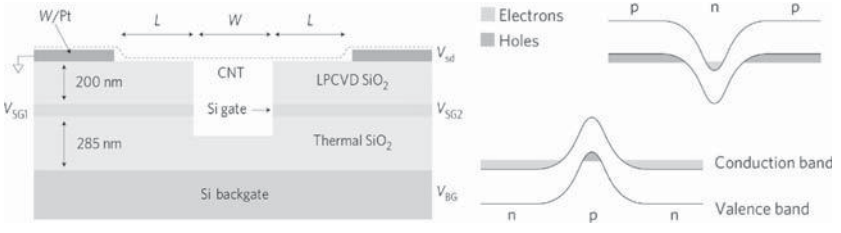


FIGURE 12.17 (*A*) Schematic a gate defined quantum-dot device. The potential of the back gate bends the energy bands of the CNT over the trench. (*B*) Energy diagram of the device for two different cases of applied voltages.[76]

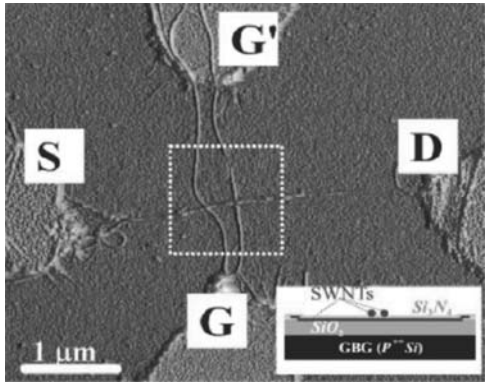


Figure 12.18 Two metallic SWNT bundles gating a semiconducting SWNT.[78]

predetermined positions is not an easy task, QD devices fabricated with this method have been reported (Fig. 12.18).[67,77,78]

12.3.3 QD Devices Based on Carbon Nanotubes Using Metal-CNT Schottky Barriers

Schottky barriers at metal-CNT interfaces in a CNT FET structure can be used as the tunnel barriers required for a QD. The current across a Schottky contact consists of thermionic current (carriers thermally excited over the Schottky barrier) and tunneling current. The small island size is not a sufficient condition for observation of quantum-dot effects at room temperature: there are reports of CNTFETs with very small channel sizes (10 to 50 nm) that show regular FET characteristics at room temperature.[79,80] Only if the thermionic current is negligible (the barrier is high enough) and the charging energy exceeds the carrier's thermal energy can the conductance oscillations be observed.[81] Various CNT single-electron transistors have been fabricated using this method.[82–86]

A problem with this method is that the minimum size of the island is again limited by the resolution of the lithography process being used. An approach to solving this problem is shadow evaporation. In this technique, one electrode is formed using photolithography. The sample is tilted during the deposition of the second electrode, so it is partially masked with the first one (Fig. 12.19). A channel with a length down to 10 nm can be fabricated using this method.[79,81]

Li et al. used this method with two different metals for source and drain electrodes and made a CNT single-electron transistor with asymmetric contacts.[87] The asymmetric barriers result in asymmetric current oscillations under positive and negative V_{DS} at low temperature (tunneling current dominant) and diodelike characteristics at room temperature (thermionic current dominant).

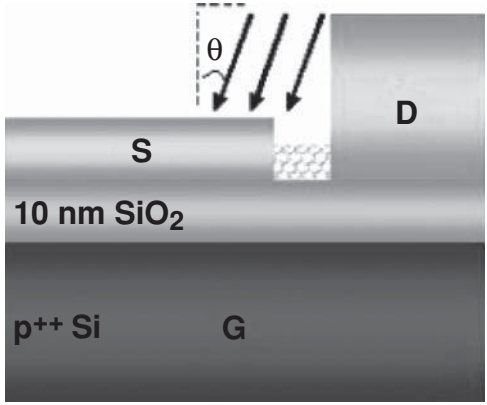


Figure 12.19 Schematic of the shadow evaporation technique.[79]

12.3.4 Inducing Structural Defects on Carbon Nanotubes

Effect of Structural Defects on Carbon Nanotubes

Substitution of a carbon atom with other atoms,[88] monovacancies,[35] divacancies,[89] and multiple vacancies[90] can affect the conductance of a carbon nanotube. These kinds of defects can be formed during the fabrication of CNTs. Although these defects affect transport through the nanotube, as long as the number of removed atoms is not considerable, they cannot form a significant potential barrier for carriers. Experimentally, it was observed that highly damaged sites in carbon nanotubes can play the role of tunnel barriers.[91–100]

QD Devices Based on the CNT Structure Using Defect Sites as Tunnel Barriers

To create nanotube QDs with defects as tunnel barriers, one can either use the defects naturally formed during the growth, or induce the required defect sites on the CNT after the growth. Matsumoto et al. reported on the multidot behavior of a CNT-based transistor made using *chemical vapor deposition* (CVD)-grown nanotubes.[91] They mentioned the defects created during the growth as the origin of the multidot behavior.

Ion beams can be used to damage the CNT in desired locations. Tsuya et al.[92] and Ishibashi et al.[93] exposed the CNT to an argon beam through narrow openings in an e-beam resist layer, formed with electron beam lithography (Fig. 12.20*A*). Using this method, the tunnel barriers can be formed at predetermined locations, and the height of the barriers can be changed by alteration of the ion beam dose. A drawback of this method is its dependence on the lithography resolution.

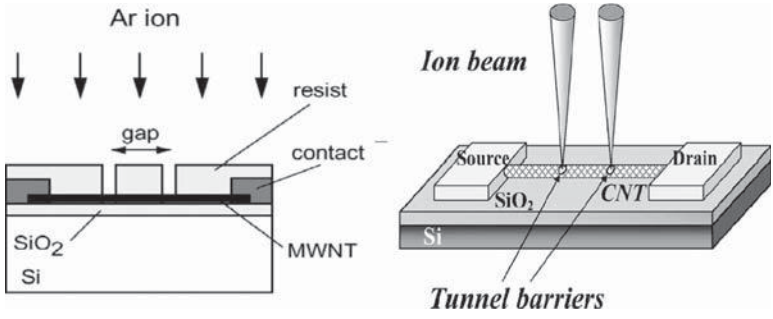


Figure 12.20 Using (*A*) lithography and ion beam[93] and (*B*) focused ion beam[94] for formation of barriers to create a QD on a CNT.

Alternatively, the ion beam itself can be focused and irradiate precisely-defined positions. Maehashi et al.[94] used a focused ion beam for introduction of defects to a CNTFET having a SWCNT channel (Fig. 12.20*B*). The CNT single-electron transistor fabricated with this method could operate at room temperature.

Park et al.[95] applied a potential difference between the metal-coated tip of an atomic force microscope and a CNT to electrically break (cut) or make tunnel barriers (nick) at certain points on the nanotube. By controlling the magnitude and duration of the voltage pulse, one can control the resulting effects on the CNT. This method can be performed in the noncontact mode of the AFM as well.[96,97] In addition to the parameters mentioned earlier, the distance between the tip and the CNT is important in this technique. Precise control of the dot size is possible with this method, and QDs with lengths as small as 15 nm were fabricated.[97] The formation of the barrier in these experiments is attributed to either carbon bond dissociation or local oxidation of the CNT.

Kamimura et al. reported the fabrication of a multidot structure using a thermal chemical process.[98] They obtained a high charging energy and were able to observe the Coulomb diamonds even at room temperature. Maeda et al. used $La(NO_3)_3$ to create the necessary defects on the CNT.[99] The oxygen in $La(NO_3)_3$ reacts with some of the carbon atoms of the CNT, and defect sites are created. Although the exact location of the barriers cannot be controlled, the number or size of the defects can be controlled by the amount of $La(NO_3)_3$ in the solution.

Iwasaki et al. used an oxygen plasma to induce defects on a CNT buried under a SiO_2 protective layer.[100] The result was a multidot structure. The number of defects can be controlled by the thickness of the SiO_2 layer (Fig. 12.21).

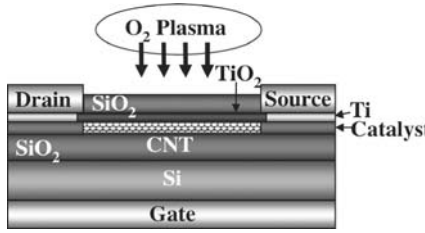


FIGURE 12.21
Using plasma for creation of defects on a CNT.[100]

12.3.5 Chemical Modulation of Carbon Nanotubes

Effect of Chemical Doping on Carbon Nanotubes

Because of the strong and fully satisfied covalent bonds between carbon atoms in a CNT structure, a carbon nanotube is chemically stable and inert. Although attaching to the surface of CNTs with covalent bonds is rather difficult for other atoms or molecules, noncovalent bonding has been shown to be quite easily achievable.[101] Various atoms and molecules such as potassium, cesium, bromine, O_2, NO_2, NH_3, and amine-rich polymers have been deposited on SWNTs and MWNTs.[101,102] Considerable alterations in the electrical properties of nanotubes in CNTFET structures due to exposure to these dopants have been reported.[103–106] Based on these mechanisms, chemical sensors for the detection of NO_2 and NH_3 gases using CNTs have been proposed.[105] CNTFETs usually show p-type behavior. This is attributed to the adsorption of oxygen from the ambient.[107] When exposed to NO_2, the conductance of the CNTFET increases significantly. The oxidizing power of adsorbed NO_2 molecules attracts electrons and increases the number of holes in the nanotube. On the other hand, NH_3 reduces the conductance because of its electron-donating nature.[101,103,105] The other materials mentioned previously induce similar trends depending on their characteristics.

Quantum-Dot Devices Based on Carbon Nanotubes Using Chemical Doping

Zhou et al. doped half of the length of a semiconducting CNT with potassium by covering the rest with *poly(methyl methacrylate)* (PMMA).[108] The resulting device exhibited regular p-n junction behavior or negative differential conductance at different electrostatic gate voltages. At low temperatures and in a specific range of gate voltages, the device current showed Coulomb diamond patterns because of single or multiple quantum dots formed on the tube as a result of fluctuations in the doping concentration. The nonuniformity of dopants leads to multiple local band bendings, which can play the role of energy barriers needed to form quantum dots.

Kong et al. reported similar results for an all-length-doped semiconducting CNT.[106] Different regimes of operation were

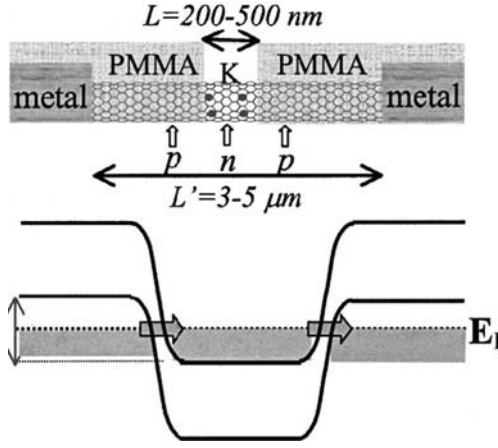


Figure 12.22 Single-electron transistor made by doping the central region of the nanotube with potassium and its energy band diagram.[107]

distinguishable on the conductivity diagram vs. gate voltage. Conductivity oscillation peaks showed different periods and shapes depending on the number and location of quantum dots formed on the CNT because of the relative condition of the bands and Fermi level as a function of gate voltage.

The same group extended the method to make a p-n-p transistor on a CNTFET by exposing 200 to 500 nm of the central region of the CNT to potassium while the rest was covered by PMMA.[107] Figure 12.22 shows a schematic of the device and its energy band diagram. At low temperatures, this device showed clear Coulomb charging and single-quantum-dot behavior. The quantum dot is formed in the n region with p-n junctions as barriers.

Cui et al.[109] modified around 10 nm of the length of a small bundle of CNTs by exposure to an oxygen plasma for a short period of time (2 s). The resulting device showed single-electron tunneling at room temperature. The authors attributed the behavior to chemical changes of the uncovered section due to exposure to oxygen plasma.

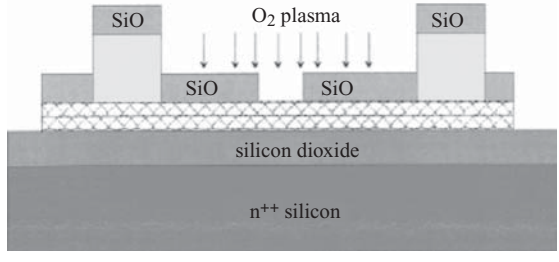


Figure 12.23 Chemical modification of a small section of CNT using oxygen plasma to make a quantum dot.[109]

To expose such a short length, they used a V_2O_5 nanowire that crossed a thin bundle of nanotubes to make a narrow opening on the tube by deposition of SiO on the entire structure and subsequent etching of the nanowire (Fig. 12.23).

12.4 Conclusions

The unique physical structure of carbon nanotubes makes them a natural choice for building quantum-dot/single-electron devices based on them: All needed is to go from their one-dimensional structure to a zero-dimensional one. In such devices the flow of electrons is controlled by the allowed energy states, which are separated because of quantum and/or charging effects.

To make the necessary potential barriers in order to create a confined, zero-dimensional region, one needs to induce localized changes in the electronic structure of the nanotube. A variety of methods can be used to achieve this. These include various types of mechanical deformation, applying electric potential, using metal-nanotube Schottky contacts, inducing mechanical defects, and using chemicals to dope the nanotube. Each of these methods has its own advantages and difficulties. Despite the challenges ahead, nanotubes seem to be very promising for this field of application.

References

1. V. N. Popov, "Carbon nanotubes: properties and applications," *Materials Science and Engineering R*, vol. 43, pp. 61-102, 2004.
2. M. P. Anantram and F. Leonard, "Physics of carbon nanotube electronic devices," *Reports on Progress in Physics*, vol. 69, pp. 507-561, 2006.
3. J. Han, "Structures and properties of carbon nanotubes," in *Carbon Nanotubes: Science and Applications*, M. Meyyappan, editor, Boca Raton, FL, CRC Press, pp. 2-21, 2005.
4. L. P. Kouwenhoven1, D. G. Austing, and S. Tarucha, "Few-electron quantum dots," *Reports on Progress in Physics*, vol. 64, pp. 701-736, 2001.
5. S. M. Reimann, and M. Manninen, "Electronic structure of quantum dots," *Reviews of Modern Physics*, vol. 74, pp. 1283-1342, 2002.
6. K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, pp. 606-632, 1999.
7. A. Szabo, and N. S. Ostlund, *Modern Quantum Chemistry: Introduction to Advanced Electronic Structure Theory*, Dover Publications, 1996.
8. K. K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall junctions," *IBM Journal of Research and Development*, vol. 32, pp. 144-158, 1988.
9. C. Wasshuber, *Computational Single-Electronics*, New York, Springer, 2001.
10. M. H. Devoret, and H. Grabert, "Introduction to single charge tunneling," in *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*, H. Grabert and M. H. Devoret, editors, New York, Plenum Press, pp. 1-18, 1992.
11. D. V. Averin and K. K. Likharev, "Coulomb blockade of single-electron tunneling, and coherent oscillations in small tunnel junctions," *Journal of Low Temperature Physics*, vol. 62, pp. 345-372, 1986.

12. J. Weis, "Single-electron devices," in *CFN Lectures on Functional Nanostructures*, K. Busch, A. Powell, C. Rothig, G. Schon, and J. Weissmuller, editors, New York, Springer, 2005.
13. A. F. J. Levi, *Applied Quantum Mechanics*, 2nd ed., Cambridge, UK, Cambridge University Press, 2006.
14. J. P. Sun, G. I. Haddad, P. Manzumder, and J. N. Schulman, "Resonant tunneling diodes: models and properties," *Proceedings of the IEEE*, vol. 86, pp. 641-661, 1998.
15. D. Goldhaber-Gordon, M. S. Montemerlo, J. C. Love, G. J. Opiteck, and J. C. Ellenbogen, "Overview of nanoelectronic devices," *Proceedings of the IEEE*, vol. 85, pp. 521-540, 1997.
16. S. Luryi, "Frequency limit of double-barrier resonant-tunneling oscillators," *Applied Physics Letters*, vol. 47, pp. 490-492, 1985.
17. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed., New York, Wiley, 2007.
18. D. K. Ferry, and S. M. Goodnick, *Transport in Nanostructures*, Cambridge, UK, Cambridge University Press, 1997.
19. H. V. Houten, C. W. J. Beenakker, and A. A. M. Staring, "Coulomb-blockade oscillations in semiconductor nanostructures," in *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*, H. Grabert and M. H. Devort, editors, New York, Plenum Press, pp. 167-216, 1992.
20. D. V. Avrin and A. N. Korotkov, "Correlated single-electron tunneling via mesoscopic metal particles: effects of the energy quantization," *Journal of Low Temperature Physics*, vol. 80, pp. 173-185, 1990.
21. D. V. Avrin, A. N. Korotkov, and K. K. Likharev, "Theory of single-electron charging of quantum wells and dots," *Physical Review B*, vol. 44, pp. 6199-6211, 1991.
22. C. W. J. Beenakker, "Theory of Coulomb-blockade oscillations in the conductance of a quantum dot," *Physical Review B*, vol. 44, pp. 1646-1656, 1991.
23. H. V. Houten, C. W. J. Beenakker, and A. A. M. Staring, "Coulomb-blockade oscillations in semiconductor nanostructures," in *Single Charge Tunneling—Coulomb Blockade Phenomena in Nanostructures*, H. Grabert and M. H. Devort, editors, New York, Plenum Press, pp. 167-216, 1992.
24. Y. Meir, N. S. Wingreen, and P. A. Lee, "Transport through a strongly interacting electron system: Theory of periodic conductance oscillations," *Physical Review Letters*, vol. 66, pp. 3048-3051, 1991.
25. A. Groshev, T. Ivanov, and V. Valtchinov, "Charging effects of a single quantum level in a box," *Physical Review Letters*, vol. 66, pp. 1082-1085, 1991.
26. Y. Q. Feng, R. G. Zhang, and S. T. Lee, "Simulation of gate-controlled Coulomb blockades in carbon nanotubes," *Journal of Applied Physics*, vol. 95, pp. 5729-5735, 2004.
27. W. Fan, and R. Zhang, "Single-electron tunneling and Coulomb blockade in carbon based quantum dots," *Frontiers of Physics in China*, vol. 4, pp. 315-326, 2009.
28. L. Yang, M. P. Anantram, J. Han, and J. Lu, "Band-gap change of carbon nanotubes: effect of small uniaxial and torsional strain," *Physical Review B*, vol. 60, pp. 13874-13878, 1999.
29. L. Yang, and J. Han, "Electronic structure of deformed carbon nanotubes," *Physical Review Letters*, vol. 85, pp. 154-157, 2000.
30. E. D. Minot, Y. Yaish, V. Sazonova, J. Y. Park, M. Brink, and P. L. McEuen, "Tuning carbon nanotube bandgaps with strain," *Physical Review Letters*, vol. 90, 156401, 2003.
31. J. Cao, Q. Wang, and H. Dai, "Electromechanical properties of metallic, quasimetallic, and semiconducting carbon nanotubes under stretching," *Physical Review Letters*, vol. 90, p. 157601, 2003.
32. T. W. Tombler, C. Zhou, L. Alexseyev, J. Kong, H. Dai, H. Liu, et al., "Reversible electromechanical characteristics of carbon nanotubes under local-probe manipulation," *Nature*, vol. 405, pp. 769-772, 2000.

33. M. Huang, Y. Wu, B. Chandra, H. Yan, Y. Shan, T. F. Heinz, et al., "Direct measurement of strain-induced changes in the band structure of carbon nanotubes," *Physical Review Letters*, vol. 100, p. 136803, 2008.
34. M. B. Nardelli and J. Bernholc, "Mechanical deformations and coherent transport in carbon nanotubes," *Physical Review B*, vol. 60, pp. R16338–R16341, 1999.
35. Y. He, C. Zhang, C. Cao, and H. P. Cheng, "Effects of strain and defects on the electron conductance of metallic carbon nanotubes," *Physical Review B*, vol. 75, p. 235429, 2007.
36. G. Y. Guo, L. Liu, K. C. Chu, C. S. Jayanthi, and S. Y. Wu, "Electromechanical responses of single-walled carbon nanotubes: interplay between the strain-induced energy-gap opening and the pinning of the Fermi level," *Journal of Applied Physics*, vol. 98, p. 44311, 2005.
37. A. Maiti, A. Svizhenko and M. P. Anantram, "Electronic transport through carbon nanotubes: effects of structural deformation and tube chirality," *Physical Review Letters*, vol. 88, p. 126805, 2002.
38. P. K. Valavala, D. Banyai, M. Seel, and R. Pati, "Self-consistent calculations of strain-induced bandgap changes in semiconducting (n,0) carbon nanotubes," *Physical Review B*, vol. 78, p. 235430, 2008.
39. S. Sreekala, X. H. Peng, P. M. Ajayan, and S. K. Nayak, "Effect of strain on the bandgap and effective mass of zigzag single-wall carbon nanotubes: first-principles density-functional calculations," *Physical Review B*, vol. 77, p. 155434, 2008.
40. Y. R. Chen C. I. Weng, and S. J. Sun, "Electronic properties of zigzag and armchair carbon nanotubes under uniaxial strain," *Journal of Applied Physics*, vol. 104, p. 114310, 2008.
41. T. Hertel, R. E. Walkup, and P. Avouris, "Deformation of carbon nanotubes by surface van der Waals forces," *Physical Review B*, vol. 58, pp. 13870-13873, 1998.
42. Mario S. C. Mazzoni, and H. Chacham, "Bandgap closure of a flattened semiconductor carbon nanotube: a first-principle study," *Applied Physics Letters*, vol. 76, pp. 1561-1563, 2000.
43. S. Peng, and K. Cho, "Nano electro mechanics of semiconducting carbon nanotube," *Journal of Applied Mechanics*, vol. 69, pp. 451-453, 2002.
44. B. Shan, G. W. Lakatos, S. Peng, and K. Cho, "First-principles study of bandgap change in deformed nanotubes," *Applied Physics Letters*, vol. 87, p. 173109, 2005.
45. K. Nishidate and M. Hasegawa, "Universal bandgap modulation by radial deformation in semiconductor single-walled carbon nanotubes," *Physical Review B*, vol. 78, p. 195403, 2008.
46. A. Svizhenko, H. Mehrez, A. M. P. Anantram, and A. Maiti, "Sensing mechanical deformation in carbon nanotubes by electrical response: a computational study," *Proceedings of SPIE*, vol. 5593, pp. 416-428, 2004.
47. H. Mehrez, A. Svizhenko, and M. P. Anantram, "Analysis of band-gap formation in squashed armchair carbon nanotubes," *Physical Review B*, vol. 71, p. 155421, 2005.
48. C. Gomez-Navarro, J. J. Saenz, and J. Gomez-Herrero, "Conductance oscillations in squashed carbon nanotubes," *Physical Review Letters*, vol. 96, p. 76803, 2006.
49. A. Nojeh, G. W. Lakatos, S. Peng, K. Cho and R. F. W. Pease, "A carbon nanotube cross structure as a nanoscale quantum device," *Nano Letters*, vol. 3, pp. 1187-1190, 2003.
50. L. Vitali, M. Burghard, P. Wahl, M. A. Schneider, and K. Kern, "Local pressure-induced metallization of a semiconducting carbon nanotube in a crossed junction," *Physical Review Letters*, vol. 96, 86804, 2006.
51. A. Rochefort, P. Avouris, F. Lesage, and D. R. Salahub, "Electrical and mechanical properties of distorted carbon nanotubes," *Physical Review B*, vol. 60, pp. 13824-13830, 1999.

52. M. S. C. Mazzoni, and H. Chacham, "Atomic restructuring and localized electron states in a bent carbon nanotube: a first-principles study," *Physical Review B*, vol. 61, pp. 7312-7315, 2000.
53. A. A. Farajian, B. I. Yakobson, H. Mizuseki, and Y. Kawazoe, "Electronic transport through bent carbon nanotubes: nanoelectromechanical sensors and switches," *Physical Review B*, vol. 67, p. 205423, 2003.
54. C. L. Kane and E. J. Mele, "Size, shape, and low energy electronic structure of carbon nanotubes," *Physical Review Letters*, vol. 78, pp. 1932-1935, 1997.
55. L. Chibotaru, S. A. Bovin, and A. Ceulemans, "Bend-induced insulating gap in carbon nanotubes," *Physical Review B*, vol. 66, p. 161401, 2002.
56. M. B. Nardelli, "Electronic transport in extended systems: application to carbon nanotubes," *Physical Review B*, vol. 60, pp. 7828-7833, 1999.
57. H. W. Ch. Postma, T. Teepan, Z. Yao, M. Grifoni, and C. Dekker, "Carbon nanotube single-electron transistors at room temperature," *Science*, vol. 293, pp. 76-79, 2001.
58. D. Bozovic, M. Bockrath, J. H. Hafner, C. M. Lieber, H. Park, and M. Tinkham, "Electronic properties of mechanically induced kinks in single-walled carbon nanotubes," *Applied Physics Letters*, vol. 78, pp. 3693-3695, 2001.
59. M. J. Biercuk, N. Mason, J. M. Chow, and C. M. Marcus, "Locally addressable tunnel barriers within a carbon nanotube," *Nano Letters*, vol. 4, pp. 2499-2502, 2004.
60. A. Bezryadin, A. R. M. Verschueren, S. J. Tans, and C. Dekker, "Multiprobe transport experiments on individual single-wall carbon nanotubes," *Physical Review Letters*, vol. 80, pp. 4036-4039, 1998.
61. P. Stokes and S. I. Khondaker, "Controlled fabrication of single electron transistors from single-walled carbon nanotubes," *Applied Physics Letters*, vol. 92, p. 262107, 2008.
62. J. U. Lee, P. P. Gipp and C. M. Heller, "Carbon nanotube p-n junction diodes," *Applied Physics Letters*, vol. 85, pp. 145-147, 2004.
63. K. Bosnick , N. Gabor, and P. McEuen, "Transport in carbon nanotube p-i-n diodes," *Applied Physics Letters*, vol. 89, p. 163121, 2006.
64. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Applied Physics Letters*, vol. 73, pp. 2447-2449, 1998.
65. S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49-52, 1998.
66. M. P. Anantram and F. Leonard, "Physics of carbon nanotube electronic devices," *Reports on Progress in Physics*, vol. 69, pp. 507-561, 2006.
67. J. Y. Park, "Carbon nanotube field-effect transistor with a carbon nanotube gate electrode," *Nanotechnology*, vol. 18, p. 95202, 2007.
68. S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, "Carbon nanotubes as Schottky barrier transistors," *Physical Review Letters*, vol. 89, p. 106801, 2002.
69. A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, pp. 654-657, 2003.
70. Y. Yaish, J. Y. Park, S. Rosenblatt, V. Sazonova, M. Brink, and P. L. McEuen, "Electrical nanoprobing of semiconducting carbon nanotubes using an atomic force microscope," *Physical Review Letters*, vol. 92, p. 46401, 2005.
71. F. Leonard and J. Tersoff, "Multiple functionality in nanotube transistors," *Physical Review Letters*, vol. 88, p. 258302, 2002.
72. N. Mason, M. J. Biercuk, and C. M. Marcus, "Local gate control of a carbon nanotube double quantum dot," *Science*, vol. 303, pp. 655-658, 2004.
73. M. J. Biercuk, S. Garaj, N. Mason J. M. Chow, and C. M. Marcus, "Gate-defined quantum dots on carbon nanotubes," *Nano Letters*, vol. 5, pp. 1267-1271, 2005.
74. H. I. Jorgensen, K. Grove-Rasmussen, J. R. Hauptmann, and P. E. Lindelof, "Single wall carbon nanotube double quantum dot," *Applied Physics Letters*, vol. 89, p. 232113, 2006.

75. K. Grove-Rasmussen, H. I. Jorgensen, T. Hayashi, P. E. Lindelof, and T. Fujisawa, "A triple quantum dot in a single-wall carbon nanotube," *Nano Letters*, vol. 8, pp. 1055-1060, 2008.
76. G. A. Steele, G. Gotz, and L. P. Kouwenhoven, "Tunable few-electron double quantum dots and Klein tunnelling in ultraclean carbon nanotubes," *Nature Nanotechnology*, vol. 4, pp. 363-367, 2009.
77. D. S. Lee, S. J. Park, S. D. Park, Y. W. Park, M. Kemell, M. Ritala, et al., "Quantum dot manipulation in a single-walled carbon nanotube using a carbon nanotube gate," *Applied Physics Letters*, vol. 89, p. 233107, 2006.
78. H. Li and Q. Zhang, "Tunable ambipolar Coulomb blockade characteristics in carbon nanotubes—gated carbon nanotube field-effect transistors," *Applied Physics Letters*, vol. 94, p. 22101, 2009.
79. A. Javey, P. Qi, Q. Wang, and H. Dai, "Ten- to 50-nm-long quasi-ballistic carbon nanotube devices obtained without complex lithography," *Proceedings of the National Academy of Sciences of the United States of America*, vol. 101, pp. 13408-13410, 2004.
80. R. V. Seidel, A. P. Graham, J. Kretz, B. Rajaskharan, G. S. Duesberg, M. Liebau, et al., "Sub-20 nm short channel carbon nanotube transistors," *Nano Letters*, vol. 5, pp. 147-150, 2005.
81. Y. Ohno, Y. Asai, K. Maehashi, K. Inoue, and K. Matsumoto, "Room-temperature-operating carbon nanotube single-hole transistors with significantly small gate and tunnel capacitances," *Applied Physics Letters*, vol. 94, p. 53112, 2009.
82. S. Moriyama, T. Fuse, M. Suzuki, Y. Aoyagi, and K. Ishibashi, "Four-electron shell structures and an interacting two-electron system in carbon-nanotube quantum dots," *Physical Review Letters*, vol. 94, p. 186806, 2005.
83. S. Sapmaz, P. Jarillo-Herrero, J. Kong, C. Dekker, L. P. Kouwenhoven, and H. S. J. van der Zant, "Electronic excitation spectrum of metallic carbon nanotubes," *Physical Review B*, vol. 71, p. 153402, 2005.
84. J. Nygard, D. H. Cobden, and P. E. Lindelof, "Kondo physics in carbon nanotubes," *Nature*, vol. 408, pp. 342-346, 2000.
85. P. Jarillo-Herrero, S. Sapmaz, C. Dekker, L. P. Kouwenhoven, and H. S. J. van der Zant, "Electron-hole symmetry in a semiconducting carbon nanotube quantum dot," *Nature*, vol. 429, pp. 389-392, 2004.
86. L. Roschier, J. Penttila, M. Martin, P. Hakonen, M. Paalanen, U. Tapper, et al., "Single-electron transistor made of multiwalled carbon nanotube using scanning probe manipulation," *Applied Physics Letters*, vol. 75, pp. 728-730, 1999.
87. H. Li, Q. Zhang, and N. Marzani, "Unique carbon-nanotube field-effect transistors with asymmetric source and drain contacts," *Nano Letters*, vol. 8, pp. 64-68, 2008.
88. M. U. Kahaly, "Defect states in carbon nanotubes and related band structure engineering: a first-principles study," *Journal of Applied Physics*, vol. 105, p. 24312, 2009.
89. S. Berber, and A. Oshiyama, "Atomic and electronic structure of divacancies in carbon nanotubes," *Physical Review B*, vol. 77, p. 165405, 2008.
90. M. Igami, T. Nakanishi, and T. Ando, "Numerical study of transport in carbon nanotubes with lattice vacancy," *Journal of the Physical Society of Japanese*, vol. 68, pp. 3146-3149, 1999.
91. K. Matsumoto, S. Kinoshita, Y. Gotoh, K. Kurachi, T. Kamimura, M. Maeda, et al., "Single-electron transistor with ultra-high Coulomb energy of 5000 K using position controlled grown carbon nanotube as channel," *Japan Journal of Applied Physics*, vol. 42, pp. 2415-2418, 2003.
92. D. Tsuya, K. Ishibashi, M. Suzuki, and Y. Aoyagi, "Local Ar beam irradiation for making tunneling barriers and its application to single electron inverter in multi-wall carbon nanotubes," *Physica E*, vol. 19, pp. 157-160, 2003.

93. K. Ishibashi, M. Suzuki, D. Tsuya, and Y. Aoyagi, "Fabrication of single electron transistors in multi-wall carbon nanotubes using Ar beam irradiation," *Microelectronic Engineering*, vol. 67, pp. 749-754, 2003.
94. K. Maehashi, H. Ozaki, Y. Ohno, K. Inoue, K. Matsumoto, S. Seki, et al., "Formation of single quantum dot in single-walled carbon nanotube channel using focused-ion-beam technique," *Applied Physics Letters*, vol. 90, 23103, 2007.
95. J. Y. Park, Y. Yaish, M. Brink, S. Rosenblatt, and P. L. McEuen, "Electrical cutting and nicking of carbon nanotubes using an atomic force microscope," *Applied Physics Letters*, vol. 80, pp. 4446-4448, 2002.
96. C. K. Hyon, A. Kojima, T. Kamimura, M. Maeda, and K. Matsumoto, "Non contact atomic force microscope electrical manipulation of carbon nanotubes and its application to fabrication of a room temperature operating single electron transistor," *Japanese Journal of Applied Physics*, vol. 44, pp. 2056-2060, 2005.
97. C. K. Hyon, T. Kamimura, M. Maeda, and K. Matsumoto, "Island size control of carbon nanotube single electron transistor operating at room temperature by AFM electrical manipulation," *Proceedings of SPIE*, vol. 6127, p. 612716, 2006.
98. T. Kamimura, M. Maeda, K. Sakamoto, and K. Matsumoto, "Room-temperature single-hole transistors made using semiconductor carbon nanotube with artificial defects near carrier depletion region," *Japanese Journal of Applied Physics*, vol. 44, pp. 461-464, 2005.
99. M. Maeda, S. Iwasaki, T. Kamimura, K. Murata, and K. Matsumoto, "Room-temperature carbon nanotube single-electron transistor with defects introduced by $La(NO_3)_3$ process," *Japanese Journal of Applied Physics*, vol. 47, pp. 5724-5726, 2008.
100. S. Iwasaki, M. Maeda, T. Kamimura, K. Maehashi, Y. Ohno, and K. Matsumoto, "Room-temperature carbon nanotube single-electron transistors fabricated using defect-induced plasma process," *Japanese Journal of Applied Physics*, vol. 47, pp. 2036-2039, 2008.
101. H. Dai, " Carbon Nanotubes: Synthesis, Integration, and Properties," *Accounts of Chemical Research*, vol. 35, pp. 1035-1044, 2002.
102. B. H. Kim, T. H. Park, S. J. Baek, D. S. Lee, S. J. Park, J. S. Kim, et al., "N-type carbon nanotube by alkaline-earth metal Sr doping," *Journal of Applied Physics*, vol. 103, 96103, 2008.
103. X. Liu, Z. Luo, S. Han, T. Tang, D. Zhang, and C. Zhou, "Band engineering of carbon nanotube field-effect transistors via area chemical gating," *Applied Physics Letters*, vol. 86, p. 243501, 2005.
104. R. S. Lee, H. J. Kim, J. E. Fischer, A. Thess, and R. E. Smalley, "Conductivity enhancement in single-walled carbon nanotube bundles doped with K and Br," *Nature*, vol. 388, pp. 255-257, 1997.
105. J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, et al., "Nanotube molecular wires as chemical sensors," *Science*, vol. 287, pp. 622-625, 2000.
106. J. Kong, C. Zhou, E. Yenilmez, and H. Dai, "Alkaline metal-doped n-type semiconducting nanotubes as quantum dots," *Applied Physics Letters*, vol. 77, pp. 3977-3979, 2000.
107. J. Kong, J. Cao, H. Dai, and E. Anderson, "Chemical profiling of single nanotubes: Intramolecular p-n-p junctions and on-tube single-electron transistors," *Applied Physics Letters*, vol. 80, pp. 73-75, 2002.
108. C. Zhou, J. Kong, E. Yenilmez, and H. Dai, "Modulated chemical doping of individual carbon nanotubes," *Science*, vol. 290, pp. 1552-1555, 2000.
109. J. B. Cui, M. Burghard, and K. Kern, " Room temperature single electron transistor by local chemical modification of carbon nanotubes," *Nano Letters*, vol. 2, pp. 117-120, 2002.

This page intentionally left blank

CHAPTER 13

Individual Carbon Nanotubes as Electromechanical Actuators: Simulations and Initial Experiments

Tissaphern Mirfakhrai and John D. W. Madden

13.1 Introduction

The wish to shrink the size of electronic integrated circuits and to miniaturize mechanical machinery, which led to the development of microelectromechanical systems (MEMS), is now fuelling the creation of mechanical machines at the nanoscale. Submicrometer-scaled machines and actuators are envisioned to move single atoms and molecules and to create artificial nanostructures. Although nanowheels and other similar structures have been demonstrated, mechanical[1,2] manipulation and the lack of miniature actuators capable of controllably applying large forces at the nanoscale still pose major challenges. Moreover, artificial musclelike structures can potentially be made by assembling millions of these nanoactuators, thus expanding their capabilities to the macroscopic world. Carbon nanotube actuators have been demonstrated at the macroscopic scale through actuation of sheets and yarns composed of nanotubes. They show promise as nanoelectromechanical actuators and could help bring nanoelectromechanical machinery to reality.

In the sections that follow, we review studies performed on *carbon nanotube* (CNT) actuators. After presenting the background and potential for this type of nanoactuator, we review the work performed

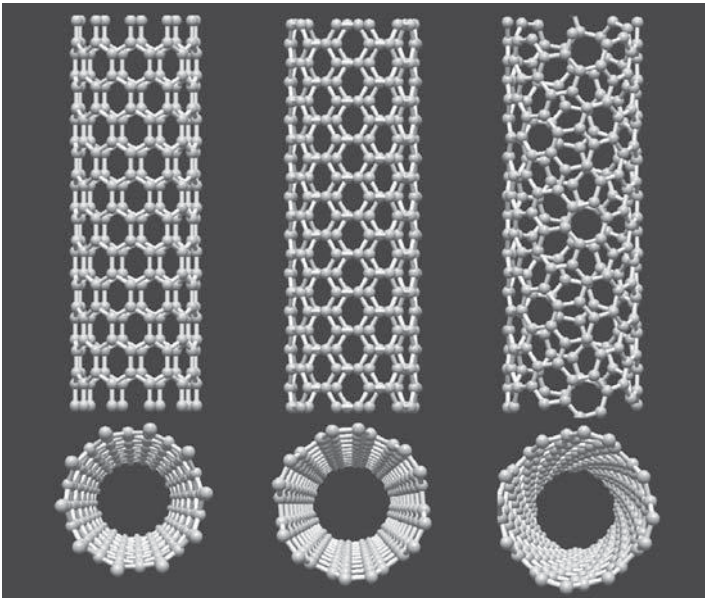


Figure 13.1 Example single-wall nanotubes. Although mechanical properties do not vary greatly with structure, armchair SWNTs (*B*) are always conducting or have very small bandgaps, but (*A*) zigzag and (*C*) chiral SWNTs can be conducting or semiconducting.

on actuation of individual CNTs. This chapter is divided into sections covering theoretical, simulation-based, and experimental investigations of actuators.

Carbon nanotubes can be thought of as sheets of graphene rolled into cylinders with nanometer diameters and lengths that have reached several millimeters.[3] *Single-walled nanotubes* (SWNTs) consist of one such rolled-up sheet, some examples of which are shown in Fig. 13.1. Since the discovery of CNTs in 1991, their electronic and mechanical properties have been studied extensively, both theoretically and experimentally. Simulations and experiments have shown that CNTs are very stiff for their diameter, having Young's moduli in the terapascal range,[4,5] and have tensile strengths of about 60 GPa,[6,7] far higher than in any bulk material. In comparison, the strongest commercially available steel wire has a tensile strength of around 5 GPa, and the strongest iron whiskers show a tensile strength of about 13 GPa.[8] It is also known that the electronic structure of CNTs depends greatly on their geometry (diameter and chirality), resulting in conducting and semiconducting CNTs of various bandgaps.[9]

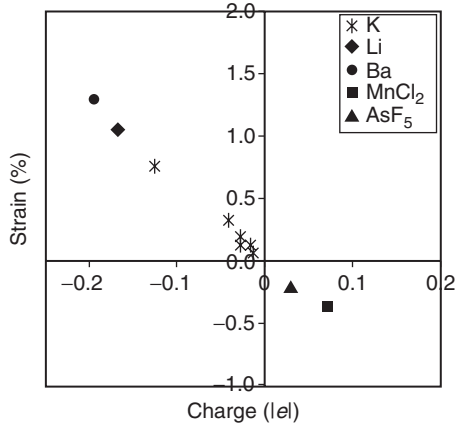


FIGURE 13.2 In-plane strain induced in graphite intercalation compounds as a function of charge per atom.[10,13–16] The points represent data obtained using various salts, as indicated.

It had been observed in the 1960s[10] that the C-C bond length in ion-intercalated graphite varies when the degree of charging of the constituent graphene sheets is changed (Fig. 13.2). Therefore, not long after the discovery of CNTs and because of the similarity of their structure to that of graphite, it was predicted that CNTs would actuate.[11] The first experimental results on actuation of CNT-based materials were published in 1999.[12] It was observed that a sheet of entangled CNTs ("Bucky paper") expands and contracts when the voltage applied to it is changed (Fig. 13.3). It has been speculated that this actuation in CNTs is again the result of C-C bond length changes.[12] In this case, the actuation was achieved by immersing the nanotube sheets in an electrolyte and charging the sheet. A double layer consisting of electronic charge in the nanotubes, and balancing ions in the solution, is formed at the nanotube-electrolyte interface. An alternative mechanism of charging involves the application of a voltage between the nanotube and adjacent electrodes. This method has been attempted in single nanotubes, as will be discussed later.

A rough approximation for the expected change in the C-C bond length can be found by considering the coulombic interactions between the partially charged carbon atoms. Electrostatic forces resulting from charging the CNTs promote expansion of the CNTs due to the repulsion between the like charges. Such expansion is a quadratic function of charge. Theoretical studies were performed to relate the change in C-C bond lengths to the charge level.[17,18] These studies predicted that upon being charged, the CNTs may expand or contract depending on the charge type and charge level and the chirality of the CNT.[19] As had been experimentally confirmed in graphite,[20,21] it was

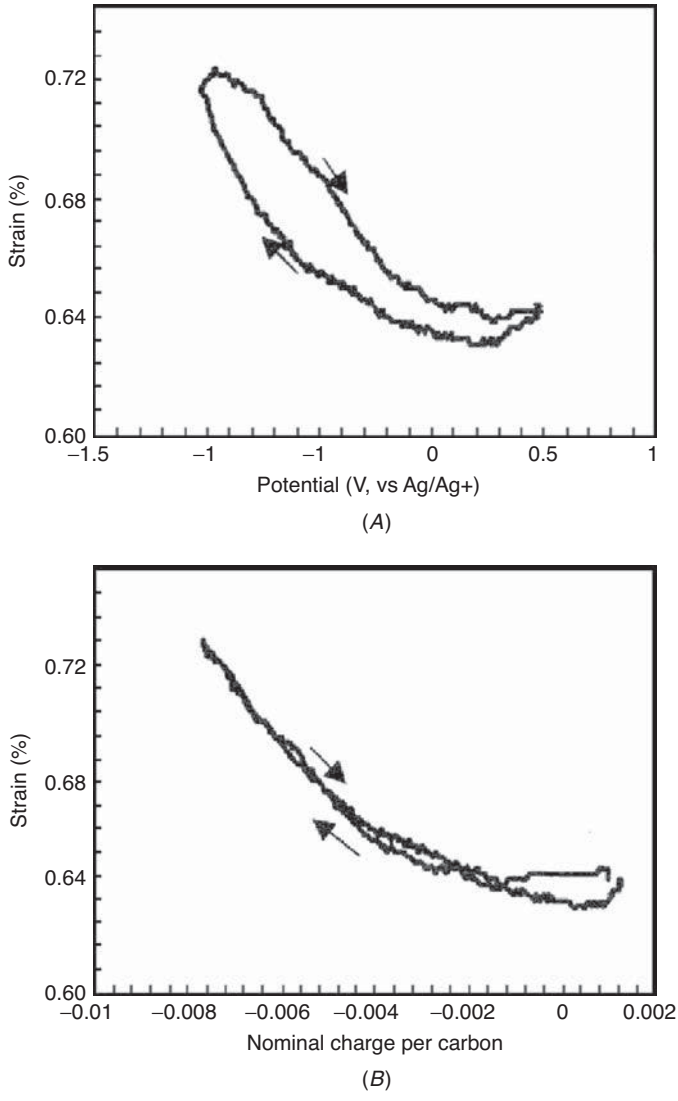


Figure 13.3 Actuation strain as a function of (*A*) applied working electrode potential and (*B*) nominal charge per carbon atom.[12]

shown that at small positive charge densities, the CNT can contract rather than expand, contrary to what is predicted by purely electrostatic considerations alone. Quantum-chemical effects, such as change of the bond order and of overlap, appear to have a significant influence on bond length as charging is varied.[18,22]

Meanwhile, the development of new macroscopic CNT structures such as fibers[23] and yarns[24] of CNTs enabled further experimental study of their actuation. At least some of these structures have been shown to contract[25,26] (e.g., Fig. 13.4*B* for a CNT yarn). This is unlike the expanson observed in sheets made of similar multi-walled CNT (Fig. 13.4*A*) [27]. Observations like these make it necessary to further investigate the mechanisms of actuation of individual CNTs. Such studies may help us understand the actuation of CNTs and pave the way for engineering applications. We now look at the measured and potential performance of carbon nanotube actuators based on their physical properties.

13.1.1 Performance and Promise of CNT Actuators

Most experimental results for macroscopic CNT actuators have been reported for CNT papers, sheets, yarns, and fibers[12,25,29,30] rather than for single nanotubes. As a result, we must infer the properties of individual nanotubes actuators from those of arrays of tubes, and from simulation results. In most of these macroscopic actuators, the charge is transferred to the CNT electrochemically, that is, by submersing the actuator in an electrolyte and applying a potential between the actuator and a counterelectrode. Ions move close to the CNT actuator surface, allowing for more charge to be stored in the CNTs than would be possible in air or vacuum. Actuation strains are typically measured under constant load, whereas actuation stresses reported are measured while the actuator length is kept constant.

In this chapter, the aim is to present and analyze what is known about single tubes. Although small bundles of tubes may also provide useful properties on the nanoscale, these are not considered here, partly because their actuation likely involves both inter- and intrachain mechanisms.

Nanotube electromechanical actuators function at a few volts, which is much more accessible in battery-powered devices than the 100 V used for piezoelectric stacks and the approximately 1,000 V used for electrostrictive actuators. The piezoelectric and electrostrictive actuators typically offer up to 0.2 to 0.3 percent actuation strain, which is smaller than the 0.5 percent CNT actuators currently attain. Nanotube actuators have been operated at temperatures up to 350°C, and operation above 1,000°C should be possible on the basis of SWNT thermal stability and industrial carbon electrode electrochemical application above this temperature (providing the actuators are sealed from oxygen[7]). Nanotube actuator strains can exceed 1 percent.[31] The maximum observed isometric actuator stress of SWNT actuators is presently 26 MPa.[7] This is about 10 times the stress initially reported for these actuators and about 100 times the stress-generation capability of natural muscle. Indeed, the SWNT's stress-generating

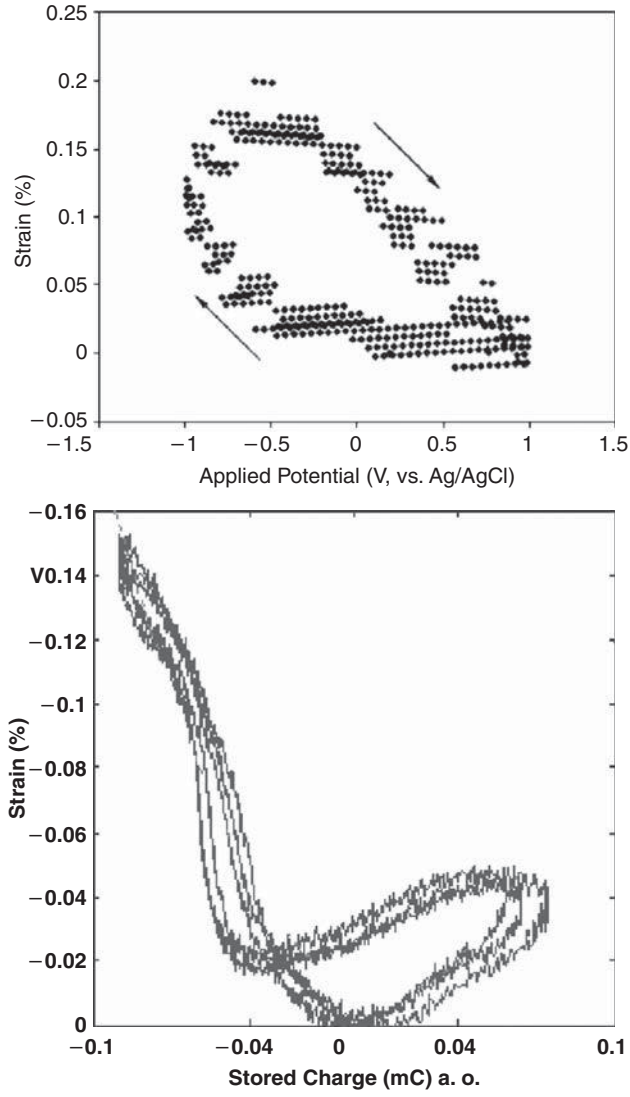


FIGURE 13.4 Actuation strains in (*A*) sheets and (*B*) twisted yarns of multiwalled CNTs from Refs. 27 and 28, respectively. Note that the strain in (*B*) is negative, which means that the actuator contracts upon charging. The horizontal charge axis in (*B*) has arbitrary origin (a. o.), because the initial charge of the actuator is not known.

ability approaches the stress-generation capability of high-modulus commercial ferroelectrics (about 40 MPa). However, these stress levels are still much lower than it is predicted should be achieved for individual nanotubes.[2] Multiwalled nanotubes have recently been shown to actuate in yarns at loads of 200 MPa, closer to the ultimate limit.[32] The maximum load and strength of macroscopic structures have so far been limited by the strength of interactions between nanotubes and their orientation relative to the axis to which stress is applied. Individual nanotube actuators should readily achieve much higher loads, provided they can be effectively attached to each other.

The achievable actuator strain is largely independent of applied load,[32] and hence, the work during isotonic (constant load) contraction linearly increases with load until the material fails. The only actuator technology that achieves significantly higher work densities than macroscopic nanotube actuators are shape memory alloys. Ultimately, carbon nanotube actuators may exceed the work densities even of shape memory alloys by at least an order of magnitude, if mechanical properties of individual tubes can be approached, and operate at stress levels in the gigapascal range. Furthermore, whereas some molecular motors have been shown to operate based on chemical principles, the possibility of electronic control of nanomechanical devices, available in electrochemically activated CNT actuators, could "greatly improve their effective switching times, control, and precision."[33]

The performance limits of nanotube-based actuators will best be seen in individual CNTs. A few experimental studies have focused on electrostatically driven mechanical responses of CNTs,[34,35] but experimental challenges make this work of uncertain value. However, simulations are able to make predictions as to the behavior of these actuators on charging. They show that mechanical response of CNTs can be driven not only by electrostatics, but also by quantum-mechanical effects. In the next section, we review various theoretical and simulation works on single CNT actuation.

13.2 Theoretical and Simulation Work

The aim of the theoretical and simulation work on CNT actuation is to find the change in the length or diameter of the CNT structure through computation. This length or diameter is influenced by the length of individual bonds within the CNT, as well as its interconnected structure. Usually, the initial coordinates of the atoms in the structure are estimated based on the geometry of the CNT of the desired chirality by computationally "rolling up" a sheet of graphene along the desired chiral vector. The CNT system is then allowed to "relax" by allowing the constituent atoms to move to reach a minimum in total energy. Excess charge is then added to the CNT structure. The lengths

of the bonds in the CNT change depending on the charge level and distribution around each bond, resulting in a change in the overall dimensions of the CNT. The dimensional change is usually studied as a function of the added charge, or added charge-per-atom.

The theoretical work involving bond-length change in carbon compounds dates back at least to the work of Pauling, who showed that the bond length in alkanes, alkenes, and alkynes with the same number of carbons follows a logarithmic relationship with the bond order (the number of electrons involved in a bond).[36] Further studies on graphite intercalation compounds in the 1950s and 1960s showed that as atoms are intercalated between graphene sheets, the carbon-carbon bond length depends on the degree of charge transfer from the intercalating atoms to the graphene.[10] Graphite intercalation compounds are formed by the insertion of atomic or molecular layers of a different chemical species called the intercalant between layers in a graphite host material. For example, when graphite is mixed with alkali metals, the metal atoms penetrate between the graphene sheets that form graphite, transferring negative charge to the neutral graphene sheets. Theoretical studies were performed to explain that change and relate it to the change in bond order produced by the charge transfer. During the 1960s and 1970s, Ruedenberg,[37] Kakitani,[38] and others refined the concept of bond order, but failed to come up with a universal relationship between the bond order and bond length. In 1981, Pietronero and Strässler[18] showed that electrostatic forces, along with changes in bond order, likely explain the bond length change observed in graphite intercalation compounds. Chan et al.[17] used first principle methods to relate the change in bond length in graphite intercalated compounds to degree of charge transfer, including both bond order and electrostatic forces. Finding a relationship between bond length and charge enables us to control actuation by controlling the amount of charge.

When actuation effects were observed in CNT materials, increasing attention was paid to applying the theoretical techniques, mentioned previously, to explain the actuation of CNTs. In this many-body system, numerical simulation techniques were applied to predict the behavior of CNTs. Because a CNT is essentially a single atomic layer at the nanoscale, atomistic methods are naturally more suitable to study the effects involved. Some continuum models have been employed to describe properties of CNTs with some level of success. However, these methods cannot capture all the effects that take place at the nanoscale. The most widely used atomistic techniques include *molecular dynamics* (MD), *tight binding* (TB), *Hartree-Fock* (HF) ab initio methods, and *density functional theory* (DFT). Various implementations of each of these techniques have been used to simulate electromechanical actuation in CNTs.

In systems such as CNTs, where numerous atoms interact to determine the properties of the overall system, higher accuracy in

computational methods usually comes at the price of longer computation times. The computation time usually increases with N^3 or N^4, depending on the method employed, where N is the number of particles simulated in the system.[39] Several computational approaches have emerged in the past 15 years that trade off accuracy and computation time. Methods such as *restricted Hartree-Fock* (RHF), *unrestricted Hartree-Fock* (UHF), and DFT are known to predict the system behavior quite accurately based on basic principles of physics, with the methods typically increasing in computational time in the order they are listed. Computational costs associated with them increase so rapidly when the systems are made large that simulating long lengths of CNTs with them is practically impossible using computing facilities in existence today. This means that only short lengths of CNTs (typically in the order of 1 nm) can be simulated using RHF, UHF, and DFT.

CNTs with longer lengths can be simulated using *periodic boundary conditions* (PBCs) with any of the foregoing methods. However, applying PBCs to a charged structure results in infinite total charge, which in common software packages makes the simulation impossible. This issue can be tackled by including a jellium, namely, a uniform distribution of charge of the opposite sign filling all space. This assumption is, of course, an approximation and may lead to artifacts and shortcomings. The simulation field in the foreseeable future thus remains a trade-off between level of accuracy and speed. In the sections that follow, we first briefly introduce relevant simulation techniques and then discuss some examples of their application to simulate actuation properties of CNTs.

13.2.1 Molecular Dynamic and Molecular Structural Mechanics Methods

Background

In classic MD methods, atoms are treated as particles in the classical sense and the interactions between them are modeled by force fields. The atoms in this arrangement resemble a group of balls with known masses, whereas the force fields between them are analogous to springs. The forces acting on the particles are computed. Using Newton's laws and based on those forces and the current positions of the particles, the direction of motion of a particle is found, and thus its new position after a given time interval. The temperature of the system is kept constant by scaling the velocities of the atoms every few steps. This adds a damping effect to the system without which it can be envisioned as a combination of masses and springs. These steps are repeated until the distances traveled by the particles in one step are smaller than a desired value, upon which the process is said to have converged.

The computation of wavefunctions in many-body systems is the most important challenge in atomistic simulation methods and greatly increases the computational cost. In MD, no wavefunction is calculated, and so this method is the cheapest in terms of computational resources needed, for example, to relax a CNT system and find its mechanical structure at its lowest energy state. This means that larger systems, such as longer CNTs, can be modeled using MD than are possible using other models with similar computational resources in comparable times. However, in some sense, MD is the least reliable among the atomistic methods, because instead of using the wavefunctions to minimize the system energy, the interactions between atoms are modeled using force fields defined by the user. Several empirical force fields have been developed to model the behavior of the carbon-carbon bond when neither atom carries electric charge.[40–42] These force fields add up the various classical forces applied to the atoms based on intuition. The parameters of such models are then determined based on the measured properties of hydrocarbon molecules.

Including excess charge in the simulations is fundamental in simulating electromechanical effects in CNTs. Attempts have also been made to include the charge in the force fields. However, those force fields are primarily empirical and developed assuming that certain conditions are invariably maintained during the cases under study; for example, no redistribution of charge among the atoms is usually allowed. In other words, unlike in quantum mechanical methods, where the system response is found based on physical principles, the results in MD are always limited by the assumptions that the user makes, which can potentially turn out to be unrealistic and do not allow for delocalization. When investigating novel systems such as CNTs, where few experimental data are available to support or refute the simulation results, methods involving empirical force fields should be used with care, and their results should not be accepted without considering the uncertainties involved. At the same time, force fields used for MD simulations can be modified and improved by incorporating effected adopted from ab initio results, thus allowing systems with larger number of atoms to be simulated.

Implementation Examples

A variation on MD technique is the molecular structural mechanics method.[43] Extensive techniques exist in the literature to compute the properties of solid structures. CNTs structurally resemble buildings made of steel bars (Figs. 13.5*A* and 13.5*B*); in fact, their class of materials (fullerenes) takes its name from an architect who designed geodesic domes using jointed bars. Each bar in such structures is described by its mechanical properties, that is, its tensile resistance, flexural rigidity, and torsional stiffness. Such properties can be assigned to each C-C bond in a CNT. Li and Chou[44] investigate the electromechanical

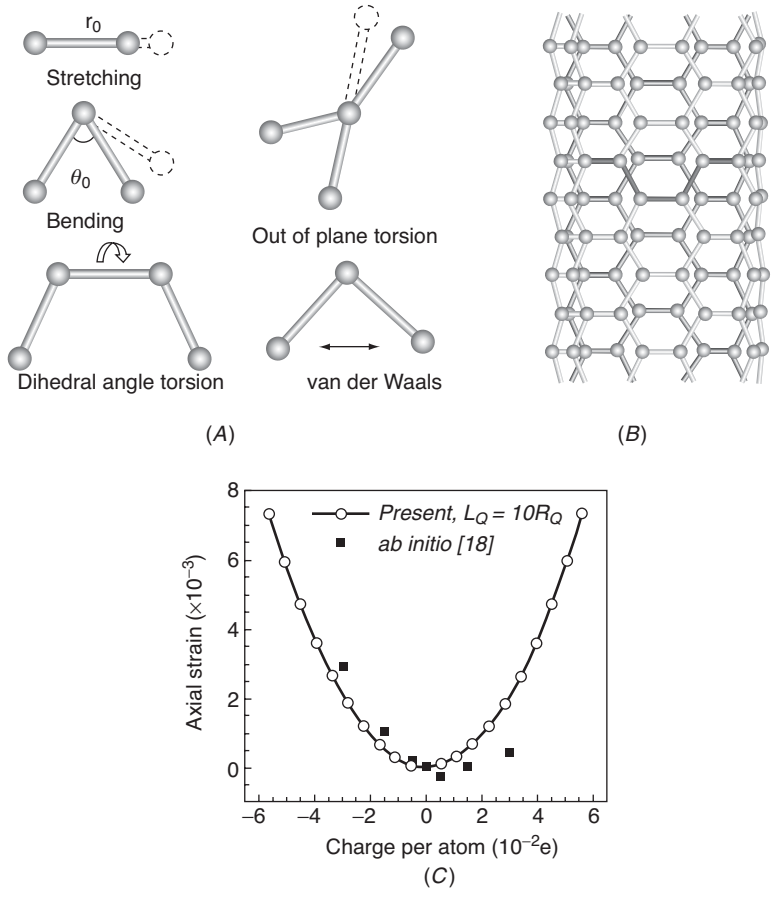


Figure 13.5 (*A*) Interatomic interactions in molecular mechanics in a CNT structure such as (*B*). (*C*) Simulated actuation strain as a function of charge, compared with results in Ref. 22.

coupling in single-walled carbon nanotubes using such structural mechanics methods. In the model system, the extra electric charge of the nanotube is assumed to be uniformly distributed on carbon atoms. The electrostatic interactions between charged carbon atoms are calculated using Coulomb's law. The deformation of the charged nanotube is obtained by using the molecular structural mechanics method and considering the electrostatic interactions as an external load acting on carbon atoms. The axial strain is found to be a symmetric function of applied charge, as seen in Fig. 13.5*C*, and the general trend in strain that is predicted is in good agreement with those of ab initio calculations,[18] also shown in Fig. 13.5*C*. The results indicate that the nanotube aspect ratio (length to diameter) has a strong effect on the

axial strain when this ratio is less than 10, and the general trend is that the strain increases with the aspect ratio in this range. The predicted peak axial and radial strains occur at nanotube diameters of around 1.2 to 1.5 nm.

Considering that most CNTs made include at least thousands of atoms, and the significant computational loads involved in simulating such large numbers of atoms with quantum levels of accuracy with present computational facilities, MD remains a promising option to simulate CNTs. It is therefore somewhat surprising that few papers employ MD techniques. One reason may be that electronic degrees of freedom are not typically implemented in MD application packages, and thus simulating charged structures remains difficult. Even in cases where charge can be added to the structure, a constant charge is typically pinned to each atom in the system, not allowing charge to redistribute as system dimensions change during actuation, and potentially leading to misleading results.

13.2.2 Tight-Binding Theory

Background

In the TB model for a solid-state lattice of atoms, it is assumed that the attractive potentials of the atomic nuclei are so dominant that the electrons are mostly bound to their ionic cores, with neighboring atoms providing only a minor perturbation to the electron orbits.[45] The full Hamiltonian, H, of the system may be approximated by the Hamiltonian of an isolated atom centered at each lattice point. The bound levels are assumed to be well localized, that is, atomic orbitals ψn, which are eigenfunctions of the single-atom Hamiltonian hat, are assumed to be very small at distances exceeding the lattice constant, such that electrons are "tightly" bound to nuclei. A solution to the time-independent single electron Schrödinger equation Φ is then assumed to be a *linear combination of atomic orbitals* (LCAO). Using an approximate form for the wavefunction, and assuming only the mth atomic energy level is important for the mth energy band, the Bloch energies can be calculated. The tight-binding model is typically used for calculations of electronic band structure but has been applied to look at mechanical deformation.

Implementation Examples

Gartstein et al.[19,46] use tight-binding theory to present a simple approach for using bond-stretching and bond-bending modes to describe the static deformations of carbon nanotubes and related actuation effects. They discuss gap energy modulation by external strains, dimensional and torsional deformations caused by charge injection, and stretch-induced torsion. They show how symmetry determines

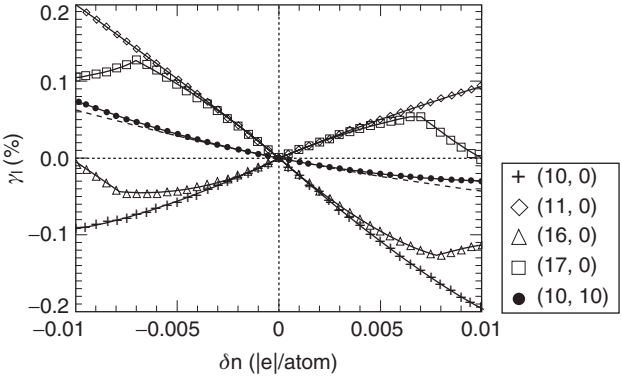


Figure 13.6 Axial strain for a series of SWNTs as a function of charge. The dashed line shows result for graphite.[19,46]

the property dependence on the chiral angle of nanotubes. The strong oscillatory dependence of these responses on the nanotube geometry is explained within an intuitively clear picture of bonding patterns. They show how anisotropic shear deformations play an important role in nanotubes, making their responses distinctly different from graphite's.

The results are surprising because they are markedly different from the response in graphite. They predict that a (10,0) and a (16,0) will show contraction upon both hole and electron injection and conversely, that a (11,0) and a (17,0) tube will expand for both signs of doping, as depicted in Fig. 13.6. Also, at a certain charge injection level the response appears to reverse for the (16,0) and (17,0) nanotubes. It should be noted that Coulombic effects, which are quadratic in their effect and certainly play the dominant role at large values of charge transfer, were not taken into consideration in these calculations.

Verissimo-Alves et al. employ the TB technique to justify why the minimum of the strain-charge curve can be located at a positive, nonzero value of charge (see Section 13.2.4 and Fig. 13.8*A*) in their own DFT simulations. They argue that the nearest-neighbor approximation, which implies that the Fermi level in a CNT is positioned between sigma energy levels and pi energy levels, is not accurate. They refine the accuracy by using next-nearest-neighbor approximation, showing that the Fermi level is in fact 1.6 eV into the pi states. Therefore, as electrons are removed from the CNT, they are first removed from antibonding states, resulting in a decrease in bond length. Eventually, as more electrons are removed, states below the Fermi level are depleted of their electrons, and the CNT starts to expand again. Thus, the reversal of the actuation direction happens after some electrons have been removed, and at a positive charge level.

13.2.3 Hartree-Fock Method

Background

The most commonly used method for calculating wavefunctions describing systems with many electrons is the Hartree-Fock (HF) method.[47] This is also an approximate method. The HF method finds the solution to Schrödinger's equation, as a function, known as the Slater determinant, that minimizes the total system energy.

Each of the electron orbitals in a molecule are typically described as a linear combination of orbitals for the individual isolated atoms (LCAO approximation), and the atomic orbitals, in turn, are represented as linear combinations of basis functions. Calculations of this sort are frequently referred to as ab initio calculations (meaning "from the beginning") because they do not rely on any experimental measurements on atoms or molecules.

The Hartree-Fock approximation underlies most common methods for calculating electron wavefunctions of atoms and molecules. The HF approximation is, furthermore, the usual starting point for more accurate calculations.

In closed-shell molecules, that is, where the number of electrons with spin up is equal to the number of electrons with spin down, each occupied molecular orbital contains two electrons, one spin up and the other spin down. This gives two orthogonal spin orbitals, but the spatial part (i.e., the x, y, z dependence) is the same, simplifying the calculation. This kind of calculation is called *restricted Hartree-Fock*. or RHF, calculation. When the number of spin-up electrons and spin-down electrons is not the same, an RHF calculation is not appropriate. Then, the spatial dependence of an orbital of a spin down electron will be different from the spatial dependence of a spin up electron, because two electrons with the same spin interact in a different way than two electrons with different spin. How does one determine if RHF is appropriate? One does it either by showing experimentally that the real system consists of closed shells, or by demonstrating that the ground state predicted by RHF is lower than that predicted by the general HF method.

Implementation Examples

Ghosh et al.[48] have performed ab initio restricted HF calculations of the electronic structure of a (5,5) single-walled nanotube in the presence of various ions. They show that the presence of ions near the nanotube causes combined axial and radial deformations of the nanotube. The presence of ions leads to a small charge transfer from the ions to the nanotubes as well as changes the p-p overlap energy. They find that the strains developed are primarily due to the electrostatic interactions with only a small contribution from the charge transfer.

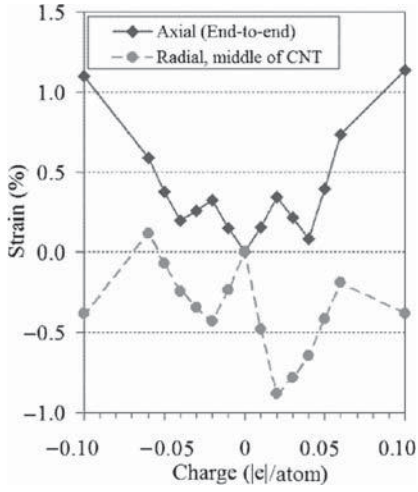
The work of Ghosh et al. is one of the few that considers the effect of ions on actuation strain. As discussed earlier, most experimentally demonstrated CNT actuators to date use ions in an electrolyte to balance the charge induced into the CNT for actuation. This enables the injection of considerably more charge into the CNT than would be possible in air or vacuum, and thus allows for larger strains. In modeling the effect of ions on actuation, Ghosh et al. allow the system, including the CNT and the ions, to relax, thus finding the distance that minimizes the system energy. They take this approach instead of relying on the data from literature for the typical distribution of distances between ions and the CNT surface. However, they do not account for the size of the solvation sphere or temperature. Their strain results are plotted later in Fig. 13.9*B*. The general actuation trend is similar to that predicted by other models, with a general parabolic response expected from the electrostatics. However, some other effects (including bond order) lead to a deviation from the predictions of other methods.

Unlike restricted HF, which assumes complete pairing of all electrons in the system (with possible exception of a last remaining electron if the total number of electrons is odd), the unrestricted HF method allows the system to have unpaired electrons in ground state. Whereas in most macroscopic systems, formation of wide bands may result in full pairing of all electrons, at nanoscale this is no longer a given, and molecular systems with non-singlet ground states are possible.[49] Therefore, this possibility should be studied for CNTs. UHF proves to be a useful tool for that purpose.

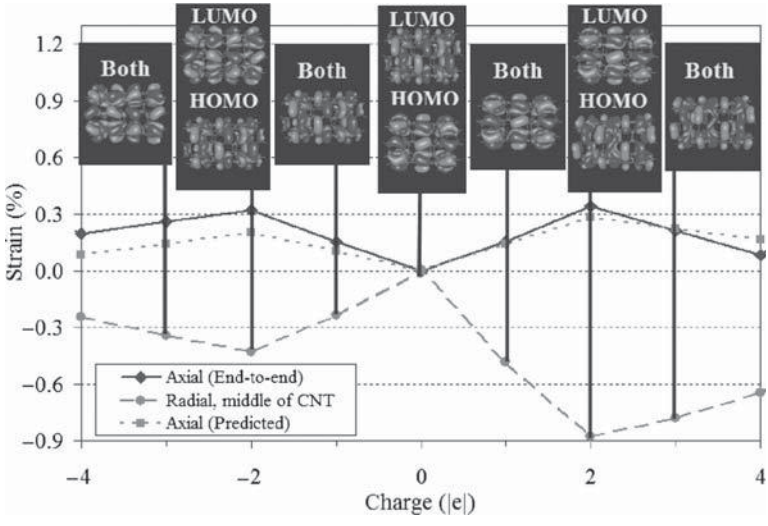
The authors of this chapter simulated the mechanical actuation of a (5,5) single-walled carbon nanotube as a result of added charge, using both the restricted and the unrestricted HF methods.[50] It is observed that whereas both positive and negative charging tend to expand the nanotube in the axial direction for most levels of charge, radial actuation is less even and symmetric with respect to charge (Fig. 13.7*A*). The spin distribution of the additional charges is also investigated, and it is predicted that in some cases unpaired spin configurations are energetically favorable and have a significant effect on actuation strains.

The work shows how bonds in CNTs may expand or contract, depending on their position within the CNT structure. This is unlike most simulations of CNT actuation that limit themselves to simulation of one unit cell of the CNT and apply periodic boundary conditions, or assume that the actuation would be uniform.

The origin of the "zigzag" response shown in Fig. 13.7 is surprisingly simple. It is shown that by injecting charge into a *molecular orbital* (MO), bonds aligned with the clouds corresponding to that orbital contract, in much the same way that a diatomic bonding molecular orbital contracts upon addition of electrons.[51] Meanwhile, bonds in the CNT with a nodal plane across them expand upon electron injection



(*A*)



(*B*)

Figure 13.7 (*A*) Axial and radial strain in a (5,5) SWNT as a function of added charge according to Ref. 50 and (*B*) a close-up of the middle part of (*A*) with the spatial distributions of HOMO and LUMO at each point superimposed.

into the corresponding orbital, thus behaving very similarly to the antibonding orbitals in a diatomic molecule. It is shown that the actuation strain in the CNT can be predicted with reasonable accuracy by looking at the spatial distribution of the molecular orbitals and by applying Pauling's rule to correspond the number of added

electrons to bond lengths. Figure 13.7*B* shows the strain as found by HF simulations and as predicted by the authors using Pauling's rule. The shortcoming of this method lies mostly in the fact that only CNTs with short lengths can be simulated using UHF at present. It is unclear whether or not the zigzag structure will be maintained in much longer tubes as energy differences between molecular orbitals shrink.

13.2.4 Density Functional Theory

Background

DFT is a method often used to simulate CNT structures. Traditional methods in electronic structure theory, and particularly the HF method, are based on complicated many-electron wavefunctions. In DFT, instead of the many-body electronic wavefunction, the total electron density is used as the basic quantity. An advantage of DFT is its relative simplicity. In a system including N electrons, the many-body wavefunction is a function of $3N$ variables (i.e., three spatial variables for each electron). Meanwhile, the density is a simpler quantity to deal with both conceptually and practically, because it is a function of only three variables.

The two Hohenberg-Kohn theorems constitute the basis of DFT.[52] The first theorem proposes that there is a one-to-one mapping between the ground-state electron density and the ground-state wavefunction of a many-particle system. The second theorem states that the total electronic energy of the system is minimized by this ground-state electron density. It should be noted that the Hohenberg-Kohn theorems only show the existence of a true total-energy density functional—it is left to the simulator to find its form.

The most widely used implementation of DFT is through the Kohn-Sham method (KS-DFT), which finds the solution to the system in terms of individual single-electron orbitals. The electron-electron interactions are taken into account through exchange correlation energy terms.

DFT has been very popular for calculations in solid-state physics since the 1970s. In many cases, DFT gives quite good agreement with experimental results for solid-state calculations, at relatively low computational costs when compared to other methods of solving the quantum-mechanical many-body problem. However, it was not considered accurate enough for calculations in quantum chemistry until the 1990s, when the approximations used in the theory were greatly refined to better model the exchange and correlation interactions.[53] DFT is now widely used to calculate electronic structure.

Implementation Examples

Verissimo-Alves and Capaz[22,54,55] performed DFT calculations of charged graphene and single-wall CNTs using the implementation

package SIESTA.[56] The simulated structures represent graphene, metallic CNTs including (5,5) and (12,0), and some semiconducting CNTs. A repeating unit cell of the crystal that contains several primitive cells (a supercell) is used. This technique facilitates the use of periodic boundary conditions. The CNT is given excess charge, and a "jellium" background charge ensures system neutrality. Without the jellium or some other method of balancing charge, total charge in the periodically repeating system tends to infinity, creating a configuration that cannot be simulated.

As seen in Fig. 13.8, both nanotubes and graphene are predicted to expand upon electron injection. On hole injection, metallic nanotubes and graphene display a nonmonotonic behavior. On increasing hole densities, the lattice constant initially contracts, reaches a minimum, and then starts to expand.

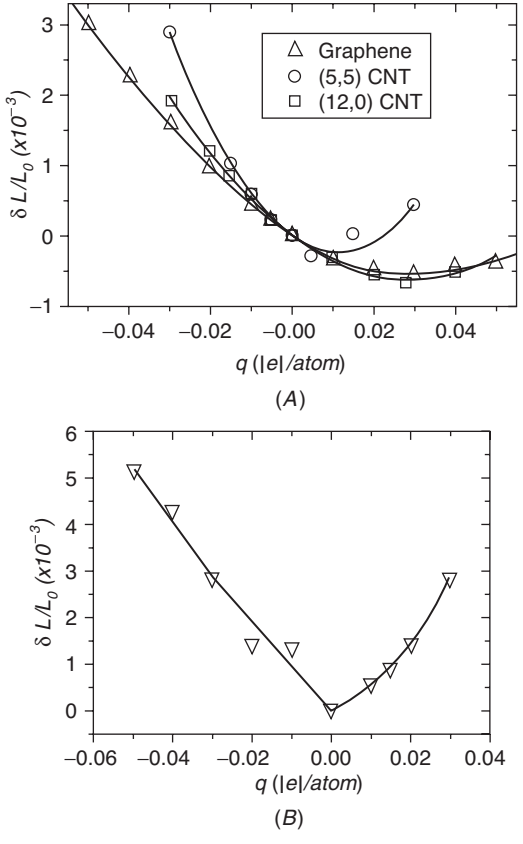


Figure 13.8 Actuation strains in (*A*) metallic and (*B*) semiconducting SWNTs as a function of charge, from Ref. 22.

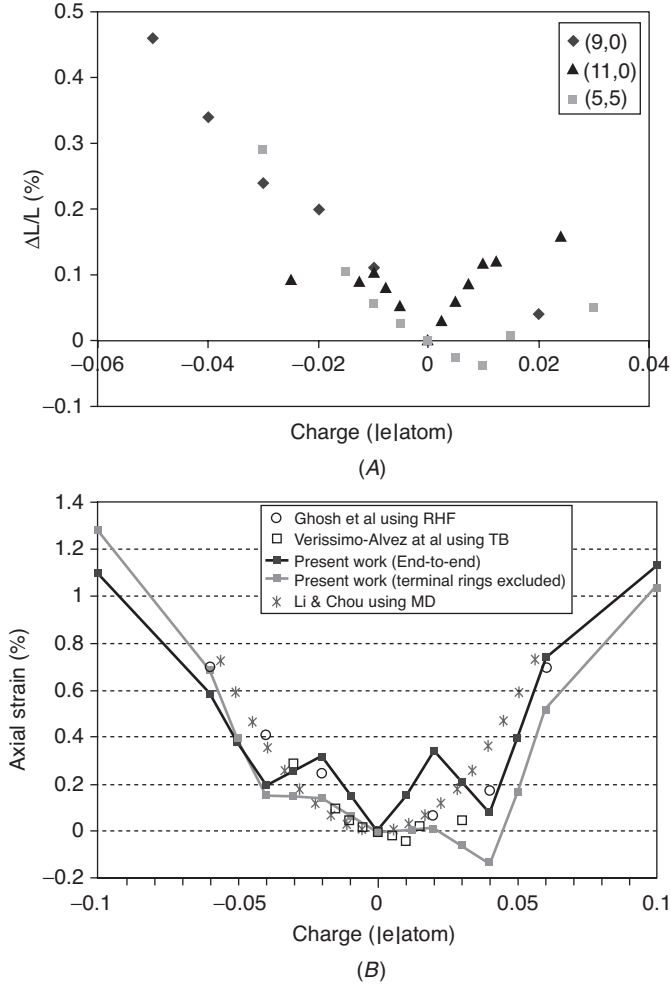


Figure 13.9 (*A*) Actuation strains from semiconducting (9,0), (11,0), and metallic (5,5) CNTs according to Ref. 55. (*B*) Comparison of the actuation results for a (5,5) CNT from papers as listed in the legend. "Present work" refers to Ref. 50.

The strain as a function of charge is shown in Fig. 13.9*A* for several CNT chiralities. An interesting effect is observed in the results: actuation strain seems to saturate in higher densities of hole injection.[55] A very similar effect takes place in actuation of macroscopic CNT actuators such as sheets and yarns.[12,25] If the macroscopic effect can be related to the saturation of actuation in individual CNTs, this can be used as a platform to quantitatively relate the actuation effects in the nanoscale to experimental observation in macroscale.

The hole densities at minimum lattice constants are 0.03 $|e|$/atom for graphene and between 0.01 and 0.03 $|e|$/atom for the metallic nanotubes studied. Semiconducting CNTs with small diameters ($d \leq 20$ Å) always expand upon hole injection. Semiconducting CNTs with large diameters ($d > 20$ Å) display a behavior intermediate between those of metallic and large-gap CNTs. Arguments based on the TB method (see TB section) are used to explain the fact that the minimum length of the CNT is achieved at a nonzero charge level. These arguments qualitatively agree with DFT results.

Sun et al. employ DFT to predict changes in nanotube length and diameter as a function of charge injection for armchair and zigzag nanotubes having different diameters.[21] Density functional theory with periodic boundary conditions is implemented using a common package known as VASP, which the authors show provides results consistent with experimental observations for intercalated graphite salts. Strain-vs.-charge relationships are predicted from dimensional changes calculated with a uniform background charge ("jellium") to represent the counterions. These jellium calculations are shown to be consistent with reported calculations that include specific counterions for intercalated graphite. The charge-to-strain relationships calculated with the jellium approximation for graphite and isolated single-walled nanotubes are asymmetric with respect to the sign of charge transfer. They show that the experimental and computed results match for graphite, and that the results from the jellium model generally agree with those computed using individual atoms.

The jellium model is then used to compute actuation strain in CNTs of various chiralities. The dependence of nanotube strain on charge approaches that for a graphite sheet for intermediate-sized metallic nanotubes and for larger diameter semiconducting nanotubes. However, the strain-charge curves depend on nanotube type when the nanotube diameter is small.

Although the results from Sun et al. match well with experimental data for graphene bond lengths, the rather linear actuation behavior they predict for most CNTs, as shown in Fig. 13.10, is surprising and inconsistent with other results. In conducting CNTs in particular, one would expect that at higher charge levels the CNT would act like a conducting needle and expand axially due to the coulomb force, unlike the contractile actuation predicted by Sun et al. at high positive charge levels. The fact that the jellium results match experimental data for graphite, while producing unexpected results for CNTs, may be because the jellium fills all space. The jellium fills the inside of the CNT as well as its outside, thus resulting in an unrealistic situation, as in general charge balance occurs on the outside of surfaces of nanotubes. Further studies are needed to determine whether the use of jellium in small-diameter nanotubes is appropriate.

As can be seen from the results just presented, there is no consensus among scholars about the actuation behavior of individual CNTs.

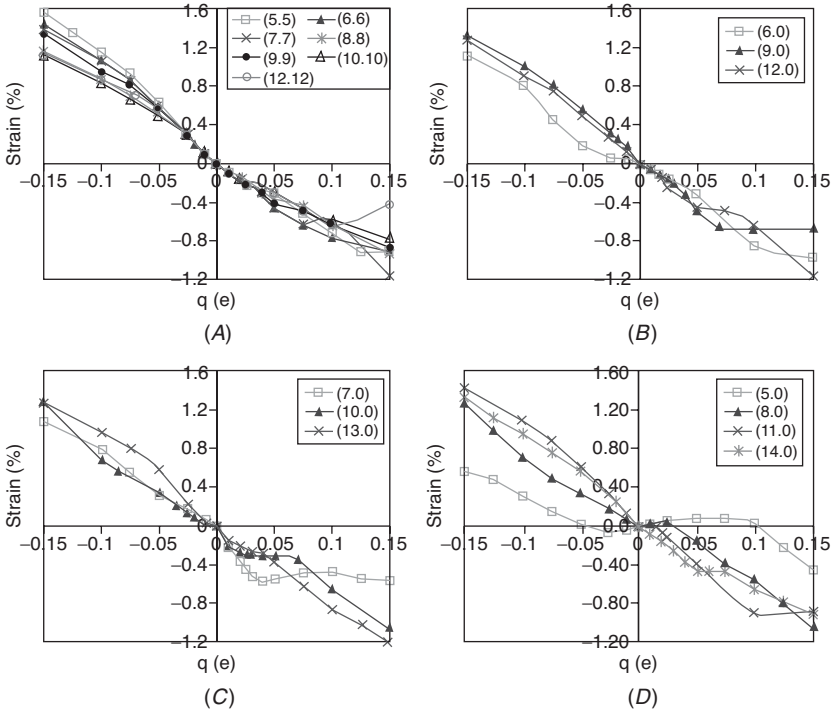


Figure 13.10 Strain as a function of charge for (*A*) (*n*, *n*) and three series of zigzag (*n*, 0) SWNTs: (*B*) $n = 3i$; (*C*) $n = 3i + 1$, and (*D*) $n = 3i + 2$, according to Ref. 21.

In fact, it is difficult even to compare various published simulation results. Not only does each technique have its own strong points and weaknesses (as discussed in this chapter), but also the structures that various groups have simulated and claimed to represent CNTs significantly differ from one another. Some of these methods include periodic boundary conditions, whereas others simulate relatively short structures.

The best simulation approach remains unclear and will have to await experimental confirmation. The experimental attempts at measuring the in-tube actuation of individual CNTs, and other experiments involving electromechanical actuation of nanoscopic CNT structures, are discussed in the following section.

Despite the differences in the predictions of simulations, they all suggest that significant strains can be achieved in carbon nanotubes on charging (between 0.2 and 2 percent). This level of strain is in the same range as has been reported for macroscopic CNT actuation of sheets and yarns. When combined with the high stiffness and tensile strength of nanotubes, the simulations are consistent with expectations of achieving unprecedented work densities from carbon

nanotubes. It is also clear that nanotubes will need to be relatively long compared to the displacement they generate (by 100 to 1000 times). Piezoelectric actuators, where strains are on the order of 0.1 percent, face a similar challenge, which is overcome by mechanical amplification, stepping, or simply using actuators that are long compared to the needed displacement.

13.3 Experimental Studies on Actuation in Individual Carbon Nanotubes

Several groups have sought to measure the actuation of individual CNTs due to the electromechanical effects expected to happen with a charged tube. Charging a CNT may also cause it to be attracted by Coulomb forces to other charged elements in its vicinity. This attractive force can result in bending a CNT, or sliding of shells of a MWNT on one another as a telescopic actuator. In fact, reported electromechanical effects due to such interaction between CNTs and their environment outnumber experimental observations that can be attributed to in-tube effects. In this section, we discuss some of the experiments that show electromechanical actuation of CNTs. An interesting experiment showing photoactuation in individual tubes is also presented.

13.3.1 Actuation Detection Using Atomic Force Microscopy

Roth and Baughman showed results suggesting the actuation of a single nanotube hanging like a bridge over a gap on a silicon substrate.[57] An AFM image of their experiment is shown in Fig. 13.11*A*. The CNT is shown hanging over a gap between two strips of gold on a Si/SiO_2 substrate. Electronic connection to the nanotube is made using an AFM probe. The substrate acts as the counterelectrode. Because there is only one nanotube, the experiment can be conducted in air or vacuum rather than having an electrolyte. When a square wave potential, as shown in Fig. 13.11*C*, is applied to the CNT using an AFM probe, the deflection in Fig. 13.11*B* is obtained, whose order general behavior is consistent with the theoretically predicted results. Moreover, the estimated strain in length is about 1 percent, which is again consistent with calculations in graphite and nanotubes. No measurement of the transferred charge is reported, and it is thus unknown at what charge levels has this strain been measured.

The interpretation of the curves in Fig. 13.11*C* as actuation of an individual CNT is uncertain. This is because it cannot be determined with absolute certainty whether this displacement of the AFM is due to the charging and the effects within CNT, or due to the electrostatic attraction between the charged CNT and some static charge accumulated nearby on the substrate. If such static charge is accumulated in the vicinity, the charged CNT, or even the cantilever itself, can be attracted to or repelled by the static charge depending on the potential

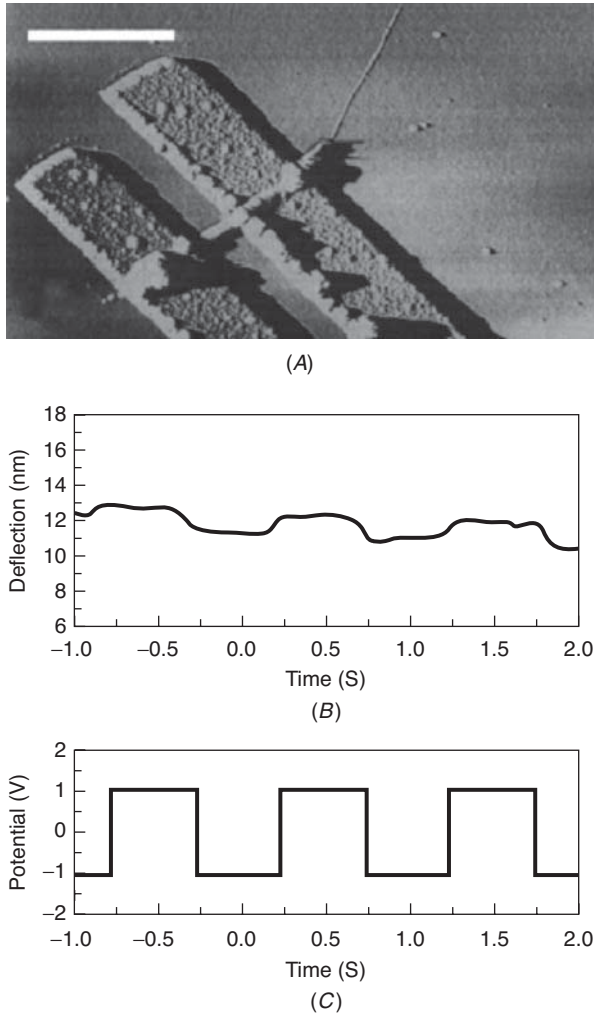


Figure 13.11 (*A*) The AFM image of a single CNT suspended between two gold strips on a Si/SiO_2 substrate (scale bar is 1 μm). (*B*) The AFM tip deflection signal and (*C*) the applied voltage between the cantilever and the substrate. From Ref. 57.

applied to the tip. Thus, a motion of the AFM cantilever is observed, which is correlated with the applied potential and cannot be easily differentiated from the presumed actuation due to changes within the CNT.

Sippel-Oakley[58] performed similar experiments at the single nanotube level to test the actuation mechanism in SWNTs. The experimental arrangement devised is illustrated in Fig. 13.12. Shown there is a nanotube suspended over a micromachined trench in a silicon

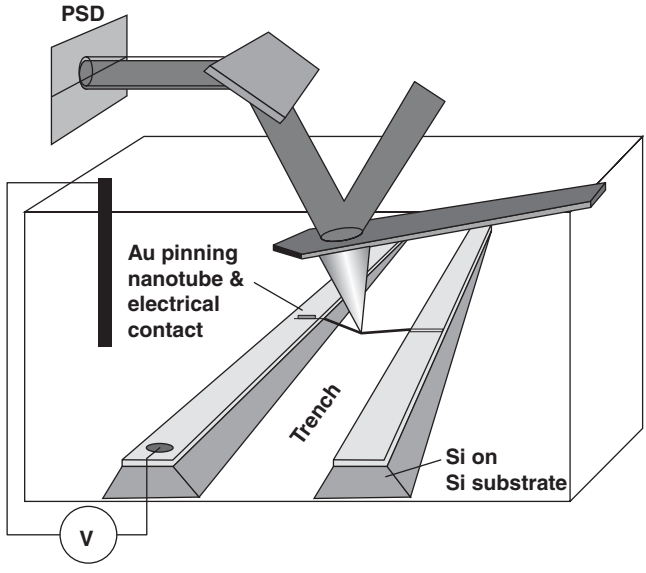


Figure 13.12 Schematic diagram of the experimental setup in Sippel-Oakley.[58]

substrate where the nanotube is pinned at its ends by metal electrodes. This experiment was performed in an electrolyte solution. Charge injection onto the nanotube occurred via a potential applied to the pinning electrodes vs. a counterelectrode in the electrolyte solution. To measure length changes, the suspended nanotube was pretensioned by a modest force applied at its center with the tip of an AFM cantilever. This deflected the center of the nanotube from the top of the trench while simultaneously deflecting the AFM cantilever from its set-point equilibrium position. If the nanotube lengthened, its center would deflect further into the trench to be detected by the corresponding relaxation of the AFM cantilever. If the nanotube is shortened, the tip would in contrast be forced upward, increasing the deflection of the cantilever from its set-point position.

Experiments were performed using 0.1 M to 1 M solutions of NaCl in water, $NaNO_3$ in water, $LiClO_4$ in acetonitrile, and $LiBF_4$ in acetonitrile, resulting in the subnanometer displacements seen in Fig. 13.13, corresponding to actuation strains of about 10^{-3} percent at potential between ± 0.75 V. This is more than two orders of magnitude smaller than the strain expected based on the theories by Baughman et al.[12]

Oakley suggests two factors to explain why charge-induced dimensional changes in these experiments are so small. First, the metals used in their fabrication processes are expected to p-dope the nanotubes, resulting in smaller dimensional changes (also, perhaps, the

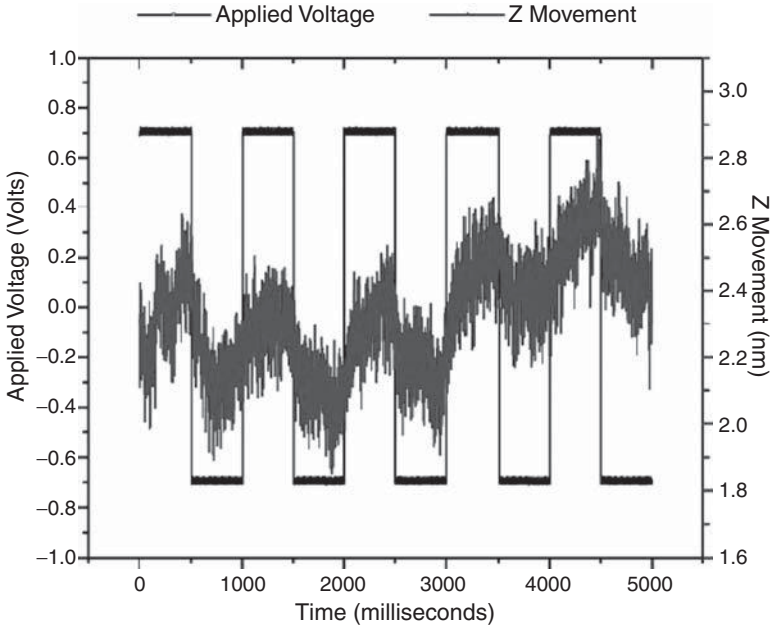


Figure 13.13 AFM signal from Sippel-Oakley[58] showing the observed actuation strain from an individual CNT.

nanotubes may be in the saturated regime seen in Fig. 13.9*A*). Additionally, there are contact barriers that prevent the injection of electrons onto the nanotubes. Because the transferred charge was not directly measured, only an estimate of the transferred charge can be obtained by theoretically estimating the capacitance of the CNT. Although the proposed mechanism may still be responsible for the results seen in the nanotube films, they conclude that the effect is too small to be consistently measured in individual nanotubes under the conditions achieved in Oakley's experiments.

13.3.2 Electrostatic and Optical Actuation

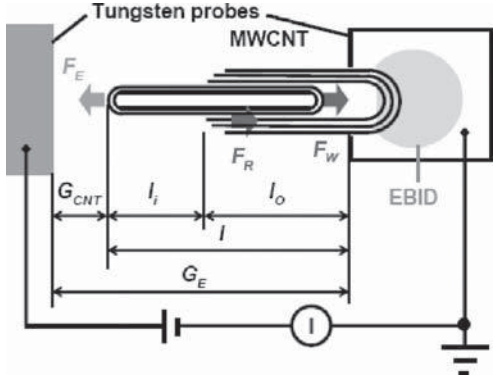
Electrostatic Actuation of Individual CNTs

A study of the electrostatic actuation in CNTs is described by Poncharal et al.[59] They use electrostatic attraction between a group of MWNTs and a counterelectrode to study the mechanical properties of CNTs, such as their modulus and bending stiffness. When a voltage between the nanotubes and a counterelectrode is varied periodically, the Coulomb force acting on the MWNT changes and makes them bend toward the counterelectrode. By changing the frequency of the applied voltage, the mechanical resonant frequency of the nanotube is found. They compare the bending behavior of a MWNT with

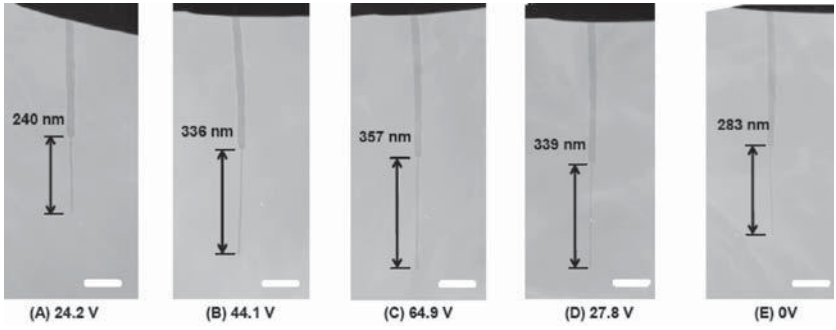
the expected behavior of a continuum-conducting cylindrical bar. They thus conclude that the CNT follows Hooke's law and that most of the charge on the CNT is stored near the tip. This is an example of electromechanical actuation not due to the effects within the CNT, but due to the electrostatic interactions between the CNT and another electrode.

Telescopic Actuation of Shells of a MWNT

Fukuda et al.[60] draw on the "telescopic" approach introduced by Cummings and Zettl[34] to actuate an MWNT using electrostatic forces. They make inner shells of an open-ended MWNT slide in and out because of the electrostatic attraction between the shells and a counterelectrode placed directly in front of the open end, as shown in Fig. 13.14. The other end of the MWNT is fixed on the substrate using electron-beam-induced deposition. On increasing the applied voltage, the inner nanotube shells slide out toward the counterelectrode.



(*A*)



(*B*)

Figure 13.14 (*A*) Schematic diagram of electrostatic actuation of telescopic MWNT. (*B*) Telescopic MWNT actuator at each applied voltage (scale bar: 100 nm).[61]

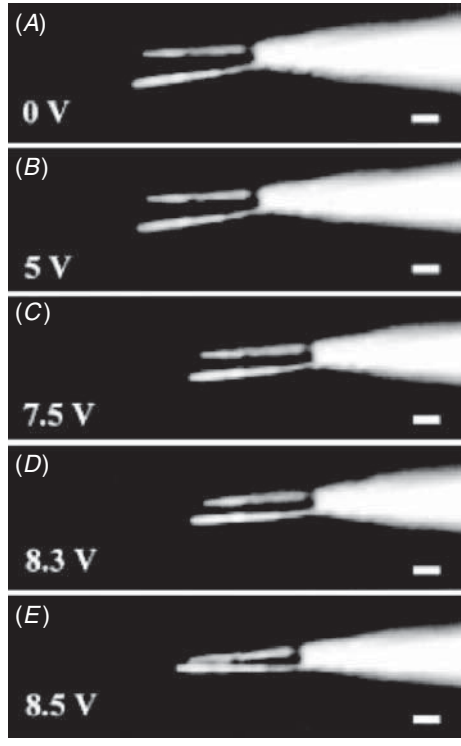


Figure 13.15 The actuation response of CNT nanotweezers at various applied voltages. Scale bar is 1 μm.[35]

The sliding resistance is reported to be quite small. This is expected, because the friction between nanotube shells is expected to be small, much like the friction between graphene layers in graphite—a well-known lubricant.[62] Once the voltage is switched back to 0 V, the inner shells return inward, probably due to attractive van der Waals forces.

One exciting aspect of this approach is that the electron emission current between the tip of the moving shells and the counterelectrode can be used as a measure of actuation strain, because the field emission current increases as the distance between the tip of the shell and the electrode is decreased. Based on the TEM images (Fig. 13.14), the actuation is not fully reversible.

Kim and Lieber use electrostatic driven bending of tubes to create what they call CNT nanotweezers.[35] They use the electrostatic attraction between two CNTs, to which opposite voltages are applied, to induce bending. The electrostatic attraction force bends the two CNTs toward each other, closing the tweezers (Fig. 13.15). The CNTs used have lengths of about 5 μm with diameters of about 50 nm. With such nanotweezers, they manage to grab and move objects as small as

500 nm in diameter. The tweezers can also be used as electrodes to probe electrical properties of the nanoobjects.

Electromechanical actuation induced by electrostatic forces between structures has advantages and disadvantages. Although deflection is typically larger and easier to create, it is necessary to apply a voltage to a nearby object to induce actuation. The creation of a nearby counterelectrode may not always be feasible. Manipulation of subcellular structures has been mentioned as one possible application of such nanomanipulators.[35] This application is interesting provided the electrostatically active portion of the tweezers can be modified so that it is not in contact with water. The electrostatic bending approach in general has the advantage of producing large deflections, but at much lower forces than are expected when charging is used to contract and expand the nanotube along its length.

Optomechanical Actuation of CNTs

A related effect is reported by Zhang and Iijima, where macroscopic movements of SWNT bundles are reported when illuminated with visible light, as shown in Fig. 13.16. The light-induced elastic effect is independent of the wavelength and polarity of the light source, as long as it is in the visible range. The degree of the deformation is, however, dependent on the intensity of the illumination.

Light-induced electrical current are detected in the filaments aligned between two metal electrodes. Therefore, Zhang and Iijima attribute the light-induced actuation to the electrical currents induced in the carbon nanotube filaments due to the light. (The photon pressure effect is excluded based on expected magnitude and direction.) The mechanism for the observed phenomenon is discussed by considering the physical interlinks of the optical, thermal, electrical, and elastic effects of nanotube bundles.[63]

13.4 Conclusions and Future Directions

Electromechanical and actuation properties of individual CNTs can open new doors toward nanoscale manipulation. Although a number of works have been published on both theoretical aspects and experimental observations, there is currently no universal model that can be used to explain and predict all the observed electromechanical effects. Simulations of CNT actuation are inconsistent in a number of respects, but they do show that a significant strain can be achieved on charging. On this basis, and given the extremely high strength and stiffness of carbon nanotubes, it is clear that CNT actuators will be capable of unprecedented performance, particularly in stress and work density.

Challenges remain, both in the implementation of single nanotube actuators and in their effective modeling. On the simulation side, the means of dealing with charge balance and the finite size available to

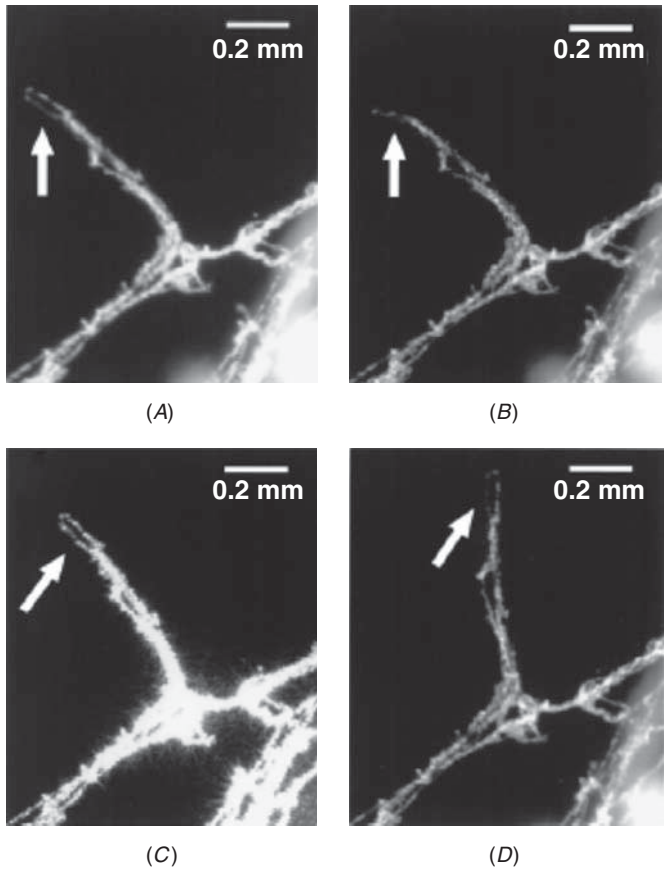


Figure 13.16 The actuation of a SWNT bundle under (*A*) strong light and (*B*) weak illumination from a halogen lamp light source. (*C*) Illumination by a He-Ne laser gives the same result as (*A*). (*D*) The same filament in an electrical field also gave a similar tip shape. The different orientation of the filament in (*D*) is because the SWNT bundle tends to align along the electrical field. The white arrows in all photographs indicate the filament tip of interest.[63]

models because of computational restrictions are two key limitations. On the experimental side, it is still a challenge to unambiguously measure the displacements of such small systems. However, this research has led to observing many interesting electromechanical effects due to the interaction of the charged CNT with its environment. These interactions can induce large displacements and bending in the CNTs. As discussed, such effects can be deployed to create nanomanipulators based on CNTs that can be used to manipulate objects at the micro- and nanoscale to create the building blocks of tomorrow's nanomachines.

When extremely large forces are needed, perhaps in the breaking of bonds or the indentation of surfaces, linear nanotube actuators present a means of producing these in a compact package.

References

1. J. F. Morin, Y. Shirai, and J. M. Tour, "En route to a motorized nanocar," *Organic Letters*, vol. 8, pp. 1713-1716, 2006.
2. S. H. Chanteau and J. M. Tour, "Synthesis of anthropomorphic molecules: the NanoPutians," *Journal of Organic Chemistry*, vol. 68, pp. 8750-8766, 2003.
3. T. Yamada, T. Namai, K. Hata, D. N. Futaba, K. Mizuno, J. Fan, et al., "Size-selective growth of double-walled carbon nanotube forests from engineered iron catalysts," *Nature Nanotechnology*, vol. 1, pp. 131-136, 2006.
4. T. T. Liu and X. Wang, "Dynamic elastic modulus of single-walled carbon nanotubes in different thermal environments," *Physics Letters A*, vol. 365, pp. 144-148, 2006.
5. X. B. Dai, H. Merlitz, and C. X. Wu, "Transverse elasticity of multi-walled carbon nanotubes," *The European Physical Journal B—Condensed Matter and Complex Systems*, vol. 54, pp. 109-112, 2006.
6. F. Li, H. M. Cheng, S. Bai, G. Su, and M. S. Dresselhaus, "Tensile strength of single-walled carbon nanotubes directly measured from their macroscopic ropes," *Applied Physics Letters*, vol. 77, pp. 3161-3163, 2000.
7. R. H. Baughman, A. A. Zakhidov, and W. A. de Heer, "Carbon nanotubes—the route toward applications," *Science*, vol. 297, pp. 787-792, 2002.
8. H. Tashiro, "The challenge for maximum tensile strength steel cord," *Nippon Steel*, vol. 80, July 1999.
9. P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon nanotube electronics," *Proceedings of the IEEE*, vol. 91, pp. 1772-1784, 2003.
10. D. E. Nixon and G. S. Parry, "The expansion of the carbon-carbon bond length in potassium graphites," *Journal of Physics C: Solid State Physics*, p. 1732, 1969.
11. R. H. Baughman, "Conducting polymer artificial muscles," *Synthetic Metals*, vol. 78, pp. 339-353, 1996.
12. R. H. Baughman, C. X. Cui, A. A. Zakhidov, Z. Iqbal, J. N. Barisci, G. M. Spinks, et al., "Carbon nanotube actuators," *Science*, vol. 284, pp. 1340-1344, 1999.
13. M. E. Preil, J. E. Fischer, S. B. Dicenzo, and G. K. Wertheim, *Physical Review B*, vol. 30, p. 3536, 1984.
14. J. E. Fischer, H. J. Kim, and V. B. Cajipe, "Neutron-diffraction studies of BaC6: c-axis compressibility, carbon–carbon bond length, and charge transfer," *Physical Review B*, vol. 36, p. 4449, 1987.
15. F. Baron, S. Flandrois, C. Hauw, and J. Gaultier, "Charge transfer and isolands in metal halides-graphite intercalation compounds: new evidence from x-ray diffraction of intercalated Mn Cl2," *Journal of Solid State Communications*, vol. 42, p. 759, 1982.
16. R. S. Markiewicz, J. S. Kasper, and V. Interrante, "Single crystal structure studies of C16AsF5," *Synthetic Metal*, vol. 2, p. 363, 1980.
17. C. T. Chan, W. A. Kamitakahara, K. M. Hoand, and P. C. Eklund, "Charge-transfer effects in graphite intercalates: ab initio calculations and neutron-diffraction experiment," *Physical Review Letters*, vol. 58, pp. 1528-1531, 1987.
18. L. Pietronero and S. Strässler, "Bond-length change as a tool to determine charge transfer and electron-phonon coupling in graphite intercalation compounds " *Physical Review Letters*, vol. 47, pp. 593-596, 1981.
19. Y. N. Gartstein, A. A. Zakhidov, and R. H. Baughman, "Mechanical and electromechanical coupling in carbon nanotube distortions," *Physical Review B*, vol. 68, p. 115415-1-11, 2003.
20. M. S. Dresselhaus and G. Dresselhaus, "Intercalation compounds of graphite," *Advances in Physics*, vol. 30, pp. 139-326.

21. G. Sun, J. Kurti, M. Kertesz, and R. H. Baughman, "Dimensional changes as a function of charge injection in single-walled carbon nanotubes," *Journal of the American Chemical Society*, vol. 124, pp. 15076-15080, 2002.
22. M. Verissimo-Alves, B. Koiller, H. Chacham, and R. B. Capaz, "Electromechanical effects in carbon nanotubes: ab initio and analytical tight-binding calculations," *Physical Review B*, vol. 67, p. 161401, 2003.
23. B. Vigolo, A. Penicaud, C. Coulon, C. Sauder, R. Pailler, C. Journet, et al., "Macroscopic fibers and ribbons of oriented carbon nanotubes," *Science*, vol. 290, pp. 1331-1334, 2000.
24. M. Zhang, K. R. Atkinson, and R. H. Baughman, "Multifunctional carbon nanotube yarns by downsizing an ancient technology," *Science*, vol. 306, pp. 1358-1361, 2004.
25. T. Mirfakhrai, J. Oh, M. Kozlov, E. C. W. Fok, M. Zhang, S. Fang, et al., "Electrochemical actuation of carbon nanotube yarns," *Smart Materials and Structures*, vol. 16, p. S243, 2007.
26. M. E. Kozlov, J. Oh, V. Seker, E. Kozlov, M. Zhang, S. Fang, et al., "Electromechanical actuation of carbon nanotube yarns, sheets and composites," paper presented at Materials Research Society fall meeting, 2005.
27. M. Hughes and G. M. Spinks, "Multiwalled carbon-nanotube actuators," *Advanced Materials*, vol. 17, pp. 443-446, 2005.
28. T. Mirfakhrai, M. Kozlov, M. Zhang, S. Fang, R. H. Baughman, and J. D. W. Madden, "Capacitive charging and background processes in carbon nanotube yarn actuators," *Proceedings of SPIE Smart Materials and Structures/NDE*, vol. 6524, 65241H1-12, 2007.
29. A. E. Aliev, J. Oh, M. E. Kozlov, A. A. Kuznetsov, S. Fang, A. F. Fonseca, et al., "Giant stroke, superelastic carbon nanotube aerogel muscles," *Science*, vol. 323, pp. 1575-1578, 2009.
30. M. Lucas, B. Vigolo, S. Badaire, D. L. Bolloc'h, A. Marucci, D. Durand, et al., "Alignment of carbon nanotubes in macroscopic fibers," in *Structural and Electronic Properties of Molecular Nanostructures*, H. K. e. al., Ed., 2002.
31. R. H. Baughman, unpublished results, 2009.
32. T. Mirfakhrai, "Carbon nanotube yarn actuators," PhD thesis, 2009, Electrical and Computer Engineering, University of British Columbia, Vancouver.
33. L. Forro, "Nanotechnology: Beyond Gedanken Experiments," *Science*, vol. 289, pp. 560-561, 2000.
34. J. Cummings and A. Zettl, "Low-friction nanoscale linear bearing realized from multiwall carbon nanotubes," *Science*, vol. 289, pp. 602-604, 2000.
35. P. Kim and C. M. Lieber, "Nanotube nanotweezers," *Science*, vol. 286, pp. 2148-2150, 1999.
36. L. Pauling, "Atomic radii and interatomic distances in metals," *Journal of the American Chemical Society*, vol. 69, pp. 542-553, 1947.
37. K. Ruedenberg, "The physical nature of the chemical bond," *Reviews of Modern Physics*, vol. 34, pp. 326-376, 1962.
38. T. Kakitani, "Theoretical study of optical absorption curves of molecules. III: Force constant and bond-bond interaction in conjugated molecules," *Progress of Theoretical Physics*, vol. 51, pp. 656-673, 1974.
39. A. Szabó and N. S. Ostlund, *Modern Quantum Chemistry: Introduction to Advanced Electronic Structure Theory*, Courier Dover, 1996.
40. D. W. Brenner, "Empirical potential for hydrocarbons for use in simulating the chemical vapor deposition of diamond films," *Physical Review B*, vol. 42, p. 9458, 1990.
41. D. G. Pettifor and I. I. Oleinik, "Analytic bond-order potentials beyond Tersoff-Brenner. I. Theory," *Physical Review B*, vol. 59, pp. 8487-8499, 1999.
42. D. G. Pettifor and I. I. Oleinik, "Bounded analytic bond-order potentials for r and p bonds. ," *Physical Review Letters*, vol. 84, pp. 4124-4127, 2000.
43. C. Li and T.-W. Chou, "A structural mechanics approach for the analysis of carbon nanotubes," *International Journal of Solids and Structures (2003)*, vol. 40, pp. 2487-2499, 2003.

44. C.-Y. Li and T.-W. Chou, "Charge-induced strains in single-walled carbon nanotubes," *Nanotechnology*, vol. 17, pp. 4624-4628, 2006.
45. J. Singleton, *Band Theory and Electronic Properties of Solids*, Oxford, UK, Oxford University Press, 2001.
46. Y. N. Gartstein, A. A. Zakhidov, and R. H. Baughman, "Charge-induced anisotropic distortions of semiconducting and metallic carbon nanotubes," *Physical Review Letters*, vol. 89, p. 045503-1, 4, 2002.
47. P. Echenique and J. L. Alonso, "A mathematical and computational review of Hartree-Fock SCF methods in quantum chemistry," *Molecular Physics*, vol. 105, pp. 3057-3098, 2007.
48. S. Ghosh, V. Gadagkar, and A. K. Sood, "Strains induced in carbon nanotubes due to the presence of ions: ab initio restricted Hartree–Fock calculations " *Chemical Physics Letters* vol. 406, pp. 10-14, 2005.
49. D. H. Cobden, M. Bockrath, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, "Spin splitting and even-odd effects in carbon nanotubes," *Physical Review Letters*, vol. 81, pp. 681-684, 1998.
50. T. Mirfakhrai, R. Krishna-Prasad, A. Nojeh, and J. D. W. Madden, "Electromechanical actuation of single-walled carbon nanotubes: an ab initio study," *Nanotechnology*, vol. 19, p. 315706, 2008.
51. T. Mirfakhrai, R. Krishna-Prasad, A. Nojeh, and J. D. W. Madden, "Bond order effects in electromechanical actuation of armchair single-walled carbon nanotubes," *Journal of Chemical Physics,* vol. 132(7), pp. 074703-1, 074703-6, 2010.
52. P. Hohenberg and W. Kohn, "Inhomogeneous electron gas," *Physical Review*, vol. 136, pp. B864-B871, 1964.
53. A. Gonis, *Theoretical Materials Science: Tracing the Electronic Origins of Materials Behavior*, Materials Research Society, 2000.
54. M. Verissimo-Alves, R. B. Capaz, B. Koiller, E. Artacho, and H. Chacham, "Polarons in carbon nanotubes," *Physical Review Letters*, vol. 86, p. 3372, 2001.
55. M. Verissimo-Alves, R. B. Capaz, B. Koiller, E. Artacho, and H. Chacham, "Ab initio studies of electromechanical effects in carbon nanotubes," *Brazilian Journal of Physics*, vol. 32, pp. 427-429, 2001.
56. A. Lopez-Bezanilla, F. Triozon, S. Latil, X. Blase, S. Roche, F. Triozon, et al., "Effect of the chemical functionalization on charge transport in carbon nanotubes at the mesoscopic scale," *Nano Letters*, vol. 9, pp. 940-944, 2009.
57. S. Roth and R. H. Baughman, "Actuators of individual carbon nanotubes,"*Current Applied Physics*, vol. 2(4), pp. 311-314, 2002.
58. J. A. Sippel-Oakley, "Charge induced actuation in carbon nanotubes," PhD thesis, University of Florida, 2005.
59. P. Poncharal, Z. L. Wang, D. Ugarte, and W. A. de Heer, "Electrostatic deflections and electromechanical resonances of carbon nanotubes," *Science*, vol. 283, pp. 1513-1516, 1999.
60. T. Fukuda, M. Nakajima, P. Liu, and M. R. Ahmad, "TEMs and SEMs focus on hybrid nanorobotic manipulation for carbon nanotube applications," *IEEE Nanotechnology Magazine*, vol. 2, pp. 19-31, 2008.
61. M. Nakajima, F. Arai, H. Matsuura, S. Arai, and T. Fukuda, "Electrostatic actuation of telescoping carbon nanotubes inside TEM," paper presented at 2005 5th IEEE Conference on Nanotechnology, Nagoya, Japan, 2005.
62. B. Bhushan and X. Ling, "Adhesion and friction between individual carbon nanotubes measured using force-versus-distance curves in atomic force microscopy," *Physical Review B*, vol. 78, p. 045429, 2008.
63. Y. Zhang and S. Iijima, "Elastic response of carbon nanotube bundles to visible light," *Physical Review Letters*, vol. 82, pp. 3472-3475, 1999.

CHAPTER 14

Low-Level Electrical Measurements at the Nanoscale

Jonathan Tucker

14.1 Introduction

Nanotechnology has the potential to improve our quality of life in diverse ways, such as faster electronics, huge memory/storage capacities for PCs, cheaper energy through more efficient energy conversion, and improved security through the development of nanoscale bio- and chemical-detection systems. Before these can become commercial realities, researchers must be able to characterize nanomaterial and nanodevice properties quickly and accurately.

Optical and electro-optical characterization techniques, such as *scanning electron microscopy* (SEM), emission microscopy, atomic force microscopy, and ultraviolet microscopy, provide valuable information on nanostructures. However, electrical characterization is essential to gain insight into phenomena that occur beneath the surface of nanomaterials. For example, gate dielectrics in advanced semiconductors can have a physical thickness of less than 1 nm; the performance of these dielectrics can only be predicted by evaluating their equivalent electrical thickness. Similar considerations apply to carbon nanotubes,

silicon wires, and graphene, which are the basis for many nano innovations.

The essence of nanotechnology research is to work at the molecular level, atom by atom, to create structures with fundamentally new properties. Some of the current research involves:

- Carbon nanotube enhanced materials and electronic devices
- Semiconducting nanowires of silicon and other materials
- Polymer nanofibers and nanowires
- Nano and molecular electronics
- Single-electron devices
- Graphene-based electronics

One of the main challenges in electrical characterization of these materials and structures is dealing with ultralow signal levels. Another challenge is the wide range of behavior that these materials and components can exhibit. For example, polymer materials can have resistances greater than 1 GΩ. However, when drawn into fibers less than 100 nm in diameter and doped with various nanoparticles, a polymer may be changed from a superb insulator into a highly conductive wire. The result is an extremely wide range of test signals. Detecting tiny electrical signals at the low end of the range requires high-sensitivity, high-resolution instruments such as electrometers, picoammeters, and nanovoltmeters. Also, using one of these instruments for high-level signals as well demands an instrument with a very wide dynamic range.

14.2 Nanotechnology Testing Overview

14.2.1 Emerging Challenges of Nanotech Testing

With nanoelectronic materials, sensitive electrical measurement tools are essential. They provide the data needed to understand the electrical properties of new materials fully and the electrical performance of new nanoelectronic devices and components. Instrument sensitivity must be much higher because electrical currents are much lower and many nanoscale materials exhibit significantly improved properties, such as conductivity. The magnitude of measured currents may be in the femtoamp range and resistances as low as microohms. Therefore, measurement techniques and instruments must minimize noise and other sources of error that might interfere with the signal.

An equally important, if often overlooked, factor is that research tools and instruments must be easy to use and cost-effective. The importance of these characteristics will grow as industry employment

grows. Some of the present tools are unnecessarily complex, with too many buttons on front displays that confuse users and make the learning curve steeper. Data transfer mechanisms are often tedious and can require extensive amounts of storage media. Spending hours just to program instruments steals from valuable research time. Those individuals who must make the hard choices about equipment investments should examine these issues carefully and compare instrument features before committing funds.

Besides the electrical measurement components of nanoscale research, there are many other difficulties when testing at the nanoscale level. For instance, it is incredibly complex to probe down to the device level for failure analysis and other testing. This requires new testing equipment, probers, and new nanotech measurement standards.

14.2.2 Electrical Properties at the Nanoscale and Measurement Considerations

In some respects, the testing of bulk materials and those created with nanotechnology is similar. However, the nature of nanotech materials requires some novel testing techniques. Because these materials are built at the atomic or molecular level, quantum mechanics comes into play. As a result of small particle sizes, the atoms and molecules of these new materials may bond differently than they might otherwise in bulk substances. There may be new electronic structures, crystalline shapes, and material behavior. Nanoparticles with these new properties can be used individually or as building blocks for bulk material. Although the discovery of bulk properties remains important, measurements also need to uncover the characteristics unique to nanoscale structures.

Particle size and structure have a major influence on the type of measurement technique used to investigate a material. Two important sets of properties change as particle sizes are reduced to nanometer dimensions, that is, the material's chemical and electrical characteristics. This even applies to biological materials. Therefore, most of these materials require chemical and electrical testing to characterize them for practical product applications. For many of them, the actual quantity being measured is a low-level current or voltage that was translated from another physical quantity.[1] Direct electrical measurements are possible on many baroscopic substances with the probing instruments and nanomanipulators now available.

As a substance is reduced to nanoscopic dimensions, both the bandgap and the distance between adjacent energy levels within the material's electron energy bands are altered. These changes, along with a particle's nanoscopic size with respect to the material's mean free path (average distance an electron travels between scattering events), directly affect the electrical resistance of a nanoparticle. More

generally, a material's bandgap directly influences whether a particle is a conductor, an insulator, or a semiconductor. These influential electronic properties allow, for example, a *carbon nanotube* (CNT) to be used to create a transistor switch.[2] One way to do this is by connecting a semiconducting CNT between two electrodes that function as a drain and source. A third electrode (the gate) is placed directly under the entire length of the carbon nanotube channel. For a semiconducting CNT, the introduction of an electric field through the channel (via the insulated gate placed in proximity to the CNT channel) can be used to change the CNT from its semiconducting state to its insulating state by increasing the gate voltage. Decreasing the gate voltage will transition the device into a conducting state. This conduction mechanism is analogous to the operation of a silicon *metal-oxide-semiconductor field-effect transistor* (MOSFET) transistor switch, which is created by doping silicon with either an electron acceptor or donor to alter the material's electronic conductivity in specific localities.

For macroscopic particles, electrons take on discrete quanta of energy that lie within energy bands, with each band consisting of many energy levels that electrons can share through their thermal energies. For a conducting material, electrons can be thermally excited into the conduction band (i.e., electrons are present in the valence as well as in the conduction band). For an insulator (bandgap greater than thermal energy of the electron), enormous energy is required for an electron to transition from the valence to the conduction band separated by the material bandgap. If a suitable amount of energy is absorbed (greater than the bandgap), then electrons can jump bands.

As a particle's size is reduced to nanoscopic dimensions, the allowable energies within the continuous bands separate into discrete levels (because there are far fewer atoms in the mix). This occurs when the separation between energy levels approaches the thermal energy of the electrons. See Fig. 14.1. With fewer energy levels within the specific energy band, the density of states of the material changes.

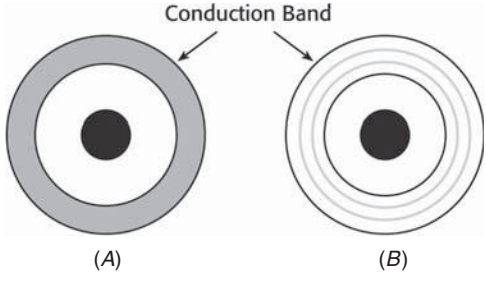


Figure 14.1 As material is reduced from macroscopic dimensions to nanoscopic size, its continuous energy bands (*A*) separate into discrete energy levels within the band (*B*) and the bandgap increases.

The density of states is a measure of the number of energy options available to an electron as it falls into a lower energy level by giving up energy or as it ascends to a higher energy level after absorbing energy. A corollary is that if the density of states is known, the size of the particle can be deduced.

Characterizing the density of states is a fundamental activity in nanoscopic material research. Density of states (3D dimensionality) as a function of energy can be expressed as

$$\rho(E) = dn_s/dE = [\{4\pi(2m)^{3/2}\}/h^3][\sqrt{(E)}]$$

This represents the number of electron states per unit volume per unit energy at energy E, where:

m = the effective mass of the particle
h = Planck's constant
E = the energy (electron orbital location) in electron volts

Although the result is independent of volume (can be applied to any size particle), this equation is of limited value if the particle size/structure is unknown. However, there are other ways to determine the density of states experimentally from which the particle size can be found.

Because the density of states can be used to predict the electrical behavior of materials, it is also possible to use electrical impedance measurements to derive density-of-states information. The density of states is found by plotting differential conductance vs. applied voltage. Differential conductance is simply (di/dv). When this conductance is plotted against voltage, the graph indicates the material's density of states. Highly conductive materials possess an abundance of free energy levels in the conduction band, that is, greater density of states (more individual allowed energy levels per unit energy). Insulating materials have an electronic structure with a dearth of occupied energy levels in the conduction band. Because density of states corresponds to the density of these energy levels, a plot of conduction vs. voltage provides a direct measure of the electronic density of states at each energy level (voltage across the device).

An approach to this technique is to use a nanomanipulator that makes low-resistance contacts to the nanoparticle. Such an arrangement allows charge transport and density-of-states measurements. This works well into the conduction region thanks to the low-resistance direct connections of the nanoprobes on the material (particle) being tested.

The nanomanipulator and its probes, along with a *source-measure unit* (SMU), are used to apply a current or voltage stimulus directly to the nanoparticle and measure its corresponding voltage or current

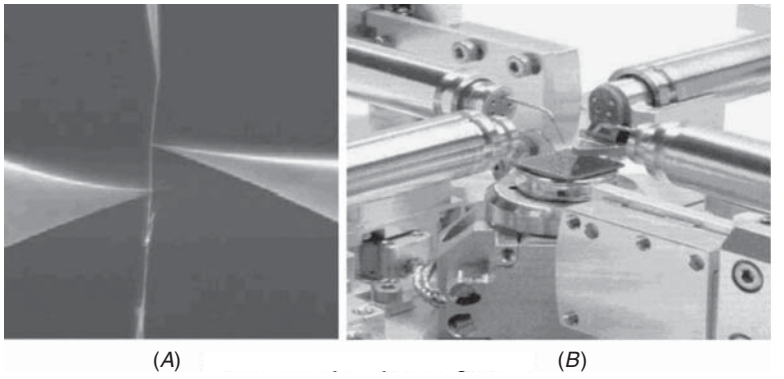


Figure 14.2 Nanomanipulator probing of nanoscale structures. (*A*) Microscopic view of low-impedance probe contact to a CNT for direct electrical measurements. (*B*) Photo of a nanomanipulator head assembly. Photos courtesy of Zyvex Corporation.

response. (See Fig. 14.2.) The advantage of electrical source-measure testing is rooted in the fact that a specific SMU measurement mode (source current/measure voltage or vice versa) can be chosen based on the relative impedance of the material or *device under test* (DUT). Furthermore, the measurement mode can change dynamically as the impedance changes, such as occurs in CNTs acting as semiconductor switches. This allows a much wider dynamic range of voltage and current stimuli and measurements, thereby optimizing parametric test precision and accuracy. SMU voltage and current sensitivity can be as good as 1 μV and 100 aA.

Electrical measurements on nanoscopic materials place stringent requirements on the instrumentation. In order to measure conductivity, impedance, or other electrical properties and relate those measurements to the density of states, a galvanic connection must be made to the nanoscopic DUT.[3] This represents one of the major hurdles to be overcome in the field of nanotechnology testing. There are only a few tools available and few device constructs that facilitate connections of this type.

Particle self-assembly can be accomplished from silicon to silicon, where conventional photolithographic techniques are used to make electrical connection pads for probing. Particles that are long enough to straddle such pads (e.g., carbon nanowires) can be connected to the pads through externally generated electrostatic fields.

Although the properties of quantum wells, wires, and dots differ, it's possible that information about a particular material in the form of a quantum dot can be inferred by examining the same material fashioned as a quantum wire or well (nanofilm). Nanofilms are particularly easy to measure because only one dimension is small. Such a film might be deposited on a conductive substrate, allowing

measurements through the volume as well as over the surface, using appropriately placed macroscopic test pads formed on the material surface. For conductive materials, separate pads for source and measure can be deposited to create a Kelvin (four-wire) connection.[4] This type of circuit eliminates test lead resistance from the measurement and improves accuracy. In any case, a quantum well (nanofilm) can be tested like any other bulk material.

Electrical Measurement Considerations

Electrical measurements on passive devices (any device that is not a source of energy) are made by following a simple procedure: stimulate the sample in some way and measure its response to the stimulus. This method also works for devices that have both passive and active properties with linear or nonlinear transfer functions. With appropriate techniques, a source-measure algorithm can be useful for characterizing sources of energy.

For nanoscopic particles, this general method takes the form of source-measure testing to quantify impedance, conductance, and resistance, which reveal critical material properties. This test methodology is useful even if the end application is not an electronic circuit.

General Considerations

Important considerations in the characterization of nanoscopic particles include the following:

1. Nanoscopic particles will not support the magnitude of currents that macroscopic device can carry (unless they are superconducting). This means that when a device is interrogated, the magnitude of a current stimulus must be carefully controlled.
2. Nanoscopic particles will not hold off as much voltage from adjacent devices as a conventional electronic component or material (such as a transistor). This is because smaller devices can be and are placed closer together. Smaller devices have less mass, and they may be affected by the forces associated with large fields. In addition, internal electric fields associated with nanoscopic particles can be very high, requiring careful attention to applied voltages.
3. Because nanoscopic devices are small, they typically have lower parasitic (stray) inductance and capacitance. This is especially useful when they are used in an electronic circuit, enabling faster switching speeds and lower power consumption than comparable macroscopic devices. However, this also means that instrumentation for characterizing their I-V curves must measure low currents while tracking the short reaction time.

Speed, Sensitivity, and Accuracy

Because nanoscopic test applications often require low-current sourcing and measurement, appropriate instrument selection and use are critical for accurate electrical characterization. Besides being highly sensitive, the instrumentation must have a short response time (sometimes referred to as high bandwidth), which is related to a DUT's low capacitance and ability to change state rapidly at low currents.

Measurement Topology

It is important to recognize that the switching speed of a source-measure test circuit may be limited by the instrumentation used to follow the state of the device. This is especially true if a nonoptimal measurement topology is used to observe the device. The two possible topologies are source current/measure voltage or source voltage/measure current.

When considering the measurement of low-impedance devices (less than 1000 Ω), the source current/measure voltage technique will generally yield the best results. Current sources are stable when applied to lower impedances, and a good signal-to-noise ratio can be achieved without great difficulty. This allows accurate low-voltage response measurements.

The alternative, source voltage/measure current, is not as well suited for low impedances. Exceptionally low values of applied voltage are required to keep device currents low and avoid destructive heating. At such low voltages, the source tends to contribute excessive noise to the measured current (response). In other words, the source's noise voltage is a significant percentage of the total applied voltage. Additionally, voltage sources are less stable with low-impedance loads. There may also be current measurement problems related to an instrument's voltage burden (the voltage that develops across the input of an ammeter circuit), which introduces additional error.

When measuring high-impedance devices (impedance greater than 10,000 Ω), the source voltage/measure current technique is best. Stable voltage sources to drive high impedances are easily constructed. When a well-designed voltage source is placed across a high impedance, it will quickly charge the stray capacitance of the DUT and test cables and rapidly settle to its final output value. The small current response of the DUT can be accurately measured with an appropriate ammeter.

The alternative, source current/measure voltage, creates problems in high-impedance measurements. To keep the voltage response low enough for practical measurements, this technique requires a low current value. This means that it will take a great deal of time to charge the device and cable capacitances. In addition, the high-voltage measurement circuits will draw some of the source current from the DUT.

Because the current is sourced, not measured, through the device, this current draw represents an error in the measurement.

Electrical Noise

Measurement topology also has an impact on electrical noise, which is the ultimate limitation on measurement sensitivity and accuracy. For low-impedance voltage measurements with a current source, the measurement circuits will be sensitive to DUT voltage noise and impedance.

For macroscopic devices, such as a resistor, the Johnson noise voltage at room temperature (270 K) is expressed as

$$V_{\mathrm{n}} = \sqrt{(4kTBR)}$$

where

k = Boltzmann's constant
T = Absolute temperature of the source in kelvins
B = Noise bandwidth in hertz
R = Resistance of the source in ohms

which can be further simplified to

$$V_{\mathrm{n}} = 6.5 \times 10^{-10}\sqrt{(BR)}$$

This equation shows that as DUT resistance R decreases, the Johnson voltage noise generated by the DUT also goes down. Conversely, high-impedance devices stimulated with a voltage source are limited by current measurement noise. The Johnson current noise of a resistor at 270 K is

$$I_{\mathrm{n}} = 6.5 \times 10^{-10}[\sqrt{(BR)}]/R$$

indicating that the noise goes down as DUT resistance increases.

For all particle sizes, in addition to Johnson noise, there could be a noise gain associated with the measurement topology chosen. Noise gain is a parasitic amplification of the noise of the measurement system that is not present when the correct measurement topology is chosen. For example, consider a source voltage/measure current topology. An operational amplifier (or op-amp) is used in many current measurement (ammeter) circuits, as shown in Fig. 14.3.

To minimize noise gain, the ammeter circuit must operate at a low gain with respect to its noninverting input terminal.

Source-Measure Instruments

A commercial dc SMU is a convenient test tool for many nanoscopic material and device measurements. SMUs change measurement topology automatically (i.e., rapidly switch between source voltage/

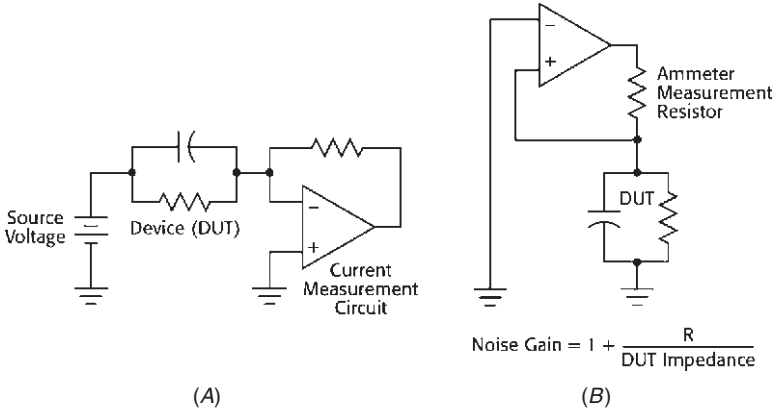


FIGURE 14.3 (*A*) Circuit model for the source voltage/measure current technique. (*B*) Modified model illustrating the noise gain (op-amp noise "gained up") when the DUT impedance is low compared to the measurement impedance.

measure current and vice versa). This makes it easier to minimize measurement noise while maximizing measurement speed and accuracy.

As described earlier for a carbon nanotube, some nanoparticles can change state with the application of an external field. When investigating such materials, an SMU can be configured to source voltage and measure current for a nanoparticle in its high-impedance state. When the material is in its low-impedance state, more accurate results are achieved by sourcing current and measuring voltage. Furthermore, the SMU has a current compliance function that can automatically limit the dc current level to prevent damage to the material or device under test. Similarly, there is a voltage compliance function when current is being sourced.

When using the compliance function, an SMU will satisfy the source value unless the user's compliance value is exceeded. For example, when an SMU is configured to source voltage with a preset current compliance, if that compliance value is exceeded, the SMU automatically starts acting as a constant current source. Its output level then will be the compliance current value. Alternately, if the SMU is set to source current with a compliance voltage, it will automatically switch to sourcing voltage (the compliance voltage) if the DUT impedance and the current it draws begin to drive the voltage higher than the compliance value.

Although a nanoscopic device, such as a CNT switch, can change states rapidly, the change in instrument state is not instantaneous. Depending on the SMU model, the switching time can range from 100 ns to 100 μs. Although such switching speeds are not fast enough to track a nanoparticle as it changes state, the time is short enough

to allow accurate measurements of both states while limiting DUT power dissipation to acceptable levels.

Pulsing Techniques

Choosing the correct measurement topology to improve measurement speed and minimize noise may still fall short of the test needs for some nanoscopic materials. For example, it appears that some CNTs can switch 1000 times faster than conventional CMOS transistor switches. This is too fast for the nanoamp ranges of commercial picoammeters. Demanding devices such as these may require other techniques to improve the speed of impedance measurements.

Low-power pulsing techniques may offer a partial solution to this problem and are available in some SMU designs. The idea is to use a much higher test current or test voltage and apply this large stimulus for a short sourcing cycle. The larger stimulus will lower the sourcing noise (by improving the signal-to-noise ratio) and improve the rise or settle time for a voltage pulse or current pulse, respectively. Quieter sources require less filtering and permit a shorter sourcing cycle time (narrower pulse width). A larger source stimulus also increases the response current or voltage so that higher instrument ranges can be used, further minimizing the effects of noise. Because there is less noise, the measurement acquisition time (integration period) can be shortened, thereby speeding up measurements.

Avoiding Self-Heating Problems

A possible source of error is self-heating due to excessive electrical current through the DUT. Such currents may even lead to catastrophic failure of the sample. Therefore, instrumentation must automatically limit source current during device testing. Programmable current and voltage compliance circuits are a standard feature of most SMU-based test systems with pulsed current capabilities, and may be required to avoid self-heating of some low-resistance structures.

When an elevated test current is required, it must be sufficiently brief so that it does not introduce enough energy to heat the DUT to destructive temperatures. (Nanoscopic devices tolerate very little heat, so the total energy dissipated in them must be maintained at low levels.) In addition, care must be taken that the magnitude of the test current is low enough that the DUT's nanoscopic channel does not become saturated. (For instance, a current channel 1.5 nm in diameter severely limits the number of electrons that can pass per unit of time.) Some nanoscopic devices can support only a few hundred nanoamps of current in their conductive state. Thus, a device's saturation current may define the maximum test current even in pulsed applications.

The following equation illustrates how duty cycle and measurement time in pulse mode affect DUT power dissipation. To calculate power dissipation in pulse mode, multiply the apparent power

dissipation ($V \cdot I$) by the test stimulus time and divide by the test repetition rate:

$$P_p = P_a \times T_t / T_r$$

where

P_p = Pulse power dissipation
P_a = Apparent power (i.e., $V \cdot I$)
T_t = Test time
T_r = Test repetition rate

Pulse mode is also useful for density-of-state measurements using a low-impedance connection, such as through a nanomanipulator. Pulsing allows measurements at previously forbidden I/V locations due to particle self-heating.

Summary

The electronic structure of nanoscopic particles is a reflection of the atomic electron energies and the distribution of orbitals for both molecularly shared and free electrons. This kind of information can be used to describe how such materials will interact in the presence of energy and other materials. The density of states in a material is directly related to its electronic structure and is useful in predicting or manipulating its properties.

It can be found through direct electrical measurements of differential conductance. Thus, the density of states can predict a material's electrical impedance and vice versa.

Still, there is a right way and a wrong way to electrically interrogate a nanoscopic material, depending on its impedance. For a low-impedance material, the source current/measure voltage method will result in the least electrical noise and allow the most accurate response measurement with the widest bandwidth. For a high-impedance material, the source voltage/measure current method is more appropriate for similar reasons. At times, the appropriate measurement mode must be used in unison with yet another voltage or current source to activate or stimulate the device.

14.3 Low-Level Measurement Techniques for Nanoscale Measurements

14.3.1 Recognizing the Sources of Measurements Errors

As good as electrical characterization and measurement systems are, making ultralow-current measurements on nanoelectronic and molecular scale devices is not trivial. Potential sources of measurement

Figure 14.4 Example of a Windows-based semiconductor characterization solution.

error must be understood and steps taken to reduce or eliminate them. Otherwise, a researcher will lack confidence in the characterization of materials and devices under test. Typically, nanoscale devices are characterized with semiconductor test instruments and probe station systems, such as the one shown in Figs. 14.4 and 14.5. The following examples and techniques can improve low-level current measurements.

Figure 14.5 Example of a powerful, dedicated system for electrical characterization of a nano and semiconductor devices and advanced materials. (Graphic courtesy of Kleindiek Nanotechnik.)

External Leakage Currents

Currents in the nanoamp to picoamp range are typically measured on nanoelectronic devices. External leakage current error sources must be minimized and instrument system leakage quantified. External leakage currents typically are generated between the measurement circuit and nearby voltage sources. These currents significantly degrade the accuracy of low-current measurements. One technique for minimizing leakage currents in a test circuit is the use of high-quality insulators (Teflon, polyethylene, or sapphire), which reduce the humidity of the test environment.

Insulators absorb water vapor from the air, with the amount absorbed dependent on the insulator material and humidity level. When the insulator contains ionic contaminants, spurious current generation can be especially troublesome in high-humidity environments. The best insulator choice is one on which water vapor does not readily form a continuous film. However, this may be unavoidable if the DUT absorbs water easily. In that case, it is best to make the measurements in an environmentally controlled, low-humidity room.

The use of guarding is a principal method of reducing leakage currents in a test circuit. A guard is a conductor connected to a low-impedance point in the circuit that is at nearly the same potential as the high-impedance lead being guarded (e.g., In/Out HI in Fig. 14.6). Guarding can isolate the high-impedance input lead of an electrometer, picoammeter, or SMU from leakage current due to voltage sources. Guarding can also reduce the effect of shunt capacitance in the measurement circuit.

Grounding and Shielding

It is important to distinguish between an instrument's common and chassis grounds. The common is the ground for the complete measurement circuit; it will affect the system's low-level measurement performance. In contrast, the chassis ground is connected to the power-line ground and is mainly used for safety reasons. Usually, there are no problems associated with connecting these grounds together. Sometimes, however, the power-line ground can be noisy. In other cases, a test fixture and probe station connected to the instrument may create a ground loop that generates additional noise. Accurate low-level measurements require a comprehensive system-grounding plan.

Although grounding and shielding are closely related, they are actually two different issues. In a test fixture or probe station, the DUT and probe typically are enclosed in soft metal shielding. The metal enclosure helps eliminate interference from power lines and high-frequency radiation (*radiofrequency* [RF] or microwave) and reduces magnetic interference. The metal normally is grounded for safety reasons. However, when an instrument is connected to a probe station

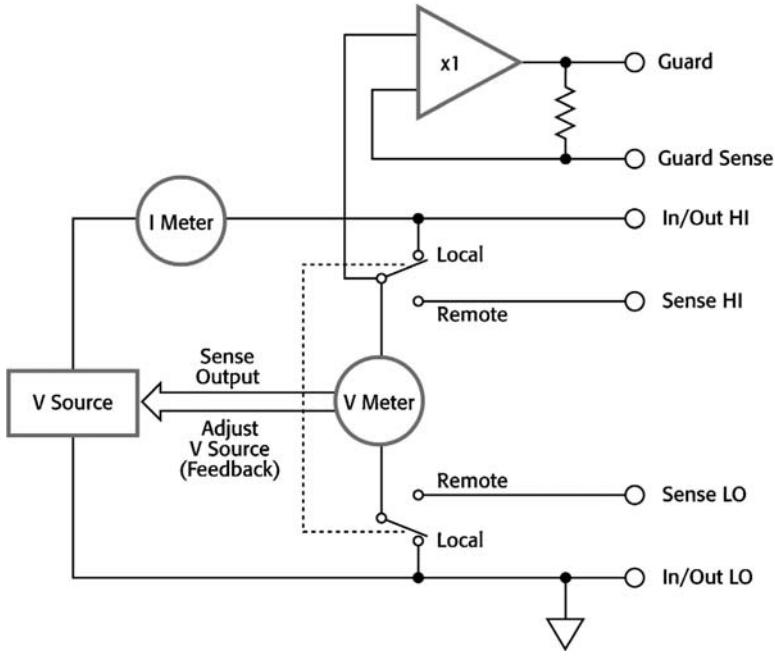


Figure 14.6 Simplified block diagram of an SMU configured to source voltage and measure current, showing guard connections.

through triaxial cables (the type used for guarded connections), physical grounding points are very important.

Noise

Even if a characterization system is properly shielded and grounded, it is still possible for noise to corrupt measurement results. Typically, instruments contribute very little to the total noise error in the measurements. (For example, a good characterization system has a noise specification of about 0.2 percent of range, meaning the p-p noise on the lowest current range is just a few femtoamps.) Noise can be reduced with proper signal averaging through filtering and/or increasing the measurement integration period (i.e., integrating over a larger number of power-line cycles).

The most likely sources of noise are other test system components, such as long cables or switching hardware inappropriate for the application. Therefore, it is advisable to use the best switch matrix available, designed specifically for ultralow-current measurements. Then, keep all connecting cables as short as possible.

Generally, system noise has the greatest impact on measurement integrity when the DUT signal is very small (i.e., low signal-to-noise

ratio). This leads to the classic problem of amplifying noise along with the signal. Clearly then, increasing the signal-to-noise ratio is key to low-level measurement accuracy.

Some characterization systems offer a low-noise preamplifier option that allows measurements down to the subfemtoamp level. To get that level of sensitivity, it is best to mount the preamps remotely on a probe station platen. With this arrangement, the signal travels only a very short distance (just the length of the probe needle) before it is amplified. Then, the amplified signal is routed through the cables and switch matrix into the measurement hardware.

Settling Time

Fast, accurate, low-current measurements depend a great deal on the way system elements work together. Measurement instruments must be properly synchronized with the prober and switching matrix, if one is used. Improper synchronization and source-measure delay may lead to a collection of signals unrelated to the real device parameters.

Settling time can vary widely for different systems, equipment, and cabling. It results mainly from capacitance inherent in switch relays, cables, etc., but may also be affected by dielectric absorption in the insulating materials of system components. High dielectric absorption can cause settling time to be quite long.

In most test situations, it is desirable to shorten test time to the minimum required for acceptable accuracy. This requires using the optimum source-measure delay, which is a function of the instrumentation source and measurement time, along with the system settling time. The latter usually is the dominant portion of source-measure delay time.

A step voltage test is typically used to characterize system settling time. A 10-V step is applied across two open-circuit probe tips, and then current is monitored continuously for a period of time. The resulting current vs. time (I-t) curve illustrates the transient segment and the steady current segment. Immediately after the voltage step, the transient current will gradually decay to a steady value. The time it takes to reach the steady value is the system settling time. Typically, the time needed to reach $1/e$ of the initial value is defined as the system time constant.

With the system leakage I-t curve in hand, the next step is to establish the acceptable measurement sensitivity or error. Suppose the task requires accurate DUT leakage measurements only at the picoamp level. Then, source-measure delay time can be established by a point on the transient portion of the system settling curve where the leakage current is at a subpicoamp level. If the expected DUT current is in the femtoamp range, then the delay time must be extended so that the transient current reaches a value lower than the expected reading before a measurement is taken.

System Leakage Current

Once the transient current has settled to its steady value, it corresponds to the system leakage current. Typically, system leakage current is expressed as amperes per volt. To determine its magnitude, simply measure the steady-state current and divide by the voltage step value. The magnitude of the system leakage current establishes the noise floor and overall sensitivity of the system. Usually, the largest leakage current contributors are the probe card and switching relays.

Extraneous Current

Errors in current measuring instruments arise from extraneous currents flowing through various circuit elements. In the current measurement model of Fig. 14.7, the current indicated on the meter (M) is equal to the actual current through the meter (I_1), plus or minus the inherent meter uncertainty. I_1 is the signal current (I_S), less the shunt current (I_{SH}) and the sum of all generated error currents (I_E).

Error Current Model

Figure 14.7 identifies the various noise and error currents generated during typical current measurements, which contribute to the error sum (I_E). The I_{SE} current generator represents noise currents produced within the DUT and its voltage source. These currents could arise due to the aforementioned leakage and dielectric absorption, or due to electrochemical, piezoelectric, and triboelectric effects. I_{CE} represents currents generated in the interconnection between the meter and the source/DUT circuit. I_{IE} represents the error current arising from all internal measuring instrument sources. I_{RE} is generated by the thermal activity of the shunt resistance. The rms value of this thermal noise current is given by

$$I_{RE} = (4kTf/R_{SH})^{1/2}$$

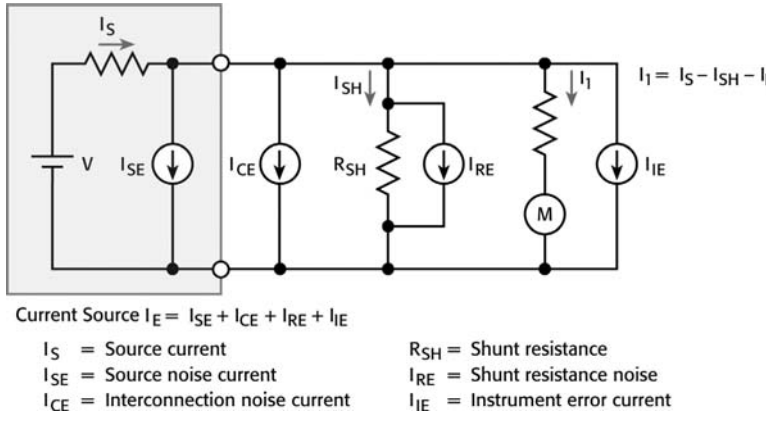


Figure 14.7 Source of current error in shunt-type ammeter.

where

k = Boltzmann's constant (1.38×10^{-23} J/K)
T = Absolute temperature in kelvins
f = Noise bandwidth in hertz
R_{SH} = Resistance in ohms

14.3.2 AC versus DC Measurement Methods for Low-Power Nanotech and Other Sensitive Devices

Sensitive Measurement Needs

Researchers today must measure material and device characteristics that involve very small currents and voltages. Examples include the measurement of resistance and I-V characteristics of nanowires, nanotubes, semiconductors, metals, superconductors, and insulating materials. In many of these applications, the applied power must be kept low in order to avoid heating the DUT, because (1) the DUT is very small and its temperature can be raised significantly by small amounts of applied power, or (2) the DUT is being tested at temperatures near absolute zero where even a millidegree of heating is not acceptable. Even if applied power is not an issue, the measured voltage or current may be quite small because of extremely low or high resistance.

Measurement Techniques and Error Sources

The key to making accurate low-power measurements is minimizing the noise. In many low-power measurements, a common technique is to apply a low-level ac current to the DUT and measure its voltage drop. An alternative is to use a dc current reversal technique. In either case, a number of error sources must be considered and controlled.

As previously mentioned, Johnson noise places a fundamental limit on resistance measurements. In any resistance, thermal energy produces the motion of charged particles. This charge movement results in Johnson noise. It has a white noise spectrum and is determined by the temperature, resistance, and frequency bandwidth values. The formula for the voltage noise generated is

$$V_{\text{Johnson}}\,(\text{rms}) = \sqrt{(4kTRB)}$$

where

k = Boltzmann's constant (1.38×10^{-23} J/K)
T = Absolute temperature in kelvins
R = DUT resistance in ohms
B = Noise bandwidth (measurement bandwidth) in hertz

Johnson noise may be reduced by:

- Reducing bandwidth with digital filtering (averaging readings) or analog filtering
- Reducing the temperature of the device
- Reducing the source resistance

External noise sources are interferences created by motors, computer screens, or other electrical equipment. They can be controlled by shielding and filtering or by removing or turning off the noise source. Because these noise sources are often at the power-line frequency, it is common practice to avoid ac test frequencies that are exact multiples or fractions of 60 Hz (or 50 Hz). With the dc reversal technique, the same result is achieved by integrating each measurement for an integer number of power-line cycles.

Thermoelectric voltages are generated when different parts of a circuit are at different temperatures and when conductors made of dissimilar metals are joined together. Reducing thermoelectric voltages can be accomplished by keeping all connections at the same temperature and using crimped copper-to-copper connections wherever possible. Given that it is rarely possible to use copper everywhere in the circuit (DUTs are rarely copper themselves), a measurement technique, such as the lock-in technique or the dc reversal method, is required to eliminate noise due to thermal effects.

Test lead resistance can also create an additive error in the resistance being measured. To prevent lead resistance from affecting measurement accuracy, the four-wire (Kelvin) measurement configuration should be used.

1/f noise is a term used to describe any noise that has increasing magnitude at lower frequencies. Noise with this characteristic can be seen in components, test circuits, and instruments. It can be caused by environmental factors, such as temperature or humidity, or by chemical processes within components, which are often given the label "aging," "burn-in," or "drift." $1/f$ noise can be observed as a current, voltage, temperature, or resistance fluctuation.

For this discussion, we are focusing on the $1/f$ voltage noise in a measurement system. Material characteristics of a DUT or a test circuit component greatly influence this type of noise. For example, carbon composite resistors typically exhibit a resistance noise of 0.01 to 0.3 percent. The noise value for metal film and wire-wound resistors is about one-tenth that of composite resistors. Semiconductors fall somewhere in between these two material types.

Measurement Systems

In sensitive *I-V* and resistance measurements, there are two parts to the instrumentation: the current source and the voltage measurement

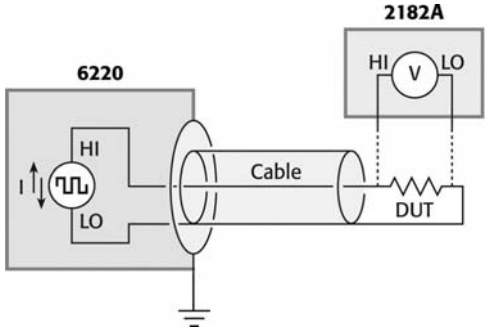


Figure 14.8 Dc reversal measurement circuit using a four-wire lead arrangement.

instrument. For the dc reversal method, a current source with reversible polarity is used, and the DUT response is measured with a nanovoltmeter.

Dc Reversal Measurement Method

This approach uses dc polarity reversals in the applied current signal to nullify noise. This is a well-established technique for removing offsets and low-frequency noise. Today's dc sources and nanovoltmeters offer significant advantages over expensive ac lock-in amplifiers in reducing the impact of error sources and the time required to achieve a low-noise measurement.

As shown in Fig. 14.8, one simply applies a current to the DUT and measures the DUT voltage, then reverses the current and remeasures the voltage. The difference of the two measurements divided by 2 is the voltage response of the DUT to the applied current level. Repeating the process and using averaging reduces the noise bandwidth and therefore, the noise. These are called "delta" measurements by some researchers.

In the past, this was a manual technique with most instruments, which limited the reversal speed to less than 1 Hz. Modern instruments now allow the technique to be automated and the reversal speed increased. The reversal speed sets the frequency that dominates the noise. Higher reversal speed removes low-frequency noise and thermal drift better, because these noise sources have lower power at higher frequencies.

To truly compensate for thermal drift, the delta method consists of alternating the current source polarity and using a moving average of three voltage readings to calculate resistance (Fig. 14.9). The three measurements are:

$$V_{M1} = V_{DUT} + V_{EMF}$$
$$V_{M2} = -V_{DUT} + V_{EMF} + \delta V$$
$$V_{M3} = V_{DUT} + V_{EMF} + 2\,\delta V$$

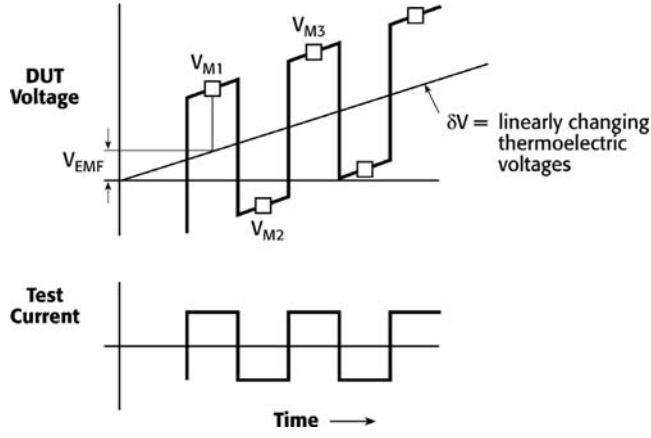


FIGURE 14.9 Test signals and thermoelectric error voltages during dc reversal (delta) measurements.

where

V_{M1}, V_{M2}, and V_{M3} are voltage measurements

V_{DUT} = The voltage drop of the DUT due to the applied current

V_{EMF} = The constant thermoelectric voltage offset at the time VM1 is taken

δV = Linearly changing thermoelectric voltage

Cancellation of both the thermoelectric voltage offset (V_{EMF}) and the thermoelectric voltage change (δV) term is possible through a mathematical computation using the three voltage measurements. First, take one-half the difference of the first two voltage measurements and call this V_A:

$$V_A = (V_{M1} - V_{M2})/2 = [(V_{DUT} + V_{EMF}) - (-V_{DUT} + V_{EMF} + \delta V)]/2$$
$$= V_{DUT} - \delta V/2$$

Likewise, take one-half the difference of the second (V_{M2}) and third (V_{M3}) voltage measurements and call this term V_B:

$$V_B = (V_{M3} - V_{M2})/2$$
$$= [(V_{DUT} + V_{EMF} + 2\delta V) - (-V_{DUT} + V_{EMF} + \delta V)]/2$$
$$= V_{DUT} + \delta V/2$$

Each of these results has eliminated the constant offset, V_{EMF}, but still has errors from the drift term, δV. The average of V_A and V_B, however, is simply V_{DUT}.

$$V_{final} = (V_A + V_B)/2 = (V_{M1} - 2V_{M2} + V_{M3})/4 = V_{DUT}$$

Successive readings can then be averaged to reduce the measurement bandwidth to reach desired noise levels.

Upon examination, the preceding mathematics is really the multiplication of a string of VM readings by a sequence of weightings +1, −1, +1, etc. It is exactly analogous to the way a lock-in amplifier multiplies its acquired signals by the sine functions, which are used as the stimulus. The commercially available current source and nanovoltmeter described in the endnote of this discussion automate the entire procedure; resistance values are calculated and displayed by the instrumentation.

Measurements on Low-Resistance DUTs

A typical low-resistance measurement application is shown in Fig. 14.10. Instrument voltage noise is generally the dominant error in low-resistance measurements, but below a certain level of device resistance, common-mode noise becomes a problem.

The four lead resistances shown in Fig. 14.10 vary from 0.1 Ω to 100 Ω, depending on the experiment. They are important to note, because with low-resistance devices, even the impedance of copper connection wires can become large compared to the DUT resistance. Further, in the case of many low-impedance experiments carried out at low temperatures, there are often RF filters (e.g., Pi filters) in each of the four device connection leads, typically having 100 Ω of resistance.

Regardless of the instruments used to carry out the ac measurements, the test current flows through the source connection leads and develops a voltage drop from the circuit ground to the connection to the DUT, denoted as Circuit Node A. Thus, the voltage at circuit node A moves up and down with an amplitude of $I_{TEST} \times R_{LEAD}$ volts, while the $V_{MEASURE}$ input is trying to detect a much smaller ac voltage of $I_{TEST} \times R_{DUT}$.

With the connections in this type of measurement circuit, the *common-mode rejection ratio* (CMRR) becomes an issue. CMRR specifies how well an instrument can reject variations in the measurement LO potential. The CMRR specification for a typical lock-in amplifier is 100 dB (a factor of 10^5 rejection). In actual measurement practice, this is more likely to fall in the range of 85 to 90 dB. By comparison,

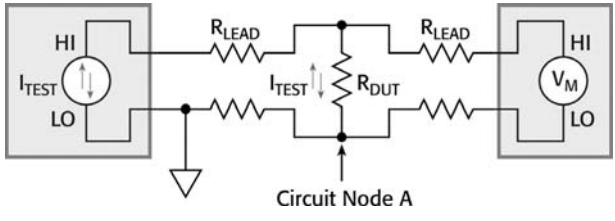


Figure 14.10 Block diagram of a typical low-resistance measurement.

nanovoltmeters are available with CMRR specifications of 140 dB. Combined with a modern current source operating in delta mode, it is possible to achieve a CMRR of better than 200 dB in actual measurements.

To understand the impact of CMRR, consider the example described previously. With only 100-dB rejection, the measurement of V_{DUT} (which should be $I_{TEST} \times R_{DUT}$) is in fact $I_{TEST} \times R_{DUT} \pm I_{TEST} \times R_{LEAD}/10^5$. Thus, there is a 1 percent error when R_{LEAD} is $10^3 \times R_{DUT}$. With 100-Ω lead resistance, it is impossible to make a measurement within ±1 percent error bounds when R_{DUT} is less than 0.1 Ω. On the other hand, a modern dc current source and nanovoltmeter, with their combined CMRR of greater than 200 dB, can measure resistances as low as 1 $\mu\Omega$ within ±1 percent error bounds, even with a 100-Ω lead resistance.

High Resistance Measurements

Values of DUT resistance greater than 10 kΩ present challenges of current noise and input loading errors. Current noise becomes visible as a measured voltage noise that scales with the DUT resistance. In dc reversal systems, current noise comes from the measurement circuit and creates additional ac and dc voltage as it flows through the DUT and/or lead resistance. A typical value is 50 pA dc with 80 fA/$\sqrt{\text{Hz}}$ noise for the reversible current source/nanovoltmeter combination.

The second limitation in measuring higher DUT resistances is the input impedance of the voltage measuring circuit, which causes loading errors. Consider the measurement of a DUT with 10 MΩ of resistance. A typical lock-in amplifier has an input impedance of about the same magnitude—10 MΩ . This means that half of the current intended for the DUT will instead flow through the instrument input, and the measured voltage will be in error by 50 percent. Even with careful subtraction schemes, it is not practical to achieve ±1 percent accuracy when measuring a DUT with a resistance greater than 1 MΩ when using a lock-in amplifier.

By contrast, a nanovoltmeter has 1,000 times higher input impedance (i.e., 10 GΩ), so it can measure up to 1 GΩ with ±1 percent accuracy. (Subtracting the loading effect of the 10 GΩ only requires knowing the input resistance to ±10 percent accuracy, which is readily measured by performing the dc reversal measurement using an open circuit as the "DUT.") Moreover, some current sources provides a guard amplifier, so the nanovoltmeter can measure the guard voltage instead of the DUT voltage directly. This reduces the current noise transmitted to the DUT down to the noise of the current source (below 20 fA/$\sqrt{\text{Hz}}$). This configuration reduces the loading error, noise, and power in situations where the lead resistance is negligible and a two-wire connection to the DUT is acceptable.

Midrange Resistance Measurements

Traditionally, lock-in amplifiers have been used for measurements in the range of 100 mΩ to 1 MΩ due to the significant limitations outside this range. Even when R_{DUT} falls in this range, using the dc reversal method may provide an advantage. For example, a lock-in amplifier has two times (or higher) white noise than a modern dc reversal system, and its $1/f$ voltage noise is 10 times higher. When working at 13 Hz (a typical frequency in lock-in measurements), a typical dc reversal system has about seven times lower voltage noise than a lock-in amplifier. This leads to 50 times less required power.

Individual Instrument Noise Comparisons

All electronic circuits generate both white noise and $1/f$ noise. The noise of low-frequency measurements is often dominated by the latter. A lock-in amplifier's front end is usually the dominant source of $1/f$ noise. Instruments used in the dc reversal method have similar issues. Therefore, comparing the noise performance of a lock-in amplifier with an instrument using the dc reversal method is essentially a case of comparing the noise performance of their front-end circuitry. Furthermore, the DUT resistance value must be considered when making these comparisons.

It is common for manufacturers to specify their white noise performance, but less common to be given a $1/f$ noise specification. To make a valid comparison, the noise level should be determined as measurements are made. Another important consideration is whether to use the system voltage noise or current noise. Figure 14.11 shows a model of a measurement system with V_n being the voltage noise of the system, I_n being the current noise, and I_S being the source current.

A signal-to-noise ratio of 1 (one possible measurement objective) is achieved when the power forced on the DUT equals the noise power of the system. This is expressed by

$$P_{DUT} = I^2{}_S \times R_{DUT} = V^2{}_n/R_{DUT} + I^2{}_n \times R_{DUT}$$

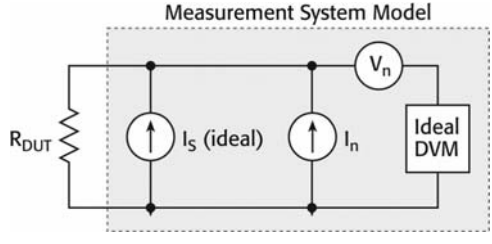


Figure 14.11 Idealized measurement circuit with current and voltage noise sources, I_n and V_n.

Voltage noise dominates when the DUT resistance is low, and current noise dominates when the DUT resistance is high. The required power is minimum when R_{DUT} equals V_n / I_n. Ultimately, a major determinant of instrument performance is how little power can be imposed on the DUT and still get a good measurement. Nevertheless, it is important to remember that very low and very high values of R_{DUT} impose different types of instrument limitations on these measurements compared to midrange values.

Noise, Applied Power, and Measurement Time Considerations

To put noise error into perspective, consider measurements with a desired signal-to-noise ratio of 100. It can be shown that noise power ($V^2_{Johnson}/R$) in the DUT measurement is a function of temperature and is not dependent on its resistance. Measuring a DUT with 1 percent RMS noise requires a signal voltage 100 times the noise voltage, and thus a signal power 10,000 (100^2) times the noise power.

Depending on which is greater, the system noise or the DUT noise should be used to determine the applied power required, which in most measurements should be as low as possible. Increasing the measurement time decreases the required power by the same factor as the increase in time. For example, if time is increased by a factor of 4 (e.g., from 0.5 s to 2 s), then the required power decreases by a factor of 4. Physics presents the only limitation on a dc reversal system, and low-temperature measurements will benefit from the full capabilities of the system to make measurements with even less power.

14.3.3 Achieving Accurate and Reliable Resistance Measurements in Low-Power and Low-Voltage Applications

Low-voltage measurements are often associated with resistance measurements of highly conductive semiconductor materials and devices. These tests normally involve sourcing a known current, measuring the resulting voltage, and calculating the resistance using Ohm's law. Because of the DUT's typically low resistance, the resulting voltage will be very small, and great care needs to be taken to reduce offset voltage and noise, which can normally be ignored when measuring higher signal levels.

However, low-voltage measurements can also result from resistance measurements of nonconductive materials and components. Electronics are continuing to shrink as consumers demand faster, more feature-rich products in ever-smaller form factors. Because of their small sizes, electronic components of today usually have limited power-handling capability. As a result, when electrically characterizing these components, the test signals need to be kept small to prevent component breakdown or other damage.

In resistance measurements, even if the resistance is far from zero, the voltage to be measured is often very small due to the need to source only a small current. Therefore, low-level voltage measurement techniques become important, not only for low-resistance measurements, but also for resistance measurements of nonconductive materials and components. For researchers and electronics industry test engineers, this power limitation often makes characterizing the resistance of modern devices and materials challenging.

There are many factors that make low-voltage measurements difficult. Various noise sources can make it difficult to resolve the actual voltage. In addition, thermoelectric voltages (thermoelectric EMFs) can cause error offsets and drift in the voltage readings. As mentioned previously, test requirements may limit the maximum current that can be applied, so simply increasing the sourced signal (test current) is not always an option. In other cases, increasing the test current could cause device heating, which can change the DUT's resistance and possibly destroy the DUT. The key to obtaining accurate, consistent measurements is eliminating factors that contribute to measurement error. For low-voltage measurement applications, such error is composed largely of white noise (random noise across all frequencies) and $1/f$ noise. Thermoelectric voltages (typically having $1/f$ distribution), a serious problem in many test environments, are generated from temperature differences in the circuit.

This discussion reviews techniques to eliminate thermoelectric voltages to allow more accurate resistance measurements, including a three-step delta measurement method for low-power/low-voltage applications

Measurement Obstacles

Temperature fluctuations are the biggest enemy of low-voltage measurements. Any junction of dissimilar metals in a measurement circuit constitutes a thermocouple. Voltage errors occur when there is an opposing junction at a different temperature. Figure 14.12 illustrates one example of this error.

In this example, the device under test is located on a silicon wafer. A tungsten probe makes contact with one terminal of the device. The other terminal is the silicon substrate. A copper base is used to make electrical contact with the substrate. The junctions of differing materials produce three separate thermocouples: at the copper-tungsten interface, at the tungsten-silicon interface, and at the silicon-copper interface. The temperature difference between the two materials at each junction generates a voltage at the voltmeter terminals. The summation of the thermoelectric voltages at each of these junctions is the total error voltage that appears at the voltmeter terminals.

The first step toward reducing measurement error is minimizing the temperature variation in the test environment. This would

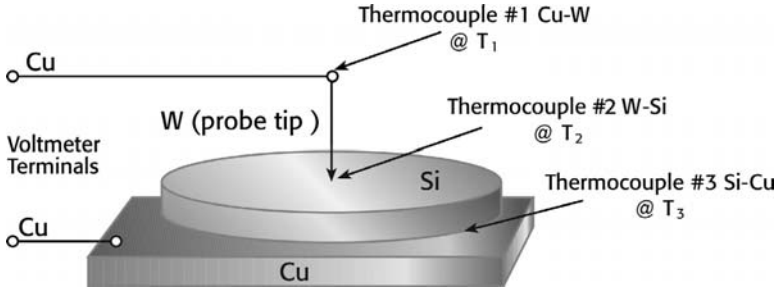


Figure 14.12 Typical thermocouple scenario. Cu-Si interface where one terminal is one device on wafer and the second terminal is at the substrate connection to a conductive base.

mean reducing the temperature difference between T_1, T_2, and T_3 in Fig. 14.12. The test setup should be isolated from drafts, air conditioning, and heat sources. The connections should be located as close to each other as possible to minimize temperature differences. Whenever possible, the designer of the setup should use connections made of the same material and select insulators with high thermal conductivity to surround the cables and junctions.

Traditional Resistance Measurements

No matter what steps are taken to minimize temperature problems, it's virtually impossible to eliminate them entirely. A standard dc resistance measurement approach does not compensate for any of these errors. Resistance is calculated using Ohm's law; that is, to find the resistance, divide the dc voltage measured across the device by the dc stimulus current (Fig. 14.13*A*). The voltage readings will be a sum of the induced voltage across the device (V_R), lead and contact resistance ($V_{\text{lead res}}$), the voltages present from the thermals (V_t), other $1/f$

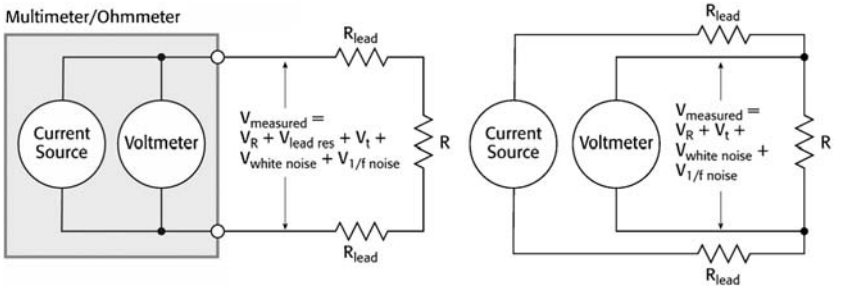


Figure 14.13 The delta method of measuring resistance. The schematic on the left shows a standard dc resistance measurement setup. Changing the standard measurement setup to the schematic on the right by using four leads eliminates errors due to the lead resistance.

noise contributions ($V_{1/f\ noise}$), and white noise ($V_{white\ noise}$). To eliminate lead resistance, use four separate leads to connect the voltmeter and current source to the device. In this way, the voltmeter will not measure any voltage drop across the source leads. However, the errors due to white noise, $1/f$ noise, and temperature differences will remain (Fig. 14.13*B*). Implementing filtering and selecting the appropriate test equipment may reduce white noise and $1/f$ noise significantly. However, these elements often determine the measurement noise floor. Temperature presents a slightly different challenge because if the temperature changes, the contribution of the V_t term changes, too. With rapidly changing thermoelectric voltages, this term may even exceed V_R, the voltage across the DUT induced by the stimulus. It is possible to reduce thermoelectric voltages using techniques such as all-copper circuit construction, thermal isolation, precise temperature control, and frequent contact cleaning. However, it would be preferable to have a method that would allow accurate resistance measurements even in the presence of large thermoelectric voltages, instead of working to minimize them.

The Delta Method of Measuring Resistance

A change in test method is required to improve accuracy and overcome measurement obstacles. A constant thermoelectric voltage may be canceled using voltage measurements made at a positive test current and a negative test current. This is called a delta reading. Alternating the test current also increases white noise immunity by increasing the signal-to-noise ratio. A similar technique can be used to compensate for changing thermoelectric voltages (Fig. 14.14).

Over the short term, thermoelectric drift may be approximated as a linear function (inset of Fig. 14.14). The difference between consecutive

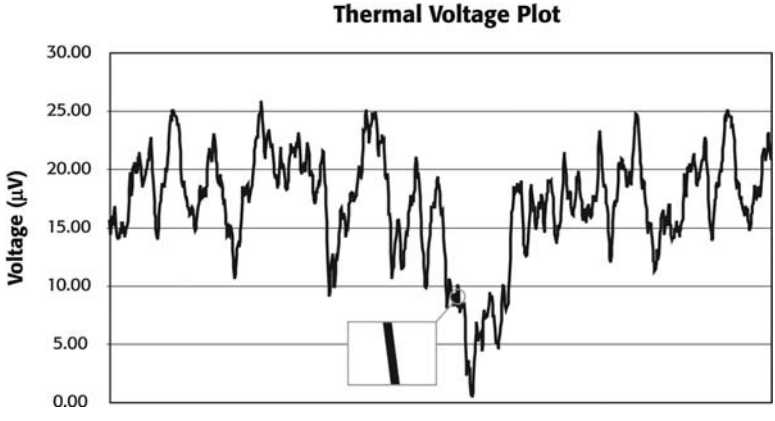


Figure 14.14 Thermoelectric drift approximated as a linear function.

voltage readings is the slope—the rate of change in thermoelectric voltage. This slope is constant, so it may be canceled by alternating the current source three times to make two delta measurements—one at a negative-going step and one at a positive-going step. In order for the linear approximation to be valid, the current source must alternate quickly and the voltmeter must make accurate voltage measurements within a short time interval. If these conditions are met, the three-step delta technique yields an accurate voltage reading of the intended signal unimpeded by thermoelectric offsets and drifts.

Examining this technique in detail reveals how it reduces measurement error. An analysis of the mathematics for one three-step delta cycle demonstrates how the technique compensates for the temperature differences in the circuit. Consider the example in Fig. 14.15:

$$\text{Test current} = \pm 10\,\text{nA}$$
$$\text{Device} = 100\text{-}\Omega\,\text{resistor}$$

Ignoring thermoelectric voltage errors, the voltages measured at each of the steps are:

$$V_1 = 1\,\mu\text{V}$$
$$V_2 = -1\,\mu\text{V}$$
$$V_3 = 1\,\mu\text{V}$$

Let us assume the temperature is linearly increasing over the short term in such a way that it produces a voltage profile like that shown in Fig. 14.15*B*, where V_t = 100 nV and is climbing 100 nV with each successive reading.

As Fig. 14.15*B* shows, the voltages now measured by the voltmeter include error due to the increasing thermoelectric voltage in the circuit; therefore, they are no longer of equal magnitude. However, the absolute difference between the measurements is in error by a constant 100 nV, so it is possible to cancel this term. The first step is to calculate the delta voltages. The first delta voltage (V_a) is equal to

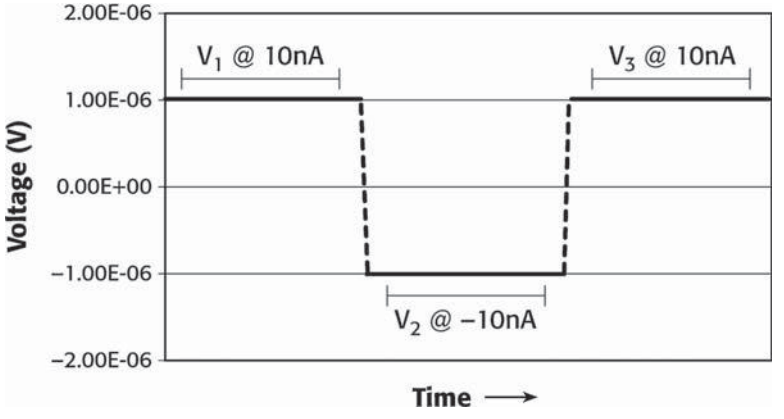
$$V_a = \text{negative-going step} = (V_1 - V_2)/2 = 0.95\,\mu\text{V}$$

The second delta voltage (V_b) is made at the positive-going current step and is equal to

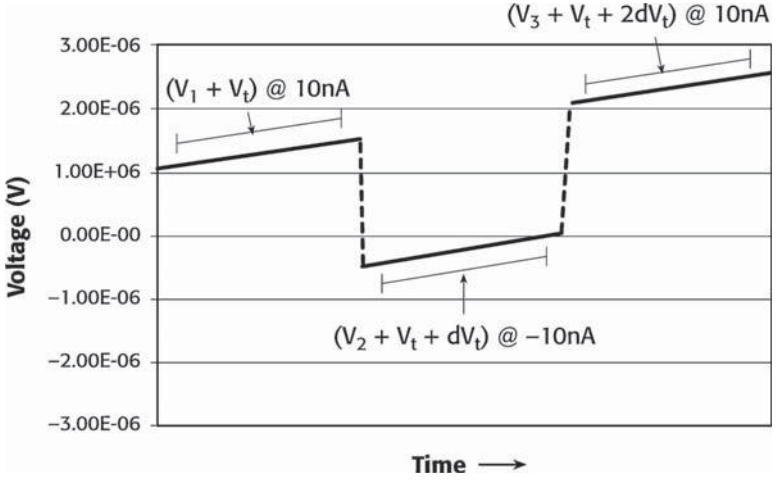
$$V_b = \text{positive-going step} = (V_3 - V_2)/2 = 1.05\,\mu\text{V}$$

The thermoelectric voltage adds a negative error term in V_a and a positive error term in the calculation of V_b. When the thermal drift is a linear function, these error terms are equal in magnitude. Thus, we can cancel the error by taking the average of V_a and V_b:

$$V_f = \text{final voltage reading}$$
$$= (V_a + V_b)/2 = (1/2) \times [(V_1 - V_2)/(2) + (V_3 - V_2)/(2)] = 100\,\mu\text{V}$$



(*A*)



(*B*)

Figure 14.15 (*A*) An alternating, three-point delta method of measuring voltage with no thermoelectric voltage error. (*B*) A linearly increasing temperature generates a changing thermoelectric voltage error, which is eliminated by the three-point delta method.

The delta technique eliminates the error due to changing thermoelectric voltages. Therefore, the voltmeter measurement is the voltage induced by the stimulus current alone. As the test continues, every reading is the average of the three most recent *analog-to-digital* (A/D) conversions, so a moving average filter is embedded in this three-step delta technique. The moving average filter further enhances white noise immunity by reducing the spread of the data. The three-step delta method clearly offers significant advantages over other dc

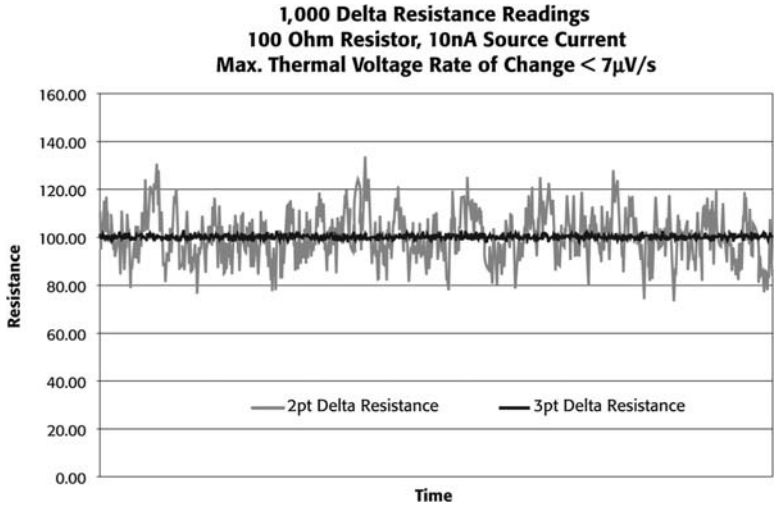


Figure 14.16 A graph comparing the results of a two- and three-point delta method shows significant noise reduction using the three-point method.

resistance measurement techniques in overcoming error due to changing temperature.

Other dc resistance measurement techniques include a two-step current reversal and offset compensation, a subset of the three-step method. The two-step method calculates an average based on only the first delta (V_a) of the three-step method. Offset compensation is really a subset of the three-step delta method where the current is alternated between some positive value and zero. The offset compensation method is commonly found in digital multimeters where the test current cannot be programmed or reversed. Although this two-point technique sufficiently compensates for constant thermoelectric error voltages, it is inadequate when the temperature is changing.

The three-step delta technique is the best choice for high accuracy resistance measurements. Figure 14.16 compares 1,000 voltage measurements of a 100-Ω resistor made with a 10-nA test current taken over approximately 100 s. In this example, the rate of change in thermoelectric voltage is no more than 7 μV/s. The two-step delta technique fluctuates with the thermoelectric error voltage ±30 Ω around the true resistance value. Thus, for any one measurement, there could be an error of up to 30 percent, which provides little confidence in the measurement's integrity. In contrast, the three-step delta technique is "tightly packed" around the average—the measurement is unaffected by the thermoelectric variations in the test circuit. It is important to note that both these measurements can be completed in the same test time.

In addition, the speed of the three-step delta method permits additional digital averaging of the data, so it has lower noise than data taken with the two-step delta technique. Figure 14.17 provides a more detailed examination of the three-step delta technique.

Equipment Requirements

Selecting appropriate measurement equipment is critical to the three-step delta method. Pairing a current source with a nanovoltmeter where the two can be operated like a single instrument and meet the accuracy and repeatability requirements of low-power and low-voltage applications is the first step. By understanding how the equipment affects the measurement, the researcher or test engineer can also minimize white noise and $1/f$ noise.

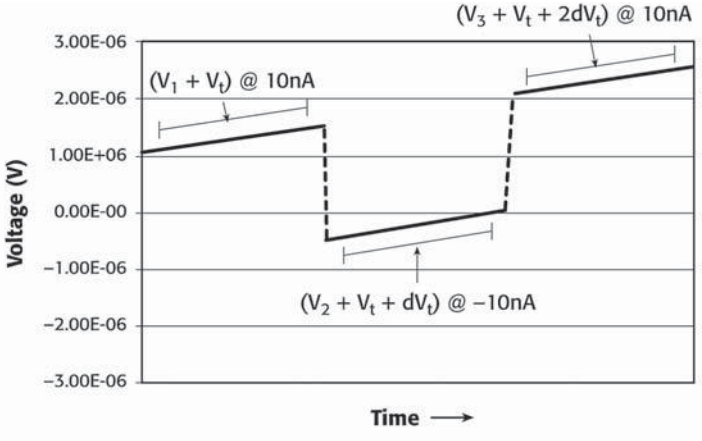
The success of the three-step delta method depends on the linear approximation of the thermal drift when this drift is viewed over a short time interval. This approximation requires the measurement cycle time to be faster than the thermal time constant of the test system, which imposes certain requirements on the current source and voltmeter used.

The current source must alternate quickly in evenly spaced steps, which helps make a fast measurement cycle time possible. The current step spacing guarantees the measurements are made at consistent intervals so the thermoelectric voltage change remains constant between these measurements.

The voltmeter must be tightly synchronized with the current source and capable of making accurate measurements in a short time interval. Synchronization favors hardware handshaking between the instruments so that the voltmeter can make voltage measurements only after the current source has settled, and the current source does not switch polarity until after the voltage measurement has been completed. The measurement speed of the voltmeter is critical in determining total cycle time; faster voltage measurements mean shorter cycle times. For reliable resistance measurements, the voltmeter must maintain this speed without sacrificing low-noise characteristics.

14.3.4 Characterizing Nanoscale Devices with Differential Conductance Measurements

As modern electronics continue to shrink, researchers increasingly look to nanotechnology for breakthroughs in device size and power consumption. In these nanoscale devices, electrical characteristics are affected by quantum behavior. In the macroscopic world, conductors may have obeyed Ohm's law (Fig. 14.18*A*), but in the nanoscale, Ohm's definition of resistance is no longer relevant (Fig. 14.18*B*). Because the slope of the I-V curve is no longer a fundamental constant of the material, a detailed measurement of the slope of that I-V curve at



V_a = negative-going step

$$= \frac{(V_1 + V_t) - (V_2 + V_t + dV_t)}{2} = \frac{(V_1 - V_2 - dV_t)}{2}$$

$$= \frac{(V_1 - V_2)}{2} - \frac{dV_t}{2}$$

V = positive-going step

$$= \frac{(V_3 + V_t + 2dV_t) - (V_2 + V_t + dV_t)}{2} = \frac{(V_3 - V_2 + dV_t)}{2}$$

$$= \frac{(V_3 - V_2)}{2} + \frac{dV_t}{2}$$

V_f = final voltage reading = average (V_a, V_b)

$$= \frac{(V_a + V_b)}{2} = \frac{(V_1 + V_3 - 2V_2)}{4}$$

For linear devices, $|V_1| = |V_2| = |V_3| = V_R$ = voltage across resistor induced by stimulus current.

Thus: $V_1 = \frac{1}{4}(4V_R) = V_R$

Figure 14.17 Detailed three-step delta calculations.

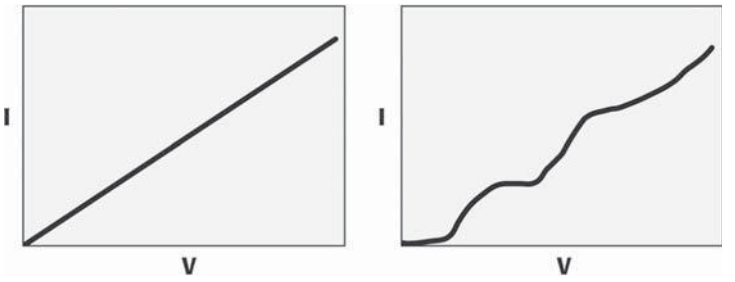


Figure 14.18 (*A*) Macroscopic scale (classical). (*B*) Nanoscale (quantum).

every point is needed to study nanodevices. This plot of differential conductance ($dG = dI/dV$) is the most important measurement made on small-scale devices, but presents a unique set of challenges.

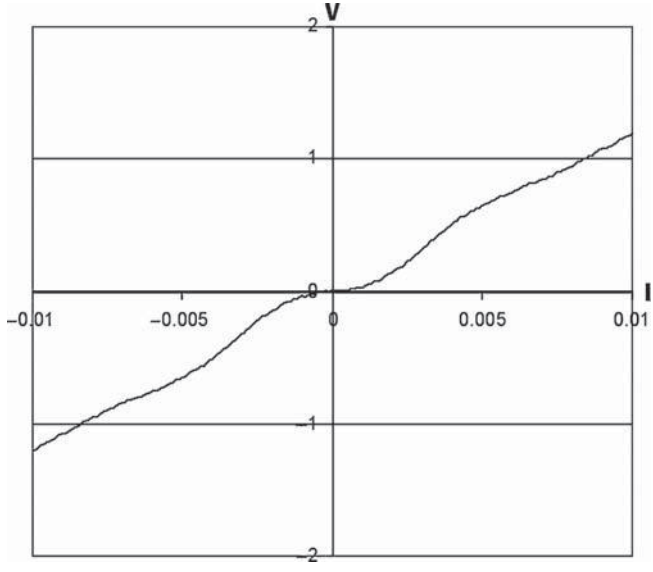
Who Uses Differential Conductance?

Differential conductance measurements are performed in many areas of research, though sometimes under different names. Table 14.1 lists some of these applications.

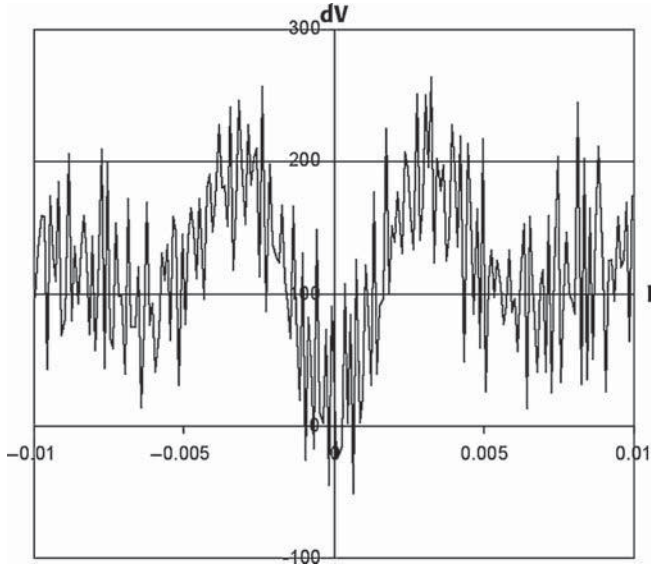
The fundamental reason for these studies is that device conductance reaches a maximum at voltages (or more precisely, at electron energies in electron volts) where electrons are most active. Thus, dI/dV is directly proportional to the density of states and is the most direct way to measure it.

Area of Research	Structures Studied	Measurement Nomenclature
Electron energy structure	Quantum dots, nanoparticles, artificial atoms	Electron energy spectroscopy
Noncontact surface characteristics	Variety of nanoscale materials and devices	Scanning tunneling spectroscopy
Electronic properties	Ultrasmall semiconductors and nanotubes with semiconducting properties	Density of states
Electrical *I*-*V* characteristics	Conduction at room and cryogenic temperatures, tunneling phenomena, etc.	Differential conductance ($dG = dI/dV$)

Table 14.1 Examples of Research Uses for Differential Conductance Measurements and Associated Nomenclatures

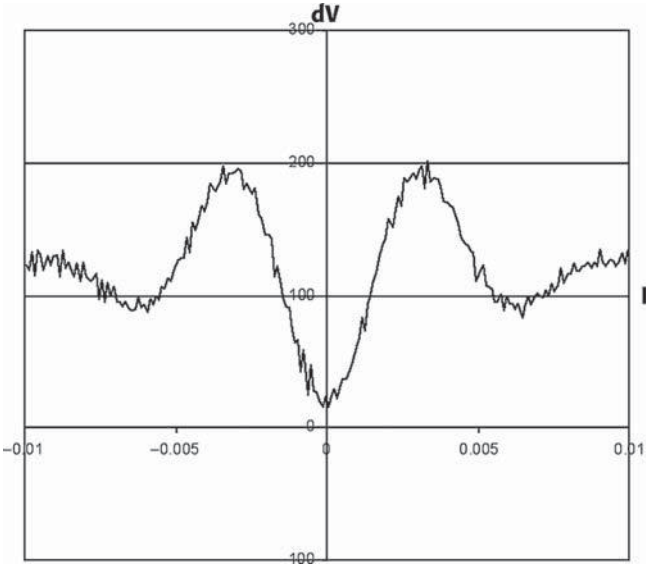


(*A*)



(*B*)

Figure 14.19 (*A*) *I-V* curve; (*B*) differentiated *I-V* curve. (*Continued*)



(*C*)

FIGURE 14.19 (*Continued*) (*C*) 100 differentiated curves, averaged together.

Existing Methods of Measuring Differential Conductance

Although there is no standardized technique for obtaining differential conductance, almost all approaches follow one of two methods: (1) Perform a current-voltage sweep (I-V curve) and take the mathematical derivative, or (2) superimpose a low-amplitude ac sine wave on a stepped dc bias; then use a lock-in amplifier to obtain the ac voltage across the DUT and the ac current through it.

The *I-V* Technique

The I-V sweep technique has the advantage of being easier to set up and control. It only requires one source and one measurement instrument, which makes it relatively easy to co-ordinate and control. The fundamental problem is that even a small amount of noise becomes a large noise when the measurements are differentiated.

Figure 14.19*A* shows an I-V curve, which is a series of sourced and measured values (V_1, I_1), (V_2, I_2), etc. Several techniques can be used to differentiate these data, but the simplest and most common uses the slope between every pair of consecutive data points. For example, the first point in the differential conductance curve would be $(I_2 - I_1)/(V_2 - V_1)$. Because of the small differences, a small amount of noise in either the voltage or current causes a large uncertainty in the conductance. Figure 14.19*B* shows the differentiated curve and the noise, which is unacceptably large for most uses. To reduce this noise,

the I-V curve and its derivative can be measured repeatedly. Noise will be reduced by $\sqrt{N}$, where N is the number of times the curve is measured. After 100 repetitions, which can take more than an hour in a typical application, it is possible to reduce the noise by a factor of 10, as shown in Fig. 14.19*C*. Although this could eventually produce a very clean data set, researchers are forced to accept high noise levels, because measuring 10,000 times to reduce the noise by a factor of 100 would take far more time than is usually available. Thus, although the I-V curve technique is simple, it forces a trade-off between high noise and very long measurement times.

The AC Technique

The ac technique superimposes a low-amplitude ac sine wave on a stepped dc bias, as shown in Fig. 14.20. The problem with this method is that, although it provides a marginal improvement in noise over the I-V technique, it imposes a large penalty in terms of system complexity (Fig. 14.21). A typical equipment list includes:

- Ac voltage source or function generator
- Dc bias source
- Series resistor or coupling capacitor to mix ac and dc signals
- Lock-in amplifier synchronized to the sources to facilitate low-level measurements
- Separate instruments to measure ac and dc voltage and current

Assembling such a system requires extensive time and knowledge of electrical circuitry. Trial-and-error methods may be required to determine the series resistor and coupling capacitor values based on the unknown DUT impedance and response frequency. Long cabling, such as that used in attaching a device in a cryostat, reduces usable

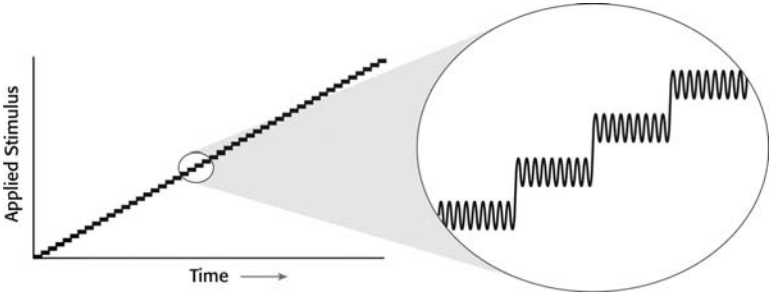


Figure 14.20 The ac technique measures the response to a sine stimulus while sweeping the dc bias through the device's operating range.

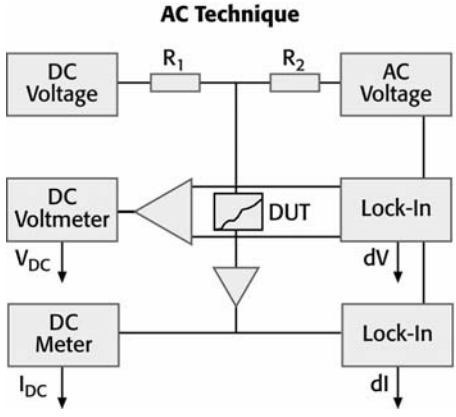


Figure 14.21 The ac technique for obtaining differential conductance can use as many as a half dozen components, making it far more complex setup than the *I-V* curve method. However, there is a reduction in the amount of noise introduced into the measurement.

frequency and increases noise. In addition, multiple instruments are susceptible to problems of ground loops and common-mode current.

Mixing the ac and dc signals is a significant challenge. It is sometimes done with series resistors and sometimes with blocking capacitors. With either method, the current through the DUT and the voltage across the DUT are no longer calibrated, so both the ac and dc components of the current and voltage must be measured. A lock-in amplifier may provide the ac stimulus, but frequently the required ac signal is either larger or smaller than a lock-in output can provide, so an external ac source is often required and the lock-in measurements must be synchronized to it.

The choice of frequency for the measurement is another complicating factor. It is desirable to use a frequency that is as high as possible, because a lock-in amplifier's measurement noise decreases at higher frequencies. However, the DUT's response frequency usually limits the usable frequency to 10 to 100 Hz, where the lock-in amplifier's measurement noise is 5 to 10 times higher than its best specification. The DUTs response frequency is determined by the device impedance and the cable capacitance, so long cabling, such as that used to attach to a device in a cryostat, reduces the usable frequency and increases noise, further reducing the intended benefit of the ac technique. Above all, the complexity of the ac method is the biggest drawback, as it requires precise coordination and computer control of six to eight instruments, and it is susceptible to problems of ground loops and common-mode current noise.

Another challenge of this method is combining the ac signal and dc bias. There is no one widely recognized product that addresses this

issue. Often, many instruments are massed together in order to meet this requirement. Such instrumentation may include a lock-in amplifier, ac voltage source or function generator (if not using the reference in the lock-in amplifier), dc bias source, dc ammeter, and coupling capacitor/circuitry to combine ac source and dc bias. In many cases, what researchers are really trying to do is source current, so the series resistors used to combine the ac and dc must be higher impedance than the device, which is unknown until the measurement is made.

Simple, Low-Noise Solution

Fortunately, there is another technique for differential conductance measurements that is easy to use and provides low-noise results. This improved method uses a four-wire, source current/measure voltage methodology. It requires a precision instrument that combines the dc and ac source components (stimulus), and a nanovoltmeter for the response measurements. The current sources combine the dc and ac components into one source, with no need to do a secondary measure of the current, because its output is much less dependent on the changing device impedance (Fig. 14.22).

With these instruments, an ac current is superimposed on a linear staircase sweep. The amplitude of the alternating portion of the current is the differential current, dI (Fig. 14.23*A*). The current source is synchronized with the nanovoltmeter by using a Trigger Link cable. After measuring the voltage at each current step, the nanovoltmeter calculates the delta voltage between consecutive steps. Each delta voltage is averaged with the previous delta voltage to calculate dV. Differential conductance, dG, is then derived from dI/dV (Fig. 14.23*B*).

Benefits of the Four-Wire, Source *I*/Measure *V* Method

This new method provides low noise results at least 10 times faster than previous methods. Only two instruments and a single sweep are required. When user-defined currents are small, the performance of

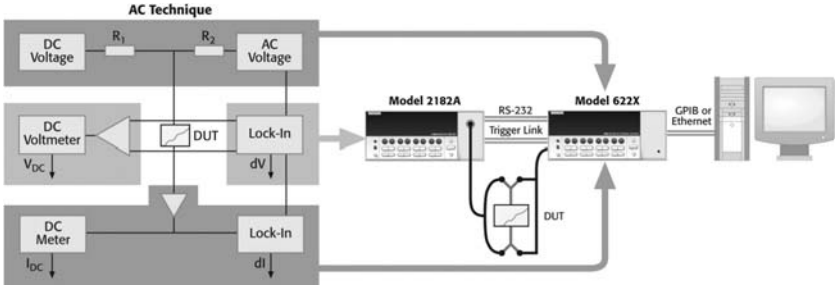


Figure 14.22 The ac technique (*left*) vs. the technique utilizing an ac/dc current source and a nanovoltmeter.

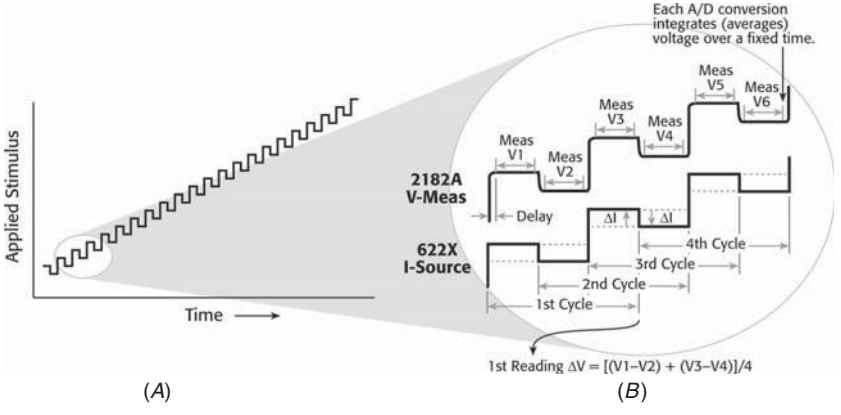


FIGURE 14.23 (*A*) Applied current during differential conductance sweep. (*B*) Detail of applied current and measured voltage.

instrumentation described earlier cannot be duplicated by any user-assembled system in terms of source accuracy, noise, and guarded measurements (the last being used to reduce dc leakage and improve system response time). Ac current can be sourced accurately, even below 10 pA. The nanovoltmeter has a sensitivity superior to lock-in amplifiers, low $1/f$ noise, and automatically compensates for offsets and drift. The four-wire connections eliminate voltage drop errors due to lead or contact resistance, because there is no current flowing through sense leads. This is important when the DUT has regions of low or moderate impedance.

Another key benefit is that more data points can be collected in areas of highest conductance (i.e., areas of greatest interest) by sourcing the sweep in equal current steps. Because of the instrumentation's inherently low source and measurement noise, only one pass is required, shortening data collection time from hours to minutes. Furthermore, the instruments' active guard eliminates the slowing effects of cable capacitance, greatly improving device settling time, measurement speed, and accuracy.

Special Cases

Some devices have nonmonotonic I-V curves. This behavior is classified as follows:

1. Current hop: A given voltage may correlate to more than one possible current.
2. *Negative differential conductance* (NDC): A given current may correlate to more than one possible voltage.

With a slight modification, the source current/measure voltage differential conductance method can be used with devices that exhibit these behaviors.

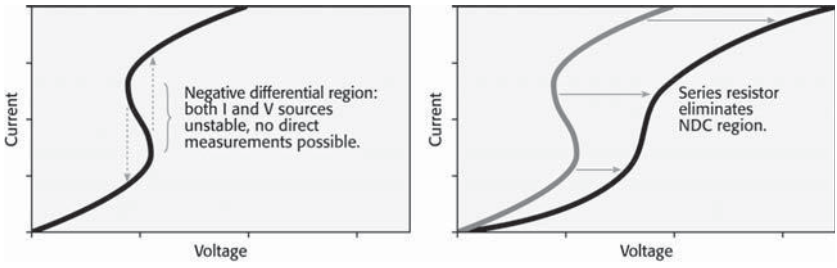


Figure 14.24 (*A*) Devices with negative differential conductance regions require special treatment. (*B*) The gray curve shows the device voltage as seen by the nanovoltmeter. The black curve shows the voltage across the device plus the series resistance as seen by the current source—no NDC region to create instability.

Current Hop Some devices exhibit an *I*-*V* curve where the current is a multi-valued function of voltage (Fig. 14.24*A*). The negative differential conductance (NDC) region cannot be characterized by applying a voltage source, because any regulated voltage source is unstable into negative resistance loads. Instead, a voltage source would produce a hysteresis curve that never traces out the NDC region (dashed lines in Fig. 14.24*A*). Interestingly, a current source is not stable over this NDC region either, but adding a series resistor in the HI lead presents a composite device to the current source, so that it does not see any NDC region. This resistance must be at least as large as the largest negative resistance throughout the NDC region of the device.

Without any change to the current source/nanovoltmeter setup, the entire differential conductance curve can be measured because the four-wire configuration connects the nanovoltmeter directly across the device and not the series resistor, whose voltage drop is rejected along with all other lead resistance. This lead resistance, which is normally considered a problem, actually makes full characterization possible with these devices.

Negative Differential Conductance If the *I*-*V* curve exhibits voltage that is a multivalued function of current, again, neither voltage nor current sources are stable over the NDC region. To stabilize this measurement, it is necessary to add a parallel resistor. The resistance should be low enough that the slope of its *I*-*V* curve exceeds the maximum slope of the negative resistance region of the device's *I*-*V* curve. That is, the resistance must be smaller than the smallest negative resistance throughout the NDC region of the device. If the chosen resistor is small enough, the slope of the combined *I*-*V* response will always be monotonic. The *I*-*V* curve traced out is now the sum of both *I*-*V* curves (Fig. 14.25*B*). Because we are measuring differential conductance, the conductance of the parallel resistor ($1/R$) can be simply subtracted from every measurement in the sweep.

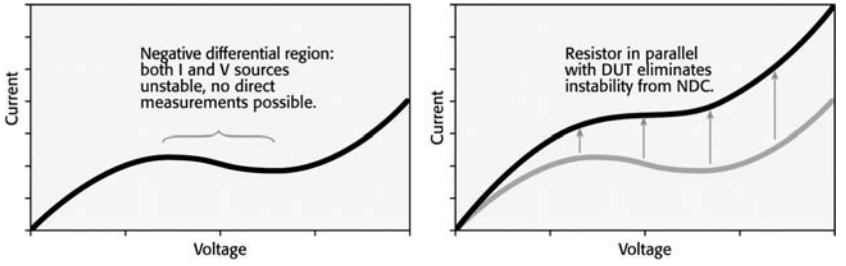


FIGURE 14.25 Even when the device shows multiple possible voltages for some currents, differential conductance can easily be obtained with the new method.

14.3.5 Counting Electrons: How to Measure Currents in the Attoampere Range

Nanoscale materials hold promise for areas such as medicine, homeland security, defense, and many other industries. Researchers in labs all over the globe are investigating the physical and electrical properties of nanoscale components as in *single-electron transistor* (SET) and quantum-dot research. This reduction in the physical size of the material under investigation creates new problems, particularly the difficulty of measuring electrical parameters such as resistance, voltage, and current accurately.

To keep pace, test and measurement instruments and techniques have had to adapt to the changing needs of researchers. Already, improvements in instrumentation make it fairly simple to measure currents of a few picoamps, and electrometers with femtoamp-level current sensitivity have been available for some time. However, measuring currents in the range of 10 aA or less is a different matter. After all, one attoamp (1×10^{-18} A) represents just six electrons per second.

Once, measuring such low currents required the use of expensive test equipment and cryogenic current comparators. Today, however, it is possible to measure changes in current as small as 1 aA at room temperature using commercially available test and measurement equipment. This discussion looks at a simple setup and technique for making repeatable and reliable measurements at the attoamp level.

Equipment Required

Making current measurements on the attoamp range requires a device that can measure currents with a few tens of attoamps of RMS noise in the range of 0.1 to 0.01 Hz and a current source with a resolution better than 1 aA. Source-measure units contain a precision voltage source, a precision current source, a voltmeter, and an ammeter. There are very few commercial off-the-shelf instruments that can make these kinds of measurements. One such instrument, a Sub-Femtoamp Remote SourceMeter instrument, has an ultralow-noise current amplifier

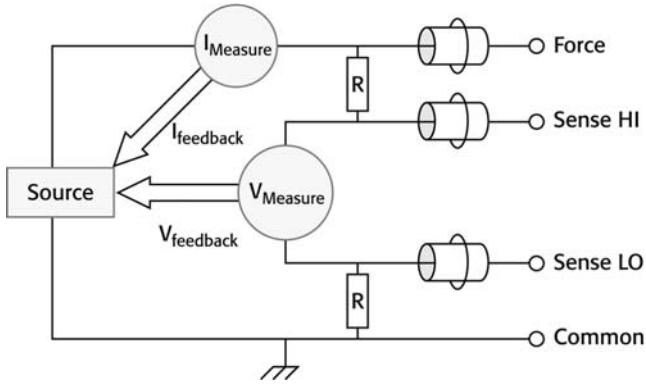


FIGURE 14.26 A source-measure unit includes a precision voltage source and a precision current source (shown here as one block), a voltmeter, and an ammeter.

and provides these functions in a single instrument. Figure 14.26 shows a typical SourceMeter instrument, with the source block representing both the voltage source and current source capability. The V_{measure} circle represents the built-in voltmeter, which gives feedback to the source block and can be used to control it. The I_{measure} circle represents the built-in ammeter; it, too, can control the source block. Note also that the instrument can provide both V_{measure} and I_{measure} functions simultaneously.

A good SMU can source very small currents, and a Sub-Femtoamp Remote SourceMeter instrument can source current with 50 aA resolution. For this application (counting electrons), a source capable of repeatedly producing 10 aA currents precisely is required. The voltage source within the Sub-Femtoamp Remote SourceMeter instrument was used to create a current source with this high resolution. To reduce the difficulty of working with extremely high-value resistors, the voltage source was first divided down by a factor of 10, then applied across a 2-TΩ resistor to the current measurement input (see Fig. 14.26). The result is 10 aA of current flowing with 200 μV applied. The 5-μV digital resolution of the source (programming resolution of the Sub-Femtoamp Remote SourceMeter) yields a 0.25 aA current resolution. It is important to recognize that this is not a true current source—its output current will be very sensitive to the load. The reason why it still works for this application is that the load is going to be a nearly perfect ammeter—that is, virtually a short circuit.

Making measurements with a few tens of attoamps of RMS noise in the bandwidth of 0.1 to 0.01 Hz required using a digital filter with a rise time of roughly 5 s. This meant that the standard deviation of 60 s worth of measured data did not exceed 100 aA. A remote preamp on

the Sub-Femtoamp Remote SourceMeter reduced cable noise, giving us 30 aA of rms noise.

Measurement Procedure

The simplest way to make attoamp current measurements is to alternate between measuring a positive signal, then a negative signal of the same magnitude, and repeatedly taking the difference. This method is still applicable, even if there is no way to generate a negative signal, by taking the difference between a positive signal and zero signal, although there is a factor of 2 noise penalty.

Current sources in typical nanotechnology applications are functions of time rather than constants, so we chose a current source that varies with time. In this case, the current took the form of a staircase function. The procedure involves taking a fixed number of readings at each step level for a total of N readings. The first of the series of readings taken with the positive source applied is averaged with the negative of the first in the series of readings taken with the negative source applied. In equation form, this is expressed as

$$I_{\mathrm{n}} = (I_{\mathrm{n}}^{+} - I_{\mathrm{n}}^{-})/2$$

The division by 2 comes about because the signal-to-noise ratio is the same in both signals, but there is twice the signal present in the full plus-to-minus signal. For signals with no negative component, the equation is identical except there is no division by 2. Doing this, for each of the readings in the series yields a series of difference readings. The whole process is repeated several times and averaged. Each difference series is averaged point-by-point, resulting in a single series of readings representing the current shape produced by the source.

Setting Up the Measurement

Choosing how fast to alternate between positive and negative sourcing requires some balancing. Faster alternations help minimize the effects of slow drifts in input current and also reduce noise. But, with teraohms of resistance in the source (which is typical for any source generating such small currents), the settling time is 1 to 2 s. If the source alternated every few seconds, most of the measurement would be of the source settling rather than the final dc value. One way to solve this is to let the source settle for 10 percent of the time after each alternation and measure for 90 percent of the time—which means a half-period of 10 times the settling time, or about 20 s.

Using this mathematical technique, the valid points from the current shape (i.e., the last 90 percent) were averaged to produce the final measurement. Estimating the error in this mean value required using the statistics of uncorrelated noise. Instead of one final current shape averaged from many difference series, N current shapes were generated. Each of these current shapes yields a mean from its valid data

points, so the collection of mean values has a standard deviation. Because the means are uncorrelated, the final answer, the mean of the N means, has a 1-sigma uncertainty equal to the standard deviation of the collection of means divided by the square root of N:

$$\sigma_{\bar{x}} = \sigma_x / \sqrt{N}$$

This was verified by generating 1,000 current shapes and plotting the standard deviations of the collections for $N = 1{,}000$, 500, 250, etc. As expected, the standard deviations of the collections dropped as the square root of the number of means in the collection.

Results

For the simplest case, using a single current value and using 40 s for each source polarity, after 1 h of measurement or 45 reversal pairs, the uncertainty was about 2.6 aA. After 12 h of averaging, the uncertainty fell to about 0.75 aA. After several such 12-h runs, the collection of results had a standard deviation consistent with 0.75 aA.

A good way to estimate the time required to achieve these results on an arbitrary system with unknown external noise sources is to measure the noise of the system in the 0.1 to 0.01 Hz bandwidth as described earlier. The test system, with the source on but constant, measured 60 aA rms in this bandwidth. If another system had 120 aA, it is reasonable to expect that each of the uncertainties achieved here could be done in approximately four times the amount of time.

Physical Precautions

The largest contributor to low-frequency noise in this sort of test setup is temperature variation. Instrument offset currents vary with ambient temperature, in this case, by less than 500 aA/°C. But even slow temperature changes from a building's heating and cooling systems could cause large current changes. One way of avoiding this problem is to simply place a cardboard box over the low-current amplifier and source fixture. Doing so nearly eliminates the problem. It is critically important that the low-current amplifier have low power dissipation (in this case, less than one-third watt) to avoid heat buildup in the enclosure.

Another concern is stray electrostatic fields. Housing the current-generating element (in this case, the source's resistors) in an electrostatic shield that is grounded for safety eliminates this problem. It is also possible to improve the settling time of the source by placing the current-generating element inside an inner electrostatic shield driven by the guard buffer.

Time-Varying Input

Using a slow staircase input instead of a simple dc signal shows that a discernable signal can be retrieved from the noise. After every

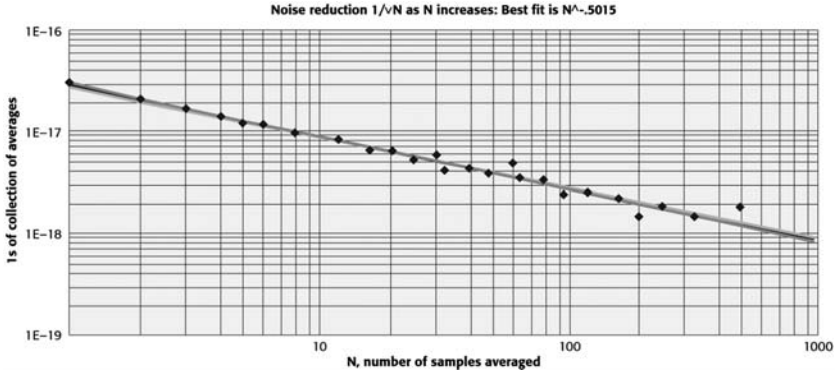


Figure 14.27 The graph depicts a plot estimating the uncertainty in the mean, which is ±0.8 aA.

90 measurements (about 18 s), the current source was incremented by 10 aA. Inverting the staircase generated the negative source period. The results are shown in Fig. 14.27.

Considering each step as a separate measurement and using the estimates described earlier, the mean of each current step has a 1-sigma uncertainty of 0.8 aA (Fig. 14.28). The measurement took 84 h, only slightly longer than the equivalent of five 12-h runs for five separate measurements. The extra time required to reduce the noise is expected. The longer alternation period allows offsets to drift more between the positive and negative measurements, so the residual noise is larger. This can also be described by noting that offset drift due to temperature change typically has a $1/f$ characteristic. That is, noise

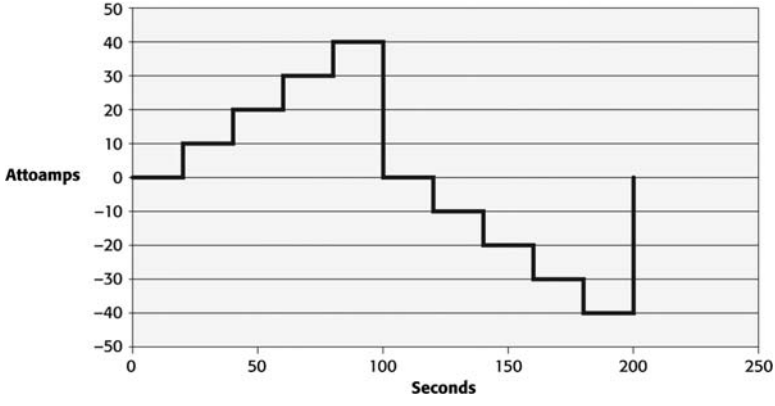


Figure 14.28 A graph of the staircase current waveform used in the experimental setup.

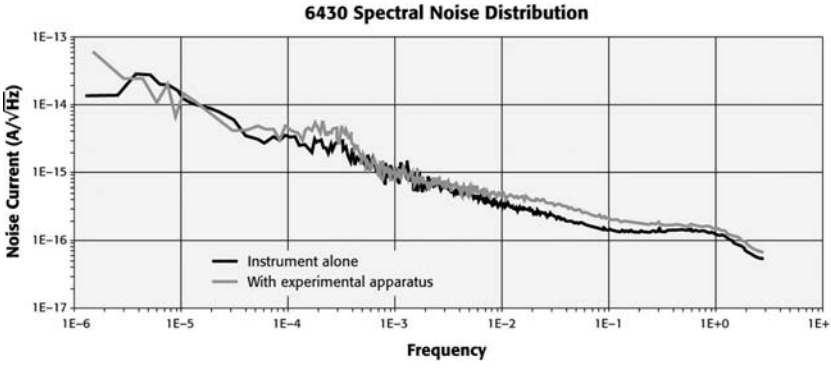


Figure 14.29 The noise spectrum of the experimental setup shows that noise decreases with increasing frequency.

current is inversely proportional to frequency (Fig. 14.29). So, although the current reversal process still narrows the bandwidth to 1/(12 h) (0.00002 Hz), the lower alternation frequency of the staircase places the measurement higher on the $1/f$ curve.

14.4 Electronic Transport Characteristics of Gallium Nitride Nanowire-Based Nanocircuits

To close out this chapter, I discuss research that was recently completed by one of my colleagues, Mary Anne Tupta, at Keithley Instruments, in conjunction with research performed at the Michigan State University by Dr. Virginia Ayres and her colleagues. The work presented here also received the "Best Student Poster" award at the IEEE Nano2006 conference held in Cincinnati, Ohio, in July 2006.

The work described here emphasizes why it is important to understand the many concepts of good electrical measurements in order to really understand what truly happens and the nanoscale. The research work involved electronic transport studies of a two-phase gallium nitride nanowire. The steps taken are briefly described here and discussed in detail later.

Current-voltage measurements were taken of gallium nitride–based three-terminal field-effect transistors fabricated via electron beam lithography. The measurements indicated a working field-effect transistor using a global back-gate configuration. Very high current levels within the nanowire were reported. Direct transport measurements were also taken via two nanomanipulator probes. High current levels in this experiment were also observed. Scanning probe recognition microscopy was used to detect the contact pad and nanowire radial boundary, and a nanowire autofocus experiment was reported.

14.4.1 Introduction

Over the past decade, nanowires and nanotubes made from a wide variety of materials have demonstrated extraordinary electronic, mechanical, and chemical characteristics. Gallium nitride (GaN) nanowires are particularly promising due to an inherently wide bandgap coupled with structurally induced electronic and optical confinement.[5] GaN-based nanocircuits have recently been shown to be viable for wide range of electronic and optical applications. GaN nanowire field-effect transistors[6–8] and logic devices[9] have shown the desired characteristics of high transconductance and good switching, and room-temperature UV lasing has been reported for GaN nanowire systems[10,11] as well as good field emission properties.[12]

Understanding the interactions of GaN nanowires within a nanocircuit architecture is critically important to maximizing the potential of the GaN nanowire building block. In particular, details of the electronic transport and carrier injection require fundamental elucidation. This discussion presents details of an investigation into electronic transport and carrier injection.

14.4.2 Materials and Methods

The approximately 50- to 100-nm GaN nanowires were grown in a direct reaction of metal gallium vapor with flowing ammonia at 850 to 900°C without a catalyst, as reported in Ref. 13. These had a two-phase coaxial zinc-blende/wurtzite structure, shown in Fig. 14.30 and reported in Ref. 14. A field-effect transistor design using a GaN nanowire as an n-type semiconducting channel was used in the experiment (GaNFET). The nanowires were dispersed on a highly doped p-type

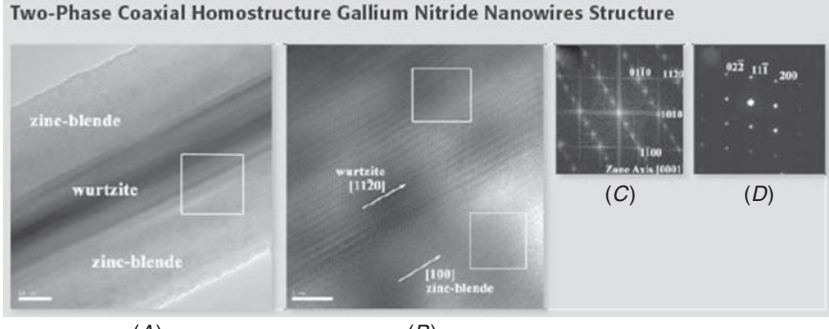


FIGURE 14.30 (*A*) TEM and (*B*) high-resolution TEM of two-phase coaxial homostructure GaN nanowires used in the experiments. The boxed area in (*A*) is shown in (*B*). Nanodiffraction, selected area electron diffraction, and fast Fourier transforms were used to identify (*C*) the inner phase as wurtzite and (*D*) the outer phase as zincblende. The two boxed areas in (*B*) are shown in (*C*) and (*D*).

silicon substrate covered with a 150-nm dielectric layer of thermally grown silicon dioxide. The GaNFET source and drain contacts were patterned using electron beam lithography, with Ti/Au used for the conducting source and drain material. The backside of the wafer was stripped of silicon dioxide using hydrofluoric acid, and Ti/Au was evaporated to form the global back gate.

Electronic transport characteristics were measured in two-point and four-point probe configurations using a Keithley 4200-SCS ultralow-noise electronic characterization system and a Keithley-Zyvex KZ100 nanoprobing system, in which specially sharpened ~30-nm radius tungsten nanoprobes were coupled with the 4200-SCS and experiments were performed under direct SEM observation.

These experiments were carried out at the corporate laboratories of Keithley Instruments (Cleveland, Ohio) and Zyvex Corporation (Richardson, Texas). Carrier injection was investigated using Scanning Probe Recognition Microscopy, a new scanning probe microscope modality under development by our group in partnership with Veeco Instruments, Santa Barbara, CA.[15]

14.4.3 Nanocircuit Electronic Transport Measurements

Current-voltage measurements were taken at Keithley Labs on a Keithley 4200-SCS, which offers very low-noise and low-current measurements. The Keithley 4200-SCS is uniquely suited for this application because high levels of noise can arise while analyzing the GaNFETs. See Fig. 14.31 Measurements indicate this FET has a good on-off ratio and is capable of handling high current. Currents measured in these devices approached 30 μA, which is similar to findings from other groups[16,17] and is very high considering the nanowire dimensions. The current density can thus be approximated as ~2.4 mA-μm^{-2}. Although the nanowire is capable of very high current densities, the gate voltages needed to achieve this are somewhat above accepted levels. A gate voltage step of –30 to 30 V was needed to clearly show current change based on gate voltage modulation. These gate levels, however, are not feasible in most devices. Other discrepancies include unpredictability of the device at negative drain-source voltages, where the gate-source voltage variation does not seem to affect the drain current as much. The reason for this anomaly is unknown at this time, but is being investigated further.

14.4.4 Nanowire Electronic Transport Measurements

Further two-point and point-to-point probe measurements were performed in the Keithley-Zyvex KZ100 nanoprobing system under direct SEM observation. The nanoprobe arrangement for the four-point measurements is shown in Fig. 14.32*A*. Placement of a probe tip resulted in the nanowire break. The probes labeled 2 and 3 were lifted

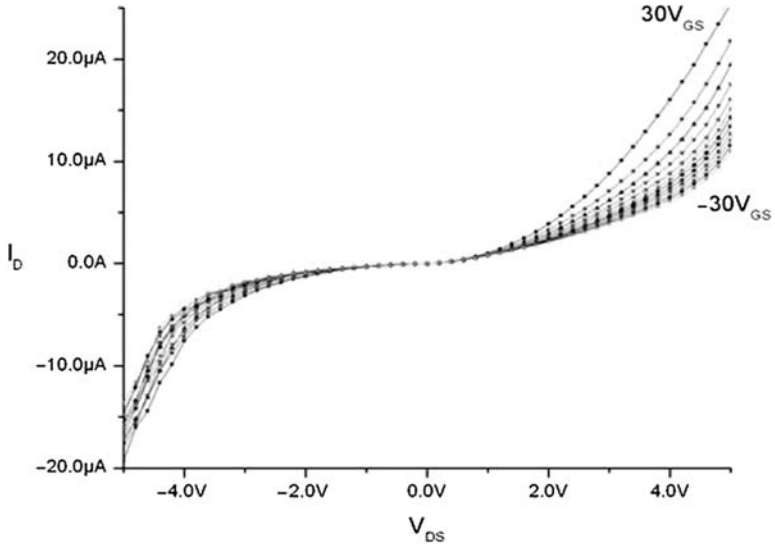


Figure 14.31 Current-voltage characteristics for a GaN nanowire FET showing the effect of gate-source and drain-source voltage variation.

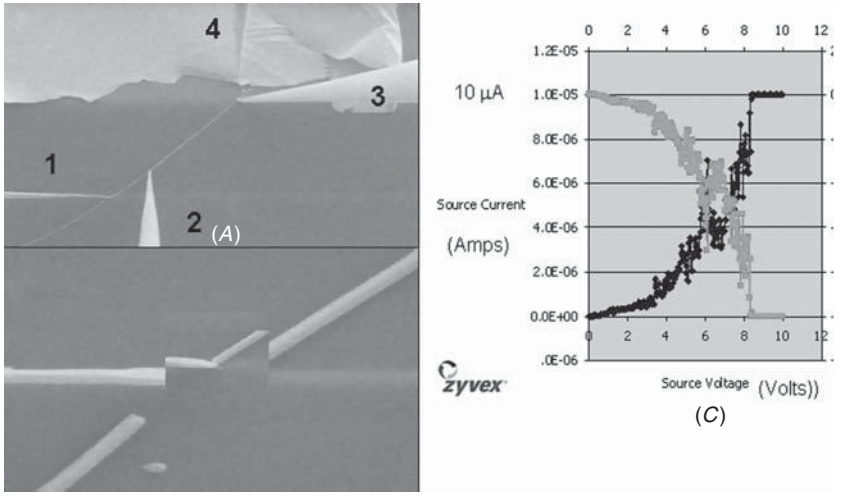


Figure 14.32 (*A*) Nanoprobe arrangement for the four-point measurements. (*B*) Probe 1 placed in direct contact with the cleaved nanowire open end. (*C*) Example high-current-density *I-V* characteristic.

out of contact with the nanowire, and the probe labeled 1 was placed in direct contact with the cleaved open end as shown in Fig. 14.32*B*. The probe labeled 4 remained on the gold contact pad as shown in Fig. 14.32*A*.

The current density to breakdown was then investigated. The results confirmed the high current capacity previously discussed. In a typical example, 10 μA of current was achieved, as shown in Figure 14.32*C*. Electrical breakdown with pull-apart in the middle of the nanowire occurred at greater than 50 μA. The gold contact pad near probe 4 did not display any sign of local heating.

14.4.5 Scanning Probe Recognition Microscopy of Nanocircuits

Scanning probe recognition microscopy (SPRM) is a new scanning probe microscope modality under development in partnership with Veeco Instruments, Santa Barbara, California.[15] In SPRM, we give the *scanning probe microscope* (SPM) system itself the power to return to a specific nanoscale feature of interest through feature recognition coupled with adaptive scan plan generation and implementation. It is a recognition-driven and learning approach, made possible through combining scanning probe microscope piezoelectric implementation with online image processing and dynamically adaptive learning algorithms. The human operator interaction is now focused on the decision-making level, rather than the execution level.

SPRM has been implemented in the main atomic force and scanning tunneling modes. The SPRM experiments are performed on a specially adapted Multimode Nano-scope IIIA (Veeco Instruments) in ambient air. For the nanocircuits investigation, several aspects of the GaNFETs are currently under investigation, which require the ability to autofocus the scan path to proceed from the conducting contact pad onto the semiconducting GaN nanowire, while avoiding the insulating oxide layer.

Our implementation, shown in Fig. 14.33, uses real-time captured information to detect the contact pad (user-defined region), the contact pad–nanowire linear junction, and the nanowire radial boundary. Our current implementation also has an adaptive learning capability with statistical methods that can be used in boundary detection adjustment to improve accuracy.

The resulting nanowire autofocus using SPRM is shown in Fig. 14.33. The image captured by the SPM is shown in Fig. 14.33*A* (dotted lines are used to artificially enhance the low-relief contact pad boundaries). The scan plan generation, shown in Fig. 14.33*B*, shows that our scanning scheme can detect and predict boundaries reliably. Thus, we can scan back and forth only on the region of interest, which starts from the left side (light points) and ends with the right side (black

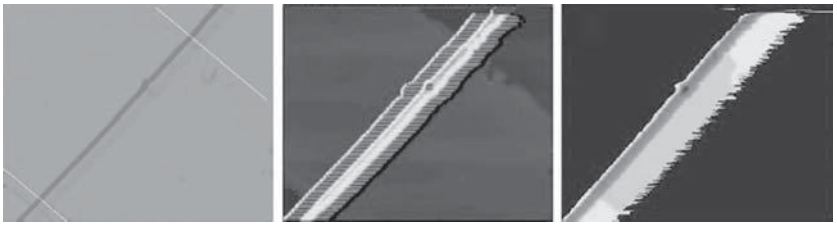


Figure 14.33 Scanning scheme implementation for GaN nanocircuit. (*A*) Image captured by standard SPM. The contact region boundaries are delineated by white dotted lines. The image size is 5 μm $\times$ 5 μm. (*B*) Scanning scheme showing lines of the scan plan. (*C*) Real-time image captured by SPRM system using the autofocused scanning scheme along the nanowire. The height variation at the contact regions is also visible.

points) in Fig. 14.33*B*. We can see that the scanning scheme can follow changes of boundaries very well because of the adaptive learning algorithm. The captured real-time autofocused image is shown in Fig. 14.33*C*. This is a still image from an .mpg movie clip of the top to bottom autofocused scan that starts from a small region on the contact pad and proceeds along the nanowire. The regions that are not actually scanned are padded with 0 (dark gray region) for display.

14.4.6 Discussion

The GaN field-effect transistors reported here may be a viable solution in many electronic devices. The high current density that these nanowires can achieve may be desirable in high-current, high-power applications. The device itself, however, needs to be improved so as to lower gate-source voltage levels, thus making this device design more practical. Optical applications are also being realized, and the biphasic nature of these nanowires may provide an optical confinement element similar to optical fibers. The possibility of carrier and exciton confinement in these nanowires may provide a wide variety of electronic device applications.

14.5 Conclusion

The science of nanotechnology is a far-reaching research topic that requires multidisciplinary skills from physics to materials science to chemistry to biology. In each discipline, a variety of potential applications and products are being researched and developed that can have a significant impact on a large number of industries. Anything from sensors, drug delivery systems, and stronger, lighter materials to the next generation of faster and smaller "beyond CMOS" electronic components will be the new innovations from nanoscience

research and will be the driver of future economies. Characterizing these nanoscale components and materials is far from trivial as many exhibit low-current, low-resistance, high-resistance, and low-power electrical properties.

To meet the challenges of nanoscience, researchers must conduct a variety of measurements, including current vs. voltage characterization, resistance, resistivity and conductivity, differential conductance, transport, and optical spectrum and energy measurements to unravel the complexities of matter at the nanoscale and to make reliable, commercializable products based on nanomaterials. To reach this end, scientists, researchers, and engineers will require sensitive electrical measurement tools and an understanding of electrical measurement principles.

This chapter has offered a practical set of best measurement practices to making precision low-level dc and pulse measurements on nanomaterials and devices. The information presented provides an aid to understanding low-level phenomena observed in the lab and theoretical and practical considerations involved in measuring low currents, high resistances, low voltages, and low resistances.

Acknowledgments

Keithley gratefully acknowledges the assistance of Dr. V. M. Ayres of Michigan State University, who granted permission to reprint Ref. 15, which received the "Best Student Poster" award at IEEE Nano2006, held July 17–20, 2006, in Cincinnati, Ohio.

References

1. *Bioimpedance Bioelectricity Basics*, New York, Wiley, 2003.
2. IBM Research Division, "Single and multiwalled carbon nanotube field effect transistors," *Applied Physics Letters*, vol. 17(73), Oct 1998.
3. "*I-V* measurements of nanoscale wires and tubes with the model 4200-SCS and Zyvex S100 nanomanipulator," Application Note no. 2481, Keithley Instruments, 2004.
4. "Four-probe resistivity and Hall voltage measurements with the model 4200-SCS," Application Note no. 2475, Keithley Instruments, 2004.
5. J. C. Johnson, H.-J. Choi, K. P. Knutsen, R. D. Schaller, P. Yang, and R. J. Saykally, "Single gallium nitride nanowire lasers," *Nature Materials Letters*, vol. 1, p. R106, 2002.
6. Y. Huang, X. Duan, Y. Cui, and C. M. Lieber, "Gallium nitride nanowire nanodevices," *Nano Letters*, vol. 2, p. R101, 2002.
7. E. Stern, G. Cheng, E. Cimpoiasu, R. Klie, S. Guthrie, J. Klemic, et al., "Electrical characterization of single GaN nanowires," *Nanotechnology*, vol. 16, p. R2941, 2005.
8. J. M. Barker, K. A. Bertness, and N. A. Sanford, "Electrical measurements of GaN nanowires deposited using electric-field assisted alignment," paper presented at the 6th International Conference on Nitride Semiconductors, Tu-P-123.

9. Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K. H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, p. R1313, 2001.
10. F. Qian, S. Gradecak, Y. Li, C. Wen, and C. M. Lieber, "Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes," *Nano Letters*, vol. 5, p. R2287, 2005.
11. S. Gradecak, F. Qian, Y. Li, H.-G. Park, and C. M. Lieber, "GaN nanowire lasers with low lasing thresholds," *Applied Physics Letters*, vol. 87, R173111, 2005.
12. C.-C. Chen, C.-C. Yeh, C.-H. Chen, M.-Y. Yu, H.-L. Liu, J.-J. Wu, et al., "Catalytic growth and characterization of gallium nitride nanowires," *Journal of the American Chemical Society*, vol. 123, p. R2791, 2001.
13. M. He, P. Zhou, S. N. Mohammad, G. L. Harris, J. B. Halpern, R. Jacobs, et al., "Growth of GaN nanowires by direct reaction of Ga with NH_3," *Journal of Crystal Growth*, vol. 231, p. 357, 2001.
14. V. M. Ayres, B. W. Jacobs, M. E. Englund, E. H. Carey, M. A. Crimp, R. M. Ronningen, et al., "Investigation of heavy ion irradiation of gallium nitride nanowires and nanocircuits," *Diamond and Related Materials*, vol. 15, pp. 1117-1123, 2006.
15. V. M. Ayres, L. Udpa, and A. Rice, "GOALI: Scanning Probe Recognition Microscopy," Award Abstract No. 0400298. Available at www.nsf.gov/awardsearch/showAward.do?AwardNumber=0400298.
16. H.-Y. Cha, H. Wu, M. Chandrashekhar, Y. C. Choi, S. Chae, G. Koley, et al., "Fabrication and characterization of pre-aligned gallium nitride nanowire field-effect transistors," *Nanotechnology*, vol. 17, p. R1264 (2006).
17. C. Y. Nam, J. Y. Kim, and J. E. Fischer, "Focused-ion-beam platinum nanopatterning for GaN nanowires: ohmic contacts and patterned growth," *Nano Letters*, vol. 5, p. R2029, 2005.

CHAPTER 15

Nano ESD: Electrostatic Discharge in the Nanoelectronic Era

Steven H. Voldman

15.1 Introduction

A new era is opening again, as semiconductors transition from microelectronics to nanoelectronics with new questions, and uncertainties. As we enter the nanoelectronic era, the devices are getting smaller, but the interest in *electrostatic discharge* (ESD) phenomena is getting larger.[1–5] The semiconductor industry has invested 40 years in the manufacturing of *complementary metal oxide semiconductor* (CMOS) technology, but what about the future? One of the driving forces for this interest in ESD is the concern over how to manufacture these new nanostructures without the destruction associated with static charge and electrostatic discharge events. To coin a new field name, "nano ESD" is of great global interest and concern as we enter the nanostructure world.[1,6–9] Will static charge affect nanostructure reliability, or the ability to manufacture them or introduce them into the marketplace? Where are we going? Are there solutions to future ESD problems? Will ESD sensitivity prove to be dependent on the type of structure and technology?

The following sections provide examples of various technologies ranging from photomasks to nanowires. The chapter first discusses examples of ESD failures where air gaps or open surfaces are present in these devices, which are also either mechanically static or mechanically dynamic structures. The focus of the chapter includes photomasks, magnetic recording devices, and microelectromechanical

machines (MEMs), but the subject is relevant to all electrostatically actuated and suspended structures (e.g., capacitors, and inductors). The chapter will then discuss silicon devices, from bulk CMOS to silicon-on-insulator (SOI), and modern nanostructures FINFETs and nanowires.

15.2 Photomasks

Photomasks are used in the formation of semiconductor devices. A photomask serves as the negative image of the desired structure to be created on the semiconductor wafer for printing purposes. A photosensitive material is formed on the wafer surface to produce the desired shape or structure. The photomask is used to expose the material, and leads to hardening of the photosensitive material. In photolithography, there is both positive tone and negative tone resist. Photomasks are typically formed using a quartz substrate, with chrome shapes on the physical surface. The production of the photomasks must be "defect free." If a defect occurs, this can lead to latent failure mechanisms and product failure.

One of the key problems is the buildup of electrostatic charge on the mask shapes. Between each chrome shape on the mask, a potential "spark gap" exists that can lead to electrical discharge when the electric potential exceeds the air breakdown. In the formation and handling of the photomasks, charging issues can lead to damage of the chrome lines.[10–19] This occurs when a differential voltage is established across the photomask, either globally or locally. In the case of local damage, a differential voltage can be established between two adjacent chrome lines. The differential voltage can be dependent on the amount of charge buildup on each structure. If the physical regions are of different physical size, or shape, then the charge collection can be different leading, to a differential voltage. Electrical breakdown can occur as either a surface breakdown or bulk air breakdown event.

Figure 15.1 shows an example of ESD discharge as a function of the spacing between two shapes on a photomask. In the figure, the failure damage indicates that the chrome material melted as a result of current flowing between the two physical shapes after electrical breakdown.[4,6,10,19] Figure 15*A–E* shows the electrical discharge as a function of gap spacing (for spacing of 1.5, 2, 2.5, 3, and 4 μm, respectively).[4] At a gap spacing of 4 μm (Fig. 15.1*E*), no damage is evident between the edge of the two chrome lines. At this gap spacing, there is evidence of onset of topography change on the upper corner of the line. In Fig. 15.1*D*, at a gap spacing of 3 μm, there is little damage evident between the edge of the two chrome lines; in this case, there are changes in the topography of the end of the line and the vertical line. In Fig. 15.1*C*, at a gap spacing of 2.5 μm, both corners and the

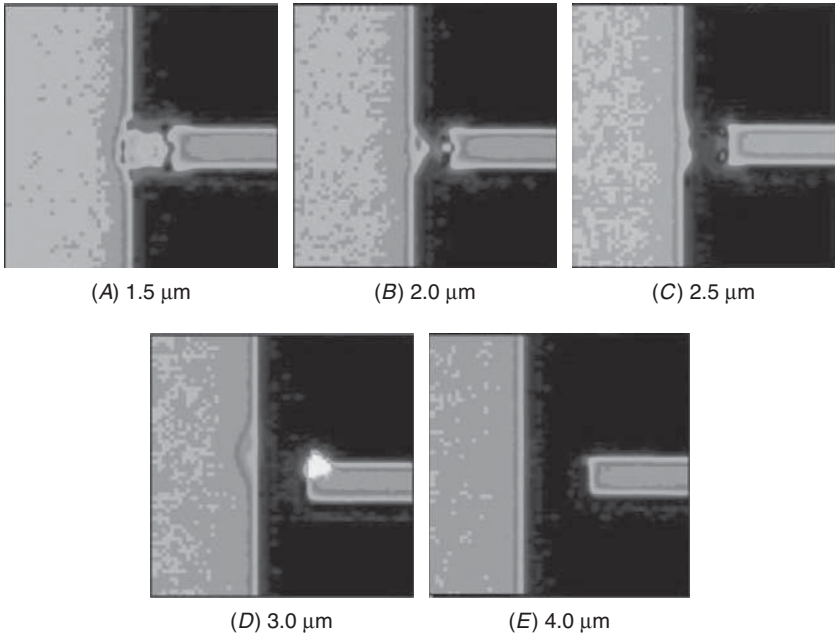


Figure 15.1 (*A–E*) Photomask damage as a function of spacing.

end of the chrome line are actively involved in the discharge process. For smaller spacings, the damage level is evident in the gap between the vertical line and the end of the chrome line.

The avalanche phenomenon is important to understand the breakdown process in air and other materials. Townsend, in 1915, noted that the breakdown occurs at a critical avalanche height,

$$H = e^{\alpha d} = \frac{1}{\gamma}$$

In this expression, the avalanche height H is equal to the exponential of the product of the probability coefficient of ionization (number of ionizing impacts per electron and unit distance in the direction of the electric field) and electrode spacing. The avalanche height H can also be expressed as the inverse of the probability coefficient of regeneration (number of new electrons released from the cathode per positive ion). The results of F. Paschen showed that the breakdown process is a function of the product of the gas pressure and the distance between the electrodes. Paschen showed that

$$pd \approx \frac{d}{l}$$

where p is the pressure, d is the distance between the plates, and l is the mean free path of the electrons. From the work of Paschen, a universal curve was established that followed the same characteristics independent of the gas in the gap. The Paschen curve is a plot of the logarithm of the breakdown voltage as a function of the logarithm of the product of the pressure and gap distance:

$$V_{\mathrm{BD}} = f(pd)$$

At very low values of the pd product, electrons must accelerate beyond the ionization limit to produce an avalanche process because the likelihood of impacts is too small. In this region, the breakdown voltage decreases with increasing value of the pressure-gap product. This occurs until a minimum condition is reached. At very high values of the pressure-gap product, the number of inelastic collisions is higher and the breakdown voltage increases. This U-shaped dependence is characteristic of gas phenomena. At the high gas pressure, secondary processes, such as light emissions occur. In another form, in air,

$$p\lambda = 5 \times 10^{-3}$$

where p is in units of torr, and λ is in centimeters. At a pressure of 1 atm, the mean free path, λ, is 0.066 μm. The energy accumulated at one mean free path is 30 eV; this translates to the energy needed to initiate avalanche breakdown. Converting to the electric field, and voltage, this is equivalent to an electric field of $E = 30\ \mathrm{V}/0.066\ \mu\mathrm{m}$, or roughly $480\ \mathrm{V}/\mu\mathrm{m}$. Hence, according to the Paschen theory, for breakdown in air (e.g., no surfaces) the breakdown voltage is less than 500 V for gap spacings less than 1 μm. Paschen showed that a breakdown relationship exists that is a function of the product of pressure and spacing. In our present-day and future devices, the region of interest is in the U-shaped section of the Paschen curve where the breakdown voltage increases at smaller spacings. As we continue to make smaller line widths for nanoelectronics, the spacing between lines also is reduced, leading to electrostatic nanodischarges occurring between the mask shapes.

The electrical response of these elements are also a function of the electrical parameters of the structure. An electrical model can be established to quantify the ESD event in photomasks.[10,19] The event model can be depicted as a first and second chrome feature on a substrate. An air gap is between the two chrome features. The ground reference is the back of the reticle. The chrome features form a capacitor between the chrome shape and the back reference plane. The capacitance of the two chrome features can then be defined associated with the total area of the chrome feature, and the thickness of the quartz substrate wafer. The resistance of the chrome feature is a function of the feature

sheet resistance and the geometric parameters. The inductance of the chrome line is associated with the inductance per unit length. The capacitors, C_1 and C_2, are the capacitors associated with the chrome feature and the substrate for the first and second chrome feature, respectively. The resistance and inductance are also the parameters for the two adjacent structures. In this representation, the capacitance and the arc resistance across the gap are not included in the model; this model assumption is valid for small gap regions, or when the gap capacitance and resistance is much smaller than the other capacitor and resistor terms. Note, in this representation, when the air gap conduction occurs, all the elements in the circuit are in a series configuration, forming an RLC response. J. Montoya, L. Levit, and A. Englisch showed that this representation could be fit to the oscillation observed during electrostatic discharge.[10,19] The current in the discharge process can be represented as a decayed sinusoidal oscillation. The current is a function of the impedance. The impedance is the frequency times the sum of the two inductors (e.g., $Z = \omega\,(L_1 + L_2)$).[10,19]

$$I(t) = \frac{V}{\omega\{L_1 + L_2\}} e^{-\alpha t} \sin\{\omega t\}$$

The decay rate is associated with the equivalent R/L decay, where the equivalent resistance is the sum of the two resistors, and the equivalent inductance is the sum of the two inductors (e.g., $(R_1 + R_2)/(L_1 + L_2)$),

$$\alpha = \frac{1}{2}\left\{\frac{R_1 + R_2}{L_1 + L_2}\right\}$$

The frequency of oscillation can be obtained from the Kirchoff's voltage loop, with a characteristic oscillation,[10,19]

$$\omega = \left\{\alpha^2 + \left(\frac{1}{C_2} - \frac{1}{C_1}\right)\left(\frac{1}{L_1 + L_2}\right)\right\}$$

The response in the electrical discharge is associated with the sum of the two inductances, the sum of the two resistances, and the capacitance to the substrate ground plane. As a result, the RLC response is a function of the mask shapes (e.g., length and width), as well as the gap distance. The air gap distance also determines the voltage at which the breakdown occurs.

The discharge itself leads to melting of the chrome wires, which can lead to mask defects in the semiconductor chip. As the spacing decreases, these nanodefects are harder to observe in mask inspection. Figure 15.2 shows an *atomic force microscope* (AFM) image of a chrome damage that can lead to latent defects. These nanodefects may prevent

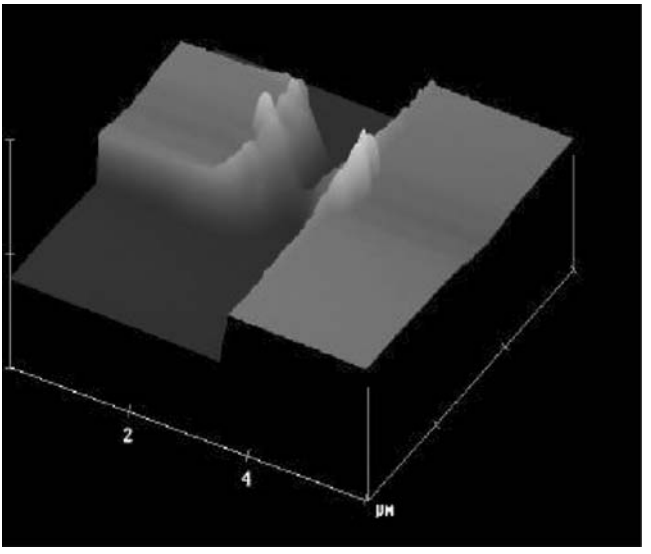


Figure 15.2 AFM image of latent defects in photomasks.

the ability to manufacture structures without yield loss. Hence, it is of interest to address the manufacturing inspection process for future nanostructures.

Figure 15.3 shows the AFM image of the ESD defect between the two masks. As is evident, the material from the mask exists between the two physical shapes.

15.3 Magnetic Recording

The magnetic recording industry uses a small thin-film *magnetoresistor* (MR) to sense the magnetic field as the disk spins under the magnetoresistor mounted on a "magnetic head." To continue to scale down the size of disk drives, and to pack in as much areal density of information as possible, the MR industry continues to evolve the MR head device to smaller structures. The industry migrated from MR heads, to the *giant magnetoresistors* (GMRs), and presently the *tunneling magnetoresistor* (TMR).

ESD and *electromagnetic interference* (EMI) have become a significant concern in the magnetic recording industry.[4,20–28] Today, magnetic recording industry devices are the most ESD-sensitive elements being manufactured; as a result, there is significant interest in how to manufacture a "Class 0" device. One of the primary reasons for low ESD robustness is there are no ESD devices or structures in hard disk drives to protect these elements.

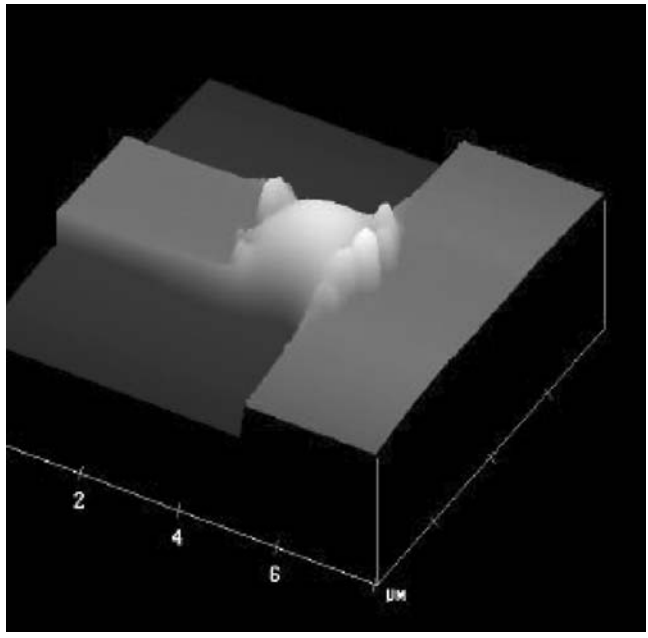
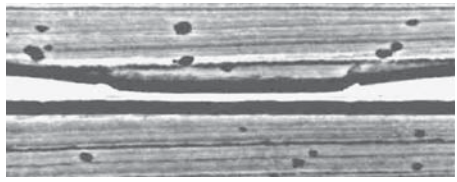


Figure 15.3 AFM image of ESD defects in photomasks.

In these devices, there are significant number of electrical, magnetic, and aerodynamic failure mechanisms. There are also material changes of state, as well as electrical circuit states (e.g., initialization). Figures 15.4*A–E* shows an example of ESD failure damage in an MR head structure as a function of resistance degradation shift.[20] As the defect changes in the MR stripe, the series resistance of the MR stripe changes. This impacts the magnetic characteristics of the MR film. The agglomeration of the MR device also changes the aerodynamic characteristics, as the MR stripe "flies" over the disk in the disk drive. Head-to-disk "crashes" can also occur, leading to disk drive failures.

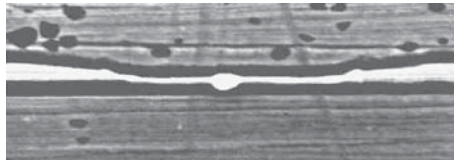
Microbreakdown can also occur between the magnetoresistor and adjacent shields and substrates.[20] Along the surface, breakdown can occur leading to damage of the MR stripe and the physical surface.

A second fundamental mechanism in MR heads is ESD failure between the MR stripe and the adjacent magnetic shield structures. As in the photomasks, an electrostatic breakdown can occur across the surface between the two adjacent structures. In the MR head, the MR shields provide magnetic shielding from stray magnetic signal away from the MR stripe. As the signal levels decrease, the MR shields are placed closer to the MR stripe to enhance the MR stripe signal levels. Similar to the photomask, there is an air gap along the *air-bearing surface* (ABS), where the MR stripe and MR shields are separated at the



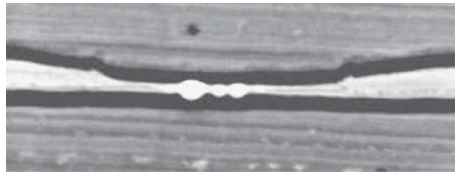
ΔR = 1%,

(*A*)



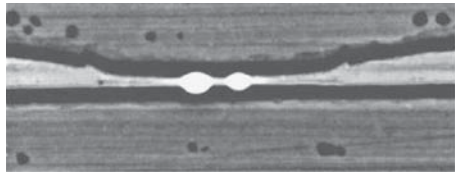
ΔR = 2%,

(*B*)



ΔR = 3%

(*C*)



ΔR = 4%

(*D*)

ΔR = 15%

(*E*)

Figure 15.4 (*A–E*) MR stripe ESD failure damage and corresponding resistance shift.

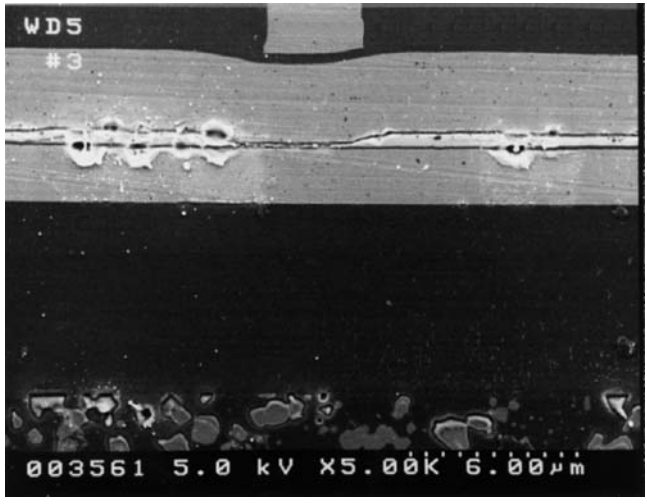


Figure 15.5 ESD damage mechanism of MR stripe to shield.

air surface. Figure 15.5 shows an example of the ESD failure between the MR stripe and the adjacent MR shields.

In this magnetic recording industry evolution, the size and film thickness are reduced to sense smaller signals; as a result, the *human body model* (HBM) ESD "robustness" decreased. In 1993, the HBM ESD sensitivity of the MR head was 150 V HBM levels. With the introduction of the GMR head, the HBM sensitivity level reduced to 35 V. This was followed by the introduction of the TMR head, whose failure levels were less than 10 V HBM. How highly charged can a human being become? People have been measured at voltages as high as 35 kV. Semiconductor components are designed typically to survive 2-kV (HBM) levels.

Today, the TMR is one of the most ESD-sensitive nanoelements being manufactured.[4,28] The TMR device is teaching semiconductor manufacturing how to build, ship, and assemble supersensitive devices, leading the way toward what the nanotechnology world will need in the future. Figure 15.6 shows the ESD damage of a TMR device.[28]

15.4 MEMs

Microelectromechanical (MEM) structures are being developed for a large range of applications from basic electrical components, microengines, and micromirrors.[4,7,29–38] For motors, MEMs are being used as "energy scavengers" converting the energy of mechanical vibration to electrical energy. MEM electrical components include capacitors,

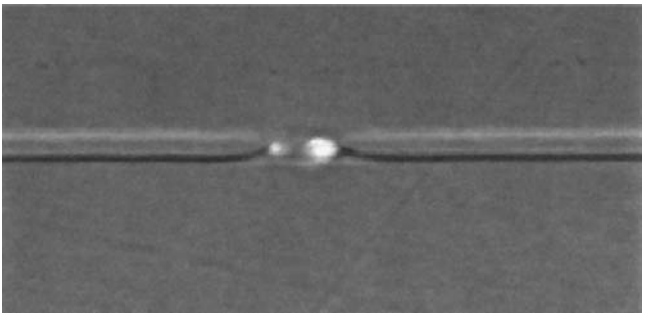


Figure 15.6 Tunneling magnetoresistor (TMR) ESD failure damage.

inductors, and switches.[4] MEMs are also being used as arrays of micromirrors.[35–38] Today, a wide range of applications are being explored, from electrical, biomedical, consumer, multimedia, hand-held electronics, and energy to military needs. A key issue that is unique and common to all these devices in the majority of MEM structures is as follows:

- MEM structures contain air gaps.
- MEM structures contain air cavities or suspended structural elements.
- MEM structures have moveable elements.
- MEM structure mechanical motion is initiated by electrostatic fields (electrostatically actuated).

As a result, the failure mechanisms of MEM structures are a function of both electrical failure and mechanical failure.[4,7,29–38] Mechanical failure can consist of creep, fatigue, wear, and "stiction." The failure of operation of a MEM structure can be associated with structural damage impeding the motion of the moveable elements. Electrical failure can be associated with surface or air gap breakdown. The electrical breakdown can lead to structural melting, electrostatic deflection, or damage to the structure; this may manifest itself as associated with resistance, capacitance, or inductive change in the operation of a MEM device. Electrical failure can be related to changes in the device dc or ac parameters or leakage current as well. Today, not all ESD failure mechanisms have been demonstrated in all MEM application spaces. Much of the observations and knowledge of these MEM ESD failures can be transferred to other MEM applications, such as MEM inductors and MEM capacitors.[4]

MEMs pose a new challenge because many of these nanoelements are electrostatically actuated. How does one avoid electrostatic

discharge problems in an electrostatically actuated element? How does one avoid electrostatic discharge in the air gaps and suspended structures? As in the photomask, electrical charging can occur between two closely spaced elements. In MEM structures, segments of the elements are closely spaced, with a gap between to provide the electrostatic actuation. As a result, an electrical spark can occur in the gap leading to melting of the component, at times causing them to "stick" together. In these MEM structures, both functional impacts and "stiction" can occur.

In electrostatically actuated devices, ESD failure is a function of a number of issues. A first failure mechanism is electrical breakdown. Electrical breakdown can occur across the air gap between the actuation source and the physical structure or membrane in the device. As discussed previously, the Paschen curve discusses the relationship between the breakdown voltage and the gap size. An interesting feature of the electrostatically actuated devices is that as the mechanical motion occurs, the gap size varies during operation. A unique difference between field emission devices (FEDs), spark gaps, magnetic recording heads (e.g., AMR, GMR, TMR, and *colossus magnetoresistor* [CMR]), and photomask structures is that in the MEM structure, the gap is variable. This gap variation is dependent on the following:

- Electrical state (e.g., actuated, nonactuated, or in a switch transition state)
- Residual charge (pre- and post-ESD events)
- Mechanical deformation (e.g., prestrained condition)
- Electric field (pre- and post-ESD events)

For the electrical state, the structure can be "open," "closed," or in a switch transition state. In this case, the gap dimension will be different. In the case that the gap space is small, material displacement can lead to "stiction," in which melting between the two surfaces can create a merging of the two structures, preventing operation. In photomasks, it serves as a defect; in MEM structures, it prevents operational function of the MEM device. The mechanical "spring constant" of the structure also influences whether or not the structure restores itself after discharge (e.g., the stiffness of the structure influences the return response).

Residual charge can lead to changes in the "initial state" of the structure, influencing the gap spacing prior to an ESD event. This "precharge" produces an electric field, inducing displacement or deflection of the structure. Hence, preconditioned states (both electrical and mechanical) lead to smaller gap spacings as well as an initial electric field, which will influence the HBM, machine model (MM), and transmission line pulse (TLP) results.

Mechanical deformation, due to prestrain conditions or nonelastic deformation, can also lead to change in the position of the actuated device. Hence, the mechanical initial state leads to smaller gap spacings as well as an initial electric field, which will influence the HBM, MM, and TLP results.

15.4.1 Micromotors

Micromechanical engines will be valuable in the future in a wide range of applications.[29,30] An example of a microengine contains gears and linear actuators. The microengine has a rotating gear. The gear rotates around a hub assembly that is attached to the substrate. The rotating gear is mechanically connected to linear actuators. The micromachine has an orthogonal comb drive; these "comb drives" contain a first set of stationary comb fingers, and a second set of grounded comb fingers. The first set is a stationary set of comb fingers that is electrically insulated from electrical ground. The second comb fingers is a grounded comb mechanically attached to a moveable shuttle structure. Springs suspend the shuttle above the ground plane and serve as an electrical ground potential.

J. Walraven of Sandia laboratories first addressed ESD damage concerns in a micromotor.[29,30] Figure 15.7 shows an example of a

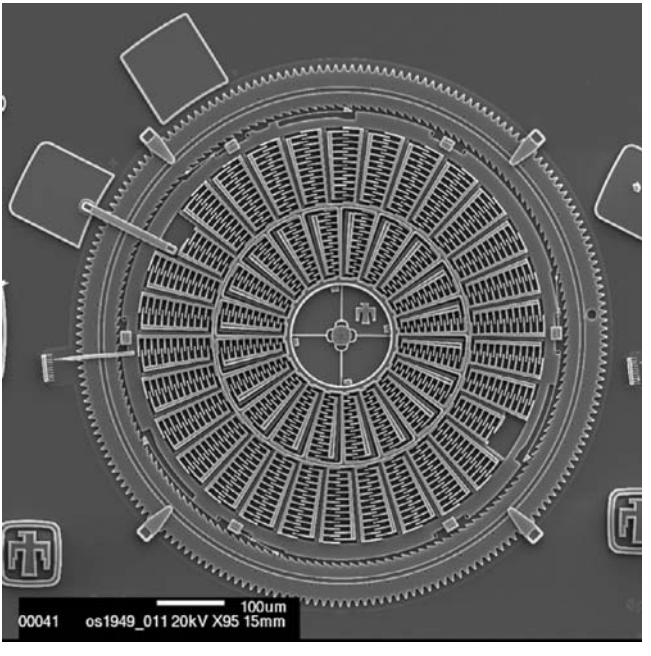


Figure 15.7 Torsional ratcheted actuator (TRA).

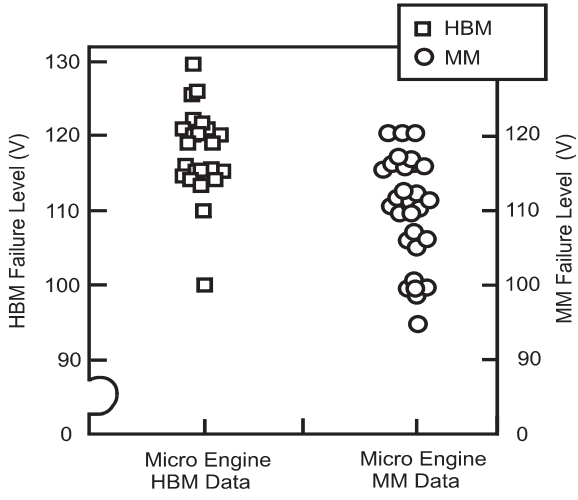


Figure 15.8 Torsional ratcheted actuator (TRA) HBM and MM ESD results.

torsional ratcheted actuator (TRA) (developed by Sandia National Laboratories). Sandia National Laboratories have been exploring the reliability of these motors from an electrostatic perspective. Electrostatic discharge testing was completed to evaluate the failure mechanisms. J. Walraven noted the existence of damage to the gear rotation and "stiction" of the motor elements. "Nanowelding" was observed from the current of the ESD event. Another reliability is the residual particles that are left after a discharge process can interfere with mechanical rotation of elements.

J. Walraven et al. showed that these actuators had an HBM ESD failure level of 100 to 130 V (HBM).[29,30] Additionally, the MM ESD failure levels were 95 to 120 V (MM)[29,30] (Fig. 15.8). In semiconductor devices, typically the ratio of HBM-to-MM ESD results is between 5:1 and 20:1. In semiconductor devices, this failure ratio is very dependent on current density and temperature to failure. But in these microengines, the failures are associated with the breakdown voltage across air gaps. Hence, the failures are more similar to spark gaps, photomasks, and magnetic recording devices than ESD failures observed in semiconductor components.

Failure analysis showed that the ESD failure mechanism is associated with second-layer polysilicon comb fingers adhering to a first-layer polysilicon ground plane. An electrical discharge occurred between these two polysilicon layers, leading to molten polysilicon at the region of failure. The electrical failure signature was determined by Thermally Induced Voltage Alteration (TIVA) analysis. TIVA analysis was verified with SEM analysis; ESD failure occurred at the polysilicon comb finger. Charged device model (CDM) testing of these structures

demonstrated that the failure levels exceeded 1,000 V (CDM); some actuators exceeded 2,000 V (CDM) with no evidence of failure.[29] In these microengines, the operational structures are not contained within the silicon substrate; these structures are electrically isolated from the substrate wafers and are less vulnerable to bulk-silicon semiconductor devices. Failure analysis verified that no damage was observed between the fixed or moveable comb fingers to the substrate. In some cases, the polysilicon damage was observed on the polysilicon comb structures; in the case where there was no adherence, the microengine was still functional. Hence, evidence shows that in some structures, although there is silicon or polysilicon damage, if the damage does not lead to physical adherence, the microengine can still maintain functional operation. But, if the discharge process leads to adhesion or "welding" of the two physical structures, the microengine cannot operate.[29,30]

15.4.2 MEMS—RF Switches

For RF applications, RF MEM switches have advantages over conventional switches. For the electrical state, the structure can be "open," "closed," or in a switch transition state. In these cases, the gap dimension will be different. ESD can be a concern in these electrostatically actuated switches.[31–34] In the case that the gap space is small, material displacement can lead to "stiction," in which melting between the two surfaces can create a merging of the two structures preventing operation. In photomasks, it serves as a defect; in MEM structures, it prevents operational function of the MEM device.

A. Tazzoli studied the impact of ESD on RF MEM switch devices.[31,34] As noted by Tazzoli,[31,34] the "spring constant" of the structure also influences whether or not the structure restores itself after discharge (e.g., the stiffness of the structure influences the return response). Mechanical deformation, due to prestrain conditions or non-elastic deformation, can also lead to change in the position of the actuated device. Hence, the mechanical initial state leads to smaller gap spacings as well as an initial electric field, which will influence the ESD results.

A second issue is the mechanical failure of structural elements (e.g., broken structure). In the case of structural elements, mechanical deformation can be evaluated using solid mechanics "beam theory." A structural element can be regarded as a beam structure with a given cross-sectional area. An example of understanding the beam deflection is a function of the support. For the example of a cantilever structure, it can be assumed that a force exists that is distributed across the beam length, where the force pulls the beam toward a planar surface. An electric field can be formed between the beam structure and the surface, leading to the applied force on the beam structure. The beam displacement is associated with the magnitude of the force, the beam length, the beam thickness, and the Young's modulus of the

beam material. The magnitude of the force is a function of the gap size between the beam and the surface (e.g., defining the electric field that is established).

A model used for MEM structures to evaluate beam displacement is the Osterberg model. The model evaluates the voltage needed to have the end of the cantilever element to touch the surface. This voltage is known as the collapse voltage. The collapse voltage where the beam deflects to the surface is

$$V_c = \left\{ \frac{16Et^3g_o^3}{81\varepsilon l^4} \right\}^{1/2}$$

where E is the Young's modulus (in units of megapascals), t is the beam thickness, g is the gap between the cantilever beam and the surface, ε is the permittivity of air, and l is the length of the beam. Broken physical elements can lead to residual materials within the air gap, influencing functional operation or electrical shorting.

Figure 15.9 shows an example of an RF switch, with an RF "input" (RF(IN)), an RF "output" (RF(OUT)), and an actuating bridge

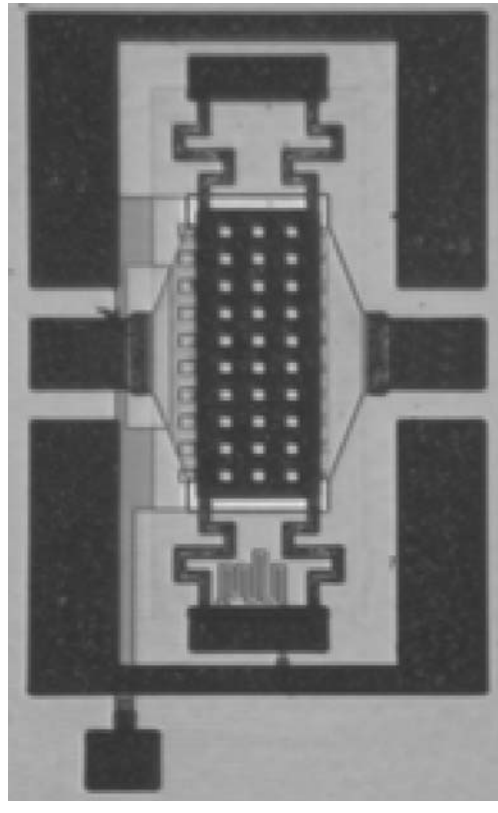


Figure 15.9
Radiofrequency (RF) switch.

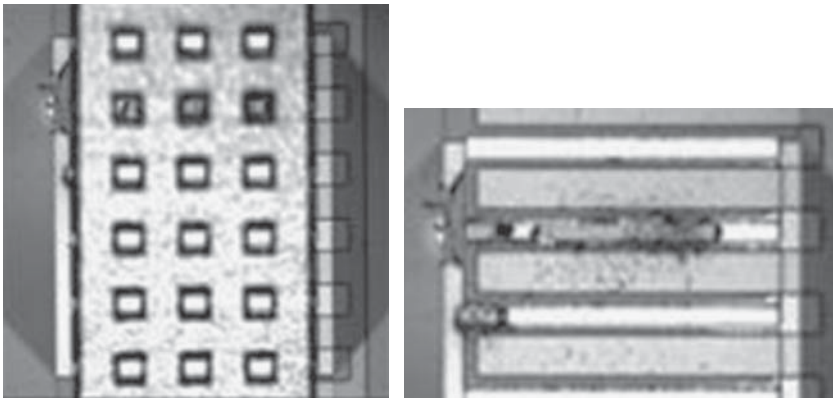


Figure 15.10 Radiofrequency (RF) MEM damage after a ESD event.

structure. In these RF MEM switches, ESD events influence the mechanical motion as well as influence the RF S-parameters.[31,34] Figure 15.10 shows the damage of the RF MEM switch after ESD stress. The ESD damage can manifest itself between the RF(IN) and RF(OUT), as well as actuator to RF input or output signals. Additionally, the ESD current can lead to "nanowelding" of the elements in the switch element, impacting its functionality, as was observed in micromotors.

15.4.3 MEMS—Micromirrors

Micromirrors have present-day and future applications in systems. Optical MEM systems contain electrostatically actuated micromirror structures.[35–38] These micromirror elements can be used in a wide range of applications that utilize coherent or incoherent light. For coherent light applications that utilize lasers, the MEM structure can be used for read heads in disk drives, laser printers, bar-code readers, and scanning machines. As a result, for hand-held or nonportable applications, these micromirror systems have significant value. Using an electrostatic actuator, the micromirror can be tilted by the capacitive coupling between the mirror and the pad on the silicon substrate. In these structures, the actuation voltage influences the tilt angle; the tilt angle is a function of the actuation voltage. As was shown in the other MEM applications, ESD failures can occur. In micromirrors, the uniqueness is that the deflection and bending of the element is critical to the application. In the MEM switch, it influences the "open" or "closed" state of the switch; hence, it is digitized, whereas the MEM micromirror is "analog" in nature.

Figure 15.11 is an SEM of the micromirror array after ESD testing. A mirror can be one of the plates of a capacitor element. Micromirrors can have a supporting beam in the center and a "left and right" capacitor plate on each side. By applying an electric field, the electrostatic

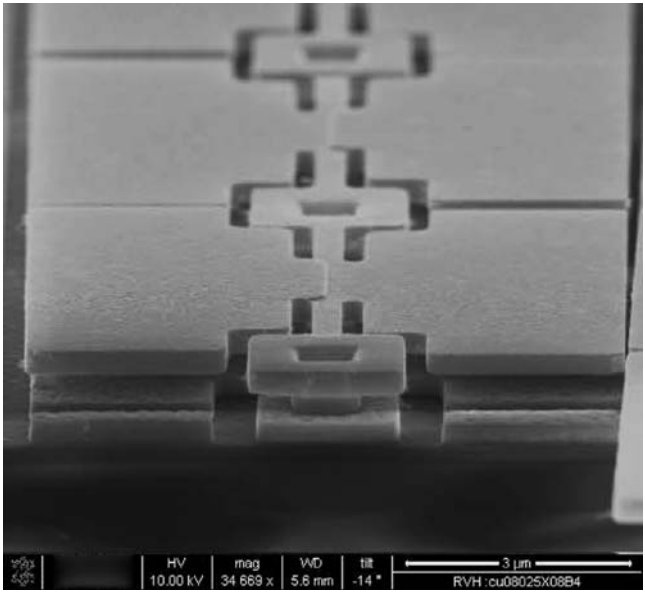


Figure 15.11 Micromirror structure.

attraction can lead to a tilting of a mirror element, like a "see-saw." The tilt angle is a function of the applied electric field. Micromirrors also exhibited ESD concerns. ESD events can lead to damage between the mirror and the actuator; this can lead to distortion of the tilt angle and rotation of the micromirror structures. In an array of micromirrors, mirrors are separated by small gaps. ESD events can occur between the mirrors due to discharge events, leading to damage of the mirror surface.[38]

As in the RF MEM switches, the ESD damage can impact the mechanical motion, and system response. In the micromirror array, ESD damage leads to reduction of the tilt angle of the structure. As the actuation voltage was increased, tilting of the micromirror still occurred, but the range of tilt angle was significantly impacted by the magnitude of the ESD event (e.g., impacting its functionality). HBM ESD testing was performed for different size micromirrors, in both single and array configuration. It was noted by S. Sangameswaran et al. that one of the failure mechanisms in a microarray is associated with failures between the adjacent micromirrors.[38] Between adjacent mirrors, an air gap exists, forming a "spark gap," which can lead to mirror-to-mirror ESD failures.

15.5 Transistors

In silicon technology, there have been both evolutionary and revolutionary transitions in the semiconductor transistor as it has been

scaled to smaller dimensions. Semiconductor dimensional scaling has gone from micrometers to nanometers over the past 30 years, where MOSFET constant electric field scaling has influenced the ESD robustness of the transistor.[1–5] In semiconductor devices, there has been a transition in the semiconductor wafer from low doping concentration to high doping, and once again to low–doped wafers.[39,40] In well design, technology evolved from single tub, to dual-well, to triple-well; this evolution was influenced by both semiconductor process equipment (e.g., MeV implantation), to semiconductor device requirements, isolation (e.g., latchup requirements), and device offerings (e.g., low-voltage and high-voltage devices). In isolation technology, it has evolved from *recessed oxide* (ROX), to *local oxidation* (LOCOS), and presently *shallow trench isolation* (STI) to provide improved topography and dimensional scaling.[39–42]

In the transistor junctions, technology evolved from single implants, to L_{DD}, to extension implants. Today, using silicon germanium (SiGe), strain engineering can be applied to change the mobility by introducing regions of tensile or compressive states. With mechanical strain, the spacing of the lattice atoms can be modified to vary the collision frequency of free carriers with the lattice atoms. Mechanical strain can also be introduced using films over the gate structure that introduce compression and tension along the silicon surface.

The interconnect system must also scale with the silicon transistor to integrate the interconnects to the MOSFET device; to achieve this, innovation in the planarity and metallurgy was introduced. Planarity was achieved using *chemical mechanical polishing* (CMP). In the metallurgy, revolutionary changes occurred in the metal films and the via contact structures, by transitioning from aluminum to copper-based interconnects, where this transition changed the ESD robustness of semiconductors.[43–46] For semiconductor chip performance, low-*k* dielectrics were introduced to lower the capacitance and line-to-line coupling of the interconnects; this also influenced the ESD robustness of the interconnects.[47] Today, *through silicon vias* (TSVs) have been introduced for multichip modules, stacked chips, and increased functional bandwidth.

15.5.1 BULK vs. SOI Technology

To achieve continued performance objectives and remain on the Moore's law curve, it was believed that MOSFET junction capacitance was a performance impediment. *Partially depleted silicon on insulator* (PD-SOI) was introduced to serve as a natural evolutionary change from the "bulk CMOS" transistor. A concern with SOI technology was the ability to achieve ESD protection and migrate bulk CMOS applications into SOI applications, without degradation of the ESD robustness of products.[1–5] ESD development began in 1991 to

demonstrate the ability to offer SOI as a mainstream replacement for bulk CMOS technology. After years of work, it was found that it is possible to provide ESD robust products in SOI.[48,49] This work opened the door for semiconductor development and provided a dilemma as well. The question for technology was whether they choose the path of bulk CMOS or SOI technology for high-performance, advanced technology. As we migrate to 22-nm and sub-22-nm technology, both are being explored as candidates for advanced CMOS.

15.5.2 FINFETs

As the silicon transistor scales from a micron technology world, to the nanodevice world, it is believed that semiconductor devices must achieve two paradigm shifts: first, introduce fully depleted transistors, and second, extend into the third dimension.

In semiconductors, to pack more transistors into more space and to provide higher performance, the transistor is leaving the two dimensional (2D) wafer and becoming more three-dimensional (3D). New 3D devices known as FINFETs (also referred to as *multiple gate field effect transistors* [MUGFETs]) are being proposed for the future CMOS technologies.[50–52] The name *FINFET* comes from the 3D vertical elongated "fin" structure of silicon from the wafer surface. Multiple-gate and wraparound-gate structures are of interest for advanced development for the desire to increase the current conduction in a MOSFET transistor per unit area. For density improvements, exploratory work in the 45-nm and 32-nm technology generations have been initiated. In the 22-nm or a future SOI technology, the possibility of usage of the fully depleted SOI transistors and SOI FINFET transistor is very likely.

Today, these transistors are being demonstrated in 45-nm technology with potential usage in the future. In these structures, the MOSFET gate "wraps around" all sides of the "fin." Each "fin" is physically isolated from the adjacent fins with a common gate extending over all fins perpendicular to the flow of the current. Figure 15.12 shows an example of a FINFET structure. Instead of a planar device surface, the FINFET is segmented into vertical pillars of silicon. The MOSFET gate wraps around the "fin" structure on three sides, meandering up and down over the parallel fin structures. The FINFET consists of parallel nanochannels to conduct the MOSFET current. ESD measurements have been reported in these FINFET transistors, providing new challenges relating to how to design and optimize the new transistors.[39,40] From a nanostructure perspective, the nanochannels influence the "electrostriction" that occurs in a planar device, quantizing the current constriction into a number of parallel channels.

ESD failure of FINFET structures is of interest because of the interrelationship of the FIN width and the nature of current

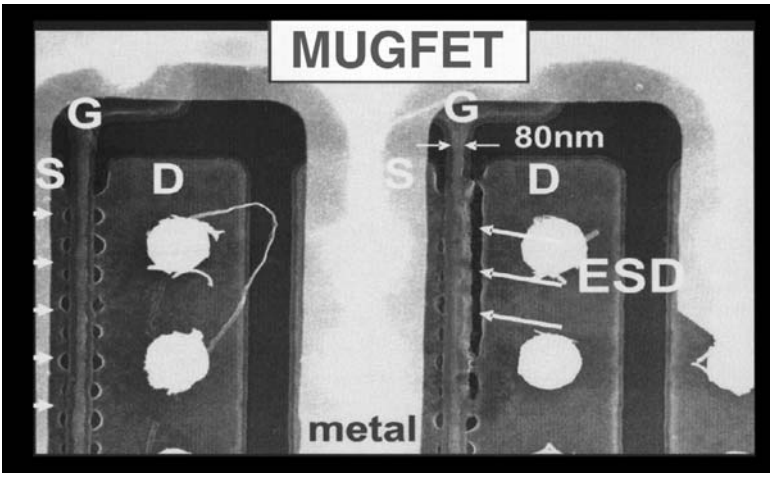


Figure 15.12 FINFET structure ESD failure damage.

electroconstriction.[1] In planar MOSFETs, the lateral current constriction across the MOSFET width has prevented the ability to predict the width scaling of the MOSFET structure during a high current state. In the FINFET structure, the FINFET is significantly smaller than the current constriction, leading the current to distribute across multiple fins.

C. Russ et al. demonstrated the first experimental work on ESD failure of a SOI FINFET structure. TLP I-V characteristics of 320 parallel fins for 150- and 90-nm-length FIN structures that have a fin width of 50 nm were evaluated.[50] A second study shows a second TLP I-V characteristic of 500 parallel fins for 250- and 120-nm lengths. ESD failure occurs at the FINFET TLP I-V I_{t2} current level. In the FINFET structure, at the ESD failure level, many of the FINFET channels are displaced as a result of the ESD event. Note that the ESD failure occurs in adjacent FINFET channels and are not randomly distributed through the structure.

These FINFET structures can be used in a diode configuration as well as a MOSFET configuration.[50] TLP I-V characteristics were compared for a planar SOI lateral diode versus a SOI FINFET structure. The response of the TLP FINFET diode structure was similar to that of the planar diode structure. In this investigation, the planar SOI lateral diode had a lower on resistance compared to the SOI FINFET diode structure.[50] In the diode-configured FINFET structure, at the ESD failure level, many of the diode SOI FINFET channels are displaced as a result of the ESD event. Note that as was shown in the prior MOSFET structure, ESD failure occurs in adjacent FINFET channels and is not randomly distributed through the structure.

15.6 Silicon Nanowires

As semiconductor devices continue to scale, there is interest in nanowires for both current conduction, and switches. *Nanowire* (NW) structures may be used in future applications in the sub-20-nm technology generation. Silicon nanowires have been demonstrated with 15-nm gate length and 4-nm radius.[53] The silicon NW can serve as a MOSFET structure that is fully depleted because the MOSFET gate structure surrounds the nanowire on all sides.[53]

A roadblock to practical implementations of these structures is the ability to survive ESD events. Experimental work has already begun to understand the ESD robustness of the silicon nanowire. The first reported ESD results were published in September 2009 by W. Liu and coworkers.[55] TLP testing was completed on NW structures that were varied in the number of parallel wires and the nanowire channel length. First, ESD results increased with the number of parallel nanowires. Second, as the nanowire channel length decreased, the TLP current increased. Using 100 parallel nanowires, the critical current to failure of the structure occurred at 20 mA. For 70 parallel channels, as the channel length decreased from 2 to 0.4 mm, the critical current-to-failure increased from 7 to 18 mA.[55]

15.7 Carbon Nanotubes

Carbon nanotubes (CNTs) are of significant interest to the nanostructure world.[1,56] CNTs are being proposed for future electronic applications, with significant amounts of research and development. CNTs may serve as circuitry on both the periphery and interior of circuit applications. Some of the questions to be asked include: How do we protect CNT circuitry? How do we build ESD protection circuits out of CNTs? Can we conduct the current using carbon nanowires? Will they have significant value for constructing ESD networks?

A reason for the ESD concern is to make sure that electrostatics do not interfere with the mainstream introduction of nanotubes into the manufacturing and the marketplace. If nanotubes and nanowires are to be a reality in future products, we must be able to establish practical techniques for manufacture processing, shipping, and handling of these components.

The reason for the interest is also the great potential of nanowires in their current-carrying capabilities! If we can learn how to harness the nanowires' advantages, tremendous advantages may be only just ahead of us. The search for ever faster, lower-power-consumption and thus smaller electronic devices is leading to structures having geometries of width and length smaller than current semiconductor image forming technology can generate. Of particular interest are structures formed from carbon nanotubes such as quantum dots, CNT wires,

and CNT field-effect transistors (CNTFETs). Circuits constructed using CNTFETs and CNT wires will require ESD protection, and structures and methods for providing such protection are virtually unknown. Accordingly, there exists a need for compatible CNT diodes and ESD circuits for protecting CNT-based electronic devices.

Carbon nanotubes are closed-cage molecules composed of sp^2-hybridized carbon atoms arranged in hexagons and pentagons. Carbon nanotubes come in two types: single-wall nanotubes, which are hollow tubelike structures, and multiwall nanotubes. Multiwall carbon nanotubes resemble sets of concentric cylinders. Single-wall- and multiwall-domain carbon nanotubes produce quantized conduction characteristics that are significantly different from those of standard electronics. The breakdown characteristics provide unique behavior that will be of interest from a functionality, reliability, and ESD perspective. Using two doped CNTs, a p-n diode can be formed to serve as a protection device. As noted by Jia Chen of IBM T. J. Watson Research, orientation and physical area of the CNTs will influence the capability of the cross-point CNT.[56] For example, a CNT diode includes a first CNT extending first in a lengthwise direction from a catalytic nanoparticle and electrically contacted by a metal contact at an end opposite the end in contact with the catalytic nanoparticle. A CNT diode also includes a second CNT extending in a second lengthwise direction from a catalytic nanoparticle and electrically contacted by a metal contact at an end opposite the end in contact with the catalytic nanoparticle. CNTs can lie in two different but parallel planes that are both parallel to a plane defined by a top surface of an insulating layer. Catalytic nanoparticles are, in one example, iron/cobalt (Fe/Co) or iron/cobalt/nickel (Fe/Co/Ni) when CNTs are formed by *chemical vapor deposition* (CVD) from carbon-containing gases, for example, a carbon monoxide (CO) and hydrogen mixture.

Today, there still remains an open question of the future of CNT ESD robustness, and whether ESD will be an impediment to CNT integration into modern-day electronic systems. Hence, it is not clear at this time whether ESD robustness of the CNT is a future advantage or disadvantage. There is significantly more work ahead to answer this question.

15.8 Conclusions

As the dimensional scaling of devices approaches the nanometer dimensions, all devices will have to address the implications of static charge, ESD, *electromagnetic interference* (EMI), and *electrical overstress* (EOS). This will be true in photomasks, magnetic recording devices, semiconductor devices, and nanowires to nanotubes.

In photomasks, magnetic recording devices, and MEM structures, there are unique failures that occur in these structures because of the presence of gaps, cavities, and floating structures. These structures in many cases are mechanically static, such as photomasks, where others are electrostatically actuated. It was shown that the ESD failure is associated with the voltage of the structure exceeding the functional electrostatic actuation voltage; this can lead to melting, fusing of moveable elements, mechanical failure, and damage to the device. In the case of mechanically static devices, such as photomasks, the residual material affects the imaging process. In the case of mechanically dynamic devices, the residuals can lead to failure of mechanical operation. Given that the yield stress of the moving structure is exceeded, mechanical damage occurs, and particle elements and broken elements ensue. A key discovery in these structures is that there is little difference between the HBM and MM results; in air gap-based failure mechanisms, the failure is associated with the voltage breakdown of the air gap; this is very different from silicon-based diode and MOSFET structures.

Additionally, many of the mechanically actuated devices are electrically isolated from the supporting substrate, leading to high CDM voltage levels. Again, this is very distinct from the silicon-based device elements and is more akin to ESD failures observed in MR heads, and photomasks. Additionally, for very short pulses, the ESD pulse width is significantly smaller than the spring constant response time of the mechanical structures. It is also clear that the failures are associated with voltage levels that exceed the functional operational voltage; MEM structures are vulnerable to voltages outside of the functional regime that can lead to air breakdown or mechanical deflections outside of the allowed range of electromechanical operation.

The challenge to silicon devices is how to maintain robustness of semiconductor components as performance objectives continue to increase. As can be seen, the migration to nanostructures may not be as difficult as anticipated based on the early experimental results on silicon nanowires.

In summary, if the nanostructure is small, and exposed to external sources, then it is a candidate for a concern associated with static charge affects. In the future, there will be a need for research and development of electrostatic breakdown for present-day and future nanostructures. In addition to the ESD issue, *electromagnetic interference* (EMI) is of concern on both a component and a system level. Electrical and magnetic fields are generated by the discharge process, which can also be a concern for future systems that contain nanostructures. Hence, there is a need to evaluate not only the nanostructure semiconductor devices and components, but "Nano-ESD" must be addressed at the system level (i.e., "System-Level Nano-ESD"). Future

systems that contain these nanostructures must also be evaluated to quantify the system-level ESD concerns.

Will there be ESD solutions in the future for these nanostructures? In the past, where ESD appeared to be a roadblock, somehow, there was a solution. It will be of interest to see how the engineering world will address Nano-ESD. Today, the question remains open and unanswered.

Acknowledgments

The author would like to thank Julian Montoya (Intel Corporation), Tze Wee Chen (Stanford University), Albert Wallash (Hitachi), Jeremy Walraven (Sandia Laboratories), Professor Augusto Tazzoli (University of Padova, Italy), Sandeep Sangameswaran (IMEC, Belgium), Jia Chen (IBM Corporation), Professor J. J. Liou, and Wen Sui (University of Central Florida).

References

1. S. Voldman, *ESD: Physics and Devices*, Chichester, UK, Wiley, 2004.
2. S. Voldman, *ESD: Circuits and Devices*, Chichester, UK, Wiley, 2005.
3. S. Voldman, *ESD: RF Technology and Circuits*, Chichester, UK, Wiley, 2006.
4. S. Voldman, *ESD: Failure Mechanisms and Models*, Chichester, UK, Wiley, 2009.
5. S. Voldman, "The impact of MOSFET technology evolution and scaling on electrostatic discharge protection," *Microelectronics Reliability*, vol. 38, pp. 1649-1668, 1998.
6. S. Voldman, "Lightning rods for nanoelectronics," *Scientific American*, vol. 287(4), pp. 90-97, 2002.
7. S. Voldman, "Nano electrostatic discharge (ESD)," *IEEE Nanotechnology Magazine*, vol. 3(3), pp. 12-15, 2009.
8. S. Voldman, "Electrostatic discharge protection in the nano-technology—will we be able to provide ESD protection in the future?" In *Proceedings of the International Conference on Semiconductors and Integrated Circuit Technology (ICSICT), Shanghai, China,* Oct 2006.
9. S. Voldman, "Electrostatic discharge in nano-technology," keynote address, conference on Application Specific Circuits and Networks (ASICON) 2007, Guilin, China, October 12-15, 2007.
10. J. Montoya, L. Levit, and A. Englisch, "A study of the mechanisms for ESD damage in reticles," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium,* pp. 394-405, 2000.
11. E. Greig et al., "Controlling static charge in photolithography areas," *Micro Magazine*, vol. 13(5), pp. 33-38, 1995.
12. A. Steinman and J. A. Montoya, "Developing an exit charge specification for semiconductor production equipment," *Micro Magazine*, vol. 15(4), pp. 32-39, 1997.
13. L. B. Levit and J. Menear, "Measuring and quantifying static charge in cleanrooms and process tools," *Solid State Technology*, vol. 41(2), pp. 85-92, 1998.
14. J. Wiley and A. Steinman, "Ultrapure materials—reticles: investigating a new generation of ESD-induced reticle defect," *Micro Magazine*, April 1999, available at www.micromagazine.com.
15. K. C. Wang, "ESD and reticle damage," paper presented at the International SEMATECH Electronic Discharge Impact and Control Workshop, SEMATECH, Austin, Texas, October 9, 2000.

16. A. Steinman, "SEMI E78-0998 electrostatic compatibility," paper presented at the International SEMATECH Electronic Discharge Impact and Control Workshop, SEMATECH, Austin, Texas, October 9, 2000.
17. L. Armentrout, "Analysis of ESD/reticle SMIF Pods," paper presented at the International SEMATECH Electronic Discharge Impact and Control Workshop, SEMATECH, Austin, Texas, October 9, 2000.
18. M. Pendley, "ESD induced EMI detection techniques," paper presented at the International SEMATECH Electronic Discharge Impact and Control Workshop, SEMATECH, Austin, Texas, October 9, 2000.
19. J. Montoya, L. Levit, and A. Englisch, "A study of the mechanisms for ESD damage in reticles," *IEEE Transactions on Electronic Packaging and Manufacturing*, vol. 24(2), pp. 78-85, 2001.
20. A. J. Wallash, T. Hughbanks, and S. Voldman, "ESD failure mechanisms of inductive and magnetoresistive recording heads," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium,* pp. 322-330, 1995.
21. H. Tian and J. K. Lee, "Electrostatic discharge damage of MR heads," in *Proceedings of INTERMAG 1995.*
22. H. Tian and J. K. Lee, "Electrostatic discharge damage of MR heads," *IEEE Transactions on Magnetics*, vol. 31(6), pp. 2624-2626, 1995.
23. T. Cheung and A. Rice, "An investigation of ESD protection for magnetoresistive heads," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 1-7, 1996.
24. C. Lam, C. Chang, and R. Karimi, "A study of ESD sensitivity of AMR and GMR recording heads," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 360-367, 1998.
25. A. Wallash and D. Smith, "Electromagnetic interference (EMI) damage to a giant magnetoresistive (GMR) recording heads," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 332-340, 1998.
26. A. Wallash and Y. K. Kim, "Magnetic changes in GMR heads caused by electrostatic discharge," *IEEE Transactions on Magnetics*, vol. 34(4), pp. 1519-1521, 1998.
27. T. W. Chen, A. J. Wallash, and R. Dutton, "Ultra-fast transmission line pulse testing of tunneling and giant magnetoresistor heads," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 258-261, 2008.
28. A. Wallash, "ESD challenges in magnetic recording: past, present and future," in *Proceedings of the International Reliability Physics Symposium (IRPS)*, pp. 222-228, 2003.
29. J. A. Walraven, J. M. Soden, D. M. Tanner, P. Tangyunyong, E. I. Cole, R. E. Anderson, et al., "Electrostatic discharge/electrical overstress susceptibility in MEMs: a new failure mode," in *Proceedings of the Society of Photo-optical Instrumentation Engineers (SPIE)*, vol. 4180, pp. 30-39, 2000.
30. J. A. Walraven, J. M. Soden, E. I. Cole, D. M. Tanner, and R. E. Anderson, "Human body model, machine model, and charged device model ESD testing of surface micromachined microelectromechanical systems (MEMS)," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 238-247, 2001.
31. A. Tazzoli, V. Peretti, E. Zanoni, and G. Meneghesso, "Transmission line pulse (TLP) testing of radio frequency (RF) micro-machined micro-electromechanical systems (MEMS)," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 295-303, 2006.
32. J. Ruan, N. Nolhier, M. Bafluer, L. Bary, F. Coccetti, T. Lisec, et al., "Electrostatic discharge failure analysis of capacitive RF MEM switches," *Microelectronic Reliability Journal*, vol. 47, pp. 1818-1822, 2007.
33. A. Tazzoli, V. Peretti, and G. Meneghesso, "Electrostatic discharge and cycling effects on ohmic and capacitive RF-MEMS switches," *IEEE Transactions on Device and Material Reliability (TDMR)*, vol. 7(3), pp. 429-437, 2007.

34. A. Tazzoli, V. Peretti, E. Autuzi, and G. Meneghesso, "EOS/ESD sensitivity of functional RF MEMS switches," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 272-280, 2008.
35. X. M. Zhang, F. S. Chau, C. Quan, and A. Q. Liu, "Modeling of optical torsion micro-mirror," in *Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE)*, vol. 3899, pp. 109-116, 1999.
36. M. R. Douglass, "Lifetime estimates and unique failure mechanisms of the digital micro-mirror device (DMD)," in *Proceedings of the International Reliability Physics Symposium (IRPS)*, pp. 9-16, 1998.
37. M. Gromova, L. Haspeslagh, A. Verbist, B. Du Bois, R. Van Hoof, B. Eyckens, et al., "Highly reliable and extremely stable SiGe micro-mirrors," in *Proceedings of the Micro-electromechanical Systems (MEMS)*, pp. 759-762, 2007.
38. S. Sangameswaran, J. De Coster, D. Linten, M. Scholz, S. Thijs, L. Haspeslagh, et al., "ESD reliability issues in microelectromechanical systems (MEMS): a case study of micromirrors," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 249-257, 2008.
39. S. Voldman and V. Gross, "Scaling, optimization, and design considerations of electrostatic discharge protection circuits in CMOS technology," *Journal of Electrostatics*, vol. 33(3), pp. 327-357, 1994.
40. S. Voldman and G. Gerosa, "Mixed voltage interface ESD protection circuits for advanced microprocessors in shallow trench and LOCOS isolation CMOS technology," in *International Electron Device Meeting (IEDM) Technical Digest, Session 10.3.1, December 1994*, pp. 277-281.
41. S. Voldman, "Shallow trench isolation double-diode electrostatic discharge circuit and interaction with DRAM circuitry," *Journal of Electrostatics*, vol. 31, pp. 237-262, 1993.
42. S. Voldman, "Electrostatic discharge protection, scaling, and ion implantation in advanced semiconductor technologies," invited talk, Process Integration Issues/Technical Trends Session, Proceedings of the Ion Implantation Conference (I2CON), Napa, California, 1999.
43. S. Voldman, "ESD robustness and scaling implications of aluminum and copper interconnects in advanced semiconductor technology," in *Proceedings of the Electrostatic Overstress/Electrostatic Discharge (EOS/ESD) Symposium, September*, pp. 316-329, 1997.
44. S. Voldman. "High current transmission line pulse characterization of aluminum and copper interconnects for advanced CMOS semiconductor technologies," in *Proceedings of the International Reliability Physics Symposium (IRPS)*, pp. 293-301, 1998.
45. S. Voldman, "The impact of MOSFET technology evolution and scaling on electrostatic discharge protection" [Review paper], *Micro-electronics Reliability*, vol. 38, pp. 1649-1668, 1998.
46. S. Voldman, "The impact of technology evolution and scaling on electrostatic discharge (ESD) protection on high-pin-count high-performance microprocessors," International Solid-State Circuits Conference Proceedings, Session WA21, San Francisco, February 15-17, 1999.
47. S. Voldman, K. Morriseau, M. Hargrove, V. McGahay, and V. Gross, "High-current characterization of dual-damascene copper Interconnects in SiO_2 and Low-K inter-level dielectrics for advanced CMOS technologies," in *Proceedings of the IEEE International Reliability Physics Symposium (IRPS)*, pp. 144-153, 1999.
48. S. Voldman, D. Hui, L. Warriner, D. Young, R. Williams, J. Howard, et al., "Electrostatic discharge protection in silicon-on-insulator technology," in *Proceedings of the IEEE International Silicon on Insulator (SOI) Conference*, pp. 68-72, 1999.
49. S. Voldman, "Electrostatic discharge (ESD) protection in silicon-on-insulator (SOI) CMOS technology with aluminum and copper interconnects in advanced microprocessor semiconductor chips," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 105-115, 1999.

50. C. Russ, H. Gossner, T. Schulz, N. Chaudhary, W. Xiong, A. Marshall, "ESD evaluation of emerging MUGFET technology," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 280-289, 2005.
51. H. Gossner, C. Russ, F. Siegelin, J. Schneider, K. Schruefer, et al. "Unique ESD failure mechanism in a MUGFET technology," in *International Electron Device Meeting (IEDM) Technical Digest*, pp. 1-4, 2006.
52. D. Tremouilles, S. Thijs, G. Groeseneken, C. Russ, J. Schneider, H. Gossner, "Understanding the optimization of Sub-45 nm FinFET devices for ESD applications," in *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, pp. 408-415, 2007.
53. K. H. Yeo, S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Cho, K. H. Hong, "Gate all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires," in *International Electron Device Meeting (IEDM) Technical Digest*, pp. 1-4, 2006.
54. N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, "High performance fully depleted silicon nanowire (diameter <5 nm) gate-all-around CMOS devices," *IEEE Electron Device Letters*, vol. 27(5), pp. 383-386, 2006.
55. W. Liu, J. J. Liou, A. Chung, Y. H. Jeong, W. C. Chen, and H. C. Lin, "Electrostatic discharge of Si nanowire field effect transistors," *IEEE Electron Device Letters*, vol. 30(9), pp. 969-971, 2009.
56. J. Chen and S. Voldman, "Carbon nanotube diodes and electrostatic discharge circuits and methods," US Patent Application 20080273280, November 6, 2008.

This page intentionally left blank

CHAPTER 16
Nanopackaging

James E. Morris

16.1 Introduction

The new and rapidly developing field of nanopackaging, and specifically of the application of nanotechnologies to microelectronics packaging, has been surveyed recently in Ref. 1. The purpose of this chapter is to expand on the material included there with a brief exposition of more recent developments.

16.2 Nanoparticles

16.2.1 Preparation

Ultimately, *nanoparticle* (NP) fabrication boils down to the various paths by which bulk material can be converted to the nanoscale. The most direct of these include mechanical grinding, etc., and physical vapor deposition (as mentioned by Hayashi et al. in Ref. 1) and spark erosion.[2] In many applications, the NPs are needed in suspension in a carrier medium, for example, Ag in epoxy, and can be precipitated directly by reduction of $AgNO_3$ in the mixture.[3] By controlling the relative concentrations of the reagents, one can also achieve some measure of shape control, from spherical, rectangular, and triangular NPs to rods.[4,5] Smaller sizes and more uniform dispersions can be achieved by ultrasonic resonance vibration dispersal[6] at megahertz frequencies.

The critical problem with NP preparation and processing is how to avoid their tendency to agglomerate into clusters, which is usually attributed to electrostatic charging effects, or to an incompatibility of hydrophilic NPs and a hydrophobic polymer matrix. Some form of surface treatment is required to inhibit this process (Fig. 16.1; see Ref. 7), and much of the art of successful NP applications lies in these various techniques. In many cases, the surface layer applied to inhibit

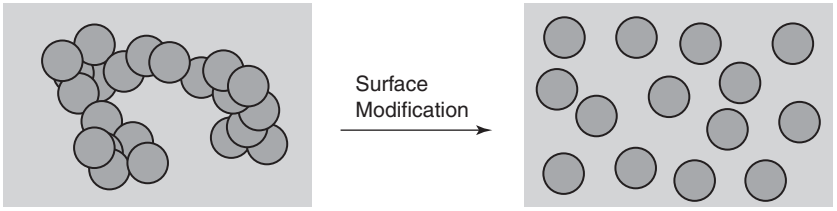


Figure 16.1 Surface treatments are necessary to avoid NP agglomeration. From Sun et al. (2004),[7] with permission.

clustering and coalescence of the NPs during preparation and processing must be subsequently removed, for example, to permit surface interactions such as sintering. For this purpose, methyloctylamine (and other secondary amines) have been shown to be better than octylamine (and other primary amines) because of thermal decomposition at lower temperatures.[8]

Other surface treatments may be developed for other requirements: for example, a graphene coating on Cu NPs to protect them against oxidation, while also providing an electrically conductive surface in conducting composite applications.[9]

16.2.2 No-Pb Solder

The performance improvement of Sn-Ag solder with the addition of Ni NPs[10] confirms earlier work (Amagai in Ref. 1). But the major potential application for nanotechnologies in solder comes from the well-established effect of *melting point* (MP) reduction (Morris in Ref. 1), which could dramatically reduce thermomechanical stress in no-Pb solder joints by lowering the alloy MPs to near those of eutectic Sn-Pb. To get there, however, one needs to get the solder particle sizes down to around 5 nm with a narrow distribution, which will be no mean feat in production. A rough rule of thumb is that 5 nm provides about 5 percent MP reduction (on the absolute scale), as demonstrated for Sn-Ag in Fig. 16.2[11,12] and for Sn-0.4Co-0.7Cu[2,13,14] and Sn-3.0Ag-0.5Cu (SAC)[13,15–17] alloys. The experimental results fit well to empirical models based on a disordered (premelted, liquid) surface layer, which accounts for the reduction in the heat of fusion as the proportion of crystalline core decreases as the NP size decreases.

16.2.3 Embedded Capacitors

Lu and Wong reviewed nanoparticle capacitors in Ref. 1, focusing on conducting particle nanocomposites. Das and Egitto also covered *printed wiring board* (PWB) interconnection vias in Ref. 1 and have recently expanded the technology to include embedded passives (Fig. 16.3), with $BaTiO_3$/epoxy nanoparticle composite capacitors.[18,19]

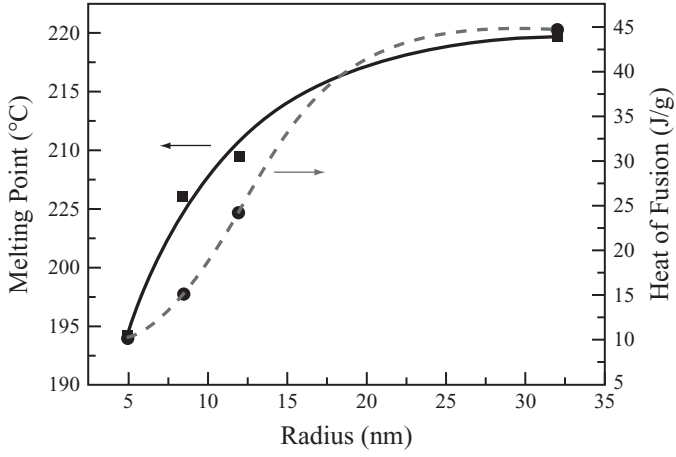


FIGURE 16.2 Sn-Ag nanoparticle MP and heat of fusion reductions as determined by differential scanning calorimetry.[11,12] From Jiang et al. (2007),[11] with permission.

Abothu et al. mixed low-*k* BCB with high-*k* $BaTiO_3$ to balance the negative and positive *temperature coefficients of capacitance* (TCCs) to achieve a zero-TCC material.[20]

16.2.4 Electrically Conductive Adhesives (ECAs)

The first attempt at an NP-based *isotropic conductive adhesive* (ICA) is shown in Fig. 16.4.[21] The percolation threshold, that is, the

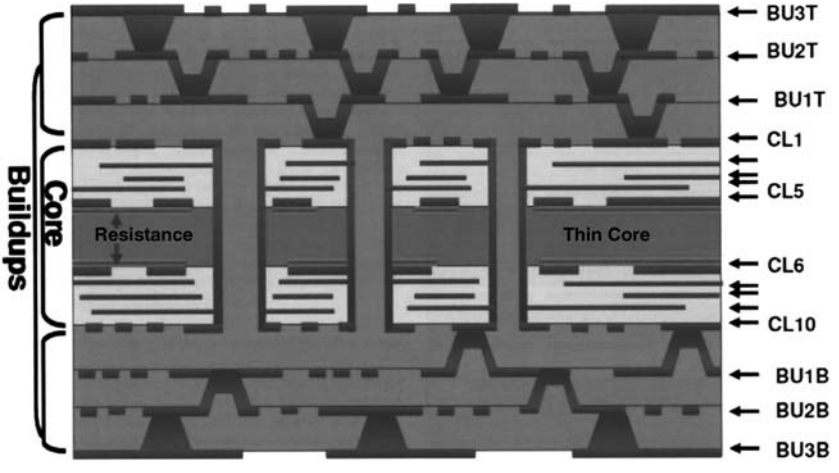


FIGURE 16.3 PWB laminate, showing embedded resistor and capacitor locations.[18,19] From Das et al. (2009),[18] with permission.

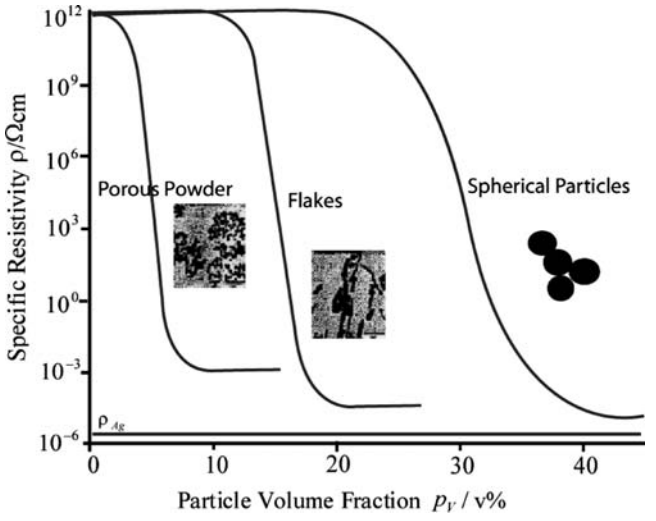


Figure 16.4 Percolation resistivity curves for Ag/epoxy composites.[21] From Kottaus et al. (1997),[21] with permission.

composition at which the electrical properties change from insulating to metallic, drops from ~40 percent for spherical particles to ~15 percent for the usual bimodal flake and powder mix, to ~5 percent for the "nanoporous" structure shown.[21,22] The reductions in the threshold Ag concentration are offset by the increased resistivities, due to a greater number of internal contact resistances and mean free path restrictions in the NP case. Once again, surface treatments can improve the dispersion of the NPs and the ICA performance.[23] In most cases, however, Ag NPs are added to the commercial flake/powder structure,[24,25] and it is important to compare like with like by maintaining constant Ag content,[24] because Lu and Wong showed in Ref. 1 that any improvement in performance gained by the addition of Ag NPs would be exceeded by the addition of an equivalent amount of Ag as powder or flakes (unless the NPs sinter). The NP coating techniques of Refs. 8 and 9 are clearly applicable to ICAs, and Ref. 26 describes a Ag-plated nanographite filler. Furthermore, the addition of SiO_2 NPs to a Cu-powder/epoxy ICA, where both Cu and SiO_2 were treated with silane to prevent agglomeration, inhibits crack propagation and improves adhesive strength.[27] The applications of nanotechnologies to ECAs have been extensively reviewed just recently.[28]

16.2.5 Sintering

The addition of Ag NPs to ICAs has a negative effect, unless they are able to sinter (Lu and Wong in Ref. 1), which requires removal of any

coating that would impede metal-to-metal contact,[29] and the same principles apply to the use of printed NP films for electrical interconnect, (Felba and Schaeffer in Ref. 1.) The conceptual breakthrough is the observation that NPs can sinter at room temperature with removal of their protective surface coating, for example, by immersion in methanol,[30,31] although the process can be hastened by heating. The technology is being widely studied,[32,33] with data on resistivity variations with time and temperature[34,35] correlated with grain growth.[36,37] A model has been proposed to account for the efficiency variation with wavelength of laser sinter/annealing of NP composites.[38] Sintering is a well-known phenomenon, of course, and extensively modeled. It is an exothermic process, but the anneal temperature controls the final equilibrium neck width of the coalesced particles as well as the rate of coalescence,[39] which explains why final conductivities increase with anneal temperatures.[40]

Sintered Ag NP systems can also be used for interfacial bonding, for example, as a *thermal interface material* (TIM),[41] with a significant high-temperature operational advantage over solders.[42]

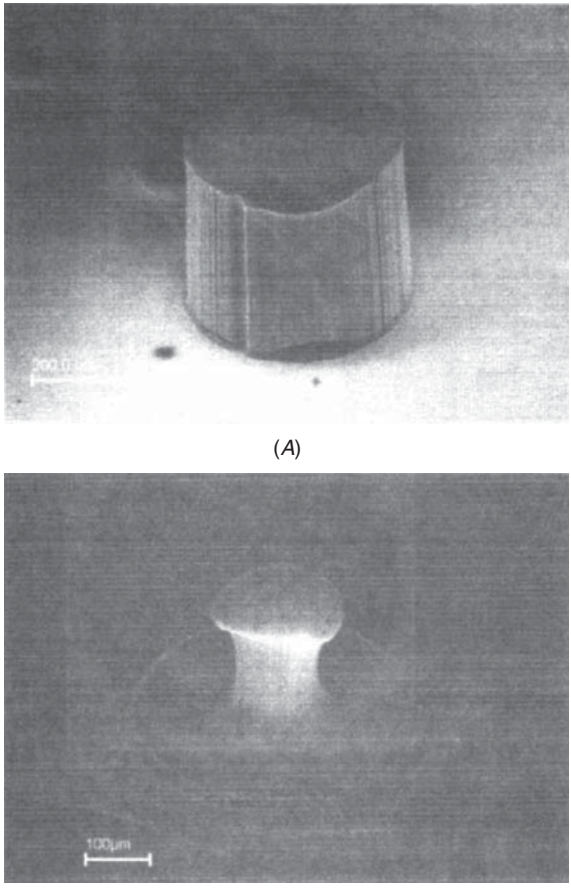
16.2.6 Nanotwins

Although not strictly nanoparticles, nanotwinned grains in copper interconnect are included as the last topic in this section. First, nanograins increase strength, and the twins reduce high-angle grain boundary scattering and block single dislocations, so copper nanotwins increase both conductivity and mechanical strength.[43] Structures are shown in Ref. 44, and a more detailed examination of fracture toughness enhancement is given in Ref. 45.

16.3 Carbon Nanotubes

16.3.1 Preparation

Carbon nanotubes (CNTs) are typically grown at high temperatures of about 900°C by *chemical vapor deposition* (CVD) on metallic seed NPs. This temperature cannot be tolerated by the fragile low-*k* dielectrics of modern nano-CMOS, and so there has been great effort to get it down to 400°C or less, with some success for *multiwalled CNTs* (MWNTs) using plasma-enhanced CVD, but less for *single-walled CNTs* (SWNTs). An alternative approach has been demonstrated of locally heating the Si substrate from the rear by thin-film spiral heaters deposited under CNT bump locations (for example), to achieve a localized ΔT of about 400°C.[46] The more common approach, required for CNTs on polymers, is to grow them at high temperature and then transfer them to the application substrate with a carrier medium, which might be solder, ICA, double-sided adhesive tape, etc.[47–52] In some cases, the CNT



(*A*)

(*B*)

Figure 16.5 The diameter of the column of CNTs (*top*) can be reduced by pulling the CNTs together.[53] From Liu et al. (2009),[53] with permission.

array may be filled in with polymer between the CNTs, because the CNTs as grown are typically well separated. Methanol can be used to pull the CNT bundle closer together, as shown in Fig. 16.5; the "mushroom top" ends can then be cut off to provide a more closely packed CNT bundle.[53]

16.3.2 Mechanical

Electromicrographs of fractured solder joints and other materials incorporating low densities of CNTs show that the CNTs extend across grain boundaries, strengthening the composite.[54]

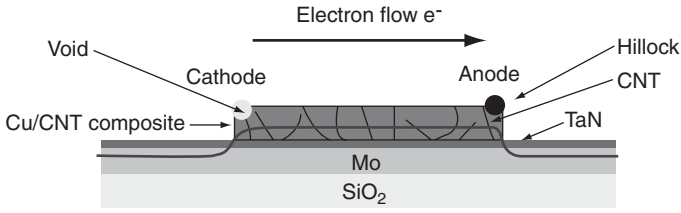


Figure 16.6 The experimental setup to measure electromigration in CNT-doped copper.[60] From Chai et al. (2008),[60] with permission.

16.3.3 Electrical: Random

Randomly dispersed CNTs in an insulating matrix can be used for electromagnetic shielding (e.g., Cheng et al. in Ref. 1), but suffer the same problems of nonuniform dispersion as NPs. Improved shielding can be obtained at low CNT densities by including an ionic liquid in the matrix.[55] The other problem with such random distributions is that the electrical contact between CNTs (not end-to-end) is relatively high resistance. Yan et al. have modeled such systems to show the effects of CNT and contact resistances, CNT length and diameter, and volume fraction on the composite resistivity and percolation threshold,[56] whereas Oh et al. demonstrated the effects of reducing the interfacial contact resistance by coating the CNTs with Ag.[57]

Naturally, CNTs have also been used as ICA filler (in one case by adding CNTs to nonconductive adhesive[58]) and have been added to Ag-ICAs as supplementary filler. Reference 59 compares the addition of CNTs to Ag-ICAs with extra Ag as NPs.

CNTs in Cu interconnect (Fig. 16.6) can substantially reduce electromigration effects,[60] which could be applied to ultrasmall solder joints where electromigration is becoming a source of concern.

16.3.4 Electrical: Aligned

To achieve the full potential of CNTs in electrical interconnections, current must flow along the CNT, from end to end, and furthermore a good ohmic electrical connection is required at the ends. A prerequisite for this is to "open" the ends, that is, to remove any hemispherical fullerene end caps, for example, by acid, steam, oxidation, plasma, or chemical-mechanical polishing.[50,61] Most CNT interconnect modeling is focused on on-chip applications,[62–70] with off-chip interconnect being considered only relatively recently.[71,72] Most compare CNT properties unfavorably with Cu, but at dc, which tends to miss the point that high-frequency performance is more important for most *very large-scale integrated* (VLSI) applications, and that CNTs win there because of the absence of skin effect.[73]

16.3.5 3D System Integration

Three-dimensional (3D) integration is the current "hot topic" in microelectronics packaging. Cu-filled *through-silicon vias* (TSVs) have reliability issues due to the coefficient of thermal expansion mismatch between Cu and Si, but the polymer-filled Cu-cylinder "barrel" technology alternative[74] has higher resistance. The viability of MWNT-filled TSVs has been demonstrated in principle, primarily with micrometer-scale bundles[75–87] (Fig. 16.7), but also for 15–nm-diameter CNTs in 35–nm-diameter holes.[88] Performance modeling is integrated into these papers and in Refs. 89 and 90, and metal/CNT contact resistance is considered in Ref. 91.

16.3.6 Thermal Dissipation

Pradham et al. have compared the thermal conductances of aligned and random SWNTs and MWNTs with graphite and show that only end-to-end heat flow through aligned SWNTs can attain the order-of-magnitude improvement in TIM performance needed for next-generation CMOS.[92] In random CNT composites, surface treatment is necessary to ensure efficient thermal transfer between the CNTs and the epoxy matrix.[93] Liu and Wang described CNT heat sink channels in Ref. 1; these and a variety of alternative structures have been modeled by Cheng,[94] who also shows that a 5 percent suspension of CNTs in the coolant can improve their thermal performance.

16.3.7 Inductance

High-Q inductance is difficult to achieve with the thin-film spiral inductors typically envisaged for embedded passives, so the concept of a CNT inductor[95] is intriguing. Such an inductor would require multiple CNT segments to achieve the spiral, but calculated Q values, based on the CNT quantum inductance and quantum resistance, are impressive. However, the quantum inductance concept is valid only for short lengths, less than the ballistic length, and has not been confirmed experimentally even then.[73]

16.3.8 Nanowires

Nanowire applications are included here for convenience. Ni nanowire contacts have been shown to have lower resistance than an equivalent flat-plate contact surface for test purposes.[96] Ag nanowires have been extensively tested as ICA fillers, both as sole filler[97,98] and together with Ag flakes in epoxy[99,100] or silicone.[101] Nanowires have also been used to construct anisotropic conductive films, for example, Cu grown in a polycarbonate template[102] or Au grown in AAO

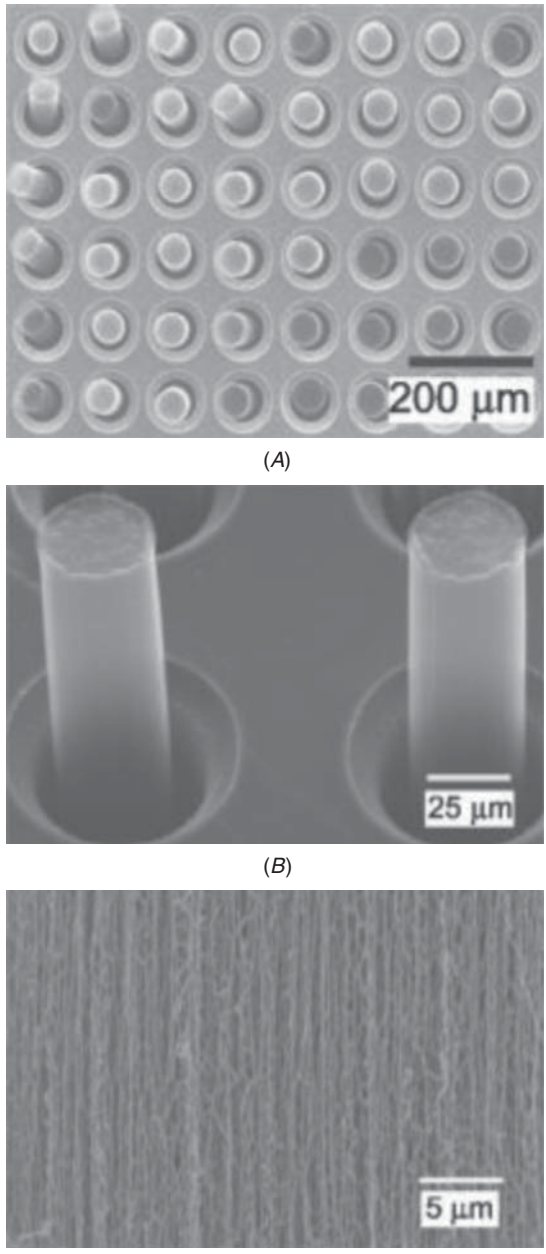


Figure 16.7 (*A*) Array of MWNT-filled TSVs, showing (*B*) individual CNT bundles and (*C*) individual CNTs.[75] From Xu et al. (2007),[75] with permission.

alumina.[103] In the latter case, the Au nanowires are tipped with Co, to keep them aligned in a magnetic field while the template is dissolved away and replaced with polymer.

16.4 Health and Environment

16.4.1 Ag Nanoparticles in the Environment[104]

Most of the NP applications described previously employ Ag, which has been used as an antibacterial disinfectant since Hippocrates, often released from $AgNO_3$ as approximately 8 to 70 ppm Ag^+, in bandages and eye drops, coated on surgical implants, on burns and fungal infections, and as a dietary supplement. Nowadays, high-volume use includes spa/pool water and air purification, odor-free socks, cosmetic preservatives, kitchen/bathroom hygiene, and in clothes and dishwashers. Most waste goes straight to the aquatic environment, where Ag^+ is second only to Hg in toxicity to aquatic organisms, with high bioassimilation and bioaccumulation efficiencies, and where it concentrates in aquatic plants and sediment. Aquatic concentrations typically range from 0.03 (1985 ocean) to 500 ng/L, but 50 ng/L is toxic to aquatic life generally, with lower levels toxic to fish and other embryos, despite the EPA standard of 1,920 to 3,200 ng/L. So there are environmental concerns with the prospect of increased releases of waste Ag, leading to calls for increased study, specifically of nano-Ag effects, and for the classification of nano-Ag as a pesticide to place it under direct EPA control.

Because much of the nano-Ag usage in packaging is the result of no-Pb legislation, it would clearly be counterproductive for it to have similar issues. But although it is definitely not benign, Ag per se is toxic to humans only in massive doses, with the primary effect of accumulating in the skin, which turns irreversibly gray/blue/black, but with no other long-term health issues. However, the effects of nano-Ag are unknown, with specific concerns that it could be absorbed directly through the skin, or into cells through the cell wall, or cross other membrane barriers, because inhaled NPs can enter the bloodstream directly, and the increased NP surface reactivity clearly increases toxicity.

16.4.2 Health Issues with CNTs [105]

CNTs are often referred to by lawyers as "the new asbestos," for obvious reasons if one considers their potential to enter the fine passages of the lung. The Royal Society identified the potential for CNTs to cause mesothelioma in 2004, and there have been several clinical studies that point to similarities. One result is the exclusion of nanotechnologies

from insurance policies, but the principal one is that the industry is on notice to take protective steps against future possible litigation. To do that, the industry must be able to demonstrate that:

- Products were designed with safety in mind.
- Workers were educated to possible exposure risks.
- The company tracks relevant research, regulations, etc. (e.g., on the NIOSH website's Nanoparticle Information Library).
- Health risks were evaluated (possibly in consortia).
- External statements are consistent with internal data/memos.
- Affirmative steps were taken to reduce exposures, e.g., with filters, gloves, washing.
- The company monitors the health of its workers and consumers.

The last point is important, because it is the industry's own workers who are most at risk. There is a parallel with ISO9000, in that it is important to document that procedures are in place, because it is ignoring the known issue that leads to punitive damages for negligence.

16.5 Conclusion

The primary issues in electronics packaging at the moment are thermal (i.e., the effective removal of the heat dissipated by the chip), embedded passives (to remove resistors and capacitors from the PWB surface), and 3D packaging (i.e., chip stacking, which requires TSV development and may lead to greater thermal problems). All of these are addressed by the nanotechnologies surveyed in this chapter. The chapter closed with a brief mention of ongoing health and environmental questions that the industry must address in its products' life-cycle analyses.

References

1. J. E. Morris, editor, *Nanopackaging: Nanotechnologies in Electronics Packaging*, New York, Springer, 2008.
2. C. Andersson, C. Zhou, B. Yang, Y. Gao, J. Liu, and Q. Zhai, in *Proceedings of the 2nd Electronic System Integration Technology Conference, 2008*, pp. 915-921, New York, IEEE, 2008.
3. Y. Li, K. Moon, and C.-P. Wong, in *Proceedings of the 56th Electronic Components and Technology Conference, San Diego, 2006*, pp. 1239-1245, New York, IEEE, 2006.
4. H. Jiang, K. Moon, and C.-P. Wong, in *Proceedings of the 10th International Symposium on Advanced Packaging Materials, Irvine, California, 2005*, New York, IEEE, 2005.

5. S. Pothukuchi, Y. Li, and C.-P. Wong, in *Proceedings of the 54th Electronic Components and Technology Conference, Las Vegas, 2004*, pp. 1965-1967, New York, IEEE, 2004.
6. M. T. Nguyen, T. T. Tsung, and H. Chang, *Journal of Vacuum Science and Technology B*, vol. 27(3), pp. 1586-1589, 2009.
7. Y. Sun, Z. Zhang, and C.-P. Wong, in *Proceedings of the 54th Electronic Components and Technology Conference, Las Vegas, 2004*, pp. 754-760, New York, IEEE, 2004.
8. M. Tobita, Y. Yasuda, E. Ide, J. Ushio, and T. Morita, *Journal of Nanoparticle Research*, vol. 21(5), pp. 486-490, 2010.
9. N. A. Luechinger, E. K. Athanassiou, and W. J. Stark, *Nanotechnology*, vol. 19, p. 445201, 2009.
10. F. Qi, L. Sun, Z. Hou, J. Wang, and C. Qin, in *Proceedings of the International Conference on Electronic Packaging and High Density Packaging (ICEPT-HDP), Shanghai, 2008*, pp. E1-06, New York, IEEE, 2008.
11. H. Jiang, K. Moon, F. Hua, and C.-P. Wong, in *Proceedings of the 57th Electronic Components and Technology Conference, Reno, Nevada, 2007*, pp. 54-58, New York, IEEE, 2007.
12. H. Jiang, K. Moon, F. Hua, and C.-P. Wong, *Chemistry of Materials*, vol. 19, pp. 4482-4485, 2007.
13. J. Liu, C. Andersson, Y. Gao, and Q. Zhai, in *Proceedings of the 10th Electronics Packaging Technology Conference, Singapore, 2008*, pp. 84-93, New York, IEEE, 2008.
14. C. D. Zou, Y. L. Gao, B. Yang, Q. J. Zhai, C. Andersson, and J. Liu, *Soldering & Surface Mount Technology*, vol. 21(2), pp. 9-13, 2009.
15. H. Jiang, K. Moon, F. Hua, and C.-P. Wong, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 1400-1404, New York, IEEE, 2008.
16. C. D. Zou, Y. L. Gao, B. Yang, X. Z. Xia, J. Zhai, C. Andersson, et al., *Journal of Electronic Materials*, vol. 38(2), pp. 351-355, 2009.
17. Y. Gao, C. Zou, B. Yang, Q. Zhai, J. Liu, E. Zhuravlev, et al., *Journal of Alloys and Compounds*, vol. 484, pp. 777-781, 2009.
18. R. N. Das, K. I. Papthomas, S. G. Rosser, T. Antesberger, J. M. Lauffer, M. D. Poliks, et al., in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 591-598, New York, IEEE, 2009.
19. R. N. Das, S. G. Rosser, K. I. Papthomas, T. Antesberger, and V. Markovich, *Circuit World*, vol. 35(4), pp. 31-39, 2009.
20. R. I. Abothu, B. W. Lee, P. Markondeya Raj, E. Engin, P. Muthana, C. K. Yoon, et al., in *Proceedings of the 56th Electronic Components and Technology Conference, San Diego, 2006*, pp. 1790-1794, New York, IEEE, 2006.
21. S. Kottaus, B. H. Guenther, R. Haug, and H. Scheafer, *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part A*, vol. 20(1), pp. 15-20, 1997.
22. D. I. Tee, M. Mariatti, C. H. See, and K. F. Chong, in *Proceedings of the 31st International Electronics Manufacturing Technology Symposium (IEMT), Malaysia, 2006*, pp. 496-505, New York, IEEE, 2006.
23. Z. Kornain, N. Amin, A. Jalar, A. Y. Cheah, and I. Ahmad, in *Proceedings of the ICSE, Malaysia, 2008*, pp. 549-553, New York, ACM, 2008.
24. P. Mach, Richter, and A. Pietrikova, in *Proceedings of the 31st International Spring Seminar on Electronics Technology, Budapest, 2008*, Paper D003, pp. 230-235, New York, IEEE, 2008.
25. D. Busek, R. Radev, and P. Mach, in *Proceedings of the 30th International Spring Seminar on Electronics Technology, Cluj-Napoca, Romania, 2007*, pp. 7-11, New York, IEEE, 2007.
26. W. Lin, X. Xi, and C. Yu, *Synthetic Metals*, vol. 159, pp. 619-624, 2009.
27. H. Zhao, T. Liang, and B. Liu, *International Journal of Adhesion and Adhesives*, vol. 27, pp. 429-433, 2007.

28. Y. Li, D. Lu, and C.-P. Wong, *Electrical Conductive Adhesives with Nanotechnologies*, New York, Springer, 2009.
29. R. Zhang and C.-P. Wong, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 150-154, New York, IEEE, 2009.
30. D. Wakuda, M. Hatamura, and K. Suganuma, in *Proceedings of the 6th International Conference on Polymers and Adhesives in Microelectronics and Photonics (Polytronic '07), Tokyo, 2007*, p. 110, New York, IEEE, 2007.
31. K. Suganuma, in *Proceedings of the 6th International Conference on Polymers and Adhesives in Microelectronics and Photonics (Polytronic '07), Tokyo, 2007*, pp. 30-35, New York, IEEE, 2007.
32. G. -Q. Lu, J. N. Calata, G. Lei, and X. Chen, in *Proceedings of the 8th International Conference on Thermal, Mechanical, and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems (EuroSime), London, 2007*, pp. 609-613, New York, IEEE, 2007.
33. M. Maruyama, R. Matsubayashi, H. Iwakuro, S. Isoda, and T. Komatsu, *Applied Physics A*, vol. 93, pp. 467-470, 2008.
34. J. Perelaer, C. E. Hendriks, A. W. M. deLaat, and U. S. Schubert, *Nanotechnology*, vol. 20, p. 165303, 2009.
35. D. Wakuda, C.-J. Kim, K.-S. Kim, and K. Suganuma, in *Proceedings of the 2nd Electronic System Integration Technology Conference, 2008*, pp. 909-913, New York, IEEE, 2008.
36. D. Wakuda, K.-S. Kim, and K. Suganuma, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 1557-1562, New York, IEEE, 2009.
37. R. N. Das, F. D. Egitto, J. M. Lauffer, M. D. Poliks, and V. R. Markovich, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 180-187, New York, IEEE, 2009.
38. K. Maekawa, K. Yamasaki, T. Niizeki, M. Mita, Y. Matsuba, N. Teraba, et al., in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 1579-1584, New York, IEEE, 2009.
39. J. S. Raut, R. B. Bhagat, and K. A. Fichthorn, *Nanostructured Materials*, vol. 10(5), pp. 837-851, 1998.
40. K.-S. Moon, H. Dong, R. Maric, S. Pothkuchi, A. Hunt, Y. Li, and C.-P. Wong, Journal of Electronic Materials, vol. 34(2), pp. 168-175, 2005.
41. V. Chhasatia, F. Zhou, Y. Sun, L. Huang, and H. Wang, in *Proceedings of the 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2008*, pp. 419-427, New York, ASME, 2008.
42. T. Morita, E. Ide, Y. Yasuda, A. Hirose, and K. Kobayashi, *Japanese Journal of Applied Physics*, vol. 47(8), pp. 6615-6622, 2008.
43. O. Anderoglu, A. Misra, H. Wang, F. Ronning, M. F. Hundley, and X. Zhang, *Applied Physics Letters*, vol. 93, p. 083108, 2008.
44. D. Xu, L. Xu, V. Sriram, K. Sun, J.-M. Yang, and K.-N. Tu, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 2060-2063, New York, IEEE, 2009.
45. H. Zhou and S. Qu, *Nanotechnology*, vol. 21, p. 035706, 2010.
46. T. Xu, H. Li, Z. Wang, and J. Miao, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 1395-1399, New York, IEEE, 2008.
47. K. Moon, W. Lin, H. Jiang, H. Ko, L. Zhu, and C.-P. Wong, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 234-240, New York, IEEE, 2008.
48. L. Zhu, D. W. Hess, and C.-P. Wong, in *Proceedings of the 56th Electronic Components and Technology Conference, San Diego, 2006*, pp. 171-176, New York, IEEE, 2006.
49. O. Hildreth, W. Lin, C. Alvarez, and C.-P. Wong, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 1460-1464, New York, IEEE, 2009.

50. I. Soga, D. Kondo, Y. Yamaguchi, T. Iwai, M. Mizukoshi, Y. Awano, et al., in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 1390-1394, New York, IEEE, 2008.
51. T. Wang, B. Carlberg, M. Jonsson, G.-H. Jeong, E. E. B. Campbell, and J. Liu, *Applied Physics Letters*, vol. 91, p. 093123, 2007.
52. H. Jiang, L. Zhu, K. Moon, Y. Li, and C.-P. Wong, in *Proceedings of the 57th Electronic Components and Technology Conference, Reno, Nevada, 2007*, pp. 463-466, New York, IEEE, 2007.
53. Z. Liu, C. Lijie, S. Kar, P. M. Ajayan, and J.-Q. Lu, *IEEE Transactions on Nanotechnology*, vol. 8(2), pp. 196-203, 2009.
54. G. Yamamoto, M. Omori, T. Hashida, and H. Kimura, *Nanotechnology*, vol. 19, p. 315708, 2008.
55. J. -C. Chiu, C.-M. Chang, J.-W. Lin, and W.-H. Cheng, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 427-430, New York, IEEE, 2008.
56. K. Y. Yan, Q. Z. Xue, Q. B. Zheng, and L. Z. Hao, *Nanotechnology*, vol. 18, p. 255705, 2007.
57. Y. Oh, D. Suh, Y. Kim, E. Lee, J. S. Mok, J. Choi, et al., *Nanotechnology*, vol. 19, p. 495602, 2008.
58. H. Jiang, M. J. Yim, K. Moon, and C.-P. Wong, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 1385-1389, New York, IEEE, 2008.
59. Z. K. Zhang, S. J. Jiang, J. Liu, and M. Inoue, in *Proceedings of the International Conference on Electronic Packaging and High Density Packaging (ICEPT-HDP), Shanghai, 2008*, pp. E3-04, New York, IEEE, 2008.
60. Y. Chai, P. C. H. Chan, Y. Fu, Y. C. Chuang, and C. Y. Liu, in *Proceedings of the 58th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2008*, pp. 412-420, New York, IEEE, 2008.
61. Z. Xiao, Y. Chai, P. C. H. Chan, B. Chen, M. Zhao, and M. Liu, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 1811-1815, New York, IEEE, 2009.
62. A. Naaemi, G. Huang, and J. D. Meindl, in *Proceedings of the 57th Electronic Components and Technology Conference, Reno, Nevada, 2007*, pp. 420-428, New York, IEEE, 2007.
63. A. Nieuwoudt, M. Mondal, and Y. Massoud, in *Proceedings of the IEEE Conference, 2007*, pp. 708-713.
64. A. Naeemi, G. Huang, and J. D. Meindl, in *Proceedings of the Electronic Components and Technology Conference, 2007*, pp. 1936-1941.
65. A. Marffucci, G. Miano, and F. Villone, in *Proceedings of the 2nd Electronic System Integration Technology Conference, 2008, Greenwich, UK*, pp. 1051-1056, New York, IEEE, 2008.
66. A. Marffucci, G. Miano, and F. Villone, *IEEE Transactions on Nanotechnology*, vol. 8(3), pp. 345-354, 2009.
67. M. S. Sarto, A. Tamburrano, and M. D'Amore, *IEEE Transactions on Nanotechnology*, vol. 8(2), pp. 214-225, 2009.
68. N. Srivastava, R. V. Joshi, and K. Bannerjee, in *Proceedings of the IEDM Conference, 2005*, New York, IEEE, 2005.
69. N. Srivastava and K. Bannerjee, in *Proceedings of the ICCAD Conference, 2005*, pp. 383-390, New York, ACM, 2005.
70. K. Bannerjee and N. Srivastava, in *Proceedings of the DAC 2006, San Francisco, 47.2 (July 2006)*, pp. 809-814, New York, ACM, 2006.
71. X. Zhang, T. Wang, J. Liu, and C. Andersson, in *Proceedings of the 2nd Electronic System Integration Technology Conference, Greenwich, UK*, 2008, pp. 633-638, New York, IEEE, 2008.
72. A. G. Chiariello, G. Miano, and A. Marffucci, in *Proceedings of the 9th IEEE Conference on Nanotechnology, Genoa, 2009*, pp. 70-73, New York, IEEE, 2009.
73. K. Banerjee, H. Li, and N. Srivastava, in *Proceedings of the 8th IEEE Conference on Nanotechnology, Arlington, Virginia, 2008*, New York, IEEE, 2008.

74. "Toshiba Manufactured Through Silicon Via First Commercial Implementation," *MicroNews (Chipworks/Yole)*, Issue 75, Dec 2008, pp. 4-5.
75. T. Xu, Z. Wang, J. Miao, X. Chen, and C. M. Tan, *Applied Physics Letters*, vol. 91, p. 042108, 2007.
76. J.-H. Ting, C.-C. Chiu, and F.-Y. Huang, *Journal of Vacuum Science and Technology B*, vol. 27(3), pp. 1086-1092, 2009.
77. W. Hoenlein, F. Kreupl, G. S. Duesberg, A. P. Graham, M. Liebau, R. Seidel, et al., *Materials Science and Engineering C*, vol. 23, pp. 663-669, 2003.
78. M. Nihei, M. Horibe, A. Kawabata, and Y. Awano, *Japanese Journal of Applied Physics*, vol. 43, pp. 1856-1859, 2004.
79. M. Nihei, M. Horibe, A. Kawabata, and Y. Awano, in *Proceedings of the IEEE International Interconnect Conference, 2004*, pp. 251-253.
80. S. Sato, M. Nihei, A. Mimura, A. Kawabata, D. Kondo, H. Shioya, et al., in *Proceedings of the IEEE International Interconnect Conference, 2006*, pp. 230-232.
81. Y. Awano, S. Sato, D. Kondo, M. Ohfuti, A. Kawabata, M. Nihei, and N. Yokoyama, *physica status solidi (a)*, vol. 203(14), pp. 3611-3616, 2006.
82. D. Yokoyama, T. Iwasaki, T. Yoshida, H. Kawarada, S. Sato, T. Hyakushima, et al., *Applied Physics Letters*, vol. 91, p. 263101, 2007.
83. M. Nihei, T. Hyakushima, S. Sato, T. Nozue, M. Norimatsu, M. Mishima, et al., in *Proceedings of the IEEE International Interconnect Conference, 2007*, pp. 204-206.
84. A. Kawabata, S. Sato, T. Nozue, T. Hyakushima, M. Norimatsu, M. Mishima, et al., *Proceedings of the IEEE International Interconnect Conference, 2008*, pp. 237-239.
85. J. C. Coiffic, M. Fayolle, S. Maitrejean, L. E. F. Foa Torres, and H. Le Poche, *Applied Physics Letters*, vol. 91, 252107, 2007.
86. T. Xu, Z. Wang, J. Miao, X. Chen, and C. M. Tan, *Applied Physics Letters*, vol. 91, p. 042108, 2007.
87. T. Wang, K. Jeppson, N. Olofsson, E. E. B. Campbell, and J. Liu, *Nanotechnology*, vol. 20, p. 485203, 2009.
88. A. P. Graham, G. S. Duesberg, R. Seidel, M. Liebau, E. Unger, F. Kreupl, et al., *Diamond and Related Materials*, vol. 13, pp. 1296-1300, 2004.
89. C. W. Tan and J. Miao, in *Proceedings of the 57th Electronic Components and Technology Conference, Reno, Nevada, 2007*, pp. 1936-1941, New York, IEEE, 2007.
90. C. W. Tan and J. Miao, in *Proceedings of the IEEE Conference on Emerging Technologies: Nanoelectronics, 2006*, pp. 75-78.
91. R. R. Jackson and S. Graham, *Applied Physics Letters*, vol. 94, 012109, 2009.
92. N. R. Pradham, H. Duan, J. Liang, and G. S. Iannacchione, *Nanotechnology*, vol. 20, p. 245705, 2009.
93. Q. Liang, W. Wang, K. Moon, and C.-P. Wong, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 460-464, New York, IEEE, 2009.
94. Z. Cheng, SMIT Center, Shanghai University, personal communication.
95. O. F. Mousa, B. C. Kim, J. Flicker, and J. Ready, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 497-501, New York, IEEE, 2009.
96. S. S. Baek and R. S. Fearing, *IEEE Transactions on Components and Packaging Technologies*, vol. 31(4), pp. 859-868, 2008.
97. H. Wu, X. Wu, J. Liu, G. Zhang, Y. Wang, Y. Zeng, et al., *Journal of Composite Materials*, vol. 40, pp. 1961-1969, 2006.
98. H. P. Wu, J. F. Liu, X. J. Wu, M. Y. Ge, Y. W. Wang, et al., *International Journal of Adhesion and Adhesives*, vol. 26, pp. 617-621, 2006.
99. C. Chen, L. Wang, R. Li, G. Jiang, H. Yu, and T. Chen, *Journal of Materials Science*, vol. 42, pp. 3172-3176, 2007.
100. D. Chen, X. Qiao, X. Qiu, F. Tan, J. Chen, and R. Jiang, *Journal of Materials Science: Materials in Electronics*, vol. 21(5), 2010.

101. A. Munari, J. Xu, E. Dalton, A. Mathewson, and K. M. Razeeb, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 448-452, New York, IEEE, 2009.
102. F. Stam, K. M. Razeeb, S. Salwa, and A. Mathewson, in *Proceedings of the 59th Electronic Components and Technology Conference, San Diego, California, 2009*, pp. 1470-1474, New York, IEEE, 2009.
103. R.-J. Lin, Y.-Y. Hsu, Y.-C. Chen, S.-Y. Cheng, and R.-H. Uang, in *Proceedings of the 55th Electronic Components and Technology Conference, Lake Buena Vista, Florida, 2005*, pp. 66-70, New York, IEEE, 2005.
104. S. N. Luoma, "Silver nanotechnologies and the environment: old problems or new challenges," Project on Emerging Nanotechnologies PEN 15, PEW Charitable Trusts and Woodrow Wilson International Center for Scholars, Sept 2008.
105. Law 360° (Portfolio Media Inc) online reports. Available at www.law360.com.

Index

F

G

L

M

N

O

Q

R

S

T