14

Power Inverters

Inversion is the conversion of dc power to ac power at a desired output voltage or current and frequency. A static inverter circuit performs this transformation.
The terms voltage-fed and current-fed are used in connection with inverter circuits.
A *voltage-fed inverter* is one in which the dc input voltage is essentially constant and independent of the load current drawn. The inverter specifies the load voltage while the drawn current shape is dictated by the load.
A *current-fed inverter* (or current source inverter) is one in which the source, hence the load current is predetermined and the load impedance determines the output voltage. The supply current cannot change quickly. This is achieved by series dc supply inductance which prevents sudden changes in current. The load current magnitude is controlled by varying the input dc voltage to the large inductance, hence inverter response to load changes is slow. Being a current source, the inverter can survive an output short circuit thereby offering fault ride-through properties.
Voltage control may be required to maintain a fixed output voltage when the dc input voltage regulation is poor, or to control power to a load. The inverter and its output can be single-phase, three-phase or multi-phase. Variable output frequency may be required for ac motor speed control where, in conjunction with voltage or current control, constant motor flux can be maintained.
Inverter output waveforms are usually rectilinear in nature and as such contain harmonics which may lead to reduced load efficiency and performance. Load harmonic reduction can be achieved by either filtering, selected harmonic-reduction chopping or pulse-width modulation.
The quality of an inverter output is normally evaluated in terms of its harmonic factor, ρ, distortion factor, μ, and total harmonic distortion, *thd*. In section 12.6.2 these first two factors were defined in terms of the supply current. For inverters the factors are redefined in terms of the output voltage harmonics as follows

$$\rho_n = \left|\frac{V_n}{V_1}\right| = n\mu_n \qquad n > 1 \tag{14.1}$$

The distortion factor for an individual harmonic is

$$\mu_n = \left|\frac{V_n}{nV_1}\right| = \frac{\rho_n}{n} \tag{14.2}$$

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]} \Big/ V_1 = \sqrt{\sum_{n\geq 2}^{\infty}\mu_n^2} = \sqrt{\sum_{n\geq 2}^{\infty}\left(\frac{\rho_n}{n}\right)^2} \tag{14.3}$$

The factor V_n/n is used since the harmonic currents produced in an inductive load attenuate with frequency. The harmonic currents produce unwanted heating and torque oscillations in ac motors, although such harmonic currents are not a drawback to the power delivered to a resistive heating load.

14.1 dc-to-ac voltage-fed inverter bridge topologies

14.1.1 Single-phase voltage-fed inverter bridge

Figure 14.la shows an H-bridge inverter for producing an ac voltage and employing switches which may be transistors (MOSFET or IGBT), or at high powers, thyristors (GTO or CGT). Device conduction patterns are also shown in figures 14.lb and c. With inductive loads (not purely resistive), stored energy at turn-off is fed through the bridge reactive feedback or freewheel diodes D_1 to D_4. These four diodes clamp the load voltage to within the dc supply rails (0 to V_s).

14.1.1i - *Square-wave output*
Figure 14.lb shows waveforms for a square-wave output ($2t_1=t_2$) where each device is turned on as appropriate for 180°, (that is π) of the output voltage cycle (state sequence 10, 01, 10, ..). The load current i_L grows exponentially through T_1 and T_2 (state 10) according to

$$V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{14.4}$$

When T_1 and T_2 are turned off, T_3 and T_4 are turned on (state 01), thereby reversing the load voltage. Because of the inductive nature of the load, the load current cannot reverse and load reactive energy flows back into the supply via diodes D_3 and D_4 (which are in parallel with T_3 and T_4 respectively) according to

$$-V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{14.5}$$

The load current falls exponentially and at zero, T_3 and T_4 become forward-biased and conduct load current, thereby feeding power to the load.
The output voltage is a square wave of magnitude $\pm V_s$ and has an rms value of V_s.
For a simple *R-L* load, with time constant $\tau = L/R$, during the first cycle with no initial load current, solving equation (14.4) yields a load current

$$i_L(t) = \frac{V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{(A)} \tag{14.6}$$

Under steady-state load conditions, the initial current is $\breve{I}$ as shown in figure 14.lb, and equation (14.4) yields

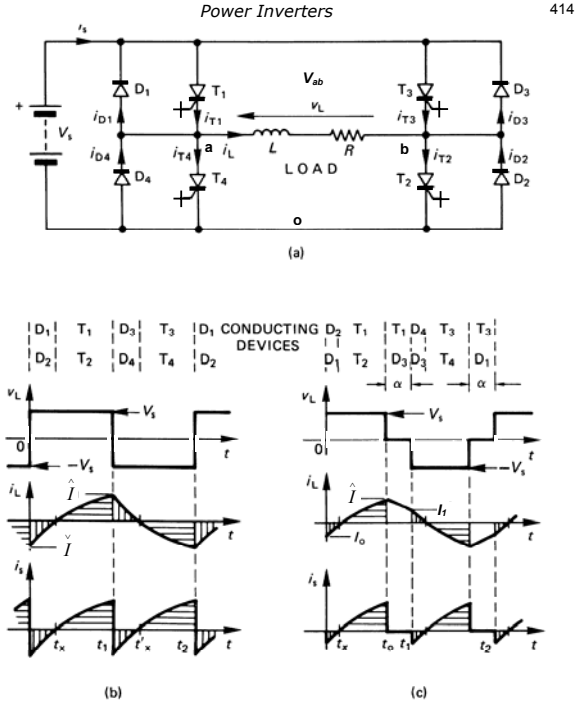

Figure 14.1. *GCT thyristor single-phase bridge inverter: (a) circuit diagram; (b) square-wave output voltage; and (c) quasi-square-wave output voltage.*

$$i_L(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - \check{I}\right)e^{\frac{-t}{\tau}} \quad \text{(A)} \qquad 0 \le t \le t_1 \quad \text{(s)} \tag{14.7}$$

for $v_L = V_s$ (V)

$\check{I} \le 0$ (A)

During the second half-cycle ($t_1 \le t \le t_2$) when the supply is effectively reversed across the load, equation (14.5) yields

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + \hat{I}\right)e^{\frac{-t}{\tau}} \quad \text{(A)} \qquad 0 \le t \le t_2 - t_1 \quad \text{(s)} \tag{14.8}$$

for $v_L = -V_s$ (V)

$\hat{I} \ge 0$ (A)

A new time axis has been used in equation (14.8) starting at $t = t_1$ in figure 14.lb. Since in steady-state $\hat{I} = -\check{I}$, the initial steady-state current $\hat{I}$ can be found from equation (14.7) when, at $t = t_1$, $i_L = \hat{I}$ yielding

$$\hat{I} = -\check{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_1}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}} = \frac{V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right) \quad \text{(A)} \tag{14.9}$$

The zero current cross-over point t_x, shown on figure 14.1b, can be found by solving equation (14.7) for t when $i_L = 0$, which yields

$$t_x = \tau\, \ell n\left(1 - \frac{\check{I}R}{V_s}\right) = \tau\, \ell n\left(1 + \frac{\hat{I}R}{V_s}\right) \quad \text{(s)} \tag{14.10}$$

The average thyristor current, $\overline{I}_{TH}$, average diode current, $\overline{I}_D$, and mean source current, $\overline{I}_s$ can be found by integration of the load current over the appropriated bounds.

$$\overline{I}_T = \frac{1}{t_2}\int_{t_x}^{t_1} i_L(t)\,dt = \frac{1}{t_2}\left[\frac{V_s}{R}(t_1 - t_o) + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - e^{\frac{-t_o}{\tau}}\right)\right] \tag{14.11}$$

where i_L is given by equation (14.7) and

$$\overline{I}_D = \frac{1}{t_2}\int_0^{t_x} -i_L(t)\,dt = \frac{1}{t_2}\left[-\frac{V_s}{R}t_x - \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_x}{\tau}} - 1\right)\right] \tag{14.12}$$

where i_L is given by equation (14.8)

Inspection of the source current waveform in figure 14.1b shows that the average source current is related to the average semiconductor device currents by

$$\overline{I}_s = 2\left(\overline{I}_{TH} - \overline{I}_D\right) = \frac{1}{t_2}\left[\frac{V_s}{R}t_1 + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - 1\right)\right] \tag{14.13}$$

The steady-state mean power delivered by the dc supply and absorbed by the resistive load component is given by

$$P_L = \frac{1}{t_1}\int_0^{t_1} V_s\, i_L(t)\ dt \ = \ V_s \bar{I}_s \qquad \text{(W)} \tag{14.14}$$

where $i_L(t)$ is given by equation (14.7). The mean load power can be used to determine the rms load current:

$$I_{Lrms} = \sqrt{P_L / R} = \sqrt{V_s \bar{I}_s / R} \qquad \text{(A)} \tag{14.15}$$

The rms output voltage is V_s and the output fundamental frequency f_o is $f_o = 1/2_{t_1} = 1/t_2$.
The instantaneous output voltage expressed as a Fourier series is given by

$$V_L = \frac{4}{\pi} V_s \sum_{n\ odd}^{\infty} \frac{1}{n} \sin n\omega_o t \qquad \text{(V)} \tag{14.16}$$

where $\omega_o = 2\pi f_o = 2\pi / t_2$ and for $n = 1$ the magnitude of the fundament frequency f_o is $4/\pi V_s$ which is an output rms fundamental voltage v_{o1} of

$$v_{o1} = \frac{2\sqrt{2}}{\pi} V_s = 0.90 V_s \qquad \text{(V)} \tag{14.17}$$

The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$\begin{aligned} i_L(\omega t) &= \frac{4}{\pi} V_s \sum_{n=1,3,5}^{\infty} \frac{1}{nZ_n} \sin\left(n\omega_o t - \phi_n\right) \\ &= \sum_{n=1,3,5}^{\infty} I_n \sin\left(n\omega_o t - \phi_n\right) \end{aligned} \tag{14.18}$$

where $I_n = \frac{4}{\pi}\frac{V_s}{nZ_n}$ whence $I_{n\,\text{rms}} = \frac{I_n}{\sqrt{2}}$

$$Z_n = \sqrt{R^2 + (n\omega_o L)^2}$$

$$\phi_n = \tan^{-1} n\omega_o L / R$$

The load power is given by the sum of each harmonic i^2R power component, that is

$$P_L = \sum_{n=1,3,5}^{\infty} \left(I_n / \sqrt{2}\right)^2 R = \sum_{n=1,3,5}^{\infty} I^2_{n\,rms} R \tag{14.19}$$

14.1.1ii - *Quasi-square-wave output*
The rms output voltage can be varied by producing a quasi-square output voltage ($2t_1=t_2$, $t_0<t_1$) as shown in figure 14.1c. After T_1 and T_2 have been turned on (state 10), at the angle π-α one device is turned off. If T_1 is turned off, the load current slowly freewheels through T_2 and D_4 (state 00) in a zero voltage loop according to

$$0 = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{14.20}$$

When T_2 is turned off and T_4 and T_3 turned on (state 01), the remaining load current rapidly reduces to zero through diodes D_3 and D_4. When the load current reaches zero, T_3 and T_4 become forward biased and the output current reverses through T_3 and T_4.

The output voltage shown in figure 14.1c consists of a sequence of non-zero voltages $\pm V_s$, alternated with zero output voltage periods. During the zero output period a diode and switch conduct, firstly T_1 and D_3 in the first period, and T_3 and D_1 in the second zero output period. In each case, a *zero voltage loop* is formed by a switch, diode, and the load. The next two zero output sequences would be T_2 and D_4 then T_4 and D_2, forming *alternating zero voltage loops* (sequence 10, 00, 01, 11, 10, ..) rather than repeating a continuous T_1 and D_3 then T_3 and D_1 sequence of zero voltage loops (sequence 10, 11, 01, 11, 10, .. or sequence 10, 00, 01, 00, 10, ..). By alternating the zero voltage loops (between states 00 and 11), losses are uniformly distributed between the semiconductors, device switching frequency is half that experienced by the load, and a finer output voltage resolution is achievable.
With reference to figure 14.lc, the load current i_L for an applied quasi square-wave voltage is defined as follows.

(i) $v_L > 0$

$$i_{L_I}(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - I_o\right) e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_o \tag{14.21}$$

for $I_o \le 0$ (A)

(ii) $v_L = 0$

$$i_{L_{II}}(t) = \hat{I}\, e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_1 - t_o \tag{14.22}$$

for $\hat{I} \ge 0$ (A)

(iii) $v_L < 0$

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + I_1\right) e^{\frac{-t}{\tau}} = -i_{L_I}(t) \qquad 0 \le t \le t_o \tag{14.23}$$

for $I_1 \ge 0$ (A)

The currents I_o , $\hat{I}$, and I_1 are given by

$$I_o = -\frac{V_s}{R}\ \frac{e^{\frac{-t_1+t_o}{\tau}} - e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \qquad \text{(A)} \tag{14.24}$$

$$\hat{I} = \frac{V_s}{R}\ \frac{1-e^{\frac{-t_o}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \qquad \text{(A)} \tag{14.25}$$

$$I_1 = -I_o \qquad \text{(A)} \tag{14.26}$$

The zero current cross-over instant, t_x, shown in figure 14.1c, is found by solving equation (14.21) for t when i_L equals zero current.

$$t_x = \tau\, \ell n\left(1 - \frac{I_o R}{V_s}\right) \tag{14.27}$$

The average thyristor current, $\bar{I}_{TH}$, average diode current, $\bar{I}_D$, and mean source current, $\bar{I}_s$ can be found by integration of the load current over the appropriated bounds (assuming alternating zero volt loops).

$$\bar{I}_T = \frac{1}{t_2}\int_{t_{s_T}}^{t_1} i_{L_T}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_0} i_{L_{TT}}(t)\,dt \qquad (14.28)$$

where i_L is given by equations (14.21) and (14.22) for the respective integrals, and

$$\bar{I}_D = \frac{1}{t_2}\int_0^{t_{s_T}} -i_{L_T}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_0} i_{L_{II}}(t)\,dt \qquad (14.29)$$

where i_L is given by equations (14.21) and (14.22) for the respective integrals.
Inspection of the source current waveform in figure 14.1b shows that the average source current is related to the average semiconductor device currents by

$$\bar{I}_s = \frac{1}{t_1}\int_0^{t_0} i_{L_I}(t)dt = 2\left(\bar{I}_{TH} - \bar{I}_D\right) \qquad (14.30)$$

The steady-state mean load and source powers are

$$P_L = \frac{1}{t_1}\int_0^{t_0} V_s\, i_L(t)\;\; dt \;\; = \;\; V_s \bar{I}_s \qquad \text{(W)} \qquad (14.31)$$

where $i_L(t)$ is given by equation (14.21). The mean load power can be used to determine the rms load current:

$$I_{Lrms} = \sqrt{P_L / R} = \sqrt{V_s \bar{I}_s / R} \qquad \text{(A)} \qquad (14.32)$$

The output fundamental frequency f_o is $f_o = 1/2t_1 = 1/t_2$.
The variable rms output voltage is

$$\begin{aligned} v_{rms} &= \sqrt{\frac{1}{t_1}\int_0^{t_0} V_s^2\,dt} \\ &= \sqrt{1-\alpha/\pi}\;\; V_s \end{aligned} \qquad (14.33)$$

and the output fundamental frequency f_o is $f_o = 1/t_2$. This equation for rms output voltage shows that only the n^{th} harmonic can be eliminated when $\cos \tfrac{1}{2} n\alpha = 0$, that is for $\alpha = \pi / n$. In so eliminating the n^{th} harmonic, from equation (14.34), the magnitude of the fundamental is reduced to $4/\pi V_s \cos \alpha/n$.
The output voltage V_L in its Fourier coefficient series form is given by

$$V_L = \frac{4}{\pi} V_s \sum_{n\,odd}^{\infty} \frac{\cos \tfrac{1}{2} n\alpha}{n} \sin n\omega_o t \qquad \text{(V)} \qquad (14.34)$$

and for $n = 1$, the rms fundamental of the output voltage v_{o1} is given by

$$v_{o1} = \frac{2\sqrt{2}}{\pi} V_s \cos \tfrac{1}{2}\alpha = 0.90 \times V_s \times \cos \tfrac{1}{2}\alpha \qquad \text{(V)} \qquad (14.35)$$

The characteristics of these load voltage harmonics are shown in figure 14.2.
The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$\begin{aligned} i_L(\omega t) &= \frac{V_L}{Z_L} = \frac{4}{\pi} V_s \sum_{n=1,3,..}^{\infty} \frac{\cos \tfrac{1}{2} n\alpha}{nZ_n} \sin\left(n\omega_o t - \phi_n\right) \\ &= \sum_{n=1,3,5}^{\infty} I_n \sin\left(n\omega_o t - \phi_n\right) \end{aligned} \qquad (14.36)$$

where $I_n = \frac{4}{\pi}\frac{V_s}{nZ_n}$ whence $I_{n\,\text{rms}} = \frac{I_n}{\sqrt{2}}$

$$Z_n = \sqrt{R^2 + (n\omega_o L)^2}$$

$$\phi_n = \tan^{-1} n\omega_o L / R$$

The load power is given by the sum of each harmonic i^2R power component, that is

$$P_L = \sum_{n=1,3,5}^{\infty} \left(I_n/\sqrt{2}\right)^2 R = \sum_{n=1,3,5}^{\infty} I_{n\,rms}^2\, R \qquad (14.37)$$

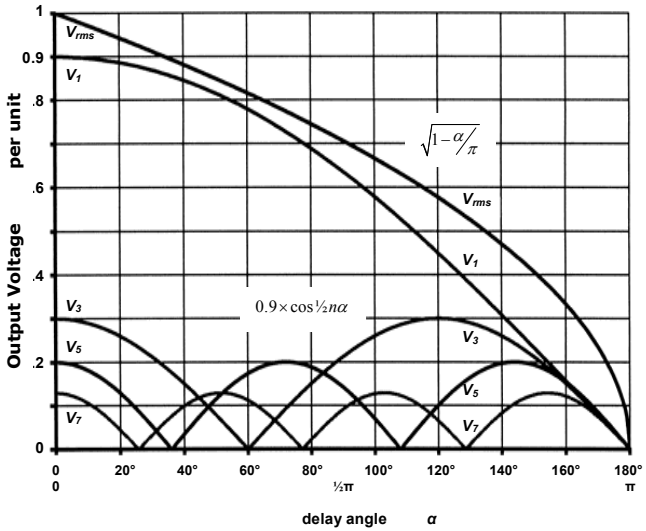

Figure 14.2. *Full bridge inverter output voltage harmonics normalised with respect to square wave rms output voltage, V_{rms}=V_s.*

A variation of the basic four-switch dc to ac single-phase H-bridge is the half-bridge version where two series switches (one pole or leg) and diodes are replaced by a split two-capacitor source, as shown in figure 14.2. This reduces the number of semiconductors and gate circuit requirements, but at the expense of halving the maximum output voltage. Example 14.3 illustrates the half-bridge and its essential features. Behaviour characteristics are as for the full-bridge, square-wave, single-phase inverter but V_s is replaced by $\frac{1}{2}V_s$ in the appropriate equations. Only a square-wave output voltage can be obtained. Since zero volt loops cannot be created, no rms voltage control is possible. The rms output voltage is $\frac{1}{2}V_s$.

Example 14.1a: ***Single-phase H-bridge with an L-R load***

A single-phase H-bridge inverter, as shown in figure 14.la, supplies a 10 ohm resistance with inductance 50 mH from a 340 V dc source. If the bridge is operating at 50 Hz, determine the load rms voltage and current and steady-state current waveforms with

i. a square-wave output
ii. a quasi-square-wave output with a 50 per cent on-time.

Solution

The time constant of the load, $\tau = 0.05\text{mH}/10\Omega = 5$ ms and $t_2 = 20$ms.

i. The output voltage rms value is 340 V ac.

Equation (14.9) gives the load current at the time when the supply polarity is reversed across the load, as shown in figure 14.lb, that is

$$\hat{I} = -\check{I} = \frac{V_s}{R}\frac{1-e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \qquad \text{(A)}$$

where $t_1 = 10$ ms. Therefore

$$\hat{I} = -\check{I} = \frac{340\text{V}}{10\Omega}\times\frac{1-e^{-2}}{1+e^{-2}} \qquad \text{(A)}$$
$$= 25.9\text{A}$$

When $v_L = +340$ V, from equation (14.7) the load current is given by

$$i_L = 34-(34+25.9)\,e^{-200t} = 34-59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

From equation (14.10) the zero current cross-over time, t_x, occurs at

$5\text{ms}\times\ell n\left(1+25.9\text{A}\times 10\Omega/340\text{V}\right) = 2.83$ ms after load voltage reversal.

When $v_L = -340$ V, from equation (14.8) the load current is given by

$$i_L = -34+(34+25.9)\,e^{-200t} = -34+59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

The mean power delivered to the load is given by equation (14.14), that is

$$P_L = \frac{1}{10\text{ms}}\int_0^{10ms} 340\text{V}\times\{34-59.9\times e^{-200t}\}\,dt$$
$$= 2755\text{ W}$$

From $P = i^2R$, the load rms current is

$$i_{Lrms} = \sqrt{P_L/R} = \sqrt{2755\text{W}/10\Omega} = 16.60\text{A}$$

ii. The quasi-square output voltage has a 5 ms on-time, t_o, and a 5 ms period of zero volts.

From equation (14.33) the rms output voltage is

$$V_s\sqrt{1-5\text{ms}/10\text{ms}} = V_s/\sqrt{2} = 240\text{V rms}.$$

The current during the different intervals is specified by equations (14.21) to (14.26). Alternately, the steady-state load current equations can be specified by determining the load current equations for the first few cycles at start-up until

steady-state conditions are attained.

First 5 ms on-period when $v_L = 340$ V and initially $i_L = 0$ A

$$i_L = 34 - 34\,e^{-200t}$$

and at 5ms, $i_L = 21.5$A

First 5 ms zero-period when $v_L = 0$ V

$$i_L = 21.5\,e^{-200t}$$

and at 5ms, $i_L = 7.9$A

Second 5 ms on-period when $v_L = -340$ V

$$i_L = -34 + (34+7.9)\,e^{-200t}$$

with $i_L = 0$ at 1 ms and ending with $i_L = -18.6$ A

Second 5 ms zero-period when $v_L = 0$ V

$$i_L = -18.6\,e^{-200t}$$

ending with $i_L = -6.8$A

Third 5 ms on-period when $v_L = 340$ V

$$i_L = 34 - (34+6.8)\,e^{-200t}$$

with $i_L = 0$ at 0.9 ms and ending with $i_L = 19.0$ A

Third 5 ms zero-period when $v_L = 0$ V

$$i_L = 19.0\,e^{-200t}$$

ending with $i_L = 7.0$A

Fourth 5 ms on-period when $v_L = -340$ V

$$i_L = -34 + (34+7.0)\,e^{-200t}$$

with $i_L = 0$ at 0.93 ms and ending with $i_L = -18.9$ A

Fourth 5 ms zero-period when $v_L = 0$ V

$$i_L = -18.9\,e^{-200t}$$

ending with $i_L = -7.0$A

Steady-state load current conditions have been reached and the load current waveform is as shown in figure 14.1c. Convergence of an iterative solution is more rapid if the periods considered are much longer than the load time constant.

The mean load power for the quasi-square wave is given by

$$P_L = \frac{1}{10\text{ms}}\int_0^{5ms} 340\text{V}\times\{34-41\times e^{-200t}\}\,dt$$
$$= 1378\text{ W}$$

The load rms current is

$$i_{Lrms} = \sqrt{P_L/R} = \sqrt{1378\text{W}/10\Omega} = 11.74\text{A}$$

♣

Example 14.1b: ***H-bridge inverter ac output factors***

In each waveform case of example 14.1a calculate

i. the average and peak current in the switches
ii. the average and peak current in the diodes
iii. the peak blocking voltage of each semiconductor type
iv. the average source current
v. the harmonic factor and distortion factor of the lowest order harmonic
vi. the total harmonic distortion

Solution

Square-wave

i. The peak current in the switch is $\hat{I}$ = 25.9 A and the current zero cross-over occurs at t_x=2.83ms. The average switch current, from equation (14.11) is

$$\bar{I}_T = \frac{1}{20\text{ms}} \int_{2.83\text{ms}}^{10\text{ms}} (34 - 59.9\, e^{-200t})\, dt$$
$$= 5.71 \text{ A}$$

ii. The peak diode current is 25.9 A. The average diode current from equation (14.12) is

$$\bar{I}_D = \frac{1}{20\text{ms}} \int_{0}^{2.83\text{ms}} (34 - 59.9\, e^{-200t})\, dt$$
$$= 1.66 \text{ A}$$

iii. The maximum blocking voltage of each device is 340 V dc.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_{TH} - \bar{I}_D\right)$$
$$= 2\times\left(5.71\text{A} - 1.66\text{A}\right) = 8.10\text{A}$$

This results in the supply delivery power of 340Vdc × 8.10A = 2754W

v. From equation (14.16), with the third as the lowest harmonic, the distortion factors are

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \frac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{3V_1}\right| = \frac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi. From equation (14.16)

$$thd = \sqrt{\sum\left(\frac{V_n}{n}\right)^2}\Big/V_1$$
$$= \sqrt{\left(\tfrac{1}{3}\right)^2 + \left(\tfrac{1}{5}\right)^2 + \left(\tfrac{1}{7}\right)^2 + \ldots..}$$
$$= 46.2 \text{ per cent}$$

Quasi-square-wave, $\alpha = \tfrac{1}{2}\pi$ (5 ms) and from equation (14.27) t_x= 0.93ms

i. The peak switch current is 18.9 A.

From equation (14.28) the average switch current, using alternating zero volt loops, is

$$\bar{I}_T = \frac{1}{20\text{ms}} \int_{0.93\text{ms}}^{5\text{ms}} (34 - 41e^{-200t})\, dt \; + \frac{1}{40\text{ms}} \int_{0}^{5\text{ms}} 19e^{-200t} dt$$
$$= 2.18 + 1.50 = 3.68 \text{ A}$$

ii. The peak diode current (and peak switch current) is 18.9 A. The average diode current, from equation (14.29), when using alternating zero volt loops, is given by

$$\bar{I}_D = \frac{1}{20\text{ms}} \int_{0}^{0.93\text{ms}} \left(-34 + 41e^{-200t}\right) dt + \frac{1}{40\text{ms}} \int_{0}^{5\text{ms}} 19e^{-200t} dt$$
$$= 0.16 + 1.50 = 1.66 \text{ A}$$

iii. The maximum blocking voltage of each device type is 340 V.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_{TH} - \bar{I}_D\right) = 2\times\left(3.68\text{A} - 1.66\text{A}\right) = 4.04\text{A}$$

This results in the supply delivery power of 340Vdc × 4.04A = 1374W

v. The harmonics are given by equations (14.1) to (14.3)

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \frac{1}{3\sqrt{2}} \Big/ \frac{1}{\sqrt{2}} = \frac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{nV_1}\right| = \frac{\rho_3}{n} = \frac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi.

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]}\Big/V_1$$
$$= \sqrt{\left(\frac{1}{3}\right)^2 + \left(\frac{-1}{5}\right)^2 + \left(\frac{1}{7}\right)^2 + \left(\frac{1}{9}\right)^2 + \ldots}$$
$$= 46.2 \text{ per cent}$$

♣

Example 14.2: ***Harmonic analysis of H-bridge with an L-R load***

For each delay case (α = 0° and α = 90°) in example 14.1, using Fourier voltage analysis, determine (ignore harmonics above the 10th):

i. the magnitude of the fundamental and first four harmonics
ii. the load rms voltage and current
iii. load power
iv. load power factor

Solution

The appropriate harmonic analysis is outline in the following table, for α = 0° and α = 90°.

n	Z_n	V_n	I_n	V_n (α=90°)	I_n
harmonic	$\sqrt{R^2+(2\pi 50nL)^2}$	$\frac{0.9V_s}{n}$	V_n/Z_n	$\frac{0.9V_s}{n}\cos(\frac{1}{2}n\alpha)$	V_n/Z_n
	Ω	V	A	V	A
1	18.62	306	16.43	216.37	11.62
3	48.17	102	2.12	-72.12	-1.50
5	79.17	61.2	0.77	-43.28	-0.55
7	110.41	43.71	0.40	30.91	0.28
9	141.72	34	0.24	24.04	0.17
		332.95V	16.59A	235.43V	11.73A

i The magnitude of the fundamental voltage is 306V for the square wave and is reduced to 216V when a phase delay angle of 90° is introduced. The table shows that the harmonics magnitudes reduce as the harmonic order increases.

ii The rms load current and voltage can be derived by the square root of the sum of the squares of the fundamental and harmonic components, that is, for the current

$$i_{rms} = \sqrt{I_1^2 + I_3^2 + I_5^2 + ...}$$

The load rms currents, from the table, are 16.59A and 11.73A, which agree with the values obtained in example 14.1a. Notice that the predicted rms voltages of 333V and 235V differ significantly from the values in example 14.1a, given by $V_s\sqrt{1-\alpha/\pi}$, namely 340V and 240.4V respectively. This is because the magnitude of the harmonics higher in order than 10 are not insignificant. The error introduced into the rms current value by ignoring these higher order voltages is insignificant because the impedance increases approximately proportionally with harmonic number, hence the resultant current is becomes smaller the order increases.

iii The load power is the load i^2R loss, that is

$$P_L = i_{rms}^2 R = 16.59^2 \times 10\Omega = 2752\text{W} \quad \text{for} \quad \alpha = 0$$
$$P_L = i_{rms}^2 R = 11.73^2 \times 10\Omega = 1376\text{W} \quad \text{for} \quad \alpha = 90°$$

iv The load power factor is the ratio of real power dissipated to apparent power, that is

$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{2752\text{W}}{16.59\text{A} \times 340\text{V}} = 0.488 \text{ for } \alpha = 0$$
$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{1376\text{W}}{11.79\text{A} \times 240.4\text{V}} = 0.486 \text{ for } \alpha = 90°$$

♣

Example 14.3: ***Single-phase half-bridge with an L-R load***

A single-phase half-bridge inverter as shown in the figure 14.3, supplies a 10 ohm resistance with inductance 50 mH from a 340 V dc source. If the bridge is operating at 50 Hz, determine for the square-wave output

v. steady-state current waveforms
vi. the load rms voltage
vii. the peak load current and its time domain solution, $i_L(t)$
viii. the average and peak current in the switches
ix. the average and peak current in the diodes
x. the peak blocking voltage of each semiconductor type
xi. the power delivered to the load and rms load current

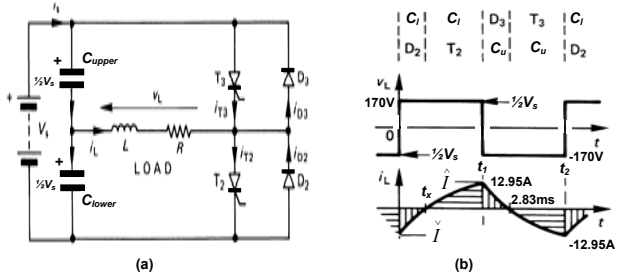

Figure 14.3. *GCT thyristor single-phase half-bridge inverter: (a) circuit diagram and (b) square-wave output voltage.*

Solution

From examples 14.1 and 14.2, τ = 5ms.

i. Figure 14.3 shows the output voltage and current waveforms, with various circuit component current waveforms superimposed. Note that no zero voltage loops can be created with the half-bridge. Only load voltages $\pm\frac{1}{2}V_s$, that is ±170V, are possible.

ii. The output voltage swing is $\pm\frac{1}{2}V_s$, ±170V, thus the rms output voltage is $\frac{1}{2}V_s$, 170V. This is, half that of the full-bridge inverter using the same magnitude source voltage V_s, 340V.

iii. The peak load current is half that given by equation (14.9), that is

$$\hat{I} = \frac{½V_s}{R}\frac{1-e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} = \frac{½V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right)$$

$$= \frac{½\times 340\text{V}}{10\Omega} \times \tanh\left(\frac{10\text{ms}}{2\times 5\text{ms}}\right) = 12.95\text{A}$$

The load current waveform is defined by equations (14.7) and (14.8), specifically

$$i_{L_I}(t) = \frac{½V_s}{R} - \left(\frac{½V_s}{R} - \check{I}\right)e^{\frac{-t}{\tau}}$$

$$= \frac{½\times 340\text{V}}{10\Omega} - \left(\frac{½\times 340\text{V}}{10\Omega} + 12.95\text{A}\right)e^{\frac{-t}{5\text{ms}}}$$

$$= 17 - 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

and

$$i_{L_{II}}(t) = -\frac{½V_s}{R} + \left(\frac{½V_s}{R} + \hat{I}\right)e^{\frac{-t}{\tau}}$$

$$= -\frac{½\times 340\text{V}}{10\Omega} + \left(\frac{½\times 340\text{V}}{10\Omega} + 12.95\right)e^{\frac{-t}{5\text{ms}}}$$

$$= -17 + 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

By halving the effective supply voltage, the current swing is also halved.

iv. The peak switch current is $\hat{I} = 12.95\mathbf{A}$.
The average switch current is given by

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{2.83\text{ms}}^{10\text{ms}} (17 - 29.95e^{\frac{-t}{5\text{ms}}})\, dt$$

$$= 2.86 \text{ A}$$

v. The peak diode current is $\hat{I} = 12.95\text{A}$.
The average diode current is given by

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_{0}^{2.83\text{ms}} \left(17 - 29.95e^{\frac{-t}{5\text{ms}}}\right) dt$$

$$= 0.83 \text{ A}$$

vi. When a switch or diode of a parallel pair conduct, the complementary pair of devices experience a voltage V_s, 340V. Thus although the load experiences half the supply voltage, the semiconductors experience twice that voltage, the same as with the full bridge inverter.

vii. The load power is found by averaging the instantaneous load power, that is

$$P_L = \frac{1}{10\text{ms}}\int_0^{10\text{ms}} 170\text{V} \times \left(17 - 29.95 \times \text{e}^{-200t}\right)\, dt$$

$$= 638.5 \text{ W}$$

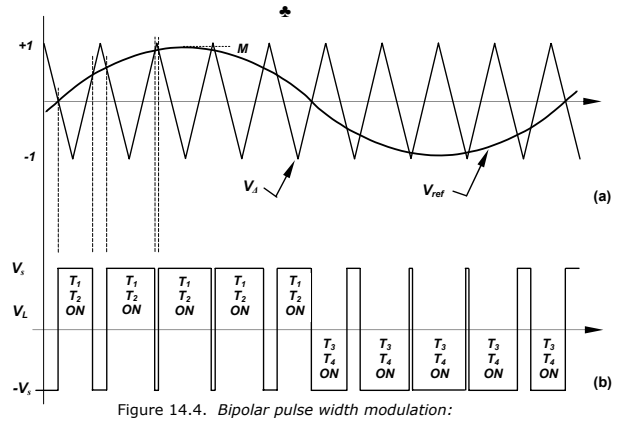

Figure 14.4. *Bipolar pulse width modulation: (a) carrier and modulation waveforms and (b) resultant load pwm waveform.*

14.1.1i - *PWM-wave output*

The output voltage and frequency of a single-phase voltage-fed inverter bridge can be control using one of two forms of pulse-width modulation, termed:

- bipolar
- multi-level, usually called unipolar

Both pwm techniques have been analysed extensively for dc voltage outputs when applied to the two quadrant and four quadrant dc choppers considered in Chapter 13, sections 13.5 and 13.6. It will be seen that the same triangular modulation principles can be applied and extended, when producing low-harmonic single-phase ac output voltages and currents. The main voltage output difference between the two methods is the harmonic content near the carrier frequency and its harmonics. Three-phase pwm is a naturally extension to the single-phase case, except single-phase pwm offers more degrees of flexibility than its application to three phase inverters, although three-phase pwm does have the attribute of triplen harmonic cancellation.

Bipolar pulse width modulation
Bipolar modulation is the simplest pwm method and involves comparing a fixed frequency triangular carrier with the ac waveform desired, called the modulation waveform. The modulation is usually a sinusoid of magnitude (modulation index) M such that $0 \le M \le 1$.

The waveforms in figure 14.4 shown that the load voltage V_L swings between the two voltage levels, $+V_s$ and $-V_s$, (hence the term bipolar output voltage), according to

- T_1 and T_2 are on when $v_{ref} > v_\Delta$ (T_3 and T_4 are off) such that $V_L = +V_s$
- T_3 and T_4 are on when $v_{ref} < v_\Delta$ (T_1 and T_2 are off) such that $V_L = -V_s$

Multi-level pulse width modulation

Two multilevel output voltage techniques can be use with the single-phase voltage fed ac bridges. Two triangular carries displaced by 180° are used.

i. The waveforms in figure 14.5 shown that the load voltage V_L swings between the two voltage levels, $+V_s$ and $-V_s$, with interspaced zero periods (hence the term multilevel, specifically three-level in this case, 0V and $\pm V_s$), according to

- T_1 is on when $v_{ref} > v_\Delta$ such that $V_{ao} = +V_s$
- T_4 is on when $v_{ref} < v_\Delta$ such that $V_{ao} = 0V$

- T_3 is on when $v_{ref} < -v_\Delta$ such that $V_{bo} = V_s$
- T_2 is on when $v_{ref} > -v_\Delta$ such that $V_{bo} = 0V$

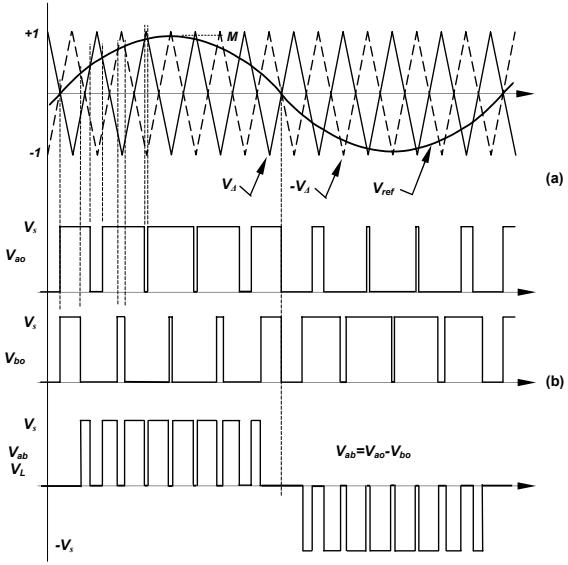

Figure 14.5. *Multilevel (3 level) pulse width modulation: (a) carriers and modulation waveforms and (b) resultant load pwm waveforms.*

The multilevel load output voltage is the difference between the two leg voltage waveforms and can be defines as follows:

- T_1 and T_2 are on such that $V_{ao} = +V_s$, $V_{bo} = 0V$, $V_{ab} = +V_s$
- $T_2$and T_3 are on such that $V_{ao} = 0V$, $V_{bo} = +V_s$, $V_{ab} = -V_s$

- T_1 and T_3 are on such that $V_{ao} = +V_s$, $V_{bo} = +V_s$, $V_{ab} = 0V$
- T_2 and T_4 are on such that $V_{ao} = 0V$, $V_{bo} = 0V$, $V_{ab} = 0V$

The two zero output states are interleaved to balance switching losses between all four bridge switches. Device switching is at the carrier frequency, but the bridge load voltage experiences twice the leg switching frequency since the two carriers are displaced by 180°.

ii. A second multilevel output voltage approach is shown in figure 14.11, where the triangular carriers are not only displaced by 180° in time, but are vertically displaced, as for multilevel inverter pwm generation, which is to be considered in section 14.4. The upper triangle modulates reference values greater than zero, while the lower triangle modulates when the reference is less than zero.

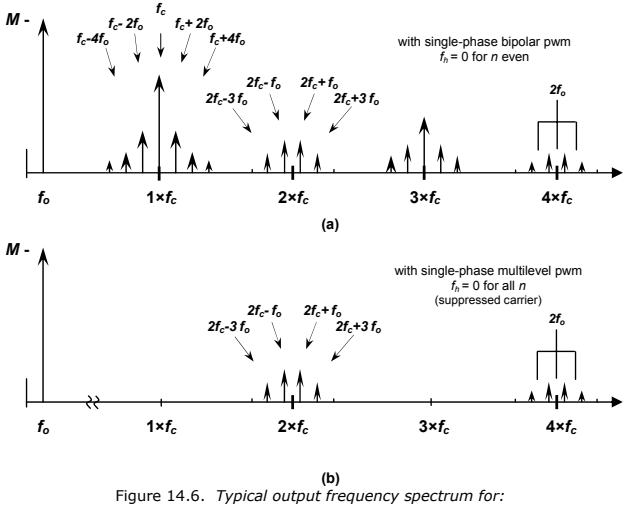

Figure 14.6. *Typical output frequency spectrum for: (a) bipolar pwm and (b) multilevel pwm.*

Spectral comparison between bipolar and multilevel pwm waveforms

The key features of the H-bridge output voltage with bipolar pwm are (fig 14.6a):

- triangular carrier has only odd Fourier component, so the output spectrum only has carrier components at odd harmonics of the carrier frequency

- the first carrier components occur at the carrier frequency, f_c
- side-band components occur space by $2f_o$ from other components, around each multiple of the carrier frequency

From figure 14.6b, the key features of the H-bridge output voltage with multilevel pwm are:

- the output switching frequency is double $2f_c$ each leg switching frequency f_c, since the switching of each leg is time shifted, hence the first carrier related components in the output occur at $2f_c$ and then at multiples of $2f_c$
- no triangular carrier Fourier components exist in the output voltage since the two carriers are 180° apart, effectively cancelling one another in spectrum terms
- side-band components occur space by $2f_o$ from other components, around each multiple of the carrier frequency $2f_c$

14.*1.2 Three-phase voltage-fed inverter bridge*

The basic dc to three-phase voltage-fed inverter bridge is shown in figure 14.7. It comprises six power switches together with six associated reactive feedback diodes. Each of the three inverter legs operates at a relative time displacement (phase) of ⅔π, 120°.

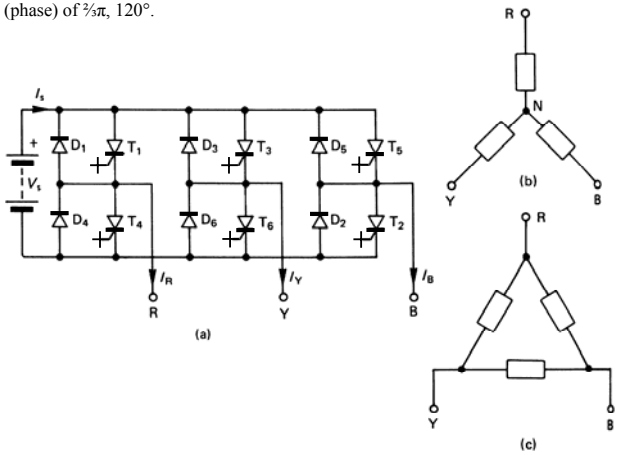

Figure 14.7. *Three-phase inverter circuit:*
(a) GCT thyristor bridge inverter; (b) star-type load; and (c) delta-type load.

14.1.2i - 180° (π) conduction

Figure 14.8 shows inverter bridge quasi-square output voltage waveforms for a 180° switch conduction pattern. Each switch conducts for 180°, such that no two semiconductor switches across the voltage rail conduct simultaneously. Six patterns exist for one output cycle and the rate of sequencing these patterns specifies the bridge output frequency. The conducting switches during the six distinct intervals are shown and can be summarised as in Table 14.1.

Table 14.1. Quasi-square-wave six conduction states - *180° conduction*.

Interval	***Three** conducting switches*								*leg state*	*voltage vector*
1	T_1	T_2	T_3						101	v_5
2		T_2	T_3	T_4					001	v_1
3			T_3	T_4	T_5				011	v_3
4				T_4	T_5	T_6			010	v_2
5					T_5	T_6	T_1		110	v_6
6						T_6	T_1	T_2	100	v_4

The three output voltage waveforms can be derived by analysing a resistive star load and considering each of the six connection patterns, as shown in figure 14.9. Effectively the resistors representing the three-phase load are sequentially cycled anticlockwise one at a time, being alternately connected to each supply rail. The output voltage is independent of the load, as it is for all voltage source inverters.
Alternatively, the generation of the three-phase voltages can be analysed analytically by using the rotating *voltage space vector* technique. With this approach, the output voltage state from each of the three inverter legs (or poles) is encoded as summarised in the table 14.1, where a '1′ signifies the upper switch in the leg is on, while a '0′ means the lower switch is on in that leg. The resultant binary number (one bit for each of the three inverter legs), represents the output voltage vector number (when converted to decimal). The six voltage vectors are shown in figure 14.10 forming sextant boundaries, where the quasi-square output waveform in figure 14.8b is generated by stepping instantaneously from one vector position to another in an anticlockwise direction. Note that the rotational stepping sequence is arranged such that when rotating in either direction, only one leg changes state, that is, one device turns off and then the complementary switch of that leg turns on, at each step. This minimises the inverter switching losses. The dwell time of the created rotating vector at each of the six vector positions, is ⅓π ($\frac{1}{6}T$) of the cycle period (T). Note that the line-to-line zero voltage states 000 and 111 are not used. These represent the condition when ***either*** all the upper switches (T_1, T_3, T_5) are on ***or*** all the lower switches (T_2, T_4, T_5) are switched on. Phase reversal can be obtained by interchanging two phase outputs, or as is the preferred method, the direction of the rotating vector sequence is reversed. Reversing is therefore effectively achieved by back-tracking along each output waveform.

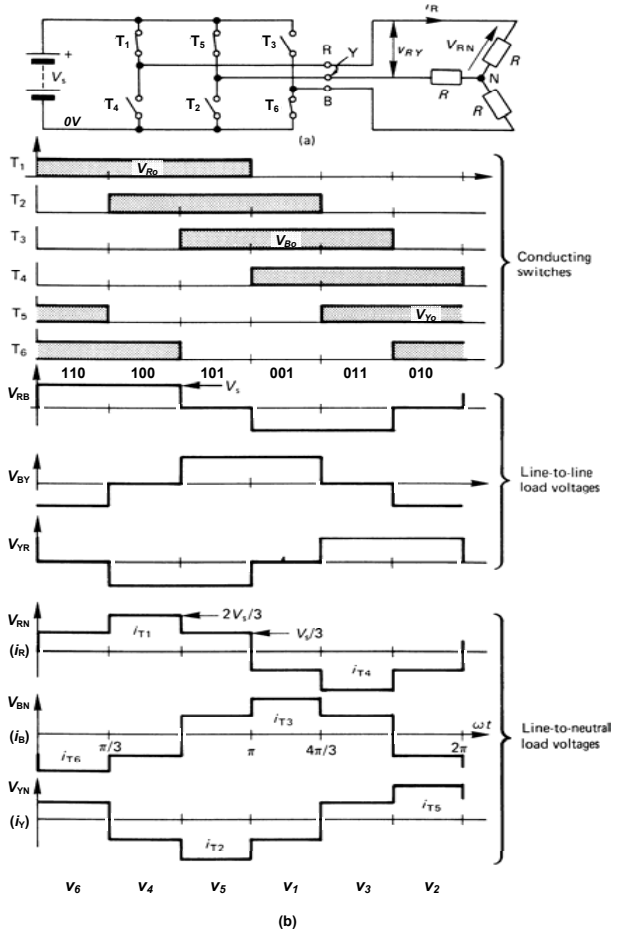

Figure 14.8. *A three-phase bridge inverter employing 180° switch conduction with a resistive load: (a) the bridge circuit showing T_1, T_5, and T_6 conducting (leg state* v_6 **:– 110**) *and (b) circuit voltage and current waveforms with each of six sequential output voltage vectors identified.*

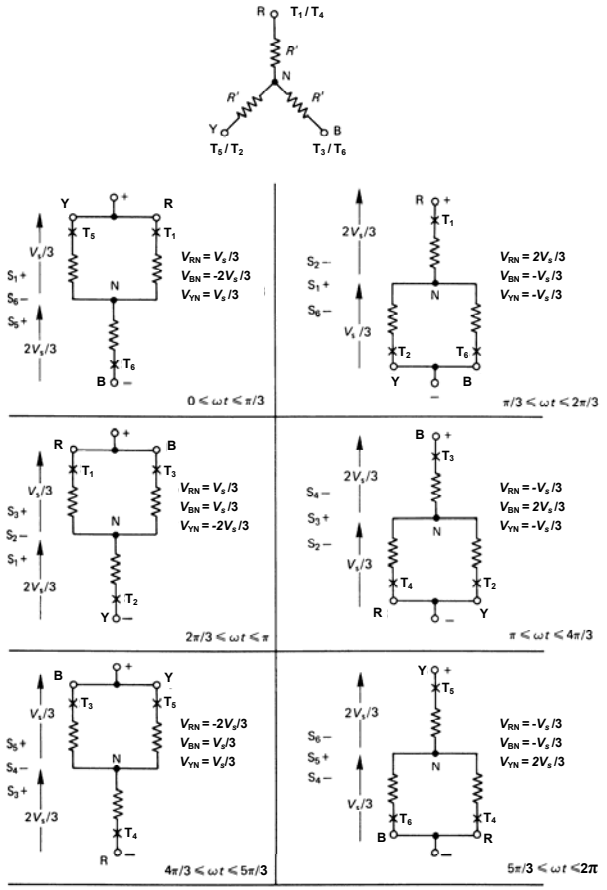

Figure 14.9. *Determination of the line-to-neutral voltage waveforms for a balanced resistive load and 180° conduction as illustrated in figure 14.8.*

With reference to figure 14.8b, the line-to-load neutral voltage Fourier coefficients are given by

$$V_{n_{L-N}} = \frac{2}{3\pi} V_s \frac{\left(2 + \cos\frac{n\pi}{3} - \cos\frac{2n\pi}{3}\right)}{n} \qquad (14.38)$$

The line-to-load neutral voltage is therefore

$$V_{n_{L-L}} = \frac{2}{\pi} V_s \sum_{\substack{n=6r\pm1 \\ r=1}}^{\infty} \frac{\sin \omega t}{n} \qquad r = 1, 2, 3, .. \qquad (14.39)$$

that is

$$v_{RN} = \frac{2}{\pi} V_s \left[\sin \omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.40)$$

similarly for v_{YN} and v_{BN}, where ωt is substituted by $\omega t + \frac{2}{3}\pi$ and $\omega t - \frac{2}{3}\pi$ respectively.

The line-to-line voltage, from equation (14.34) with $\alpha = \frac{1}{3}\pi$, gives Fourier coefficients defined by

$$V_{n_{L-L}} = \frac{4}{\pi} V_s \frac{\left(\cos\frac{n\pi}{6}\right)}{n} \qquad (14.41)$$

The line-to-line voltage is thus

$$V_{n_{L-L}} = \frac{2\sqrt{3}}{\pi} V_s \sum_{\substack{n=6r\pm1 \\ r=1}}^{\infty} \left\|\cos\frac{n\pi}{6}\right\| \frac{\sin \omega t}{n} \qquad r = 1, 2, 3, \ldots \qquad (14.42)$$

(the $\| \ \|$ symbol provides the sign), that is

$$v_{RB} = \frac{2\sqrt{3}}{\pi} V_s \left[\sin \omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \qquad (14.43)$$

and similarly for v_{BY} and v_{YR}. Figure 14.8b shows that v_{RB} is shifted $\frac{1}{6}\pi$ with respect to v_{RN}, hence to obtain the three line voltages while maintaining a v_{RN} reference, ωt should be substituted with $\omega t + \frac{1}{6}\pi$, $\omega t - \frac{1}{2}\pi$ and $\omega t - \frac{5}{6}\pi$, respectively.

Since the interphase voltages consist of two square waves displaced by $\frac{2}{3}\pi$, no triplen harmonics (3, 6, 9, . . .) exist. The outputs comprise harmonics given by the series $n = 6r \pm 1$ where $r \geq 0$ and is an integer. The nth harmonic has a magnitude of $1/n$ relative to the fundamental.

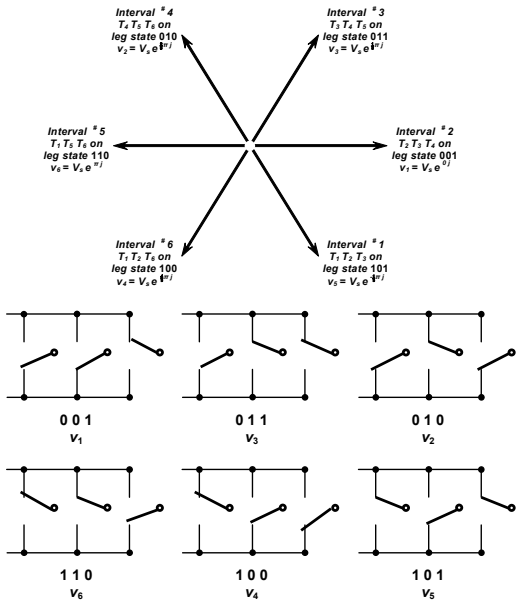

Figure 14.10. *Generation and arrangement of the six quasi-square inverter output voltage states.*

By examination of the interphase output voltages in figure 14.8 it can be established that the mean half-cycle voltage is $\frac{2}{3}V_s$ and the rms value is $\sqrt{\frac{2}{3}}\ V_s$, namely 0.816 V_s. From equation (14.43) the rms value of the fundamental is $\sqrt{6}\ V_s / \pi$, namely 0.78 V_s, that is $3/\pi$ times the total rms voltage value.

The three-phase inverter output voltage properties are summarised in Table 14.2.

Table 14.2. Quasi-squarewave voltage properties

Conduction period	Fundamental voltage		Characteristic		
	peak	rms	Total rms	Distortion Factor	THD
	$\hat{V}_1$	V_1	V_{rms}	μ	thd
180°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{2}{\pi}V_s = 0.637V_s$	$\frac{\sqrt{2}}{\pi}V_s = 0.450\,V_s$	$\frac{\sqrt{2}}{3}V_s = 0.471V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{2\sqrt{3}}{\pi}V_s = 1.10\,V_s$	$\frac{\sqrt{6}}{\pi}V_s = 0.78\,V_s$	$\sqrt{\frac{2}{3}}V_s = 0.816V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
120°	**(V)**	**(V)**	**(V)**		
Phase Voltage $V_{L\text{-}N}$	$\frac{\sqrt{3}}{\pi}V_s = 0.551\,V_s$	$\frac{\sqrt{6}}{2\pi}V_s = 0.390\,V_s$	$\frac{1}{\sqrt{6}}V_s = 0.408V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{3}{\pi}V_s = 0.955V_s$	$\frac{3}{\sqrt{2}\pi}V_s = 0.673\,V_s$	$\frac{1}{\sqrt{2}}V_s = 0.707V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$

***14.1.2ii* - 120° (⅔π) conduction**

The basic three-phase inverter bridge in figure 14.7 can be controlled with each switch conducting for 120°. As a result, at any instant only two switches (one upper and one non-complementary lower) conduct and the resultant quasi-square output voltage waveforms are shown in figure 14.11. A 60° (⅓π), dead time exists between two series switches conducting, thereby providing a safety margin against *simultaneous conduction* of the two series devices (for example T_1 and T_4) across the dc supply rail. This safety margin is obtained at the expense of a lower semi-conductor device utilisation and rms output voltage than with 180° device conduction. The device conduction pattern is summarised as in Table 14.3.

Figure 14.8b for 180° conduction and 14.11b for 120° conduction show that the line to neutral voltage of one conduction pattern is proportional to the line-to-line voltage of the other. That is from equation (14.34) with $\alpha = ⅓\pi$

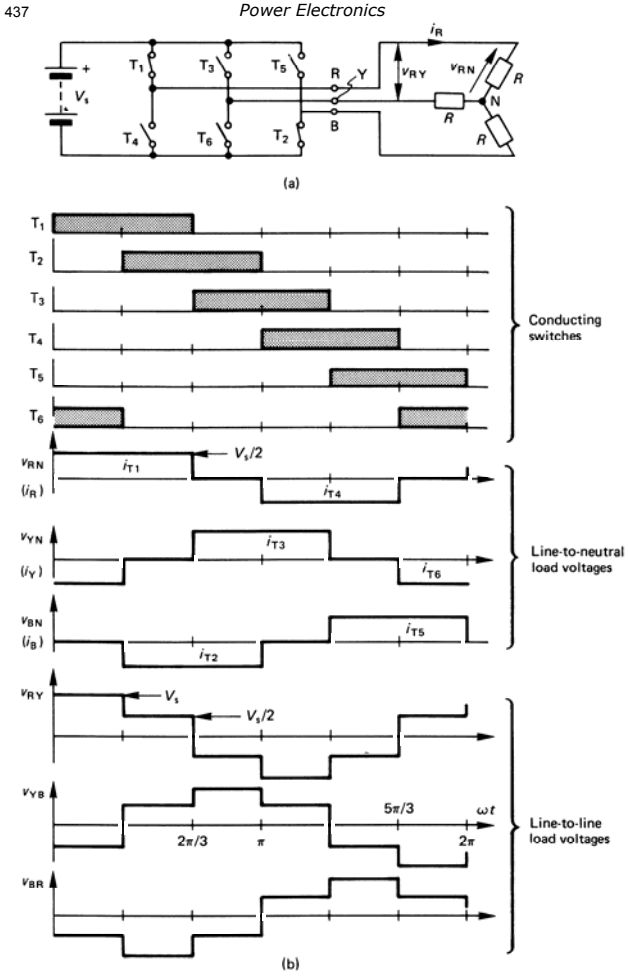

Figure 14.11. *A three-phase bridge inverter employing 120° switch conduction with a resistive star load: (a) the bridge circuit showing T_1 and T_2 conducting and (b) circuit voltage and current waveforms.*

$$v_{RN}\left(\tfrac{1}{3}\pi\right) = \tfrac{1}{2}v_{RY}\left(\pi\right) = \frac{\sqrt{3}}{\pi}V_s\left[\sin\omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \tag{14.44}$$

and

$$v_{RY}\left(\tfrac{1}{3}\pi\right) = \tfrac{3}{2}v_{RN}\left(\pi\right) = \frac{3}{\pi}V_s\left[\sin\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots\right] \quad \text{(V)} \tag{14.45}$$

Also $v_{RY} = \sqrt{3}\, v_{RN}$ and the phase relationship between these line and phase voltages, of $\frac{1}{6}\pi$, has not been retained. That is, with respect to figure 14.11b, substitute ωt with $\omega t + \frac{1}{6}\pi$ in equation (14.44) and $\omega t + \frac{1}{3}\pi$ in equation (14.45).
The output voltage properties for both 120° and 180° switch conduction are summarised in the Table 14.2.

Table 14.3. Quasi-squarewave conduction states - *120° conduction*.

Interval	***Two** conducting devices*						
1	T_1	T_2					
2		T_2	T_3				
3			T_3	T_4			
4				T_4	T_5		
5					T_5	T_6	
6						T_6	T_1

14.1.3 Inverter output voltage and frequency control techniques

It is a common requirement that the output voltage and/or frequency of an inverter be varied in order to control the load power or, in the case of an induction motor, to control the shaft speed and torque. The six modulation control techniques to be considered are:

- Variable voltage dc link
- Single-pulse width modulation
- Multi-pulse width modulation
- Multi-pulse, selected notching modulation
- Sinusoidal pulse width modulation
- Triplen injection
    - Triplens injected into the modulation waveform
    - Voltage space vector modulation

14.1.3i - Variable voltage dc link

The rms voltage of a square-wave can be changed and controlled by varying the dc link source voltage. A *variable dc link* voltage can be achieved with a dc chopper as considered in chapter 13 or an ac phase-controlled thyristor bridge as considered in sections 11.2 and 11.5. A dc link *L-C* smoothing filter may be necessary.

14.1.3ii - Single-pulse width modulation

Simple pulse-width control can be employed as considered in section 14.1.1b, where a single-phase bridge is used to produce a quasi-square-wave output voltage as shown in figure 14.1c.
An alternative method of producing a quasi-square wave of controllable pulse width is to transformer-add the square-wave outputs from two push-pull bridge inverters as shown in figure 14.12a. By phase-shifting the output by α, a quasi-square sum results as shown in figure 14.12b.

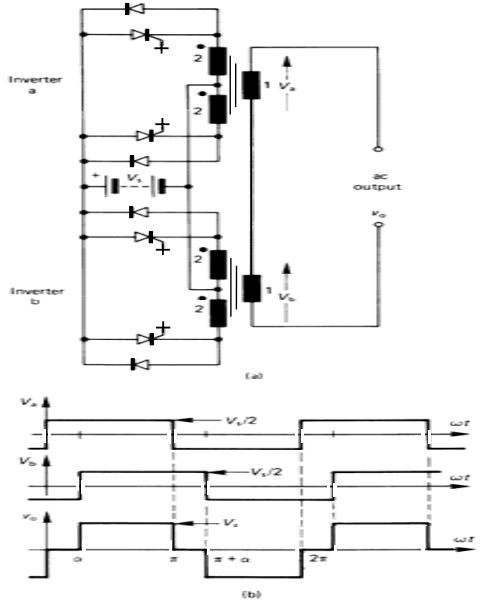

Figure 14.12. *Voltage control by combining phase-shifted push-pull inverters: (a) two inverters with two transformers for summing and (b) circuit voltage waveforms for a phase displacement of α.*

The output voltage can be described by

$$V_o = \sum_{n\ odd}^{\infty} v_{an} \sin n\omega t \qquad \text{(V)} \qquad (14.46)$$

where

$$v_{an} = \frac{2}{\pi}\int_{-½\pi}^{½\pi} V_s \cos n\alpha\, d\alpha = \frac{4}{n\pi} V_s \cos(½n\alpha) \qquad \text{(V)} \qquad (14.47)$$

The rms output voltage is

$$V_r = V_s\sqrt{1 - \alpha/\pi} \qquad \text{(V)} \qquad (14.48)$$

and the rms value of the fundamental is

$$V_1 = \frac{2\sqrt{2}}{\pi} V_s \cos ½\alpha \qquad \text{(V)} \qquad (14.49)$$

As α increases, the magnitude of the harmonics, particularly the third, becomes significant compared with the fundamental magnitude. This type of control may be used in high power applications.

14.1.3iii - Multi-pulse width modulation

An extension of the single-pulse modulation technique is multiple-notching as shown in figure 14.13. The bridge switches are controlled so as to vary the on to off time of each notch, δ, thereby varying the output rms voltage which is given by $V_{rms} = \sqrt{\delta}\, V_s$. Alternatively, the number of notches can be varied.

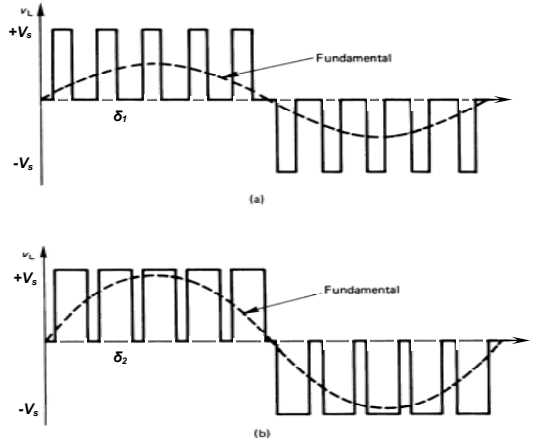

Figure 14.13. *Inverter control giving variable duty cycle of five notches per half cycle: (a) low duty cycle, δ_1, hence low fundamental magnitude and (b) higher duty cycle, δ_2, for a high fundamental voltage output.*

The harmonic content at lower output voltages is significantly lower than that obtained with single-pulse modulation. The increased switching frequency does increase the magnitude of higher harmonics and the switching losses.

14.1.3iv - Multi-pulse, selected notching modulation

Selected elimination of lower-order harmonics can be achieved by producing an output waveform as shown in figure 14.14. The exact switching points are calculated off-line so as to eliminate the required harmonics. For *n* switchings per half cycle, *n* selected harmonics can be eliminated.
In figure 14.14 two notches per half cycle are introduced; hence any two selected harmonics can be eliminated. The more notches, the lower is the output fundamental. For example, with two notches, the third and fifth harmonics are eliminated. From

$$b_n = \frac{4}{\pi}\int_0^{½\pi} f(\theta)\sin n\theta\, d\theta \quad \text{for} \quad n = 1, 2, 3, ... \qquad (14.50)$$

$$b_3 = \frac{4}{3\pi} V_s\left(1 - 2\cos 3\alpha + 2\cos 3\beta\right) = 0$$

and

$$b_5 = \frac{4}{5\pi} V_s\left(1 - 2\cos 5\alpha + 2\cos 5\beta\right) = 0$$

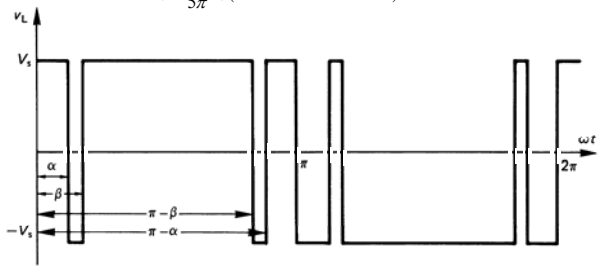

Figure 14.14. *Output voltage harmonic reduction for a single-phase bridge using selected notching.*

Solving yields $\alpha = 23.6°$ and $\beta = 33.3°$. The fundamental rms component of the output voltage waveform is 0.84 of a square wave, which is $(2\sqrt{2}/\pi)V_s$. Ten switching intervals exist compared with two per cycle for a square wave, hence switching losses and control circuit complexity are increased.
In the case of a three-phase inverter bridge, the third harmonic does not exist, hence the fifth and seventh (b_5 and b_7) can be eliminated with $\alpha = 16.3°$ and $\beta = 22.1$. The 5th, 7th, 11th, and 13th can be eliminated with the angles 10.55°, 16.09°, 30.91°, and 32.87° respectively. Because the waveforms have quarter wave symmetry, only angles for 90° need be stored.

The output rms voltage magnitude can be varied by controlling the dc link voltage or by transformer-adding two phase-displaced bridge outputs as demonstrated in figure 14.12. The rms magnitude can be changed by introducing an extra constraint to be satisfied, along with the harmonic eliminating constraints.
The multi pulse selected notching modulation technique can be extended to the *optimal pulse-width modulation method,* where harmonics may not be eliminated, but minimised according to a specific criterion. In this method, the quarter wave output is considered to have a number of switching angles. These angles are selected so as, for example, to eliminate certain harmonics, minimise the rms of the ripple current, or any other desired performance index. The resultant non-linear equations are solved using numerical methods off-line. The computed angles are then stored in a ROM look-up table for use. A set of angles must be computed and stored for each desired level of the voltage fundamental and output frequency.
The optimal pwm approach is particularly useful for high-power, high-voltage GCT thyristor inverters, which tend to be limited in switching frequency by device switching losses.

14.1.3v - Sinusoidal pulse-width modulation (pwm)

1 - Natural sampling

(a) Synchronous carrier
The output voltage waveform and method of generation for synchronous carrier, natural sampling sinusoidal pwm, suitable for the single-phase bridge of figure 14.1, are illustrated in figure 14.11. The switching points are determined by the intersection of the triangular carrier wave f_c and the reference modulation sine wave, f_o. The output frequency is at the sine-wave frequency f_o and the output voltage is proportional to the magnitude of the sine wave. The amplitude M ($0 \leq M \leq 1$) is called the modulation index. For example, figure 14.11a shows maximum voltage output ($M = 1$), while in figure 14.11b where the sine-wave magnitude is halved ($M = 0.5$), the output voltage is halved.
If the frequency of the modulation sinewave, f_o, is an integer multiple of the triangular wave carrier-frequency, f_c that is, $f_c = nf_o$ where n is integer, then the modulation is *synchronous,* as shown in figure 14.11. If n is odd then the positive and negative output half cycles are symmetrical and the output voltage contains no even harmonics. In a three-phase system if n is a multiple of 3 (and odd), the carrier is a triplen of the modulating frequency and the spectrum does not contain the carrier or its harmonics.

$$f_c = (6q + 3) f_o = nf_o \qquad (14.51)$$

for $q = 1, 2, 3$.
Sinusoidal pwm requires a carrier of much higher frequency than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave.

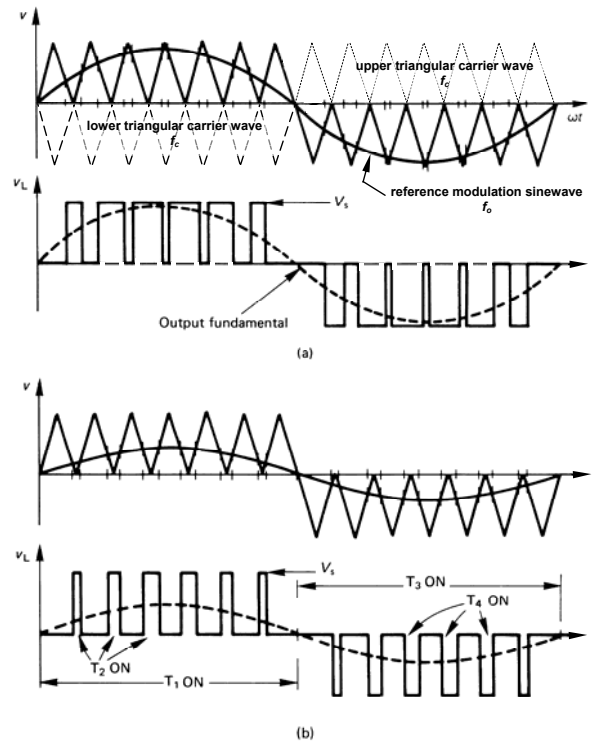

Figure 14.11. *Derivation of trigger signals for multi-level naturally sampled pulse-width modulation waveforms: (a) for a high fundamental output voltage (M = 1) and (b) for a lower output voltage (M = 0.5), with conducting devices shown.*

If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics.
Rather than using a triangular carrier, which has an alternating offset as shown in figure 14.11, a triangular carrier without an offset can be used. Now the output only approximates the ideal. Figure 14.12 shows this pwm generation technique

and voltage output waveform applied to the three-phase inverter in figure 14.7. The offset carrier is not applicable to three-phase pwm generation since complementary switch action is required. That is, one switch in the inverter leg must always be on. It will be noticed that, unlike the output in figure 14.11, no zero voltage output periods exist. This has the effect that, in the case of GCT thyristor bridges, a large number of commutation cycles is required. When zero output periods exist, as in figure 14.11, one GCT thyristor is commutated and the complementary device in that leg is not turned on. The previously commutated device can be turned back on without the need to commutate the complementary device, as would be required with the pwm technique illustrated in figure 14.12. Commutation losses are reduced, control circuitry simplified and the likelihood of simultaneous conduction of two series devices is reduced.

The alternating zero voltage loop concept can be used, where in figure 14.11b, rather than T_1 being on continuously during the first half of the output cycle, T_2 is turned off leaving T_1 on, then when either T_1 or T_2 must be turned off, T_1 is turned off leaving T_2 on.

(b) Asynchronous carrier

When the carrier is not an integer multiple of the modulation waveform, asynchronous modulation results. Because the output frequency, f_o, is usually variable over a wide range, it is difficult to ensure $f_c = nf_o$. To achieve synchronism, the carrier frequency must vary with frequency f_o. Simpler generating systems result if a fixed carrier frequency is used, resulting in asynchronism between f_o and f_c at most output frequencies. Left over, incomplete carrier cycles create slowly varying output voltages, called subharmonics, which may be troublesome with low carrier frequencies, as found in high-power drives. Natural sampling, asynchronous sinusoidal pwm is usually restricted to analogue or ASIC implementation. The harmonic consequences of asynchronous-carrier natural-sampling are similar to asynchronous-carrier regular-sampling in 2 to follow.

2 - Regular sampling

Asynchronous carrier

When a fixed carrier frequency is used, usually no attempt is made to synchronise the modulation frequency. The output waveforms do not have quarter-wave symmetry which produces subharmonics. These subharmonics are insignificant if $f_c >> f_o$, usually, $f_c > 20f_o$.

The implementation of sinusoidal pwm with microprocessors or digital signal processors is common because of flexibility and the elimination of analogue circuitry associated problems. The digital pwm generation process involves scaling, by multiplication, of the per unit sine-wave samples stored in ROM. The multiplication process is time-consuming, hence natural sampling is not possible. In order to minimise the multiplication rate, the sinusoidal sine-wave reference is replaced by a quantised stepped representation of the sine-wave. Figure 14.17 shows two methods used. Sampling is synchronised to the carrier frequency and the multiplication process is performed at three times the sampling rate for three-phase pwm generation (once for each phase).

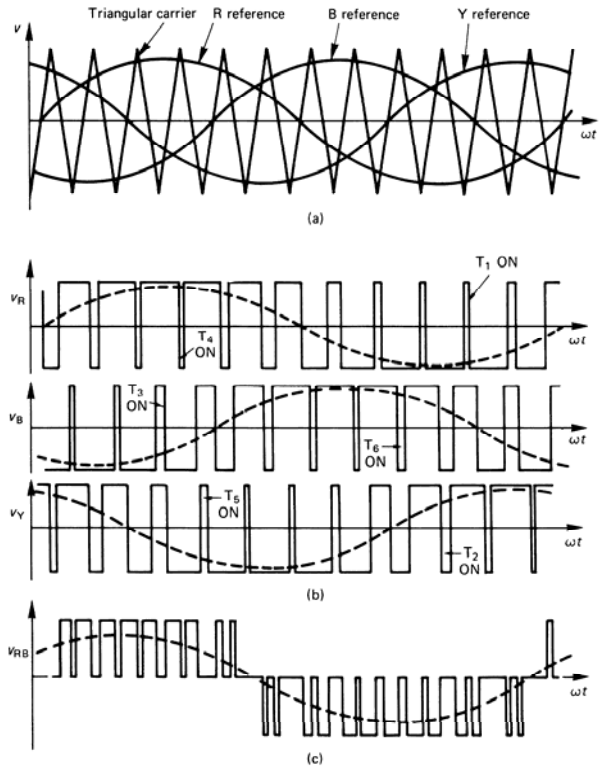

Figure 14.12. *Naturally sampled pulse-width modulation waveforms suitable for a three-phase bridge inverter: (a) reference signals; (b) conducting devices and fundamental sine waves; and (c) one output line-to-line voltage waveform.*

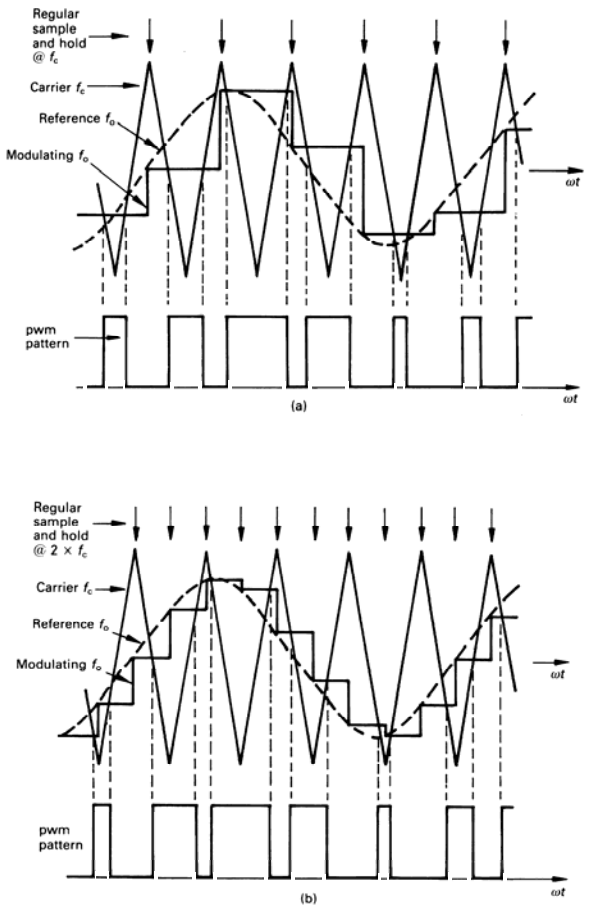

Figure 14.17. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation: (a) symmetrical modulation and (b) asymmetrical modulation.*

Symmetrical modulation

Figure 14.17a illustrates the process of symmetrical modulation, where sampling is at the carrier frequency. The quantised sine-wave is stepped and held at each sample point. The triangular carrier is then compared with the step sine-wave sample. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier with the stepped sine-wave, about the non-sampled carrier peak, are equidistant about the carrier peak. The pulse width, independent of the modulation index *M,* is symmetrical about the triangular carrier peak not associated with sampling, as illustrated by the upper pulse in figure 14.18. The pulse width is given by

$$t_{ps} = \frac{1}{2f_c}\left(1 - M \sin 2\pi f_o t_1\right) \tag{14.52}$$

where t_1 is the time of sampling.

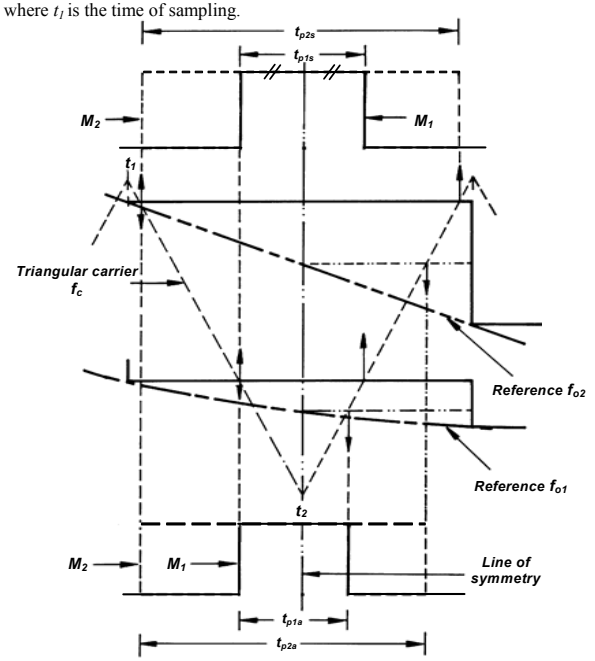

Figure 14.18. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation, showing double edge: (upper) asymmetrical modulation and (lower) symmetrical modulation.*

Asymmetrical modulation

Asymmetrical modulation is produced when the carrier is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency, as shown in figure 14.17b. Each side of the triangular carrier about a sampling point intersects the stepped waveform at different step levels. The resultant pulse width is asymmetrical about the sampling point, as illustrated by the lower pulse in figure 14.18 for two modulation waveform magnitudes. The pulse width is given by

$$t_{pa} = \frac{1}{2f_c}\left(1 - \tfrac{1}{2}M\left(\sin 2\pi f_o t_1 + \sin 2\pi f_o t_2\right)\right) \qquad (14.53)$$

where t_1 and t_2 are the times at sampling such that $t_2 = t_1 + 1/2f_c$.

Figure 14.18 shows that a change in the modulation index M varies the pulse width on each edge, termed *double edge modulation.* A triangular carrier produces double edge modulation, while a sawtooth carrier produces *single edge modulation,* independent of the sampling technique.

3 - Frequency spectra of pwm waveforms

The most common form of sinusoidal modulation for three-phase inverters is regular sampling, asynchronous, fixed frequency carrier, pwm. If $f_c > 20f_o$, low frequency subharmonics can be ignored. The output spectra consists of the modulation frequency f_o with magnitude M. Also present are the spectra components associated with the triangular carrier, f_c. For any sampling, these are f_c and the odd harmonics of f_c. (The triangular carrier f_c contains only odd harmonics). These decrease in magnitude with increasing frequency. About the frequency nf_c are components of f_o spaced at $\pm 2f_o$, which generally decrease in magnitude when further away from nf_c. That is, at f_c the harmonics present are f_c, $f_c \pm 2f_o$, $f_c \pm 4f_o$, ... while about $2f_c$, the harmonics present are $2f_c \pm f_o$, $2f_c \pm 3f_o$,..., but $2f_c$ is not present. The typical output spectrum is shown in figure 14.19. The relative magnitudes of the sidebands vary with modulation depth and the carrier related frequencies present, f_h, are given by

$$f_h = \left(\tfrac{1}{2} + \frac{-1^{n+1}}{2}\right) n f_c \pm \left(2k - \left(\tfrac{1}{2} + \frac{-1^{n}}{2}\right)\right) f_o \qquad (14.54)$$

where $k = 1, 2, 3,....$ (sidebands) and $n = 1, 2, 3,....$ (carrier)

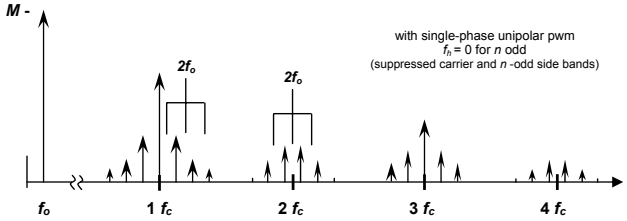

Figure 14.19. *Location of carrier harmonics and modulation frequency sidebands, showing all sideband separated by $2f_m$.*

Although the various pwm techniques produce other less predominate spectra components the main difference is seen in the magnitude of the carrier harmonics and sidebands. The magnitudes increase as the pwm type changes from naturally sampling to regular sampling, then from asymmetrical to symmetrical modulation, and finally from double edge to single edge. With a three-phase inverter, the carrier and its harmonics do not appear in the line-to-line voltages since the carrier is co-phase to the three modulation waveforms.

14.1.3vi - Phase dead-banding

Dead banding is when one phase (leg) is in a fixed on state, and the remaining phases are appropriately modulated so that the phase currents remain sinusoidal. The dead banding occurs for 60° periods of each cycle with the phase with the largest magnitude voltage being permanently turned on. Sequentially each switch is clamped to the appropriate link rail. The leg output is in a high state if it is associated with the largest positive phase voltage magnitude, while the phase output is zero if it is associated with the largest negative phase magnitude. Thus the phase outputs are cycled, being alternately clamped high and low for 60° every 180° as shown in figure 14.20. A consequence of dead banding is reduced switching losses since each leg is not switched at the carrier frequency for 120° (two 60° periods 180° apart). A consequence of dead banding is increased ripple current. Dead banding is achieved with discontinuous modulating reference signals. Dead banding for a continuous 120° per phase leg is also possible but the switching loss savings are not uniformly distributed amongst the six inverter switches.

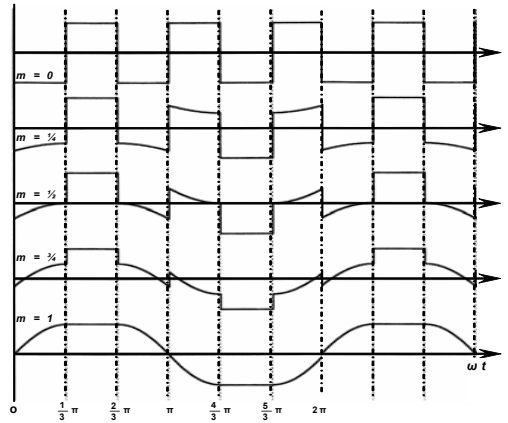

Figure 14.20. *Modulation reference waveform for phase dead banding.*

14.1.3vii - Triplen Injection modulation

The magnitude of the fundamental can be increased from 0.827pu to 0.955pu without introducing output voltage distortion, by the injection of triplen components, which are co-phasal in a three-phase system, and therefore do not appear in the line currents. Two basic approaches can be used to affect this undistorted output voltage magnitude increase.

- Triplen injection into the modulation waveform or
- Voltage space vector modulation

- Triplens injected into the modulation waveform

An inverter reconstitutes three-phase voltages with a maximum magnitude of 0.827 ($3\sqrt{3}/2\pi$) of the fixed three-phase input ac supply. A motor designed for the fixed mains supply is therefore under-fluxed at rated frequency and not fully utilised on an inverter. As will be shown, by adding third harmonic voltage injection, the flux level can be increased to 0.955 ($3/\pi$) of that produced on the three-phase ac mains supply.

If overmodulation ($M > 1$) is not allowed, then the modulation wave $M \sin \omega t$ is restricted in magnitude to $M = 1$, as shown in figure 14.21a.

If $V_{RN} = M \sin\omega t \le 1$pu
and $V_{YN} = M \sin(\omega t + \frac{2}{3}\pi) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M \sin(\omega t - \frac{1}{6}\pi)$
where $0 \le M \le 1$

In a three-phase pwm generator, the fact that harmonics at $3f_o$ (and multiples of $3f_o$) vectorally cancel can be utilised effectively to increase M beyond 1, yet still ensure modulation occurs for every carrier frequency cycle.

Let $V_{RN} = M' \sin\omega t + \frac{1}{6}\sin 3\omega t) \le 1$ pu
and $V_{YN} = M' (\sin(\omega t + \frac{2}{3}\pi) + \frac{1}{6} \sin 3(\omega t + \frac{2}{3}\pi)) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M' \sin(\omega t - \frac{1}{6}\pi)$

V_{RN} has a maximum instantaneous value of 1 pu at $\omega t = \pm\frac{1}{3}\pi$, as shown in figure 14.21b. Therefore

$$V_{RN}\left(\omega t = \tfrac{1}{3}\pi\right) = \frac{\sqrt{3}}{2} M' = 1$$

that is

$$\widehat{M}' = \frac{2}{\sqrt{3}} \widehat{M} = 1.155 \widehat{M} \qquad (14.55)$$

Thus the fundamental of the phase voltage is $M' \sin \omega t = 1.155\, M \sin \omega t$. That is, if the modulation reference $\sin \omega t + \frac{1}{6} \sin 3\omega t$ is used, the fundamental output voltage is 15.5 per cent larger than when $\sin \omega t$ is used as a reference. The increased fundamental is shown in figure 14.21b.

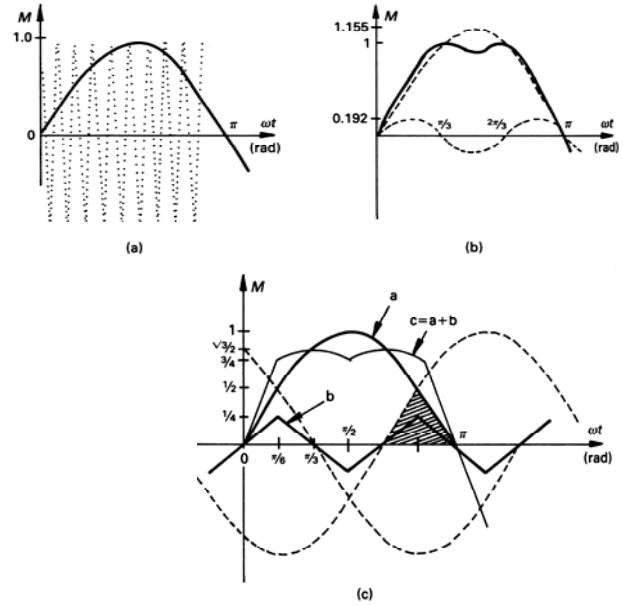

Figure 14.21. *Modulation reference waveforms: (a) sinusoidal reference, sin ωt; (b) third harmonic injection reference, sin ωt + $\frac{1}{6}$sin 3ωt; and (c) triplen injection reference, sin ωt + (1/√3π)(9/8sin3ωt - 80/81sin9ωt + . . .} where the near triangular waveform b is half the magnitude of the shaded area.*

The spatial voltage vector technique injects the triplens according to

$$V_{RN} = M' \left\{ \sin \omega t + \frac{1}{\sqrt{3}\pi} \sum_{r=0}^{\infty} \frac{(-1)^r}{\left[(2r+1) - \frac{1}{3}\right]\left[(2r+1) + \frac{1}{3}\right]} \right\} \sin\left[(2r+1)3\omega t\right] \qquad (14.56)$$

The Fourier triplen series represents half the magnitude of the shaded area in figure 14.21c (the waveform marked 'b'), which is formed by the three-phase voltage waveforms. The spatial voltage vector waveform is defined by

$$\begin{cases} \frac{3}{2} \sin(\omega t) & 0 \le \omega t \le \frac{1}{6}\pi \\ \frac{\sqrt{3}}{2} \sin(\omega t + \frac{1}{6}\pi) & \frac{1}{6}\pi \le \omega t \le \frac{1}{2}\pi \end{cases} \qquad (14.57)$$

The use of this reference increases the duration of the zero volt loops, thereby decreasing inverter output ripple. The maximum modulation index is 1.155. Third harmonic injection, yielding M = 1.155, is a satisfactory approximation to spatial voltage vector.

- *Voltage space vector pwm*

When generating three-phase quasi-square output voltages, the inverter switches step progressively to each of the six switch output possibilities (states). In figure 14.10, when producing the quasi-square output, each of these six states is represented by an output voltage space vector. Each vector has a ⅓π displacement from its two adjacent states, and each has a length V_s which is the pole output voltage relative to the inverter 0V rail. Effectively, the quasi-square three-phase output is generated by a rotating vector of length V_s, jumping successively from one output state to the next in the sequence, and in so doing creating six sectors. The speed of rotation, in particular the time for one rotation, determines the inverter output frequency. The sequence of voltage vectors $\{v_1, v_3, v_2, v_6, v_4, v_5\}$ is arranged such that stepping from one state to the next involves only one of the three poles changing state. Thus the number of inverter devices needing to change states (switch) at each transition, is minimised.
[If the inverter switches are relabelled, upper switches T_1, T_2, T_3 - right to left; and lower switches T_4, T_5, T_6 - right to left: then the rotating voltage sequence becomes $\{v_1, v_2, v_3, v_4, v_5, v_6\}$]
Rather than stepping ⅓π radians per step, from one voltage space vector position to the next, thereby producing a six-step quasi-square fixed magnitude voltage output, the rotating vector is rotated in smaller steps based on the position being updated at a constant rate (carrier frequency). Furthermore, the vector length can be varied, to a magnitude less than V_s.
To incorporate a variable rotating **vector length** (modulation depth), it is necessary to vary the average voltage in each carrier period. Hence pulse width modulation is used in the period between each finite step of the rotating vector. Pulse width modulation requires the introduction of zero voltage output states, namely all the top switches on (state 111, v_7) or all the lower switches on (state 000, v_0). These two extra states are shown in figure 14.22, at the centre of the hexagon. Now the pole-to-pole output voltage can be zero, which allows duty cycle variation to achieve variable average output voltage for each phase, within each carrier period, proportional to the magnitude of the position vector.
To facilitate **vector positions** (angles) that do not lie on one of the six quasi-square output vectors, an intermediate vector $V_{o/p}e^{j\theta}$ is resolved into the vector sum of the two quasi-square vectors adjacent to the rotating vector. This process is shown in figure 14.23 for a voltage vector $V_{o/p}$ that lies in sector I, between output states v_1 (001) and v_3 (011). The voltage vector has been resolved into the two components V_a and V_b as shown.
The time represented by quasi-square vectors v_1 and v_3 is the carrier period T_c, in each case. Therefore the portion of T_c associated with v_a and v_b is scaled proportionally to v_1 and v_3, giving t_a and t_b.

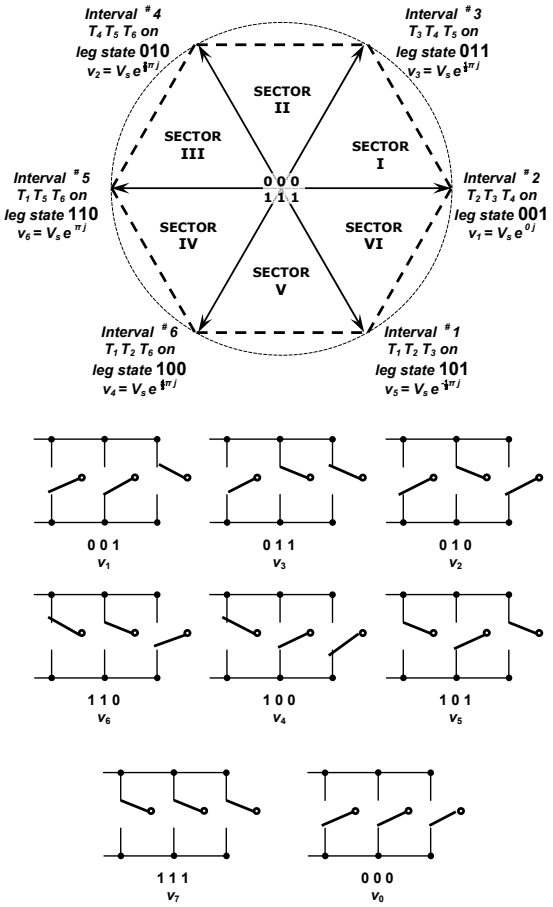

Figure 14.22. *Instantaneous output voltage states for the three legs of an inverter.*

$$\frac{t_a}{T_c} = \frac{|V_a|}{|v_1|} = \frac{\frac{2}{\sqrt{3}} V_{o/p} \sin\left(\frac{1}{3}\pi - \theta\right)}{V_s}$$

$$\frac{t_b}{T_c} = \frac{|V_b|}{|v_3|} = \frac{\frac{2}{\sqrt{3}} V_{o/p} \sin\theta}{V_s} \qquad (14.58)$$

where $|v_1| = |v_3|$

The two sine terms in equation (14.58) generate two sine waves displaced by 120°, identical to that generated with standard carrier based sinusoidal pwm.
The sum of t_a and t_b cannot be greater than the carrier period T_c, thus

$$t_a + t_b \le T_c$$
$$t_a + t_b + t_o = T_c \qquad (14.59)$$

where the slack variable t_o has been included to form an equality. The equality dictates that vector v_1 is used for a period t_a, v_3 is used for a period t_b, and during period t_o, the null vector, v_0 or v_7, at the centre of the hexagon is used, which do not affect the average voltage during the carrier interval T_c.
A further constraint is imposed in the time domain. The rotating voltage vector is a fixed length for all rotating angles, for a given inverter output voltage. Its length is restricted in both time and space. Obviously the resolved component lengths cannot exceed the pole vector length, V_s. Additionally, the two vector magnitudes are each a portion of the carrier period, where t_a and t_b could be both equal to T_c, that is, they both have a maximum length V_s. The anomaly is that voltages v_a and v_b are added vectorially but their durations (times t_a and t_b) are added linearly. The longest time $t_a + t_b$ possible is when t_o is zero, as shown in figures 14.23a and 14.22a, by the hexagon boundary. The shortest vector to the boundary is where both resolving vectors have a length ½V_s, as shown in figure 14.23b. For such a condition, $t_a = t_b = ½T_c$, that is $t_a + t_b = T_c$. Thus for a constant inverter output voltage, when the rotating voltage vector has a constant length, $\hat{V}_{o/p}$, the locus of allowable rotating reference voltage vectors must be within the circle scribed by the maximum length vector shown in figure 14.23b. As shown, this vector has a length $v_1 \cos 30°$, specifically $0.866V_s$. Thus the full quasi-square vectors v_1, v_2, etc., which have a magnitude of $1 \times V_s$, cannot be used for generating a sinusoidal output voltage. The excess length of each quasi-square voltage (which represents time) is accounted for by using zero state voltage vectors for a period corresponding to that extra length (1- cos 30° at maximum output voltage).
Having calculated the necessary periods for the inverter poles (t_a, t_b, and t_o), the carrier period switching pattern can be assigned in two ways.

- Minimised current ripple
- Minimised switching losses, using dead banding

Each approach is shown in figure 14.24, using single edged modulation. The waveforms are based on the equivalent of symmetrical modulation where the pulses are symmetrical about the carrier trough. By minimising the current ripple, seven switching states are used per carrier cycle, while for loss minimisation (dead banding) only five switching states occur, but at the expense of increased ripple

current in the output current. When dead banding, the zero voltage state v_0 is used in even numbered sextants and v_7 is used in odd numbered sextants.
Sideband and harmonic component magnitudes can be decreased if double-edged modulation placement of the states is used, which requires recalculation of t_a, t_b, and t_o at the carrier crest, as well as at the trough.

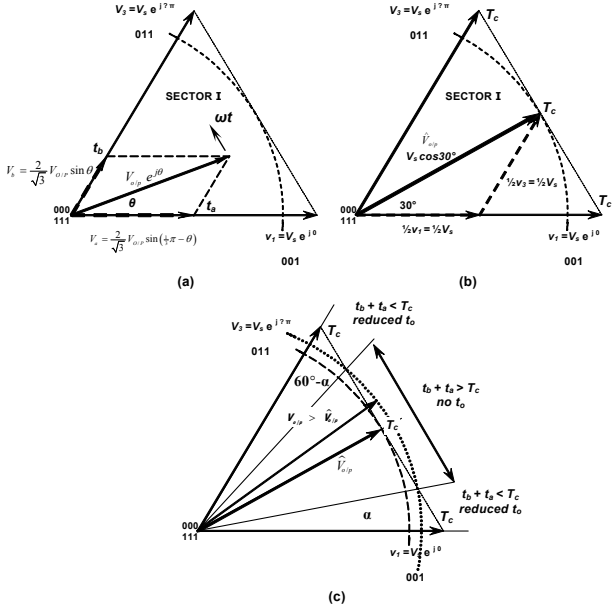

Figure 14.23. *First sector of inverter operational area involving pole outputs 001 and 011: (a) general rotating voltage vector; (b) maximum allowable voltage vector length for undistorted output voltages; and (c) over modulation.*

Over-modulation is when the magnitude of the demanded rotating vector is greater than $\hat{V}_{o/p}$ such that the zero voltage time reduces to zero, $t_o = 0$, during a portion of the time of one rotation of the output vector. Initially this occurs at 30° $\left(\frac{1}{6}\pi\left(2N_{\text{sector}} - 1\right)\right)$ when the output vector length reaches $\hat{V}_{o/p}$, as shown in figure 14.23b. As the demand voltage magnitude increases further, the region around the 30° vector position where t_o ceases to occur, increases as shown in figure 14.23c. When the output rotational vector magnitude increases to V_s, the maximum possible, angle α reduces to zero, and t_o ceases to occur at any rotational angle.

The values of t_a, t_b, and t_o (if greater than zero), are calculated as usual, but pulse times are assigned pro rata to fit within the carrier period T_c.

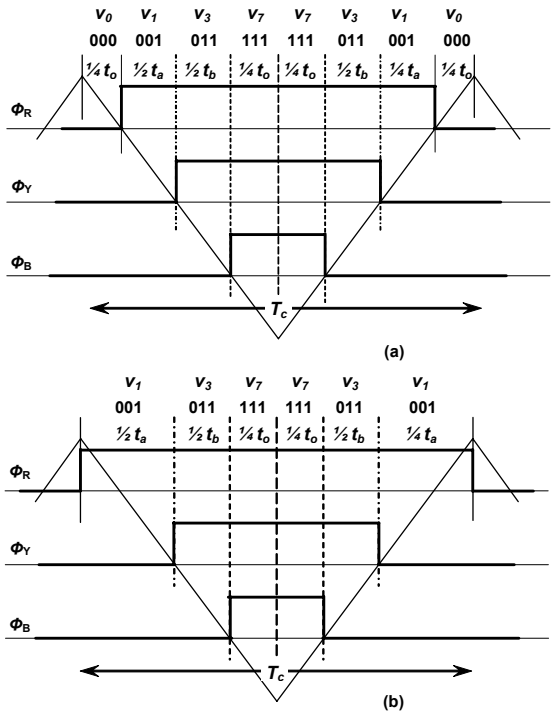

Figure 14.24. *Assignment of pole periods t_a and t_b based on: (a) minimum current ripple and (b) minimum switching transitions per carrier cycle, T_c.*

14.2 dc-to-ac controlled current-sourced inverters

In current-fed inverters (or alternatively current sourced inverter, *CSI*) the dc supply is of high reactance, being inductive so as to maintain the required inverter output bidirectional current independent of the inverter load.

14.2.1 Single-phase current fed inverter

A single-phase, controlled current-sourced bridge is shown in figure 14.25a and its near square-wave output current is shown in figure 14.25b. No freewheel diodes are required and the thyristors required forced commutation and have to withstand reverse voltages. An inverter path must be maintained at all times for the source controlled current.

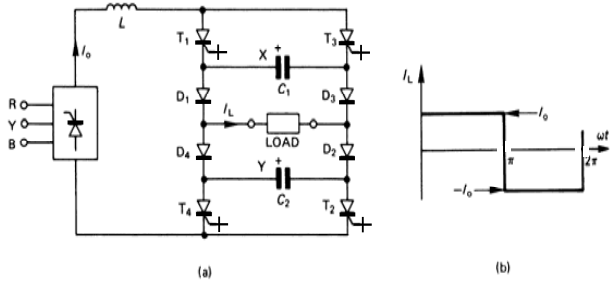

Figure 14.25. *Single-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform.*

Consider thyristors T_1 and T_2 on and conducting the constant load current. The capacitors are charged with plates X and Y positive as a result of the previous commutation cycle.

- ***Phase I***

  Thyristors T_1 and T_2 are commutated by triggering thyristors T_3 and T_4. The capacitors impress negative voltages across the respective thyristors to be commutated off, as shown in figure 14.26a. The load current is displaced from T_1 and T_2 via the path T_3-C_1-D_1, the load and D_2-C_2-T_4. The two capacitors discharge in series with the load, each capacitor reverse biasing the thyristor to be commutated, T_1 and T_2 as well as diodes D_3 to D_4. The capacitors discharge linearly (due to the constant current source).

- ***Phase II***

  When both capacitors are discharged, the load current transfers from D_1 to D_2 and from D_3 to D_4, which connects the capacitors in parallel with the load via diodes D_1 to D_2. The plates X and Y now charge negative, ready for the next commutation cycle, as shown in figure 14.26b. Thyristors T_1 and T_2 are now forward biased and must have attained forward blocking ability before the start of phase 2.

The on-going thyristor automatically commutates the outgoing thyristor. This repeated commutation sequencing is a processed termed *auto-sequential thyristor commutation*. The load voltage is load dependent and usually has controlled voltage spikes during commutation.

Since the GTO and CGT both can be commutated from the gate, the two commutation capacitors C_1 and C_2 are not necessary. Commutation overlap is still essential. Also, if the thyristors have reverse blocking capability, the four diodes D_1 to D_4 are not necessary. IGBTs require series blocking diodes, which increases on-state losses. In practice, the current source inverter is only used in very high-power applications (>1MVA), and the ratings of the self-commutating thyristor devices can be greatly extended if the simple external capacitive commutation circuits shown in figure 14.25 are used to reduce thyristor turn-off stresses.

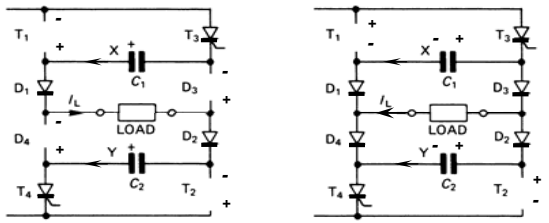

Figure 14.26. *Controlled-current sourced bridge inverter showing commutation of T_1 and T_2 by T_3 and T_4: (a) capacitors C_1 and C_2 discharging and T_1, T_2, D_3, and D_4 reversed biased and (b) C_1, C_2, and the load in parallel with C_1 and C_2 charging.*

14.2.2 Three-phase current fed inverter

A three-phase controlled current-sourced inverter is shown in figure 14.27a. Only two thyristors can be on at any instant, that is, the 120° thyristor conduction principle shown in figure 14.11 is used. A quasi-square line current results, as illustrated in figure 14.27b. There is a 60° phase displacement between commutation of an upper device followed by commutation of a lower device. An upper device (T_1, T_3, T_5) is turned on to commutate another upper device, and a lower device (T_2, T_4, T_6) commutate another lower device. The three upper capacitors are all involved with each upper device commutation, whilst the same constraint applies to the lower capacitors. Thyristor commutation occurs in two distinct phases.

- ***Phase I***

  In figure 14.28a the capacitors C_{13}, C_{35}, C_{51} are charged with the shown polarities as a result of the earlier commutation of T_5. T_1 is commutated by turning on T_3. During commutation, the capacitor between the two commutating switches is in parallel with the two remaining capacitors which

are effectively connected in series. Capacitor C_{13} provides displacement current whilst in parallel, C_{35} and C_{151} in series also provide thyristor T_1 displacement current, thereby reverse biasing T_1.

- ***Phase II***

  When the capacitors have discharged, T_1 becomes forward biased, as shown in figure 14.28b, and must have regained forward blocking capability before the applied positive *dv/dt*. The capacitor voltages reverse as shown in figure 14.28b and when fully charged, diode D_1 ceases to conduct. Independent of this commutation, lower thyristor T_2 is commutated by turning on T_4, 60° later.

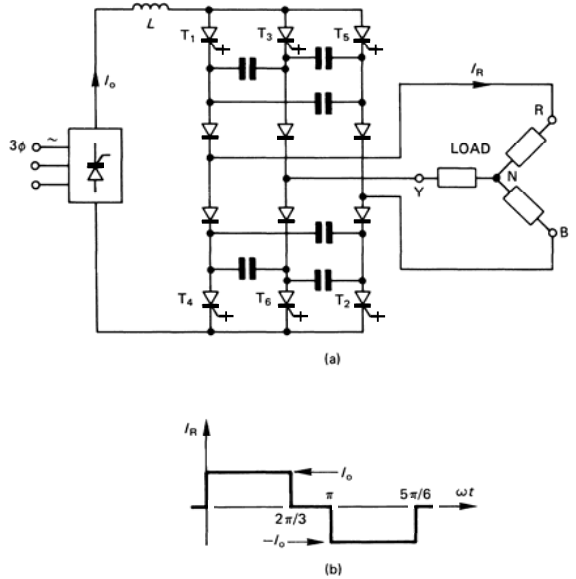

Figure 14.27. *Three-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform for one phase showing 120° conduction.*

As with the single-phase current sourced inverter, assisted capacitor commutation can greatly improve the capabilities of self-commutating thyristors, such as the GTO thyristor and GCT. The output capacitors stiffen the output ac voltage.

A typical application for a three-phase current-sourced inverter would be to feed and control a three-phase induction motor. Varying load requirements are met by changing the source current level over a number of cycles by varying the link inductor input voltage.

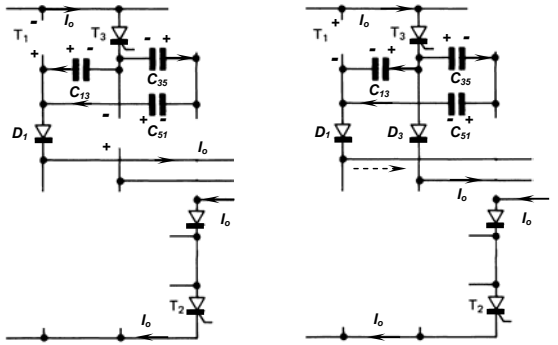

Figure 14.28. *Controlled-current sourced bridge three-phase inverter showing commutation of T_1 and T_3: (a) capacitors C_{13} discharging in parallel with C_{35} and C_{51} discharging in series, with T_1 and D_3 reversed biased (b) C_{13}, C_{35}, and C_{51} charging in series with the load , with T_1 forward biased.*

An important advantage of the controlled current source concept, as opposed to the constant voltage link, is good fault tolerance and protection. An output short circuit or simultaneous conduction in an inverter leg is controlled by the current source. Its time constant is usually longer than that of the input converter, hence converter shut-down can be initiated before the link current can rise to a catastrophic level.

PWM techniques are applicable to current fed inverters in order to reduce current harmonics, thereby reducing load losses and pulsating motor shaft torques. Since current fed inverters are most attractive in very high-power applications, inverter switching is minimised by using optimal pwm. The central 60° portion about the maximums of each phase cannot be modulated, since link current must flow and during such periods both the other phases require the opposite current direction. Attempts to over come such pwm restrictions include using a current sourced inverter with additional parallel current displacement paths as shown in figure 14.29. The auxiliary thyristors, T_{upper} and T_{lower}, and capacitors, C_R, C_Y, and C_B, provide alternative current paths (extra control states) and temporary energy storage. The auxiliary thyristor can be commutated by the extra capacitors.

Characteristics and features of current fed inverters

- The inverter is simple and can utilise rectifier grade thyristors. The switching devices must have reverse blocking capability and experience high voltages (both forward and reverse) during commutation.
- Commutation capability is load current dependent and a minimum load is required. This limits the operating frequency and precludes use in UPS systems. The limited operating frequency can result in torque pulsations.

- The inverter can recover from an output short circuit hence the system is rugged and reliable – fault tolerant.
- The converter-inverter configuration has inherent four quadrant capability without extra power components. Power inversion is achieved by reversing the converter average voltage output with a delay angle of $\alpha > \frac{1}{2}\pi$, as in the three-phase fully controlled converter shown in figure 11.18 (or 14.5.3). In the event of a power supply failure, mechanical braking is necessary. Dynamic braking is possible with voltage fed systems.
- Current fed inverter systems have sluggish performance and stability problems on light loads and at high frequency. On the other hand, voltage fed systems have minimal stability problems and can operate open loop.
- Each machine must have its own controlled rectifier and inverter. The dc link of the voltage fed scheme can be used by many inverters or many machines can utilise one inverter. A dc link offers limited ride-through.
- Current feed inverters tend to be larger in size and weight, because of the link inductor and filtering requirements.

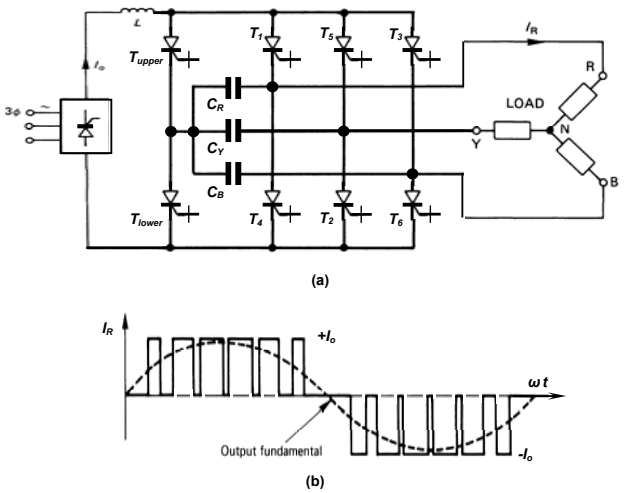

Figure 14.29. *Three-phase controlled-current sourced bridge inverter with alternative commutation current paths: (a) bridge circuit with a current source input and two extra thyristors and (b) load current waveform for one phase showing 180° conduction involving pwm switching.*

14.3 Resonant inverters

The voltage source inverters considered in 14.1 involve inductive loads and the use of switches that are hard switched. That is, the switches experience simultaneous maximum voltage and current during turn-on and turn-off with an inductive load. The current fed inverters considered in 14.2 required capacitive circuits to commutate the bridge switches. When self-commutatable devices are used in current fed inverters, hard switching occurs. In resonant inverters, the load enables commutation of the bridge switches with near zero voltage or current switch conditions, resulting in low switching losses. A characteristic of resonant circuits is that at regular, definable instants

- for a step load voltage, the series *L*-*C*-*R* load current sinusoidally reverses or
- for a step load current, the parallel *L*-*C*-*R* load voltage sinusoidally reverses.

If the load can be resonated, as considered in chapter 6.2.3, then switching stresses can be significantly reduced for a given power through put, provided switching is synchronised to the *V* or *I* zero crossing.

Three types of resonant converters utilise zero voltage or zero current switching.

- load-resonant converters
- resonant-switch dc-to-dc converters
- resonant dc link and forced commutated converters

The single-phase load-resonant converter, which is extensively used in induction heating applications, is presented and analysed in this chapter. Such resonant load converters use an *L*-*C* load which oscillates, thereby providing load zero current or voltage intervals at which the converter switches can be commutated with minimal electrical stress. Resonant switch dc-to-dc converters are presented in chapter 15.9.

Two basic resonant-load single-phase inverters are used, depending on the *L*-*C* load arrangement:

- current fed inverter with a parallel *L*-*C* resonant (tank) load circuit:
  switch turn-off at zero load voltage instants and turn-on with zero voltage
  switch overlap is essential (a continuous source current path is required)
- voltage fed inverter with a series connected *L*-*C* resonant load:
  switch turn-off at zero load current instants and turn-on with zero current
  switch under lap is essential (to avoid dc voltage source short circuiting)

Each load circuit type can be fed from a single ended circuit or H-bridge circuit depending on the load *Q* factor. This classification is divided according to

- symmetrical full bridge for low *Q* load circuits (class D)
- asymmetrical singled ended circuit for a high *Q* load circuit (class E)

High *Q* circuits can also use a full bridge inverter configuration, if desired, for higher through-put power.

In induction heating applications, the resistive part of the resonant load, called the work-piece, is the active load to be heated - melted, where the heating load is usually transformer coupled. Energy transfer control complication is usually associated with the fact that the resistance of the load work-piece changes as it heats up and melts, since resistivity is temperature dependant. However, control is essentially independent of the voltage and current levels and is related to the resonant frequency which is *L* and *C* dependant. Inverter bridge operation is near

the load resonant frequency so that the output waveform is essentially sinusoidal. By ensuring operation is below the resonant frequency, such that the load is capacitive, the resultant leading current can be used to self commutate thyristor converters which may be used in high power series resonant circuits. This same capacitive load commutation effect is obtained for parallel resonant circuits with thyristor current fed inverters operating just above resonance. The output power is controlled by controlling the converter output frequency.

14.3.1 L-C resonant circuits

L-*C*-*R* resonant circuits, whether parallel or series connected are characterised by the load impedance being capacitive at low frequency and inductive at high frequency for the series circuit, and visa versa for the parallel case. The transition frequency between being capacitive and inductive is the resonant frequency, ω_o, at which frequency the *L*-*C*-*R* load circuit appears purely resistive and maximum power is transferred to the load, *R*. *L*-*C*-*R* circuits are classified according to circuit quality factor Q_s resonant frequency, ω_o, and bandwidth, ***BW***, for both parallel and series circuits. The characteristics for the parallel and series resonant circuits are related since every practical series *L*-*C*-*R* circuit has a parallel equivalent, and visa versa.

As shown in figure 14.30 each resonant half cycle is characterised by

- the series resonant circuit current is zero at maximum capacitor stored energy
- the parallel resonant circuit voltage is zero at maximum inductor stored energy

The capacitor in a series resonant circuit must have an external path through which to release its stored energy. The parallel resonant circuit can release its stored inductive energy within its parallel circuit, without an external circuit. The stored energy can transfer back and forth between the *L* and *C*, gradually dissipating in the circuit *R*.

14.3.1i - Series resonant *L*-*C*-*R* circuit

The series *L*-*C*-*R* circuit current for a step input voltage V_s, with initial capacitor voltage v_o and series inductor current i_o is given by

$$i(\omega t) = \frac{V_s - v_o}{\omega L} \times e^{-\alpha t} \times \sin \omega t + i_o \times e^{-\alpha t} \times \frac{\omega_o}{\omega} \times \cos(\omega t + \phi) \qquad (14.60)$$

where

$$\omega^2 = \omega_o^2 (1 - \xi^2) \qquad \omega_o = \frac{1}{\sqrt{LC}} \qquad \alpha = \frac{R}{2L} \qquad \frac{1}{2Q_s} = \xi = \frac{R}{2\omega_o L}$$

ξ is the damping factor. The capacitor voltage is important because it specifies the energy retained in the *L*-*C*-*R* circuit at the end of each half cycle.

$$v_c(\omega t) = V_s - (V_s - v_o)\frac{\omega_o}{\omega} e^{-\alpha t} \cos(\omega t - \phi) + \frac{i_o}{\omega C} e^{-\alpha t} \sin \omega t \qquad (14.61)$$

where

$$\tan \phi = \frac{\alpha}{\omega} \quad \text{and} \quad \omega_o^2 = \omega^2 + \alpha^2$$

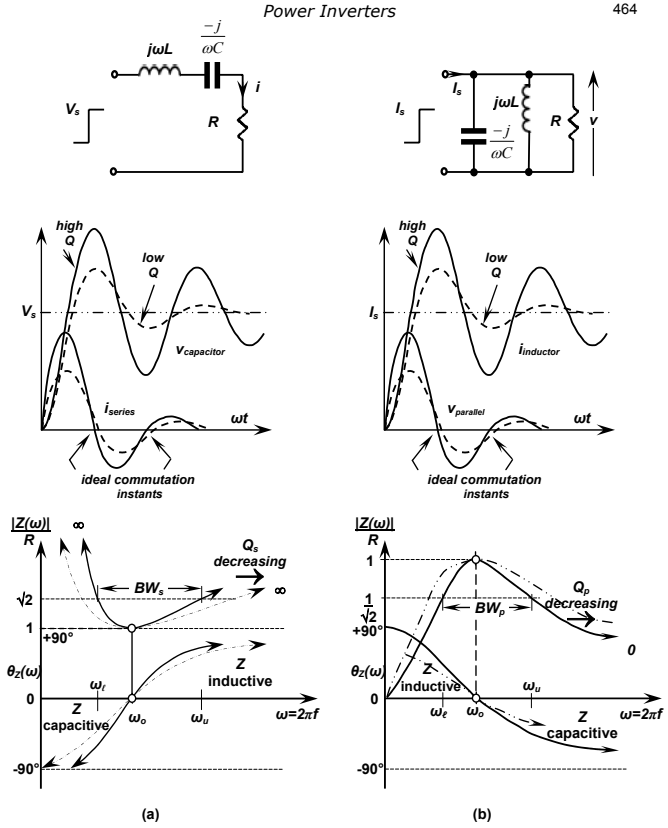

Figure 14.30. *Resonant circuits, step response, and frequency characteristics: (a) series L-C-R circuit and (b) parallel L-C-R circuit.*

At the series circuit resonance frequency ω_o, the lowest possible circuit impedance results, Z=R, hence it can be termed, low-impedance resonance. The series circuit quality factor or figure of merit, Q_s is defined by

$$Q_s = \frac{\text{reactive power}}{\text{average power}} = \frac{2\pi \times \text{maximum stored energy}}{\text{energy dissipated per cycle}} = \frac{2\pi \tfrac{1}{2} L i^2}{\tfrac{1}{2} R i^2 / f_o} = \frac{\omega_o L}{R} = \frac{1}{2\xi} = \frac{Z_o}{R} \tag{14.62}$$

where

$$Z_o = \sqrt{\frac{L}{C}} \qquad (\Omega)$$

The half-power bandwidth BW_s is given by

$$BW_s = \frac{\omega_o}{Q_s} = \frac{2\pi f_o}{Q_s} \tag{14.63}$$

and upper and lower half-power frequencies are related by $\omega = \sqrt{\omega_\ell \omega_u}$.

$$\omega_\ell^u = \omega_o \pm \alpha$$
$$f_\ell^u = f_o \pm \frac{R}{4\pi L} \tag{14.64}$$

Figure 14.30a shows the time-domain step-response of the series *L-C-R* circuit for a high Q load and a low Q case. In the low Q case, to maintain and transfer sufficient energy to the load R, the circuit requires re-enforcement every half sine cycle, while with a high circuit Q, re-enforcement is only necessary once per sinusoidal cycle. Thus for a high circuit Q, full bridge excitation is not necessary, yielding a simpler power circuit as shown in figure 14.31a and b.
The energy transferred to the load resistance R, per half cycle $1/2f_r$, is

$$W_{\frac{1}{2}} = \int_0^{\pi} i(\omega t)^2 R \, d\omega t \tag{14.65}$$

The active power transferred to the load depends on the repetition rate of the excitation, f_r.

$$P = W_{\frac{1}{2}} \times f_r \qquad (\text{W}) \tag{14.66}$$

14.3.1ii - Parallel resonant *L-C-R* circuit

The load for the parallel case is a parallel *L-C* circuit, where the active load is represented by resistance in the inductive path. For analysis, the series *L-R* circuit is converted into its parallel *R-L* equivalent circuit, thus forming the equivalent parallel *L-C-R* circuit shown in figure 14.30b. A parallel resonant circuit is used in conjunction with a current source inverter, thus the parallel circuit is excited with a step input current. The voltage across a parallel *L-C-R* circuit for a step input current I_s, with initial capacitor voltage v_o and initial inductor current i_o is given by

$$v(\omega t) = v_c(\omega t) = \frac{I_s - i_o}{\omega C} \times e^{-\alpha t} \times \sin \omega t + v_{co} \times e^{-\alpha t} \times \frac{\omega_o}{\omega} \times \cos(\omega t + \phi) \tag{14.67}$$

The inductor current is important since it specifies the tank circuit stored energy at the end of each half cycle.

$$i_L(\omega t) = I_s - (I_s - i_o) \times \frac{\omega_o}{\omega} \times e^{-\alpha t} \times \cos(\omega t - \phi) + \frac{v_o}{\omega L} \times e^{-\alpha t} \times \sin \omega t \tag{14.68}$$

where

$$\alpha = \frac{1}{2CR}$$

The circuit Q for a parallel resonant circuit is

$$Q_p = \omega_o RC = \frac{R}{\omega_o L} = \frac{R}{Z_o} = \frac{1}{Q_s} \qquad (14.69)$$

where Z_o and ω_o are defined as in equations (14.60) and (14.62), except L, C, and R refer to the parallel circuit values.

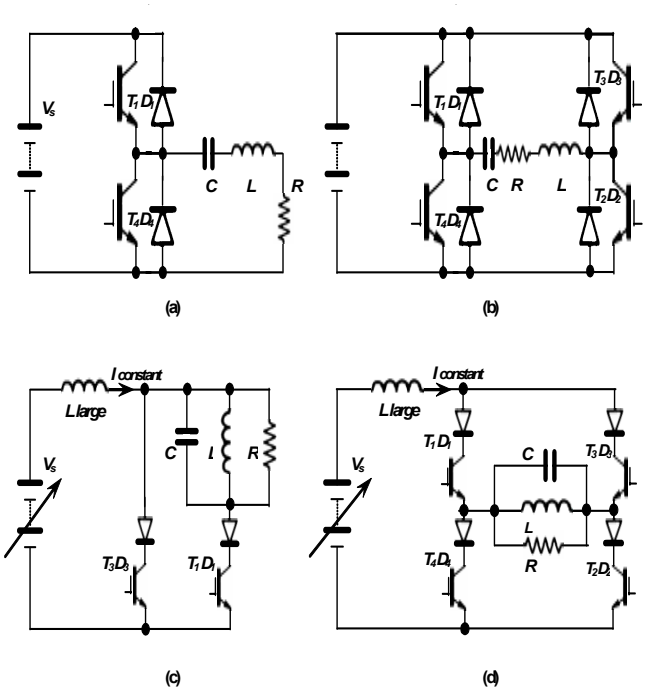

Figure 14.31. *Resonant converter circuits: (a) series L-C-R with a high Q; (b) low Q series L-C-R; (c) parallel L-C-R and high Q; and (b) low Q parallel L-C-R circuit.*

The half-power bandwidth BW_p is given by

$$BW_p = \frac{\omega_o}{Q_p} = \frac{2\pi f_o}{Q_p} \qquad (14.70)$$

and upper and lower half power frequencies are related by $\omega = \sqrt{\omega_l \omega_u}$.
At the parallel circuit resonance frequency ω_o, the highest possible circuit impedance results, $Z=R$, hence it can be termed, high-impedance resonance.
The energy transferred to the load resistance R, per half cycle $1/2f_r$, is

$$W_{½} = \int_0^{\pi} v(\omega t)^2 / R \, d\omega t \qquad (14.71)$$

The active power to the load depends on the repetition rate of the excitation, f_r.

$$P = W_{½} \times f_r \qquad \text{(W)} \qquad (14.72)$$

14.3.2 Series resonant inverters

Series resonant circuits use a voltage source inverter as considered in 14.1.1 and shown in figure 14.31a and b. If the load Q is high, then the resonance of energy from the energy source, V_s, need only be re-enforced every second half-cycle, thereby simplifying converter and control requirements. A high Q circuit is characterised by successive half-cycle capacitor voltage peak magnitudes being of similar magnitude, that is the decay rate is

$$\frac{v_{c_n}}{v_{c_{n+1}}} = e^{\frac{\pi}{2Q}} \approx 1 \quad \text{for } Q \gg 1 \qquad (14.73)$$

Thus there is sufficient energy stored in C to be transferred to the load R, without need to involve the supply V_s. The circuit is simpler and control is easier.
Also, for any Q, each converter can be used with or without the shown freewheel diodes. Without freewheel diodes, the switches have to block high reverse voltages due to the energy stored by the capacitor. MOSFET and IGBTs require series diodes to achieve the reverse voltage blocking requirements. In high power resonant applications, the reverse blocking abilities of the GTO and GCT make it an ideal converter switch. Better load resonant control is obtained if freewheel diodes are not used.

14.3.2i - Series resonant inverter – single inverter leg

Operation of the series load asymmetrical circuit in figure 14.31a depends on the timing of the switches.

1 - Lagging operation (advancing the switch turn-off angle)

If the converter is operated at a frequency above resonance (effected by commutating the switches before the end of an oscillation cycle), the inductor reactance dominates and the load appears inductive. The load current lags the voltage as shown in figure 14.32. This figure shows the conducting devices and that a switch is turned on when its parallel diode is conducting. Turn-on therefore occurs at a low voltage, while turn-off is as with a hard switched inductive load.
Operation and switch timing is as follows:

Switch T1 is turned on while its anti-parallel diode is conducting and the current in the diode reaches zero and the current transfers to, and begins to oscillate through the switch T1. The capacitor charges to a maximum voltage and before

the current reverses, the switch T1 is turned off. The current is diverted through diode D4. T4 is turned on which allows the oscillation to reverse. Before the current in T4 reaches zero, it is turned off and current is diverted to diode D1, which returns energy to the supply. The resonant cycle is repeated when T1 is turned on before the current in diode D1 reaches zero and the process continues.

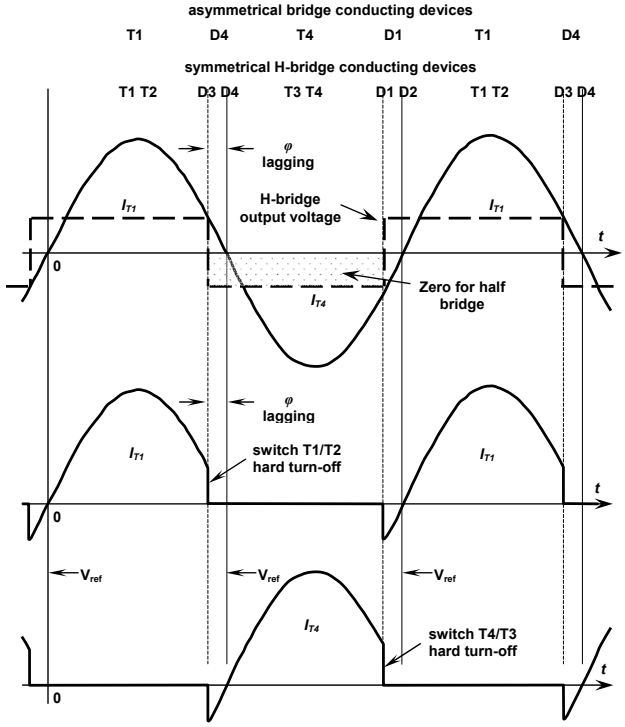

Figure 14.32. *Series L-C-R high Q resonance using the converter circuit in figure 14.31a and b, with a lagging power factor φ.*

2 - Leading operation (delaying the switch turn-on angle)

By operating the converter at a frequency below resonance (effectively by delaying switch turn-on until after the end of an oscillation cycle), the capacitor reactance

dominates and the load appears capacitive. The load current leads the voltage as shown in figure 14.33. This figure shows the conducting devices and that a switch is turned off when its parallel diode is conducting. Turn-off therefore occurs at a low current, while turn-on is as with a hard switched inductive load. Fast recovery diodes are therefore essential.

Operation and switch timing is as follows:

Diode D4 is conducting when switch T1 is turned on, which provides a step input voltage V_s to the series *L-C-R* load circuit, and the current continues to oscillate. The capacitor charges to a maximum voltage and the current reverses through D1, feeding energy back into the supply. T1 is then turned off with zero current.

The switch T4 is turned on, commutating D1, and the current oscillates through the zero volt loop created through T4 and the load. The oscillation current reverses through diode D4, when T4 is turned off with zero current.

T1 is turned on and the process continues.

Without the freewheel diodes the half oscillation cycles are controlled completely by the switches. On the other hand, with freewheel diodes, the timing of switch turn-on and turn-off is determined by the load current zeros, if maximum energy transfer to the load is to be gained.

The series circuit steady-state current at resonance for the asymmetrical bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.60) $i_o = 0$:

$$i(\omega t) = \frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \tag{14.74}$$

which is valid for the + V_s loop (through T1) and zero voltage loop (through T4) modes of cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle.

In steady-state the successive capacitor voltage maxima are

$$\hat{V}_c = V_s \frac{1}{1-e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{V}_c = -V_s \frac{e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} \tag{14.75}$$

The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} \times V_s = V_s \times \coth(\alpha\pi/2\omega) \approx \frac{2\omega}{\alpha\pi} \times V_s \tag{14.76}$$

The energy transferred to the load *R*, per half sine cycle (per current pulse) is

$$W = \int_0^{\pi/\omega} i^2 R dt = \int_0^{\pi/\omega} \left(\frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \right)^2 R\, dt \tag{14.77}$$
$$= \tfrac{1}{2} C V_s^2 \coth\left(\alpha\pi/2\omega\right)$$

14.3.2ii - Series resonant inverter – H-bridge inverter

When the load Q is not high, the capacitor voltage between successive absolute peaks decays significantly, leaving insufficient energy to maintain high efficiency energy transfer to the load *R*. In such cases the resonant circuit is re-enforced with energy from the dc source V_s every half-resonant cycle, by using a full H-bridge as shown in figure 14.31b.

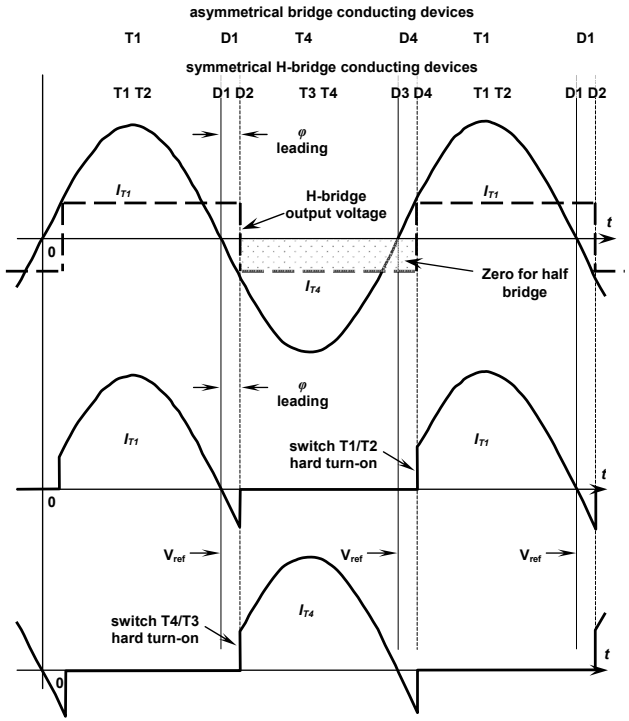

Figure 14.33. *Series L-C-R high Q resonance using the converter circuit in figure 14.31a and b, with a leading power factor φ.*

Operation is characterised by turning on switches T1 and T2 to provide energy from the source during one half of the cycle, then having turned T1 and T2 off, T3 and T4 are turned on for the second resonant half cycle. Energy is again drawn from the supply V_s, and when the current reaches zero, T3 and T4 are turned off.
Without bridge freewheel diodes, the switches support high reverse bias voltages, but the switches control the start of each oscillation half cycle. With freewheel diodes the oscillations can continue independent of the switch states. The diodes return energy to the load, hence reducing the energy transferred to the load. Correct timing of the switches minimises currents in the freewheel diodes, hence minimises the energy needlessly being returned to the supply. Energy to the load

is maximised. As with the asymmetrical bridge, the switches can be used to control the effective load power factor. By advancing turn-off to before the switch current reaches zero, the load can be made to appear inductive, while delaying switch turn-on produces a capacitive load effect. The timing sequencing of the conducting devices, for load power factor control, are shown in figures 14.32 and 14.33.
The series circuit steady-state current at resonance for the symmetrical H-bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.60) $i_o = 0$:

$$i(\omega t) = \frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \tag{14.78}$$

which is valid for the $\pm V_s$ voltage loops of cycle operation at resonance, provided the time reference is moved to the beginning of each half-cycle.
In steady-state the capacitor voltage maxima are

$$\hat{V}_c = V_s \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} = V_s \times \coth(\alpha\pi/2\omega) = -\check{V}_c \tag{14.79}$$

The peak-to-peak capacitor voltage is therefore

$$V_{c_{p-p}} = 2 \times \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} V_s = 2V_s \coth(\alpha\pi/2\omega) \approx \frac{4\omega}{\alpha\pi} \times V_s \tag{14.80}$$

The energy transferred to the load R, per half sine cycle (per current pulse) is

$$\begin{aligned} W &= \int_0^{\pi/\omega} i^2 R\, dt = \int_0^{\pi/\omega} \left(\frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin \omega t \right)^2 R\, dt \\ &= 2CV_s^2 \coth\left(\alpha\pi \big/ 2\omega\right) \end{aligned} \tag{14.81}$$

Notice the voltage swing is twice that with the asymmetrical bridge, hence importantly, the power delivered to the load is increased by a factor of four.
From the series ac circuit, the voltage across the resistor, v_R, at a given frequency, ω, is given by

$$v_R(\omega) = V_i \frac{R}{R + j\left(\omega L - \frac{1}{\omega C}\right)} \tag{14.82}$$

The magnitude of the resistor voltage is therefore

$$\begin{aligned} v_R(\omega) &= V_i \frac{R}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} = V_i \frac{1}{\sqrt{1 + \left(\frac{\omega L}{R} - \frac{1}{\omega RC}\right)^2}} \\ &= V_i \frac{1}{\sqrt{1 + Q^2\left(\frac{\omega}{\omega_o} - \frac{\omega_o}{\omega}\right)^2}} \end{aligned} \tag{14.83}$$

If the input voltage V_i is expressed as a Fourier series then the resistor current can be derived in terms of the summation of all the harmonic component according to

$$\sum_{n=1}^{\infty} i_R(n\omega) = \sum_{n=1}^{\infty} v_R(n\omega) / R \tag{14.84}$$

For a square wave input voltage, V_s, of frequency $\omega \approx \omega_o$, the input voltage fundament of magnitude $4V_s/\pi$ produces the dominant load current component, since higher frequency components are attenuated by second order *L*-*C* filtering action.

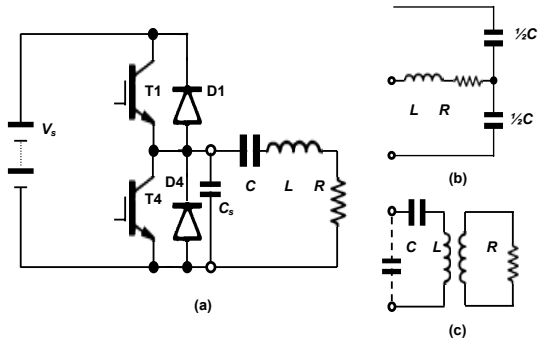

Figure 14.34. *Different resonant load arrangements: (a) switch turn-off snubber capacitor C_s; (b) split capacitor; and (c) series coupled circuit for induction heating.*

14.3.2iii - Circuit variations

Figure 14.34a shows an asymmetrical bridge with a turn-off snubber C_s, where $C_s << C$, hence resonant circuit properties are not affected. The capacitive turn-off snubber is only effective if switch turn-off is advanced such that switch hard turn-off would normally result, that is, the resonant circuit appears capacitive. The snubber acts on both switches since small signal wise (short dc sources), switches T1 and T4 are in parallel.
Figure 14.34b shows a series resonant load used with split resonant capacitance. Resonance re-enforcement occurs every half cycle as with the full H-bridge topology, but only two switches are used.
Figure 14.35c shows a transformer-coupled series circuit which equally could be a parallel circuit with *C* in parallel with the coupled circuit, as shown. Under light loads, the transformer magnetising current influences operation.

14.3.3 Parallel resonant inverters

Parallel resonant circuits use a current source inverter as considered in 14.2.1 and shown in figure 14.31c and d. If the load *Q* is high, then resonance need only be re-enforced every second half-cycle, thereby simplifying converter and control requirements. A common feature of parallel resonant circuits fed from a current

source, is that commutation of the switches involves overlap where the output of the current source is briefly shorted.

14.3.3i - Parallel resonant inverter – single inverter leg

Figure 14.31c shows an asymmetrical converter for high *Q* parallel load circuits. Energy is provided from the constant current source every second half cycle by turning on switch T1. When T1 is turned on (and T3 is then turned off) the voltage across the *L*-*C*-*R* circuit resonates from zero to a maximum and back to zero volts. The energy in the inductor reaches a maximum at each zero voltage instant. T3 is turned on (at zero volts) to divert current from T1, which is then turned off with zero terminal voltage. The energy in the load inductor resonates within the load circuit, with the load in an open circuit state, since T1 is off. The sequence continues when the load voltage resonates back to zero as shown in figure 14.30b.
The parallel circuit steady-state voltage at resonance for the asymmetrical bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.67) $v_o = 0$:

$$v(\omega t) = \frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \tag{14.85}$$

which is valid for both the $+I_s$ loop and open circuit load modes of cycle operation, provided the time reference is moved to the beginning of each half-cycle.
In steady-state the successive inductor current maxima are

$$\hat{I}_L = I_s \frac{1}{1-e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{I}_L = I_s \frac{-e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} \tag{14.86}$$

The energy transferred to the load *R*, per half sine cycle (per voltage pulse) is

$$W = \int_0^{\pi/\omega} v^2/R \; dt = \int_0^{\pi/\omega} \left(\frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \right)^2 / R \, dt \tag{14.87}$$
$$= \tfrac{1}{2} L I_s^2 \coth\left(\frac{\alpha\pi}{2\omega}\right)$$

14.3.3ii - Parallel resonant inverter – H-bridge inverter

If the load *Q* is low, or maximum energy transfer to the load is required, the full bridge converter shown in figure 14.30d is used.
Operation involves T1 and T2 directing the constant source current to the load and when the load voltage falls to zero, T3 and T4 are turned on (and T1 and T2 then turned off). Overlapping the switching sequence ensures a path always exists for the current source. At the next half sinusoidal cycle voltage zero, T1 and T2 are turned on and then T3 and T4 are turned off.
The parallel circuit steady-state voltage for the symmetrical H-bridge can be approximated by assuming $\omega_o \approx \omega$, such that in equation (14.67) $v_o = 0$:

$$v(\omega t) = \frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin \omega t \qquad 0 \le \omega t \le \pi \tag{14.88}$$

which is valid for both the + I_s loops of cycle operation, provided the time reference is moved to the beginning of each half-cycle.
In steady-state the successive inductor current maxima are

$$\hat{I}_L = I_s \frac{1+e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}} = I_s \times \coth\left(\alpha\pi/2\omega\right) = -\check{I}_L \qquad (14.89)$$

The energy transferred to the load R, per half sine cycle (per voltage pulse) is

$$W = \int_0^{\pi/\omega} v^2/R \; dt = \int_0^{\pi/\omega} \left(\frac{2}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{I_s}{\omega C} \times e^{-\alpha t} \times \sin\omega t \right)^2 / R \, dt$$

$$= 2LI_s^2 \coth\left(\frac{\alpha\pi}{2\omega}\right)$$

As with a series resonant circuit, the full bridge delivers four times more power to the load than the asymmetrical bridge circuit. Similarly, the load power and power factor can be controlled by operating above or below the resonant frequency, by delaying or advancing the appropriate switching instances.

Example 14.4: ***Half-bridge with a series L-C-R load***

An asymmetrical half-bridge inverter as shown in the figure 14.31a, with the dc rail *L-C* decoupling shown in figure 14.36, supplies a 1 ohm resistance load with series inductance 100 μH from a 340 V dc source. If the bridge is to operating at 10kHz, determine:

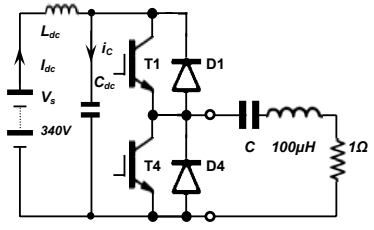

Figure 14.36. *Asymmetrical-bridge series-resonance circuit.*

i. the necessary series C for resonance at 10kHz and the resultant Q
ii. the peak load current, its steady-state time domain solution, and peak capacitor voltages
iii. the bridge rms voltage and fundamental voltage across the *L-C-R* load
iv. the power delivered to the load and the frequency when half power is delivered to the load. What is the switching advance/delay time?
v. the peak blocking voltage of each semiconductor type (and for the case when the freewheel diodes are not employed)
vi. the average, rms, and peak current in the switches and diodes
vii. the resonant capacitor specification

viii. the dc supply current and the dc link capacitor rms current
ix. summarise conditions if the load is supplied from an H-bridge and also calculate the load power supplied at the third harmonic frequency, 3ω.

Solution

i. From $\omega_o = 2\pi f_o = 1/\sqrt{LC}$ the necessary capacitance for resonance at 10kHz and 100μH is

$$C = \frac{1}{\left(2\times\pi\times 10kHz\right)^2 \times 100\mu H} = 2.5\mu F$$

The circuit quality factor Q is given by

$$Q = \frac{Z_o}{R} = \sqrt{\frac{L}{C}} / R = \sqrt{\frac{100\mu H}{2.5\mu F}} / 1\Omega = 6.3$$

Therefore

$\alpha = 5\times10^3$ Ω/H ω = 62.6 krad/s (9.968 kHz)
ξ = 0.079 BW_s = 9.97 krad/s (1.587kHz)
Z_o = 6.3 Ω

ii. The steady-state current is given by equation (14.74)

$$i(\omega t) = \frac{1}{1-e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin\omega t$$

$$= 245.5 \times e^{-5000t} \times \sin\left(2\pi 10\text{kHz} \times t\right)$$

Since the Q is high, a reasonably accurate estimate of the peak current results if the current expression is evaluated at sin(½π), that is t =25μs, which yields $\hat{i}$ = 216.7A.
The rms load current is 216.7A/√2 = 153.2A rms
From equation (14.75) the maximum capacitor voltages are

$$\hat{V}_c = V_s \frac{1}{1-e^{-\alpha\pi/\omega}} \quad \text{and} \quad \check{V}_c = V_s \frac{-e^{-\alpha\pi/\omega}}{1-e^{-\alpha\pi/\omega}}$$

$$= \frac{340\text{V}}{1-e^{-0.25}} \qquad = -\frac{340\text{V}e^{-0.25}}{1-e^{-0.25}}$$

$$= 1537\text{V} \qquad = -1197\text{V}$$

iii. The bridge output voltage is a square wave of magnitude 340V and 0V, with a 50% duty cycle. The rms output voltage is therefore 340/√2=240.4V.
Since the load is at resonance, the current is in phase with the fundamental of the bridge output voltage. The fundament voltage magnitude is given by

$$b_1 = \frac{1}{\pi}\int_0^{\pi} V_s \sin 1\omega t = \frac{2V_s}{\pi} = 216.5\text{V peak}$$

$$\equiv \frac{\sqrt{2}V_s}{\pi} = 153\text{V rms}$$

The rms load current results because of the fundamental voltage, that is, the peak sine current is 216.5V/1Ω = 216.5A peak or 153V/1Ω = 153A rms. This agrees with the current values calculated in part b.

iv. The power delivered to the load is given by

$$P = i_{rms}^2 R = i_{b1}^2 R$$
$$= 153\text{A}^2 \times 1\Omega = 23.41\text{kW}$$

Substitution into equation (14.77) gives 23.15kW at a pulse rate of 2×10kHz. Alternately

$$P = V_s \times \bar{I} = V_s \times 0.45 \times I_{rms}$$
$$= 340\text{V} \times 0.45 \times 153\text{A} = 23.42\text{kW}$$

The half-power frequencies are when the reactive voltage equals the resistive voltage.

$$f_t^u = f_o \pm \frac{R}{4\pi L}$$
$$= 10\text{kHz} \pm 796\text{Hz}$$

Thus at 9204 Hz and 10796 Hz the voltage across the resistive part of the load is reduced to $1/\sqrt{2}$ of the inverter output voltage. The power (proportional to voltage squared) is therefore halved at the half-power frequencies.

Operating above resonance, $f > f_o$ produces an inductive load and this is achieved by turning T1 and T4 off prematurely. Zero current turn-on occurs, but hard switching results at turn-off. To operate at the 10796Hz (92.6μs) upper half-power frequency the period has to be reduced from 100μs (10kHz) to 92.6μs. The period of each half cycle has to be reduced by ½×(100μs - 92.6μs) = 3.7μs

Operating below resonance, $f < f_o$ produces a capacitive load and this is achieved by turning T1 and T4 on late. Zero current turn-off occurs, but hard switching results at turn-on. By delaying turn-on of each switch by ½×(109μs - 100μs), 4.5μs, the effective oscillation frequency will be decreased to the lower half-power frequency, 9204Hz.

v. The bridge diodes, which do not conduct at resonance, clamp switch and diode maximum supporting voltages to the rail voltage, 340V dc.

Note that if clamping diodes were not employed the device maximum off-state voltages would occur during switch change over, when one switch has just been turned off, and just before the on-going switch is turned on. The load current is zero, so the load terminal voltage is the capacitor voltage.

Switch T1 would need to support
- a forward voltage of V_s - $\check{v}$ = 340V + 1197V =1537V = $\hat{v}$ and
- a reverse voltage of $\hat{v}$ - V_s = 1537V - 340V = 1197V = - $\check{v}$, while

Switch T4 supports
- a forward voltage of $\hat{v}$ = 1537V and
- a reverse voltage of - $\check{v}$ = 1197V.

Thyristor family devices must be used, or devices with a series connected diode, which will increase the converter on-state losses.

vi. At resonance the two freewheel diodes do not conduct.

The rms load current is 153.2 A at 10 kHz, where switch T1 conducts half the cycle and T4 conducts the other half which is the opposite polarity of the cycle. Each switch therefore has an rms current rating of 153.2/√2 = 108.3A rms.

Since both switches conduct the same current shape, each has an average current rating of a half-wave rectified sine of magnitude 216.5A, that is

$$\bar{I}_{T1} = \frac{1}{2\pi}\int_0^{\pi} 216.5\sin\omega t\, dt = \frac{1}{\pi} \times 216.5\text{A}$$
$$= 0.45 \times 216.5/\sqrt{2} = 97.4\text{A}$$

By Kirchhoff's current law, this current value for T1 is also equal to the average dc input current from the supply V_s.

vii. The capacitor has a bipolar voltage and current requirement of ±1537V and ±216.7 A. The rms ratings are therefore ≈1087V rms and 153A rms. A metallised polypropylene capacitor capable of 10kHz ac operation, with a maximum dv/dt rating of approximately ½×(1537+1197)×ω, that is 85.6V/μs, is required.

viii. The dc supply current is the average value of the half-wave rectified sinusoidal load current, which is the average current in T1. That is

$$I_{dc} = 0.45 \times 153.1\text{A rms}$$
$$= 68.9\text{A dc}$$

The rms current in the dc link capacitor is related to the dc input current and switch T1 rms current (as found in part f), by

$$I_c = \sqrt{I_{T1}^2 - I_{dc}^2}$$
$$= \sqrt{108.3^2 - 68.9^2} = 83.6\text{A rms}$$

ix. The load dependant parameters C, ω_o, ω, α, Q, BW, ξ, and half power points remain unchanged.

From equation (14.78) the steady-state current is double that for the asymmetrical bridge,

$$i(\omega t) = \frac{2}{1 - e^{\frac{-\alpha\pi}{\omega}}} \times \frac{V_s}{\omega L} \times e^{-\alpha t} \times \sin\omega t$$
$$= 491 \times e^{-5000t} \times \sin\left(2\pi 10\text{kHz} \times t\right)$$

The peak current is $\hat{i}$ = 433.4A.

The rms load current is 433.4A/√2 = 306.4A rms

From equation (14.79) both the maximum capacitor voltages are

$$\hat{V}_c = V_s \frac{1 + e^{-\alpha\pi/\omega}}{1 - e^{-\alpha\pi/\omega}} = -\check{V}_c$$
$$= 340\text{V} \frac{1 + e^{-0.25}}{1 - e^{-0.25}} = 2734\text{V}$$

The power delivered to the load is four times the asymmetrical case and is

$$P = i_{rms}^2 R = 306.4\text{A}^2 \times 1\Omega = 93.88\text{kW}$$

The average switch current is 194.8A, but the average supply current is four times the asymmetrical case and is 275.5.6A.
For a square wave, the third harmonic is a third the magnitude of the fundamental. From equation (14.83), for operation at the lower half power frequency 9204Hz, (which would result in the larger harmonic component magnitude) $f_3 = 27.6$kHz.

$$v_R\left(\omega_{½}^{-}\right) = ⅓ \times \frac{4V_s}{\pi} \times \frac{1}{\sqrt{1+Q^2\left(\frac{3\omega_{½}^{-}}{\omega_o} - \frac{\omega_o}{3\omega_{½}^{-}}\right)^2}}$$

$$= ⅓ \times \frac{4 \times 340\text{V}}{\pi} \times \frac{1}{\sqrt{1+6.3^2\left(\frac{3 \times 2\pi 9.204k\text{Hz}}{2\pi 10\text{kHz}} - \frac{2\pi 10\text{kHz}}{3 \times 2\pi 9.204k\text{Hz}}\right)^2}}$$

$$= ⅓ \times \frac{4 \times 340\text{V}}{\pi} \times \frac{1}{\sqrt{1+6.3^2\left(\frac{3 \times 9.204}{10} - \frac{10}{3 \times 9.204}\right)^2}}$$

$$= 144.3\text{V} \times 0.066 = 9.53\text{V}$$

The magnitude of the third harmonic current is therefore 9.5V/1Ω = 9.5A or 6.7A rms. The load power at this frequency is 45.1W. This is clearly insignificant compared to the fundament power of 93.88kW being delivered to the 1 Ω load.

♣

14.3.4 Single-switch current source series resonant inverter

The inverter in figure 14.35 is applicable to high Q load circuits such that the output is essentially sinusoidal, with zero average current. Based on the operating mechanisms, a sinusoidal current implies the switch has a 50% duty cycle. The switch turns on and off at zero volts so switch losses are low and the operating frequency can be high. The input inductor L_{large} in conjunction with the input voltage source, during steady state operation, act as a current source input, I_s, for the resonant circuit, such that $V_s I_s$ is equal to the power delivered to the load R.
When the switch T1 is turned on, with zero terminal voltage, it conducts both the constant current I_s and the current i_o resonating in the output circuit, as shown in the circuit waveforms in figure 14.35. The resonating load current builds up. The switch T1, which is in parallel with C_s, is turned off. Current from the switch is diverted to C_s, which charges from an initial voltage of zero. C_s thus forms a turn-off snubber in parallel with T1. The charge on C_s eventually resonates back to zero at which instant the switch is turned on, again, with zero turn-on loss.
The resonant frequency is $\omega_o = 1/\sqrt{L_o C_o}$ and because of the high Q, a small change in the switching frequency significantly decreases the output current, hence output voltage.
As with any current source inverter, the peak switch voltage is in excess of V_s. Since the current is sinusoidal, the average load voltage and inductor voltage are zero. Therefore the average voltage across C_o and C_s is the supply voltage V_s. The peak switch voltage can be estimated to be in excess of V_s /0.45 which is based on a half-wave rectified average sinusoidal voltage.

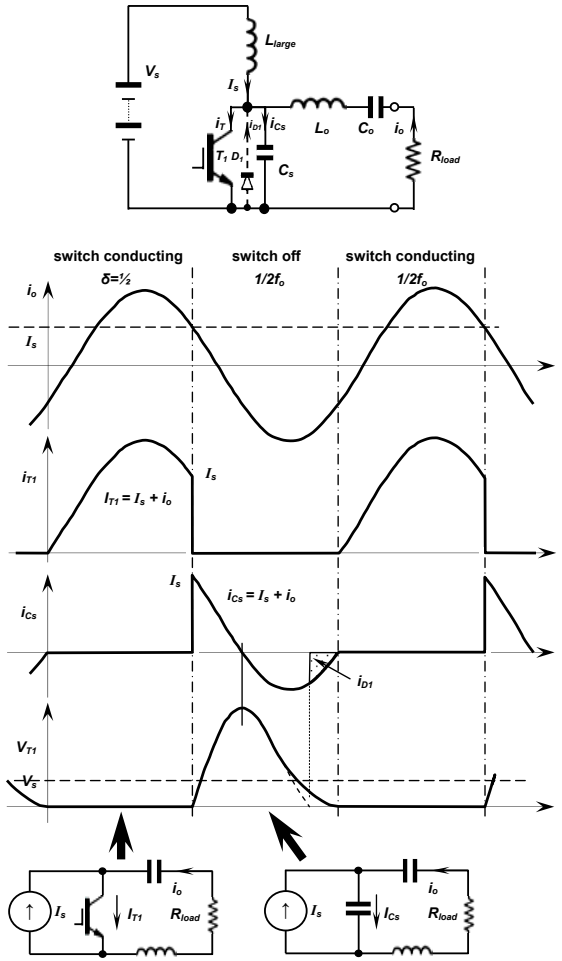

Figure 14.35. *Single-switch, current-source resonant converter circuit and waveforms.*

If the load conditions change and the switch duty cycle is varied from δ = ½, circuit voltages increase and capacitor C_s voltage discharges before the circuit current reaches zero. The capacitor and switch are bypassed with current flowing through the diode D1. This diode prevents the switch from experiencing a negative voltage and the capacitor from charging negatively.
Although such resonant converters offer features such as low switching losses and low radiated EMI, optimal control and performance are difficult to maintain and extremely high circuit voltages occur at low duty cycles.

14.4 Multi-level voltage-source inverters

The conventional three-phase, six-switch dc to ac voltage-source inverter is shown in figure 14.7. Each of the three inverter legs has an output which can provide one of two voltage levels, V_s, when the upper switch (or diode) is on, and 0 when the lower switch (or diode) conducts. The quality of the output waveform is determined by the resolution and switching frequency of the pwm technique used.

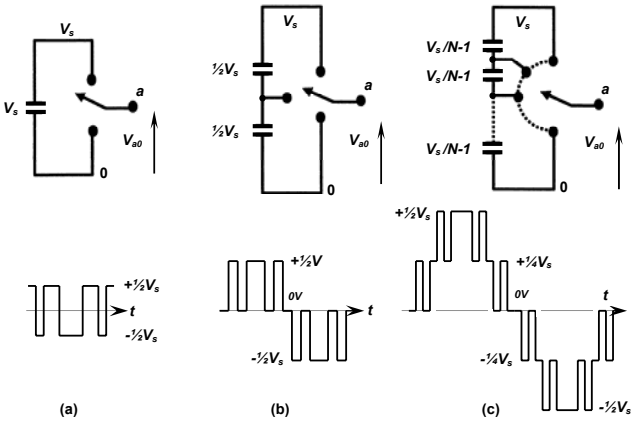

Figure 14.37. *One phase leg of a voltage-source bridge inverter with: (a) two levels; (b) three levels; and (c) N-levels, with N-1 capacitors and waveform for five levels.*

A multilevel inverter (directly or indirectly) divides the dc rail, so that the output of the leg can be more than two levels, as shown in figure 14.37 for a diode clamped multilevel inverter model. In this way, the output quality is improved because both pulse width modulation and amplitude modulation can be used. The output pole is made from more than two series connected switches, so the total dc rail can be the sum of the voltage rating of the individual switches. Very high output voltages can

be achieved, where each device does not experience a voltage in excess of its individual rating.
A multilevel inverter allows higher output voltages with low distortion (due to the use of both pulse width and amplitude modulation) and reduced output *dv/dt*.
There are three main types of multilevel converters

- Diode clamped
- Flying capacitor, and
- Cascaded H-bridge

14.4.1 Diode clamped multilevel inverter

Figure 14.37 shows the basic principle of the diode clamped (or neutral point clamped) multilevel inverter, where only one dc supply, V_s, is used and N is the number levels present in the output voltage between the leg output and the inverter negative terminal, $V_{a\text{-}neg}$. The capacitors split the dc rail voltage into a number of lower voltage levels, each of which can be tapped and connected to the leg output through switches. Only one string of series connected capacitors is used for any number of output phase legs.
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{14.90}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{14.91}$$

The number of capacitors required, independent of the number of phase, is

$$N_{cap} = N - 1 \tag{14.92}$$

while the number of clamping diodes per phase is

$$D_{clamp} = 2(N - 1) \tag{14.93}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{14.94}$$

and the number of switches in each leg is

$$S_n = 2(N - 1) \tag{14.95}$$

The basic three-level inverter is shown in figure 14.38, along with the basic three-level voltage from the leg output to centre tap of the capacitor string, R (neutral point). When switch T_1 is on, its complement T_1' is off, and visa versa. Similarly for the pair of switches T_2 and T_2'. Specifically T_1 and T_2 on give the output $+½V_s$, T_1' and T_2' on give the output $-½V_s$, and T_2 and T_1' on give the output 0. Essential to attaining these output levels, are the clamping diodes D_u and D_l. These two diodes clamp the outer switches to the capacitor string mid-point, which is half the dc rail voltage. In this way, no switch experiences a voltage in excess of half the dc rail voltage. Inner switches must be turned on (or off) before outer switches are turned on (or off).
The five-level inverter uses four capacitors and eight switches in each inverter leg. A set of clamping diodes (three in total for each leg) clamp the complementary switches in each leg. The output is characterised by having five levels, $\pm½V_s$, $\pm¼V_s$, and zero. Some of the clamping diodes experience voltages in excess of that experienced by the main switches. Series connection of some of the clamping

diodes avoids this limitation, but at the expense of increasing the number of clamping diodes from 2× (*N*-1) to (*N*-1)×(*N*-2) per phase. Thus, depending on the diode position in the structure, two diodes have blocking requirements of

$$V_{RB} = \frac{N-1-k}{N-1} V_s \qquad (14.96)$$

where $1 \le k \le N\text{-}2$. These diodes require series connection of diodes, if all devices in the structure are to support $V_s/(N\text{-}1)$. For $N > 2$, capacitor imbalance occurs. The general output voltage, to the centre of the capacitor string is given by

$$V_{an} = \frac{V_s}{N-1}(T_1 + T_2 + .. \quad .. + T_{N-1} - \tfrac{1}{2}(N-1)) \qquad (14.97)$$

Table 14.4. Conduction paths in the diode clamped three-level inverter

V_{out}	On switches	Current path		Active clamping diodes
		$+ i_L$	$- i_L$	
½ V_s	T_1 T_2	T_1 T_2	D_1 D_2	none
0	T_1' T_2	D_{cu} T_2	T_1' D_{cl}	D_{cu} D_{cl}
-½ V_s	T_1' T_2'	T_1' T_2'	D_1' D_2'	none

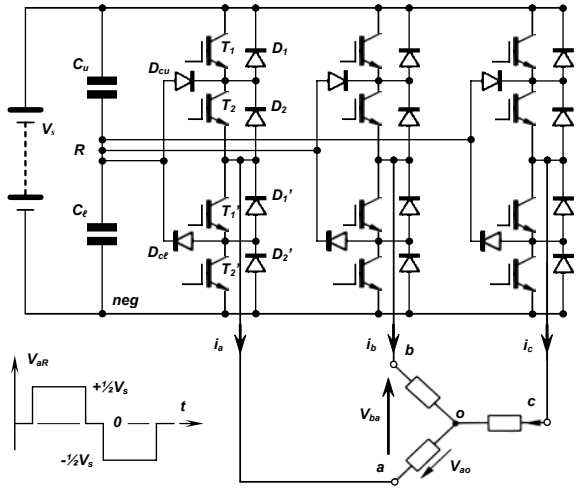

Figure 14.38. *Three-phase, voltage-source, three-level, diode-clamped (NPC) bridge inverter.*

14.4.2 Flying capacitor multilevel inverter

One leg of a fly-capacitor clamped five-level voltage source inverter is shown in figure 14.39, where capacitors are used to clamp the switch voltages to ¼V_s. The available output voltages are ±½V_s, ±¼V_s, and 0, where the output is connected to the dc link (V_s and 0) indirectly via capacitors. Figure 14.39 shows that in general, switches T_n and T_{n+1} connect to capacitor C_n. The configuration offers more available switch states than the clamped diode inverter, and this redundancy allows better, flexible control of capacitor voltages. For example, Table 14.5 shows that there are six states for obtaining 0V output, and four states for each of ±¼V_s. The output states ±½V_s do not involve the capacitors, hence they offer no redundant states. The basic switch restriction is that only one complementary switch (e.g., T_4 or T_4') is on at any time, so as to prevent shorting of a flying capacitor.
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \qquad (14.98)$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \qquad (14.99)$$

The number of capacitors required, which is dependent of the number of phase, is for each phase,

$$N_{cap} = \tfrac{1}{2}(N-1)(N-2) \qquad (14.100)$$

Table 14.5. Five-level flying-capacitor inverter output states (phase A to R)

mode	V_{AR}	switching states				capacitors			paths
		T_1	T_2	T_3	T_4	C_1	C_2	C_3	
1	½V_s	1	1	1	1	=	=	=	½V_s
2	¼V_s	1	1	1	0	=	=	+	½V_s -V_{C3}
N-1 states		1	1	0	1	=	+	-	½V_s -V_{C2}+V_{C3}
		1	0	1	1	+	-	=	½V_s-V_{C1}+V_{C2}
		0	1	1	1	-	=	=	-½V_s+V_{C1}
3	0	1	1	0	0	=	+	=	½V_s -V_{C2}
N^2-4N+1 states		1	0	1	0	+	-	+	½V_s-V_{C1}+V_{C2} -V_{C3}
		0	1	1	0	-	=	+	-½V_s+V_{C1}-V_{C3}
		1	0	0	1	+	=	-	½V_s-V_{C1+}-V_{C3}
		0	1	0	1	-	+	-	-½V_s+V_{C1}-V_{C2}+V_{C3}
		0	0	1	1	=	-	=	-½V_s +V_{C2}
4	-¼V_s	1	0	0	0	+	=	=	½V_s-V_{C1}
N-1 states		0	1	0	0	-	+	=	-½V_s+V_{C1}-V_{C2}
		0	0	1	0	=	-	+	-½V_s -V_{C2} -V_{C3}
		0	0	0	1	=	=	-	-½V_s +V_{C3}
5	-½V_s	0	0	0	0	=	=	=	-½V_s

The number of possible switch states is

$$n_{states} = N^{phases} \tag{14.101}$$

and the number of switches in each leg is

$$S_n = 2(N-1) \tag{14.102}$$

The current output paths in Table 14.5 are made up by the series (and parallel) connection of the flying capacitors through the turn-on of the appropriate switches. Capacitors shown as negative are discharging in the formed path, while those shown as positive are charging. Use of the shown redundant states allows control of the voltage level on all the flying capacitors, while providing the desired output voltages.

A feature of the flying capacitor multilevel inverter is its ride through capability due to the large capacitance used. On the other hand, the capacitors have a high voltage rating and suffer from high current ripple, since they conduct the full load current when connected into an active output voltage state. Capacitor initial charging is also problematic' especially given the capacitors for each leg are independent.

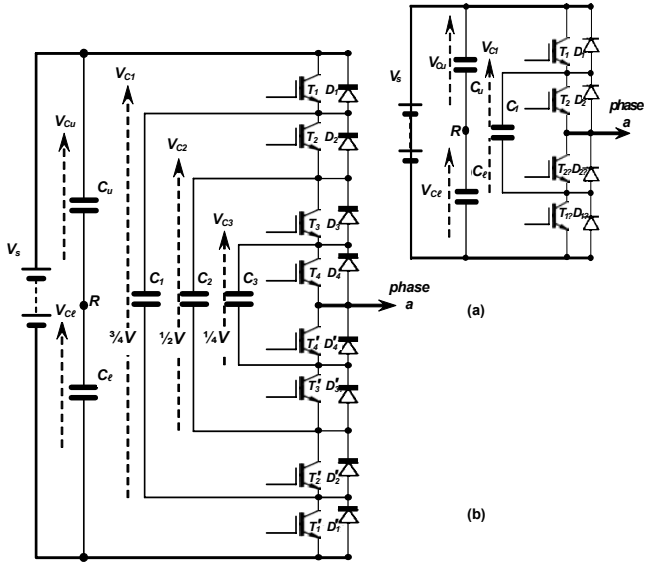

Figure 14.39. *One leg of a voltage-source: (a) three-level and (b) five-level, flying capacitor clamped bridge inverter.*

14.4.3 Cascaded H-bridge multilevel inverter

The *N*-level cascaded H-bridge, multilevel inverter comprises ½(*N*-1) series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source. Three output voltages are possible, $\pm V_s$, and zero, giving a total number of states of $3^{½(N-1)}$, where *N* is odd. Figure 14.40 shows one phase of a seven-level cascaded H-bridge inverter.

The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches.

Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

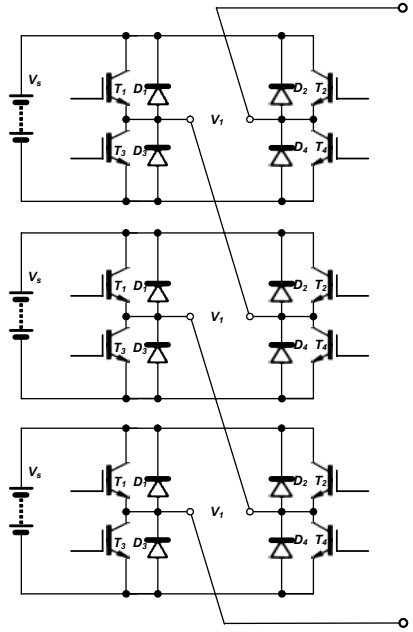

Figure 14.40. *One leg of a voltage-source, seven-level, cascaded H-bridge inverter.*

The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \qquad (14.103)$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \qquad (14.104)$$

The number of capacitors or isolated supplies required per phase is

$$N_{cap} = \tfrac{1}{2}(N - 1) \qquad (14.105)$$

The number of possible switch states is

$$n_{states} = N^{phases} \qquad (14.106)$$

and the number of switches in each leg is

$$S_n = 2(N - 1) \qquad (14.107)$$

Table 14.6. Three output states of H-bridge and their current paths.

V_e	On switches	Bidirectional current paths	
		$+ i_L$	$- i_L$
V_s	T_2 T_3	T_2 T_3	D_2 D_3
0	none	D_4 D_1	D_2 D_3
$-V_s$	T_1 T_4	T_1 T_4	D_2 D_3

A comparison between the three basic multilevel inverters is possible from the numerical summary of component numbers for each inverter, as in Table 14.7. The diode clamped inverter requires many clamping diodes; the flying capacitor inverter requires many independent capacitors; while the cascaded inverter requires many isolated power supplies.

Table 14.7. Multilevel inverter component count, per phase.

Inverter type	levels			switches & diodes	diodes clamping	flying capacitors	Level capacitors	Isolated supplies
	$V_{A\text{-}0V}$	$V_{A\text{-}B}$	$V_{A\text{-}N}$					
diode clamped	*N*	*2N-1*	*4N-3*	*2(N-1)*	*(N-1)(N-2)*	0	*(N-1)*	0
fly capacitor	*N*	*2N-1*	*4N-3*	*2(N-1)*	0	*½(N-1)(N-2)*	*(N-1)*	0
cascade	*N*	*2N-1*	*4N-3*	*2(N-1)*	0	0	*½ (N-1)**	*½(N-1)**

* either / or

14.4.4 PWM for multilevel inverters

Two basic approaches can be used to generate the necessary pwm signal for multilevel inverters. Each approach is based on the extension of a two level equivalent.

- Modulating waveform comparison with offset triangular carriers
- Space vector modulation based on a rotating vector in multilevel space

14.4.4i Multiple offset triangular carriers

Various sinusoidal pwm techniques were considered in section 14.1.3v and 14.1.3vi of this chapter. Figure 14.41 shows how a triangular carrier is associate with each complementary switch pair, four carriers (*N*-1) for the five-level inverter as illustrated. The parts of figure 14.41 show how the four individual carriers can be displaced with respect to one another. The figure also shows how triplen injection is incorporated. The appropriate five-level switch states, as in tables 14.4 to 14.6, can be used to decode the necessary switching sequences. To minimise losses, switching only occurs between adjacent levels.

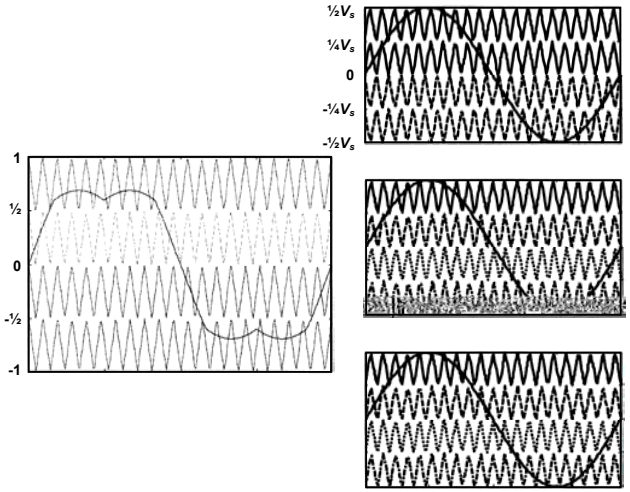

Figure 14.41. *Multi-carrier based pwm generation for one phase of a voltage-source, five-level, inverter.*

14.4.4ii Multilevel rotating voltage space vector

Space vector modulation for the two-level inverter was considered in section 14.1.3vi of this chapter. The basic hexagon shape for two levels is extended to higher levels as shown in figure 14.42, for three levels. The number of triangles, vectors, and states increases rapidly as the level number increases.

Table 14.8. Properties of *N*-level vector spaces

levels	states	triangles	vectors	vectors in each hexagon
N	N^3	$6(N-1)^2$	$3N(N-1)+1$	
2	8	6	7	(1+6)
3	27	24	19	(1+6)+12
5	125	96	61	(1+6)+12+18+24

From table 14.8, the states for the two and three level inverters can be specified as follows.

The 2-level inverter

The zero state matrix is

[000 111]

The first and only hexagon is shown in figure 14.22a.

[100 110 010 011 001 101]

The three level inverter

The zero state matrix is

[000 111 222]

The first hexagon matrix is

$$\begin{bmatrix} 100 & 110 & 010 & 011 & 001 & 101 \\ 211 & 221 & 121 & 122 & 112 & 212 \end{bmatrix}$$

The second hexagon matrix is

[200 210 220 120 020 021 022 012 002 102 202 201]

These pole states are shown figure 14.42.

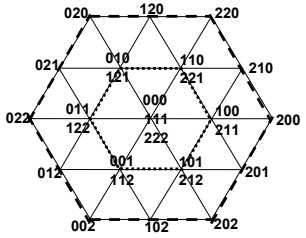

Figure 14.42. *Rotating voltage space vector approached applied to three phases of a voltage-source three-level, inverter.*

A`0´ represents the minimum voltage obtainable from the multilevel converter and *N-1* represents the maximum value. For example, in a two-level converter,`0´ is equivalent to 0V and `1´ is equivalent to $V_s$, where $V_s$ is the converter DC link voltage. In a three-level converter`0´ is equivalent to $-½V_s$,`1´ is equivalent to 0 V, and '2' is equivalent to $½V_s$ where V_s is the link voltage of the multilevel converter.

When the rotating vector is drawn in the vector space, it is decomposed into vectors bordering the triangle it lies in. When operating in the outer hexagon, the vectors states used in the inner most hexagon mean that that level of the converter is operating with a six-step quasi-square output voltage waveform, to which is added a modulated square waveform for the next higher level.

14.5 Reversible converters

Power inversion by phase angle control is attained with a fully controlled single-phase converter as discussed in section 11.3.3. Power regeneration is also possible with the fully controlled three-phase converter shown in figure 11.17. If a fully controlled converter supplies a dc machine, two-quadrant control is possible (QI and QIV), motoring in one direction of rotation and generating in the other direction. Power regeneration into the supply is achieved by reversing the dc output voltage by controlling the converter phase delay angle.

The dual or double converter circuit in figure 14.43a and b will accommodate four-quadrant dc machine operation, where the circuit performs as two fully controlled converters in anti-parallel. Each converter is able to rectify and invert, but because of their inverse parallel connection, one converter (the positive converter P) operates in quadrants QI and QIV, while the other (the negative converter N) operates in quadrants QII and QIII, as shown in figure 14.44.

The two converters can be operated synchronously, called *simultaneous control* or independently where one is always blocking, called *independent control*.

14.5.1 Independent control

Simultaneous converter control can be used if continuous load current can be guaranteed. Only one converter, depending on the quadrant, need operate at anyone time (the other is in a blocking state), as shown in figure 14.43a. No circulating currents arise due to possible mismatched converter output voltages. The continuous current condition may be difficult to ensure at light load levels. Additional series armature inductance, L in figure 14.43a and b, helps with current smoothing and ensuring continuous machine current.

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I, with $0° \le \alpha_1 \le 90°$ for the positive converter P. The negative converter, N, is in the fully blocking state, with all thyristors turned off.
- The positive converter is put into the inverting mode with $90° \le \alpha_1 \le 180°$, changing the average output voltage from positive to negative. The machine current rapidly falls to zero. The machine rotational speed slows, the rate depending on the load inertia.
- After a dead time, the positive converter blocks and the negative converter N starts in a motor braking mode in quadrant II. The motor speed falls rapidly to zero.

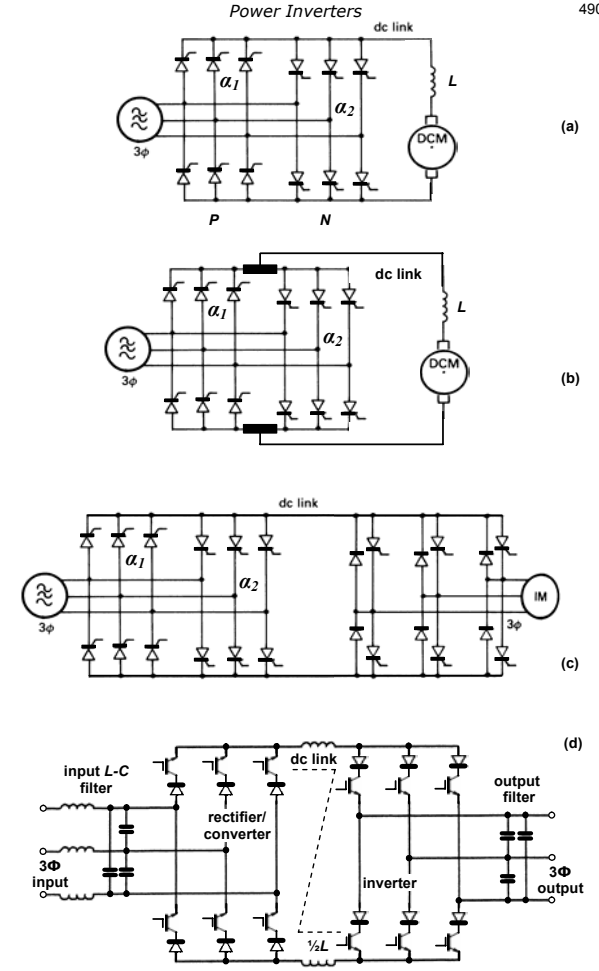

Figure 14.43. *Reversible converter allowing four-quadrant control of: (a) a dc machine with independent converters; (b) a dc machine with simultaneously controlled converters; and (c) voltage and (d) current feed induction machine.*

- The second converter operates in quadrant III and rapidly accelerates the motor in the opposite direction, with $0° \le \alpha_2 \le 90°$.

The dead time before turning on the negative converter N is to ensure the positive converter P is fully off, otherwise the three-phase input voltage lines may short through the converters. Such a current condition cannot be controlled with line-commutated thyristors. Operation is characterised by transitions from QI to QII to QIII for reversal, and transitions from QIII to QIV to QI for returning to the original direction of rotation.

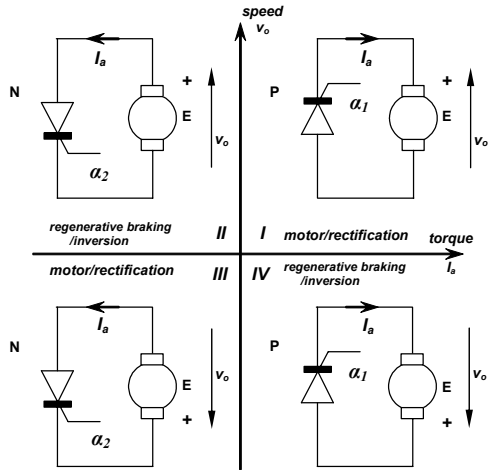

Figure 14.44. *Four quadrants of reversible converter operation.*

14.5.2 Simultaneous control

Simultaneous converter control, also called circulating current control, functions with both converters always in operation which give a faster dynamic response than when the converters are used mutually exclusively. To avoid supply short circuits requires that the output voltage of both converters (rectifier V_r and inverter V_i) be the same in order to minimise circulating currents.

$$\begin{aligned} \overline{V}_r + \overline{V}_i &= 0 \\ V\cos\alpha_1 + V\cos\alpha_2 &= 0 \\ \cos\alpha_1 + \cos\alpha_2 &= 0 \\ \text{that is } \alpha_1 + \alpha_2 &= 180° \end{aligned} \qquad (14.108)$$

As shown in equation (14.108), this implies that both converters operate with firing angles that sum to 180°. Each converter produces the opposite polarity output voltage, which is cancelled by reversing the relative output connections. Under such conditions the load current can be maintained continuous. To minimize any circulating current due to ripple voltage produced by instantaneous voltage difference between the two converters, inductance is usually inserted between each converter and the dc machine load, as shown in figure 14.43b. Adversely the cost and weight are increased, and the supply power factor and drive efficiency are decreased, compared to that obtained with independently controlled converters.

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I for the rectifying, positive converter, with $0° \leq \alpha_1 \leq 90°$. The other converter is operating in the inverting mode with $90° \leq \alpha_2 \leq 180°$, such that $\alpha_1 + \alpha_2 = 180°$. The output voltage for both converters is the same, and the negative converter N carries only the circulating current.
- For rotational direction reversal, $\alpha_1 \geq 90°$ and $\alpha_2 \leq 90°$, such that $\alpha_1 + \alpha_2 = 180°$. The armature back emf voltage now exceeds the converter output voltages, and current diverts to the negative converter N and the machine regeneratively brakes, operating in quadrant II. The current rapidly falls to zero and the positive converter P carries only the ac circulating current.
- The speed rapidly falls to zero, with $\alpha_1 = \alpha_2 = 90°$ giving zero output voltage, so as to control the armature current since the back emf is zero. Then with $\alpha_2 < 90°$ the machine rapidly accelerates in quadrant III, in the reverse direction to the original rotation.

For reversing the direction of rotation from Q III the operation sequence is QIII to QIV to QI. Since no converter dead time is introduced, a fast dynamic response can be attained. A small dc circulating current is deliberately maintained, that is greater in magnitude than the peak of the ac ripple current. The ac current can then flow continuously in both converters, both of which can operate in the continuous conduction mode without the need for continuous converter current reversal operation.

14.5.3 Inverter regeneration

The bridge freewheel diodes of a three-phase inverter restrict the dc rail or dc link voltage from reversing. The dual or double converter circuit in figure 14.43c will allow inversion with a three-phase voltage fed inverter. One converter rectifies, the other converter inverts, functioning as a self-commutated inverter, transferring power from the dc link to the ac supply. Complete four-quadrant control of the three-phase ac machine on the inverter is achieved in conjunction with control of the dc to ac inverter. That is, motor reversal is achieved by effectively interchanging the pwm control signals associated with two phases. The real power flow back into the ac supply is controlled by the converter phase delay angle, while the reactive power flow is controlled by the voltage magnitude. The angle and voltage are not independent. In the case of a pwm controlled inverter fed ac

machine, the ac to dc converter can be uncontrolled, using all diodes, since dc output voltage reversal is not utilised.

Figure 14.43d shows a fully reversible current controlled converter/inverter configuration, using self-commutating devices. The use of self-commutated switches (rather than mains commutated converter thyristors) offers the possibility to minimise the input current distortion and to reduce the inductor size hence improve the dynamic current response. The switch series diodes are essential since the shown IGBTs have no useable reverse blocking capability. The use of reverse blocking GCTs avoids the need for the series blocking diodes, which reduces the on-state voltage losses but increases gate drive complexity. Series connection of devices is necessary above a few kV, and above 1 MVA the GCT dominates.

14.6 Standby inverters and uninterruptible power supplies

Standby inverters and uninterruptible power supplies (ups's) provide a 50/60 Hz supply in the event of an ac mains failure. An ups must provide ac output such that mains failure is undetected by the load. To achieve this, an ups continually feeds the load from an inverter. A load that can tolerate a short interruption of the ac supply is fed from a *standby inverter* which becomes operational within 1-5 ms after the ac supply failure. In communications, computing, and automated production lines, ups's are essential for even brownouts (V and f outside bounds for reliable equipment operation), while in lighting and heating applications, standby inverters are used since a few missing ac cycles (due to a blackout – total interruption of the mains power)) may be tolerated. In each power supply case, the alternative energy source is a standby dc battery. The ups keeps the battery charged when the ac input is supplying the output power.

14.6.1 Single-phase UPS

A basic single-phase UPS is shown in figure 14.45. A key safety objective is to retain the supply neutral at both the supply input and the ac output, without resorting to any from of isolating transformer. Consequently, the input ac mains is half-wave rectified by diodes D_R^+ and D_R^-. Boost converters on the positive and negative groups ensure supply sinusoidal input current and unity power factor. The output H-bridge (T_1-T_4) uses pwm and feedback control to produce a fixed frequency and magnitude output (and ac mains phase synchronisation if required), which is filtered by an *L*-*C* filter. In the event of a loss of the ac supply, the backup batteries, V^+ and V^-, provide energy to the boost converters, hence to the output inverter. The battery backup voltage magnitude is much less than the ac supply magnitude and diodes, D_B^+ and D_B^-, isolate the batteries from the rectified ac supply voltage. The shown ups has two basic limitations that manufactures strive to overt.

- If the battery is to be connected to neutral, then two batteries are necessary. Proprietary attempts using only one battery involve circuit complications and limitations. At best, with one battery, it is one forward biased diode voltage drop from neutral.

- Because the batteries supplies are not isolated during normal operation, during part of the mains cycle near zero voltage, the batteries provide energy. This decreases their lifetime and necessitates more complicated trickle charge circuits. The input current is also distorted at the 0V crossover. Replacement of the blocking diodes D_B by switches involves complexity and battery backup operation requires detection and is not fail safe.

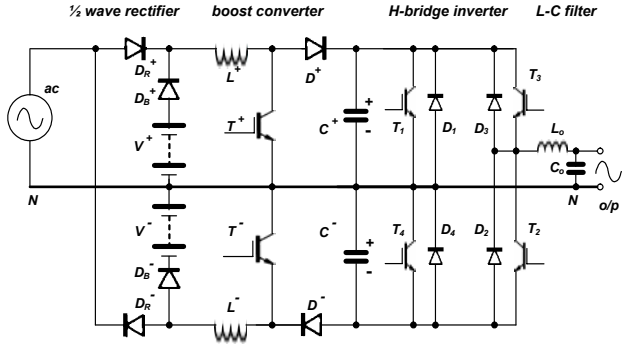

Figure 14.45. *Single-phase uninterruptible power supply.*

14.6.2 Three-phase ups

Figure 14.46 shows a basic three-phase ups, used up to a few tens of kilowatts. The ac supply is rectified and filtered. A forward converter controls the dc link voltage to just above the battery voltage level. This dc voltage is boosted to a dc level such that after inversion it provides the required output voltage magnitude. If the input ac fails or droops, the dc link power is provided by the battery via diode V_B. The output inverter is usually operational in a pwm mode, which allows precise frequency control, voltage control, ac mains phase synchronisation, and mini-misation of low frequency output harmonics. With pwm control minimal filtering is required, which minimises the filter weight, cost, size, and losses. A three-phase ups can utilise third harmonic injection (14.1.4(iv)).
A three-phase boost input converter can be used to maintain sinusoidal ac supply input currents at unity power factor.

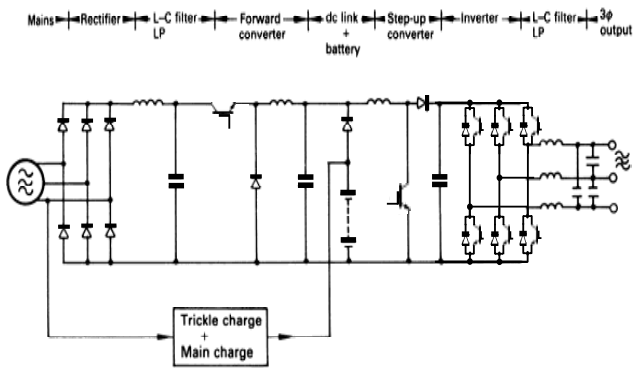

Figure 14.46. *Three-phase uninterruptible power supply.*

14.7 Power filters

Power *L-C* filters are used to reduce harmonics or ripple from

- the rectifier output (dc filter)
- the inverter output (ac filter).

L-C low-pass, second-order filters are shown in figures 14.43, 14.45, and 14.46. In figure 14.46, the *L-C* smoothing filter at the rectifier output, filters the ac mains frequency components leaving dc. The same type of filter is used in the inverter output to filter pwm harmonics, leaving the relative low frequency modulation frequency.
The *L-C* filter fundamental cut-off frequency is dependent on *L, C,* and the load impedance Z_L

$$\frac{v_o}{v_i} = \frac{1}{1 + j\omega L\left(\frac{1}{Z_L} + j\omega C\right)} = \frac{1}{1 - \omega^2 LC + j\frac{\omega L}{Z_L}} \qquad (14.109)$$

The simplest design approach is to assume a non-load condition, $Z_L \to \infty$, whence the filter cut-off frequency is $f_o = 1/\left(2\pi\sqrt{LC}\right)$.
Frequency components below f_o, including dc, are passed. Those components above f_o are attenuated by a second order fall-off in gain. Any frequency components inadvertently around the resonant frequency, f_o, will be amplified. For this reason, the filter may be damped with parallel connected *R-C* snubbers.

Reading list

See chapter 11 reading list.

Problems

14.1. The inverter in figure 14.7 is supplied from a 340 V dc source. The load has a resistance of 10 ohms and an inductance of 10 mH. The basic operating frequency is 50 Hz, with three notches per half cycle giving half the maximum output, similar to that shown in figure 14.13.
Determine the load current waveform over the first two cycles and determine the power delivered to the load based on the current waveform of the final half cycle.

14.2. The inverter and load in problem 14.1 are controlled so as to eliminate the third and fifth harmonics in the output voltage.
Determine the load current waveform over the first two cycles and the power delivered to the load based on the current waveform of the last half cycle.

14.3. Output voltage harmonic reduction can be achieved by employing multi-phase, selected notching modulation control on a three-phase bridge as discussed in 14.1.4. An output as in figure 14.14 with $\alpha = 16.3°$ and $\beta = 22.1°$ eliminates the 5th and 7th harmonics.
Determine the fundamental voltage output component and compare it with that of a square wave. Determine the output rms voltage.

14.4. With the aid of figure 14.11 determine the line-to-neutral and line-to-line output voltage of a dc to three-phase inverter employing 120° device conduction.
Calculate the interphase:

i. mean half-cycle voltage
ii. rms voltage
iii. rms voltage of the fundamental.

14.5. The three-phase inverter bridge in figure 14.4 has a 600 V dc rail and a 10 Ω per phase load. For 180° and 120° conduction calculate:

i. the rms phase current
ii. the power delivered to the load
iii. the switch rms current.

[24.5 A, 18 kW, 17.3 A; 28.3 A, 24 kW, 14.15 A]